TPS7H1301-SP and TPS7H1302-SP 3V to 6.3V Input, 400mA, Radiation-Hardened Charge Pump Voltage Inverter with Integrated Low Dropout Regulator

1 Features

- Total ionizing dose (TID) characterized
  - Radiation hardness assurance (RHA) availability of up to 100krad(Si)
- Single-event effects (SEE) characterized
  - Single-event latchup (SEL), single-event burnout (SEB), and single-event gate rupture (SEGR) immune up to linear energy transfer (LET) = 75MeV·cm^2 /mg
  - Single-event functional interrupt (SEFI) and single-event transient (SET) characterized up to LET = 75MeV·cm^2 /mg
- Inverts a positive input voltage and regulates the negative supply
- Up to 400mA output current
- 2.5Ω (typical) inverter output impedance, V_{IN} = 5V
- ±1.5% regulation output accuracy
- 500kHz (typical) fixed-frequency, adjustable negative output voltage operation (TPS7H1301)
- 1MHz (typical) fixed-frequency, fixed –1.8V output (TPS7H1302)
- 45dB (typical) LDO PSRR at 100kHz with 100mA load current
- Plastic packages outgas tested per ASTM E595
- Available in military (–55°C to 125°C) temp range

2 Applications

- Satellite electrical power systems (EPS)
- Command and data handling (C&DH)
- Optical imaging payload
- Radar imaging payload
- Power for analog circuits
  - Data converters: ADCs and DACs (analog-to-digital and digital-to-analog converters)
  - Op amps (operational amplifiers)
  - Imaging sensors

3 Description

The TPS7H1301 and TPS7H1302 are charge pump positive-to-negative voltage inverters with an integrated negative low dropout regulator (LDO). Both devices accept a positive input supply voltage range of 3V to 6.3V and deliver up to 400mA of output current, with integrated enable and power-good functionality.

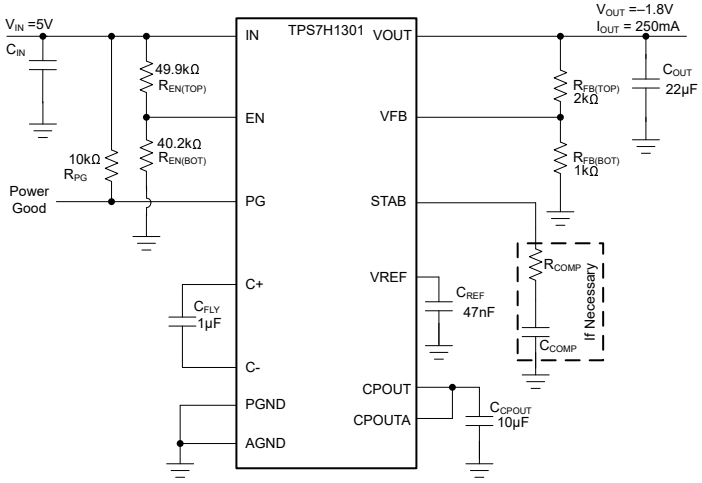
The TPS7H1301 features a 500kHz (typical) charge pump switching frequency and provides adjustable output voltage regulation. Its STAB pin enables direct access to the negative LDO error amplifier for external compensation, offering design flexibility for optimized transient response.

The TPS7H1302 delivers a fixed –1.8V output voltage with a 1MHz (typical) charge pump switching frequency. By eliminating the need for external feedback resistors, the TPS7H1302 reduces both external component count and overall solution size.

Device Information

PART NUMBER (1)	GRADE	PACKAGE (2)
5962R2421501VXC	QMLV-RHA	14-pin ceramic 8.03mm × 9.12mm Mass = 1.22g
5962R2421502VXC (4)		
TPS7H1301HBL/EM	Engineering Sample	
TPS7H1302HBL/EM (4)		
5962R2421501PYE (3)	QMLP-RHA	28-pin plastic 4.40mm × 9.70mm Mass = 198mg
5962R2421502PYE (3)		
TPS7H1301MPWPTSEP (3)	SEP	
TPS7H1302MPWPTSEP (3)		

(1) For additional information view the Device Options Table
(2) Dimension and mass values are nominal.
(3) Product preview.
(4) Advanced information



Typical Application Circuit TPS7H1301

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4 Device Options Table

Generic Part Number	Radiation Rating [1]	Grade	Package	Orderable Part Number
TPS7H1301-SP	TID characterization up to 100 krad(Si) and DSEE free up to LET = 75 MeV·cm^2 /mg	QMLV-RHA	14-pin ceramic flat pack (CFP) HBL	5962R2421501VXC
		QMLP-RHA	28-pin plastic HTSSOP (PWP)	5962R2421501PYE [3]
	None	Engineering Sample [2]	14-pin ceramic flat pack (CFP) HBL	TPS7H1301HBL/EM
TPS7H1302-SP	TID characterization up to 100 krad(Si) and DSEE free up to LET = 75 MeV·cm^2 /mg	QMLV-RHA	14-pin ceramic flat pack (CFP) HBL	5962R2421502VXC [4]
		QMLP-RHA	28-pin plastic HTSSOP (PWP)	5962R2421502PYE [3]
	None	Engineering Sample [2]	14-pin ceramic flat pack (CFP) HBL	TPS7H1302HBL/EM [4]
TPS7H1301-SEP	TID of 50krad(Si) RLAT, DSEE free to 43MeV·cm^2 /mg	Space Enhanced Plastic	28-pin plastic HTSSOP (PWP)	TPS7H1301MPWPTSEP [3]
TPS7H1302-SEP	TID of 50krad(Si) RLAT, DSEE free to 43MeV·cm^2 /mg	Space Enhanced Plastic	28-pin plastic HTSSOP (PWP)	TPS7H1302MPWPTSEP [3]

(1) TID is total ionizing dose, RLAT is radiation lot acceptance testing, and DSEE is destructive single event effects. Additional information is available in the associated TID reports and SEE reports for each product.
(2) These units are intended for engineering evaluation only. The units are processed to a non-compliant flow (such as no burn-in and only 25°C testing). These units are not designed for qualification, production, radiation testing, or flight use. Parts are not warranted as to performance over temperature or operating life.
(3) Product preview
(4) Advanced information

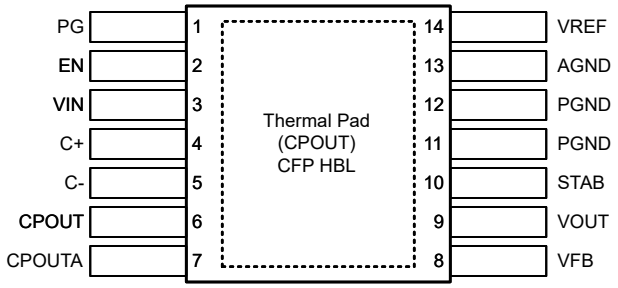
5 Device Comparison Table

Generic Part Number	Charge Pump F_{SW}	Output Voltage Range	External Compensation
TPS7H1301	500kHz	–6V to –0.6V	Yes
TPS7H1302	1000kHz	–1.8V (fixed)	No

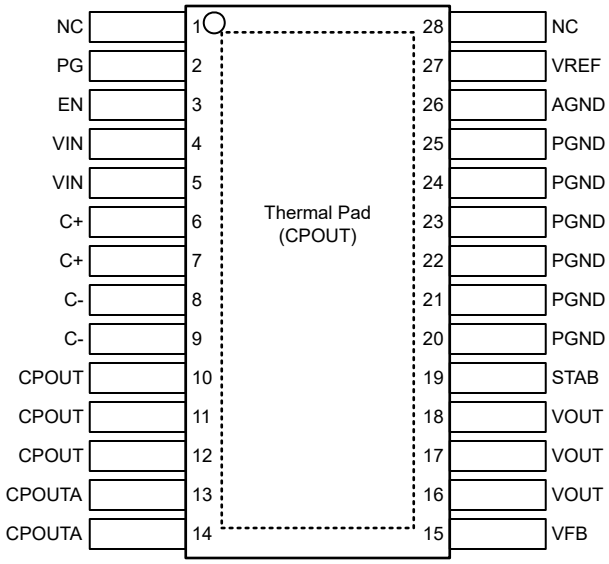
6 Pin Configuration and Functions

TPS7H1301

HBL Package
14-pin CFP
Top View

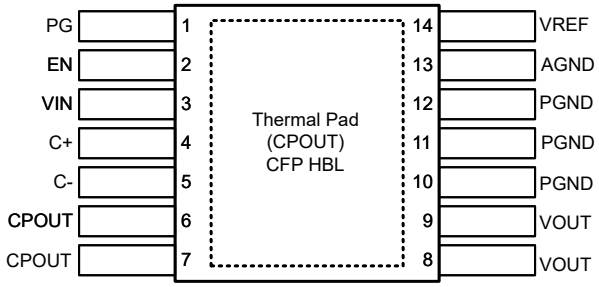


PWP Package
28-pin HTSSOP
Top View



TPS7H1302

HBL Package
14-pin CFP
Top View



PWP Package
28-pin HTSSOP
Top View

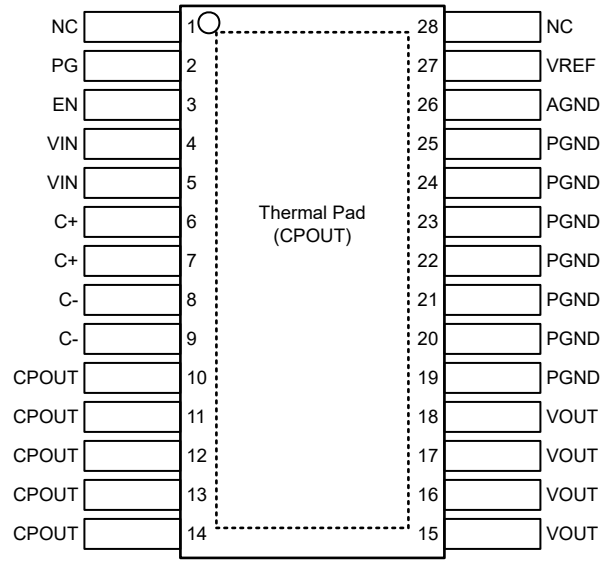


Table 6-1. TPS7H1301 Pin Functions Table

PIN			TYPE[1]	DESCRIPTION
NAME	HBL (14) No.	PWP (28) No.		
PG	1	2	O	Power good indicator. The PG pin is connected to the drain terminal of an internal MOSFET that pulls the applied external voltage to GND when criteria for power good indication is not satisfied. Use a pull-up resistor to pull this pin up to VIN or the desired logic level. When unused, it is recommended to short PG to PGND; the PG pin can be left floating.
EN	2	3	I	Enable. Driving this pin to logic high enables the device; driving the pin to logic low disables the device. If enable functionality is not required, connect this pin to VIN. Do not float this pin.
VIN	3	4,5	P	Positive power supply input; connect a 10µF low-ESR ceramic capacitor to VIN and PGND. Input capacitance larger than 10µF can be used to lessen ripple induced by the charge pump.
C+	4	6,7	P	Positive terminal for flying capacitor, connect a 1µF low-ESR ceramic capacitor to C+ and C-.
C-	5	8,9	P	Negative terminal for flying capacitor, connect a 1µF low-ESR ceramic capacitor to C+ and C-.
CPOUT	6	10 to 12	P	Negative unregulated charge pump output voltage, externally connect to CPOUTA. Connect a 10µF low-ESR ceramic capacitor to the CPOUT - CPOUTA node and PGND
CPOUTA	7	13, 14	P	Negative voltage input for integrated LDO, externally connect to CPOUT. Connect a 10µF low-ESR ceramic capacitor to the CPOUT-CPOUTA node and PGND
VREF	14	27	O	Reference pin, outputs a nominal –0.6V. Connect a 47nF ceramic capacitor between VREF and AGND.
AGND	13	26	P	Analog ground (0V) connection.
PGND	11, 12	20 to 25	P	Power ground (0V) connection for charge pump.
STAB	10	19	O	The STAB pin is directly connected to the output from the internal OTA (operational transconductance) error amplifier to aid in measuring or optimizing the control loop. Standard compensation networks can be applied to the STAB (see Section 10.2.2.6); however, an output capacitance of 22µF typically achieves high stability margins, without the need for an external compensation network.
VOUT	9	16 to 18	P	Output power pin. The regulated output voltage. A single 22µF or two 10µF ceramic capacitora are recommended. Capacitance values between 10µF and 100µF are generally supported; depending on output capacitor, input voltage, output voltage setting and load current, use of the STAB pin can further improve stability performance.
VFB	8	15	I	The output voltage feedback input through voltage dividers. See Section 9.3.5 for guidance on how to adjust the output of the LDO.
NC	N/A	1, 28	—	No connect. These pins are not internally connected. It is recommended to connect these pins to PGND to prevent charge buildup; however, these pins can also be left open or tied to any voltage between CPOUT and V_{IN}.
Thermal pad	—	—	—	Low electrical impedance path to CPOUT. It is recommended to connect the thermal pad to a large plane for effective heat dissipation. This connection can either be an electrical connection to CPOUT, or it can be electrically isolated. The thermal pad is tied internally to CPOUT.
Metal lid	Lid	N/A	—	The lid is internally connected to the thermal pad and CPOUT through the seal ring.

(1) I = Input, O = Output, P = Power, I/O = Input or Output, - = Other

Table 6-2. TPS7H1302 Pin Functions Table

Pin			TYPE[1]	DESCRIPTION
NAME	HBL (14) No.	PWP (28) No.		
PG	1	2	O	Power good indicator. The PG pin is connected to the drain terminal of an internal MOSFET that pulls the applied external voltage to GND when criteria for power good indication is not satisfied. Use a pull-up resistor to pull this pin up to VIN or the desired logic level. When unused, it is recommended to short PG to PGND; the PG pin can be left floating.
EN	2	3	I	Enable. Driving this pin to logic high enables the device; driving the pin to logic low disables the device. If enable functionality is not required, connect this pin to VIN. Do not float this pin.
VIN	3	4,5	P	Positive power supply input; connect a 10µF low-ESR ceramic capacitor to VIN and PGND. Input capacitance larger than 10µF can be used to lessen ripple induced by the charge pump.
C+	4	6,7	P	Positive terminal for flying capacitor, connect a 470nF or two 220nF low-ESR ceramic capacitor to C+ and C-.
C-	5	8,9	P	Negative terminal for flying capacitor.
CPOUT	6	10 to 12	P	Negative unregulated charge pump output voltage, externally connect to CPOUTA. Connect 4.7µF or two 2.2µF low-ESR ceramic capacitor to the CPOUT-CPOUTA node and PGND
CPOUTA	7	13, 14	P	Negative voltage input for integrated LDO, externally connect to CPOUT. Connect a 4.7µF or two 2.2µF low-ESR ceramic capacitor to the CPOUT-CPOUTA node and PGND
VREF	14	27	O	Reference pin, outputs a nominal –0.6V. Connect a 47nF ceramic capacitor between VREF and AGND.
AGND	13	26	P	Analog ground (0V) connection.
PGND	10 to 12	19 to 25	P	Power ground (0V) connection for charge pump.
VOUT	8, 9	15 to 18	P	Output power pin; regulated output voltage is –1.8V (typ). A single 22µF or two 10µF ceramic capacitors are recommended. Capacitance values between 10µF and 100µF are generally supported.
NC	N/A	1, 28	—	No connect. These pins are not internally connected. It is recommended to connect these pins to PGND to prevent charge buildup; however, these pins can also be left open or tied to any voltage between CPOUT and V_{IN}.
Thermal pad	—	—	—	Internally connected to CPOUT. It is recommended to connect the thermal pad to a large plane for effective heat dissipation. This connection can either be an electrical connection to CPOUT, or it can be electrically isolated. The thermal pad is tied internally to CPOUT.
Metal lid	Lid	N/A	—	The lid is internally connected to the thermal pad and CPOUT through the seal ring.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input Voltage	VIN	–0.3	7.5	V
	EN	–0.3	7.5	
	PG	–0.3	7.5	
	VFB (TPS7H1301 only)	–7.5	0.3	
	CPOUTA	–6.8	0.3	
Output Voltage	VREF	–3.6	0.3	V
	STAB (TPS7H1301 only)	CPOUT	CPOUT +7.5	
	C+	GND-0.3	VIN	
	C-	CPOUT	GND+0.3	
	CPOUT	–6.8	0.3	
	VOUT	–6.8	0.3	
Input Current	IN	0	600	mA
Output Current	OUT	0	600	mA
T_{STG}	Storage temperature	–65	150	°C
T_J	Junction temperature	–55	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±1000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	±250	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input Voltage	VIN	3		6.3	V
	EN	0		7	
	PG	0		7	
	CPOUTA(1) (3)	–6.3		–2	
Output Voltage	VOUT (TPS7H1301)	–6		–0.6	V
	CPOUT(1) (3)	–6.3		–2	
	VOUT (TPS7H1302)(2)		–1.8		
I_{OUT}	Output Current	0		400	mA
T_J	Junction temperature	–55		125	°C

(1) Selection of capacitors for CFLY and CPOUT affect overall charge pump resistance, voltage droop, and overall voltage present on CPOUT; see the Application Section for droop voltage calculation equation.
(2) See accuracy specification in the Electrical Characteristics Table for the TPS7H1302's V_{OUT} operating bounds.
(3) $V_{CPOUT(min)}$ represents the minimum charge pump output voltage magnitude required to maintain regulation at –1.8V output with 75mA load current.

7.4 Thermal Information

THERMAL METRIC(1)		TPS7H1301-SP TPS7H1302-SP	TPS7H1301-SP, SEP TPS7H1302-SP, SEP	UNIT
		CFP HBL	PWP (HTSSOP)	
		14	28	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	25.1	24.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	6.3	15.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.3	6.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.4	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	9.1	6.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.5	0.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

7.5 Electrical Characteristics

Over 3V ≤ V_{IN} ≤ 6.3V, $V_{OUT\ (set)}$ = –1.8V (TPS7H1302 fixed; TPS7H1301 set via $R_{FB(TOP)}$ = 2kΩ, $R_{FB(BOT)}$ = 1kΩ), I_{OUT} = 10mA, C_{REF} = 47nF, over operating temperature range (T_A = –55℃ to 125℃). Typical values are at T_A = 25℃, unless otherwise noted; includes RLAT at T_A = 25℃ if sub-group number is present for QML RHA and SEP devices[1].

PARAMETER		TEST CONDITIONS	SUB-GROUP	MIN	TYP	MAX	UNIT
POWER SUPPLIES and CURRENTS							
V_{UVLOR}	Input supply UVLO rising				2.7		V
V_{UVLOF}	Input supply UVLO falling				2.53		
$V_{UVLO(HYS)}$	Input supply UVLO Hysteresis				220		mV
I_Q	Quiescent Current	TPS7H1301 IOUT = 0A, V_{EN} = 7V	1, 2, 3		15	45	mA
		TPS7H1302[2] IOUT = 0A, V_{EN} = 7V	1, 2, 3		12	45	
I_{SHDN}	Shutdown Current	V_{EN} = 0V, I_{OUT} = 0A	1, 2, 3		0.8	1.5	mA
I_{FB}	Feedback leakage current	TPS7H1301 V_{FB} = –0.6V	1, 2, 3		25	100	nA
ENABLE							
$V_{EN(rising)}$	Enable rising threshold (turn-on)		1, 2, 3	0.57	0.6	0.625	V
$V_{EN(falling)}$	Enable falling threshold (turn-off)		1, 2, 3	0.445	0.5	0.555	V
$t_{EN(delay)}$	EN propagation delay	EN high to PG high at: VIN = 5V, VOUT = –1.8V	1, 2, 3		14	18	ms
$I_{EN(LKG)}$	Enable leakage current	V_{EN} = 7V	1, 2, 3		25	330	nA
$T_{SD(enter)}$	Thermal shutdown enter temperature				160		℃
$T_{SD(exit)}$	Thermal shutdown exit temperature				130		℃
POWER GOOD							
$V_{PG(rise)}$	Power good rising threshold as a percent of V_{OUT}	Slew rate V_{OUT} = 10V/s	1, 2, 3	91.8%	94.8%	98.05%	
$V_{PG(fall)}$	Power good falling threshold as a percent of V_{OUT}	Slew rate V_{OUT} = 10V/s	1, 2, 3	86.25%	90%	94.1%	
$V_{PG(OL)}$	Power good output low	$I_{PG(SINK)}$ = 2mA	1, 2, 3		90	190	mV
$V_{IN(MIN\_PG)}$	Minimum V_{IN} for valid PG (V_{PG} = 0.5V)	$I_{PG(sink)}$ = 0.5mA	1, 2, 3		0.8	1	V
$I_{PG(LKG)}$	Power good leakage	TPS7H1301 V_{PG} = 7V, V_{FB} = –0.6V TPS7H1302 V_{PG} = 7V, V_{OUT} = –1.8V	1, 2, 3		0.05	2	µA

7.5 Electrical Characteristics (continued)

Over 3V ≤ V_{IN} ≤ 6.3V, $V_{OUT\ (set)}$ = –1.8V (TPS7H1302 fixed; TPS7H1301 set via $R_{FB(TOP)}$ = 2kΩ, $R_{FB(BOT)}$ = 1kΩ), I_{OUT} = 10mA, C_{REF} = 47nF, over operating temperature range (T_A = –55℃ to 125℃). Typical values are at T_A = 25℃, unless otherwise noted; includes RLAT at T_A = 25℃ if sub-group number is present for QML RHA and SEP devices(1).

PARAMETER		TEST CONDITIONS			SUB-GROUP	MIN	TYP	MAX	UNIT
CHARGE PUMP									
$R_{DISCHARGE}$	CPOUT discharge resistance	C_{CPOUT} = 10µF	V_{CPOUT} = –0.3V				75		Ω
$t_{DISCHARGE}$	CPOUT discharge time (CPOUT = –0.3V) to GND	C_{CPOUT} = 10µF					6.5		ms
f_{SW}	Switching frequency (TPS7H1301)				9, 10, 11	400	500	600	kHz
f_{SW}	Switching frequency (TPS7H1302)(2)				9, 10, 11	800	1000	1200	kHz
$f_{SW(FB)}$	Foldback mode switching frequency (TPS7H1301)						125		kHz
$f_{SW(FB)}$	Foldback mode switching frequency (TPS7H1302)(2)						250		kHz
$R_{DS(ON1)}$	Switch array MOSFET1 drain source resistance	I_{RDSON} = 100mA, V_{IN} = 5V			1, 2, 3		300	480	mΩ
$R_{DS(ON2)}$	Switch array MOSFET2 drain source resistance						175	345	
$R_{DS(ON3)}$	Switch array MOSFET3 drain source resistance						235	300	
$R_{DS(ON4)}$	Switch array MOSFET4 drain source resistance						220	370	
$R_{CP(OUT)}$	Output resistance to CPOUT (TPS7H1301)	C_{FLY} = 1µF, C_{CPOUT} = 10µF, C_{OUT} = 22µF	I_L = 150mA	V_{IN} = 3V			4.5		Ω
			I_L = 250mA	V_{IN} = 5V			3.5		
				V_{IN} = 6.3V			3.1		
$R_{CP(OUT)}$	Output resistance to CPOUT (TPS7H1302)(2)	C_{FLY} = 0.47µF, C_{CPOUT} = 4.7µF, C_{OUT} = 22µF	I_L = 150mA	V_{IN} = 3V			4.8		Ω
			I_L = 250mA	V_{IN} = 5V			3.7		
				V_{IN} = 6.3V			3.3		
V_{DROOP}	Droop Voltage V_{DROOP} = VIN – $\lvert V_{CPOUT}\rvert$ (TPS7H1301)	C_{FLY} = 1µF, C_{CPOUT} = 10µF, C_{OUT} = 22µF	V_{IN} = 3V(4)	I_{OUT} = 10mA			135		mV
				I_{OUT} = 250mA			1260		
			V_{IN} = 5V	I_{OUT} = 10mA			105		
				I_{OUT} = 400mA			1400		
			V_{IN} = 6.3V	I_{OUT} = 10mA			93		
				I_{OUT} = 400mA			1240		
V_{DROOP}	Droop Voltage V_{DROOP} = VIN – $\lvert V_{CPOUT}\rvert$ (TPS7H1302)(2)	C_{FLY} = 0.47µF, C_{CPOUT} = 4.7µF, C_{OUT} = 22µF	V_{IN} = 3V(4)	I_{OUT} = 10mA			144		mV
				I_{OUT} = 250mA			1344		
			V_{IN} = 5V	I_{OUT} = 10mA			111		
				I_{OUT} = 400mA			1591		
			V_{IN} = 6.3V	I_{OUT} = 10mA			100		
				I_{OUT} = 400mA			1420		

7.5 Electrical Characteristics (continued)

Over 3V ≤ V_{IN} ≤ 6.3V, $V_{OUT\ (set)}$ = –1.8V (TPS7H1302 fixed; TPS7H1301 set via $R_{FB(TOP)}$ = 2kΩ, $R_{FB(BOT)}$ = 1kΩ), I_{OUT} = 10mA, C_{REF} = 47nF, over operating temperature range (T_A = –55℃ to 125℃). Typical values are at T_A = 25℃, unless otherwise noted; includes RLAT at T_A = 25℃ if sub-group number is present for QML RHA and SEP devices(1).

PARAMETER		TEST CONDITIONS		SUB-GROUP	MIN	TYP	MAX	UNIT
DROPOUT								
I_{DO}	Dropout current (TPS7H1301)(3)	$V_{OUT(set)}$ = –1.8V $I_{OUT(meas.)}$ = 98% × $V_{OUT(NOM)}$	V_{IN} = 3V	1, 2, 3	75	125		mA
			V_{IN} = 3.3V	1, 2, 3	100	150		
			V_{IN} = 4V	1, 2, 3	200	300		
			V_{IN} = 5V	1, 2, 3	400			
			V_{IN} = 6V	1, 2, 3	400			
		$V_{OUT(set)}$ = –5V $I_{OUT(meas.)}$ = 98% × $V_{OUT(NOM)}$	V_{IN} = 5.5V	1, 2, 3	40	50		
			V_{IN} = 6.3V	1, 2, 3	250	300		
	Dropout current (TPS7H1302)(3) (2)	$V_{OUT(set)}$ = –1.8V $I_{OUT(meas.)}$ = 98% × $V_{OUT(NOM)}$	V_{IN} = 3V	1, 2, 3	75	125		
			V_{IN} = 3.3V	1, 2, 3	100	150		
			V_{IN} = 4V	1, 2, 3	200	300		
		$V_{OUT(set)}$ = –1.8V $I_{OUT(meas.)}$ = 97% × $V_{OUT(NOM)}$	V_{IN} = 5V	1, 2, 3	400			
			V_{IN} = 6V	1, 2, 3	400			
ACCURACY								
V_{ACC}	Output voltage accuracy (TPS7H1301)	–5V ≤ V_{OUT} ≤ $V_{CP(OUT)}$ - V_{DO} 1mA ≤ I_{OUT} ≤ 400mA		1, 2, 3	–1.5%		1.5%	
V_{ACC}	Output voltage accuracy (TPS7H1302)(2)	1mA ≤ I_{OUT} ≤ 250mA		1, 2, 3	–1.5%		1.5%	
		400mA		1, 2, 3	–1.5%		2%	
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation	3.3V ≤ V_{IN} ≤ 6.3V	ΔV = 3V I_{OUT} = 150mA	1, 2, 3		100	1300	µV/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation (TPS7H1301)	10mA ≤ I_{OUT} ≤400mA V_{IN} = 5V, V_{OUT} = –1.8V		1, 2, 3		8	35	mV/A
	Load regulation (TPS7H1302)(2)	10mA ≤ I_{OUT} ≤400mA V_{IN} = 5V, V_{OUT} = –1.8V		1, 2, 3		24	90	mV/A
V_{REF}	Internal reference voltage	(TPS7H1301)		1, 2, 3	–0.609	–0.600	–0.591	V
		(TPS7H1302)		1, 2, 3	–0.610	–0.600	–0.593	
STABILITY								
GM	Gain margin (TPS7H1301)	V_{IN} = 5V, V_{OUT} = –1.8V, I_{OUT} = 250mA, C_{OUT} = 22µF, C_{FLY} = 1µF, $C_{P(OUT)}$ = 10µF T_A = 25℃, No external compensation				31		dB
PM	Phase margin (TPS7H1301)	V_{IN} = 5V, V_{OUT} = –1.8V, I_{OUT} = 250mA, C_{OUT} = 22µF, C_{FLY} = 1µF, $C_{P(OUT)}$ = 10µF T_A = 25℃, No external compensation				58		°

7.5 Electrical Characteristics (continued)

Over 3V ≤ V_{IN} ≤ 6.3V, $V_{OUT\ (set)}$ = –1.8V (TPS7H1302 fixed; TPS7H1301 set via $R_{FB(TOP)}$ = 2kΩ, $R_{FB(BOT)}$ = 1kΩ), I_{OUT} = 10mA, C_{REF} = 47nF, over operating temperature range (T_A = –55℃ to 125℃). Typical values are at T_A = 25℃, unless otherwise noted; includes RLAT at T_A = 25℃ if sub-group number is present for QML RHA and SEP devices(1).

PARAMETER		TEST CONDITIONS		SUB-GROUP	MIN	TYP	MAX	UNIT
RIPPLE, NOISE AND PSRR								
$PSRR_{LDO}$	LDO power-supply rejection ratio	V_{CPOUT} = –5V, V_{OUT} = –1.8V, I_{OUT} = 250mA	f_{ripple} = 100Hz			60		dB
			f_{ripple} = 1kHz			58		dB
			f_{ripple} = 10kHz			47		dB
			f_{ripple} = 100kHz			45		dB
			f_{ripple} = 500kHz			26		dB
			f_{ripple} = 1MHz			26		dB
$V_{RIP(CP)}$	Voltage ripple at charge pump (BW < 2Mhz)	I_{OUT} = 400mA, V_{IN} = 5V, V_{OUT} = –1.8V				120		mV_{PP}
$V_{RIP(OUT)}$	Voltage ripple at device output (BW < 2Mhz)	I_{OUT} = 400mA, V_{IN} = 5V, V_{OUT} = –1.8V				3		mV_{PP}
V_{N_OUT}	Output noise voltage (bandwidth from 10Hz to 100kHz)	V_{IN}= 5V, V_{OUT} = –1.8V, I_{OUT} = 250mA				20		μV_{RMS}

(1) See the 5962R2421501 SMD for additional information on the QML RHA devices and see the VID for additional information on the SEP devices.
(2) Advanced Information
(3) See Parameter Measurement Information
(4) There is no inherent charge pump current limitation at V_{IN} = 3V, output current is characterized to 250mA to accommodate LDO headroom at –1.8V.

7.6 Quality Conformance Inspection

MIL-STD-883, Method 5005 - Group A

SUBGROUP	DESCRIPTION	TEMP (°C)
1	Static tests at	25
2	Static tests at	125
3	Static tests at	–55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	–55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	–55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	–55

7.7 Typical Characteristics

V_{IN} = 5V, V_{OUT} = –1.8V, T_A= 25ºC ,C_{REF} = 47nF, C_{FLY} = 1µF, C_{CPOUT} = 10µF and C_{OUT} = 22µF, no R_{COMP}, no C_{COMP} unless otherwise noted.

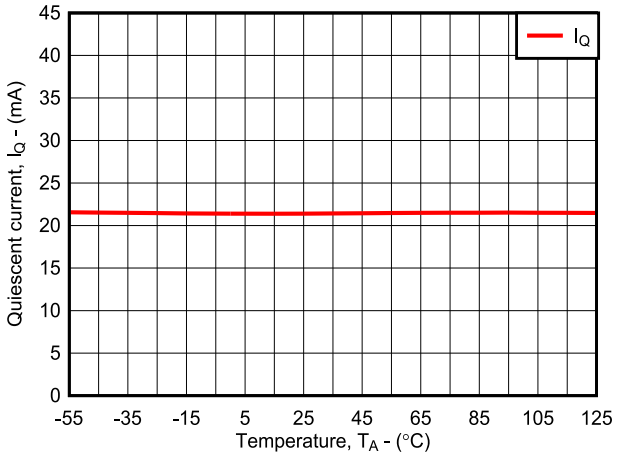


Figure 7-1. Quiescent Current vs. Temperature - TPS7H1301

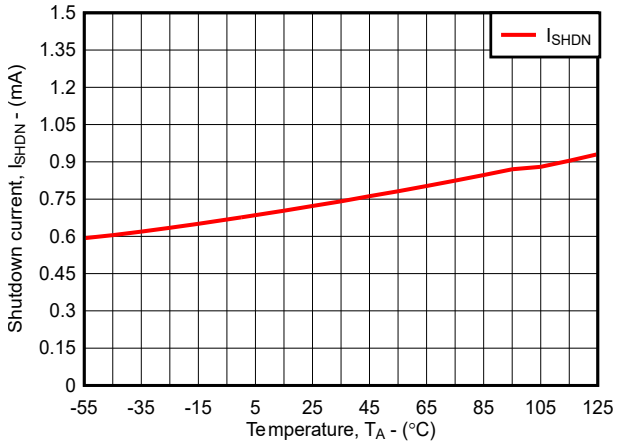


Figure 7-2. Shutdown Current vs. Temperature - TPS7H1301

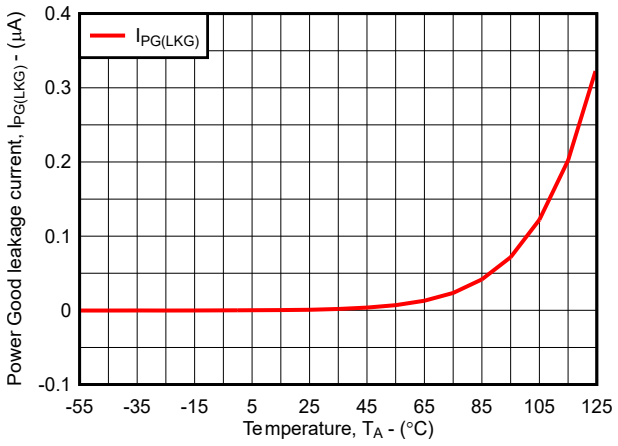


Figure 7-3. Power Good Leakage Current vs. Temperature

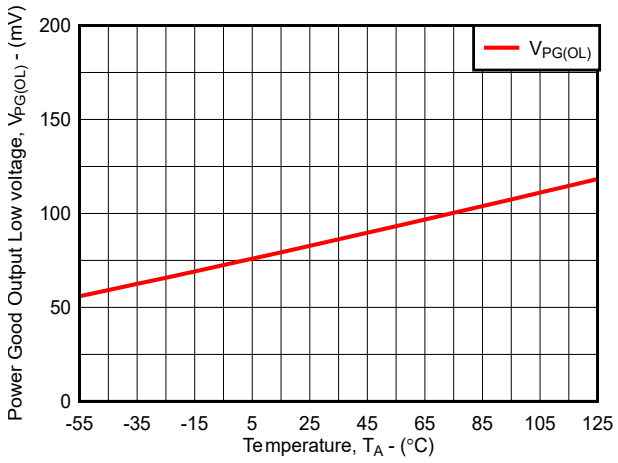


Figure 7-4. Power Good Output Low vs. Temperature

7.7 Typical Characteristics (continued)

V_{IN} = 5V, V_{OUT} = –1.8V, T_A= 25ºC ,C_{REF} = 47nF, C_{FLY} = 1µF, C_{CPOUT} = 10µF and C_{OUT} = 22µF, no R_{COMP}, no C_{COMP} unless otherwise noted.

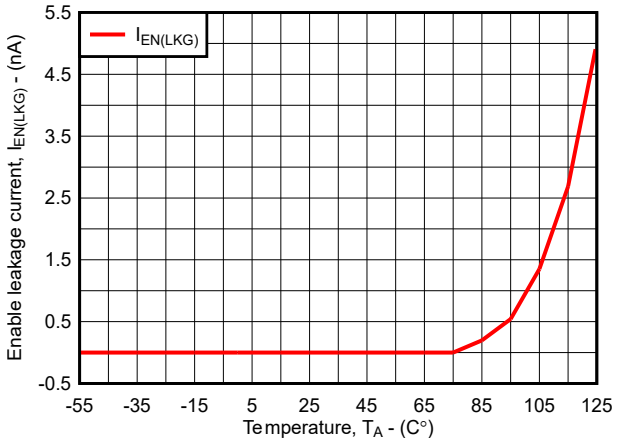


Figure 7-5. Enable Leakage vs Temperature

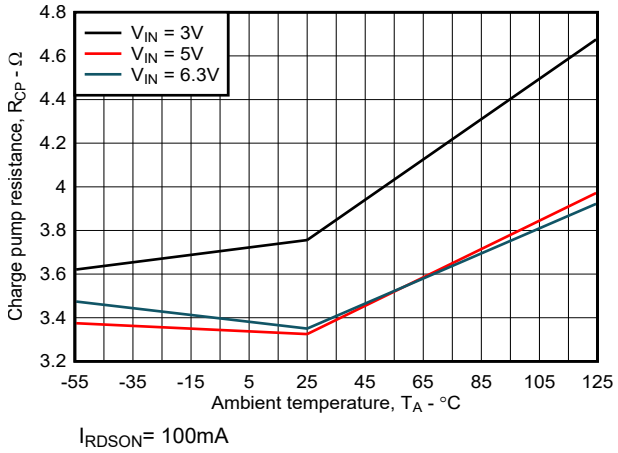


Figure 7-6. Charge pump resistance, R_{CP} vs Temperature

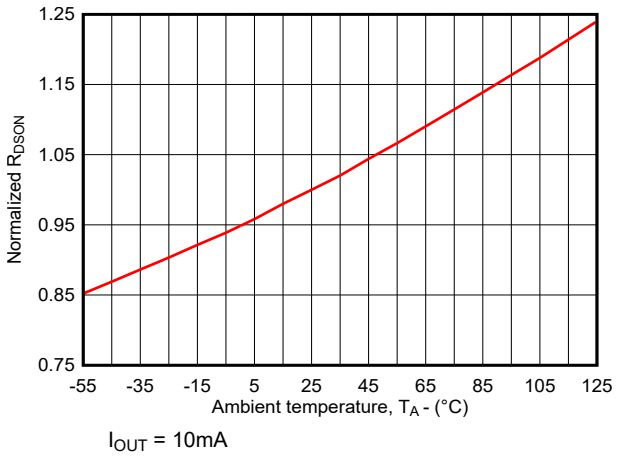


Figure 7-7. Normalized R_{DSON} vs Temperature

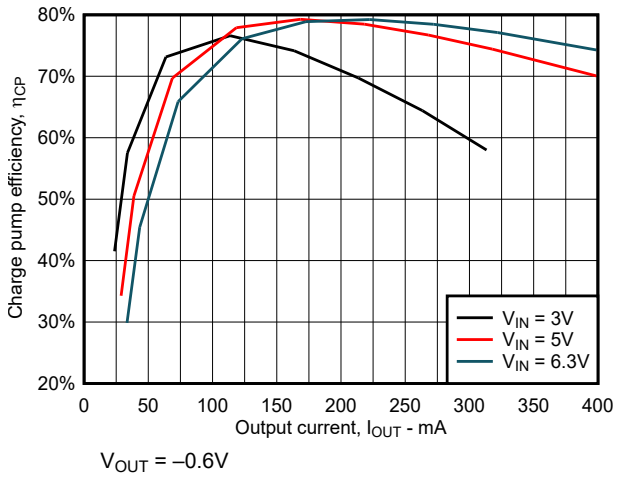


Figure 7-8. Charge Pump Efficiency (TPS7H1301)

7.7 Typical Characteristics (continued)

V_{IN} = 5V, V_{OUT} = –1.8V, T_A= 25ºC ,C_{REF} = 47nF, C_{FLY} = 1µF, C_{CPOUT} = 10µF and C_{OUT} = 22µF, no R_{COMP}, no C_{COMP} unless otherwise noted.

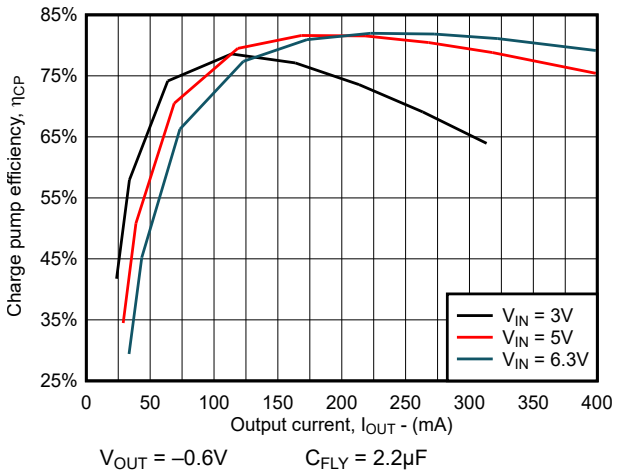


Figure 7-9. Charge Pump Efficiency (TPS7H1301)

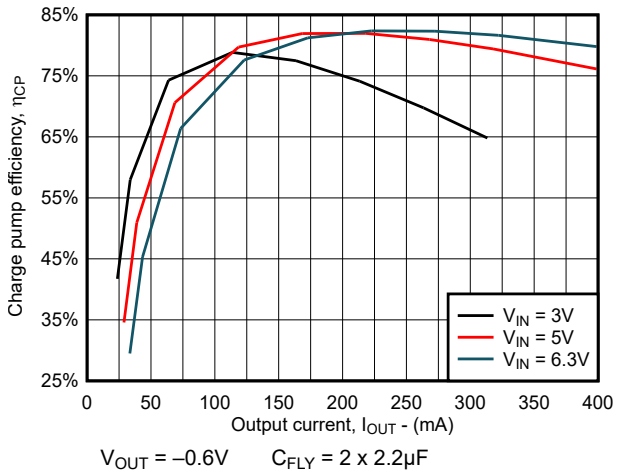


Figure 7-10. Charge Pump Efficiency (TPS7H1301)

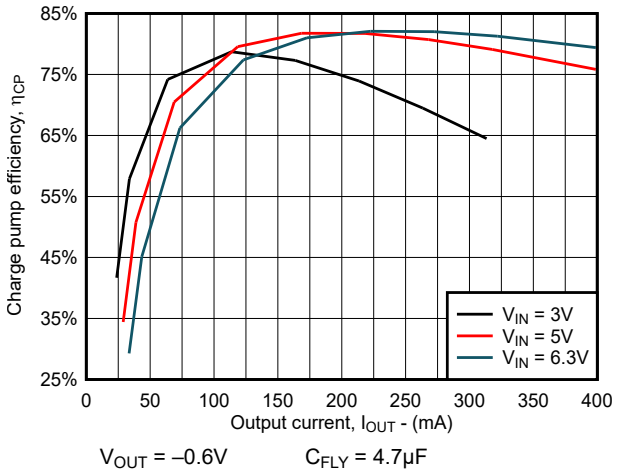


Figure 7-11. Charge Pump Efficiency (TPS7H1301)

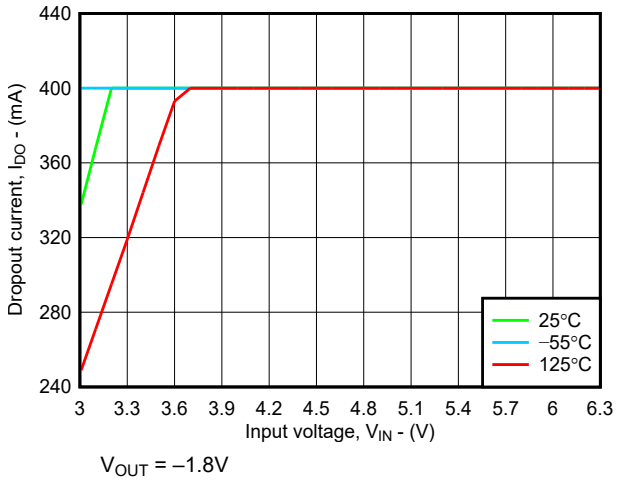


Figure 7-12. Dropout Current vs Input Voltage (TPS7H1301)

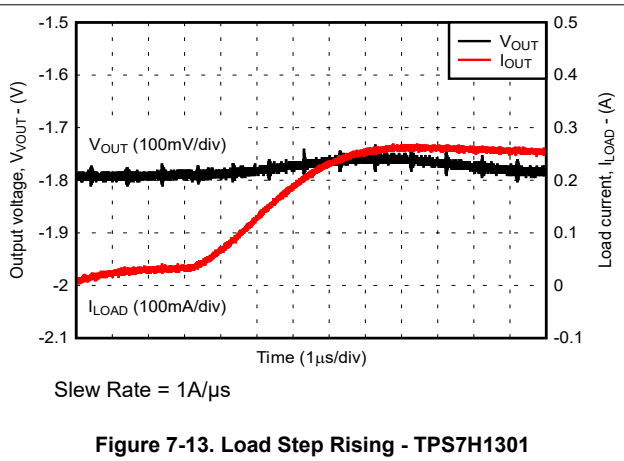


Figure 7-13. Load Step Rising - TPS7H1301

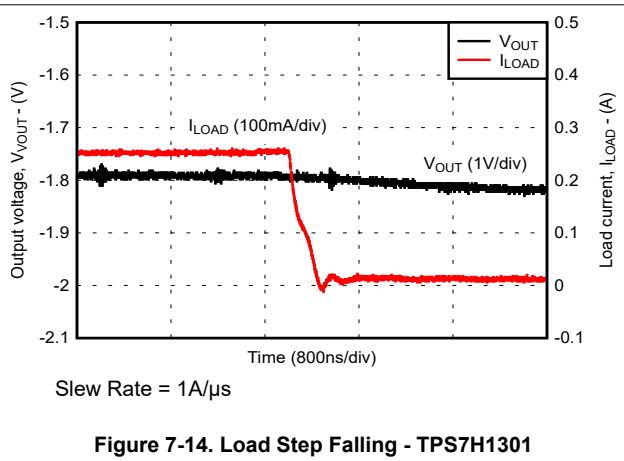
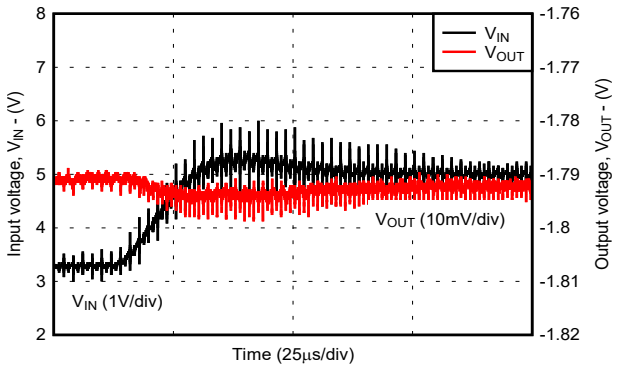


Figure 7-14. Load Step Falling - TPS7H1301

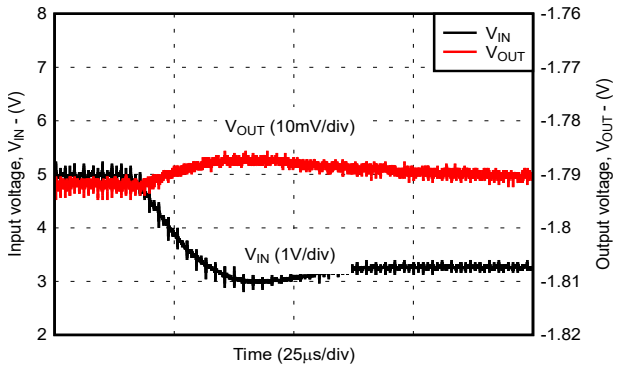
7.7 Typical Characteristics (continued)

V_{IN} = 5V, V_{OUT} = –1.8V, T_A= 25ºC ,C_{REF} = 47nF, C_{FLY} = 1µF, C_{CPOUT} = 10µF and C_{OUT} = 22µF, no R_{COMP}, no C_{COMP} unless otherwise noted.



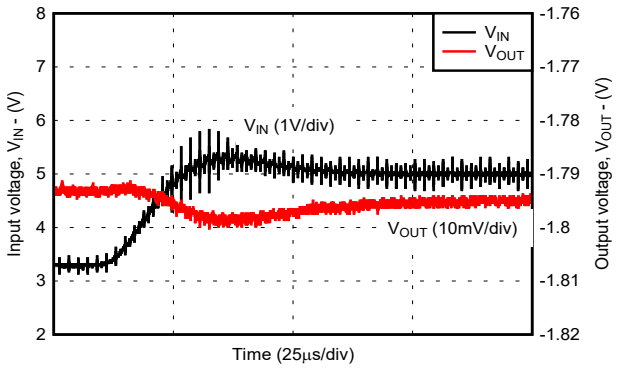
Slew Rate = 10V/ms I_{LOAD}=250mA

Figure 7-15. Line Step Rising - TPS7H1301



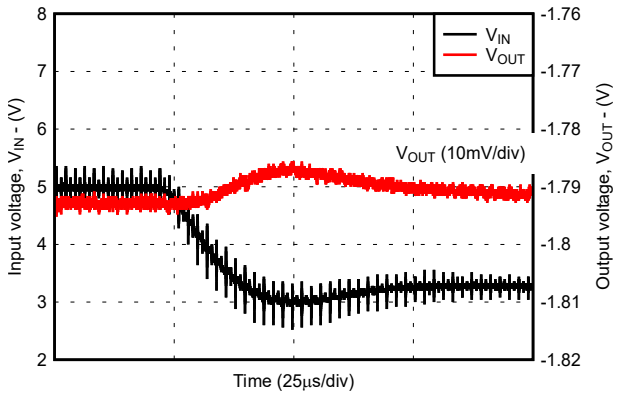
Slew Rate = 10V/ms I_{LOAD}=250mA

Figure 7-16. Line Step Falling - TPS7H1301



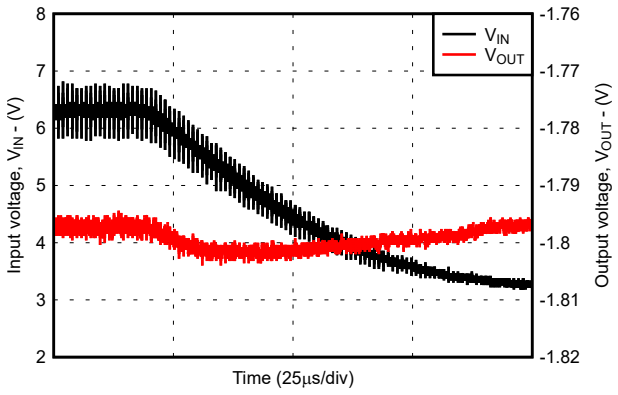
Slew Rate = 10V/ms I_{LOAD}=10mA

Figure 7-17. Line Step Rising - TPS7H1301



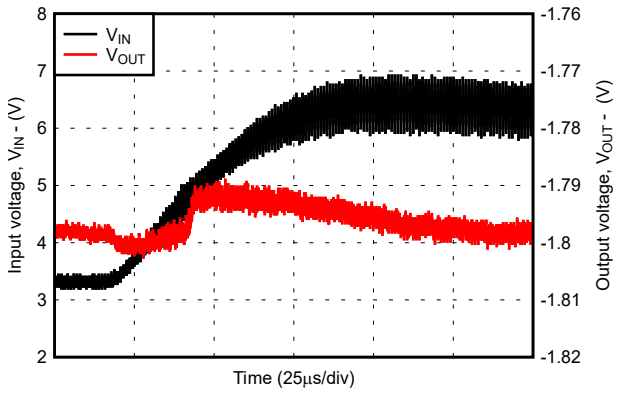
Slew Rate = 10V/ms I_{LOAD}=10mA

Figure 7-18. Line Step Falling - TPS7H1301



Slew Rate = 10V/ms I_{LOAD}=250mA C_{FLY}=470nF C_{CPOUT}=4.7µF

Figure 7-19. Line Step Falling - TPS7H1302

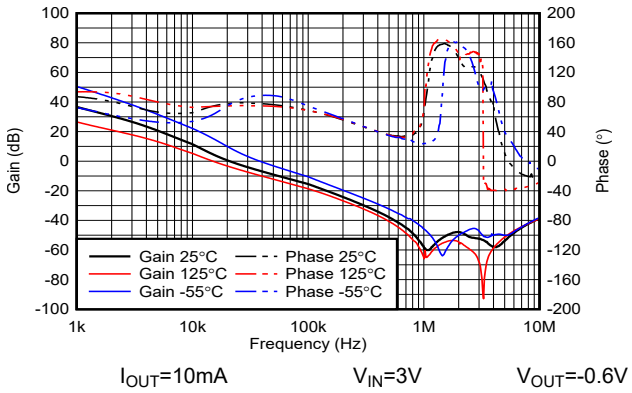


Slew Rate = 10V/ms I_{LOAD}=250mA C_{FLY}=470nF C_{CPOUT}=4.7µF

Figure 7-20. Line Step Rising - TPS7H1302

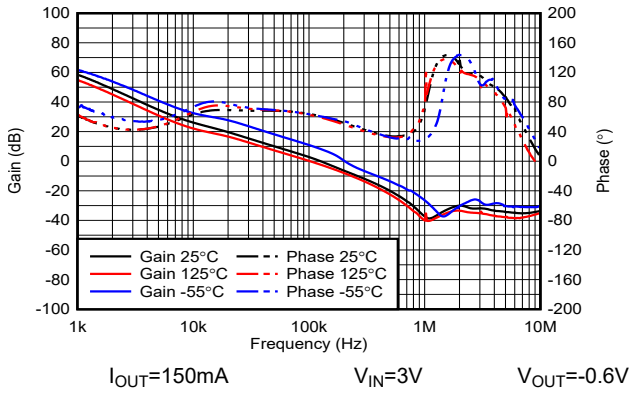
7.7 Typical Characteristics (continued)

V_{IN} = 5V, V_{OUT} = –1.8V, T_A= 25ºC ,C_{REF} = 47nF, C_{FLY} = 1µF, C_{CPOUT} = 10µF and C_{OUT} = 22µF, no R_{COMP}, no C_{COMP} unless otherwise noted.



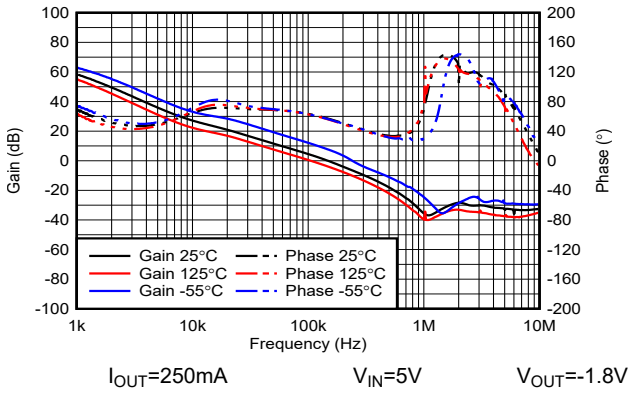
I_{OUT}=10mA V_{IN}=3V V_{OUT}=-0.6V

Figure 7-21. Gain and Phase vs Frequency (Bode) - TPS7H1301



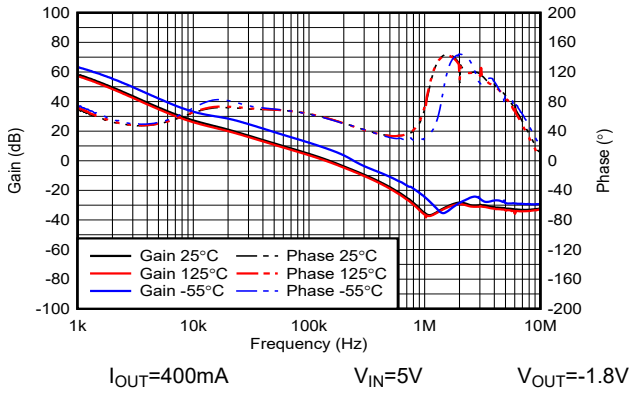
I_{OUT}=150mA V_{IN}=3V V_{OUT}=-0.6V

Figure 7-22. Gain and Phase vs Frequency (Bode) - TPS7H1301



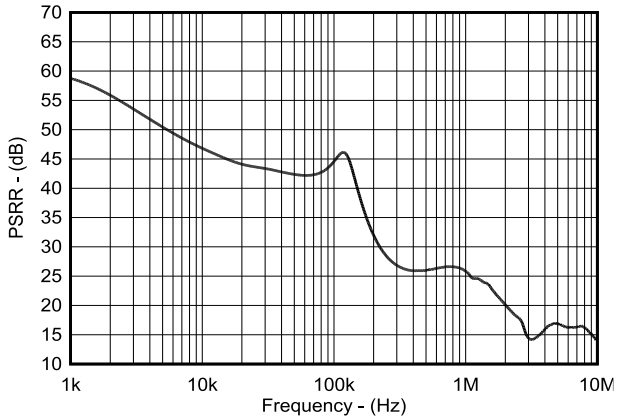
I_{OUT}=250mA V_{IN}=5V V_{OUT}=-1.8V

Figure 7-23. Gain and Phase vs Frequency (Bode) - TPS7H1301



I_{OUT}=400mA V_{IN}=5V V_{OUT}=-1.8V

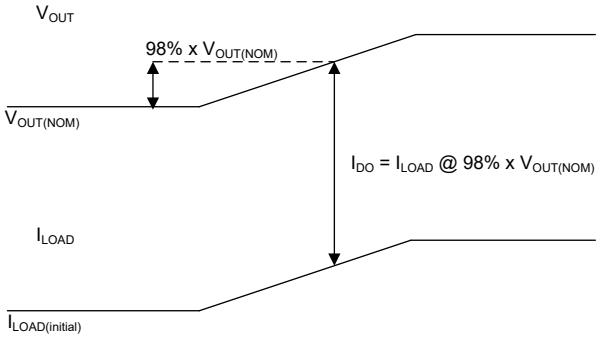
Figure 7-24. Gain and Phase vs Frequency (Bode) - TPS7H1301



V_{IN} = 5V V_{CPOUT} = –5V V_{OUT} = –1.8V
I_{OUT} = 250mA

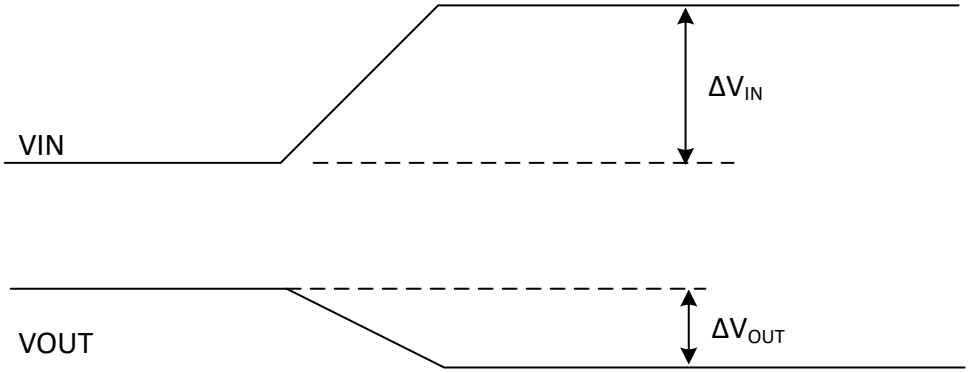
Figure 7-25. PSRR vs Frequency

8 Parameter Measurement Information



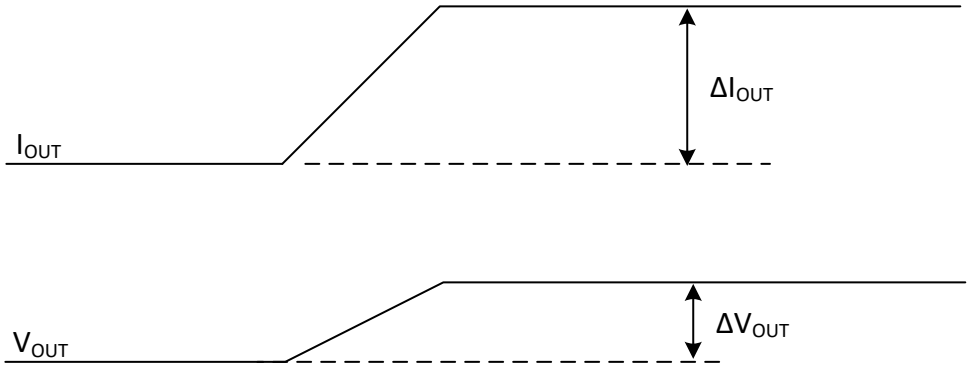
A. $V_{OUT(NOM)}$ is the measured output voltage. V_{LIM} is the specified percentage of output voltage permitted to rise above the specified $V_{OUT(NOM)}$. I_{load} is the load current applied on V_{OUT}. When V_{OUT} falls to 98% of the nominal value ($V_{OUT(NOM)}$), the dropout current is recorded.

Figure 8-1. Dropout Current Measurement



A. Line regulation ΔV_{OUT} / ΔV_{IN} = 100µV/V (typ). For example a 1V change in V_{IN} (ΔV_{IN} = 1V), results in a 100µV change in V_{OUT} (ΔV_{OUT} = 100µV). Line regulation is a DC parameter; therefore this waveform can only be considered valid after transients die out or for a slow V_{IN} slew rate.

Figure 8-2. Line Regulation Measurement



A. Load regulation: ΔV_{OUT} / ΔI_{OUT} = 8mV/A (typ). For example a 100mA change in I_{OUT} (ΔI_{OUT} = 100mA), results in a 0.8mV (typ TPS7H1301) change in V_{OUT} (ΔV_{OUT} = 0.8mV). Load regulation is a DC parameter; therefore this waveform can be considered valid after transients die out or for a slow I_{OUT} slew rate.

Figure 8-3. Load Regulation Measurement

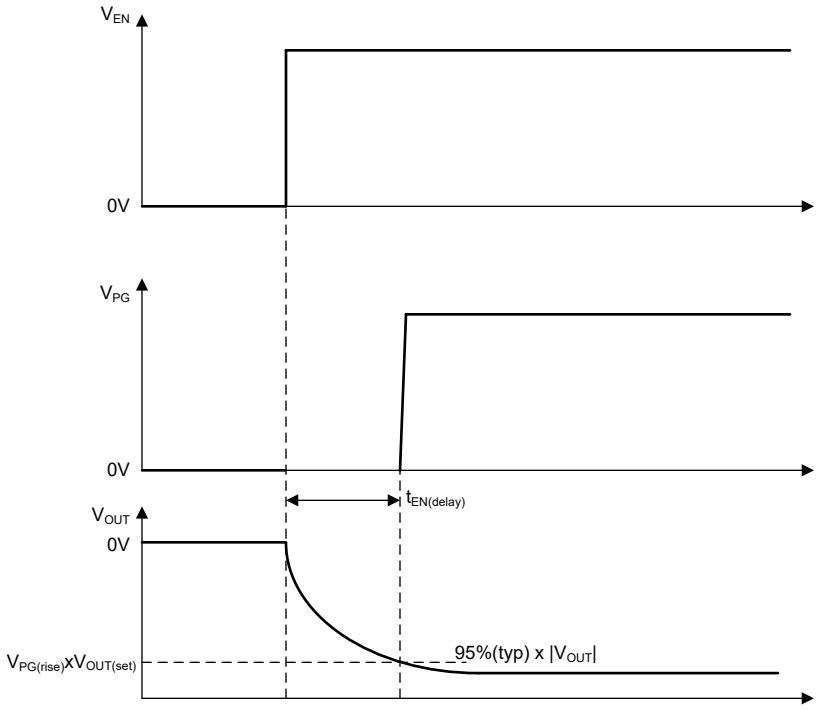


Figure 8-4. Enable Power Good Timing Measurement

9 Detailed Description

9.1 Overview

The TPS7H1301 (adjustable output) and TPS7H1302 (fixed output) generate a precision negative regulated voltage by integrating a low dropout (LDO) regulator with an inverting charge pump. This architecture enables in situ negative voltage generation without requiring auxiliary negative supplies from the satellite bus or bulky inverting buck-boost converters, making the TPS7H1301 and TPS7H1302 well suited for negative voltage applications requiring up to 400mA of load current. LDO regulation of the charge pump output (V_{CPOUT}) enables dropout-free operation for input voltages, V_{IN} greater than 5V, while reducing output voltage ripple.

TPS7H1301 (Adjustable Output) The TPS7H1301 provides access to the error amplifier output via the STAB pin for external compensation if needed. The device is internally compensated to typically achieve at least 6dB gain margin and 50° phase margin, without utilizing external compensation. The charge pump operates at 500kHz and is optimized for use with a 1µF ceramic flying capacitor (C_{FLY}) and a 10µF charge pump output capacitor (C_{CPOUT}). The output voltage is easily programmed from –6V to –0.6V with ±1.5% accuracy using external feedback resistors connected to the VFB pin.

TPS7H1302 (Fixed Output) The TPS7H1302 provides a fixed –1.8V output, ±1.5% accuracy using internal feedback resistors; which eliminates external voltage-setting resistors and reduces component count. The charge pump operates at 1MHz, enabling a more compact implementation with reduced capacitor values: 0.47µF for C_{FLY} and 4.7µF for C_{CPOUT}. The higher switching frequency and integrated feedback network provide a space-efficient implementation with robust stability.

9.2 Functional Block Diagram

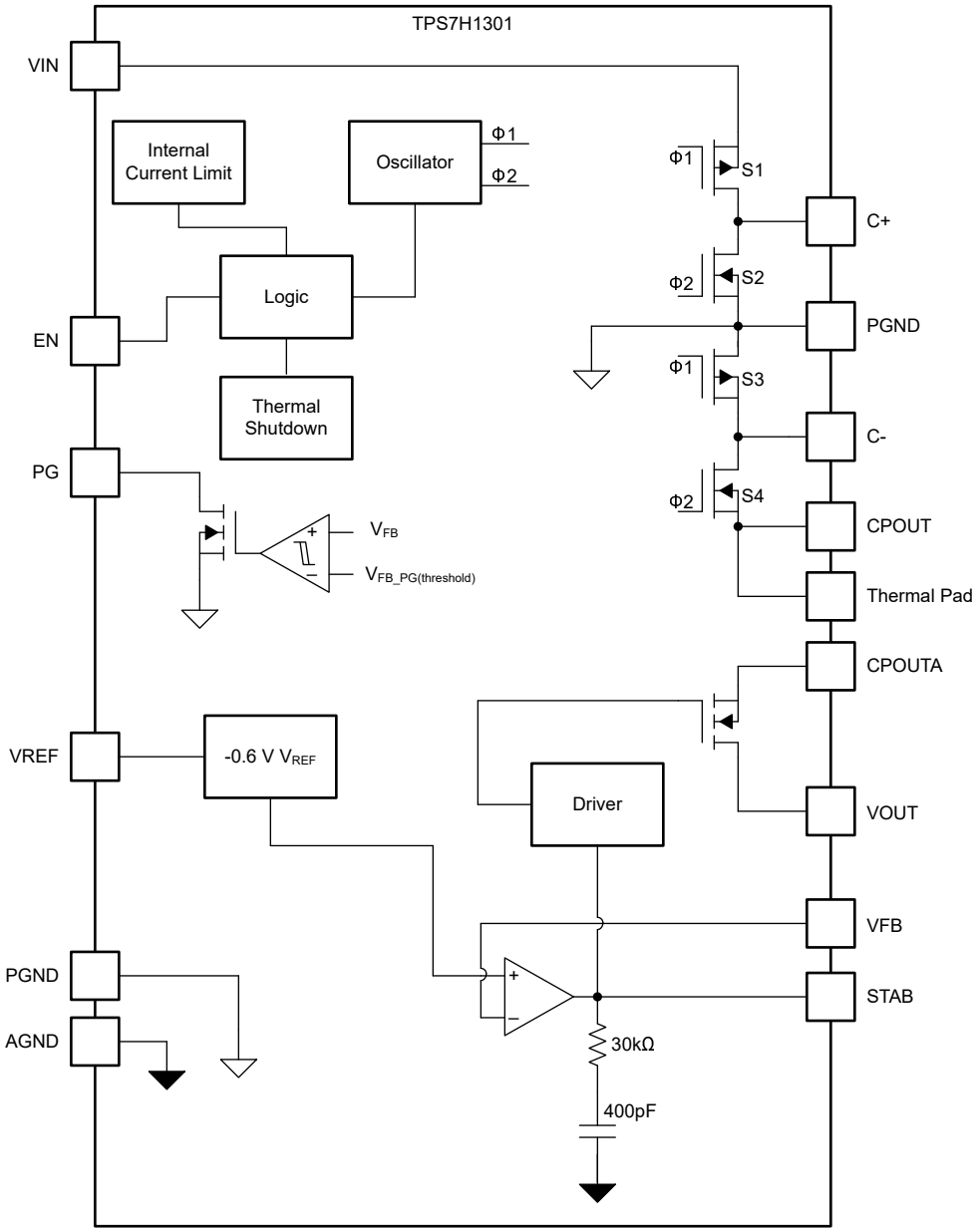


Figure 9-1. TPS7H1301 Functional Block Diagram

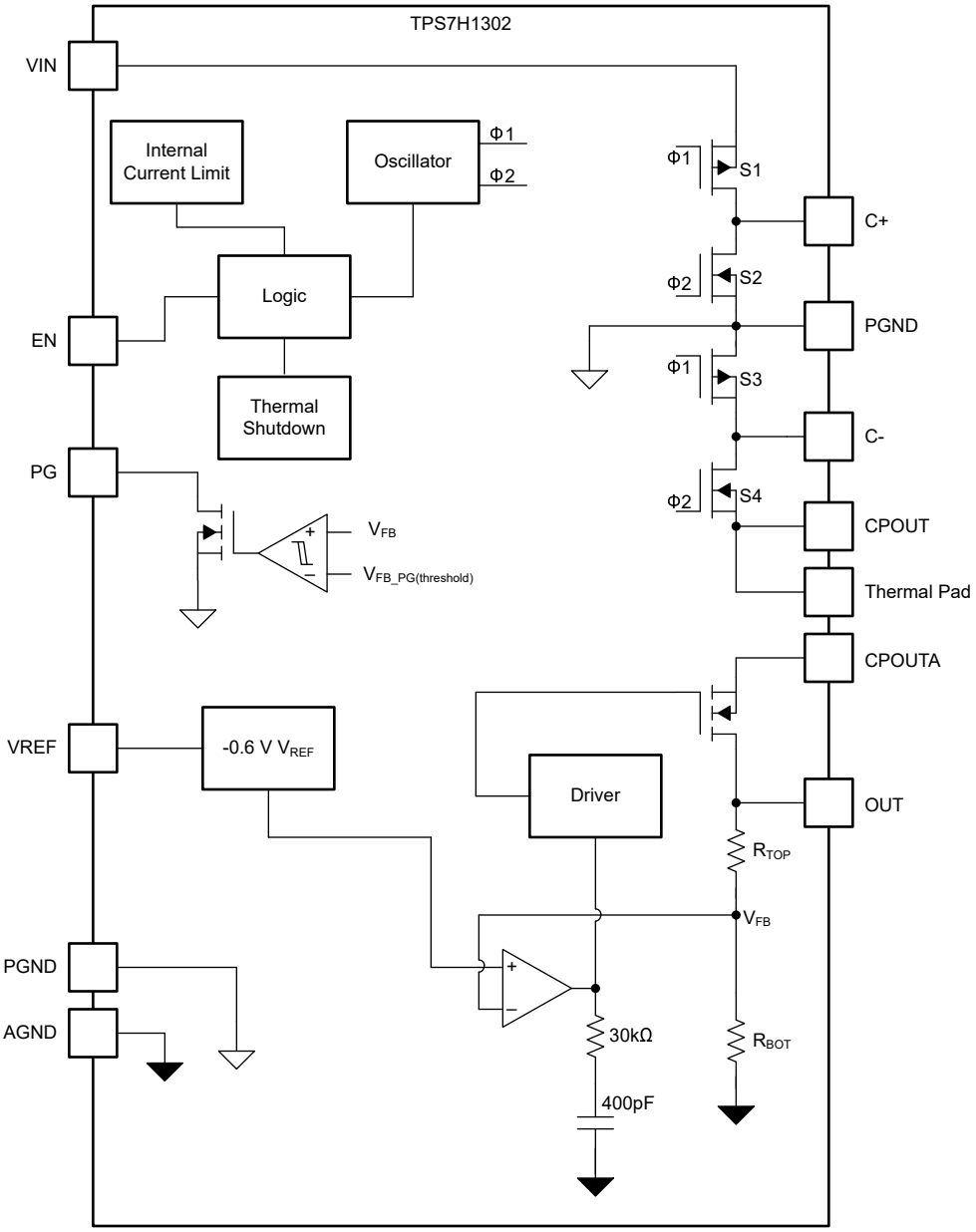


Figure 9-2. TPS7H1302 Functional Block Diagram

9.3 Feature Description

9.3.1 Enable

When the enable pin is low, the device enters shutdown mode and does not regulate the output voltage. Normally, an external resistor divider from VIN to GND is used to drive the EN pin.

The input voltage has a typical UVLO rising voltage of 2.7V and a UVLO falling voltage of 2.53V.

Connection of the Enable pin directly to V_{IN} is possible; refer to Equation 1 for resistor sizing guidance at the desired turn-on voltage.

$$V_{IN(rising)} = V_{EN(rising)} \times (R_{EN(TOP)} + R_{EN(BOT)}) / R_{EN(BOT)} \quad (1)$$

Similarly, a VIN(falling) voltage can also be calculated using Equation 2. The $V_{IN(rising)}$ and $V_{IN(falling)}$ can be thought of as configurable UVLO (undervoltage lockout) thresholds.

$$V_{IN(falling)} = V_{EN(falling)} \times (R_{EN(TOP)} + R_{EN(BOT)}) / R_{EN(BOT)} \quad (2)$$

While the TPS7H1301 and TPS7H1302 commence turn on at a V_{EN} voltage of 0.6V (typ), TI recommends that the final value be above 0.8V. A final turn on value in excess of 0.8V provides appropriate margin above the enable threshold during normal operation to prevent SEFIs during exposure to heavy ions. This recommendation is achieved by satisfying Equation 3.

$$V_{IN(final)} \times R_{EN(BOT)} / (R_{EN(TOP)} + R_{EN(BOT)}) = V_{EN(final)} > 0.8V \quad (3)$$

Alternatively, the EN pin can be driven directly from a microcontroller or FPGA. The low voltage threshold of the enable pin aids in supporting 1.1V, 1.8V, 2.5V, and 3.3V logic levels. Similarly, a final V_{EN} above 0.8V for direct logic level driving is recommended (achieved with standard logic levels).

9.3.2 Charge Pump

The charge pump is implemented as an inverting charge pump that converts V_{IN} to a negative voltage (referenced to PGND).

9.3.2.1 Charge Pump Operation

The voltage inverter portion of the TPS7H1301 and TPS7H1302 contains four CMOS switches that are switched in sequence to invert the input supply voltage. Energy transfer and storage are provided by external capacitors. Figure 9-3 shows the voltage switches: S1 and S2 are in Φ1, while S3 and S4 are in Φ2.

- CFLY Charging
  - Φ1 connects switch S1 to the positive terminal of C_{FLY} to V_{IN}, switch S3 connects the negative terminal of CFLY to PGND
  - Φ2 opens switches S2 and S4
- CFLY Inversion
  - Φ2 connects switch S2 to the positive terminal of C_{FLY} to PGND, switch S4 connects the negative terminal of CFLY to CPOUT
  - Φ1 opens switches S1 and S3
  - The resultant voltage on CPOUT is –VIN - R_{CP} x I_{OUT}

When a load is added, the output voltage drop (V_{DROOP}) is determined by the parasitic resistance (RDSON of the MOSFET switches and equivalent series resistance (ESR) of the C_{FLY} and C_{CPOUT} capacitor) and the charge transfer loss between the capacitors (see Equation 4 to calculate V_{DROOP}, charge pump R_{CP} can be calculated using Equation 5, typical charge pump values are shown in Charge Pump Resistance and Equation 6).

$$V_{DROOP} = I_{LOAD} \times R_{CP} \quad (4)$$

$$R_{CP} = \frac{1}{(f_{SW} \times C_{FLY})} + 2 \times R_{DS(ON\_Total)} + 4 \times R_{ESR(CFLY)} + R_{ESR(CPOUT)} \quad (5)$$

$$R_{DS(ON\_Total)} = \sum_{i=1}^{4} R_{DS(ONi)} \quad (6)$$

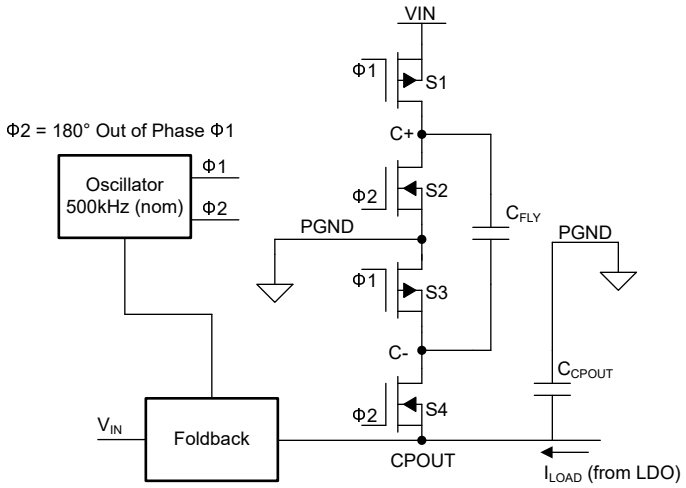


Figure 9-3. Inverting Charge Pump

9.3.2.2 Foldback Switching

When the voltage at CPOUT (V_{CPOUT}) falls below 60% to 80% of the input voltage magnitude (V_{IN}), the oscillator switching frequency reduces to 25% of the nominal switching frequency. This frequency foldback typically occurs during device start-up and short-circuit events where V_{CPOUT} drops below 70% of V_{IN} magnitude.

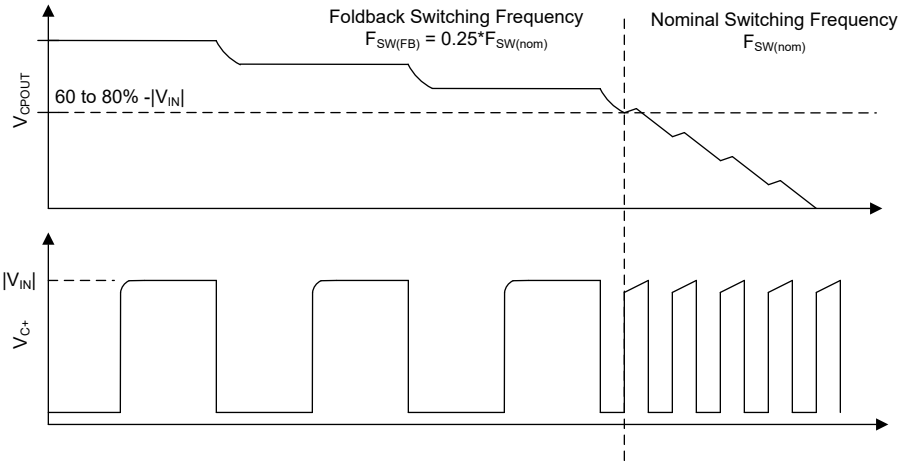


Figure 9-4. Foldback Frequency

9.3.3 Startup

During startup, the TPS7H1301 and TPS7H1302 charge pump begins switching in Frequency Foldback mode. Simultaneously, the negative LDO enters a quasi soft-start mode that limits load current until the Frequency Foldback sequence exits (when $|V_{CPOUT}| > 60$ to 80% $|V_{IN}|$).

During Frequency Foldback, V_{CPOUT} continues approaching the negative magnitude of V_{IN} while the voltage at V_{OUT} remains at the initial condition. After exiting Frequency Foldback, the OTA of the negative LDO activates, load current begins flowing, and Power Good criteria evaluation commences.

9.3.4 Power Good

The Power Good terminal features an open-drain configuration and can be used to sequence multiple LDOs. The PG terminal remains pulled low until the output voltage reaches 95% (typ) of the final regulation level. Once this threshold is met, the PG pin releases and is pulled high through an external pull-up resistor.

Since the PG pin uses an open-drain architecture, the PG pin can be pulled up to any voltage within the recommended maximum limit of 7V, providing flexible interfacing options for system-level power sequencing applications.

9.3.5 Output Voltage

The TPS7H1301 output voltage is user-programmable within the range of -6V to -0.6V. Programming is accomplished using an external resistor divider network with:

- R_{TOP}: Connected between V_{OUT} and V_{FB}
- R_{BOTTOM}: Connected between V_{FB} and GND

Use Equation 7 to determine V_{OUT}.

$$V_{OUT} = \frac{\left(R_{FB(TOP)} + R_{FB(BOT)}\right) \times V_{FB}}{R_{FB(BOT)}} \quad (7)$$

where

- V_{FB} = –0.6V (typ)

The TPS7H1302 has a fixed output voltage of -1.8V and is not user configurable.

9.3.6 Dropout

For a standard output voltage of –1.8V, input voltage exceeding 5V, and load currents below 200mA both the TPS7H1301 and TPS7H1302 do not enter dropout conditions due to the minimum input voltage (V_{IN}) and drop voltage (V_{Droop}) providing sufficient headroom.

The TPS7H1301 and TPS7H1302 integration of a charge pump and LDO, presents unique considerations in regard to LDO dropout. Firstly, when V_{OUT} is sufficiently lower than the magnitude of V_{IN} the output of the charge pump is sufficiently large enough to provide enough input voltage headroom across load current. Typically, an input voltage of 5V with an output voltage of –1.8V or higher satisfies this no dropout condition.

Secondly, when the magnitudes of VIN and VOUT are relatively close, the load current is the determining factor as to when the LDO enters dropout.

Dropout current, I_{DO}, for the TPS7H1301 is defined as the load current when the output voltage rises to 98% of the initial value at the configured output voltage. For the TPS7H1302, the dropout current output voltage criteria needs to accommodate load regulation; therefore, for load currents below 200mA, the percentage of V_{OUT} that is permitted to rise above (V_{LIM}) is 98%. When the applied load current on the TPS7H1302 is 400mA, V_{LIM} is adjusted to 97% of V_{OUT}; which is necessary to accommodate the TPS7H1302's load current. See Dropout Current Measurement for the test waveforms used to measure dropout.

During dropout conditions, the pass transistor operates in the ohmic (triode) region and functions as a resistive switch. The dropout voltage specification defines the minimum input voltage margin above the nominal programmed output voltage required to maintain output regulation. When the input voltage falls below this minimum threshold (VIN < VOUT + VDO), the output voltage concurrently decreases proportionally, falling out of regulation.

9.3.7 Output Voltage Accuracy

Voltage Reference and Output Accuracy

Both the TPS7H1301 and TPS7H1302 feature precise voltage references that are essential for minimizing the intrinsic error of the LDO.

Output Voltage Accuracy Specification

Output voltage accuracy defines the minimum and maximum output voltage error relative to the expected nominal output voltage. The accuracy specifications in the Section 7.5 table apply to the operating region where 3V ≤ VIN ≤ 6.3V.

TPS7H1301 Accuracy:

- **±1.5% specification** applies across:
  - Complete temperature range: -55℃ to 125℃
  - Full input voltage range: 3V to 6.3V
  - Output voltage range: -5V to -0.6V
  - Full load range: 10mA ≤ I_{OUT} ≤ 400mA
- **For output voltages between –6V and –5V, the output accuracy is ±3% typically**

TPS7H1302 Accuracy:

- **±1.5% specification** applies across:
  - Complete temperature range: -55℃ to 125℃
  - Output current range: 10mA ≤ I_{OUT} ≤ 250mA
  - Input voltage range: 3V to 6.3V

The TPS7H1302's internal feedback network measures the output voltage V_{OUT}; the TPS7H1302 is trimmed to deliver a fixed output of –1.8V. External resistances between the TPS7H1302 and the output load introduces a voltage "drop" (voltage rises toward ground) proportional to the applied load and trace resistance of the PCB. Minimize the PCB trace resistance as much as possible by placing the TPS7H1302 as close as possible to the load and making the PCB trace not too narrow; consider using a thicker copper trace layer (2oz.).

Important Measurement Details:

A few additional details to the measurement are noted:

- **Comprehensive Testing**: The V_{IN}, I_{OUT}, and temperature ranges verify the specification applies across all load and temperature combinations through testing multiple bias conditions covering various corners.
- **Minimum Load Current**: Test conditions specify a minimum of 10mA (not 0mA) for robust accuracy measurements. However, in normal applications, neither the TPS7H1301 nor TPS7H1302 requires a minimum load current for stability.
- **Included Error Terms**: TI does not recommend adding the following error terms to the V_{ACC} specification, as the following characteristics are inherently covered by the V_{ACC} parameter:
  - V_{FB} accuracy (TPS7H1301 only)
  - Feedback pin leakage ($I_{FB(LKG)}$) with a 1k Ω R_{TOP} resistor applied
  - $\Delta V_{OUT}/\Delta V_{IN}$ (line regulation)
  - $\Delta V_{OUT}/\Delta I_{OUT}$ (load regulation)
  - V_{OUT} temperature coefficient
- **Additional Error Sources**: Errors from feedback resistor tolerances can be added to the V_{ACC} specification.
- **Additional Resources**: For more information on determining accuracy, see the respective Detailed Design Procedures:
  - TPS7H1301
  - TPS7H1302

9.3.8 Output Noise

Output Noise

LDO output noise is defined as the internally-generated intrinsic noise produced by the semiconductor circuits within the regulator. The TPS7H1301 and TPS7H1302 devices exhibit typical output noise of 20µVRMS measured over a bandwidth of 10Hz to 100kHz.

Impact of External Compensation (TPS7H1301 only)

When an external compensation network is connected to the STAB pin, the applied network reduces the control loop bandwidth. This reduction in loop bandwidth can diminish the ability of the internal circuitry to suppress internally generated noise, potentially resulting in higher output noise levels compared to the standard configuration.

9.3.9 Power Supply Rejection Ratio

The Power Supply Rejection Ratio (PSRR) of the TPS7H1301 and TPS7H1302 quantifies the ability of the device to attenuate input noise present at V_{CPOUT} from appearing at the regulated output V_{OUT}. PSRR is mathematically defined as the ratio of input voltage variation to the corresponding output voltage variation, the rejection of input ripple is typically expressed as a positive value in decibels (dB). PSRR is mathematically defined in Equation 8.

$$\text{PSRR} = 20 \times \log_{10}\left(\frac{V_{CPOUT(AC)}}{V_{OUT(AC)}}\right) \quad (8)$$

A higher PSRR value indicates better noise rejection.

Noise Source Characteristics

The primary source of input noise in these devices originates from the switching ripple generated by the internal inverting charge pump circuit. This switching noise manifests at the fundamental switching frequency and associated switching frequency harmonics:

- TPS7H1301: 500kHz (typ) switching frequency
- TPS7H1302: 1000kHz (typ) switching frequency

Impact of External Compensation (TPS7H1301 only)

When an external compensation network is implemented, the resulting reduction in control loop bandwidth directly affects PSRR performance. A narrower loop bandwidth limits the ability of the regulator to reject input disturbances, particularly at higher frequencies, leading to diminished overall PSRR performance compared to the standard configuration.

9.3.10 Stability

9.3.10.1 Stability of the TPS7H1301

Stability Margins and Design Requirements

Traditional stability margins for space-rated integrated circuits typically impose more stringent requirements than those for industrial and consumer electronics applications. Standard criteria include a minimum gain margin of 6dB and phase margin of 50°. The TPS7H1301 incorporates internal compensation circuitry designed to maintain conservative stability margins across the following operating conditions:

- $3V \le V_{IN} \le 6.3V$
- $-5V \le V_{OUT} \le -0.6V$
- $3mA \le I_{OUT} \le 400mA$
- $C_{OUT} = 22\mu F$
- $-55°C \le T_A \le 125°C$

Typically no supplemental external compensation is necessary when operating in the conditions above. When applications require enhanced stability performance or when using specific output capacitor types (e.g. tantalum capacitors), or output capacitor networks, the optional STAB pin allows for external compensation network adjustment to optimize loop stability.

Intrinsic Stability Performance

The TPS7H1301 features wide intrinsic stability margins, providing robust performance across varying load conditions, temperature ranges, and input voltage variations. This inherent stability reduces design complexity and component count while facilitating reliable operation in demanding space applications. Figure 9-5 illustrates the internal compensation with R_{COMP} and C_{COMP}; these values are specified by design to be 30kΩ and 400pF.

External Compensation Capability

For applications requiring enhanced stability margins or operating under extreme conditions, the STAB pin provides access to an external RC compensation network. This compensation architecture, illustrated in Figure

9-5, connects directly to the output stage of the error amplifier, positioning the external network strategically before the buffer stage of the pass element.

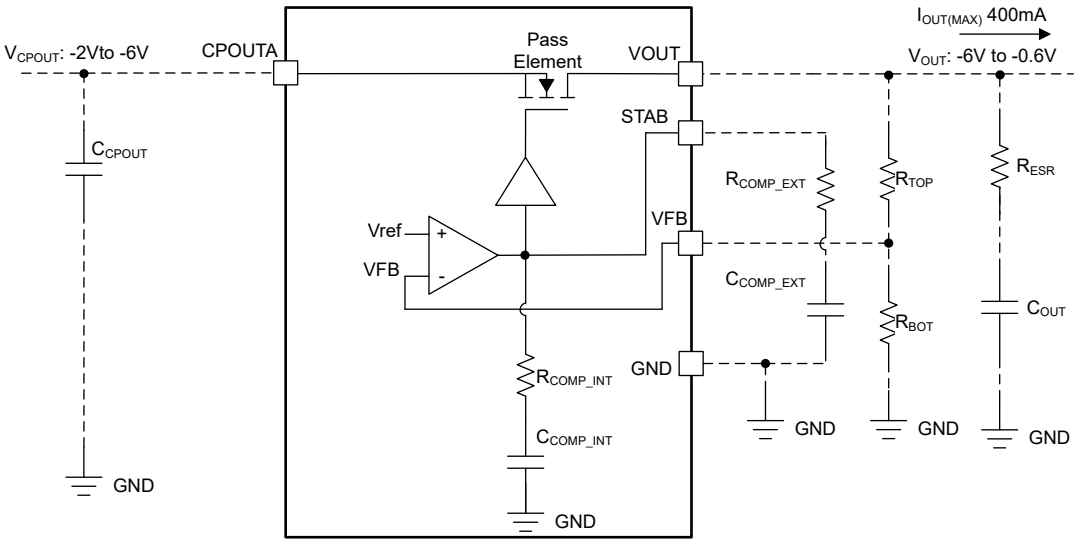


Figure 9-5. Simplified Compensation Schematic

9.3.10.2 Stability of the TPS7H1302

Intrinsic Stability

The TPS7H1302 is designed with the same wide intrinsic stability margins as the TPS7H1301, providing robust performance across varying load conditions, temperature ranges, and input voltage variations. This inherent stability reduces design complexity, while the integrated feedback resistor network further reduces component count, facilitating reliable operation in demanding space applications. Figure 9-6 illustrates the internal compensation with R_{COMP} and C_{COMP}; these are specified by design to be 30kΩ and 400pF.

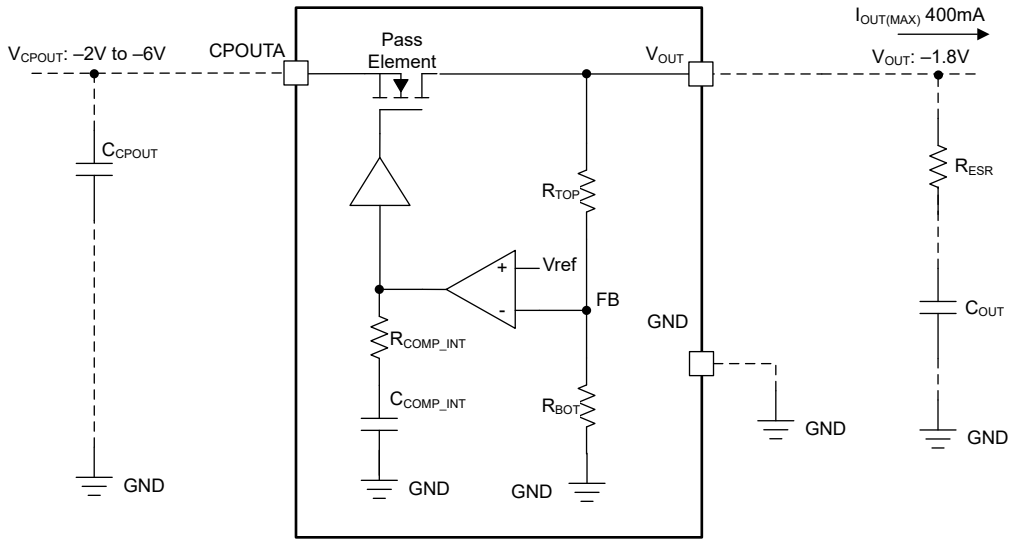


Figure 9-6. TPS7H1302 Simplified Compensation Schematic

9.3.11 Thermal Shutdown

Upon exceeding the TPS7H1301 and TPS7H1302 thermal shutdown temperature limit, the integrated thermal shutdown circuitry activates to turn-off the device when the die temperature exceeds $T_{SD(enter)}$. As the die cools

below $T_{SD(exit)}$, the device resumes regulation. The typical $T_{SD(enter)}$ of 160°C and $T_{SD(exit)}$ of 130°C provides a large hysteresis (30°C typical). The large hysteresis is intended to allow the device to sufficiently cool before attempting to resume regulation.

9.4 Device Functional Modes

9.4.1 Enable Disable

The table below shows the device functional modes:

Table 9-1. Device Functional Modes

EN PIN	DEVICE STATUS
High	Regulation mode
Low	Shutdown mode

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

There are a variety of use cases for the TPS7H1301 and TPS7H1302; the following use cases are discussed in this section:

1. –1.8V LDO implementing configurable turn-on, charge pump configuration and adjustable output configuration with the TPS7H1301
2. Expanded current operation with two TPS7H1301s in parallel
3. –1.8V LDO with fixed output using the TPS7H1302
4. Improving noise performance of the TPS7H1302

10.2 Typical Application TPS7H1301

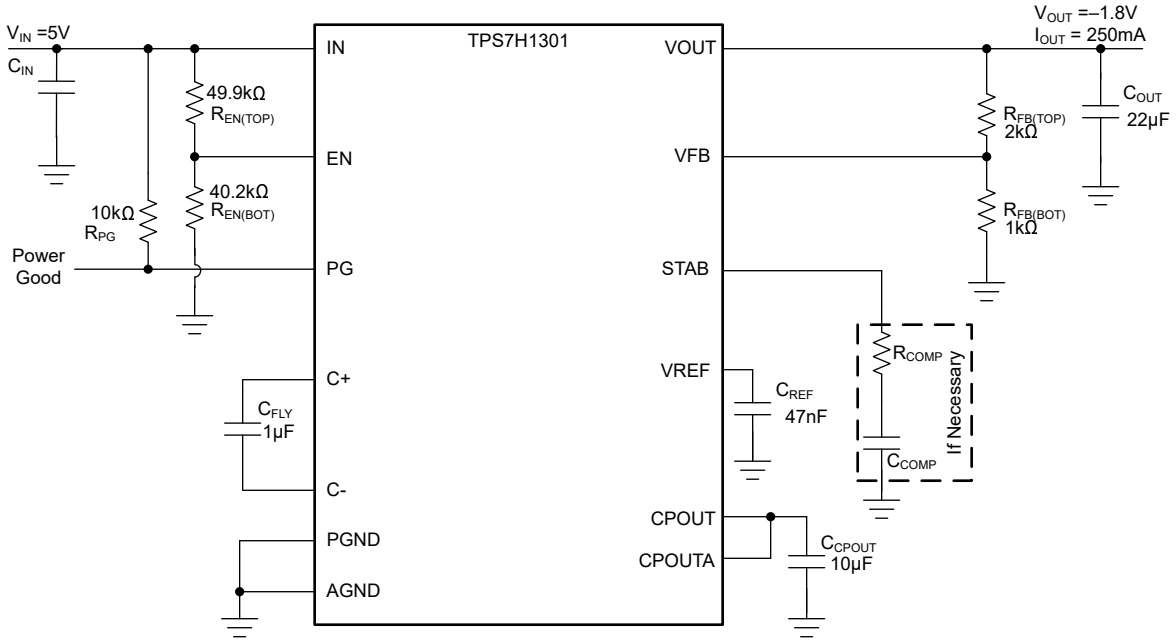


Figure 10-1. Typical Application Circuit TPS7H1301

10.2.1 Design Requirements TPS7H1301

This example highlights a design using the TPS7H1301EVM evaluation module (EVM). For more details, please refer to the EVM user's guide, TPS7H1301EVM-CVAL Evaluation Module (EVM) User's Guide (SNVU944). A few parameters must be known to start the design process. These parameters are typically determined at the system level. For this example, we start with the following known parameters:

Table 10-1. Design Parameters

PARAMETER	VALUE
V_{IN}	5V
V_{OUT}	–1.8V
I_{OUT}	250mA
V_{EN}	1.6V

10.2.2 Detailed Design Procedure TPS7H1301

10.2.2.1 Capacitor Selection

Capacitor selection is essential for the operation of the TPS7H1301 and the TPS7H1302 (referred together as the TPS7H130x). In general, TI recommends selecting capacitors which are at least 16V ceramic capacitors for C_{FLY} and C_{CPOUT}; prioritize low-ESR values, place all capacitors as close to the TPS7H130x as permissible.

10.2.2.1.1 Input Capacitor (C_{IN}) Selection

TI recommends placing a 10µF 25V (or higher) ceramic capacitor as close as possible to the input pin of the TPS7H130x; additional capacitance and bypass capacitance are considered optional.

The input capacitor (C_{IN}) serves as a charge reservoir that facilitates rapid charge transfer from the supply to the flying capacitors during the charge phase. This capacitor prevents input voltage sag at the beginning of each charge phase when flying capacitors connect to the input. Additionally, the input capacitor filters input noise, protecting sensitive internal analog circuitry that derives bias from the input line.

Effect on Input Ripple

Input capacitance has a direct and proportional relationship with input voltage ripple:

- Increasing input capacitance → Proportionally decreases input voltage ripple
- Decreasing input capacitance → Proportionally increases input voltage ripple

10.2.2.1.2 C_{FLY} TPS7H1301

C_{FLY} is the charge pump capacitor that transfers charge from the input to the charge pump output (CPOUT pin).

For typical high-current applications, TI recommends at a minimum a nominally rated 1µF ceramic output capacitor for stable operation. Polarized capacitors (tantalum, aluminum, electrolytic, and so forth) must not be used for the flying capacitor, as polarized capacitors can become reverse-biased during operation.

If C_{FLY} is sized too small, the charge pump is unable to support high current applications; conversely if C_{FLY} is too large, the charge pump current becomes excessive for the charge pump switches and causes increased input and output voltage ripple.

Sizing C_{FLY}

Size C_{FLY} to a nominal ratio of 1:10 to 1:2 of the charge pump output capacitance C_{CPOUT}.

Use Equation 9 to size C_{FLY}, f_{SW} is 500kHz (typ.) and ΔV_{CFLY} takes into account voltage overshoot at the C_{FLY} capacitor nodes. For applications with nominal V_{IN} conditions 5V or lower and output currents below 250mA, using a factor of 0.2 in Equation 10 is sufficient; as V_{IN} and I_{OUT} increase above 5V or 250mA the ΔV_{CFLY} needs to be adjusted lower (apply a factor of 0.1), which aids in preventing excessive overshoot on pin C+ and C-.

$$C_{FLY} = \frac{I_{OUT}}{f_{SW} \times \Delta V_{CFLY}} \quad (9)$$

$$\Delta V_{CFLY} = (0.1\ to\ 0.2) \times V_{IN} \quad (10)$$

Applying Equation 9 yields the following:

$$C_{FLY} = \frac{250mA}{500kHz \times 0.2} = 2.5\mu F \quad (11)$$

The result of Equation 11 is 2.5µF which satisfies the C_{FLY} to C_{CPOUT} ratio, for this Detailed Design Procedure example, 1µF is selected to align with characterization data in the Section 7.5 table which is a more onerous configuration as a 1µF lowers LDO headroom vs. a 2.5µf at CFLY.

Effects of C_{FLY}

Dropout Current and charge pump operational efficiency are reliant on the charge pump resistance and voltage droop, which is directly affected by the choice of C_{FLY}; selecting a capacitor that is too small or too high ESR increases charge pump output resistance, such that the resulting voltage droop lowers the available headroom for the integrated LDO and reduces overall charge pump efficiency; refer to Figure 7-8 through Figure 7-12 to see how CFLY selection changes the charge pump efficiency.

Consideration of C_{FLY} capacitor characteristics, such as DC bias, temperature coefficient are essential in assessing the contribution of the capacitor to charge pump resistance; Equation 12 calculates the fly capacitors contribution to the overall charge pump output resistance and V_{DROOP}. Note, that the min switching frequency (f_{SW}) from the Electrical Characteristics table is the more conservative estimation parameter; as min f_{SW} results in a higher charge pump resistance.

$$R_{CFLY} = \frac{1}{f_{SW} \times C_{CFLY(min)}} + 4 \times R_{ESR(CFLY)} \quad (12)$$

As Equation 12 shows, a typical reduction in output capacitance due to DC Bias and temperature typically reduces overall C_{FLY} capacitance by 15% to 25% and thus increases charge pump output resistance.

To calculate $C_{FLY(min)}$ consult the capacitor manufacturer data and apply the overall tolerance, DC Bias, and temperature derating: For example, a 25V 1µF X7R capacitor with the following parameters:

- Case Size: 0805
- Tolerance: -5%
- DC Bias @ 5V: -4.56%
- Temperature derating @ 125ºC: -14.56%
- R_{ESR} @ 400kHz: 10mΩ

Table 10-2 is an example tradeoff for selecting either a solitary 1µF (nom.) capacitor or a 2.2µF (nom) capacitors; the overall contribution of C_{FLY} to the resistance of the charge pump is compared against overall charge pump efficiency.

Table 10-2. C_{FLY} Comparison

Attribute	1µF	2.2µF
Part Number	KGM21AR71C105JL	KGM21AR71C225KL
QTY	1	1
Case Size	0805	0805
Voltage Rating	16V	16V
Dielectric	X7R	X7R
Derating Parameters		
Tolerance	-5%	-10%
DC Bias @ 5V	-4.56%	-10.3%
Tempco. @ 125ºC	-14.56%	-15%
Results		
Effective Capacitance	0.775µF	1.51µF

Table 10-2. C_{FLY} Comparison (continued)

Attribute	1µF	2.2µF
ESR	10mΩ	10mΩ (effective res.)
R_{CFLY}	3.45Ω	1.69Ω
Peak charge pump efficiency, V_{IN} = 5V	79%	83.5%

To calculate the minimum capacitance for C_{FLY} use :

$$C_{FLY(min)} = C_{FLY(nom)} \times (Tol.) \times (DC\ Bias) \times (Temp) \quad (13)$$

Applying Equation 13 for the 1µF (nom.) capacitor:

$$C_{FLY(min)} = 1\mu F \times (1 - 0.05) \times (1 - 0.0456) \times (1 - 0.1456) = 0.775\mu F \quad (14)$$

The worst case contribution of C_{FLY} is calculated by applying Equation 12 (1µF (nom.) example)

$$R_{CFLY} = \frac{1}{400kHz \times 0.775\mu F} + 4 \times 10m\Omega = 3.45\Omega \quad (15)$$

Table 10-2 shows that the additional component count of the two 0.68µF capacitors offers a significant reduction in the contribution of C_{FLY} to overall charge pump output resistance. Applications at higher operating temperatures, operating currents, or lower V_{IN} benefit from more from overall lower charge pump output resistance. This design examples uses a V_{IN} of 5V and a I_{LOAD} of 250mA is sufficiently served by the 1µF C_{FLY} capacitor.

Overall the selected value for CFLY, affects charge pump resistance and charge pump efficiency; refer to figures Figure 7-8 to Figure 7-11 to see how CFLY selection affects overall charge pump efficiency.

10.2.2.1.3 CPOUT Capacitor TPS7H1301

The Charge Pump Output Capacitor (C_{CPOUT}) is recommended to be configured using a 10µF 16V (or greater voltage rating) ceramic capacitor with a low ESR value. The ESR of C_{CPOUT} does contribute to the output resistance of the charge pump and can be added to the contributions of the charge pump FET $R_{DS(ON)}$, C_{FLY} ESR, and trace resistance at pins C+ and C-.

CPOUT Effect on Charge Pump Output Ripple

Charge pump output capacitance (C_{CPOUT}) and switching frequency has a direct and proportional relationship with charge pump output voltage ripple. The TPS7H1301 operates at a fixed frequency of 500kHz; therefore:

- Increasing CPOUT capacitance → Proportionally decreases charge pump output ripple
- Decreasing CPOUT capacitance → Proportionally increases charge pump output ripple

$$V_{Ripple\_CPOUT(LF)} = \frac{I_{OUT}}{C_{CPOUT}} \times \frac{0.5}{fsw} \quad (16)$$

Calculating Charge Pump Output Ripple

The low frequency charge pump output ripple can use Equation 16 to calculate the output ripple. Using the switching frequency for the TPS7H1301, f_{SW} = 500kHz (typ) and the load current, 250mA; the charge pump output ripple is calculated to be:

$$V_{Ripple\_CPOUT(LF)} = \frac{250mA}{10\mu F} \times \frac{0.5}{500kHz} = 25mV_{pp} \quad (17)$$

The charge pump output ripple is separate from high frequency ripple caused by parasitic elements in the circuit.

Sizing of C_{CPOUT} also affects the output ripple. When using values other than 10µF, TI recommends sizing C_{FLY} and C_{IN} to further optimize performance.

10.2.2.1.4 Bypass Capacitors

Bypass capacitors are not required for use with the TPS7H130x; however, given the hard switching nature of the charge pump voltage inverter section, 100nF or smaller bypass capacitors at CPOUT, and VOUT offers high frequency noise reduction. Smaller ceramic capacitors across CFLY (connected to C+ and C-) can perform as bypass capacitors as a method to further reduce high frequency noise in the charge pump, polarized capacitors are not permitted for use.

10.2.2.1.5 Output Capacitor

TI recommends using a 22µF ceramic 25V capacitor with a low ESR (<50mΩ) for VOUT; this capacitor serves the output of the negative LDO. Output capacitors with excessively high ESR, impacts overall LDO stability.

10.2.2.2 Charge Pump Output Resistance

Restating Equation 5 from Section 9.3.2.1 gives the total charge pump output resistance and is referenced as Equation 18 in this section for convenience; which accounts for C_{FLY}, the integrated FETs, and the ESR of C_{CPOUT} contribution to the overall charge pump output resistance.

$$R_{CP} = \frac{1}{(f_{SW} \times C_{FLY})} + 2 \times R_{DS(ON\_Total)} + 4 \times R_{ESR(CFLY)} + R_{ESR(CPOUT)} \quad (18)$$

Applying Equation 18:

$$R_{DS(ON_{Total})} = 300m\Omega + 175m\Omega + 235m\Omega + 220m\Omega = 935m\Omega \left(typ\right) \quad (19)$$

Using the maximum $R_{DS(ON)}$ values for the switches is a conservative approach to prevent underestimating charge pump output resistance and the resultant voltage drop under load current (V_{DROOP}).

10.2.2.3 Configuring LDO Output

Re-arranging Equation 7 and selecting $R_{FB(top)}$ to 2kΩ results in the following:

$$R_{FB(BOT)} = \frac{R_{FB(TOP)}}{\left(\frac{V_{OUT}}{V_{FB}} - 1\right)} \quad (20)$$

Applying Equation 20 is shown in Equation 21, which results in an $R_{FB(BOT)}$ value of 1kΩ. TI recommends using precision 0.1% resistors for the feedback resistor network.

$$R_{FB(BOT)} = \frac{2k\Omega}{\left(\frac{-1.8V}{-0.6V} - 1\right)} = 1k\Omega \quad (21)$$

10.2.2.4 Output Noise

Consider the following for performance in noise sensitive applications:

- Implement appropriate bypass capacitors and filtering components for high-frequency noise suppression
- Evaluate the trade-off between stability compensation and noise performance when using external STAB pin networks

10.2.2.5 PSRR Design Implications

For applications requiring high PSRR performance:

- Consider the frequency-dependent nature of PSRR when evaluating system performance
- Account for the trade-off between stability margins (via external compensation) and PSRR capability
- Consider C_{OUT} influence (frequency response)
- Account for application load and resultant LDO headroom
- Pay particular attention to noise rejection at the switching frequencies and harmonics
- Refer to the PSRR vs. frequency graphs for detailed performance characteristics across the operational bandwidth

10.2.2.6 Stability Design Considerations

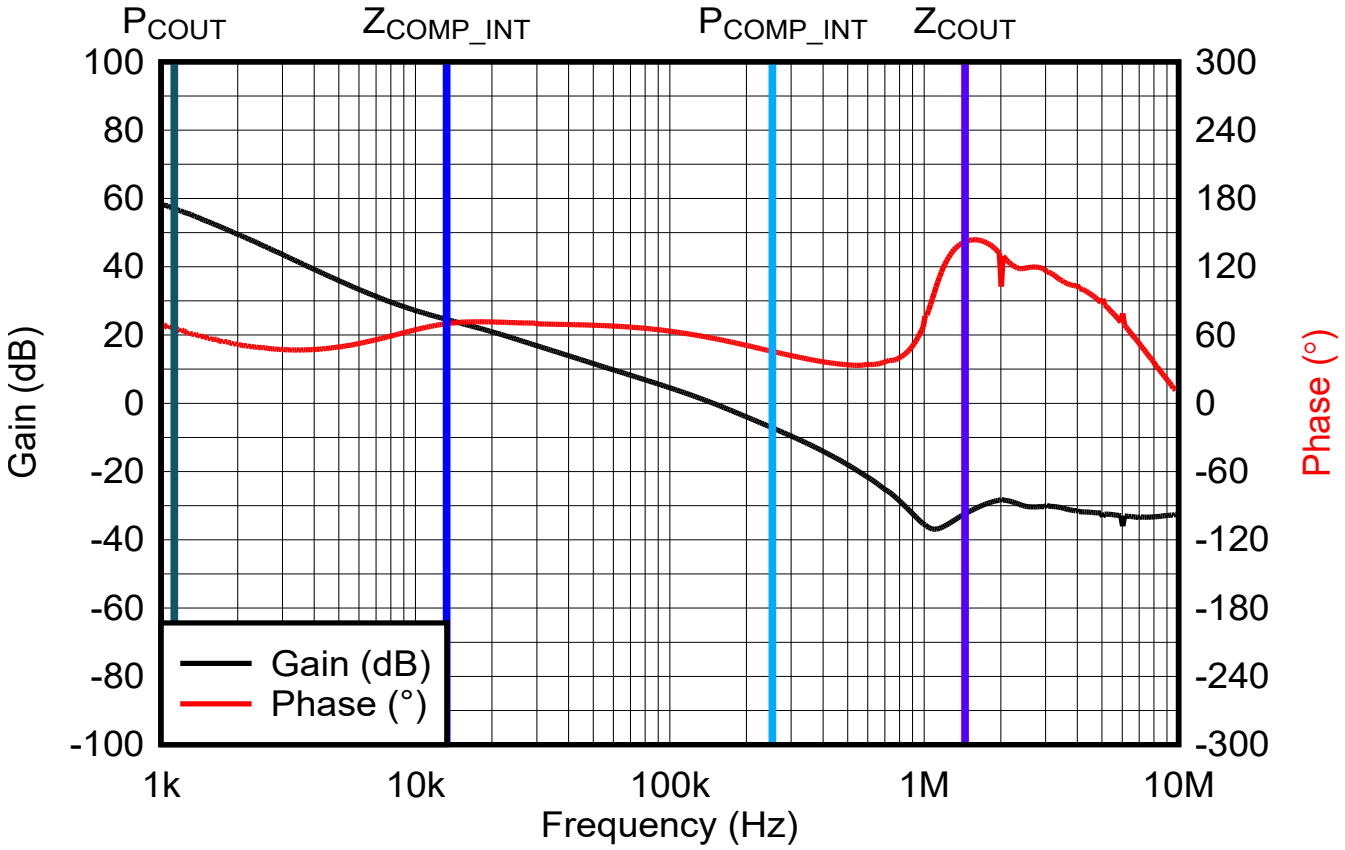


Figure 10-2. Simplified Pole Zero Analysis

The stability of the LDO is influenced primarily by the dominant load pole and zero for the output capacitor (P_{COUT}, Z_{COUT}) and the internal compensation network (P_{COMP_INT}, Z_{COMP_INT}). Figure 10-2 illustrates where the pole and zero of the output capacitor and the internal compensation pole and zero of the LDO are located.

The pole and zero of the output capacitor are calculated using Equation 22 and Equation 23:

$$P_{COUT} = \frac{1}{2\pi \times R_{LOAD} \times C_{OUT}} \quad (22)$$

$$Z_{C_{OUT}} = \frac{1}{2\pi \times ESR_{C_{OUT}} \times C_{OUT}} \quad (23)$$

Applying Equation 22 and Equation 23 results in the following location of the respective pole and zero:

$$P_{COUT} = \frac{1}{2\pi \times 7.2\Omega \times 22\mu F} = 1003Hz \quad (24)$$

$$Z_{C_{OUT}} = \frac{1}{2\pi \times 5m\Omega \times 22\mu F} = 1.446MHz \quad (25)$$

The internal compensation network pole and zero are calculated using Equation 26 and Equation 27:

$$P_{COMP\_INT} = \frac{C_{COMP\_INT} + C_{OTA}}{2\pi \times R_{COMP} \times C_{COMP\_INT} \times C_{OTA}} \quad (26)$$

$$Z_{COMP\_INT} = \frac{1}{2\pi \times R_{COMP} \times C_{COMP\_INT}} \quad (27)$$

C_{OTA} is the error amplifier's output capacitance; which is specified by design to be 20pf.

Applying Equation 26 and Equation 27 results in the following location of the respective pole and zero:

$$P_{COMP\_INT} = \frac{400pF + 20pF}{2\pi \times 30k\Omega \times 400pF \times 20pF} = 253kHz \quad (28)$$

$$Z_{COMP\_INT} = \frac{1}{2\pi \times 30k\Omega \times 400pF} = 13.3kHz \quad (29)$$

When applying an external compensation network utilizing the STAB pin utilize Equation 30 and Equation 31:

$$P_{COMP\_EXT} = \frac{(C_{COMP\_INT} \backslash\backslash C_{COMP\_EXT}) + C_{OTA}}{2\pi \times (R_{COMP\_INT} \backslash\backslash R_{COMP\_EXT}) \times (C_{COMP\_INT} \backslash\backslash C_{COMP\_EXT}) \times C_g} \quad (30)$$

$$Z_{COMP\_EXT} = \frac{1}{2\pi \times (R_{COMP\_INT} \backslash\backslash R_{COMP\_EXT}) \times (C_{COMP\_INT} \backslash\backslash C_{COMP\_EXT})} \quad (31)$$

10.2.3 Application Curves

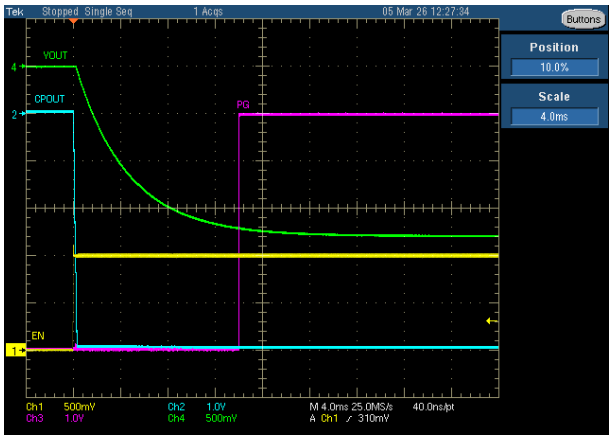


Figure 10-3. Startup

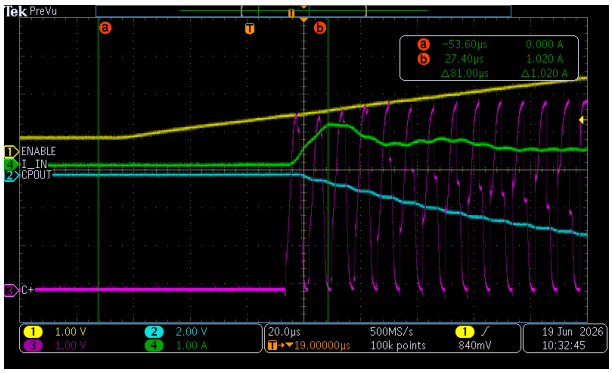


Figure 10-4. Start Up Inrush Current

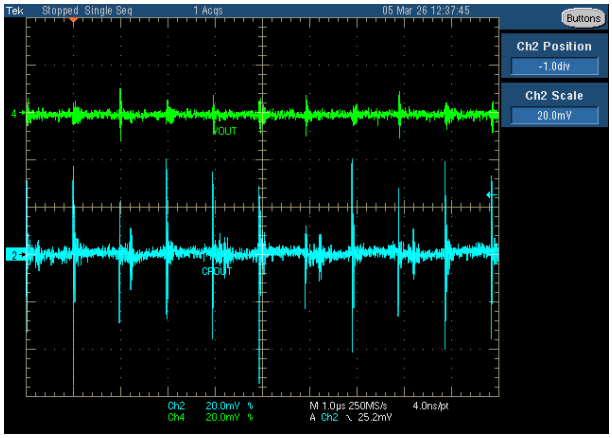


Figure 10-5. Charge Pump Output, V_{CPOUT} and Output Voltage, V_{OUT}

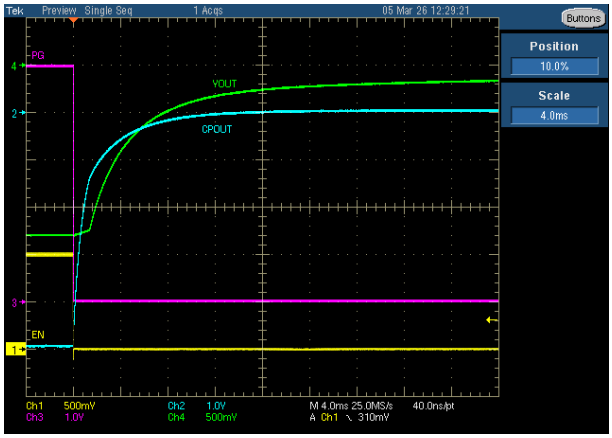


Figure 10-6. Shutdown

10.3 Typical Application TPS7H1301 Parallel Operation

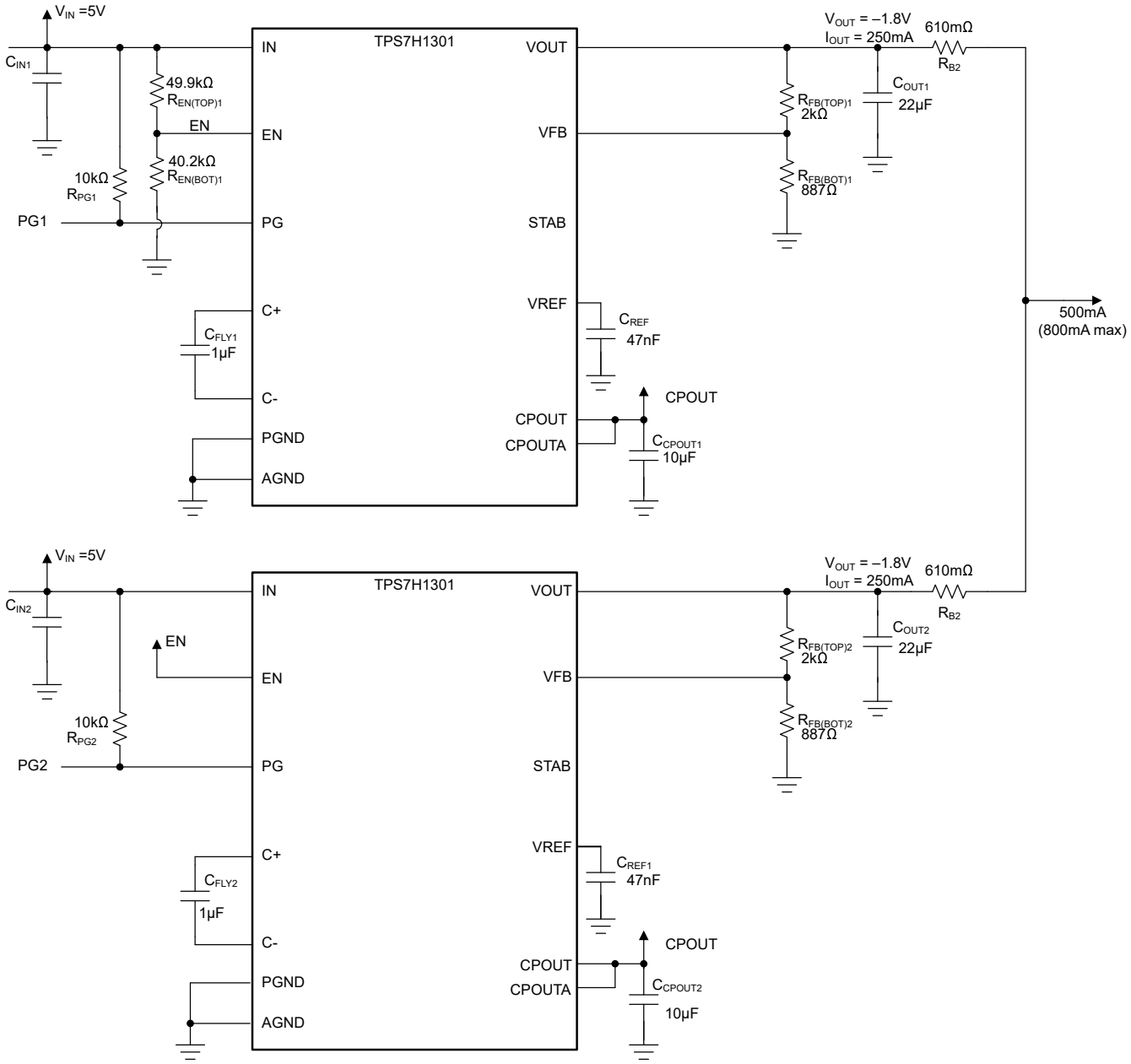


Figure 10-7. Typical Application TPS7H1301 Parallel Configuration

10.3.1 Design Requirements

Figure 10-7 depicts two TPS7H1301's configured for parallel operation to supply a 500mA load.

Table 10-3. Design Parameters

PARAMETER	VALUE
V_{IN}	5V±10%
V_{OUT}	–1.8V
I_{OUT}	500mA

The parallel configuration can facilitate load currents up to 800mA.

10.3.2 Detailed Design Procedure Parallel TPS7H1301

The overall connection methodology for operating two TPS7H1301's in parallel is to connect the charge pump outputs (CPOUT) together and to have the regulated outputs connected with ballast resistors. Reference voltage (VREF), feedback (FB), power good (PG), and external compensation (STAB) for each device are separated. Enabling (EN) of both devices facilitates both simultaneous and individual control.

Configuration of two TPS7H1301's in parallel is further described in Table 10-4:

Table 10-4. Parallel Configuration Notes

Device	Pin	Connection	Note
1	V_{IN}	Connect to positive input supply and 10µF	Shared node with Device 2.
	EN	Connection to logic level control pin or an external voltage divider	Shared node with Device 2.
	PG	Connect a 10kΩ to V_{IN} and PG	Separate node for Device 2 PG pin, a solitary pullup resistor (R_{PG}) can be shared with Device 2.
	CFLY+	Connect a 1µF ceramic capacitor to CFLY+ and CFLY-	Separate fly capacitor from Device 2.
	CFLY-		
	PGND	Connect in PCB to GND plane	Shared node with all AGND and PGND Pins.
	AGND		
	VOUT	Connect a 22µF ceramic capacitor	A ballast resistor is required prior to connection to the load.
	VFB		Feedback network is not shared with both devices.
	STAB		External compensation network is separate from Device 2's external compensation.
	VREF	Connect a 47nF capacitor.	VREF capacitor is separate from Device 2's VREF.
	CPOUT	Connect a 10µF Ceramic capacitor	CPOUT and CPOUTA for both device are on the same node. Both devices require a 10µF allocated to each device.
	CPOUTA		

Table 10-4. Parallel Configuration Notes (continued)

Device	Pin	Connection	Note
2	V_{IN}	Connect to positive input supply and 10µF	Shared node with Device 1.
	EN	Connection to logic level control pin or an external voltage divider.	Shared node with Device 1.
	PG	Connect a 10kΩ to V_{IN} and PG	Separate node for Device 1 PG pin, a solitary pullup resistor (R_{PG}) can be shared with Device 1.
	CFLY+	Connect a 1µF ceramic capacitor to CFLY+ and CFLY-	Separate fly capacitor from Device 1.
	CFLY-		
	PGND	Connect in PCB to GND plane	Shared node with all AGND and PGND Pins.
	AGND		
	VOUT	Connect a 22µF ceramic capacitor	A ballast resistor is required prior to connection to the load.
	VFB		Feedback network is not shared with both devices.
	STAB		External compensation network is separate from Device 1's external compensation.
	VREF	Connect a 47nF capacitor.	VREF capacitor is separate from Device 1's VREF.
	CPOUT	Connect a 10µF Ceramic capacitor.	CPOUT and CPOUTA for both device are on the same node. Both devices require a 10µF allocated to each device.
	CPOUTA		

10.3.2.1 Parallel Ballast Resistor

To calculate the ballast resistor value, calculate the following aspects:

1. Worst-case output voltage mismatch, ΔV_{max}
2. Ballast resistor value ($R_{Ballast}$) and power rating
3. Voltage drop of the ballast resistor,$V_{DROOP(Ballast)}$
4. Configuring feedback resistor network to account for $R_{Ballast}$ operation

Worst-Case Output Voltage mismatch ΔV_{max}

ΔV_{OUT} is determined by the contribution of the LDO output accuracy (V_{ACC}) and the precision of the feedback resistors (R_{tol}). The TPS7H1301 has an output accuracy (V_{ACC}) of ±1.5% across voltage, current, temperature and TID; the voltage reference (V_{ref}) has a typical value of 600mV±9mV (min / max).

TI recommends using precision 0.1% feedback resistor; lower tolerance values are permissible; however in parallel applications the lower feedback resistor tolerance directly degrades parallel configuration performance.

Equation 32 is used to calculate the maximum voltage difference possible when considering the combined accuracy of the LDO and feedback resistor tolerances; Equation 33 is a numerical example using 0.1% feedback resistor tolerances.

$$\Delta V_{max} = 2 \times (V_{ACC}\% + 2 \times R_{tol}\%) \times |V_{OUT}| \quad (32)$$

$$\Delta V_{max} = 2 \times (1.5\% + 2 \times 0.1\%) \times |-1.8V| = 61mV \quad (33)$$

Calculate the Required Ballast Resistance

The ballast resistor requires the designer to select a maximum current difference between the LDOs; the individual typical load is 250mA for this application's 2 LDO 500mA parallel combination, a higher mismatch tolerance of 20% (ΔI_{max}) is sufficient.

For applications in which the individual load current are closer to the Recommended Operating Condition (ROC) maximum current rating of 400mA (per LDO), TI recommends a tighter ΔI_{max} selection (e.g... 10% or lower). Furthermore, the current mismatch needs to be subtracted from the maximum parallel output, which satisfies the individual LDOs $I_{OUT(max)}$ rating of 400mA.

$$\Delta I_{max} = \frac{\Delta V_{max}}{R_{B1} + R_{B2}} = \frac{\Delta V_{max}}{2 \times R_B},\ R_{B1} = R_{B2} \quad (34)$$

Solving for R_B in Equation 34 yields Equation 35, which is then applied in Equation 36.

$$R_B = \frac{\Delta V_{max}}{2 \times \Delta I_{max}} \quad (35)$$

$$R_B = \frac{61mV}{2 \times 50mA} = 610m\Omega \quad (36)$$

Selecting the nearest E192 (0.1% tol) value, R_B=612mΩ, for E96 (1% tol) a value of 604mΩ can be selected.

Ballast Resistor Droop Voltage and Power

Equation 37 determines $V_{DROOP(Ballast)}$ is the voltage drop introduced by each R_B:

$$V_{DROOP(Ballast)} = 0.5 \times I_{OUT} \times R_B \quad (37)$$

Applying Equation 37 is shown in Equation 38:

$$V_{DROOP(Ballast)} = 0.5 \times 500mA \times 612m\Omega = 153mV \quad (38)$$

Use Equation 39 to determine the power dissipated in R_B; which is shown in Equation 40.

$$P_{Ballast} = (0.5 \times I_{OUT})^2 \times R_B \quad (39)$$

$$P_{Ballast} = (0.5 \times 500mA)^2 \times 612m\Omega = 38.3mW \quad (40)$$

The resultant dissipated power for R_B is 38.3mW which can support 1/8W resistors; this is possible due to the precision feedback resistors. Using less precise feedback resistors results in a larger ΔV_{max}; a substantial increase in ΔV_{max} increases R_B resistance, power dissipation, and $V_{DROOP(Ballast)}$. Selection of feedback resistor (R_{FB}) precision introduces a tradeoff of ΔI_{max}, total output current, and minimum input voltage $V_{IN(min)}$.

Configuring LDO output

The LDO output voltage must now update the feedback network to output a regulated voltage that takes into account $V_{DROOP(Ballast)}$; use Equation 41 to calculate the updated output voltage setting, $V_{OUT(Parallel)}$:

$$V_{OUT(\text{Parallel})} = V_{OUT} - V_{DROOP(Ballast)} \quad (41)$$

$$V_{OUT(\text{Parallel})} = -1.8V - 152.5mV = -1.9525V \quad (42)$$

Equation 41 nets a new output voltage setting of –1.9525V; applying Equation 20 is shown in equation Equation 43.

$$R_{FB(BOT)\_Parallel} = \frac{2000k\Omega}{\left(\frac{-1.9525V}{-0.6V} - 1\right)} = 887\Omega \quad (43)$$

Minimum Input Voltage

The minimum input voltage of the TPS7H1301 and TPS7H1302 in parallel operation needs to consider the following:

1. V_{DROOP}, charge pump voltage drop as configured with C_{FLY} and C_{CPOUT}.
2. $V_{DROOP(Ballast)}$, voltage drop of R_B
3. $V_{OUT(Parallel)}$, configured output voltage of LDO before R_B
4. V_{DO}, dropout voltage of the LDO at the applied current for each LDO.

$$V_{IN(\min)} \geq V_{DROOP} + V_{OUT(Parallel)} + V_{DO} \quad (44)$$

10.3.3 Application Performance Plots

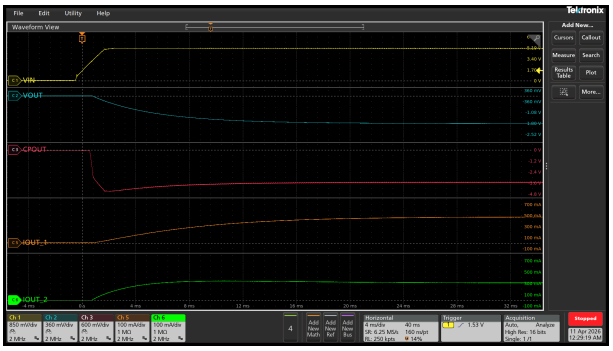


Figure 10-8. Startup Waveform Parallel Configuration TPS7H1301

10.4 Typical Application TPS7H1302

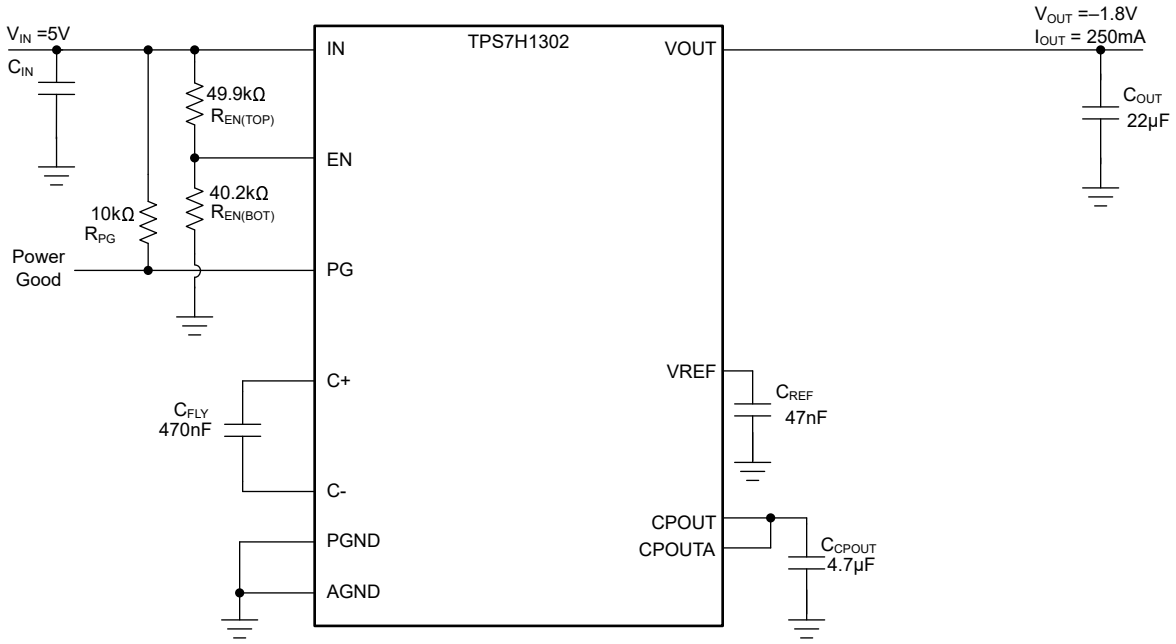


Figure 10-9. Typical Application TPS7H1302

10.4.1 Design Requirements TPS7H1302

The TPS7H1302 provides a fixed output of –1.8V, while eliminating the need for feedback resistors and external compensation networks. This application example shows how to power parts such as the DAC39RF22-SEP.

Table 10-5. Design Parameters

PARAMETER	VALUE
V_{IN}	5V±10%
V_{OUT}	–1.8V±1.5%
High Frequency Ripple, $V_{RIP(HF)}$	±25mV
I_{OUT}	250mA

10.4.2 Detailed Design Procedure TPS7H1302

This example highlights a design using the -1.8V fixed output of the TPS7H1302. The TPS7H1302 facilitates the removal of the feedback resistors and external compensation; furthermore the 1MHz switching frequency of the charge pump reduces the required capacitance of capacitors C_{FLY} and C_{CPOUT}. The TPS7H1302EVM includes non-populated pads at the C_{IN}, C_{FLY}, C_{CPOUT}, and C_{OUT} positions to facilitate implementing different capacitor networks, for more details please refer to the EVM user's guide, TPS7H1302EVM-CVAL Evaluation Module (EVM) User's Guide (SLVUE11). For this example the following known parameters are used to begin the design:

Table 10-6. Design Parameters

PARAMETER	VALUE
V_{IN}	5V±10%
V_{OUT}	-1.8V
I_{OUT}	250mA
V_{EN}	1.6V

10.4.2.1 Capacitor Selection TPS7H1302

Guidance for capacitor selection for C_{IN} and C_{OUT} is identical to the TPS7H1301; see sections Section 10.2.2.1.1 and Section 10.2.2.1.5. The charge pump of the TPS7H1302 operates at an f_{SW} of 1MHz, which requires different values of C_{FLY} and C_{CPOUT}.

10.4.2.2 CFLY Capacitor TPS7H1302

TI recommends a C_{FLY} capacitor value of 470nF; applying Equation 12 nets a nominal contribution to the charge pump resistance of:

$$R_{CFLY} = \frac{1}{1000kHz \times 470nF} + 4 \times 10m\Omega = 2.17\Omega \left(nom\right) \quad (45)$$

Using min f_{SW} and derated C_{FLY} values nets the following resistance:

$$R_{CFLY} = \frac{1}{800kHz \times 364nF} + 4 \times 10m\Omega = 3.47\Omega \left(max\right) \quad (46)$$

10.4.2.3 CPOUT Capacitor TPS7H1302

TI recommends the CPOUT capacitor for the TPS7H1302 with a 4.7µF 16V (or greater voltage) ceramic capacitor with a low ESR value. Applying Equation 16:

$$V_{Ripple\_CPOUT(LF)} = \frac{250mA}{4.7\mu F} \times \frac{0.5}{1000kHz} = 26.6mV_{pp} \quad (47)$$

10.4.2.4 Stability TPS7H1302

The TPS7H1302 is designed for stable operation with a 22µF ceramic output capacitor; the TPS7H1302 does not have an external feedback pin and STAB pin for external compensation; however, the TPS7H1302 shares the same error amp architecture as the TPS7H1301. For applications in which a 22µF is not desirable, confirm the new configuration is stable by performing load step tests at target slew rates then verifying no excessive ringing is present.

10.4.3 TPS7H1302 Application Performance Plots

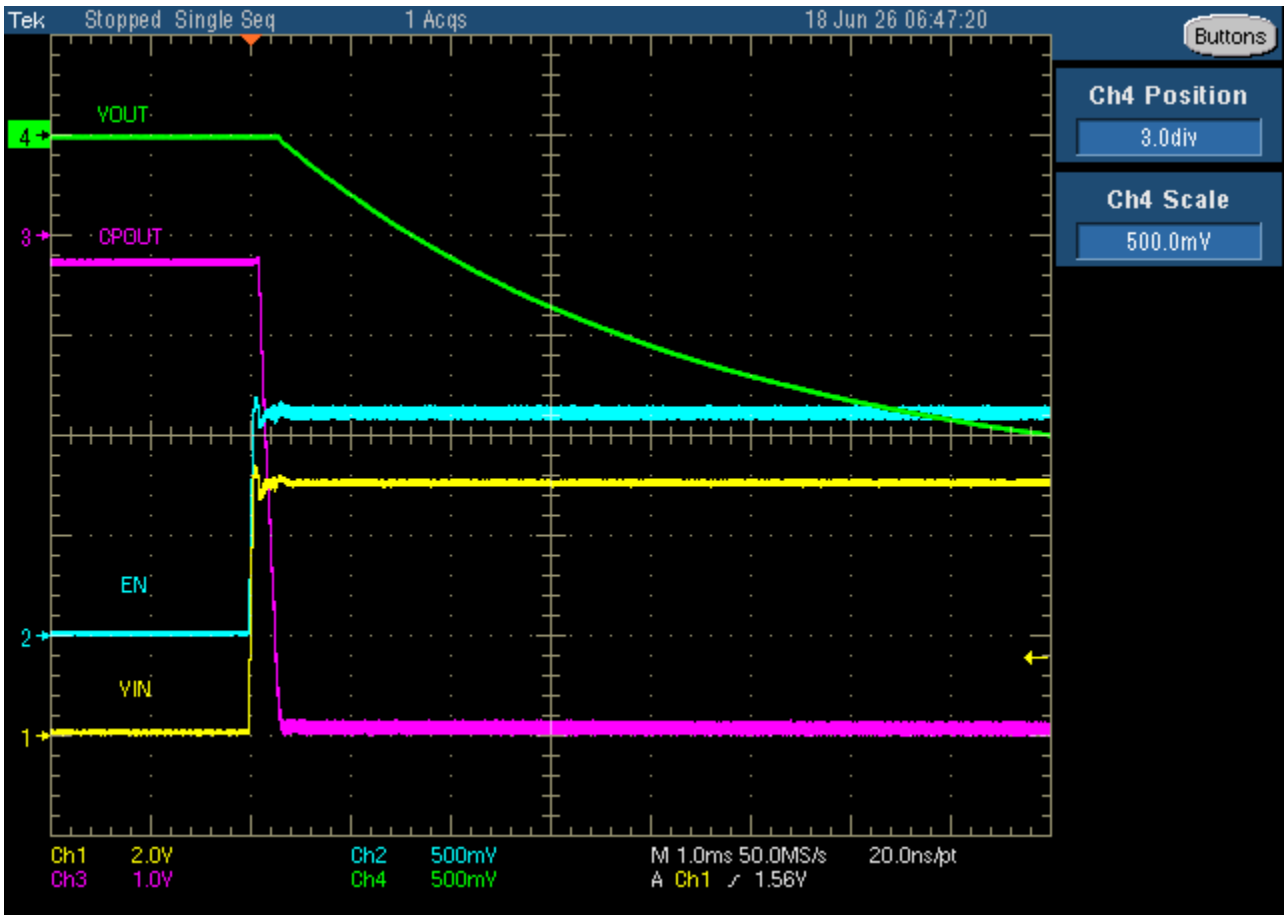


Figure 10-10. TPS7H1302 Startup

10.5 TPS7H1302 Low Noise Configuration

Both the TPS7H1301 and TPS7H1302 have designated pins for the charge pump output and negative LDO input, pins CPOUT and CPOUTA respectively. For applications seeking to minimize noise from the charge pump, the placement of filter between CPOUT and CPOUTA significantly improves noise performance.

Figure 10-11 shows the placement of filter configured for a cut off frequency of 10MHz.

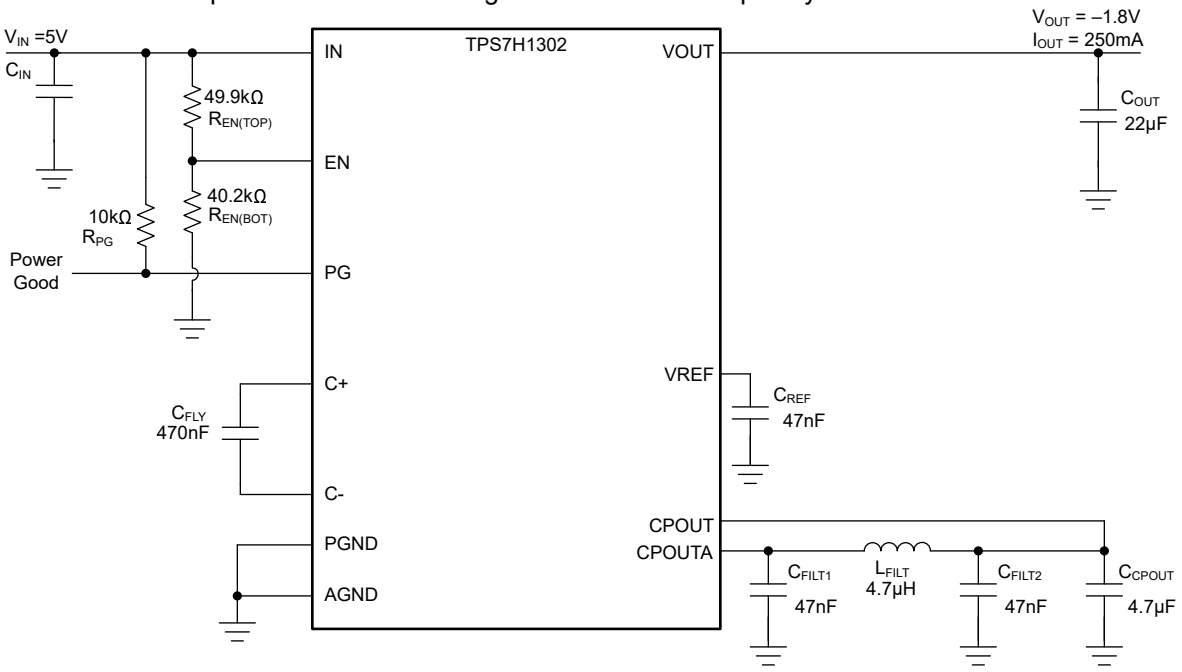


Figure 10-11. Typical Application Low Noise Configuration

10.5.1 Design Requirements TPS7H1302 Low Noise

This example highlights the implementation of a filter at the CPOUT to CPOUTA node by incorporating a filter between the charge pump output and negative LDO input greatly reduces the amount noise the LDO needs to attenuate. For applications powering the DAC39RF22-SEP, the base configuration (Figure 10-9) does not cause any adverse effects to DAC functionality; however further reduction of power supply noise improves DAC performance.

Figure 10-12 show the AC coupled measurements of V_{CPOUT} and V_{OUT}; Figure 10-13 shows the FFT measurement of V_{CPOUT} and V_{OUT}. The switching frequency spike at 1MHz is visible in Figure 10-13 followed by several even order harmonics on both V_{CPOUT} and V_{OUT}.

Table 10-7. Design Parameters

PARAMETER	VALUE
V_{IN}	5V±10%
V_{OUT}	–1.8V
I_{OUT}	250mA
V_{EN}	1.6V

10.5.2 Application Performance Plots

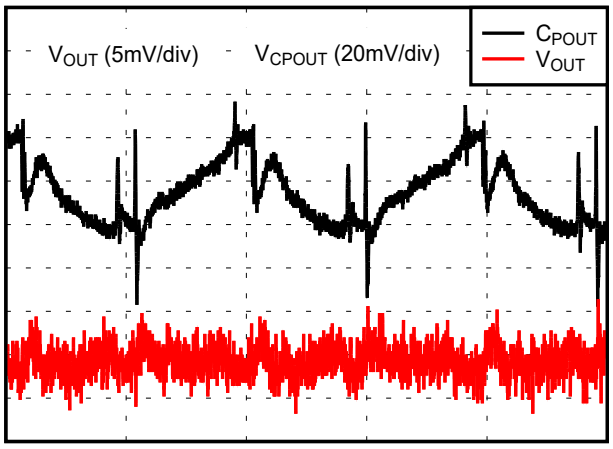


Figure 10-12. TPS7H1302 Output Base Configuration

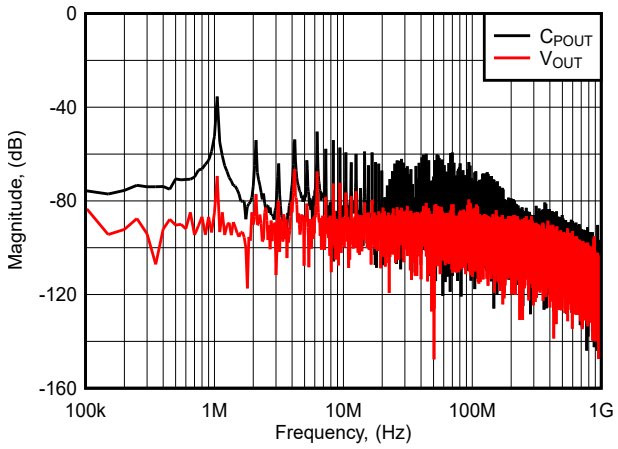


Figure 10-13. TPS7H1302 FFT Base Configuration

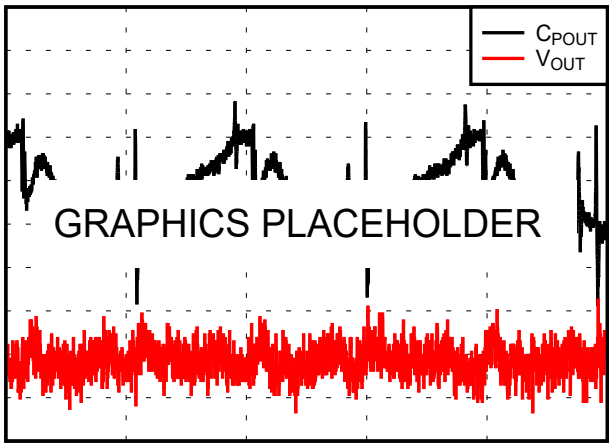


Figure 10-14. TPS7H1302 V_{CPOUT} and V_{OUT} Time Domain

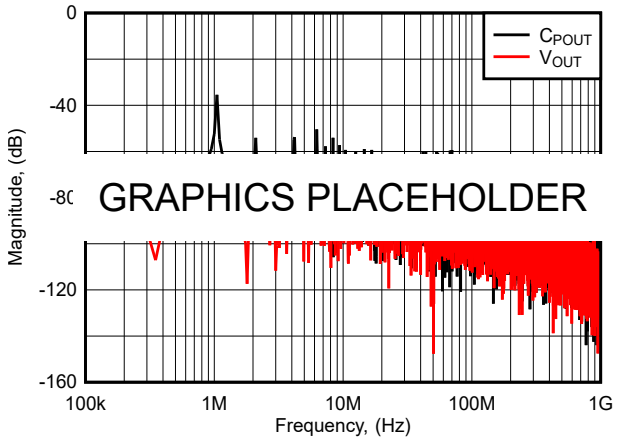


Figure 10-15. TPS7H1302 FFT Low Noise Configuration

10.6 Power Supply Recommendations

The TPS7H1301 and TPS7H1302 are designed to operate from an input voltage supply range between 3V and 6.3V. This input supply must be well regulated and capable of supplying the required input current. If the input supply is located far from the TPS7H1301/2, additional bulk capacitance can be required.

10.7 Layout

10.7.1 Layout Guidelines

Apply the following PCB layout practices for the TPS7H1301 and TPS7H1302:

- Place C_{IN} on the top layer (same layer as the TPS7H130x) and as close as possible to the device. Connecting the input capacitor through short, wide traces to both the VIN and GND pins reduces the inductive voltage spikes that occur during switching, which cause voltage spikes on the VIN line.
- Place C_{CPOUT} on the top layer (same layer as the TPS7H130x) and as close as possible to the VOUT and GND pins. The returns for both C_{IN} and C_{CPOUT} must come together at one point, as close as possible to the GND pin. Connecting C_{CPOUT} through short, wide traces reduces the series inductance on the CPOUT, CPOUTA and GND pins that can cause additional noise and voltage spiking on CPOUT and GND lines.

For best performance C_{CPOUT} must connect back to the thermal pad of the device. Isolation of CPOUT and CPOUTA from the thermal pad is permissible; however, this practice introduces additional noise.

- Place C_{FLY} on top layer (same layer as the TPS7H130x) and as close as possible to the device. Connect the flying capacitor through short, wide traces to both the C+ and C– pins.
- Place COUT on the top layer (same layer as the TPS7H130x) and as close to the VOUT pin as possible.
- Place the output voltage feedback resistors on the top layer (same layer as TPS7H1301) and as close as possible to the respective VFB pin. For best performance the ground connection of R_{BOT} must connect back to the GND connection.
- Connections using long trace lengths, narrow trace widths, or connections through vias for VIN, CPOUT, C_{FLY}, and VOUT must be avoided. These add parasitic inductance and resistance that results in inferior performance, especially during transient conditions.

10.7.2 Layout Example

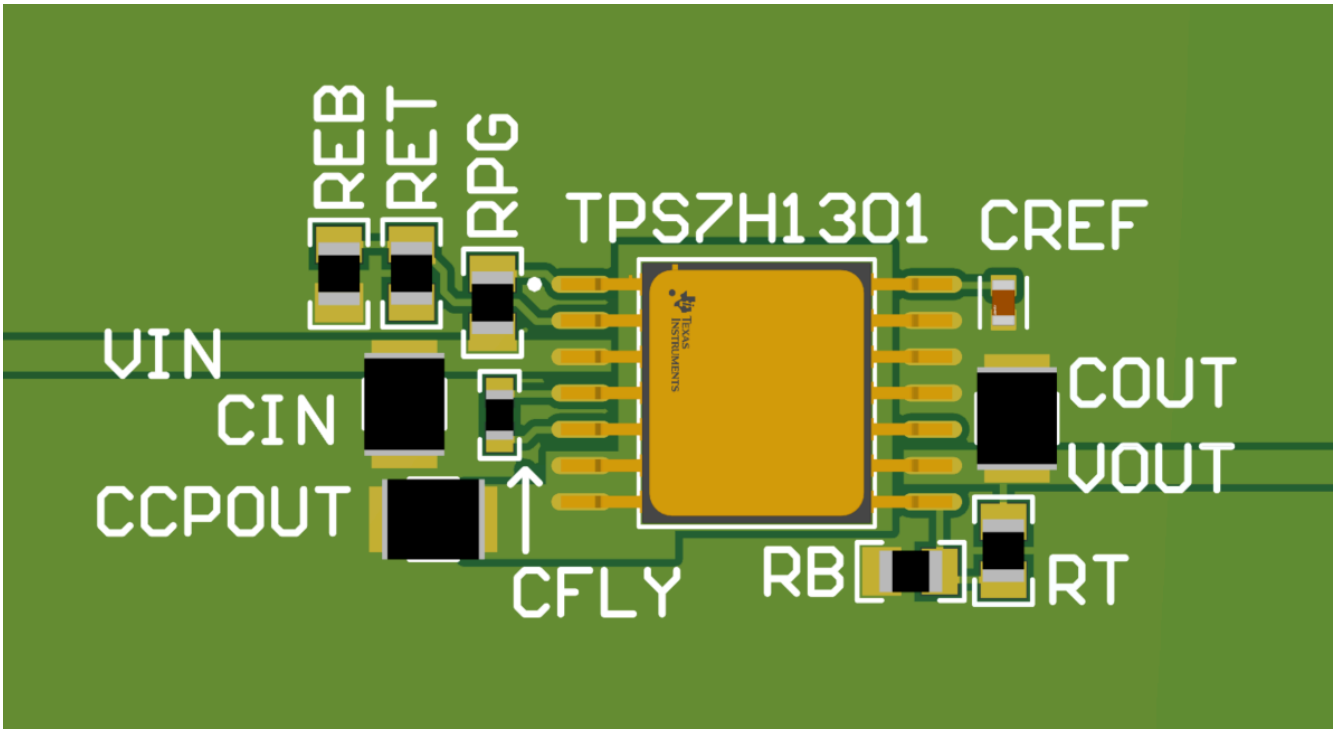


Figure 10-16. TPS7H1301 Layout Example

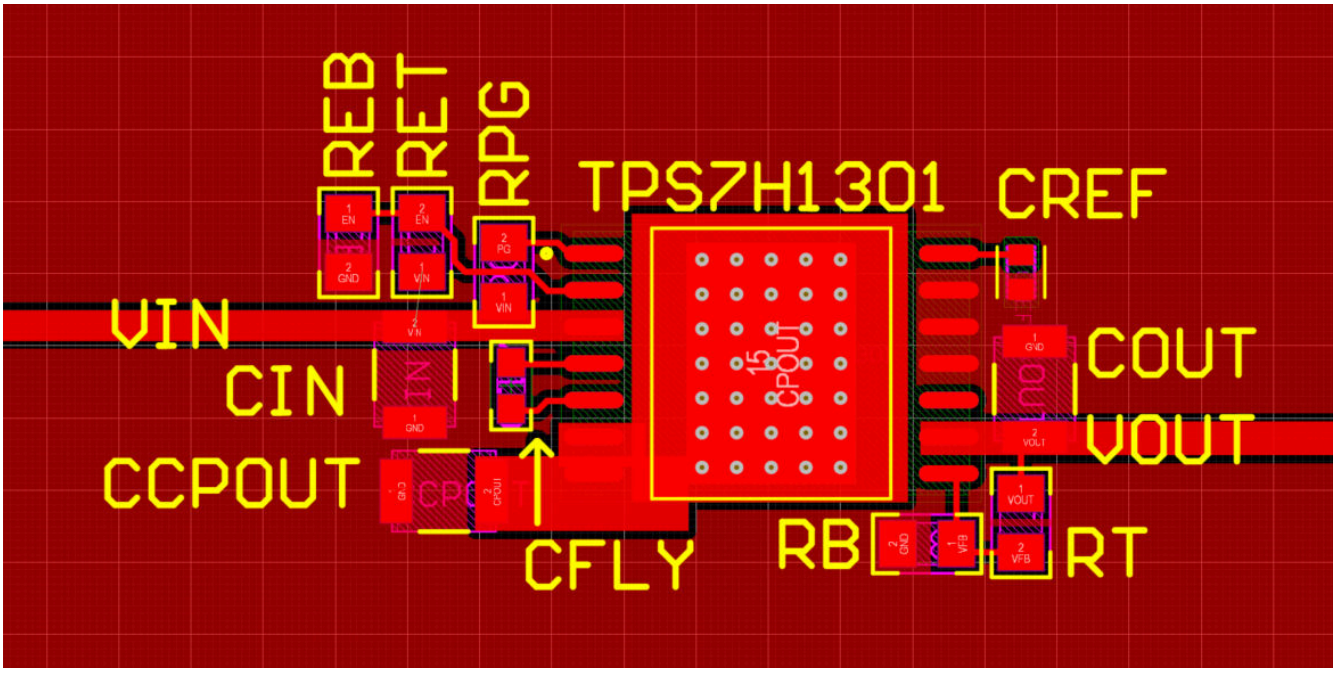


Figure 10-17. TPS7H1301 Layout Example

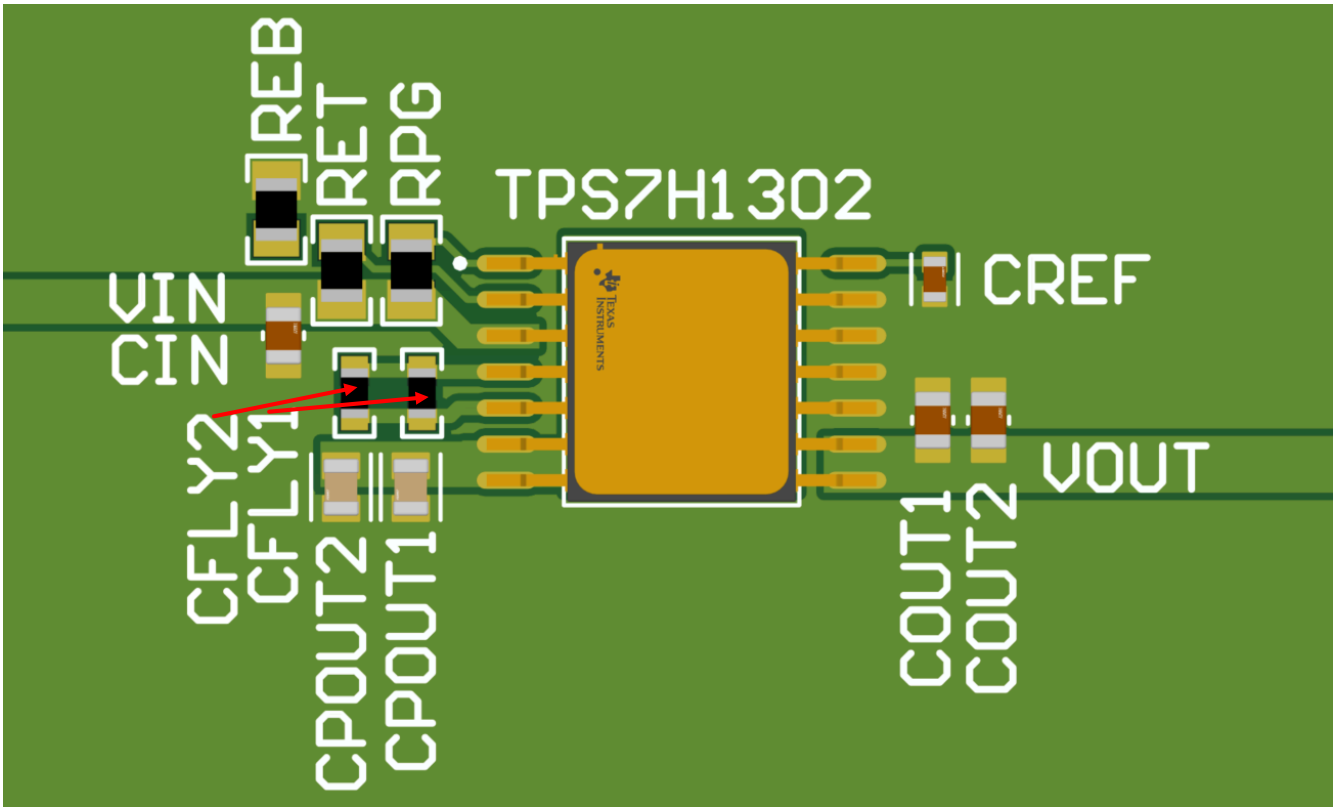


Figure 10-18. TPS7H1302 Layout Example

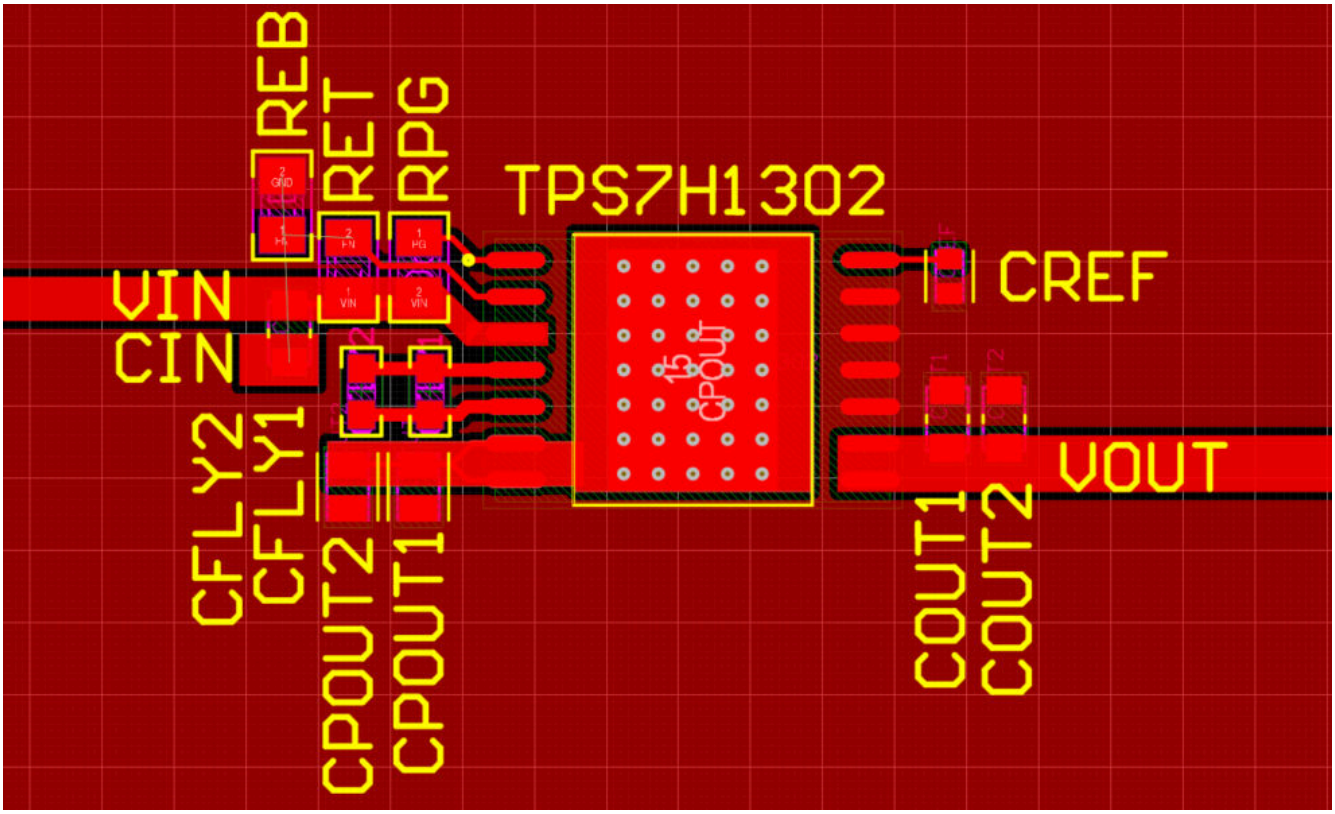


Figure 10-19. TPS7H1302 Layout Example

11 Device and Documentation Support

11.1 Device Support

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, TPS7H1301EVM-CVAL Evaluation Module (EVM)
- Texas Instruments, TPS7H1302EVM-CVAL Evaluation Module (EVM)
- Texas Instruments, TPS7H1301 total ionizing dose (TID) radiation report
- Texas Instruments, TPS7H1301 single event effects (SEE) radiation report
- Texas Instruments, TPS7H1301 neutron displacement damage (NDD) radiation report
- Defense Logistics Agency (DLA), Standard Microcircuit Drawing, 5962R24215

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.5 Trademarks

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11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Revision History

Changes from Revision * (March 2026) to Revision A (August 2026)	Page
• Updated orderable part numbers 5962R2421501VXC and TPS7H1301HBL/EM from Advance Information to Production Data	1
• Updated typical application schematic for clarity	1
• Updated TPS7H1301-SP from Advance Information to Production Data	3
• Updated TPS7H1302 from Product Preview to Advance Information	3
• Updated TPS7H1301 and TPS7H1302 pin diagram images layout for ease of comparison	5
• Updated pin aliases in associated figures and pin description for pin 7 (HBL package) and pins 13 and 14 (PWP package) TPS7H1301 and TPS7H1302	5
• Changed the respective pin aliases from "CPOUT" to "CPOUTA"	5
• Updated capacitor connected to VREF to 47nF	5
• Changed pin alias from "IN" to "VIN"	8

- Changed pin alias from "FB" to "VFB". Moved pin alias "VFB" to Input Voltage section....8
- Changed pin aliases from "C1+" and "C1-" to "C+" and C-"....8
- Added pin alias CPOUTA to input voltage 8
- Changed pin alias from "OUT" to "VOUT"....8
- Updated charged device model rating to ±250V....8
- Changed pin alias from "IN" to "VIN"....9
- Added pin alias CPOUTA to input voltage....9
- Added footnotes....9
- Changed pin alias from "OUT" to "VOUT"....9
- Updated various electrical specification and test conditions to align with Production data of the TPS7H1301 and Advance Information for the TPS7H1302....10
- Added efficiency plots....15
- Updated plots re-graphed with modified extents and intervals to provide additional clarity of plot data....15
- Changed value for C_{REF} from 470nF to 47nF....15
- Updated Dropout Current Measurement I_{DO} measurement diagram....20
- Updated load regulation measurement note to include typical load regulation performance in example calculation....20
- Updated detailed description overview to improve clarity for the TPS7H1301 and TPS7H1302....22
- Updated Functional Block Diagrams (FBD) for TPS7H1301 and TPS7H1302 23
- Added thermal pad and new pin alias "CPOUTA" to show negative LDO input....23
- Updated detailed description to improve clarity for internal charge pump operation 25
- Updated Section 9.3.6 description for the TPS7H1302....27
- Updated formatting for clarity....27
- Updated TPS7H1302 accuracy description....27
- Updated formatting for clarity....27
- Updated text for clarity....29
- Updated simplified compensation schematics for the TPS7H1301 and TPS7H1302 to incorporate updated pin aliases....29
- Updated text for clarity....29
- Added additional application examples Parallel TPS7H1301, Typical Configuration TPS7H1302, and a low noise TPS7H1302....32
- Updated guidance on capacitor selection Figure 10-1 32
- Updated Figure 10-1 to reflect pin alias changes....32
- Added additional CFLY sizing guidance....33
- Deleted bypass capacitors at CFLY to ground; small bypass are to be connected from C+ to C-....36
- Added Section 10.3 39
- Added new typical application section to support Advance Information release of the TPS7H1302....44
- Added new design requirements section to support Advance Information for the TPS7H1302....47
- Added layout guidelines and new layout examples for the TPS7H1301 and TPS7H1302....48
- Added guidance for PCB layout....48
- Added TPS7H1302 example layouts....48
- Added link for related documentation to TPS7H1302EVM-CVAL....52

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status	Material type	Package | Pins	Package qty | Carrier	RoHS	Lead finish/Ball material	MSL rating/Peak reflow	Op temp (°C)	Part marking
5962R2421501VXC	Active	Production	CFP (HBL) | 16	1 | Tube	RoHS Exempt	NIAU	N/A for Pkg Type	–55 to 125	5962R2421501VXC
5962R2421502VXC	Preview	Preproduction	CFP (HBL) | 16	1 | Tube	RoHS Exempt	NIAU	N/A for Pkg Type	–55 to 125	5962R2421502VXC
TPS7H1301HBL/EM	Active	Production	CFP (HBL) | 16	1 | Tube	RoHS Exempt	NIAU	N/A for Pkg Type	–55 to 125	TPS7H1301HBL/EM EVAL ONLY
TPS7H1302HBL/EM	Preview	Preproduction	CFP (HBL) | 16	1 | Tube	RoHS Exempt	NIAU	N/A for Pkg Type	–55 to 125	TPS7H1302HBL/EM EVAL ONLY

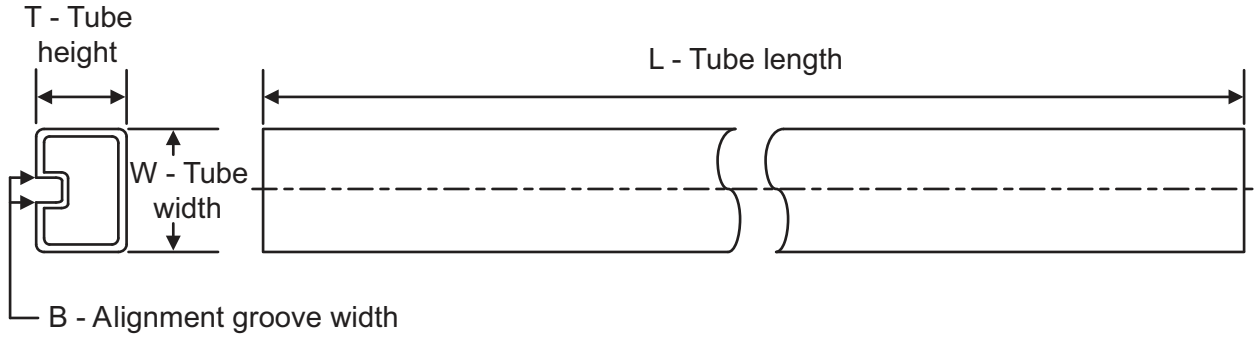
OTHER QUALIFIED VERSION OF TPS7H1301-SP, TPS7H1302-SP:

- Space: TPS7H1301-SP, TPS7H1302-SP

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

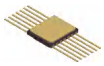
13.1 Tube Information



Device	Package Type	Package Name	Pins	SPQ	L (mm)	W (mm)	T (mm)	B (mm)
5962R2421501VXC	CFP	HBL	14	25	506.98	26.16	6220	NA
5962R2421502VXC	CFP	HBL	14	25	506.98	26.16	6220	NA
TPS7H1301HBL/EM	CFP	HBL	14	25	506.98	26.16	6220	NA
TPS7H1302HBL/EM	CFP	HBL	14	25	506.98	26.16	6220	NA

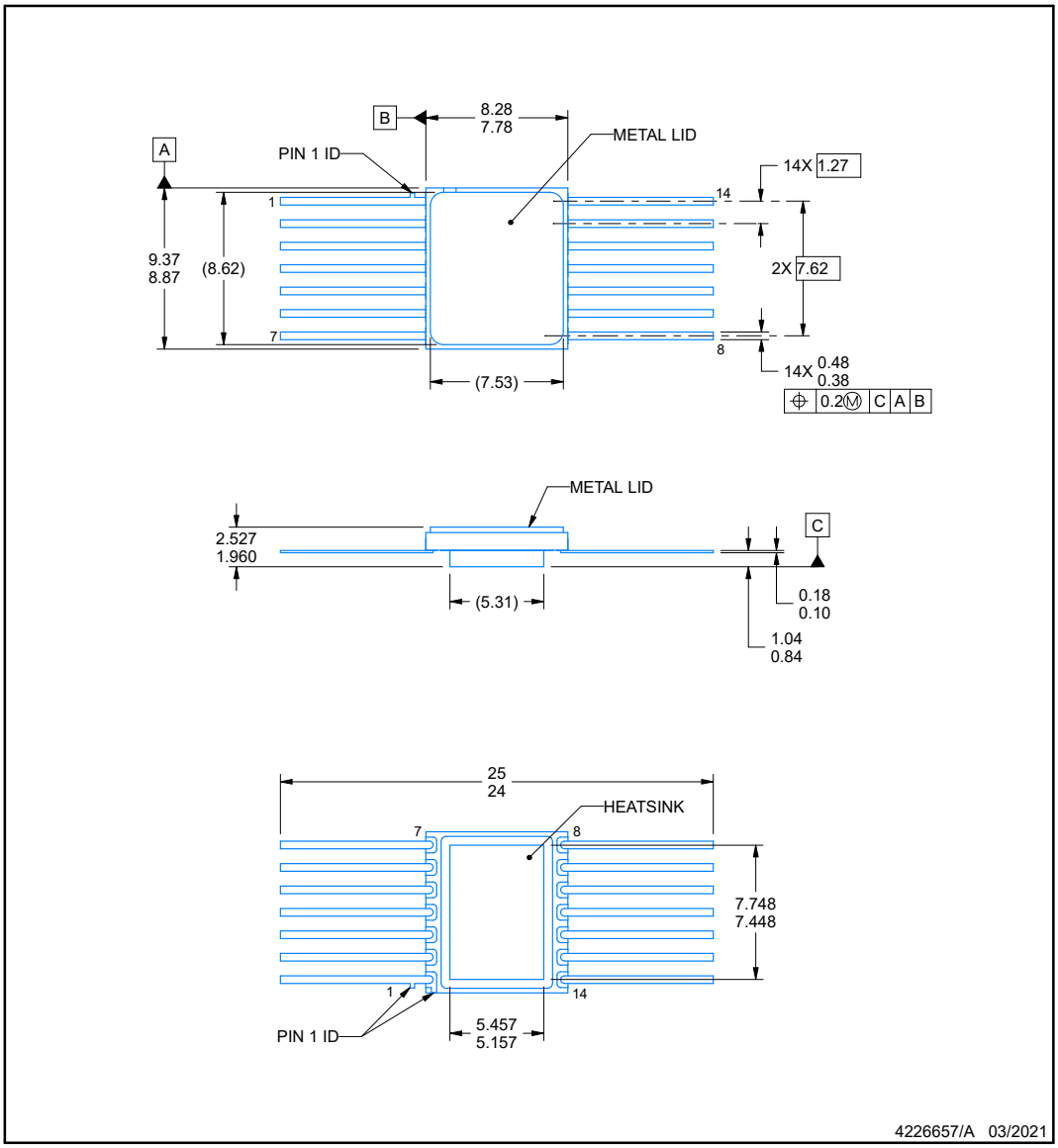
PACKAGE OUTLINE

HBL0014A



CFP - 2.527 mm max height

CERAMIC DUAL FLATPACK



NOTES:

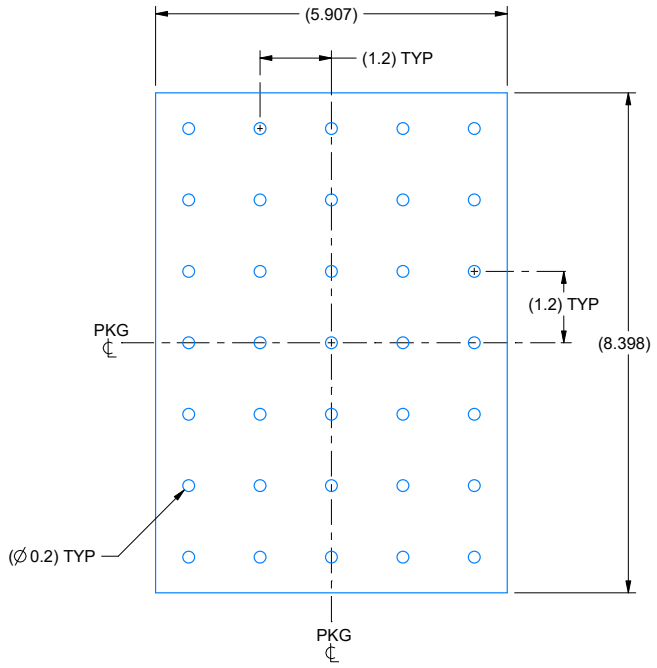
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a metal lid. Lid is connected to Heatsink and pin 6
4. The terminals are gold plated.

EXAMPLE BOARD LAYOUT

HBL0014A

CFP - 2.527 mm max height

CERAMIC DUAL FLATPACK



HEATSINK LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:10X

4226657/A 03/2021

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