TPS7H4203-SP and TPS7H4203-SEP 10V to 38V Input 3A Radiation-Hardened Synchronous Buck Converter

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1 Features

- Total ionizing dose (TID) characterized
  - Radiation hardness assurance (RHA) availability of up to 100krad(Si)
- Single-event effects (SEE) characterized
  - Single-event latchup (SEL), single-event burnout (SEB), and single-event gate rupture (SEGR) immune up to linear energy transfer (LET) = 75MeV-cm^2/mg
  - Single-event functional interrupt (SEFI) and single-event transient (SET) characterized up to LET = 75MeV-cm^2/mg
- Input voltage range from 10V to 38V
- 3A maximum output current
- High efficiency (typical values for PVIN = 28V, V_{OUT} = 12V, f_{SW} = 250kHz)
  - 91.8% at 3A
- Integrated 214mΩ (HS) and 100mΩ (LS) MOSFETs (typ. at T_A = 25°C)
- Flexible switching frequency options:
  - 100kHz to 500kHz, accurate (±10%), adjustable internal oscillator
  - 100kHz to 500kHz external sync capability
  - SYNC pin can be configured as an output with 180° out of phase at f_{SW} = 250kHz to parallel 2 devices
- 1V ± 1% voltage reference over line, temperature, and radiation
- Monotonic start-up into prebiased outputs
- Adjustable slope compensation and soft-start
- Adjustable input enable and power-good output for power sequencing
- Power-good output monitor for undervoltage and overvoltage
- Overvoltage protection
- Supports inverting buck-boost topology
- Plastic packages outgas tested per ASTM E595
- Available in military (–55°C to 125°C) temperature range

2 Applications

- Space satellite point of load supply
- Satellite electrical power systems (EPS)
- Communications payload
- Radar imaging payload
- Radiation-hardened power supplies

3 Description

The TPS7H4203 is a 10V to 38V, 3A synchronous buck converter optimized for use in a space environment. The peak current mode converter offers high efficiency, excellent transient performance, and a lower component count.

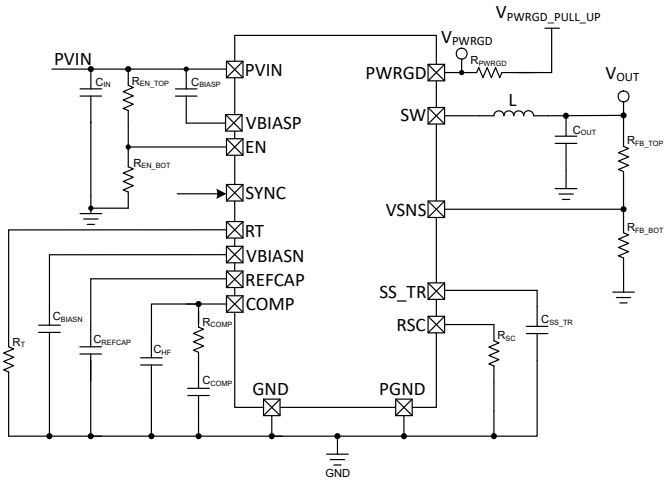
The TPS7H4203 wide voltage range allows it to function as a point-of-load regulator, converting power directly from 28V or 12V rails. The SS_TR pin controls the output voltage startup ramp, while the EN and PWRGD pins enable power sequencing capabilities.

Two devices can be configured in parallel without an external clock for increased current capabilities. Additionally, the device includes configurable loop compensation and slope compensation. Internal protection for overload, overvoltage, and over temperature are also incorporated.

Device Information

PART NUMBER(1)	GRADE	PACKAGE(4)
5962R2521102VXC(2)	QMLV-RHA	24-pin ceramic 7.84mm × 19.28mm
TPS7H4203HLA/EM(2)	Engineering sample	
5962R2521101PYE(2)	QMLP-RHA	28-pin plastic 4.4mm × 9.7mm Mass = 128.4mg
TPS7H4203MPWPTSEP(3)	SEP	

(1) For additional information view the Device Comparison Table
(2) Product preview
(3) Advanced information
(4) The body size (length × width) is a nominal value and does not include pins



Simplified Application

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4 Device Comparison Table

GENERIC PART NUMBER	RADIATION RATING(1)	GRADE(2)	PACKAGE	ORDERABLE PART NUMBER
TPS7H4203-SP	TID of 100krad(Si) RLAT, DSEE free to 75MeV-cm^2/mg	QMLV-RHA	24-pin CFP HLA	5962R2521102VXC(4)
		QMLP-RHA	28-pin HTSSOP PWP	5962R2521101PYE(4)
	None	Engineering model(3)	24-pin CFP HLA	TPS7H4203HLA/EM(4)
TPS7H4203-SEP	TID of 50krad(Si) RLAT, DSEE free to 43MeV-cm^2/mg	Space Enhanced Plastic	28-pin HTSSOP PWP	TPS7H4203MPWPTSEP(5)
SN0030HLA	N/A	Mechanical "dummy" package (no die)	24-pin CFP HLA	SN0030HLA(4)

(1) TID is total ionizing dose and DSEE is destructive single event effects. Additional information is available in the associated TID reports and SEE reports for each product.
(2) For additional information about part grade, view TI Part Ratings.
(3) These units are intended for engineering evaluation only. They are processed to a non-compliant flow (such as no burn-in and only 25°C testing). These units are not suitable for qualification, production, radiation testing, or flight use. Parts are not warranted as to performance over temperature or operating life.
(4) Product preview.
(5) Advanced information.

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5 Pin Configuration and Functions

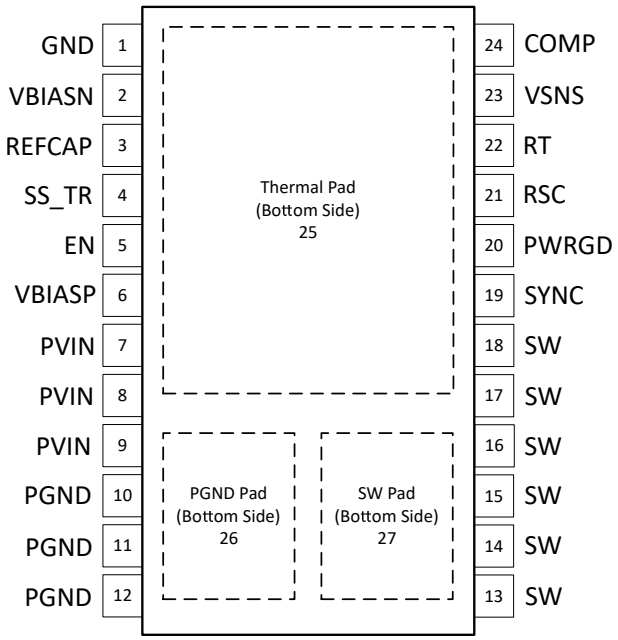


Figure 5-1. HLA Package, 24-Pin CFP (Top View)

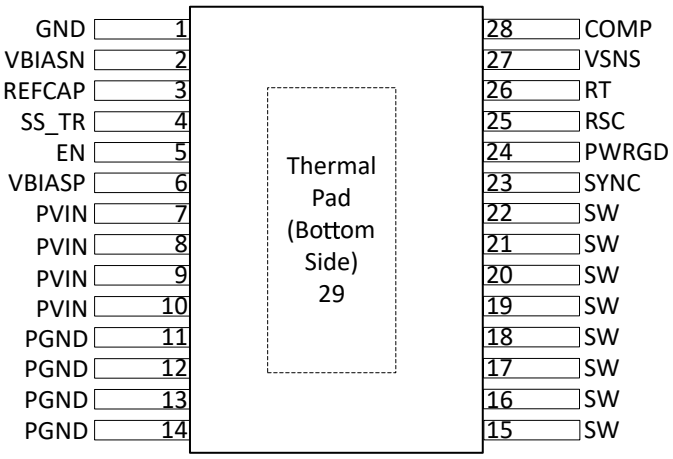


Figure 5-2. PWP Package, 28-Pin HTSSOP (Top View)

Table 5-1. Pin Functions

PIN			I/O[1]	DESCRIPTION
NAME	CFP (30)	HTSSOP (28)		
GND	1	1	—	Ground. Return for control circuitry.
VBIASN	2	2	O	Regulator output capacitor pin. A 470pF capacitor must be placed between this pin and GND. The output voltage, is nominally 6.3V. Do not load this pin with any additional external circuitry.
REFCAP	3	3	O	Reference capacitor pin. A 1nF external capacitor is required for the internal bandgap reference. The voltage, V_{REFCAP}, is nominally 1.2V. Do not connect external circuitry to this pin.
SS_TR	4	4	I/O	Soft-start and tracking. An external capacitor connected between this pin and GND slows down the rise time of the internal reference during start-up. It can also be used for tracking and sequencing. Do not leave this pin floating.
EN	5	5	I	Enable. Driving this pin to logic high enables the device; driving the pin to logic low disables the device. Use a resistor divider from PVIN to GND to externally set the device turn-on level, if desired. The maximum voltage this pin can tolerate is 5.5V.
VBIASP	6	6	I/O	High side (PMOS) FET driver voltage decoupling capacitor. A 470pF capacitor must be placed between this pin and PVIN. Do not load this pin with any additional external circuitry.
PVIN	7–9	7–10	I	Power stage and I.C. input voltage. Power for the output stage of the switching regulator and all the internal circuitry. Connect the external decoupling capacitors as close to the pins as possible.
PGND	10–12	11–14	—	Power stage ground. Return for low-side power MOSFET. Connect to GND on the PCB.
SW	13–18	15-22	O	Switching node pins. Switch node output to connect to the external inductor filter.
SYNC	19	23	O	Synchronization pin. This pin is used as an output clock sync pin (to synchronize other devices or aid in device monitoring) or an input for an external clock. SYNC outputs a clock signal 180 degrees out of phase with the switching frequency when RT is floating at a fixed frequency of 250kHz.

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Table 5-1. Pin Functions (continued)

PIN			I/O[1]	DESCRIPTION
NAME	CFP (30)	HTSSOP (28)		
PWRGD	20	24	I/O	Power Good pin. This is an open-drain pin. Connect this pin through a pull-up resistor to the desired logic level (≤ 5.5V). PWRGD is in a high impedance state when the output voltage is within 5% (typ) of its programmed value. PWRGD is in a low impedance state when the output voltage is outside 8% (typ) of its programmed value or when there is a fault condition.
RSC	21	25	I/O	Slope compensation pin. A resistor from RSC to GND sets the desired slope compensation.
RT	22	26	I	A resistor connected between RT and GND sets the switching frequency of the converter. The switching frequency range is 100kHz to 500kHz. If RT is left floating the SYNC pin becomes an output clock with 180 degrees out of phase with the switching frequency. When using an external clock in SYNC mode, set the RT resistor value to match the SYNC frequency.
VSNS	23	27	I/O	Inverting input of the transconductance (gm) error amplifier.
COMP	24	28	O	Compensation pin. Error amplifier output and input to the PWM current comparator. Connect frequency compensation components to this pin.
THERMAL PAD	25	29	—	Thermal pad internally connected to GND. Connect to a large ground plane for thermal dissipation. While it is recommended to electrically connect to GND or PGND; it can be left electrically disconnected if desired.
PGND PAD	26	N/A	—	Power ground pad. This pad is used to provide a low electrical resistance path for the low-side power MOSFET to PGND. It must be connected to the PGND pins.
SW PAD	27	N/A	O	Switch node. This pad is used to provide a low electrical resistance path for the switching current. It must be connected to the SW pins.
Metal lid	Lid	N/A	—	Internally connected to GND.

(1) I = Input, O = Output, I/O = Input or Output, — = Other

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6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
Input voltage	PVIN, SW, VBIASP	–0.3	50	V
	PWRGD, VSNS, EN, RT, SYNC, COMP, RSC, SS_TR	–0.3	6	
	VBIASN	-0.3	8	
	REFCAP	–0.3	2	
Output voltage	SW	–1	50	V
	SW (3)	–3	50	
	REFCAP	–0.3	2	
Vdiff	GND to exposed thermal pad	–0.2	0.2	V
Source current	SW		Current limit	A
	PGND		Current limit	
	RT, RSC		100	µA
	COMP		300	
Sink current	PVIN		Current limit	A
	SW		Current limit	
	PGND		Current limit	
	COMP		300	µA
	PWRGD		5	mA
Operating junction temperature, T_J		–55	150	°C
Storage temperature, T_{stg}		–65	150	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to GND
(3) When the transient time is less or equal than 10ns

6.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted) (1)

		MIN	NOM	MAX	UNIT
Input voltage	PVIN (Electrical)	10		42	V
	PVIN (DSEE-free)(2)	10		38	
Input voltage	PWRGD, VSNS, EN, RT, SYNC, COMP, RSC, SS_TR	0		5.5	V
Output voltage	SW	0		38	V
	SS_TR	0	1.5	2	
	COMP	0		2.1	
	VBIASP	PVIN-7.6	PVIN-7	PVIN-5.7	
	VBIASN		6.3	7.5	
	REFCAP		1.2	1.3	
Source current	SW_{AVG}	0		3	A
	RT, RSC			100	µA
	COMP			200	
Sink current	PWRGD	0		2	mA
	COMP			200	µA
Soft Start Capacitance	C_{SS_TR}			220	nF
Inductor Ripple Current	Δi_L	400			mA
Operating junction temperature	T_J	–55		125	°C
Input voltage slew rate	SR_{PVIN}	0.0001		0.1	V/µs

(1) All voltages values are with respect to GND.
(2) With LET ≤ 75MeV×cm^2/mg and diode from SW to PGND. See SEE report for full details.

6.4 Thermal Information

THERMAL METRIC(1)		TPS7H4203 CFP HLA 30 PINS	TPS7H4203 HTSSOP PWP 28 PINS	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	21.5	24.6	℃/W
$R_{\theta JC_TOP}$	Junction-to-case (top) thermal resistance	4.3	15.5	
$R_{\theta JC_BOT}$	Junction-to-case (bottom) thermal resistance	0.33	1.1	
$R_{\theta JB}$	Junction-to-board thermal resistance	6.3	6.4	
ψ_{JT}	Junction-to-top characterization parameter	1.2	0.2	
ψ_{JB}	Junction-to-board characterization parameter	6.1	6.4	

(1) For more information about the traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report (SPRA953)

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6.5 Electrical Characteristics

Over 10V ≤ PVIN ≤ 38V, open loop configuration, over operating temperature range T_A = –55°C to 125°C, typical values are at T_A = 25°C, includes group E radiation testing at T_A = 25°C; unless otherwise noted

PARAMETER		TEST CONDITIONS		SUB-GROUP(1)	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
V_{UVLOR_PVIN}	PVIN internal UVLO rising threshold	I_{OUT} = 0A, V_{EN} = 1V		1, 2, 3	9.21	9.48	9.74	V
V_{UVLOF_PVIN}	PVIN internal UVLO falling threshold	I_{OUT} = 0A, V_{EN} = 1V		1, 2, 3	8.44	8.78	9.15	
I_{SHDN_PVIN}	PVIN shutdown supply current	V_{EN} = 0V		1, 2, 3		0.41	0.53	mA
I_{Q_PVIN}	PVIN operating quiescent current (non switching)	V_{EN} = 1V, VSNS = 1.2V		1, 2, 3		6.28	8.1	
ENABLE								
V_{EN_RISING}	Enable rising threshold (turn-on)			1, 2, 3	573	605	633	mV
$V_{EN_FALLING}$	Enable falling threshold (turn-off)			1, 2, 3	475	502	525	
$t_{EN_PVIN_RISING_PD}$	Enable propagation delay when: EN, PVIN are tied together.	EN high before PVIN > V_{UVLOR_PVIN} to SS_TR high, C_{SS_TR} = 1nF	See Figure 7-1	1, 2, 3		398	700	µs
$t_{EN_RISING_PD}$	Enable propagation delay	EN high to SS_TR high when PVIN>$V_{UVLOR_PVIN(MAX)}$ for at least $t_{EN_PVIN_RISING_PD}$, C_{SS_TR} = 1nF	See Figure 7-2	1, 2, 3		310	420	
$t_{EN_FALLING_PD}$	Disabled propagation delay	EN low to SS_TR low, C_{SS_TR} = 1nF	See Figure 7-3	1, 2, 3		8.3	15	
I_{EN_LKG}	Enable input leakage current	V_{EN} = 5.5V		1, 2, 3			350	nA
VOLTAGE REFERENCE								
V_{REF}	Internal voltage reference (including error amplifier V_{IO})	See(2)		1, 2, 3	0.99	1	1.01	V
V_{REFCAP}	REFCAP voltage			1, 2, 3		1.2		
VBIASN	Internal linear reference voltage			1, 2, 3	5	6.3	7.3	
ERROR AMPLIFIER								
V_{COMP_OV}	V_{COMP} to skip high side turn on			1, 2, 3		739		mV
I_{VSNS_LKG}	VSNS input leakage current	VSNS = 1V, V_{COMP} = 1.1V		1, 2, 3		0.32	100	nA
gm_{EA}	Error amplifier transconductance	–10µA < I_{COMP} < 10µA, V_{COMP} = 1.1V		9,10,11	175	252	425	µS
EA_{RO}	Error amplifier output resistance			1		23		MΩ
$EA_{DC\text{-}GAIN}$	Error amplifier DC gain	VSNS = 1V		1, 2, 3		5800		V/V
EA_{ISRC}	Error amplifier source	V_{COMP} = 1.1V, ± 100mV input overdrive		1, 2, 3		25	40	µA
EA_{ISNK}	Error amplifier sink					24	40	
EA_{BW}	Error amplifier bandwidth			1		2.56		MHz
gm_{PS}	Power stage transconductance	0.9V ≤ V_{COMP} ≤ 1V		1, 2, 3	8	10	12	S

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6.5 Electrical Characteristics (continued)

Over 10V ≤ PVIN ≤ 38V, open loop configuration, over operating temperature range T_A = –55°C to 125°C, typical values are at T_A = 25°C, includes group E radiation testing at T_A = 25°C; unless otherwise noted

PARAMETER		TEST CONDITIONS		SUB-GROUP(1)	MIN	TYP	MAX	UNIT
OVERCURRENT PROTECTION								
I_{OC}	High-side switch overcurrent threshold	See Figure 8-18		1, 2, 3	6.1	7.2	8.5	A
t_{OC}	High-side current limit fault time	See Figure 8-18		1, 2, 3		44		µs
$COMP_{SHDN}$	COMP shutdown voltage	See Figure 8-19		1, 2, 3	1.65	2	2.35	V
$I_{OC_LS_SNK}$	Low-side switch overcurrent sinking threshold	Slew rate = 1.27mA/µs		1, 2, 3	1.3	2	2.6	A
$t_{PD_LS_SNK}$	Low-side sinking current limit propagation delay			1, 2, 3		360		ns
SOFT START AND TRACKING								
I_{SS_TR}	Soft start charge current	0.5V ≤ V_{SS_TR} ≤ 1V		1, 2, 3	8	11	13	µA
$R_{SS_TR_DISCHARGE}$	Soft start discharge pull-down resistor	V_{SS_TR} = 50mV		1, 2, 3		72	103	Ω
$SS_TR_{SHDN_TIME}$	Active soft start pull down time after $COMP_{SHDN}$(3) event or EN=low	C_{SS_TR} = 1nF from 90% falling to 10% rising in V_{SS_TR}, See Figure 8-19		1, 2, 3	190	316	450	µs
SLOPE COMPENSATION								
SC	Slope compensation	R_{SC} = 505kΩ		1		0.21		A/µs
		R_{SC} = 200kΩ		1		0.5		
		R_{SC} = 96.5kΩ		1		1		
		R_{SC} = 80.6kΩ		1		1.17		
MINIMUM ON, OFF AND DEAD TIME								
t_{ON_MIN}	Minimum on time	50% of rising edge to 50% of falling edge of V_{SW}, I_{SW} = 300mA		9, 10, 11		254	380	ns
t_{OFF_MIN}	Minimum off time	50% of falling edge to 50% of rising edge of V_{SW}		9, 10, 11		211	305	
t_{DEAD}	Dead time	PVIN=28V		9, 10, 11		35		
SWITCHING FREQUENCY AND SYNCHRONIZATION								
f_{SW}	Internally programmed switching frequency	R_{RT} = open		4, 5, 6	200	250	320	kHz
f_{SW}	RT externally programmed switching frequency	R_{RT} = 97.6kΩ		4, 5, 6	90	100	110	
		R_{RT} = 37.9kΩ		4, 5, 6	225	250	275	
		R_{RT} = 18.7kΩ		4, 5, 6	450	500	550	
t_{SYNC_DLY}	SYNC to SW delay	See Internal to External Clock Switchover and External to Internal Clock Switchover		9, 10, 11		320	400	ns
V_{SYNC_VIH}	SYNC input high			1, 2, 3	4.5			V
V_{SYNC_VIL}	SYNC input low			1, 2, 3			0.6	V
$SYNC_{PH}$	$f_{SW_PRIMARY}$ to $f_{SW_SECONDARY}$ phase shift	RT unpopulated		4, 5, 6		180		°
f_{SYNC}	SYNC input frequency range			4, 5, 6	100		500	kHz
D_{SYNC}	SYNC input duty cycle range	external clock duty cycle		4, 5, 6	40%		60%	
$t_{CLK_I_E}$	Internal clock to external clock detection time	RT populated	See Internal to External Clock Switchover	9, 10, 11		1	2	× T_{SYNC}
$t_{CLK_E_I}$	External clock to internal clock detection time	RT populated	See External to Internal Clock Switchover	9, 10, 11		2	4	× T_{OSC}

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6.5 Electrical Characteristics (continued)

Over 10V ≤ PVIN ≤ 38V, open loop configuration, over operating temperature range T_A = –55°C to 125°C, typical values are at T_A = 25°C, includes group E radiation testing at T_A = 25°C; unless otherwise noted

PARAMETER		TEST CONDITIONS		SUB-GROUP(1)	MIN	TYP	MAX	UNIT
FOLDBACK								
$V_{TH_FOLDBACK_RISING}$	VSNS rising voltage threshold to be out of foldback			1, 2, 3		271		mV
$V_{TH_FOLDBACK_FALLING}$	VSNS falling voltage threshold to be in foldback			1, 2, 3		248		mV
$f_{SW_DIVIDE_BY_2_OR_4}$	Switching frequency to divide by 2 or 4 during foldback.			4, 5, 6		167		kHz
POWER GOOD								
$PWRGD_{UV_FAULT}$	VSNS falling threshold (fault)	See Figure 8-3		1, 2, 3	90%	92%	95%	x V_{REF}
$PWRGD_{UV_GOOD}$	VSNS rising threshold (good)			1, 2, 3	93%	95%	98%	x V_{REF}
$PWRGD_{OV_FAULT}$	VSNS rising threshold (fault)	See Figure 8-4		1, 2, 3	104%	108%	111%	x V_{REF}
$PWRGD_{OV_GOOD}$	VSNS falling threshold (good)			1, 2, 3	102%	105%	107%	x V_{REF}
I_{PWRGD_LKG}	Output open high leakage	COMP tied VSNS , V_{PWRGD} = 5.5V		1, 2, 3			550	nA
V_{PWRGD_VOL}	Power good output low	I_{PWRGD_SINK} ≤ 2mA		1, 2, 3		116	200	mV
$PVIN_{MIN_PWRGD}$	Minimum PVIN for valid PWRGD output	Measured when V_{PWRGD} ≤ 0.5V at 100µA at PVIN slewrate of 0.1V/µs, See Figure 8-5		1, 2, 3			2.8	V
THERMAL SHUTDOWN								
T_{SD_ENTER}	Thermal shutdown enter temperature	I_{OUT} = 0A				180		°C
T_{SD_EXIT}	Thermal shutdown exit temperature					148		°C
T_{SD_HYS}	Thermal shutdown hysteresis					32		°C
MOSFET								
$R_{DS_ON_HS}$	High-side switch resistance(4)	I_{OUT} = 1A	T_A = –55°C	3		155	210	mΩ
			T_A = 25°C	1		214	320	mΩ
			T_A = 125°C	2		292	380	mΩ
$R_{DS_ON_LS}$	Low-side switch resistance(4)	I_{OUT} = 1A	T_A = –55°C	3		73	90	mΩ
			T_A = 25°C	1		100	124	mΩ
			T_A = 125°C	2		140	180	mΩ

(1) Subgroups are applicable for QML parts. For subgroup definitions, see the Quality Conformance Inspection
(2) Use this V_{REF} value to set the output voltage. Measured in a non-switching configuration as shown in Figure 7-4.
(3) The device does not begin startup until the time constant is satisfied in order to provide proper soft start functionality.
(4) Measured at pins with lead length ≈ 3mm for HLB ceramic package

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6.6 Quality Conformance Inspection

MIL-STD-883, Method 5005 - Group A

SUBGROUP	DESCRIPTION	TEMP (°C)
1	Static tests at	25
2	Static tests at	125
3	Static tests at	–55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	–55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	–55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	–55

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6.7 Typical Characteristics

28-pin HTSSOP (PWP) package, PVIN = 28V, VOUT = 12V, C_{IN} = 81.8µF, C_{OUT} = 132.3µF, C_{SS} = 22nF, L = 27µH (Würth Elektronik Model: 7447709270), T_A = 25°C, unless otherwise noted. The efficiency plots at f_{SW} = 500kHz used an L = 10µH (Würth Elektronik Model: 7447709100)

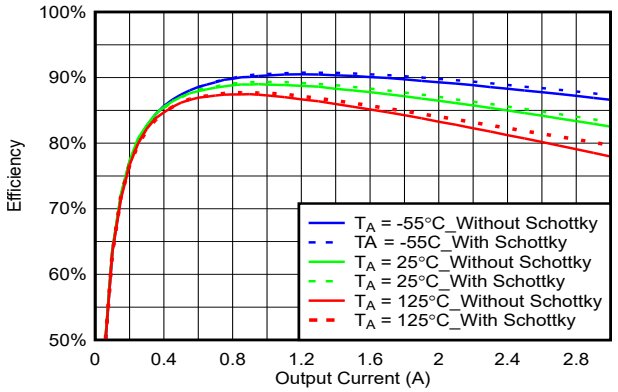


Figure 6-1. Efficiency vs Load Across Temperature With and Without External Schottky Diode at f_{SW} = 100kHz, PVIN = 12V, V_{OUT} = 3V

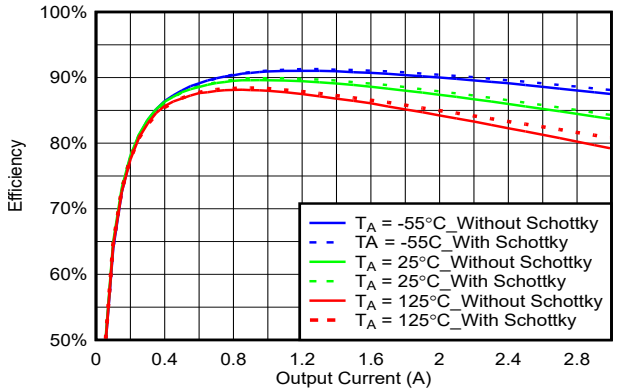


Figure 6-2. Efficiency vs Load Across Temperature With and Without External Schottky Diode at f_{SW} = 100kHz, PVIN = 12V, V_{OUT} = 3.3V

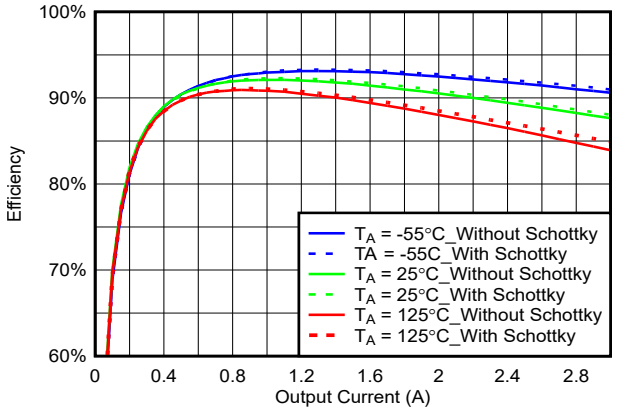


Figure 6-3. Efficiency vs Load Across Temperature With and Without External Schottky Diode at f_{SW} = 100kHz, PVIN = 12V, V_{OUT} = 5V

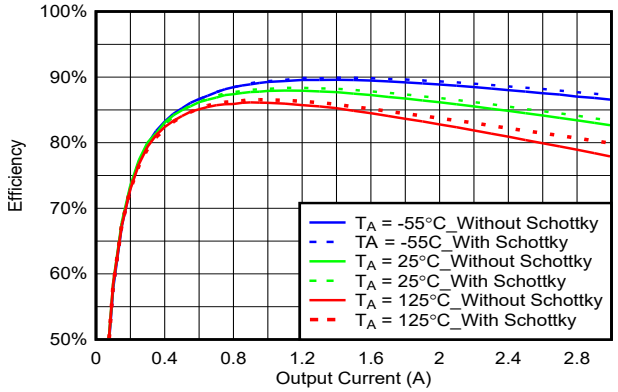


Figure 6-4. Efficiency vs Load Across Temperature With and Without External Schottky Diode at f_{SW} = 100kHz, PVIN = 15V, V_{OUT} = 3V

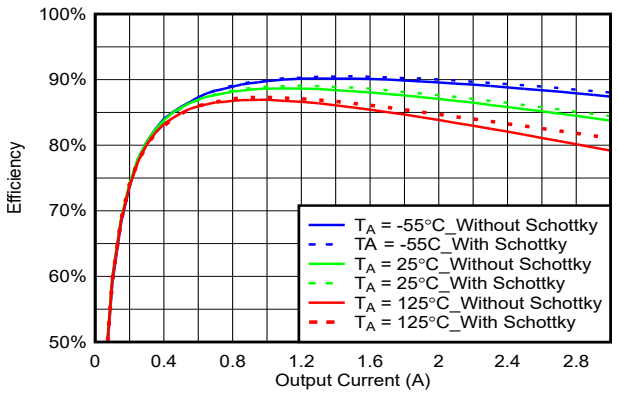


Figure 6-5. Efficiency vs Load Across Temperature With and Without External Schottky Diode at f_{SW} = 100kHz, PVIN = 15V, V_{OUT} = 3.3V

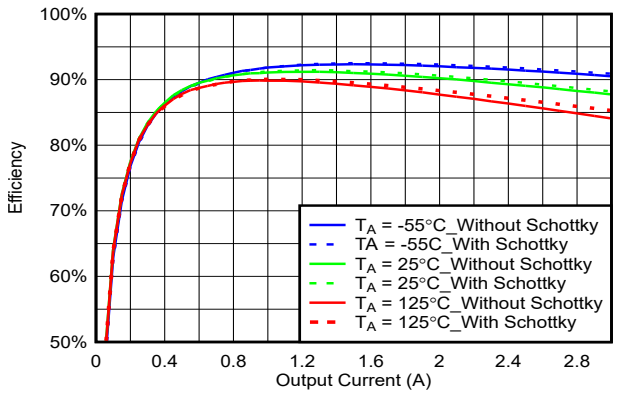


Figure 6-6. Efficiency vs Load Across Temperature With and Without External Schottky Diode at f_{SW} = 100kHz, PVIN = 15V, V_{OUT} = 5V

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6.7 Typical Characteristics (continued)

28-pin HTSSOP (PWP) package, PVIN = 28V, VOUT = 12V, C_{IN} = 81.8µF, C_{OUT} = 132.3µF, C_{SS} = 22nF, L = 27µH (Würth Elektronik Model: 7447709270), T_A = 25°C, unless otherwise noted. The efficiency plots at f_{SW} = 500kHz used an L = 10µH (Würth Elektronik Model: 7447709100)

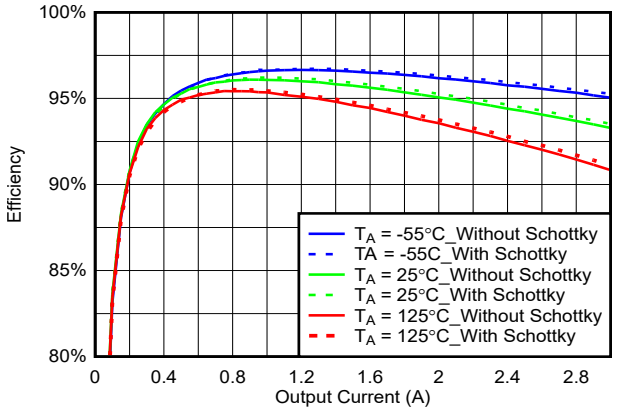


Figure 6-7. Efficiency vs Load Across Temperature With and Without External Schottky Diode at f_{SW} = 100kHz, PVIN = 15V, V_{OUT} = 12V

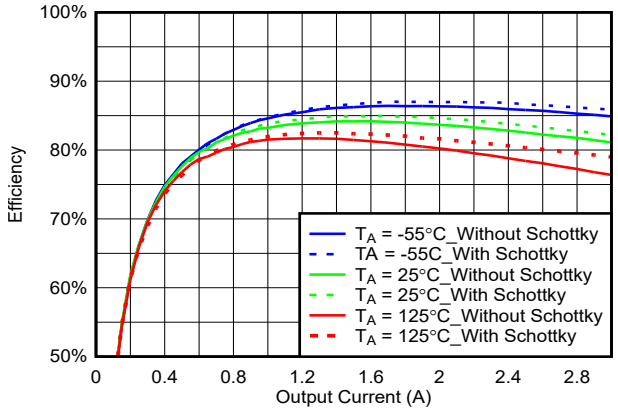


Figure 6-8. Efficiency vs Load Across Temperature With and Without External Schottky Diode at f_{SW} = 100kHz, PVIN = 28V, V_{OUT} = 3V

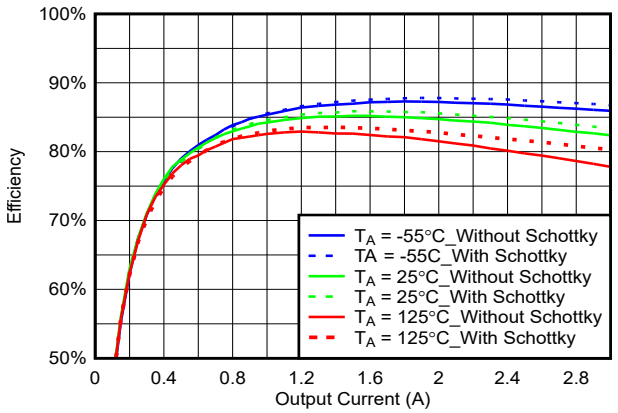


Figure 6-9. Efficiency vs Load Across Temperature With and Without External Schottky Diode at f_{SW} = 100kHz, PVIN = 28V, V_{OUT} = 3.3V

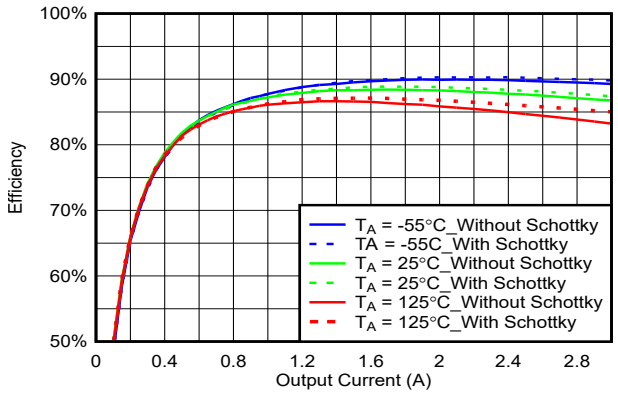


Figure 6-10. Efficiency vs Load Across Temperature With and Without External Schottky Diode at f_{SW} = 100kHz, PVIN = 28V, V_{OUT} = 5V

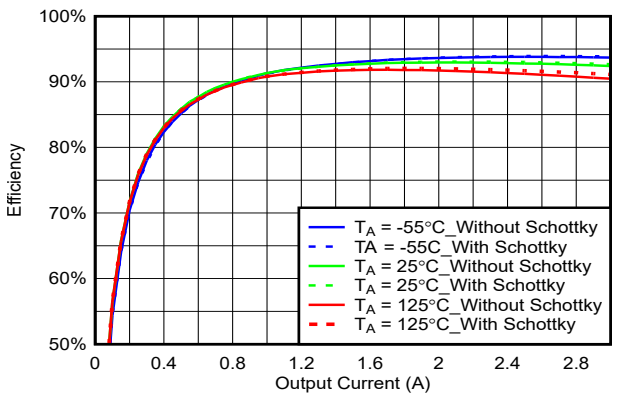


Figure 6-11. Efficiency vs Load Across Temperature With and Without External Schottky Diode at f_{SW} = 100kHz, PVIN = 28V, V_{OUT} = 12V

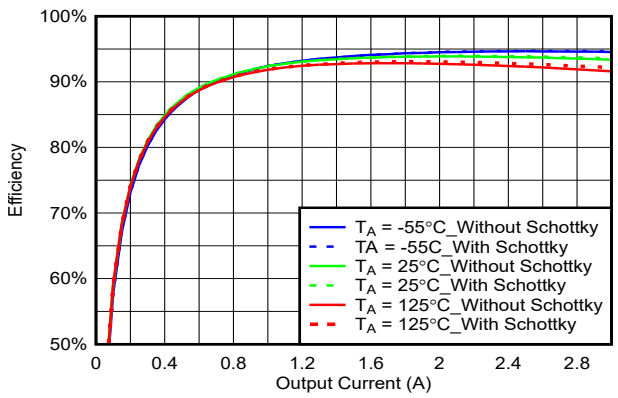


Figure 6-12. Efficiency vs Load Across Temperature With and Without External Schottky Diode at f_{SW} = 100kHz, PVIN = 28V, V_{OUT} = 15V

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6.7 Typical Characteristics (continued)

28-pin HTSSOP (PWP) package, PVIN = 28V, VOUT = 12V, C_{IN} = 81.8µF, C_{OUT} = 132.3µF, C_{SS} = 22nF, L = 27µH (Würth Elektronik Model: 7447709270), T_A = 25°C, unless otherwise noted. The efficiency plots at f_{SW} = 500kHz used an L = 10µH (Würth Elektronik Model: 7447709100)

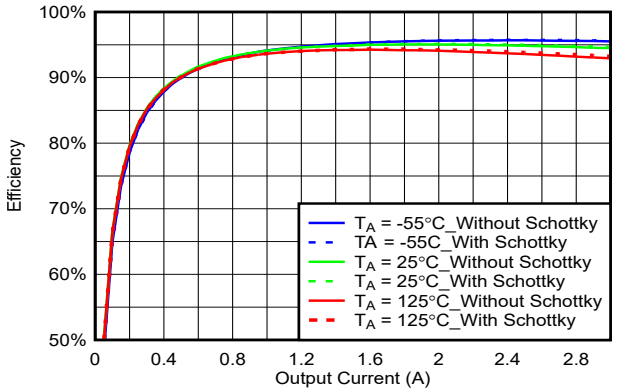


Figure 6-13. Efficiency vs Load Across Temperature With and Without External Schottky Diode at f_{SW} = 100kHz, PVIN = 28V, V_{OUT} = 18V

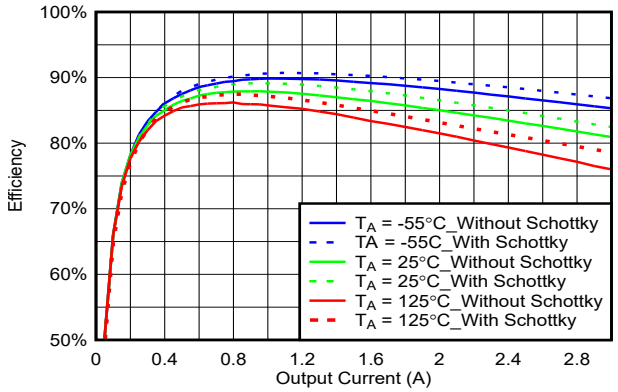


Figure 6-14. Efficiency vs Load Across Temperature With and Without External Schottky Diode at f_{SW} = 250kHz, PVIN = 12V, V_{OUT} = 3V

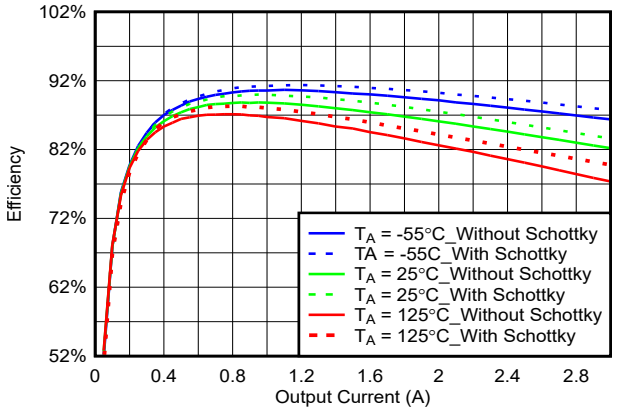


Figure 6-15. Efficiency vs Load Across Temperature With and Without External Schottky Diode at f_{SW} = 250kHz, PVIN = 12V, V_{OUT} = 3.3V

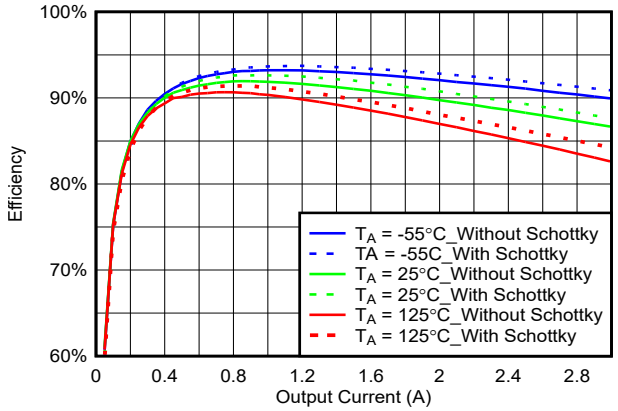


Figure 6-16. Efficiency vs Load Across Temperature With and Without External Schottky Diode at f_{SW} = 250kHz, PVIN = 12V, V_{OUT} = 5V

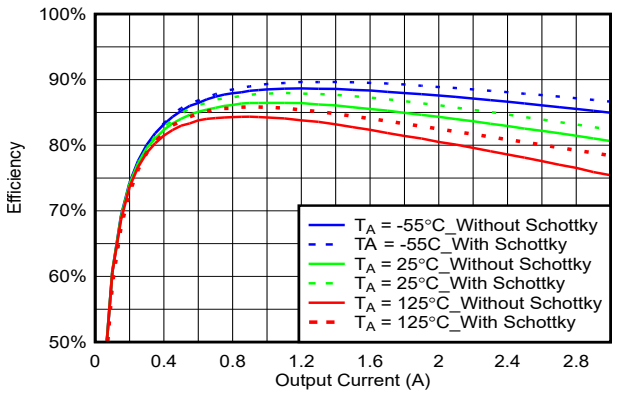


Figure 6-17. Efficiency vs Load Across Temperature With and Without External Schottky Diode at f_{SW} = 250kHz, PVIN = 15V, V_{OUT} = 3V

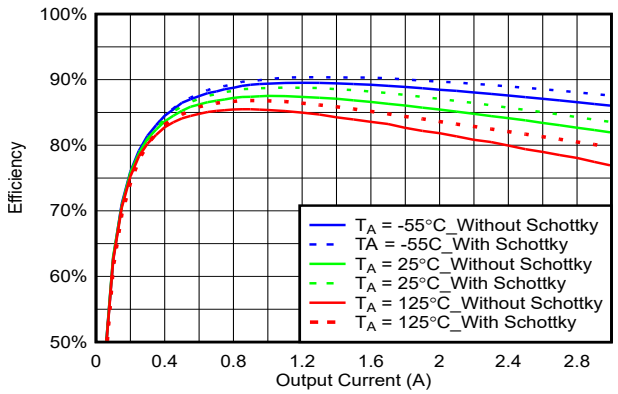


Figure 6-18. Efficiency vs Load Across Temperature With and Without External Schottky Diode at f_{SW} = 250kHz, PVIN = 15V, V_{OUT} = 3.3V

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6.7 Typical Characteristics (continued)

28-pin HTSSOP (PWP) package, PVIN = 28V, VOUT = 12V, C_{IN} = 81.8µF, C_{OUT} = 132.3µF, C_{SS} = 22nF, L = 27µH (Würth Elektronik Model: 7447709270), T_A = 25°C, unless otherwise noted. The efficiency plots at f_{SW} = 500kHz used an L = 10µH (Würth Elektronik Model: 7447709100)

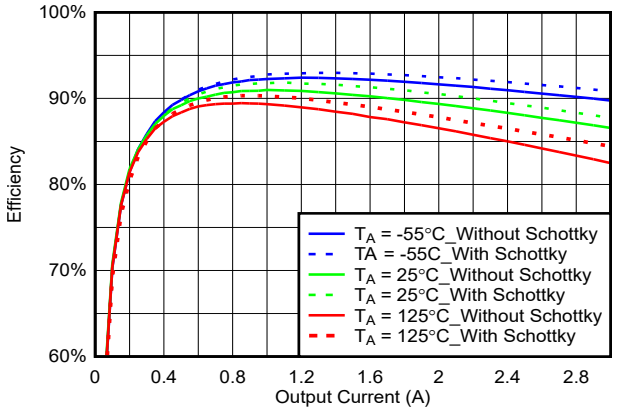


Figure 6-19. Efficiency vs Load Across Temperature With and Without External Schottky Diode at f_{SW} = 250kHz, PVIN = 15V, V_{OUT} = 5V

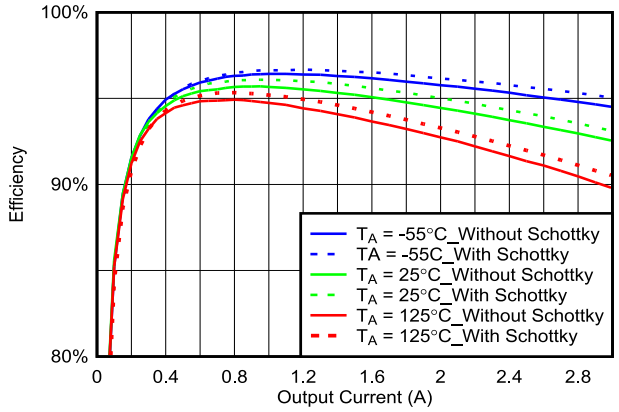


Figure 6-20. Efficiency vs Load Across Temperature With and Without External Schottky Diode at f_{SW} = 250kHz, PVIN = 15V, V_{OUT} = 12V

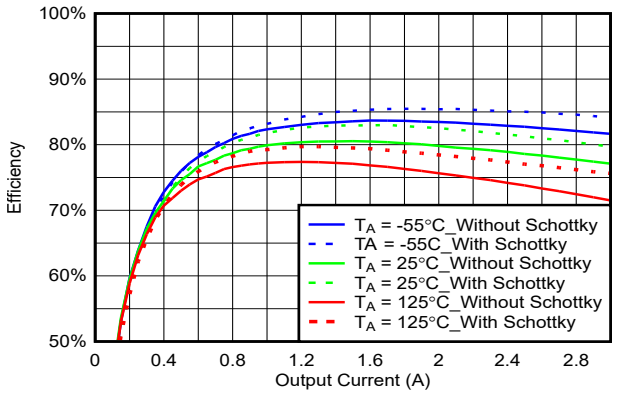


Figure 6-21. Efficiency vs Load Across Temperature With and Without External Schottky Diode at f_{SW} = 250kHz, PVIN = 28V, V_{OUT} = 3V

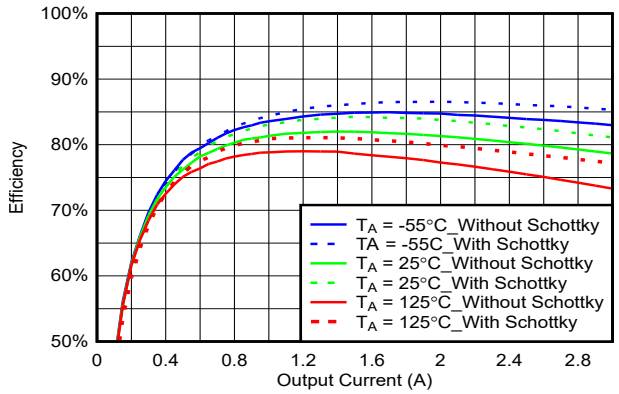


Figure 6-22. Efficiency vs Load Across Temperature With and Without External Schottky Diode at f_{SW} = 250kHz, PVIN = 28V, V_{OUT} = 3.3V

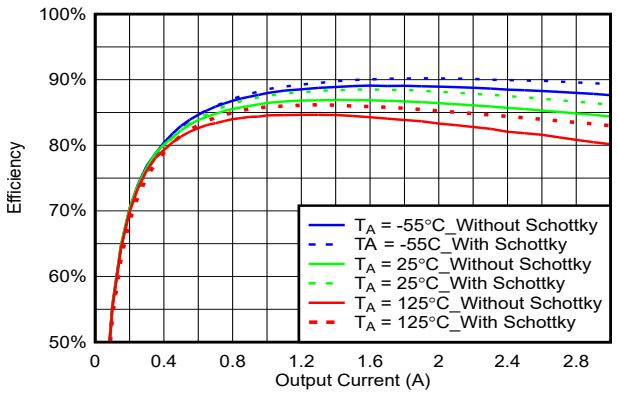


Figure 6-23. Efficiency vs Load Across Temperature With and Without External Schottky Diode at f_{SW} = 250kHz, PVIN = 28V, V_{OUT} = 5V

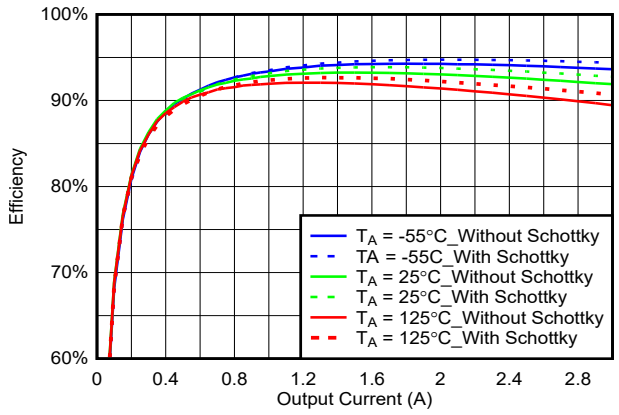


Figure 6-24. Efficiency vs Load Across Temperature With and Without External Schottky Diode at f_{SW} = 250kHz, PVIN = 28V, V_{OUT} = 12V

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6.7 Typical Characteristics (continued)

28-pin HTSSOP (PWP) package, PVIN = 28V, VOUT = 12V, C_{IN} = 81.8µF, C_{OUT} = 132.3µF, C_{SS} = 22nF, L = 27µH (Würth Elektronik Model: 7447709270), T_A = 25°C, unless otherwise noted. The efficiency plots at f_{SW} = 500kHz used an L = 10µH (Würth Elektronik Model: 7447709100)

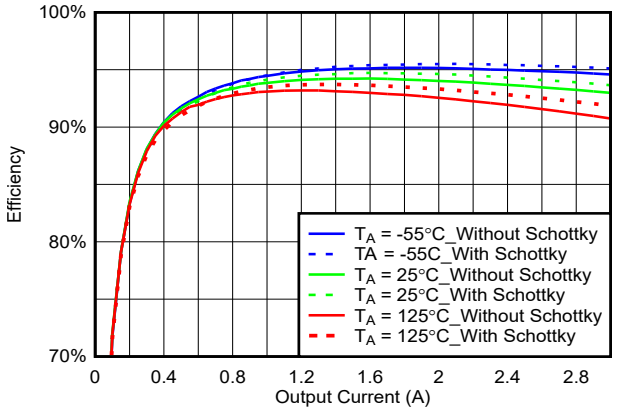


Figure 6-25. Efficiency vs Load Across Temperature With and Without External Schottky Diode at f_{SW} = 250kHz, PVIN = 28V, V_{OUT} = 15V

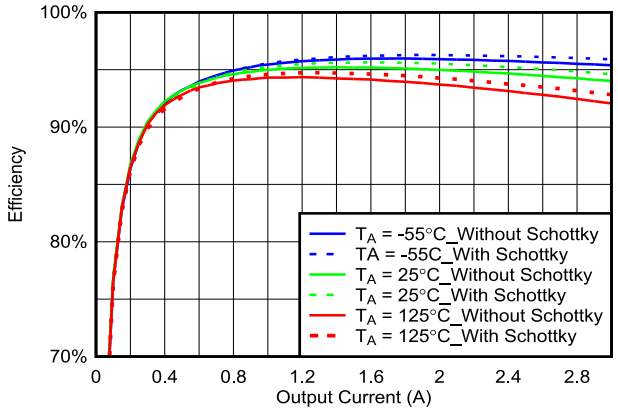


Figure 6-26. Efficiency vs Load Across Temperature With and Without External Schottky Diode at f_{SW} = 250kHz, PVIN = 28V, V_{OUT} = 18V

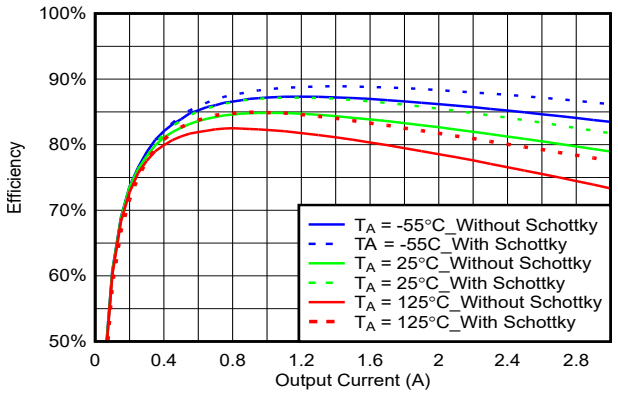


Figure 6-27. Efficiency vs Load Across Temperature With and Without External Schottky Diode at f_{SW} = 500kHz, PVIN = 12V, V_{OUT} = 3V

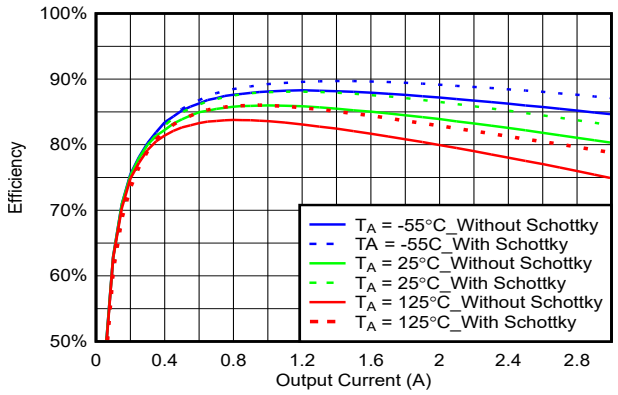


Figure 6-28. Efficiency vs Load Across Temperature With and Without External Schottky Diode at f_{SW} = 500kHz, PVIN = 12V, V_{OUT} = 3.3V

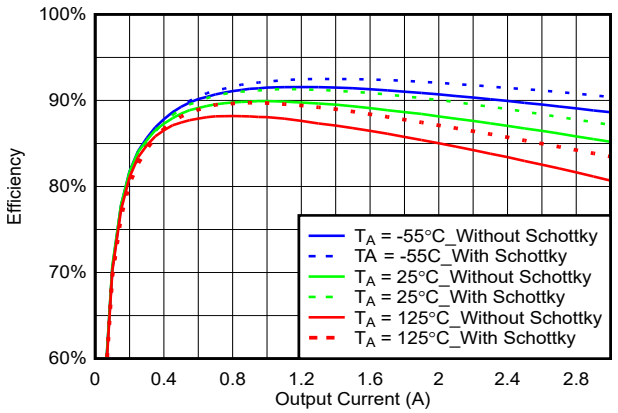


Figure 6-29. Efficiency vs Load Across Temperature With and Without External Schottky Diode at f_{SW} = 500kHz, PVIN = 12V, V_{OUT} = 5V

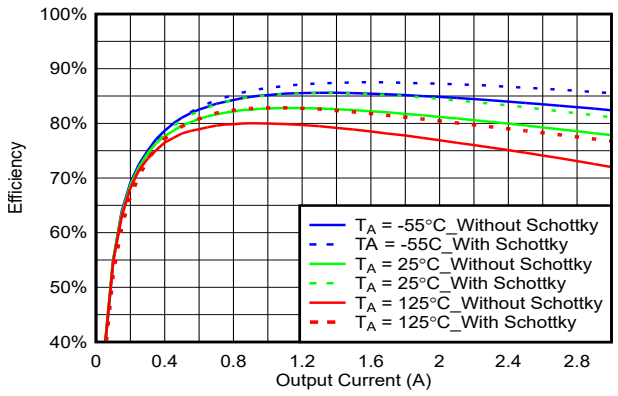


Figure 6-30. Efficiency vs Load Across Temperature With and Without External Schottky Diode at f_{SW} = 500kHz, PVIN = 15V, V_{OUT} = 3V

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6.7 Typical Characteristics (continued)

28-pin HTSSOP (PWP) package, PVIN = 28V, VOUT = 12V, C_{IN} = 81.8µF, C_{OUT} = 132.3µF, C_{SS} = 22nF, L = 27µH (Würth Elektronik Model: 7447709270), T_A = 25°C, unless otherwise noted. The efficiency plots at f_{SW} = 500kHz used an L = 10µH (Würth Elektronik Model: 7447709100)

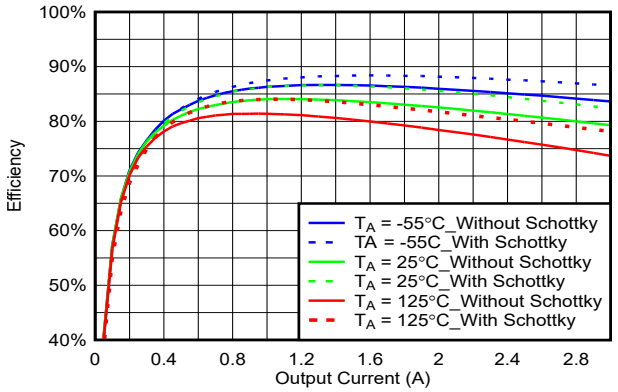


Figure 6-31. Efficiency vs Load Across Temperature With and Without External Schottky Diode at f_{SW} = 500kHz, PVIN = 15V, V_{OUT} = 3.3V

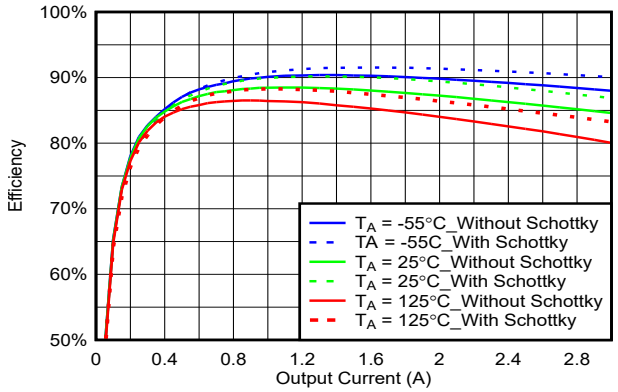


Figure 6-32. Efficiency vs Load Across Temperature With and Without External Schottky Diode at f_{SW} = 500kHz, PVIN = 15V, V_{OUT} = 5V

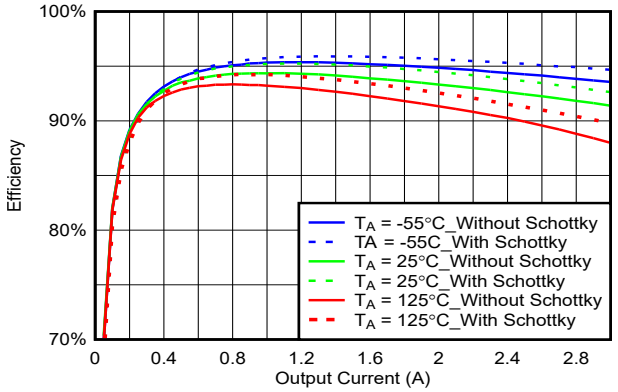


Figure 6-33. Efficiency vs Load Across Temperature With and Without External Schottky Diode at f_{SW} = 500kHz, PVIN = 15V, V_{OUT} = 12V

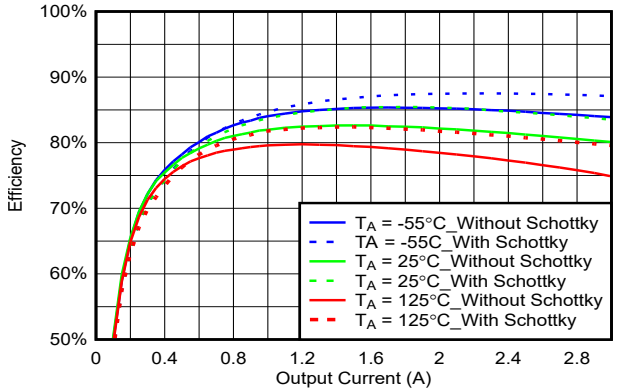


Figure 6-34. Efficiency vs Load Across Temperature With and Without External Schottky Diode at f_{SW} = 500kHz, PVIN = 28V, V_{OUT} = 5V

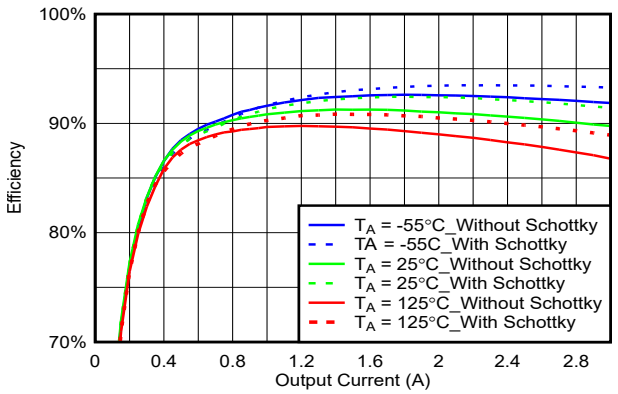


Figure 6-35. Efficiency vs Load Across Temperature With and Without External Schottky Diode at f_{SW} = 500kHz, PVIN = 28V, V_{OUT} = 12V

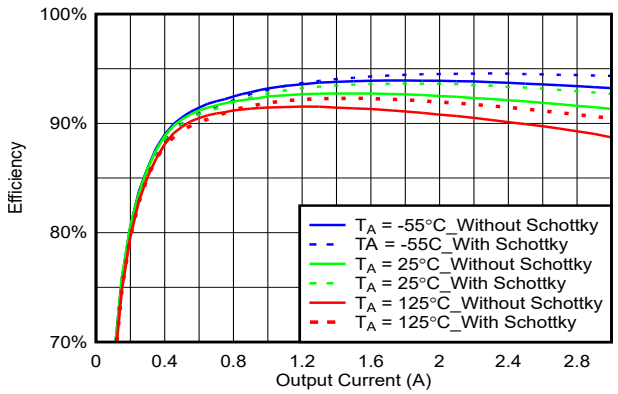


Figure 6-36. Efficiency vs Load Across Temperature With and Without External Schottky Diode at f_{SW} = 500kHz, PVIN = 28V, V_{OUT} = 15V

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6.7 Typical Characteristics (continued)

28-pin HTSSOP (PWP) package, PVIN = 28V, VOUT = 12V, C_{IN} = 81.8µF, C_{OUT} = 132.3µF, C_{SS} = 22nF, L = 27µH (Würth Elektronik Model: 7447709270), T_A = 25°C, unless otherwise noted. The efficiency plots at f_{SW} = 500kHz used an L = 10µH (Würth Elektronik Model: 7447709100)

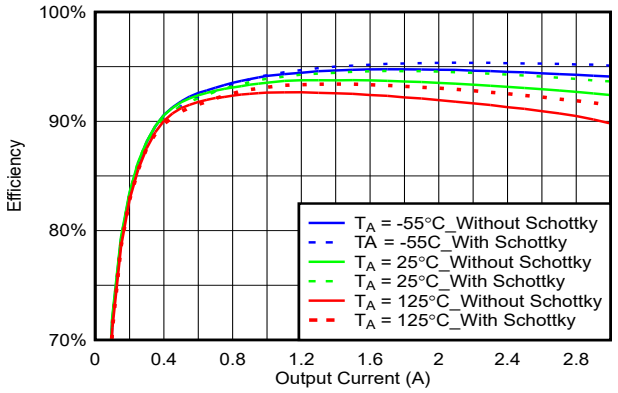


Figure 6-37. Efficiency vs Load Across Temperature With and Without External Schottky Diode at f_{SW} = 500kHz, PVIN = 28V, V_{OUT} = 18V

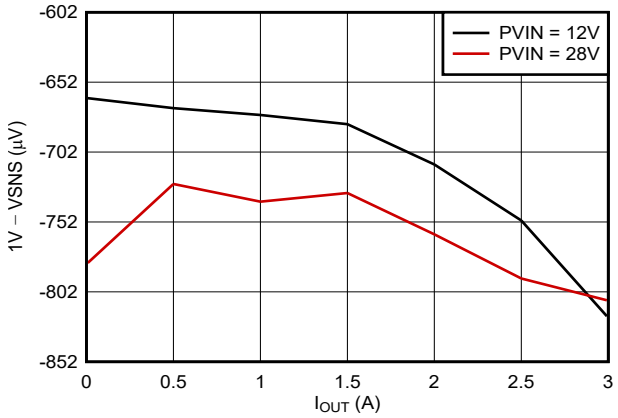


Figure 6-38. Delta VSNS vs Load at T_A = 25°C

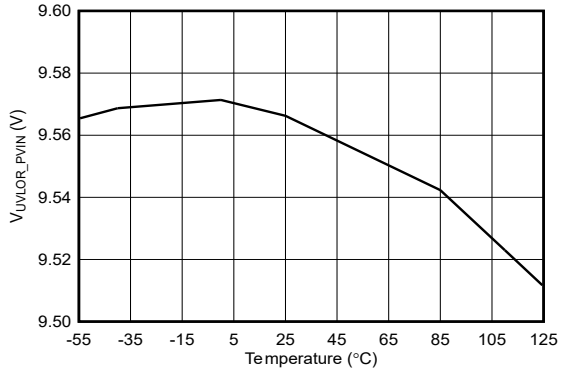


Figure 6-39. PVIN Internal UVLO Rising Threshold vs Ambient Temperature

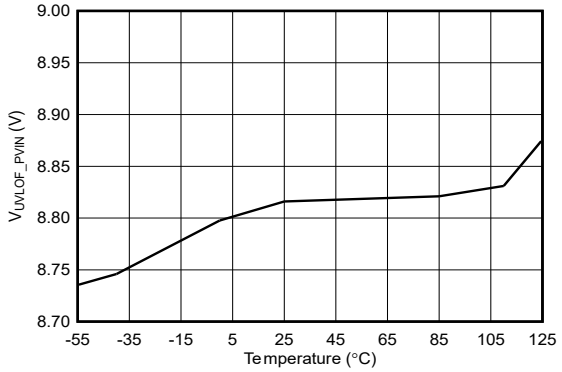


Figure 6-40. PVIN Internal UVLO Falling Threshold vs Ambient Temperature

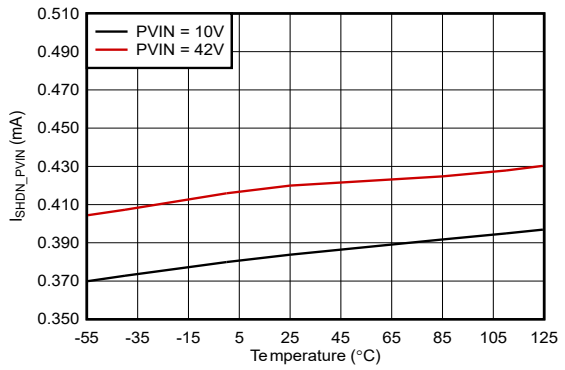


Figure 6-41. PVIN Shutdown Supply Current vs Ambient Temperature OVER PVIN Voltage

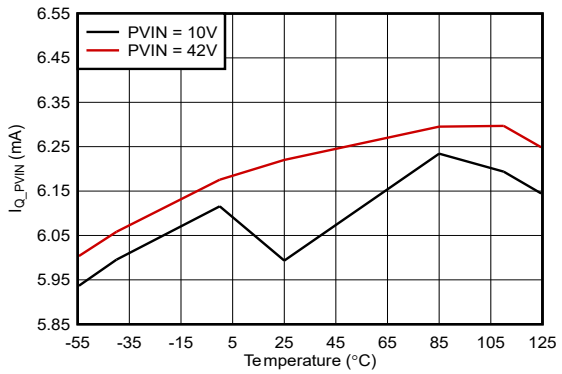


Figure 6-42. PVIN Quiescent Supply Current (Non-Switching) vs Ambient Temperature OVER PVIN Voltage

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6.7 Typical Characteristics (continued)

28-pin HTSSOP (PWP) package, PVIN = 28V, VOUT = 12V, C_{IN} = 81.8µF, C_{OUT} = 132.3µF, C_{SS} = 22nF, L = 27µH (Würth Elektronik Model: 7447709270), T_A = 25°C, unless otherwise noted. The efficiency plots at f_{SW} = 500kHz used an L = 10µH (Würth Elektronik Model: 7447709100)

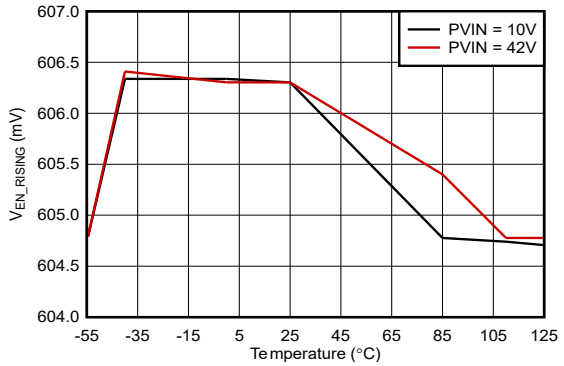


Figure 6-43. Enable Rising Threshold vs Ambient Temperature OVER PVIN Voltage

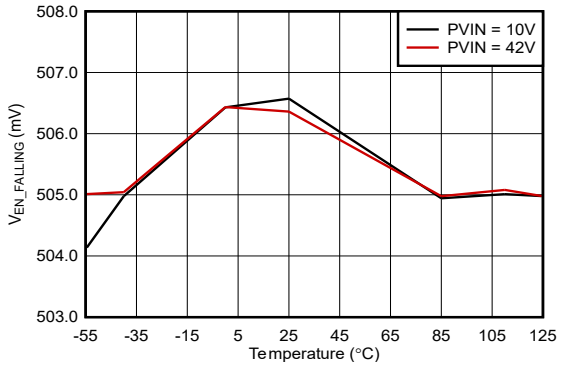


Figure 6-44. Enable Falling Threshold vs Ambient Temperature OVER PVIN Voltage

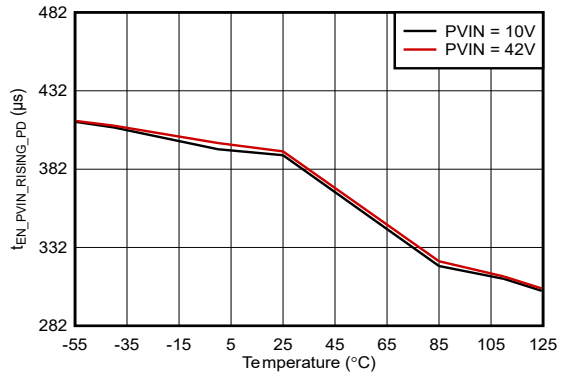


Figure 6-45. Enable Propagation Delay (PVIN = EN, Tied Together) vs Ambient Temperature OVER PVIN Voltage

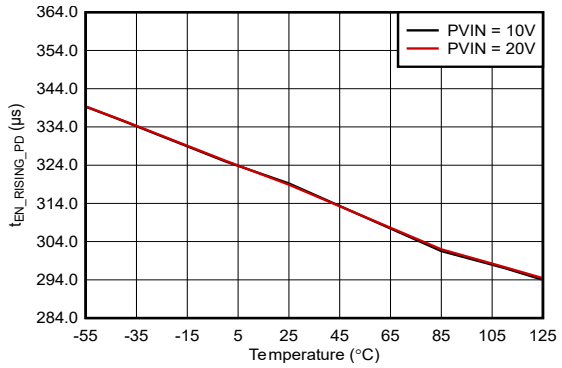


Figure 6-46. Enable Propagation Delay vs Ambient Temperature OVER PVIN Voltage

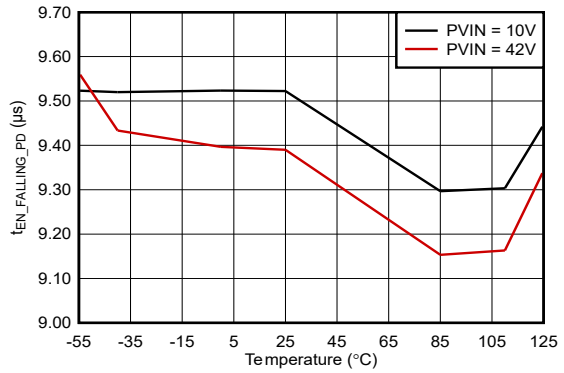


Figure 6-47. Disabled Propagation Delay vs Ambient Temperature OVER PVIN Voltage

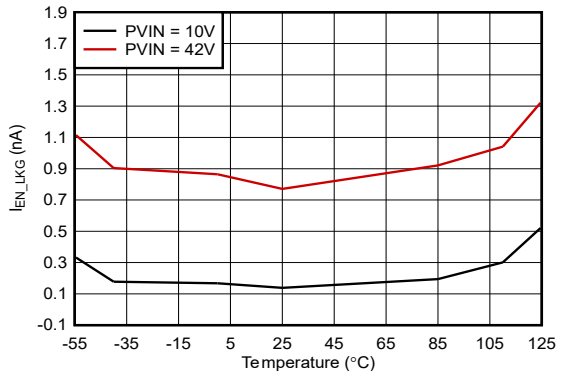


Figure 6-48. Enable Leakage Current vs Ambient Temperature OVER PVIN Voltage

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6.7 Typical Characteristics (continued)

28-pin HTSSOP (PWP) package, PVIN = 28V, VOUT = 12V, C_{IN} = 81.8µF, C_{OUT} = 132.3µF, C_{SS} = 22nF, L = 27µH (Würth Elektronik Model: 7447709270), T_A = 25°C, unless otherwise noted. The efficiency plots at f_{SW} = 500kHz used an L = 10µH (Würth Elektronik Model: 7447709100)

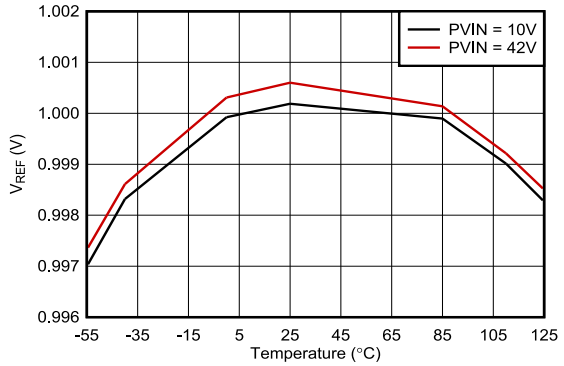


Figure 6-49. Internal Voltage Reference of Error Amplifier vs Ambient Temperature OVER PVIN Voltage

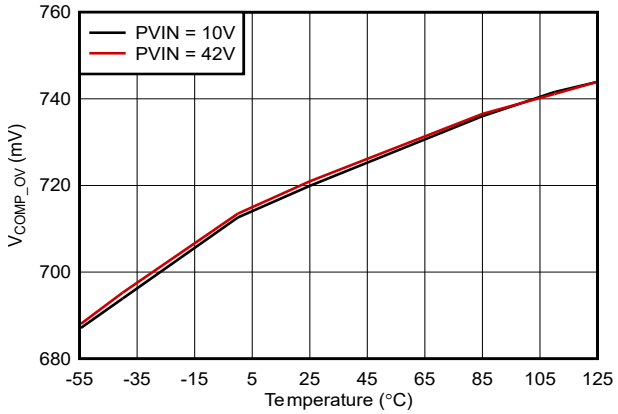


Figure 6-50. COMP Voltage to Skip High Side Turn-on vs Ambient Temperature OVER PVIN Voltage

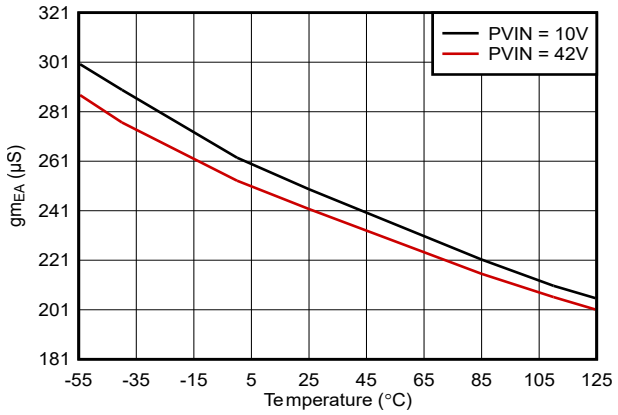


Figure 6-51. Error Amplifier Transconductance vs Ambient Temperature OVER PVIN Voltage

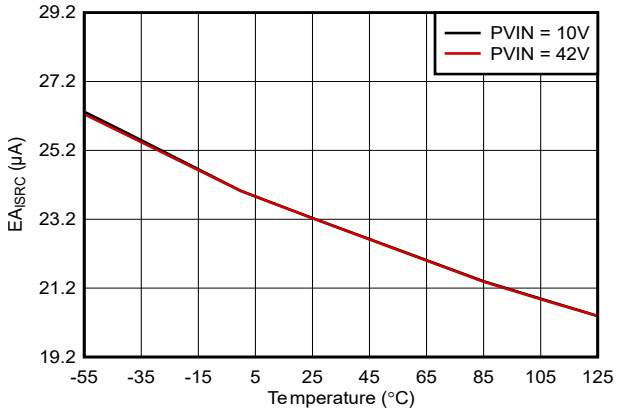


Figure 6-52. Error Amplifier Source Current vs Ambient Temperature OVER PVIN Voltage

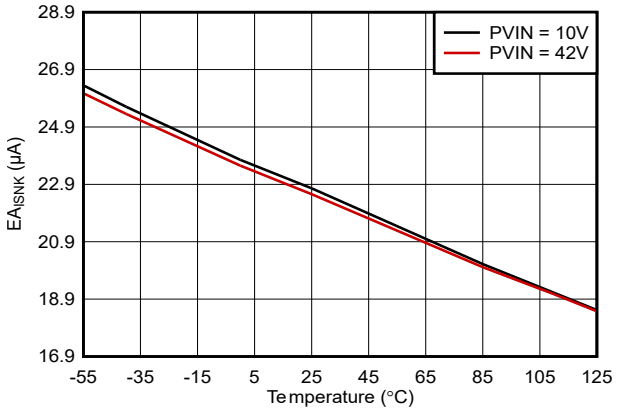


Figure 6-53. Error Amplifier Sink Current vs Ambient Temperature OVER PVIN Voltage

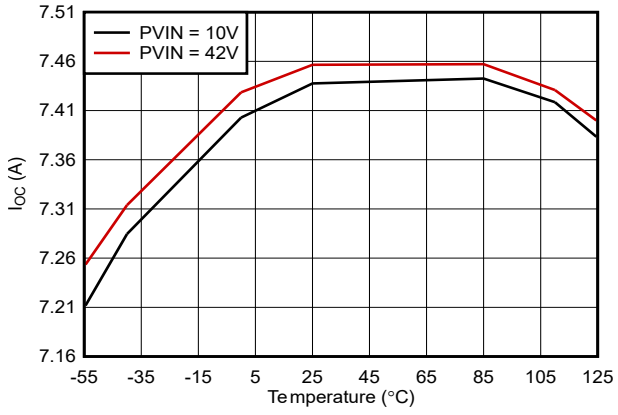


Figure 6-54. High Side Switch Overcurrent Threshold vs Ambient Temperature OVER PVIN Voltage

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6.7 Typical Characteristics (continued)

28-pin HTSSOP (PWP) package, PVIN = 28V, VOUT = 12V, C_{IN} = 81.8µF, C_{OUT} = 132.3µF, C_{SS} = 22nF, L = 27µH (Würth Elektronik Model: 7447709270), T_A = 25°C, unless otherwise noted. The efficiency plots at f_{SW} = 500kHz used an L = 10µH (Würth Elektronik Model: 7447709100)

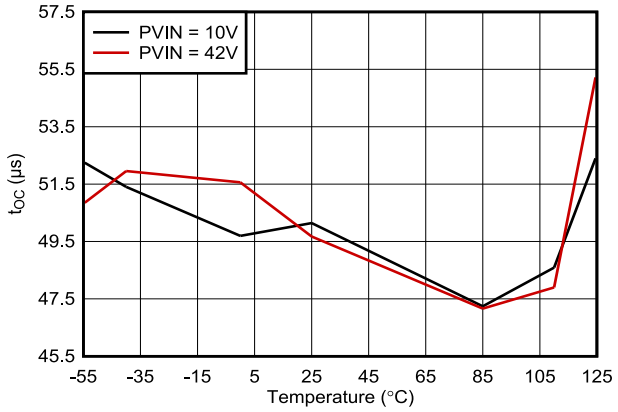


Figure 6-55. High Side Current Limit Fault Time vs Ambient Temperature OVER PVIN Voltage

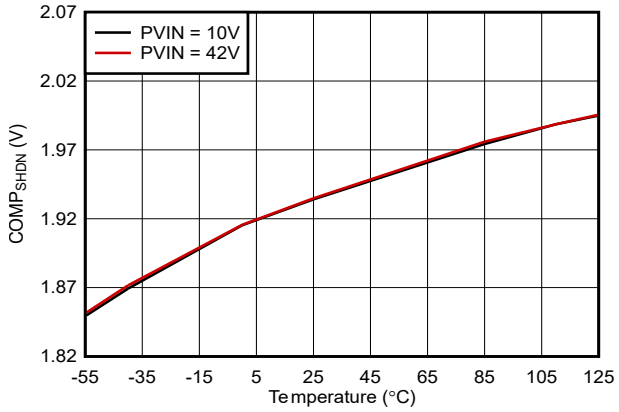


Figure 6-56. COMP Shutdown Voltage vs Ambient Temperature OVER PVIN Voltage

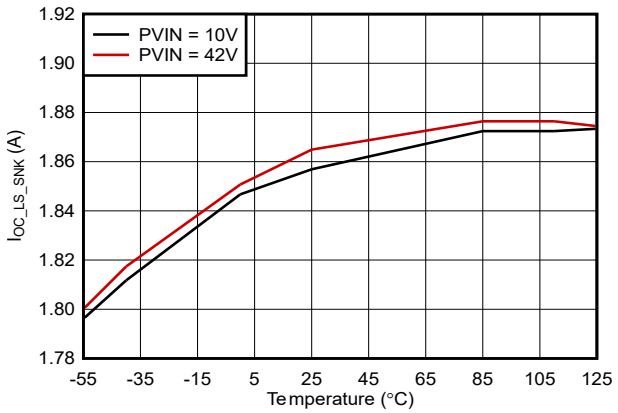


Figure 6-57. Low Side Switch Overcurrent Sinking Threshold vs Ambient Temperature OVER PVIN Voltage

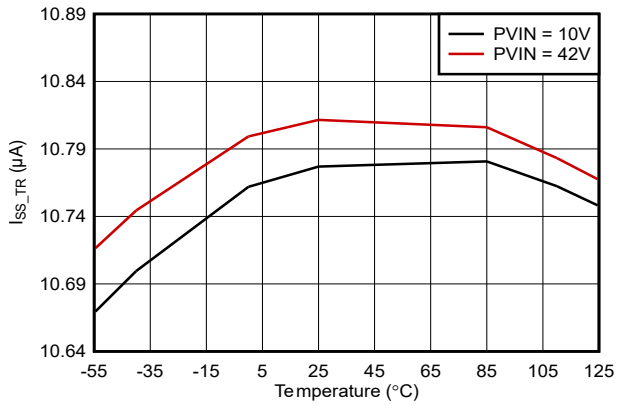


Figure 6-58. Soft Start Charge Current vs Ambient Temperature OVER PVIN Voltage

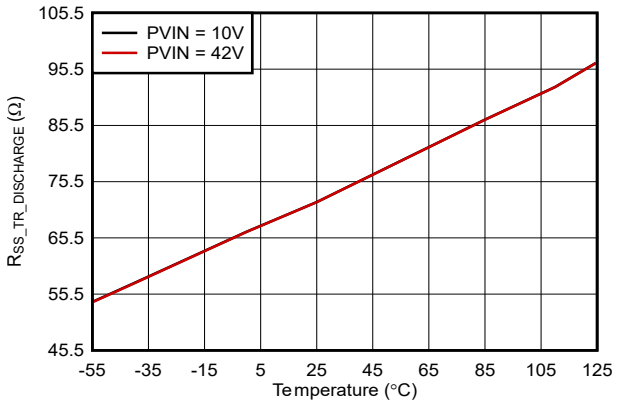


Figure 6-59. Soft Start Discharge Pull-Down vs Ambient Temperature OVER PVIN Voltage

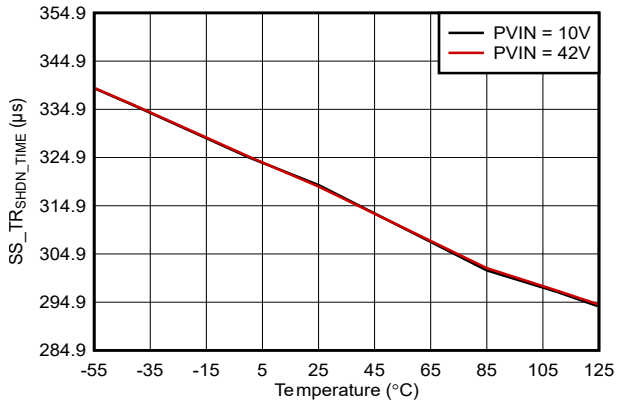


Figure 6-60. Active Soft-Start Pull-Down Time for a $COMP_{SHDN}$ Event vs Ambient Temperature OVER PVIN Voltage

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6.7 Typical Characteristics (continued)

28-pin HTSSOP (PWP) package, PVIN = 28V, VOUT = 12V, C_{IN} = 81.8µF, C_{OUT} = 132.3µF, C_{SS} = 22nF, L = 27µH (Würth Elektronik Model: 7447709270), T_A = 25°C, unless otherwise noted. The efficiency plots at f_{SW} = 500kHz used an L = 10µH (Würth Elektronik Model: 7447709100)

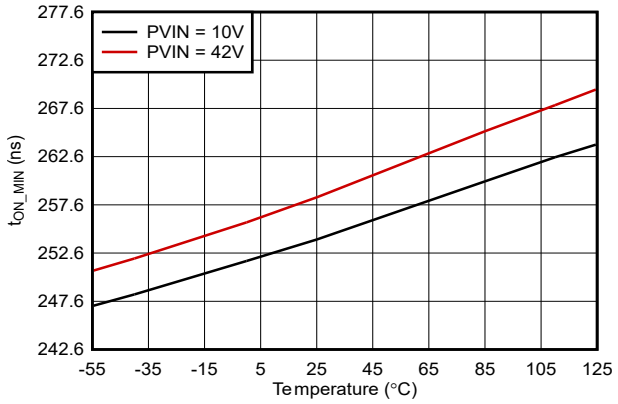


Figure 6-61. Minimum On Time vs Ambient Temperature OVER PVIN Voltage

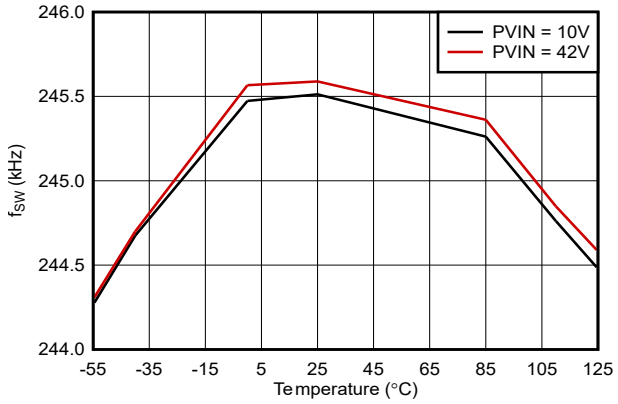


Figure 6-62. Internal Programmed Switching Frequency vs Ambient Temperature OVER PVIN Voltage

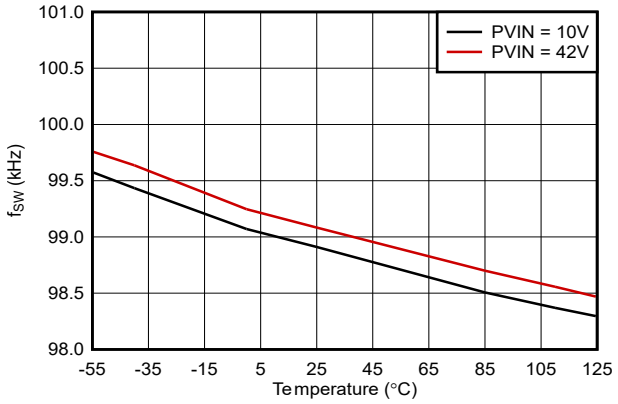


Figure 6-63. Externally Programmed Switching Frequency (RT = 97.6kΩ) vs Ambient Temperature OVER PVIN Voltage

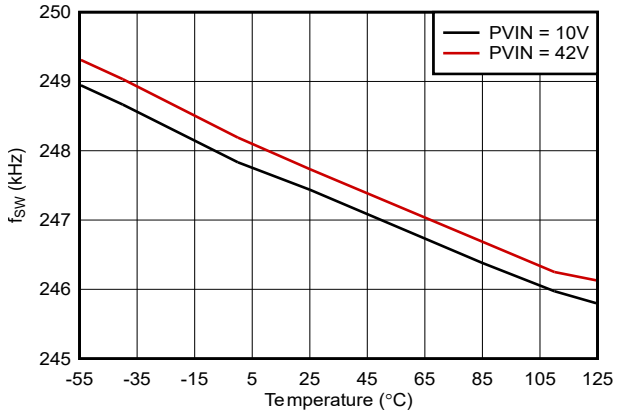


Figure 6-64. Externally Programmed Switching Frequency (RT = 37.9kΩ) vs Ambient Temperature OVER PVIN Voltage

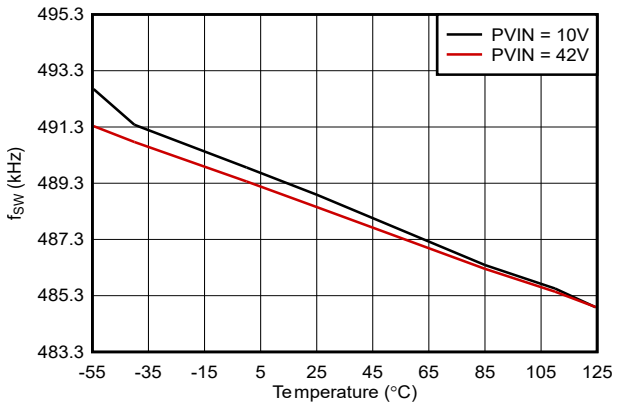


Figure 6-65. Externally Programmed Switching Frequency (RT = 18.7kΩ) vs Ambient Temperature OVER PVIN Voltage

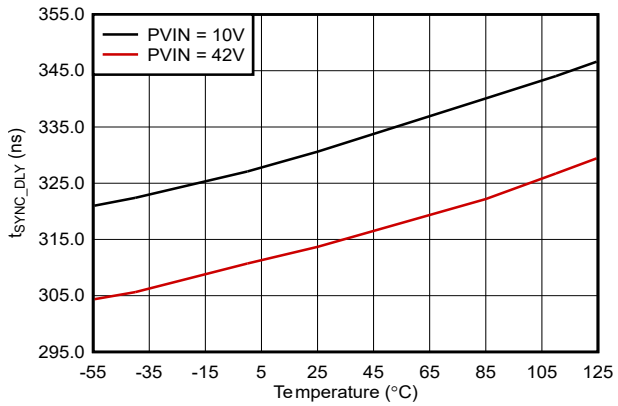


Figure 6-66. SYNC to SW Delay vs Ambient Temperature OVER PVIN Voltage

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6.7 Typical Characteristics (continued)

28-pin HTSSOP (PWP) package, PVIN = 28V, VOUT = 12V, C_{IN} = 81.8µF, C_{OUT} = 132.3µF, C_{SS} = 22nF, L = 27µH (Würth Elektronik Model: 7447709270), T_A = 25°C, unless otherwise noted. The efficiency plots at f_{SW} = 500kHz used an L = 10µH (Würth Elektronik Model: 7447709100)

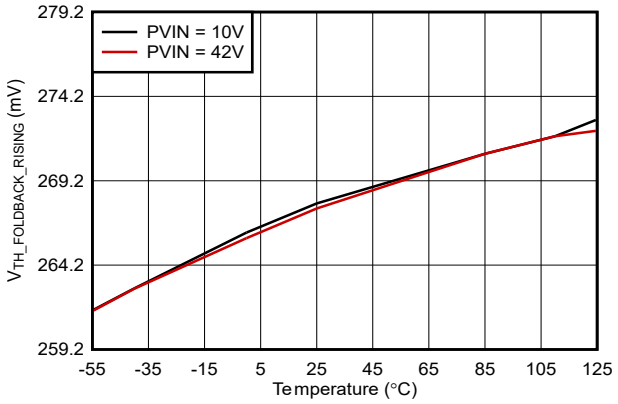


Figure 6-67. VSNS Rising Threshold Voltage to be out of Foldback vs Ambient Temperature OVER PVIN Voltage

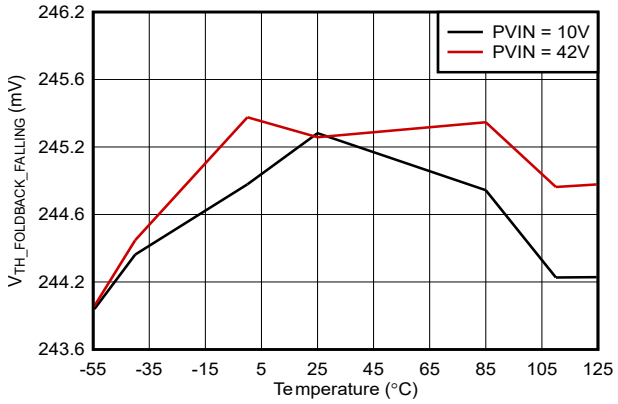


Figure 6-68. VSNS Falling Threshold Voltage to be Into Foldback vs Ambient Temperature OVER PVIN Voltage

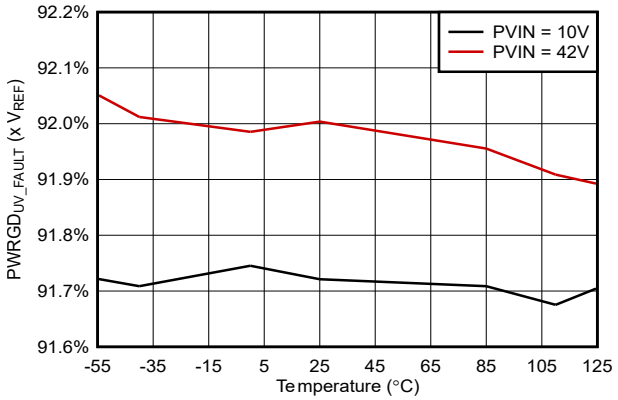


Figure 6-69. VSNS Undervoltage Falling Fault Threshold vs Ambient Temperature OVER PVIN Voltage

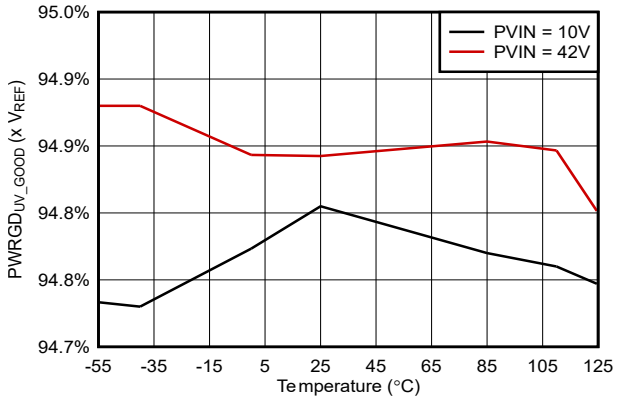


Figure 6-70. VSNS Undervoltage Rising Good Threshold vs Ambient Temperature OVER PVIN Voltage

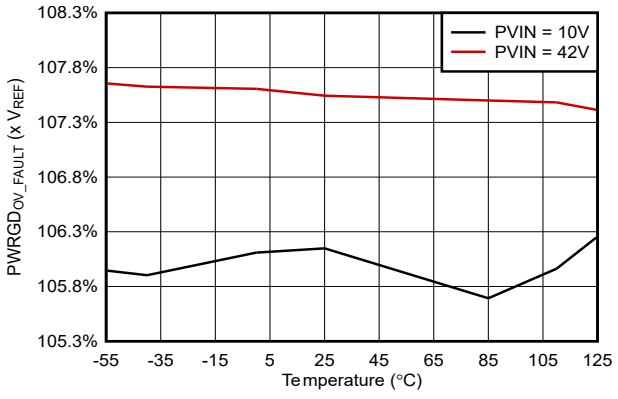


Figure 6-71. VSNS Overvoltage Falling Fault Threshold vs Ambient Temperature OVER PVIN Voltage

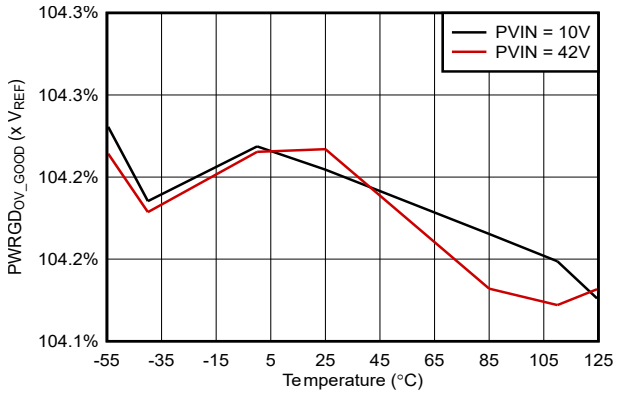


Figure 6-72. VSNS Overvoltage Rising Good Threshold vs Ambient Temperature OVER PVIN Voltage

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6.7 Typical Characteristics (continued)

28-pin HTSSOP (PWP) package, PVIN = 28V, VOUT = 12V, C_{IN} = 81.8µF, C_{OUT} = 132.3µF, C_{SS} = 22nF, L = 27µH (Würth Elektronik Model: 7447709270), T_A = 25°C, unless otherwise noted. The efficiency plots at f_{SW} = 500kHz used an L = 10µH (Würth Elektronik Model: 7447709100)

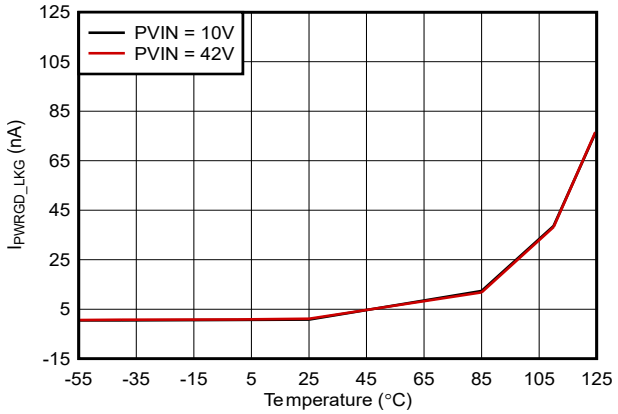


Figure 6-73. PWRGD Open Input Leakage at V_{PWRGD} = 5.5V vs Ambient Temperature OVER PVIN Voltage

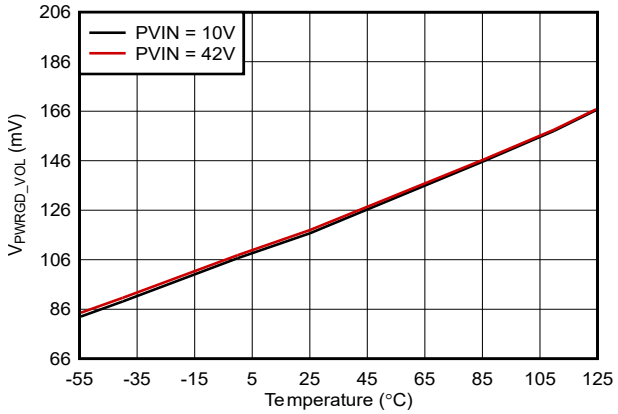


Figure 6-74. PWRGD Output Low vs Ambient Temperature OVER PVIN Voltage

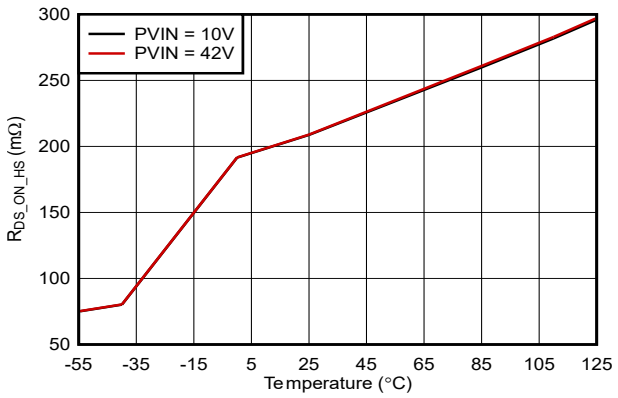


Figure 6-75. High Side Switch Resistance vs Ambient Temperature OVER PVIN Voltage

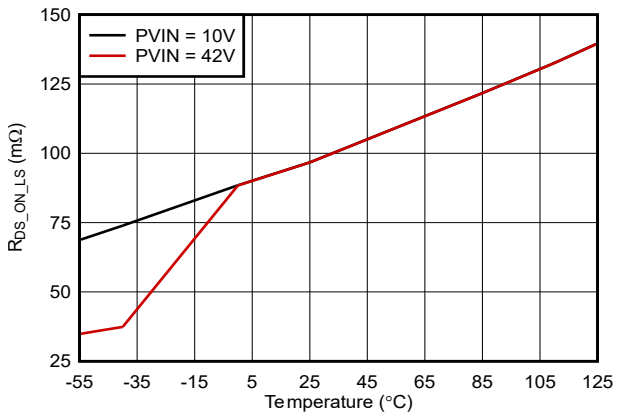


Figure 6-76. Low Side Switch Resistance vs Ambient Temperature OVER PVIN Voltage

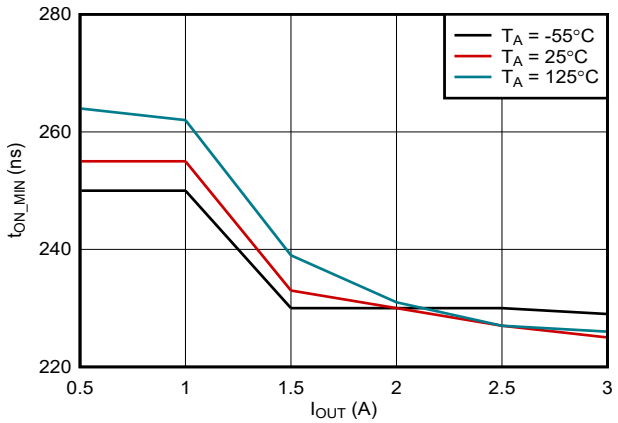


Figure 6-77. t_{ON_MIN} vs I_{OUT} OVER Temperature at PVIN = 28V (in Open Loop)

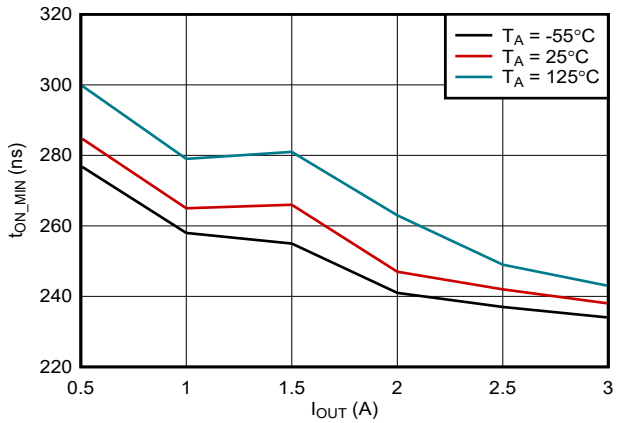
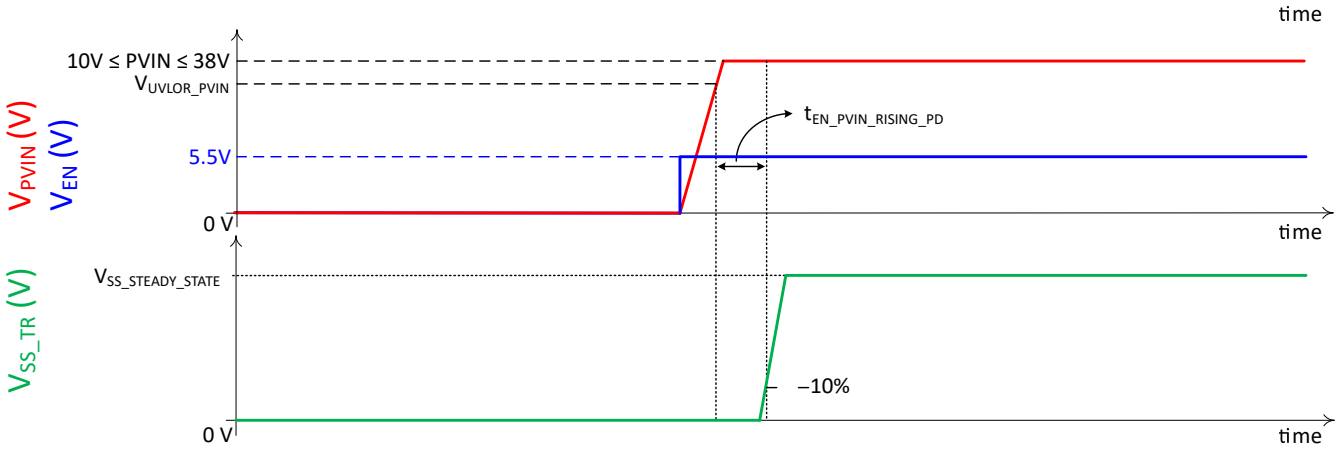


Figure 6-78. t_{ON_MIN} vs I_{OUT} OVER Temperature at PVIN = 12V (in Open Loop)

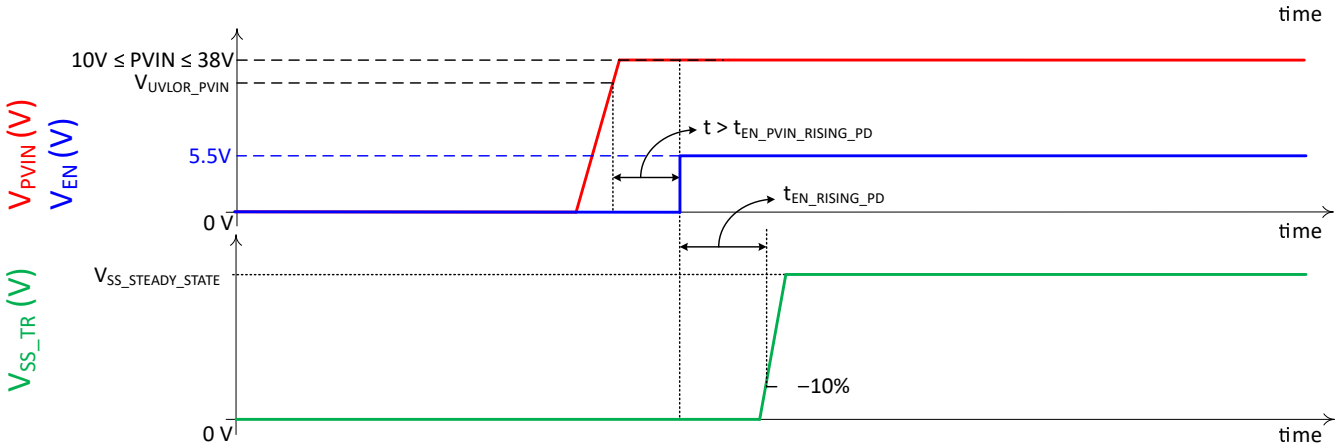
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7 Parameter Measurement Information



A. With error amp in unity gain and SS_TR = 1nF.

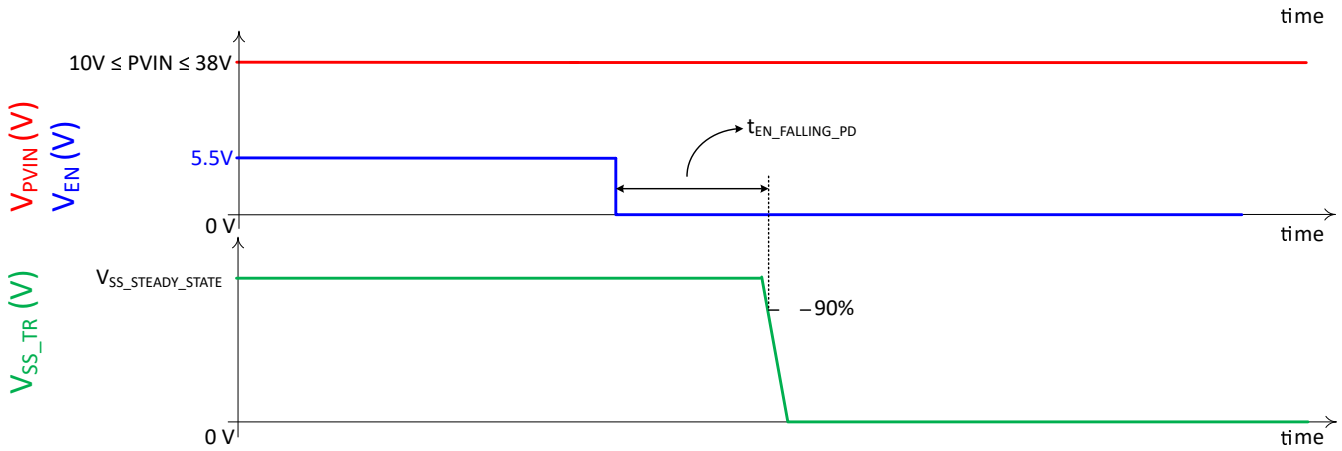
Figure 7-1. Rising Enable Propagation Delay When EN is Valid Before PVIN > V_{UVLOR_PVIN} ($t_{EN_PVIN_RISING_PD}$)



A. With error amp in unity gain and SS_TR = 1nF. When EN is low the internal REFCAP and VBIASP voltages are turned off for reduced current consumption.

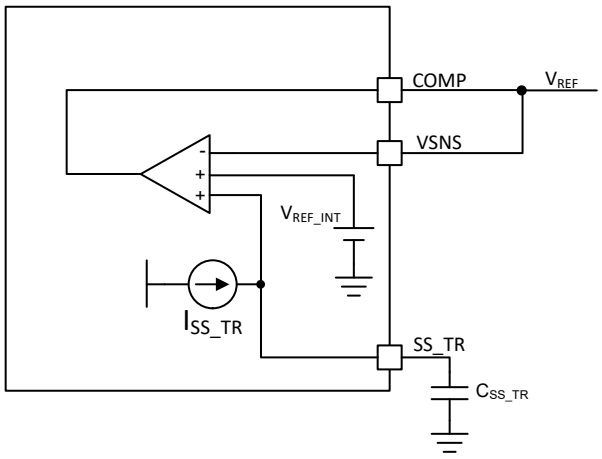
Figure 7-2. Rising Enable Propagation Delay When EN is Forced High After PVIN is Stable (PVIN> V_{UVLOR_PVIN}) For At Least $t_{EN_PVIN_RISING_PD}$ ($t_{EN_RISING_PD}$)

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A. With error amp in unity gain and SS_TR = 1nF. When EN is low the internal REFCAP and VBIASP output voltages are turned off for reduced current consumption.

Figure 7-3. Falling Enable Propagation Delay ($t_{EN_FALLING_PD}$)



A. This accurate reference voltage value includes the error amplifier offset, V_{IO}. Use this value to set the output voltage.

Figure 7-4. Reference Voltage Measurement

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8 Detailed Description

8.1 Overview

The TPS7H4203 is a 10V to 38V,3A synchronous step-down (buck) converter with two integrated MOSFETs: a PMOS for the high side and an NMOS for the low side. To improve performance during line and load transients, the device implements constant-frequency, peak-current-mode control, which also simplifies external frequency compensation. The programmable switching frequency range of 100kHz to 500kHz allows for efficiency and size optimization when selecting the output filter components. The MOSFETs are sized to optimize efficiency for low-duty-cycle applications.

The device is designed for safe monotonic startup into pre-biased loads. The default startup occurs when PVIN reaches typically 9.48V. The EN pin connects to the non-inverting input of a comparator with a stable reference and built-in hysteresis. The EN reference voltage is typically 605mV with 103mV of hysteresis. The maximum total operating current is 8.1mA when the device is enabled, not switching and under no load. When disabled, the device draws a maximum supply current of 0.53mA. When the device is disabled, internal blocks such as REFCAP and VBIASP are also disabled to reduce current consumption.

The device has a power-good comparator (PWRGD) with hysteresis that monitors the output voltage through the VSNS pin. The PWRGD pin is an open-drain MOSFET that pulls low when the VSNS pin voltage is less than 92% or greater than 108% of the reference voltage V_{REF}, and asserts high when the VSNS pin voltage is between 95% and 105% of V_{REF}, typically.

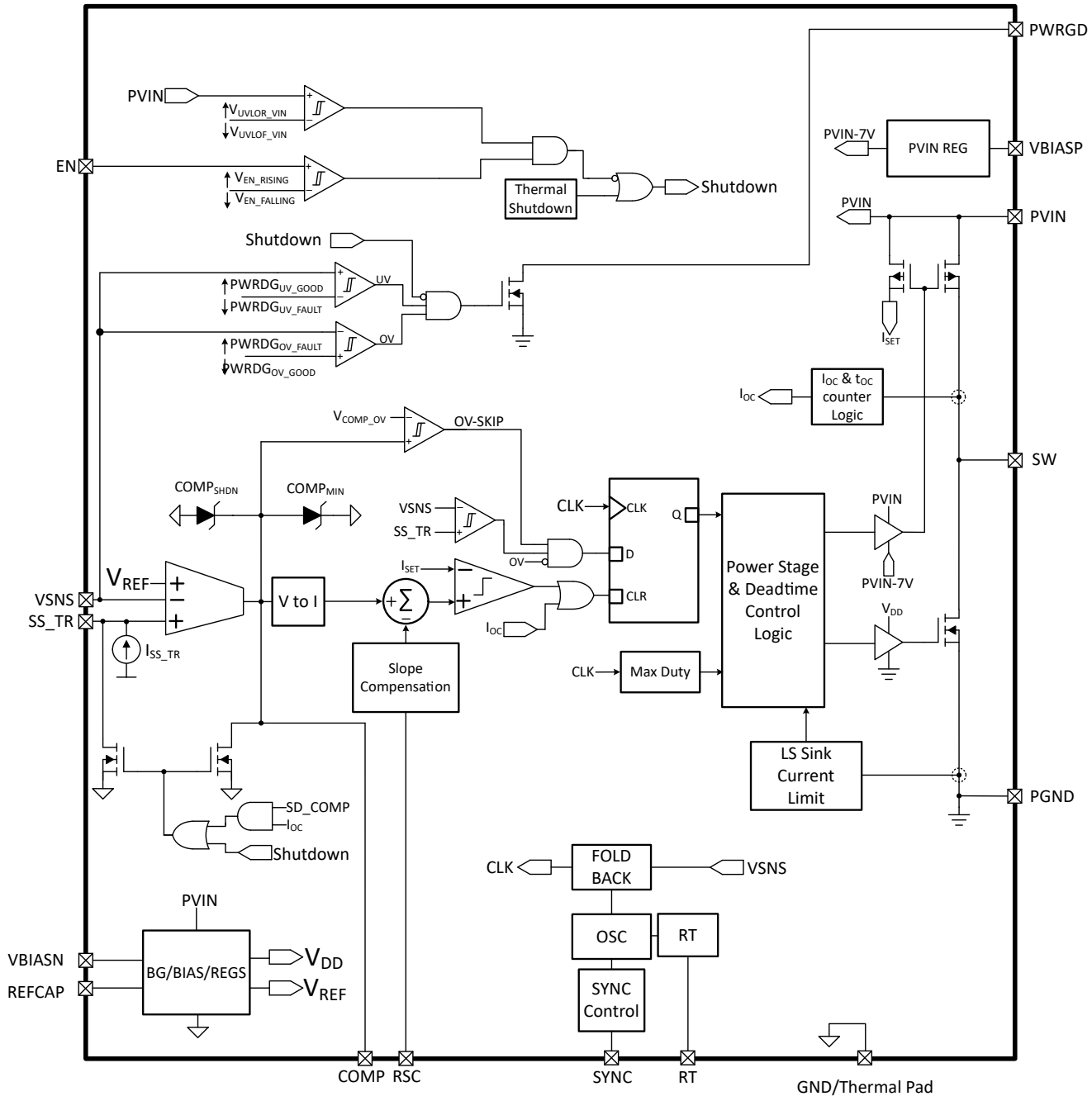
The SS_TR (soft-start and tracking) pin minimizes inrush currents and provides power-supply sequencing during power-up. Connect a small-value capacitor or resistor divider to this pin for soft-start or critical power-supply sequencing requirements. The maximum C_{SS_TR} capacitor value is 220nF. Due to minimum on-time (t_{ON_MIN}), VSNS can exceed the SS pin voltage during startup. When this occurs, the device enters pulse-skipping mode.

The device is protected against output overvoltage, overload, and thermal fault conditions. The device minimizes excessive output overvoltage transients by using the overvoltage comparator circuit in power-good and the overvoltage COMP comparator (V_{COMP_OV}). When overvoltage protection activates, both the high-side and low-side MOSFETs turn off and remain off until the VSNS pin voltage drops below 105% of V_{REF} (typically). The device implements overload protection for both the high-side MOSFET and the low-side MOSFET (sinking), which helps control inductor current and prevent current runaway. The switching frequency folds back when the VSNS voltage drops below 248mV to protect the FETs from overstress during hard-short faults. The device also shuts down if the junction temperature exceeds the thermal shutdown trip point (typically 180°C). When the junction temperature drops 32°C (typical) below the thermal shutdown trip point, the device automatically restarts under control of the soft-start circuit.

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8.2 Functional Block Diagram



A. V_{REF} is a nominal 1V reference derived from the bandgap voltage.

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8.3 Feature Description

8.3.1 Power VIN Pins (PVIN)

The PVIN pins provide power to all internal control circuitry and the load, and have a recommended voltage range of 10V to 38V. The PVIN pins incorporate an internal undervoltage lockout (UVLO) comparator with typical rising and falling voltages of 9.48V and 8.78V, respectively. This maintains the internal circuitry of the device in a known off state until a minimum voltage is reached. If the voltage falls below these values, the device turns off.

As described in Section 8.3.4, use a voltage divider connected to the EN to configure the effective device UVLO externally, if desired. Connect the input bulk capacitance (C_{IN}) as close to PVIN pins as possible. A minimum input capacitance of 4.7µF is required at PVIN.

8.3.2 Voltage Reference

The device generates an internal nominal 1.2V bandgap reference voltage. This is the voltage present on the REFCAP pin during steady-state operation. A 1nF capacitor to ground is required at the REFCAP pin for proper electrical operation and to maintain robust SET performance of the device. This bandgap voltage is used to derive the nominal 1V reference voltage for the error amplifier, V_{REF}.

The reference voltage fed into the error amplifier is used to set the output voltage. However, error amplifiers have intrinsic offset that contributes to overall accuracy error. V_{REF} is measured with the error amplifier in unity gain, so the measurement includes the offset error. V_{REF} is typically 1V and is designed to be accurate to ±1% across line (input voltage), temperature, and TID. Because V_{REF} is measured in an open-loop configuration, the effects of switching frequency and load are not included in the specification. However, these effects are minimal compared to the already considered effects, see Figure 6-38.

8.3.3 Setting V_{OUT}

The output voltage is set with a resistor voltage divider. A top resistor is connected from the output voltage node (V_{OUT}) to the VSNS pin, and a bottom resistor is connected from VSNS to GND. Refer to Figure 8-1 for the connection configuration. TI recommends using 0.1% tolerance resistors.

Begin with a 10kΩ resistor for R_{F_TOP} and use Equation 1 to determine the appropriate value for the bottom feedback resistors (R_{F_BOT}). For better efficiency during light-load conditions, higher-value resistors can be used. However, be aware that excessively high resistance values can make the regulator more susceptible to noise and can cause noticeable voltage errors due to the VSNS input current (I_{VSNS_LKG}). See SLVA450 for details on how resistor value selection affects accuracy.

$$R_{F_BOT}\,(\Omega) = \left(\frac{V_{REF}\,(V)}{V_{OUT_TARGET}\,(V) - V_{REF}\,(V)}\right) \times R_{F_TOP}\left(\Omega\right) \quad (1)$$

where:

- V_{REF} = 1V (typ)
  - For more details on the V_{REF} parameter, refer to the VOLTAGE REFERENCE section in Electrical Characteristics.
- V_{OUT_TARGET} represents the desired nominal output voltage in Volts (V).
- R_{F_TOP} represents the selected top resistor in the resistive voltage divider in Ohms (Ω).

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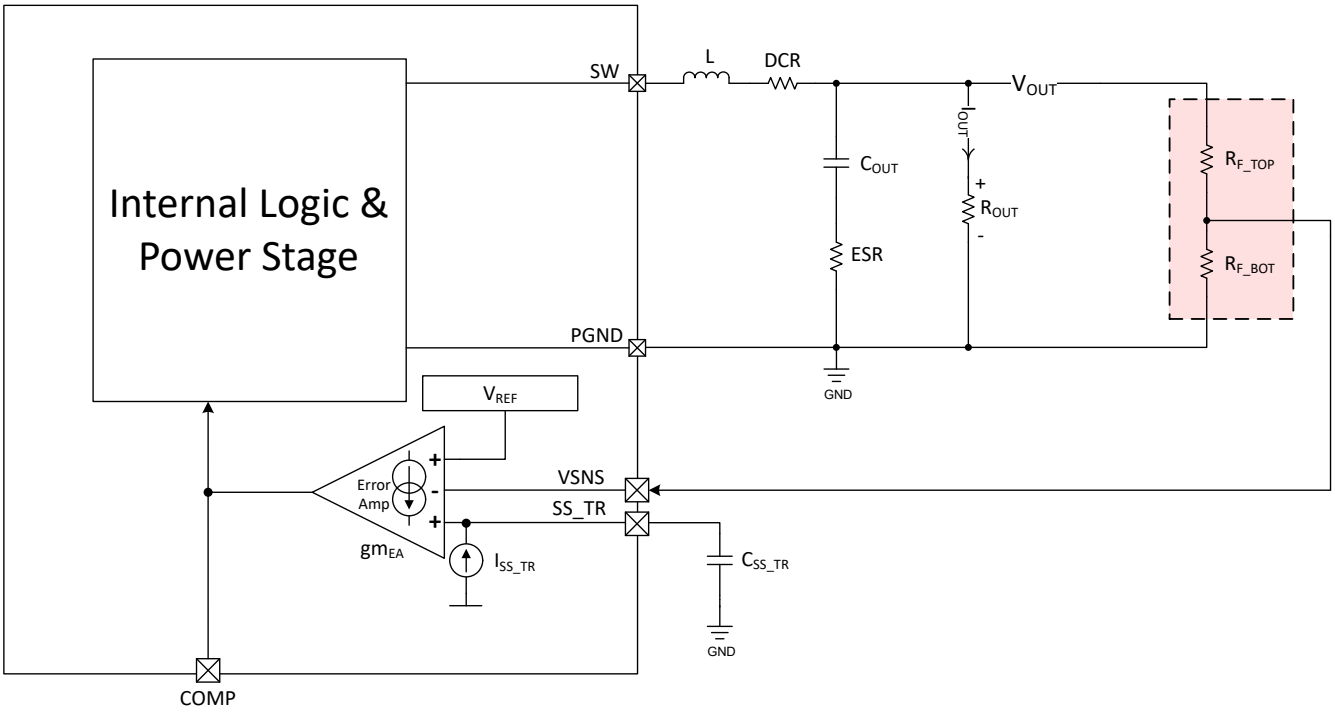


Figure 8-1. Programming V_{OUT} using Resistive Feedback Divider

8.3.3.1 Pulse-Width Limitations

The TPS7H4203 enforces a maximum pulse-width on the modulator. Operating near the upper-bound of the pulse-width can result in erratic SW pulses and excessive power dissipation due to internal device parasitics. To minimize this scenario, the TPS7H4203 enforces minimum off time. By consequence a maximum output voltage limit is imposed. On the other hand, the minimum on-time is imposed due to system requirements along with circuit limitations.

The maximum and minimum boundaries of the output voltage (V_{OUT}) can be approximated as described in the following sections:

- Minimum Output Voltage
- Maximum Output Voltage

8.3.3.1.1 Minimum Output Voltage

Minimum on-time (t_{ON_MIN}) limitations arise due to blanking time, limited sourcing and sinking driver capability, and propagation delays in the TPS7H4203. By consequence the minimum output voltage is limited by:

- Minimum on time (t_{ON_MIN}).
- Reference voltage (V_{REF}).

This minimum output voltage can be calculated using Equation 2:

$$V_{OUT_MIN}\left(V\right) \cong \begin{cases} PVIN\ (V) \times t_{ON_MIN}\ (s) \times f_{SW}\ (Hz), & if\ V_{OUT_MIN} \geq V_{REF} \\ V_{REF}\ (V), & Otherwise \end{cases} \quad (2)$$

Where:

- V_{OUT_MIN} is the minimum achievable output voltage in Volts (V)
- PVIN is the operating power input voltage of the I.C. and load in Volts (V)
- t_{ON_MIN} is the minimum on-time of the TPS7H4203 in seconds (s)
  - Refer to *MINIMUM ON, OFF and DEAD TIME* section in Electrical Characteristics for more details.
- f_{SW} is the switching frequency in Hertz (Hz)

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  - Refer to *SWITCHING FREQUENCY AND SYNCHRONIZATION* section in Electrical Characteristics for more details.
- V_{REF} is the internal reference voltage in Volts (V)
  - Refer to *VOLTAGE REFERENCE* section in Electrical Characteristics for more details.

Table 8-1 shows the calculated minimum output voltage at selected cases of PVIN and f_{SW}.

Table 8-1. Calculated Minimum Output Voltages

f_{SW} (kHz)	V_{IN} (V)	V_{OUT_MIN} (V)(4)
100(1)	10	V_{REF}(5)
	12	
	28	1.17
	38	1.59
	42	1.29
250(2)	10	1.05
	12	1.25
	28	2.93
	38	3.97
	42	4.39
500(3)	10	2.09
	12	2.51
	28	5.85
	38	7.94
	42	8.78

(1) The maximum switching frequency value for R_{RT} = 97.6kΩ is used for the calculation.
(2) The maximum switching frequency value for R_{RT} = 37.9kΩ is used for the calculation.
(3) The maximum switching frequency value for R_{RT} = 18.7kΩ is used for the calculation.
(4) The maximum value for the t_{ON_MIN} = 380ns is used for the calculation.
(5) V_{REF} is the internal reference voltage.

8.3.3.1.2 Maximum Output Voltage

Unlike NMOS/NMOS buck regulators, where the maximum voltage limitation stems from bootstrap capacitor re-charge rates, the TPS7H4203 uses internal circuitry to enforce the minimum off time. The maximum output voltage can be approximated using Equation 3.

$$V_{OUT_MAX}\,(V) \cong PVIN\,(V) \times \left[1 - \left(t_{OFF_MIN}\,(s) \times f_{SW}\,(Hz)\right)\right] \quad (3)$$

Where:

- V_{OUT_MAX} is the maximum achievable output voltage in Volts (V).
- PVIN is the operating power input voltage of the I.C. and load in Volts (V).
- t_{OFF_MIN} is the minimum off-time in seconds (s).
  - Refer to *MINIMUM ON, OFF and DEAD TIME* section in Electrical Characteristics for more details.
- f_{SW} is the switching frequency in Hertz (Hz).
  - Refer to *SWITCHING FREQUENCY AND SYNCHRONIZATION* section in Electrical Characteristics for more details.

Table 8-2 shows the calculated maximum output voltage at selected cases of PVIN and f_{SW}.

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Table 8-2. Calculated Maximum Output Voltages

f_{SW} (kHz)	V_{IN} (V)	V_{OUTx_MAX} (V)(4)
100(1)	10	9.66
	12	11.60
	28	27.06
	38	36.73
	42	40.59
250(2)	10	9.16
	12	10.99
	28	25.65
	38	34.81
	42	38.48
500(3)	10	8.32
	12	9.99
	28	23.30
	38	31.63
	42	34.95

(1) The maximum switching frequency value for R_{RT} = 97.6kΩ is used for the calculation.
(2) The maximum switching frequency value for R_{RT} = 37.9kΩ is used for the calculation.
(3) The maximum switching frequency value for R_{RT} = 18.7kΩ is used for the calculation.
(4) The maximum value for the t_{OFF_MIN} = 305ns is used for the calculation

8.3.4 Enable

The EN pin provides electrical on/off control for the TPS7H4203 and connects to the non-inverting input of a comparator with hysteresis (103mV typical).

When the EN pin is at a logical low level (V_{EN} < 475mV), the device enters shutdown mode and stops regulating the output voltage. During shutdown, both FETs remain in a high-impedance state, and the current consumption of the device decreases to a maximum of 0.53mA. When the device is disabled, the soft-start pull-down is turned on (active) to discharge the soft-start capacitor. The soft-start has a maximum pull-down resistance of 103Ω and remains active for a minimum of 190µs ($SS_TR_{SHDN_TIME}$). To activate the device, apply a logical high voltage to the EN pin (V_{EN} > 633mV). Once enabled, the output voltage begins regulation under soft-start control.

If desired, users can adjust the turn-on or turn-off voltage threshold externally by connecting a resistive divider between PVIN and GND, with the output connected into the EN pin as shown in Figure 8-2. The resistor values can be selected to enable or disabled the device when the input voltage reaches a specific desired level (or threshold) during a rising or falling input voltage.

The external undervoltage lockout (UVLO) must be set higher than the maximum value of the internal PVIN UVLO, which is 9.74V during rising input voltage and 9.15V during falling input voltage. While users can control either the external rising or falling UVLO threshold, the opposite edge is determined by the internal enable reference and hysteresis voltage (that is, the rising and falling enable references).

To program an external UVLO, follow these steps:

1. Select the desired external rising or falling undervoltage lockout voltage. This is referred to as V_{UVLO_TARGET}.
2. Select the top resistor value for the resistive voltage divider (R_{EN_TOP}).
   - A good starting value is 10kΩ. Higher values can be used in the application to minimize power consumption. However, this comes at the expense of greater susceptibility to noise, and the error associated with the EN leakage (I_{EN_LKG}) becomes more noticeable. The maximum value for the top resistor is 400kΩ.

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3. Calculate the bottom resistor for the resistive voltage divider (R_{EN_BOT}) using Equation 4.
   - In this equation, V_{EN} refers to the enable reference voltage for the desired edge to control (rising or falling). Use:
     - $V_{EN} = V_{EN_RISING}$ (605mV typical) when the rising voltage UVLO is the desired edge to control.
     - $V_{EN} = V_{EN_FALLING}$ (502mV typical) when the falling voltage UVLO is the desired edge to control.
4. Select the closest standard resistor value (based on the resistor tolerance series) to minimize error.
5. Calculate the external nominal rising and falling UVLO for the desired channel using Equation 5 and Equation 6, respectively. Use the selected components values for the top and bottom resistors.

$$R_{EN_BOT_TARGET}\left(\Omega\right) = \left(\frac{V_{EN}\left(V\right)}{V_{UVLO_TARGET}\left(V\right) - V_{EN}\left(V\right)}\right) \times R_{EN_TOP}\left(\Omega\right) \quad (4)$$

$$V_{UVLO_RISING}\left(V\right) = \left(1 + \frac{R_{EN_TOP}\left(\Omega\right)}{R_{EN_BOT}\left(\Omega\right)}\right) \times V_{EN_RISING}\left(V\right) \quad (5)$$

$$V_{UVLO_FALLING}\left(V\right) = \left(1 + \frac{R_{EN_TOP}\left(\Omega\right)}{R_{EN_BOT}\left(\Omega\right)}\right) \times V_{EN_FALLING}\left(V\right) \quad (6)$$

Where:

- $R_{EN_BOT_TARGET}$ is the calculated bottom resistor in ohms (Ω) to set the external UVLO at the desired V_{UVLO_TARGET} in volts (V).
- V_{EN} is the enable reference voltage in volts (V), given the desired edge to control.
- R_{EN_TOP} is the selected top resistor for the divider in ohms (Ω).
- R_{EN_BOT} is the selected bottom resistor for the divider in ohms (Ω).
- V_{EN_RISING} (605mV typical) is the enable reference during a rising voltage in volts (V)
- $V_{EN_FALLING}$ (502mV typical) is the enable reference during a falling voltage in volts (V)
- V_{UVLO_RISING} is the calculated actual rising external UVLO in volts (V).
- $V_{UVLO_FALLING}$ is the calculated actual falling external UVLO in volts (V).

Alternatively, the EN pin can be driven directly from a microcontroller or FPGA. The low voltage threshold of the enable pin supports of 1.1V, 1.8V, 2.5V, and 3.3V logic levels.

If needed, a small capacitor can be placed in parallel with EN and GND as shown in Figure 8-2. This capacitor can be used to:

- Minimize noise in the EN pin voltage.
- Filter fast transients that otherwise can turn on/off the channel.
- Delay the turn-on of the device.

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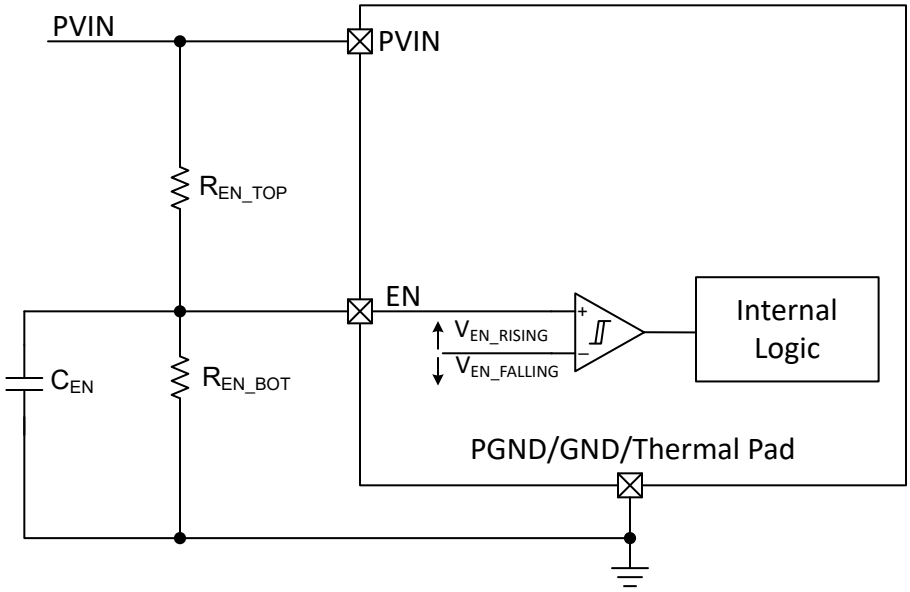


Figure 8-2. External UVLO Resistive Divider in EN

Note

Disabling the device through the EN pin shuts down the VBIASP and REFCAP rails to minimize current consumption. During shutdown, VBIASP is pulled to PVIN and REFCAP is pulled to GND.

8.3.5 Power Good (PWRGD)

The PWRGD pin is an open-drain output that is asserted when the output voltage (V_{OUT}) reaches an appropriate range. This assertion occurs by comparing the voltage at the VSNS pin with internal ratiometric reference voltages derived from REFCAP ($PWRGD_{UV_GOOD}$ and $PWRGD_{OV_FAULT}$). The PWRGD pin requires an external pull-up resistor to a voltage source with the desired logic level. The maximum recommended pull-up voltage for the PWRGD pin is 5.5V. Select a pull-up resistor value that limits the maximum current sunk by PWRGD to under the recommended operating condition of 2mA. A 10kΩ pull-up resistor is generally sufficient. While larger resistor values minimize power dissipation, the weaker pull-up strength can allow switching noise to couple into the PWRGD signal.

The PWRGD signal logical states are:

1. Asserted (high impedance or logic high): when the V_{OUT} voltage in percent of final (nominal) value is:
   - Between 93% to 98% during a rising voltage (from an undervoltage or power-up condition).
   - Between 102% to 107% during a falling voltage (from an overvoltage condition).
2. Deasserted (low impedance or logic low) when the V_{OUT} voltage in percent of final (nominal) value is:
   - Between 90% to 95% during a falling voltage (or an undervoltage condition).
   - Between 104% to 111% during a rising voltage (or overvoltage condition).

The responses of PWRGD to UV_GOOD and UV_FAULT are shown in Figure 8-3, while the OV_FAULT and OV_GOOD are presented on Figure 8-4. The PWRGD is in a defined state when the PVIN input voltage is greater than 2.8V, but has reduced current sinking capability (See Figure 8-5). PWRGD achieves full current sinking capability when PVIN reaches the V_{UVLOR_PVIN} (9.74V max). During an overvoltage event as detected by the $PWRGD_{OV_FAULT}$ threshold, the high and low side FETs are forced into high impedance to protect the load. Once the output voltage overvoltage is cleared as detected by the $PWRGD_{OV_GOOD}$ threshold the SW resumes pulsing.

In addition to the above description, PWRGD is deasserted (forced low) during other conditions that cause regulation to stop such as:

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- PVIN UVLO
- Thermal shutdown
- The device is disabled by forcing a logic low in EN
- The COMP voltage reaches $COMP_{SHDN}$ (typically 2V)
  - $COMP_{SHDN}$ forces a re-start of VOUT by discharging the SS_TR capacitor for a typical 316µs

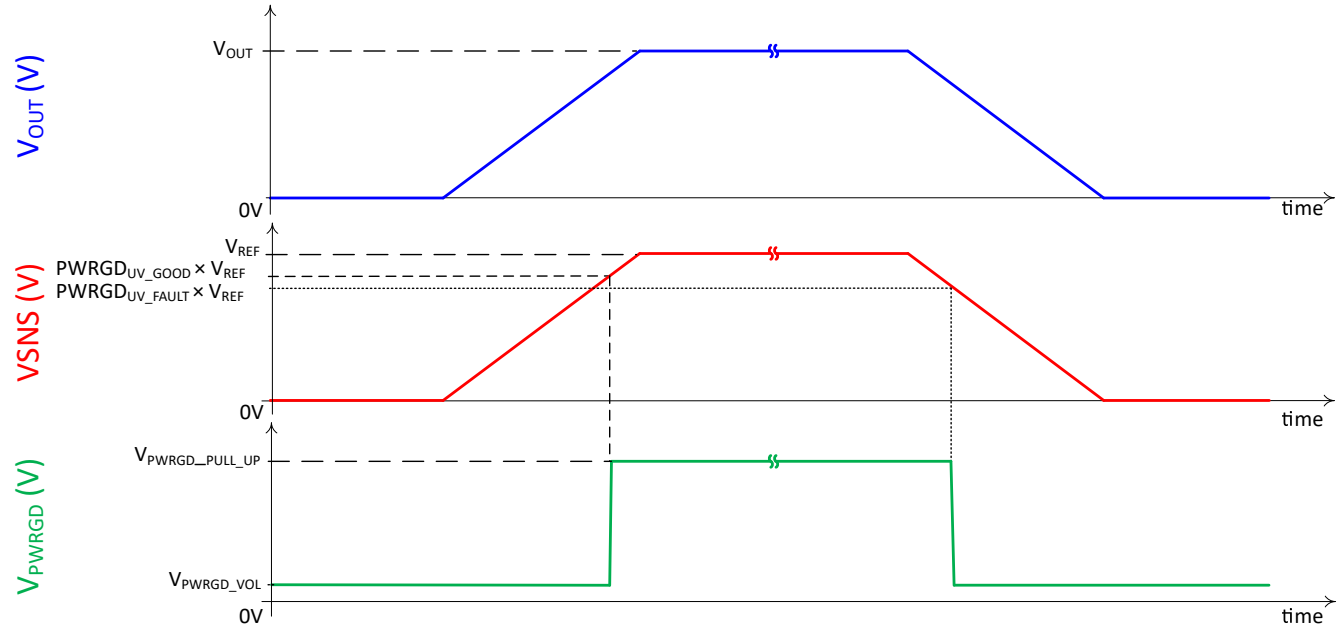


Figure 8-3. PWRGD Undervoltage (UV) Thresholds

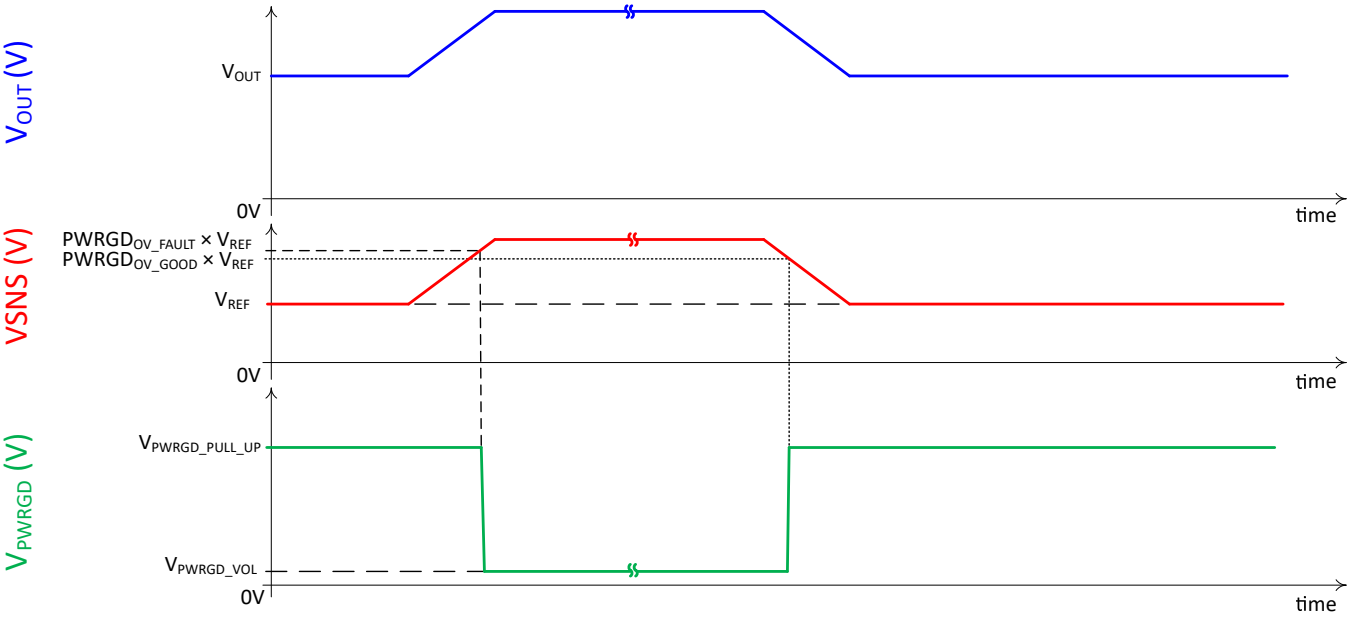


Figure 8-4. PWRGD Overvoltage (OV) Thresholds

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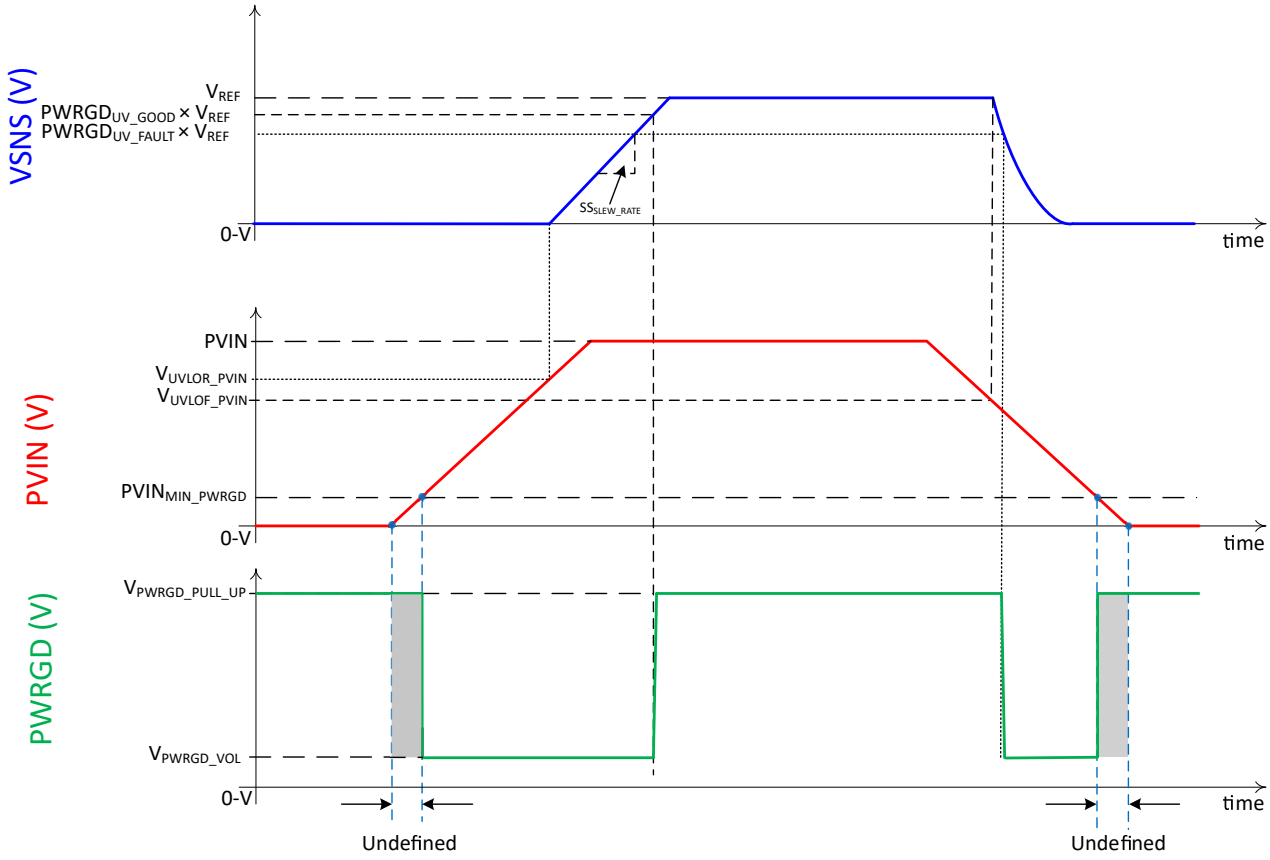


Figure 8-5. PWRGD in Valid States After PVIN > $PVIN_{MIN_PWRGD}$

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8.3.6 Adjustable Switching Frequency and Synchronization

There are three clocking mode options available on the TPS7H4203:

1. Internal Clock Mode
2. External Clock Mode
3. Internal Clock: Primary-Secondary

The RT and SYNC pin configurations for these modes are detailed in Table 8-3. The switchover from internal to external and vice versa is described in the Clock Switchover section.

Table 8-3. Clock Modes

MODE	INPUT CONFIGURATION FOR CLOCK	SYNC CLOCK	
	RT	SYNC State	SYNC OUTPUT
Internal clock	Resistor from RT to GND	N/A	No output
External clock		Input	Input f_{SW} clock in phase
Internal clock: Primary-Secondary	Open	Output	Output f_{SW}= 250kHz with 180° out of phase of primary.

8.3.6.1 Internal Clock Mode

In internal clock mode (also sometimes called internal oscillator mode), a resistor is connected between the RT pin and GND to configure the switching frequency, f_{SW}, of the device. The nominal switching frequency is adjustable from 100kHz to 500kHz depending on the RT resistor value, which can be calculated using Equation 7. Figure 8-6 shows the relationship curve between the RT resistor value and the configurable switching frequency range.

$$\mathrm{RT}\left(\mathrm{k\Omega}\right) = 9863.7 \times \left[\frac{1}{f_{SW}(\mathrm{kHz})}\right] - 1.142 \tag{7}$$

where

- RT in kΩ
- f_{SW} in kHz

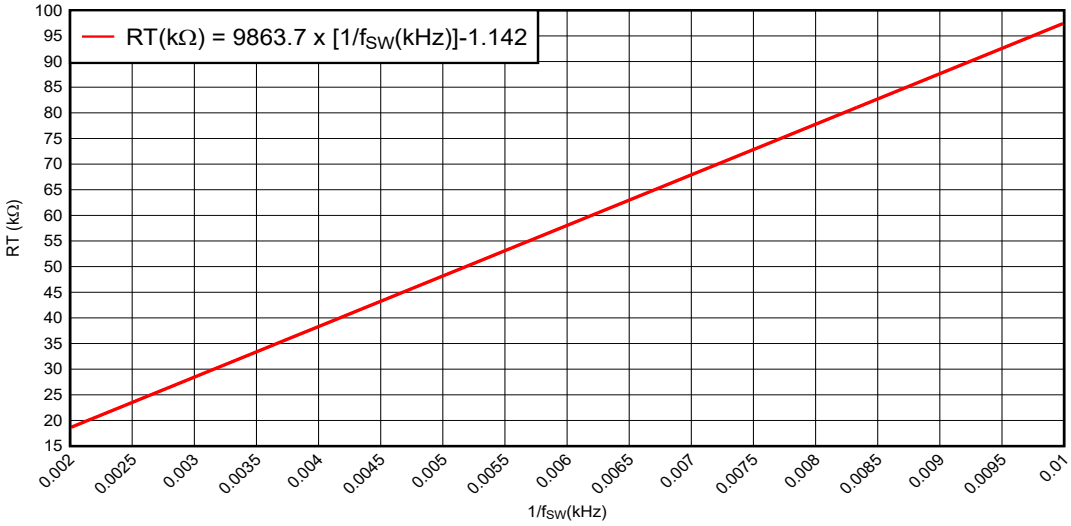


Figure 8-6. Nominal RT vs Switching Frequency

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8.3.6.2 External Clock Mode

In external clock mode (also called external oscillator mode), a resistor is connected between the RT pin and GND to set the desired switching frequency. The resistor value can be calculated using Equation 7.

The SYNC input requires a toggling (CLK) signal that meets the following requirements:

- Duty cycle between 40% and 60%.
- Frequency within ±20% of the programmed nominal switching frequency by RT resistor.
- Low logic voltage level as: $0V \le V_{SYNC} \le 0.6V$.
- High logic voltage level as: $4.5V \le V_{SYNC} \le 5.5V$.

The external clock can be provided by an oscillator, FPGA, or other compatible device. Alternatively, the external clock can also be provided by another TPS7H4203 device that is configured in primary-secondary mode. This configuration is detailed in Section 8.3.6.3.

Note

When the SYNC pin is not used (internal oscillator mode), the SYNC pin must be connected to GND via a low impedance to minimize coupling. Noise coupled into the pin is interpreted as an external clock if internal thresholds are met, potentially causing erratic pulses at the switch node. A 50Ω resistor from the SYNC pin to GND is a recommended option when switching the device from internal to external oscillator mode; this resistor provides a low-impedance termination and serves as the de facto standard for maintaining signal integrity.

8.3.6.3 Internal Clock: Primary-Secondary

Primary-secondary device synchronization is a system-level configuration that uses a primary device in internal clock mode and a secondary device in external synchronization mode. When this mode is selected, the switching frequency is internally fixed to a nominal value of 250kHz. This configuration enables paralleling of two devices, with an 180° (degrees) phase shift, minimizing output current ripple.

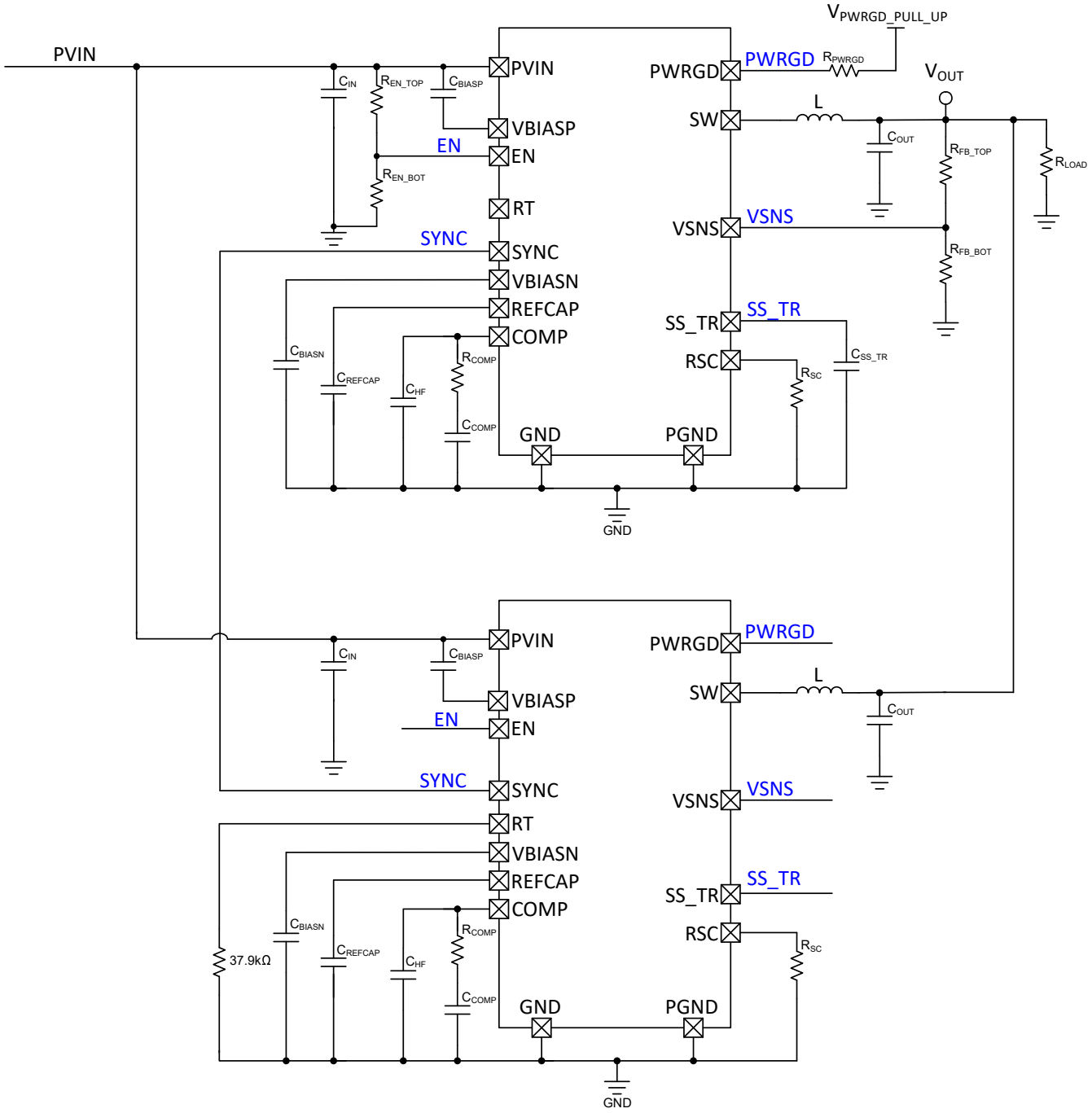
The primary device is configured in internal oscillator mode by floating (open) the RT pin. When the RT pin is left floating the device is internally configured as:

- f_{SW} = 250kHz
- SYNC outputs a clock at 250kHz with a 180° phase shift with respect to the internal clock.
  - The phase shift between SYNC and $SW_{PRIMARY}$ is greater than 180°, due to internal delays. However this offset is canceled on the secondary as both devices have similar delays. The effective phase shift between the $SW_{PRIMARY}$ and $SW_{SECONDARY}$ is nominally 180°.
  - SYNC output high level is typically 5V.

The secondary device is configured by connecting a 37.9kΩ on the RT pin and shorting the SYNC pins together.

Figure 8-7 shows a simplified schematic of the primary-secondary configuration. Tie together the signals colored blue for parallel operation. See Section 9.2.4 for additional information.

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A. The TPS7H4203 at the top is referred to as the primary device since it generates the clock signal used by the secondary TPS7H4203 at the bottom.

Figure 8-7. Simplified Parallel Schematic

8.3.6.4 Clock Switchover

The TPS7H4203 requires a resistor connected from RT to GND in both internal and external clock modes. This resistor programs the internal oscillator to the desired frequency. When a clock signal is detected on the SYNC pin, the device switches (or synchronizes) to the external clock within $2\times T_{SYNC}$ ($t_{CLK_I_E}$) clock periods of the SYNC clock. Due to internal circuit propagation delays, the switch node exhibits a small timing difference (or phase shift) as specified by the t_{SYNC_DLY} (typically 320ns). Refer to Figure 8-8 for more details.

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If the SYNC clock is not detected (or loss), the TPS7H4203 switches to the internal clock. The switchover occurs within 4×T_{OSC} ($t_{CLK_E_I}$) clock periods of the internal oscillator clock, see Figure 8-9.

Note

During the transition from external to internal oscillator, switching is suspended; consequently, V_{OUT} drops as L and C_{OUT} supply the load current. The drop magnitude depends on these components. When switching resumes, the control loop extends the duty cycle to restore V_{OUT}. The aggressiveness of this correction depends on the loop crossover frequency (f_C); a higher f_C results in a faster, larger duty-cycle extension. Depending on L, C_{OUT}, and f_C, this correction can momentarily trip the current limit and/or trigger a COMP shutdown event. If loss-of-clock is possible in the application, validate the system response (L, C_{OUT}, f_C) to confirm the current limit is not triggered during this transition.

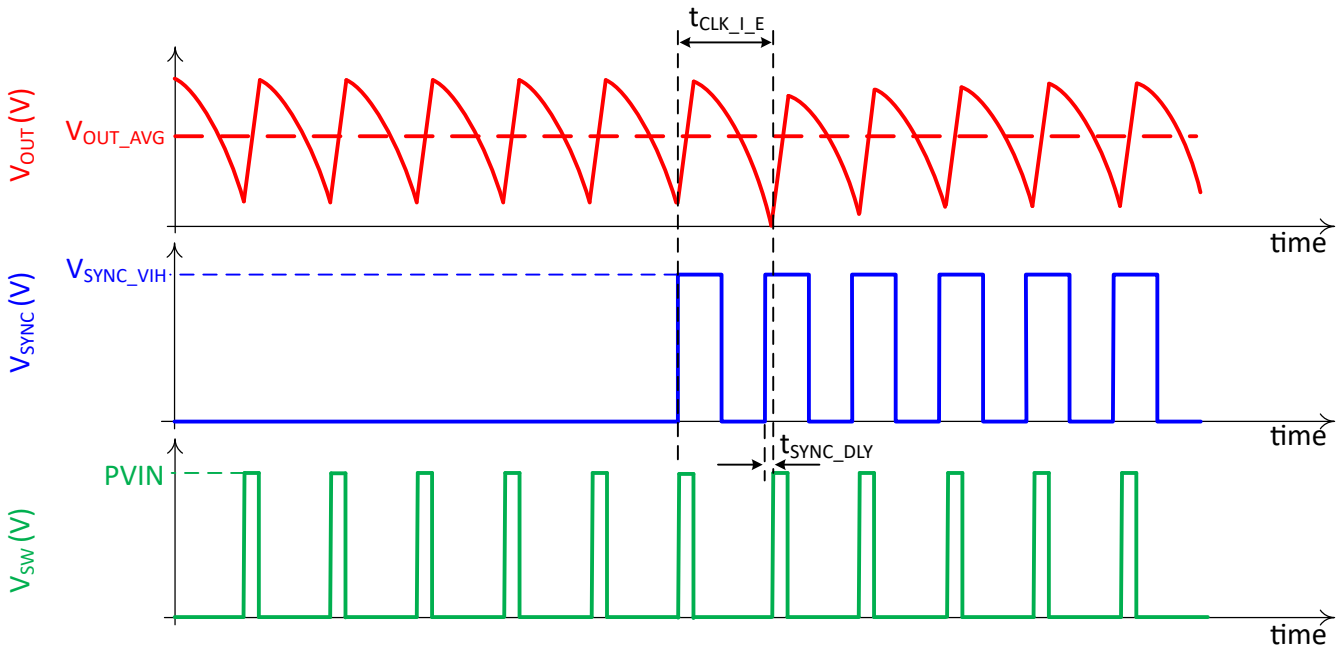


Figure 8-8. Internal to External Clock Switchover

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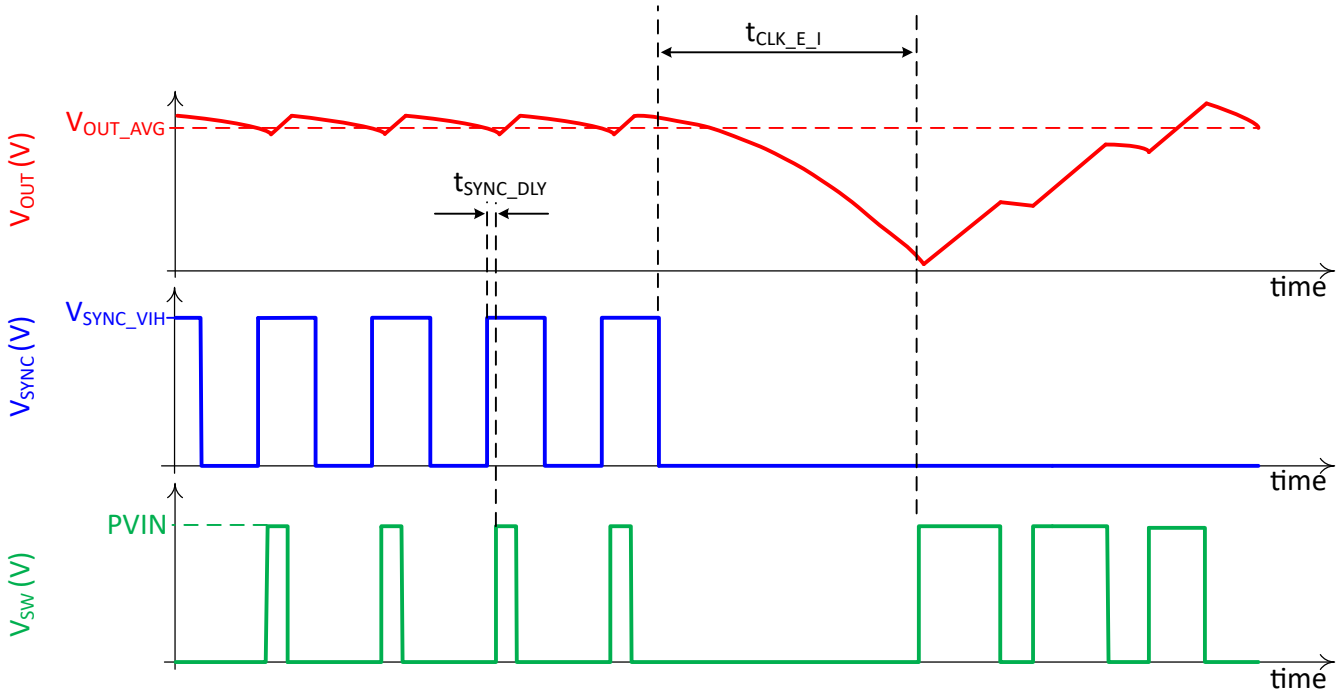


Figure 8-9. External to Internal Clock Switchover

8.3.7 Switching Frequency Foldback

During strong short circuits (low impedance) at the output voltage of the converter, the current is limited internally. However, this increased current state results in abnormal power dissipation in the internal FETs. To minimize switching losses in the device, the TPS7H4203 reduces the switching frequency through a foldback mechanism. This frequency foldback action occurs when the VSNS voltage falls below $V_{TH_FOLDBACK_FALLING}$ (typically 248mV).

The oscillator (or switching frequency) is reduced by a ratio of 2 or 4, depending on the programmed frequency as determined by the RT resistor. If the switching frequency is programmed above 167kHz, the ratio is 4; otherwise, it is 2. This behavior also occurs during start-up (or soft-start) when VSNS is below $V_{TH_FOLDBACK_FALLING}$.

Note

When the device is in foldback mode (VSNS < $V_{TH_FOLDBACK_FALLING}$), the low-side switch is prevented from turning on, and conduction occurs through the body diode of the low-side FET.

8.3.8 Turn-On Behavior

8.3.8.1 Pulse Skipping During Start-up

The device enters pulse-skipping mode (hysteretic mode) during startup when VSNS exceeds the voltage at the SS_TR pin (VSNS>V_{SS_TR}). During this period, the high-side and low-side switches remains off (SW is high impedance) until VSNS falls below the SS_TR pin voltage again. This occurs because a lower output voltage is required than what can be supported by the minimum on-time specification.

As a result, instantaneous output voltage pulses can be higher or lower than the desired voltage level. This behavior is most evident when operating at high frequencies with high loop bandwidth or with high PVIN-to-V_{OUT} ratios. For more details on how to minimize this behavior, refer to SLVA866.

When the minimum on-pulse duration exceeds the minimum controllable on-time, pulse-skipping behavior is typically not observed during startup.

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8.3.8.2 Soft-Start (SS_TR)

The device uses the V_{SS_TR} as the tracking reference during start-up. A C_{SS_TR} capacitor connected from the SS_TR pin to GND implements soft-start timing by providing a slow ramp tracking reference. Equation 8 shows the nominal equation for the soft-start time, t_{SS_TR}, which is the time required for V_{OUT} to reach the programmed voltage.

$$t_{SS_TR}\left(ms\right) = \frac{V_{REF}(V) \times C_{SS_TR}(nF)}{I_{SS_TR}(\mu A)} \quad (8)$$

where:

- V_{REF} is the reference voltage in Volts. Typically 1V
- I_{SS_TR} is the soft start current in micro-amps (µA). Typically 11µA
- C_{SS_TR} is the soft start capacitor in nano-farads (nF).

During start-up when the output capacitor bank is discharged, a large in-rush current is required to quickly charge the bank. If this current is not controlled below the sourcing current limit, non-linearities can be observed due to the protection features of the device.

As good practice, the soft-start capacitor value — determined by a given output capacitor, maximum output current, and output voltage — cannot be lower than the value calculated by Equation 9. Once the desired soft-start time has been determined, the designer can use Equation 10 to calculate appropriate soft-start capacitor value.

$$t_{SS_TR}\,(s) = \left(\frac{C_{OUT}(F)}{6.1 - I_{OUT}(A)} \times V_{OUT}(V)\right) + \left(500 \times 10^{-6}\,s\right) \quad (9)$$

Where:

- C_{OUT} is the output capacitor in Farads (F)
- 6.1A is the minimum value from the high-side switch overcurrent threshold (I_{OC})
- I_{OUT} is the maximum expected load in Amps (A)
- V_{OUT} is the nominal output voltage in Volts (V)
- 500x 10^{-6} seconds (500µs) is the time offset from when the device is enabled to when it starts switching. This value can vary due to the loop compensation capacitors. The bigger the compensation capacitor (or lower loop cross-over frequency) the bigger this time constants are.

$$C_{SS_TR}\left(nF\right) = \frac{t_{SS_TR}(ms) \times I_{SS_TR}\,(\mu A)}{V_{REF}(V)} \quad (10)$$

Where:

- t_{SS_TR} is the minimum nominal soft-start time in milliseconds (ms)
- I_{SS_TR} (11µA) is the nominal soft-start current in micro-amps (µA)
  - For more details on the I_{SS_TR} refer to *SOFT START AND TRACKING* section in Electrical Characteristics.
- I_{OUT} is the maximum expected load in Amps (A)
- V_{OUT} is the nominal output voltage in Volts (V)

The SS_TR pin is discharged through the internal $R_{SS_TR_DISCHARGE}$ pull-down resistor (typically 72Ω) when any of the following four scenarios occur:

1. The input UVLO is triggered (PVIN < V_{UVLOF_PVIN})
2. The EN pin voltage is a logic low (V_{EN} < $V_{EN_FALLING}$)
3. The COMP pin reaches the $COMP_{SHDN}$ threshold
4. A thermal shutdown event occurs

When the SS_TR pin is discharged, the device cannot restart again until the $SS_TR_{SHDN_TIME}$ expires (typically 316µs) to provide proper soft-start behavior.

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Note

The Soft-Start pin must not be left floating. Depending on system components such as L, C_{OUT}, and the loop crossover frequency (f_{CO}), an open soft-start pin can prevent device startup by causing the device to hit current limits and reach the $COMP_{SHDN}$ voltage threshold.

8.3.8.3 Safe Start-Up Into Prebiased Outputs

The TPS7H4203 prevents the low-side MOSFET from continuously discharging a pre-biased output voltage. This is achieved by forcing the device to always begins switching by turning on the high-side PMOS, in conjunction with pulse-skipping (hysteretic) mode control during start-up.

8.3.8.4 Tracking and Sequencing

Many of the common power-supply sequencing methods can be implemented using the SS_TR, EN, and PWRGD pins of the TPS7H4203 such as:

- Sequential Start-Up Using EN and PWRGD
  - The sequencing methodology described in this section only offer sequence up control. For a more comprehensive sequence control the designers can use the TPS7H3014, a 3V to 14V space-grade sequencer.
- Ratiometric Start-Up Using Connected SS_TR Pins
- Ratiometric and Simultaneous Start-Up

Note

The diagrams shown in this section show two TPS7H4203 devices; however, this method can be used for as many regulators as needed. In this section, $V_{OUT_PRIMARY}$ and V_{OUT1}, as well as $V_{OUT_SECONDARY}$ and V_{OUT2}, are used interchangeably.

8.3.8.4.1 Sequential Start-Up Using EN and PWRGD

The block diagram connections for the sequential start-up method are shown in Figure 8-10, along with the timing diagram in Figure 8-11.

The PWRGD pin of the first device connects to the EN pin of the second device, enabling the second power supply after the primary supply reaches regulation. If additional delay is desired between sequencing the first and second devices, an optional C_{PWRGD} capacitor can be added to the PWRGD pin. This creates an RC delay based on the values of the power-good pull-up resistor and capacitor used.

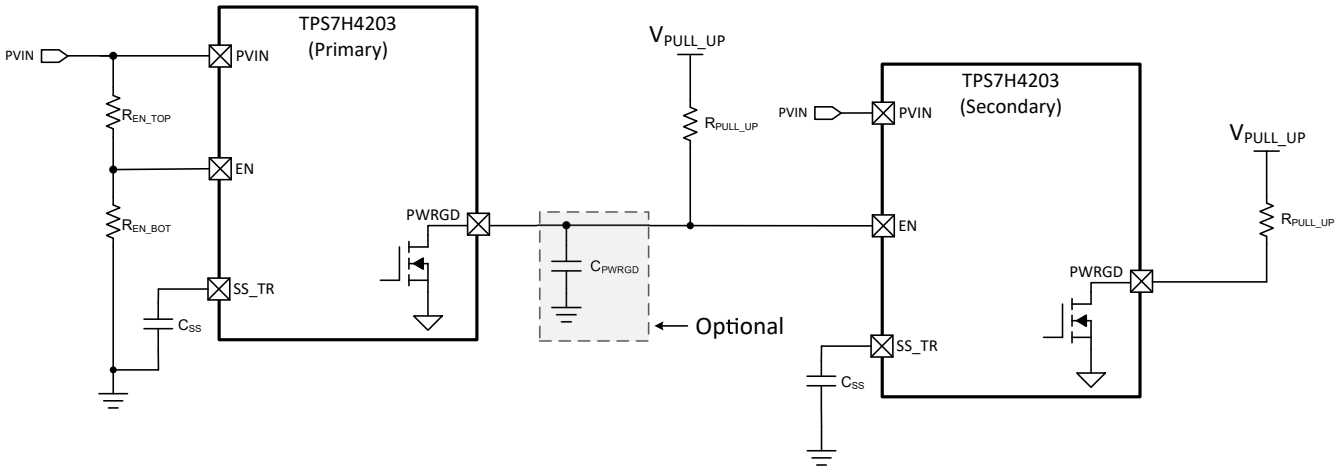
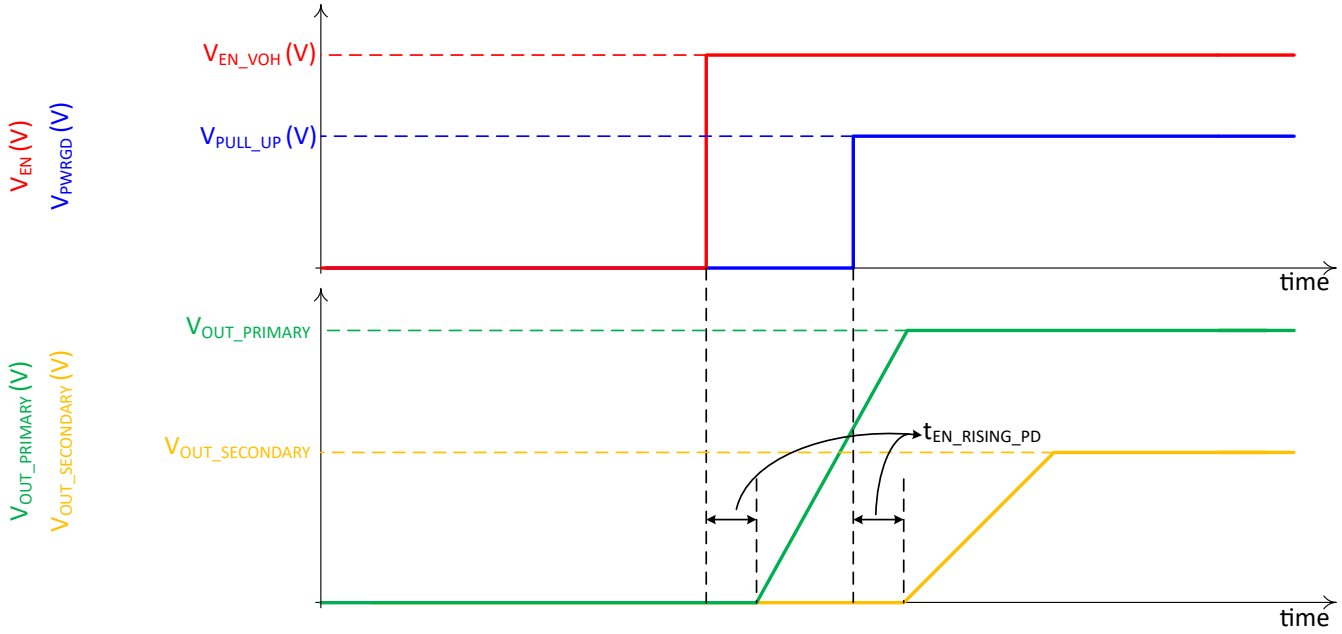


Figure 8-10. Sequential Start-Up Sequence Using PWRGD and EN Pins

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A. The red waveform is the EN of the primary device and the blue waveform is the PWRGD = EN (tied together) of the secondary device

Figure 8-11. Sequential Start-Up Sequence Using PWRGD and EN Pins Timing Diagram

8.3.8.4.2 Ratiometric Start-Up Using Connected SS_TR Pins

Figure 8-12 and Figure 8-13 shows the method for implementing ratiometric sequencing by connecting the EN and SS_TR pins of two devices together. This configuration forces both devices to turn on simultaneously since the devices share the same EN signal. The soft-start time (t_{SS_TR}) is identical for both devices because the shared soft-start reference, causing both devices to reach regulation simultaneously.

It is important to note that when multiple devices have the SS_TR pins tied together, the current that charges the soft-start capacitor (C_{SS_TR}) increases proportionally with the number of TPS7H4203 regulators connected, refer to Equation 11.

$$t_{SS_TR}\left(ms\right) = \frac{V_{REF}(V) \times C_{SS_TR}(nF)}{N \times I_{SS_TR}(\mu A)} \quad (11)$$

where:

- V_{REF} is the reference voltage in Volts. Typically 1V
- I_{SS_TR} is the soft start current in micro-amps (µA). Typically 11µA
- N is number of SS_TR pins connected together
- C_{SS_TR} is the soft start capacitor in nano-farads (nF)

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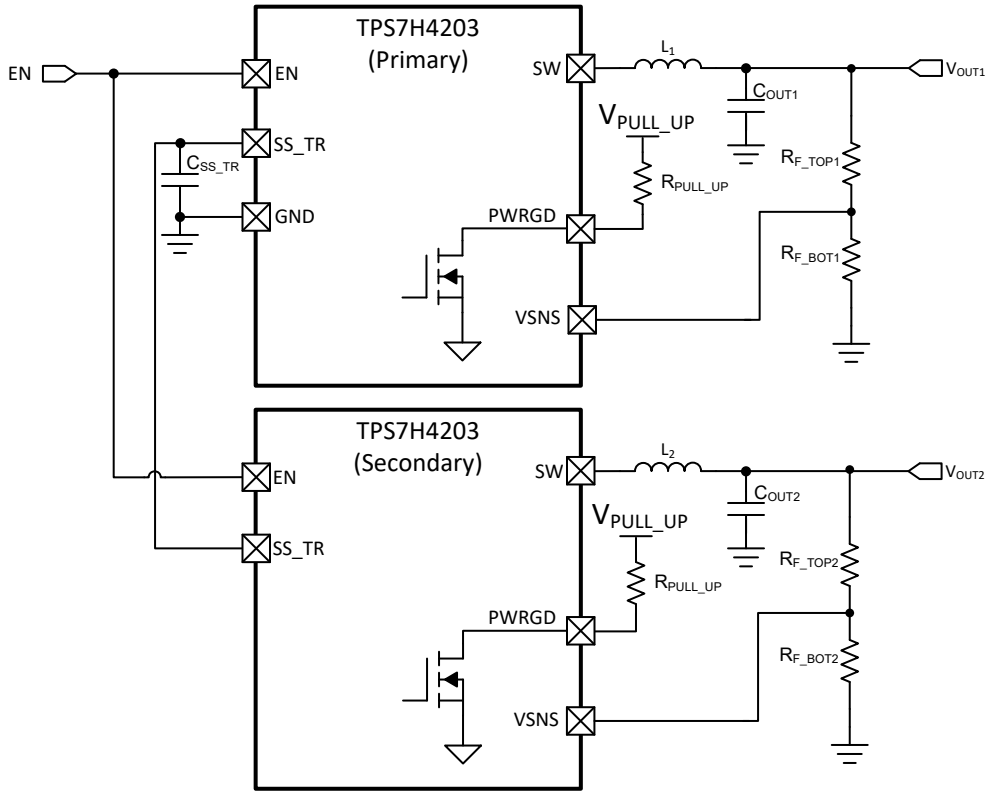
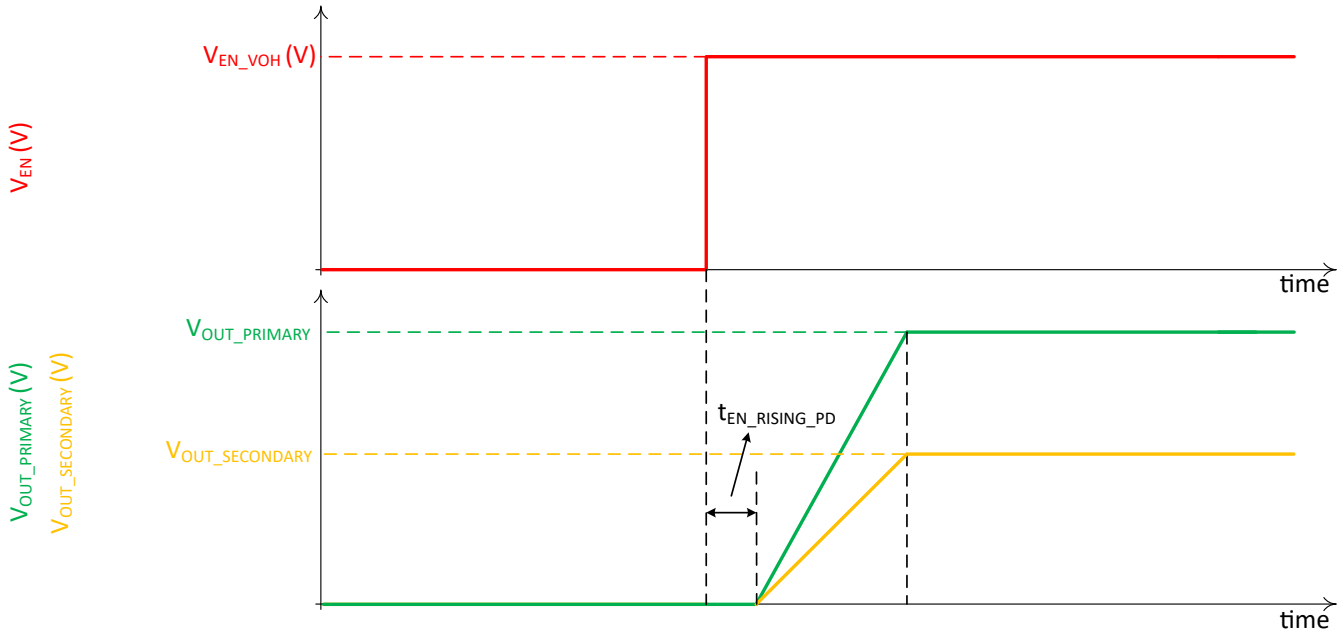


Figure 8-12. Ratiometric Start-Up Using the SS_TR Pins



A. Since the output voltages are different and the soft-start time (t_{SS_TR}) is the same for both devices, the slew rates are different.

Figure 8-13. Ratiometric Start-Up Using the SS_TR Pins Timing Diagram

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8.3.8.4.3 Ratiometric and Simultaneous Start-Up

In ratiometric and simultaneous start-up configurations, the enable pins of the converters are shared (tied together) to force the devices to start regulation simultaneously. The SS_TR pin of the primary device is configured with a capacitor connected to GND to set the desired soft-start time (t_{SS_TR}), as per Equation 8. The SS_TR pin of the secondary device is connected to the output of the primary device (V_{OUT1}) through a resistive divider, as shown in Figure 8-14. In this configuration, the $V_{OUT_SECONDARY}$ soft-start slope is determined by the $V_{OUT_PRIMARY}$ slope and is controlled by the R_1 and R_2 resistive divider.

In this configuration $V_{OUT_PRIMARY}$ (or V_{OUT1}) can lead, lag or simultaneously ramp with $V_{OUT_SECONDARY}$ (or V_{OUT2}). To select the appropriate resistors for such applications refer to Equation 12 to Equation 16.

If $V_{OUT_PRIMARY} > V_{OUT_SECONDARY}$ then in Equation 12:

- Positive values of ΔV means $V_{OUT_PRIMARY}$ leads $V_{OUT_SECONDARY}$
- Negative values of ΔV means $V_{OUT_SECONDARY}$ leads $V_{OUT_PRIMARY}$
  - Same as $V_{OUT_PRIMARY}$ lags $V_{OUT_SECONDARY}$
- Use ΔV = 0 for simultaneous tracking

Figure 8-15 through Figure 8-17 shows the timing diagrams for the possible application cases.

$$\Delta V\,(V) = V_{OUT_PRIMARY}\,(V) - V_{OUT_SECONDARY}\,(V) \tag{12}$$

$$R_{TH}\left(\Omega\right) = \frac{V_{SS_OFFSET}\,(V)}{I_{SS_TR}(A)} \tag{13}$$

$$k = \frac{V_{REF}\,(V) - \left[2 \times V_{SS_OFFSET}\,(V)\right]}{V_{OUT_SECONDARY}\,(V) + \Delta V\,(V)} \tag{14}$$

$$R_1\left(\Omega\right) = \frac{R_{TH}(\Omega)}{k} \tag{15}$$

$$R_2\left(\Omega\right) = \frac{R_{TH}\,(\Omega)}{1-k} \tag{16}$$

Where:

- V_{SS_OFFSET} is an arbitrary SS_TR voltage at $V_{OUT_PRIMARY}$ = 0V, set by I_{SS_TR} and the R1/R2 divider. A smaller offset voltage decreases the series resistance (R1 + R2), thereby increasing the load on $V_{OUT_PRIMARY}$.
- I_{SS_TR} = 11x 10^{-6}A (or 11µA) typically
- V_{REF} = 1V typically

Note

The V_{SS_TR} of the secondary device when $V_{OUT_PRIMARY}$ reaches steady state cannot exceed 5.5V. This voltage can be calculated using Equation 17.

$$V_{SS_TR}\left(V\right) = \left(V_{OUT_PRIMARY}\left(V\right) \times \left[\frac{R_2\,(\Omega)}{R_1(\Omega) + R_2(\Omega)}\right]\right) + \left(\left[\frac{R_1(\Omega) \times R_2(\Omega)}{R_1(\Omega) + R_2(\Omega)}\right] \times I_{SS_TR}\left(A\right)\right) \tag{17}$$

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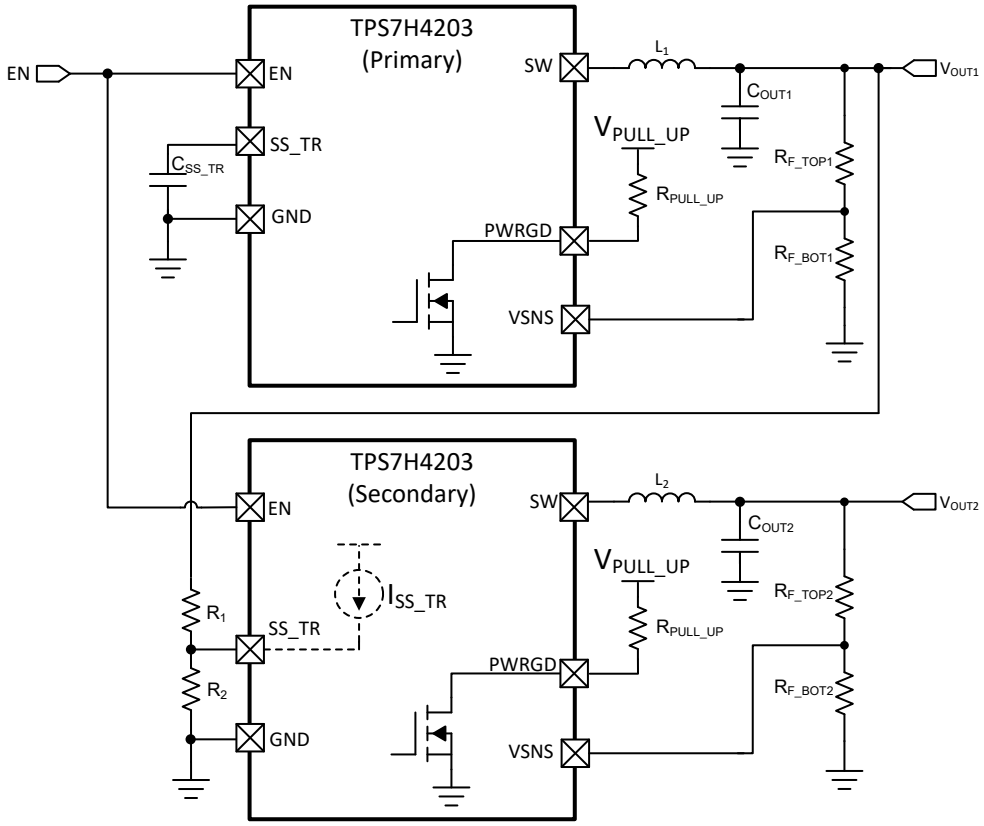


Figure 8-14. Ratiometric and Simultaneous Start-Up Using EN, $V_{OUT_PRIMARY}$ and SS_TR

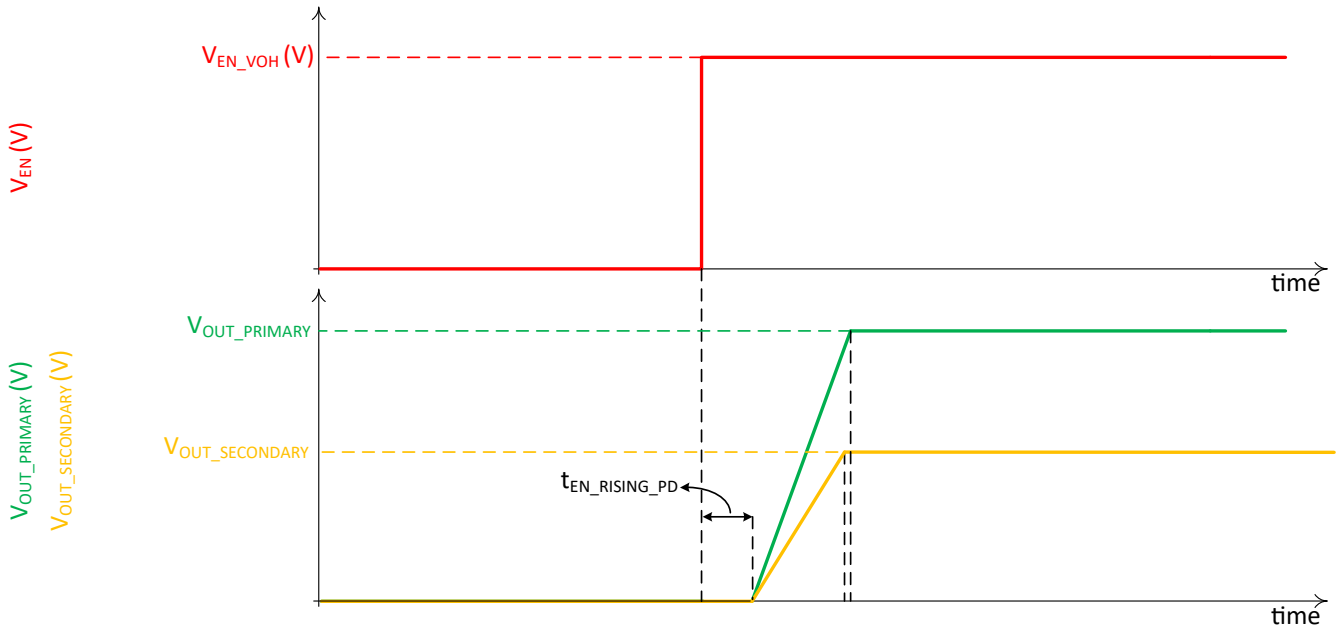


Figure 8-15. Ratiometric Start Up With $V_{OUT_PRIMARY}$ Leading $V_{OUT_SECONDARY}$

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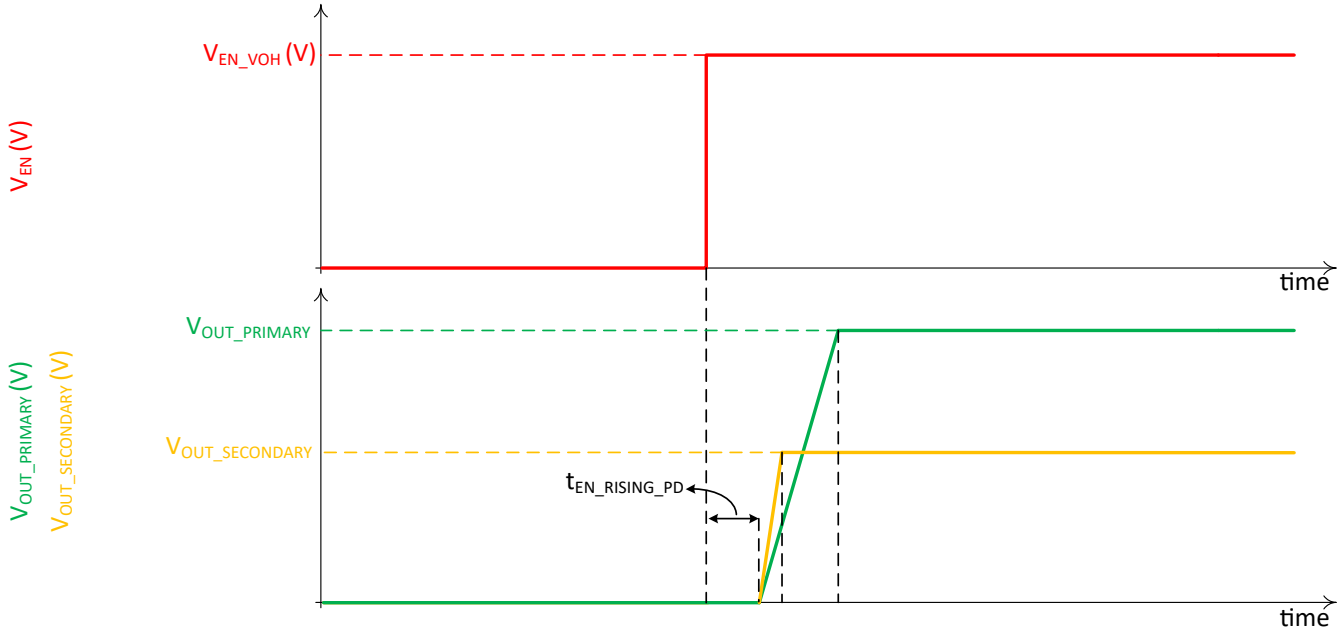


Figure 8-16. Ratiometric Start Up With $V_{OUT_SECONDARY}$ Leading $V_{OUT_PRIMARY}$

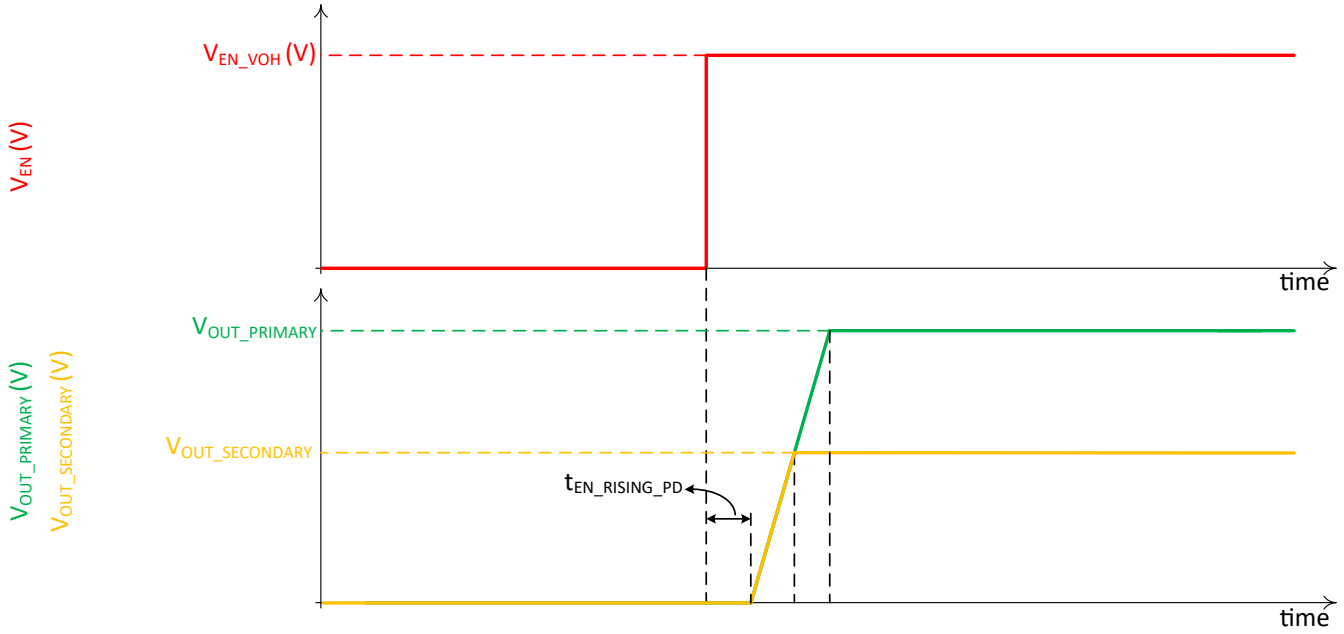


Figure 8-17. Simultaneous Start Up

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8.3.9 Protection Modes

The following protection modes are detailed in the following sections:

- Overcurrent Protection: Section 8.3.9.1
  - High-Side Overcurrent Protection (I_{OC}): Section 8.3.9.1.1
  - COMP Shutdown: Section 8.3.9.1.2
  - Low-Side Overcurrent Sinking Protection: Section 8.3.9.1.3
- Output Overvoltage Protection (OVP): Section 8.3.9.2
- Thermal Shutdown: Section 8.3.9.3

8.3.9.1 Overcurrent Protection

The TPS7H4203 uses multiple overcurrent protection mechanisms to safeguard both the device and the load. Primary protection is provided by a high-side MOSFET current limit (I_{OC}, typically 7.2A). When the high-side current exceeds I_{OC}, the device stops switching for the t_{OC} duration (typically 44µs). In the event of a short circuit or low-impedance load, V_{COMP} increments to compensate for the output voltage drop. If V_{COMP} exceeds $COMP_{SHDN}$ while an I_{OC} event is detected, the device halts switching for the $SS_TR_{SHDN_TIME}$ period (typically 316µs). In both scenarios, the high-side and low-side switches enter a high-impedance state for the respective protection durations (44µs for I_{OC} and 316µs for $COMP_{SHDN}$). Additionally, to reduce internal stress, the switching frequency folds back (by a factor of 2 or 4) when VSNS falls below $V_{TH_FOLDBACK_FALLING}$ (typically 248mV). Finally, a low-side sinking overcurrent protection is included, which immediately turns off the low-side switch upon detection to prevent excessive sinking current. Detailed descriptions of these mechanisms follow in the subsequent sections.

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8.3.9.1.1 High-Side Overcurrent Protection (I_{OC})

The TPS7H4203 implements a high-side current limit that protects the device and the load. During the on-time, the high-side FET current is compared to an internal current limit reference (I_{OC}). When the current through the high-side FET exceeds the current limit value of 7.2A (typ.), the device stops switching and holds both the high-side and low-side FETs open (SW is high impedance) for the duration of t_{OC} (typically 44µs). During this time, the inductor current begins conducting through the low-side FET body diode to the load. Depending on the slew rate of the high-side current — controlled by the inductor, PVIN, and V_{OUT} — the current through the high-side FET can exceed the current limit value due to the limited bandwidth of the comparator used to detect the overcurrent event.

Note

The I_{OC} current limit is a DC threshold specification. Under hard-short conditions, the current can exceed this specification due to internal propagation delay and blanking time. The total typical delay is 100ns.

The simplified waveforms of this operation are shown in Figure 8-18.

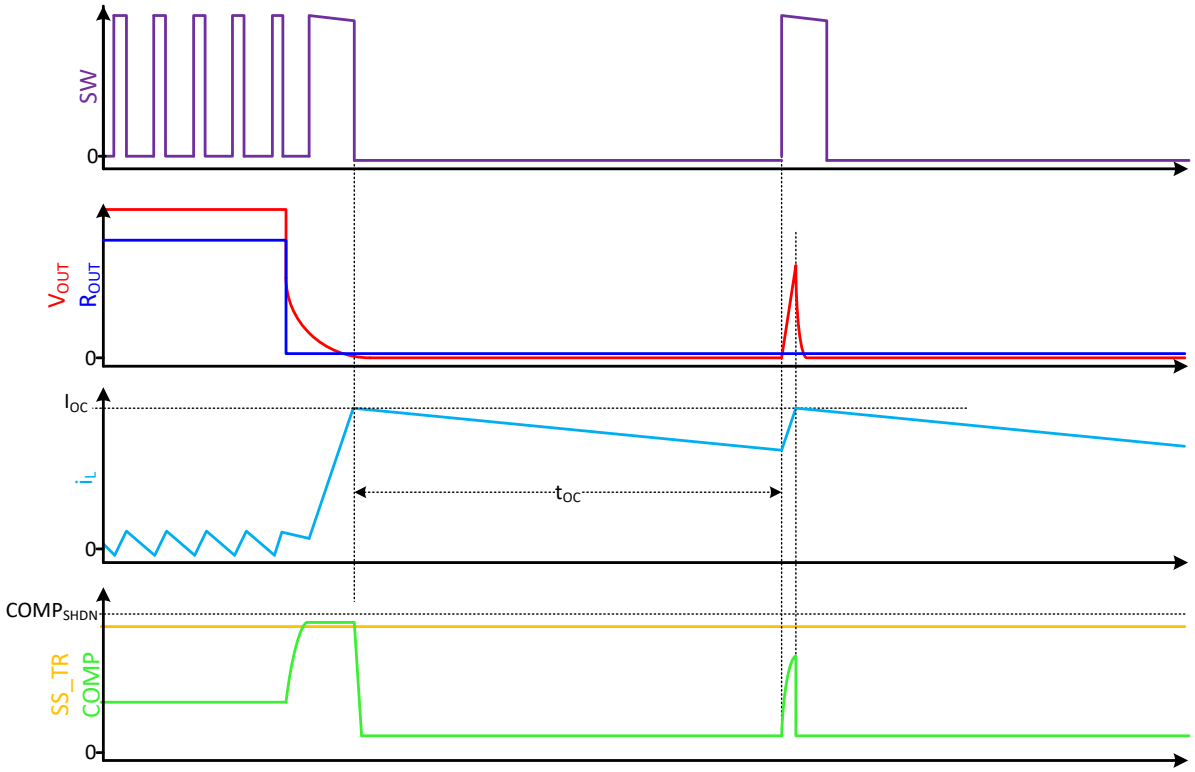


Figure 8-18. High-Side Overcurrent Protection (I_{OC})

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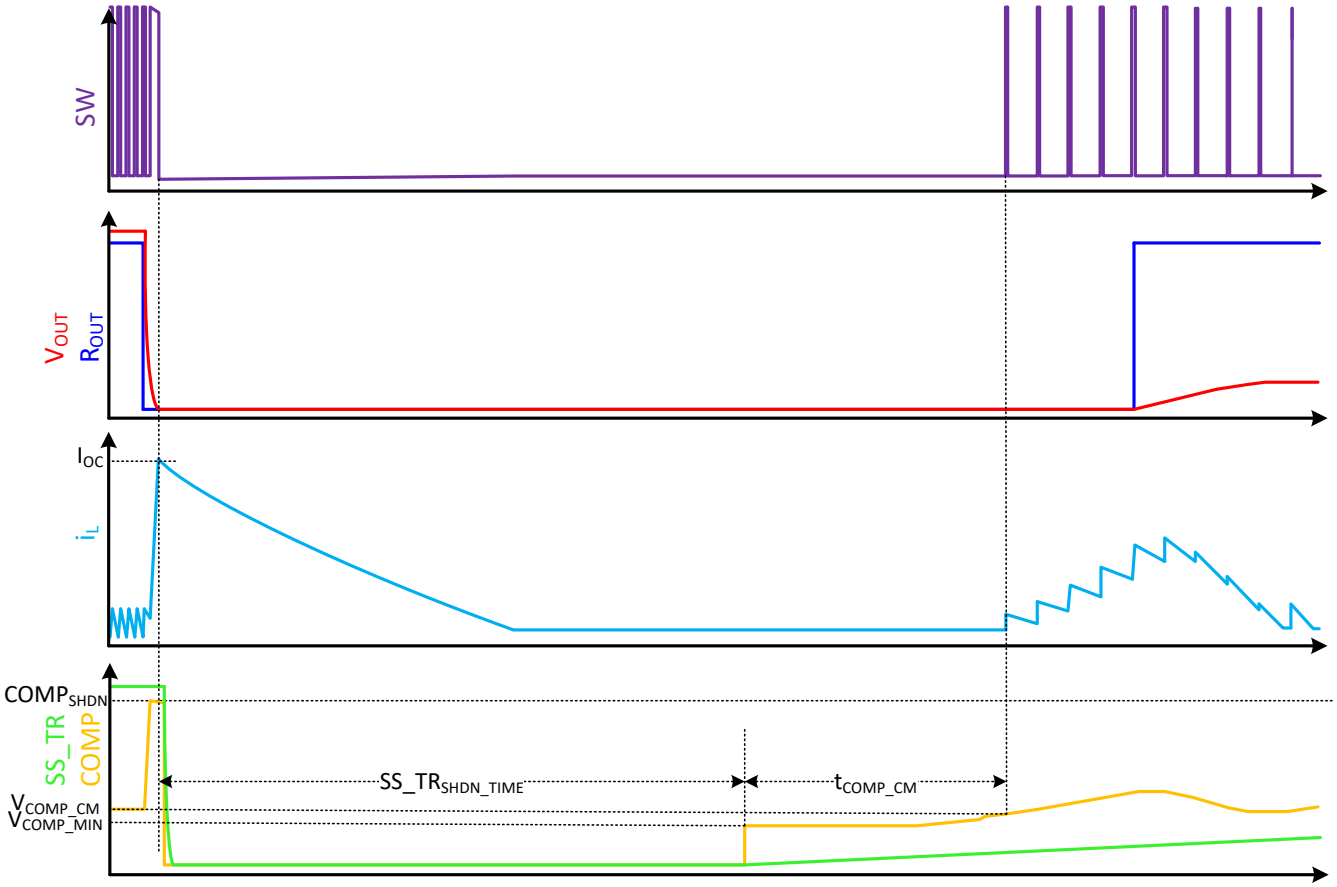
8.3.9.1.2 COMP Shutdown

Since the voltage on the COMP pin is proportional to the device output current, comparing the COMP voltage against a reference voltage provides an additional method to protect the device from overcurrent events. Specifically, if COMP rises above $COMP_{SHDN}$ voltage (typically 2V), the device stops switching for a prolonged period, typically 316µs ($SS_TR_{SHDN_TIME}$). During this time both the high-side and low-side FETs are open (SW is high impedance). This off-time is significantly longer compared to the t_{OC} time of 44µs.

This feature complements the I_{OC} current limit. Since the slew rate of COMP is limited by the overall loop bandwidth and by the drive strength of the error amplifier, the time required for COMP to reach $COMP_{SHDN}$ voltage during a fault depends on the loop compensation. For this reason, COMP can reach $COMP_{SHDN}$ at the same time (or before) the t_{OC} timer is triggered. For a $COMP_{SHDN}$ event to occur, both of the following conditions must be true:

1. The current through the high side is greater than the I_{OC} (typically 7.2A).
2. COMP voltage is greater than $COMP_{SHDN}$ (typically 2V).

An example of the COMP shutdown functionality is shown in the simplified waveforms of Figure 8-19.



A. The typical voltage for V_{COMP_MIN} = 650mV and V_{COMP_CM} = 850mV

Figure 8-19. COMP Shutdown Protection

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8.3.9.1.3 Low-Side Overcurrent Sinking Protection

Under certain conditions, such as during light load operation, the low-side MOSFET can sink current from the load. When a high current load is suddenly removed or V_{OUT} is raised above the set point, the low-side sink current can become excessive. To address this, low-side overcurrent sinking protection is provided.

If the low-side sinking current limit is exceeded, the low-side MOSFET turns off immediately for the remainder of that clock cycle. In this scenario, both MOSFETs remain off until the start of the next cycle. When the low-side MOSFET turns off, the switch node voltage increases and forward biases the high-side MOSFET body diode, while the high-side MOSFET remains off at this stage.

8.3.9.2 Output Overvoltage Protection (OVP)

The TPS7H4203 incorporates an output overvoltage protection (OVP) circuit to minimize output voltage overshoot. The OVP circuit uses two methods to detect an overvoltage condition:

1. VSNS Threshold Comparison: The OVP circuit engages when VSNS > ($PWRGD_{OV_FAULT}$ × V_{REF}), which corresponds to V_{OUT} rising above 108% of its nominal value. When this condition is detected, both the high-side and low-side FETs are turned off, placing the SW node in a high-impedance state. The inductor current free-wheels through the body diode of the low-side FET, which dissipates more power compared to active low-side FET conduction.
2. COMP Voltage Clamping: The TPS7H4203 also detects overvoltage conditions by comparing the COMP voltage to an internal reference (typically 739mV , or V_{COMP_OV}). During an overvoltage event, the error amplifier decrements the COMP voltage to maintain regulation. When the device detects this condition on V_{COMP}, the SW node is also placed in a high-impedance state.

An example that could cause an overvoltage condition is when the power supply output is overloaded for a sustained period of time. Therefore, the error amplifier compares the actual output voltage to the reference voltage. If the VSNS pin voltage is lower than the reference voltage for a considerable time, the output of the error amplifier demands maximum output current. After the condition is removed, the regulator output rises and the error amplifier output transitions to the steady-state voltage. In some applications with small output capacitance, the power supply output voltage can respond faster than the error amplifier. This leads to the possibility of an output overshoot. The OVP feature minimizes this overshoot.

If the VSNS pin voltage is greater than the OVP threshold, the high-side MOSFET is turned off, preventing current from flowing to the output and minimizing output overshoot. When the VSNS voltage drops lower than the OVP threshold and the V_{COMP} is greater than the common mode voltage, then the high-side MOSFET is allowed to turn on at the next clock cycle.

8.3.9.3 Thermal Shutdown

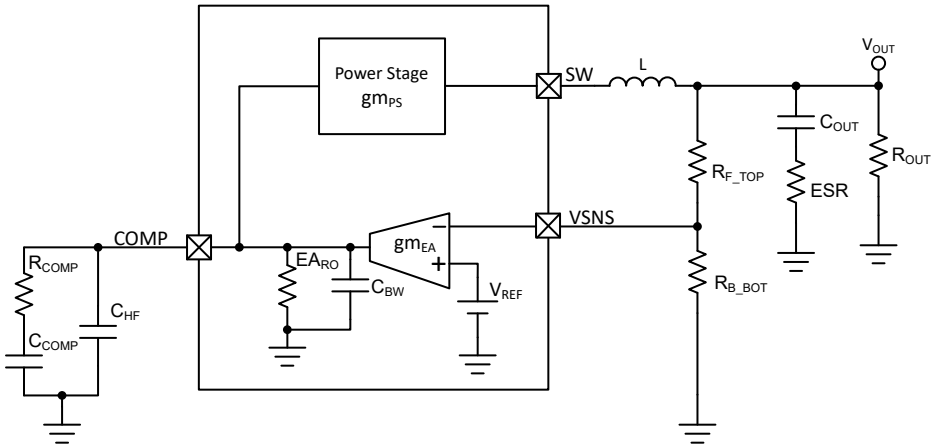
When the junction temperature exceeds 180℃ (typ.), the internal thermal shutdown circuitry turns off both high-side and low-side FETs, leaving the SW node in a high-impedance state. Once the junction temperature drops below 148℃ (typ.), the device re-initiates the power-up sequence under soft-start control. This protection mechanism prevents damage to the device during overtemperature conditions.

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8.3.10 Error Amplifier and Loop Response

Figure 8-20 illustrates a simplified model for the device control loop. The simplified model can be used to aid in determining the frequency response and transient response of the buck regulator system. The simplified model is composed of an operational transconductance error amplifier (OTA), the power stage, an external feedback network, and the external compensation network. The effects of slope compensation are not reflected in this simplified model. More information is provided on the following sections:

1. Error Amplifier
2. Power Stage Transconductance
3. Slope Compensation
4. Frequency Compensation



A. The compensation network illustrated in this figure is a Type 2A.

B. SS_TR is excluded from this model, as it is not relevant under steady-state conditions with small perturbations.

Figure 8-20. Simplified Small Signal Model For Loop Response

8.3.10.1 Error Amplifier

The TPS7H4203 device uses a transconductance error amplifier, which compares the VSNS voltage to the internal VREF voltage reference. The key typical specifications of the error amplifier are:

- Transconductance: 252µS(1µS = 1µA/V)
- DC Gain: 5800V/V (75.27dB)
- Output Resistance: 23MΩ
- Unity Gain Bandwidth: 2.56MHz
- Dynamic Voltage Range: 850mV to 2V

The frequency compensation network is connected between the COMP pin and GND. When the device is disabled the output of the error amplifier (COMP) is internally pull down. This occur when:

1. The input UVLO is triggered (PVIN < V_{UVLOF_PVIN})
2. The EN pins is in a logic low (V_{EN} < $V_{EN_FALLING}$)
3. A thermal shutdown event occurs

When the device is enabled (PVIN > V_{UVLOR_PVIN}, V_{EN} > V_{EN_RISING} and no thermal fault) the COMP voltage is pull-up to the minimum COMP clamp voltage (typically 650mV) and the soft-start pull down is deactivated (V_{SS_TR} begins rising). The device does not begin switching until the V_{COMP} > V_{COMP_CM} (typically 850mV), see Figure 8-19. The time it takes the COMP voltage to reach the 850mV is a function of the soft-start capacitor and the compensation network. Smaller soft-start capacitors and higher loop crossover frequency results in faster times to reach the internal reference voltage of 850mV and vice versa. As mention on the Output Overvoltage Protection (OVP), the error amplifier output voltage is also compared against an internal reference of 739mV to detect overvoltage conditions.

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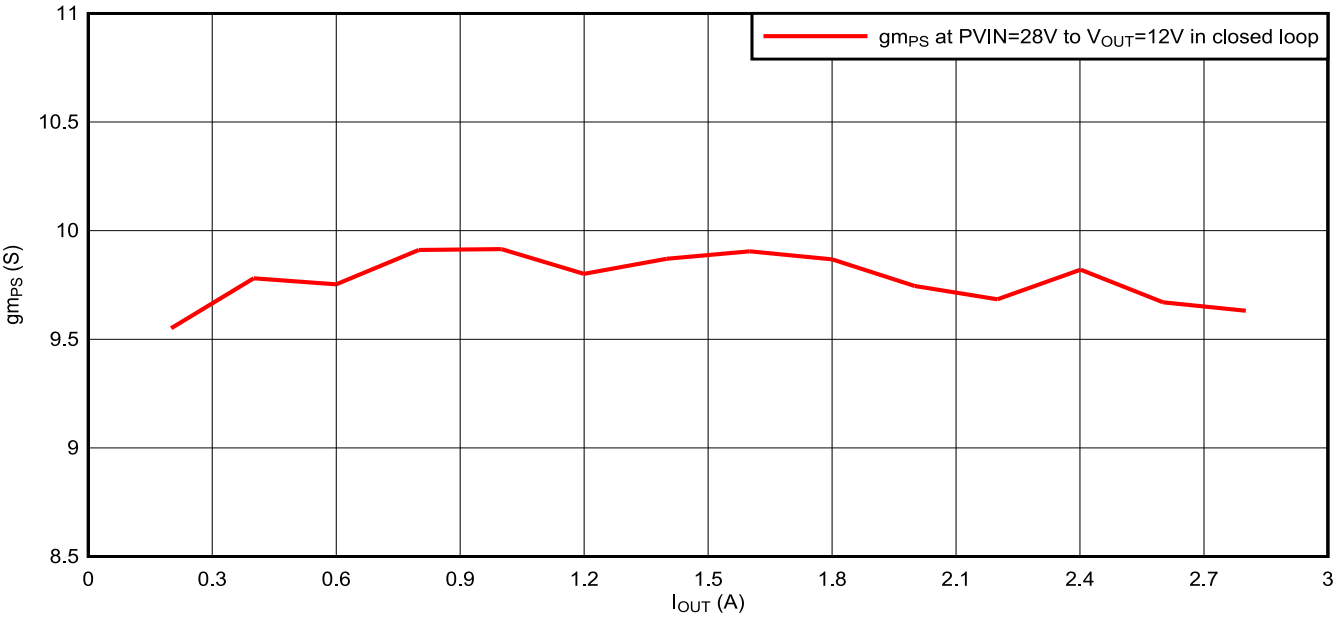
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8.3.10.2 Power Stage Transconductance

The power stage transconductance of the TPS7H4203 (gm_{PS}) is typically 10S (1S =1A/V). The gm_{PS} gain remains constant across the dynamic voltage range of the error amplifier (850mV to $COMP_{SHDN}$(typically 2V), see Figure 8-21. For the minimum and maximum values of gm_{PS}, refer to the *ERROR AMPLIFIER* section in the Electrical Characteristics table.

Note

The gm_{PS} as specified in the *ERROR AMPLIFIER* section of the Electrical Characteristics table is characterized in an open-loop configuration. The closed-loop gm_{PS} is affected by system efficiency. Refer to the typical efficiency plots for performance under different system configurations (Section 6.7).



A. In closed loop with PVIN=28V and V_{OUT}=12V.

Figure 8-21. gm_{PS} vs Load Current (I_{OUT})

8.3.10.3 Slope Compensation

The desired slope compensation (SC) can be configured using a resistor connected from the RSC pin to GND. The TPS7H4203 device subtracts a compensating ramp from the V_{COMP} control signal across all duty cycles. Various values of R_{SC} and the corresponding slope compensation values are shown in the *SLOPE COMPENSATION* section in the Electrical Characteristics table. Equation 18 is provided to approximate the value of R_{SC} needed to achieve a desired slope compensation. The fitting along with the data and error are shown in Data, Fit and Error for RSC vs Slope Compensation.

$$R_{SC}\,(k\Omega) = \frac{92.42}{SC\left(\frac{A}{\mu s}\right) - 0.03} \tag{18}$$

where

- R_{SC} is the suggested value of resistance in kΩ to achieve the desired slope compensation in A/µs
- SC is the desired value of slope compensation in A/µs

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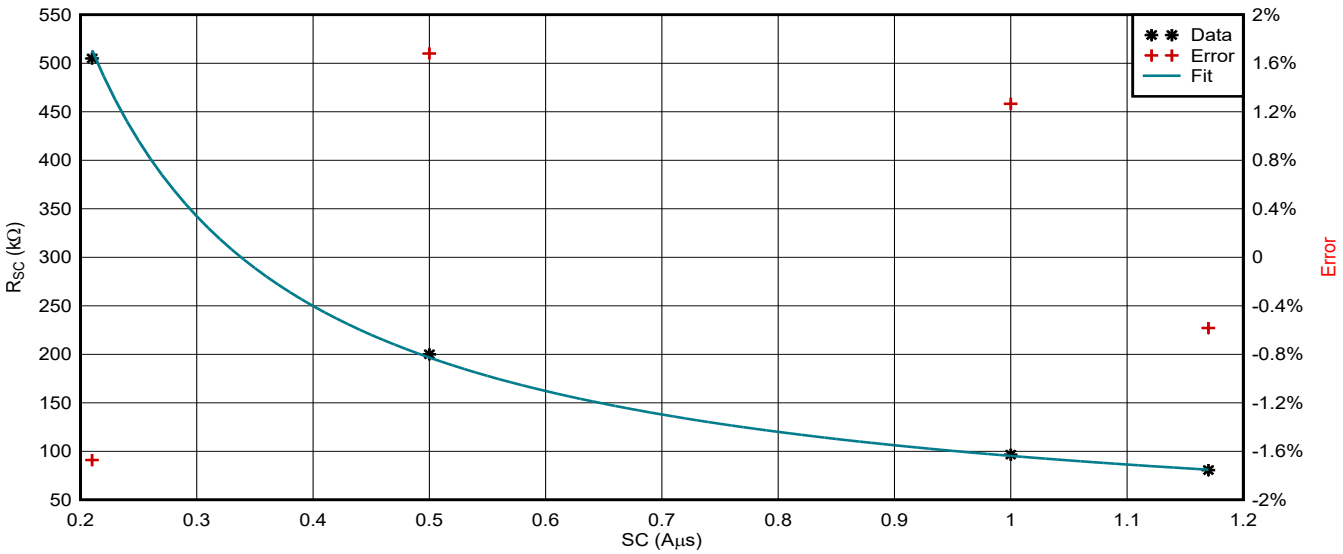


Figure 8-22. Data, Fit and Error for RSC vs Slope Compensation

A commonly suggested value for slope compensation is defined as the output voltage divided by the inductor value as presented on: Equation 19, for more details see SLUA101.

$$SC_{IDEAL}\left(\frac{A}{\mu s}\right) = \frac{\Delta i_L}{\Delta t_{OFF}} = -\frac{V_{OUT}\,(V)}{L\,(\mu H)} \quad (19)$$

8.3.10.4 Frequency Compensation

External frequency compensation is required for the TPS7H4203. Several industry-standard techniques are available for compensating DC-DC regulators. For the TPS7H4203, Type 2A compensation is most often recommended, though other approaches are also acceptable. Refer to Section 9.2.2.10 in the Application section for a specific example.

8.4 Device Functional Modes

The device uses fixed-frequency, peak current mode control. As a synchronous buck converter, it normally operates in continuous current mode under all load conditions.

The output voltage is divided down through external resistors, and VSNS is compared to an internal voltage reference (V_{REF}) by an error amplifier that drives the COMP pin. An internal oscillator initiates the turn-on of the high-side power switch.

The error amplifier output is then converted into a current reference, which is compared to the high-side power switch current. When the switch current reaches the current reference level generated by the COMP voltage, the high-side power switch turns off and the low-side power switch turns on.

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS7H4203 is a radiation hardened synchronous buck converter. The device is used to convert a higher DC input voltage to a lower DC output voltage at a maximum of 3A. The TPS7H4203 can be used over an input voltage range of 10V to 38V.

9.2 Typical Application

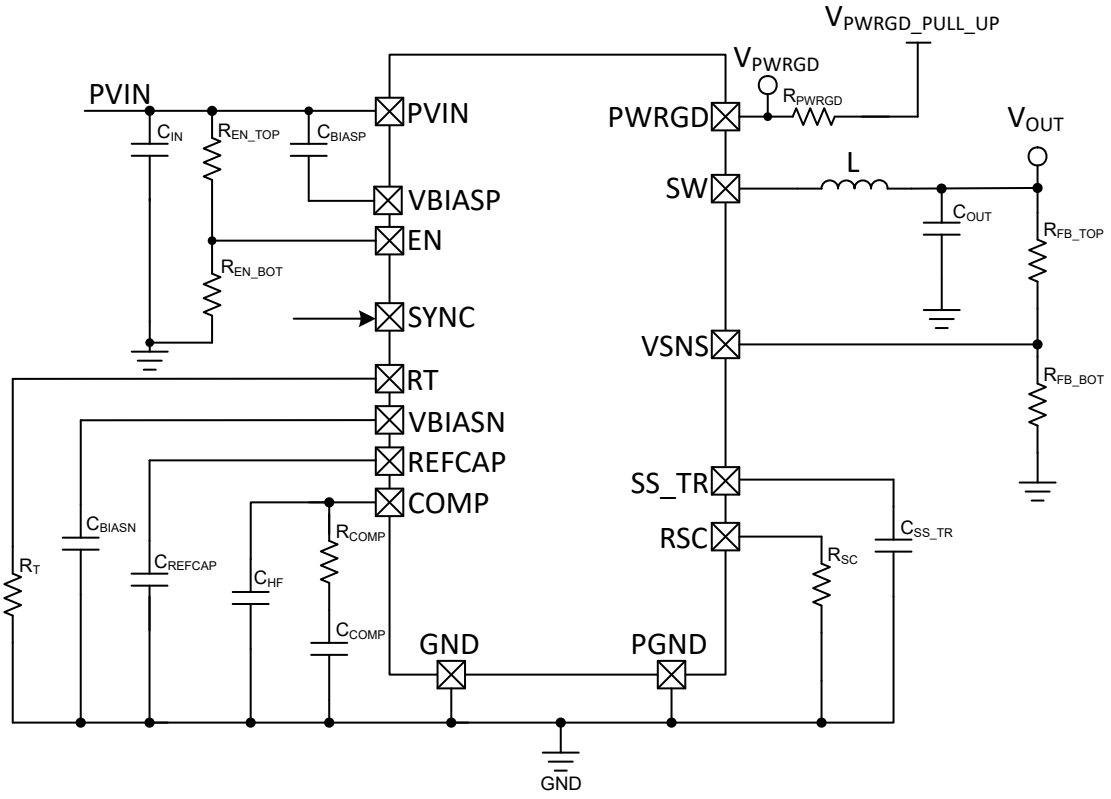


Figure 9-1. Typical Application

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9.2.1 Design Requirements

Table 9-1. Design Parameters

DESIGN PARAMETER	DESIGN VALUE
Input voltage (PVIN)	28V ± 10%
Output voltage (V_{OUT})	12V ± 1.5%
Maximum output current (I_{OUT})	3A
Transient response for a full-load (3A) load step (ΔI_{OUT})	ΔV_{OUT} = 240mV (or 2% of V_{OUT})
Output voltage ripple (V_{OUT_RIPPLE})	12mV_{PP} (or 0.1% of V_{OUT})
Input voltage ripple (V_{IN_RIPPLE})	126mV_{PP} (or 0.5% of V_{IN_MIN})
Start input voltage (rising PVIN)	19.6V
Switching frequency (f_{SW})	250kHz
$V_{PWRGD_PULL_UP}$	3.3V

9.2.2 Detailed Design Procedure

9.2.2.1 Operating Frequency

The first step is to select a switching frequency for the regulator. There is a trade-off between higher and lower switching frequencies. Higher switching frequencies can reduce the overall solution size by allowing the use of lower-valued inductors and smaller output capacitors compared to a power supply operating at a lower frequency. However, higher switching frequencies introduce additional switching losses, which negatively impact efficiency and thermal performance of the converter. In this design, a switching frequency of 250kHz is selected, as it is a specified frequency listed in the *SWITCHING FREQUENCY AND SYNCRONIZATION* section of the Electrical Characteristics table. Based on this table, an RT resistor value of 37.9 kΩ is selected. For frequencies not specified in the *SWITCHING FREQUENCY AND SYNCRONIZATION* section, designers can refer to Equation 7 to select the correct resistor value.

9.2.2.2 Output Inductor Selection

To calculate the value of the output inductor, use Equation 21. K_L is a coefficient that represents the amount of inductor ripple current relative to the maximum output current, I_{OUT}, as shown in Equation 20. Since the output capacitors must have a ripple current rating greater than or equal to the inductor ripple current, choosing the right inductor is tightly coupled to the output capacitors selection. In general, the inductor ripple value is at the discretion of the designer depending on specific system needs. Typical values for K_L range from 10% to 50%. Increase the value of K_L for low output current to reduce the value of the output inductor. Selecting the right inductor value is a balance between DC output voltage ripple and AC (or transient) response.

$$K_L = \frac{\Delta i_L}{I_{OUT}} \tag{20}$$

$$L \geq \left(\frac{V_{IN_MAX} - V_{OUT}}{I_{OUT} \times K_L}\right) \times \left(\frac{V_{OUT}}{V_{IN_MAX} \times f_{SW}}\right) \tag{21}$$

Note

A minimum inductor ripple current of 400mA is required to maintain operation above the noise floor of the pulse-width modulator (PWM) comparator and minimize switch-node jitter.

For this design example, a K_L = 40% is selected and the maximum input voltage (V_{IN_MAX}) is calculated to be 30.8V (28V + 10%). Once the designer selects the inductor and the real value is known, the key inductor specification can be calculated as:

1. Inductor ripple current (Equation 22)
2. Inductor RMS current (Equation 23)

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3. Inductor peak current (Equation 24)

The inductor design details are presented on Table 9-2.

$$\Delta i_L = \left(\frac{V_{IN_MAX} - V_{OUT}}{L}\right) \times \left(\frac{V_{OUT}}{V_{IN_MAX} \times f_{SW}}\right) \quad (22)$$

$$i_{L_RMS} = \sqrt{{I_{OUT}}^2 + \frac{1}{12} \times \left(\frac{V_{OUT} \times (V_{IN_MAX} - V_{OUT})}{V_{IN_MAX} \times L \times f_{SW}}\right)^2} \quad (23)$$

$$i_{L_PEAK} = I_{OUT} + \frac{\Delta i_L}{2} \quad (24)$$

Table 9-2. Inductor Design Calculations

Calculated Inductor Value (µH)	Selected Inductor Value (µH)	Inductor Ripple Current (A)	Inductor RMS Current (A)	Inductor Peak Current (A)
24.4	27	1.09	3.02	3.54

For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults, or transient load conditions, the inductor current can increase above the previously calculated peak inductor current level. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the maximum switch current limit, rather than the peak inductor current, the TPS7H4203 has a maximum current limit of 8A. The selected inductor is 7447709270 (Manufacturer Part #). This inductor value drops to approximately 14µH at 8A and has an RMS current rating of 4.6A.

9.2.2.3 Output Capacitor Selection

There are several key considerations when determining the value of the output capacitor. The selection is primarily driven by:

- The allowable voltage deviation due to a large, abrupt change in load current (load step).
- The desired output voltage ripple, caused by the natural switching action of the power stage.

The output capacitance must be selected based on the more stringent of these two criteria (refer to Equation 25). When selecting capacitors, attention should be given to maintaining a sufficient voltage rating, temperature rating, and accounting for any effective capacitance changes due to DC bias effects. It is also important to note that the value of the output capacitor directly influences the modulator pole of the converter frequency response, as described in Section 9.2.2.10.

$$C_{OUT}(F) \geq \max\left(C_{OUT_LOAD_STEP}(F), C_{OUT_RIPPLE}(F)\right) \quad (25)$$

The first criterion is the desired response to a load step. A load step typically occurs when the regulator is temporarily unable to supply sufficient output current during a large, fast increase in load current demand — for example, during a transition from no load to full load in dynamic loads such as processors. The output capacitor must be sized to supply the additional current to the load until the control loop responds to the change. Equation 26 provides the minimum output capacitance required from an electrical standpoint to meet this requirement. This is a first-order approximation and does not account for the ESR and ESL of the output capacitor. For ceramic capacitors, the ESR is typically small enough to be neglected. However, for space applications and large capacitance values, tantalum capacitors are commonly used, and their ESR must be taken into consideration.

$$C_{OUT_LOAD_STEP}(F) = \frac{2 \times \Delta I_{OUT}(A)}{f_{SW}(Hz) \times \Delta V_{OUT_LOAD_STEP}(V)} \quad (26)$$

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Where:

- ΔI_{OUT} — Worst case change in load current (load step), in Amperes (A). For this design, a full-load step of 3A is used.
- f_{SW} — Switching frequency of the converter, in Hertz (Hz). The selected switching frequency is 250kHz.
- $\Delta V_{OUT_LOAD_STEP}$ — Allowable change in output voltage due to the load step, in Volts (V). The target is to remain below a 2% change in the nominal output voltage.

The next criteria is the capacitance required to meet the output voltage ripple specification. Equation 27 is used to calculate the necessary capacitance to meet this criterion. In this design, the maximum desired output voltage ripple is less than 0.1% of V_{OUT} (or $12mV_{PP}$)

$$C_{OUTx_RIPPLE}(F) = \frac{\Delta i_L(A)}{8 \times f_{SW}(Hz) \times \Delta V_{OUT_RIPPLE}(V)} \quad (27)$$

Where:

1. Δi_L — Inductor ripple current in Amperes (A). Refer to Table 9-2 for more details.
2. f_{SW} —Switching frequency of the converter in Hertz (Hz). In this case the selected switching frequency is 250kHz.
3. ΔV_{OUT_RIPPLE} —Target output voltage ripple due to the switching nature of the converter in Volts (V). In this design the target is to be less than 0.1% of the nominal output voltage (or $12mV_{PP}$)

Finally, the ESR of the capacitor must be considered when meeting the output voltage ripple specification. The upper bound for the ESR can be calculated using Equation 28. The calculated results are shown in Table 9-3.

$$ESR \leq \frac{\Delta V_{OUT_RIPPLE}(V)}{\Delta i_L(A)} \quad (28)$$

Table 9-3. Output Capacitor Design Calculations

$C_{OUT_LOAD_STEP}$ (µF)	C_{OUT_RIPPLE} (µF)	MAXIMUM ESR (mΩ)
99	45.2	11

Additional deratings for aging, temperature, and DC bias should be factored in, which increases the minimum required output capacitance. Furthermore, capacitors have limits on the amount of ripple current they can handle without failing or generating excess heat; the selected capacitor bank must be rated for the ripple current calculated using Equation 22. For the selected inductor and nominal output voltage the ripple current is shown on Table 9-2.

For this specific design, taking all of the above requirements into account, three 33µF (for a total of 99µF) Tantalum capacitor are selected (T543X336M050ATE040, manufacturer part #). The selected capacitor has a maximum ESR of 40mΩ (13.33mΩ for all three) and a maximum RMS current rating of 1.94A (per capacitor for a total of ≅6A). The ripple current in this design is ≅1A as presented on Table 9-2. Additionally, two 0.1µF ceramic capacitor is added in parallel for high-frequency filtering, resulting in a total capacitance of 99.2µF. Using Equation 29 we can calculate the expected ripple voltage, the results are shown in Table 9-4.

$$\Delta V_{OUT_RIPPLE} = \frac{\Delta i_L(A)}{8 \times f_{SW}(Hz) \times C_{OUT}(F)} + [ESR(\Omega) \times \Delta i_L(A)] \quad (29)$$

Table 9-4. Expected Output Voltage Ripple for the Selected Equivalent Output Capacitance

ΔV_{OUT_RIPPLE} (mV)	ΔV_{OUT_RIPPLE} in % of V_{OUT}
20	0.17

9.2.2.4 Input Capacitor Selection

The input supply to the TPS7H4203 must be well regulated with sufficient capacitor bypassing for proper electrical performance. A minimum ceramic capacitor of at least 4.7µF effective capacitance near the PVIN input is required; however, additional bulk capacitance is generally needed to handle the high input currents. As with

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output capacitor selection, care must be taken when selecting input capacitors to provide a sufficient voltage rating, temperature rating, and consideration of any effective capacitance changes due to DC bias effects. The capacitor must also have a ripple current rating greater than the maximum input current ripple, calculated using Equation 30.

$$i_{CIN_RMS}\left(A\right) = I_{OUT}\left(A\right) \times \sqrt{\left(\frac{V_{OUT}\left(V\right) \times \left[V_{IN_MIN}\left(V\right) - V_{OUT}\left(V\right)\right]}{V_{IN_MIN}\left(V\right)^{2}}\right)} \tag{30}$$

The minimum input capacitance can then be determined using Equation 31 by selecting a maximum desired input ripple voltage, ΔV_{IN_RIPPLE}. For this design, an input ripple voltage of ≤ 0.5% of the minimum PVIN voltage (25.2V) is selected (ΔV_{IN_RIPPLE} ≤ 126mV).

$$C_{IN}(F) \geq \frac{0.25 \times I_{OUT}(A)}{\Delta V_{IN_RIPPLE}(V) \times f_{SW}(Hz)} \tag{31}$$

The input capacitor design calculations are shown in Table 9-5.

Table 9-5. Input Capacitor Design Calculations

i_{CIN_RMS} (A)	LOWER BOUND FOR C_{IN} (µF)
1.5	23.8

Note, however, that Equation 31 does not account for the effects of ESR on the input ripple voltage,therefore, additional capacitance is used. Specifically, a 33µF tantalum capacitor (Model: T543X336M050ATE040) and 14.8µF ceramic capacitors are selected, yielding a total input capacitance of 47.8µF. The tantalum capacitor have a RMS current rating of 2.49A. These capacitors should be place as close to the PVIN pins as possible.

9.2.2.5 Soft-Start Capacitor Selection

The soft-start capacitor C_{SS_TR} determines the amount of time required for the output voltage to reach its programmed value during power-up. This is useful when a load requires a controlled voltage slew rate. It is also beneficial when the output capacitance is large, as is typical with space-grade buck converters, since a large amount of current is needed to quickly charge the capacitor to the output voltage level. The high currents required to charge the capacitor can cause the TPS7H4203 to reach its current limit, draw excessive current from the input power supply, or cause the input voltage rail to sag. Limiting the output voltage slew rate effectively mitigates these issues. The soft-start capacitor value can be calculated using Equation 9 and Equation 10, and the calculated values, along with the selected values, are shown in Table 9-6. To minimize in-rush current, the soft-start value was optimized using lab measurements. While lower soft-start values produced inductor peak currents of ~7A, the selected setting limits the maximum inductor current to approximately 3.68A.

Table 9-6. Soft-Start Capacitor Design Calculations

$t_{SS_TR_NOMINAL}$ (ms)	$C_{SS_TR_NOMINAL}$ (nF)	$C_{SS_TR_SELECTED}$ (nF)
0.89	8.86	68

9.2.2.6 Rising VIN Set Point (Configurable UVLO)

An external resistor divider from PVIN to GND is used to enable the TPS7H4203 when a desired input voltage threshold is reached. This effectively acts as an adjustable undervoltage lockout (UVLO). A turn-on voltage (V_{UVLO_RISING}) of 10V is selected. A top resistor (R_{EN_TOP}) of 10kΩ is then chosen as a reasonable tradeoff, large enough to minimize power dissipation yet low enough to prevent excessive noise coupling at the high-impedance node.

Using Equation 4, a bottom resistor (R_{EN_BOT}) of 640Ω is calculated. The nearest selected standard resistor (using 1% tolerance) value is 690Ω. Using the selected top and bottom resistor values, the nominal rising and falling external undervoltage lockout thresholds can be calculated. Based on Equation 5 and Equation 6, the nominal rising and falling UVLO voltages are found to be 10.2V and 8.42V, respectively. Since the internal falling UVLO threshold is greater than the calculated 8.42V, the internal UVLO dominates the falling response.

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Note

The maximum voltage the EN pin can tolerate is 5.5V. The upper bound for the R_{EN_TOP} is 400kΩ.

9.2.2.7 Output Voltage Feedback Resistor Selection

The resistor divider network, comprised of R_{FB_TOP} and R_{FB_BOT}, is used to set the output voltage. For this design, a value of 10kΩ was selected for R_{FB_TOP}. Additionally, a 49.9Ω resistor was placed in series with R_{FB_TOP} to aid in control loop measurements. Using the approximated combined resistance of 10.05kΩ and Equation 1, R_{FB_TOP} is calculated to be 914Ω. The nearest standard 0.1% resistor value of 909Ω was selected.

9.2.2.8 Output Voltage Accuracy

To determine the output voltage DC accuracy, the following sources of error are considered:

- V_{REF} within the Electrical Characteristics table is the predominant source of error. This encompasses the error due to the reference voltage and error amplifier offset. The across temperature minimum of 0.99V, maximum of 1.01V, and typical of 1V results in an accuracy of ± 1%
- The V_{REF} specification is not measured in a switching, closed-loop configuration. Figure 6-38 can be used to see the effects of output current (load regulation) and switching. However, it is seen that across the complete 3A load, there is only 663µV deviation. This deviation is considered small enough such that load regulation is not included in this accuracy calculation.
- The external error due to the resistor tolerance of R_{FB_TOP} and R_{FB_BOT} must be added. Since the errors are assumed to be uncorrelated, the errors are added as a root sum of squares. For the selected 0.1% tolerance R_{FB_TOP} and R_{FB_BOT} resistors, the total error is shown in Equation 32.

$$R_{ERROR} = \pm\sqrt{0.1\%^2 + 0.1\%^2} = \pm 0.14\% \quad (32)$$

Equation 33 is used to calculate the system error for output voltage accuracy. The total error is calculated to be ±1.01%, well below the ±1.5% target.

$$SYSTEM_{ERROR} = \pm\sqrt{V_{REF_ERROR}{}^2 + R_{ERROR}{}^2} \quad (33)$$

Lifetime drift data can similarly be incorporated. Group C data is available to aid in this calculation. For this example, lifetime drift is assumed to be minimal compared to the other sources of error and is therefore excluded from the calculation.

9.2.2.9 Slope Compensation Requirements

While different slope compensation values may be selected for different applications, a commonly suggested value for slope compensation is defined as the output voltage divided by the inductance value, as shown in Equation 19. Once the slope compensation is calculated, the necessary RSC resistor value is determined using Equation 18.

Note

While the slope compensation is specified as a positive value in the Electrical Characteristics, it is internally subtracted from V_{COMP}. The negative sign in Equation 19 is inherent to the internal circuitry.

Table 9-7. Slope Compensation Design Calculations

SC_{IDEAL} (A/µs)	RSC Calculated (kΩ)	RSC Selected (kΩ)
0.447	221	226

9.2.2.10 Compensation Component Selection

The control loop of the TPS7H4203 is described in Section 8.3.10. The component selection for compensating this device is as shown below. Other industry standard approaches for compensating a peak current mode control buck regulator are also acceptable.

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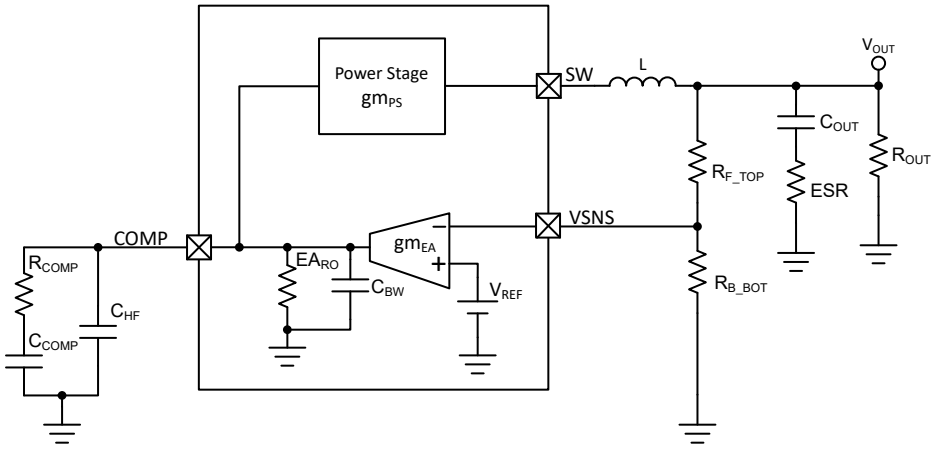


Figure 9-2. Type 2A Compensation With Simplified Loop

1. Determine the desired (or target) crossover frequency, f_{CO_TARGET}. A good starting method is to set the crossover frequency between 10% (1/10) and 20% (1/5) of the switching frequency. This generally provides a good transient response and make sure that the modulator poles do not degrade the phase margin. For this design, 25kHz was the selected target crossover frequency.
2. Determine the required gain from the compensated error amplifier using Equation 34:

$$A_{VM} = \frac{2\pi \times f_{CO_TARGET}\,(\mathrm{Hz}) \times C_{OUT}\,(F)}{gm_{PS}\,(S)} \tag{34}$$

where gm_{PS} is the power stage transconductance (typically 10S)

3. R_{COMP} can be determined by Equation 35:

$$R_{COMP}\,(\Omega) = \frac{A_{VM}}{gm_{EA}(S)} \times \frac{V_{OUT}\,(V)}{V_{REF}\,(V)} \tag{35}$$

where gm_{EA} is the transconductance of the error amplifier (typically 252µS) and V_{REF} is the reference voltage (typically 1V).

4. Calculate the power stage dominant pole determined by Equation 36:

$$f_{PS_POLE}(\mathrm{Hz}) = \frac{I_{OUT}\,(A)}{2\pi \times C_{OUT}(\mathrm{F}) \times V_{OUT}(V)} \tag{36}$$

5. Place a compensation zero at the dominant pole by selecting C_{COMP} as determined by Equation 37:

$$C_{COMP}\,(\mathrm{F}) = \frac{1}{2\pi \times f_{PS_POLE}(\mathrm{Hz}) \times R_{COMP}\,(\Omega)} \tag{37}$$

6. Calculate the ESR zero from the output capacitor bank by Equation 38:

$$f_{PS_ZERO_ESR}(\mathrm{Hz}) = \frac{1}{2\pi \times \mathrm{ESR}\,(\Omega) \times C_{OUT}(\mathrm{F})} \tag{38}$$

7. C_{HF} is used to cancel the zero from the equivalent series resistance (ESR) of the output capacitor C_{OUT} and is calculated using Equation 39:

$$C_{HF}\,(\mathrm{F}) = \frac{1}{2\pi \times R_{COMP}\,(\Omega) \times f_{PS_ZERO_ESR}(\mathrm{Hz})} \tag{39}$$

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Note

If the frequency of ESR zero is higher than half the switching frequency, use half the switching frequency instead of the ESR zero in Equation 39.

Table 9-8. Compensation Components Calculation

A_{VMx} (V/V)	R_{COMP} (kΩ)	f_{PS_POLE}(Hz)	C_{COMP} (nF)	$f_{PS_ZERO_ESR}$ (kHz)	C_{HF} (pF)
1.56	74.2	401	5.35	120	18

Table 9-9. Selected Compensation Components

R_{COMP} (kΩ)	C_{COMP}(nF)	C_{HF} (pF)
69	5.6	22

Note that the components selected using these equations are often only starting values in a design. Optimizations can be made after lab testing to further improve the frequency response and provide a closer match to the desired crossover frequency.

9.2.2.11 SW to PGND Schottky Diode

A Schottky diode is connected from SW to PGND, providing a low-impedance path for inductor current during dead time. For optimal efficiency and performance, select a diode with low or no reverse recovery time. Note that true Schottky diodes have no reverse recovery time. While using a Schottky diode is good design practice, it may not be required depending on the maximum voltage on PVIN in the application due to Destructive Single Event Effects (DSEE). For more details, refer to the Table 9-10.

Another benefit of using a Schottky diode is increased efficiency during low duty cycle operation, refer to the efficiency plots under the Typical Characteristics section.

Table 9-10. DSEE PVIN Maximum Voltage With and Without a Schottky Diode

Facility	Ion	Schottky Diode in System ?	Maximum PVIN Voltage (V)
TAMU Cyclotron Institute K500	^{165}Ho	Yes	40
		No	38
MSU FRIB K500	^{169}Tm	Yes	38
		No	36

9.2.3 Application Curves

Typical plots are shown for the following conditions:

- PVIN = 28V
- V_{OUT} = 12V
- I_{OUT} = 3A
- Switching frequency (f_{SW}) = 250kHz

Note

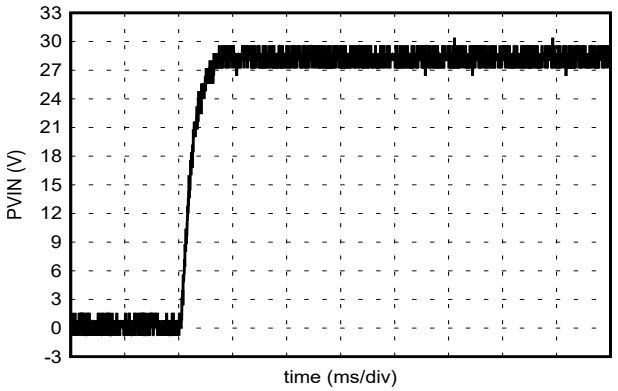
Data points were decimated for plotting purposes, which can result in missed peaks. The original, non-decimated numerical important values are shown below the plots for accuracy.

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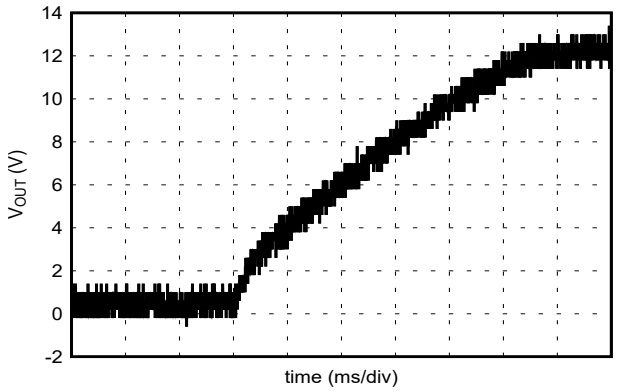
9.2.3 Application Curves (continued)

Typical plots are shown for the following conditions:



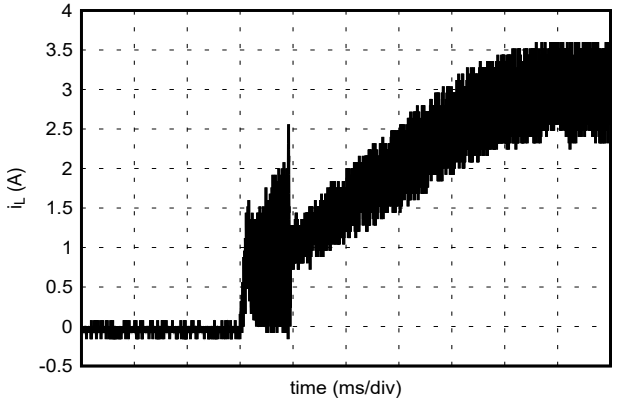
PVIN slew rate of ≅ 47mV/µs (using 10% to 90% voltage as reference voltages)

Figure 9-3. PVIN Voltage Turn on Voltage With a 3A Resistive Load



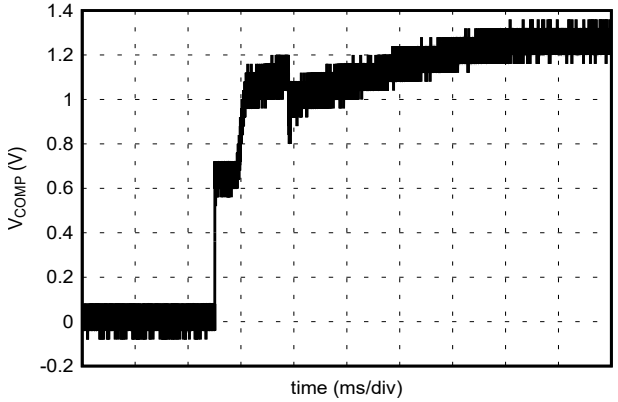
V_{OUT} soft-start time is ≅ 4.47ms (using 10% to 90% voltage as reference voltages)

Figure 9-4. Output Voltage (V_{OUT}) Turn-on Voltage With a 3A Resistive Load



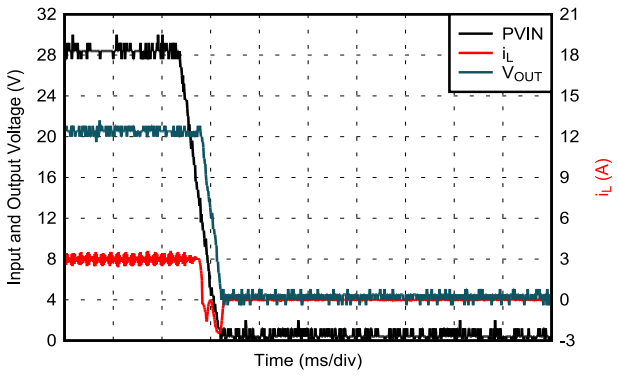
i_L maximum current is 3.68A

Figure 9-5. Inductor Current (i_L) Turn-on Voltage With a 3A Resistive Load



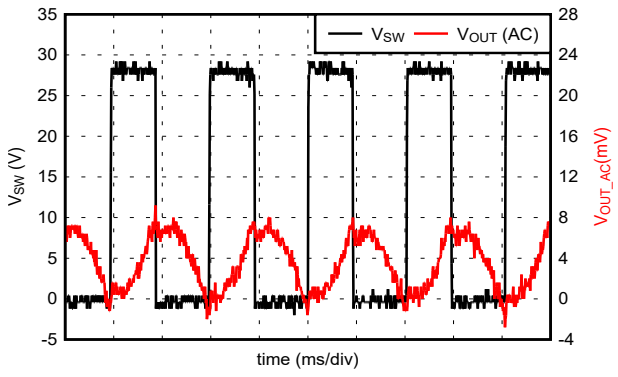
The bandwidth is limited to 20MHz

Figure 9-6. Compensation Voltage (V_{COMP}) Turn-on Voltage With a 3A Resistive Load



V_{OUT} is bandwidth limited to 20MHz

Figure 9-7. PVIN, Inductor Current and Output Voltage During a Power-Down With a 3A Resistive Load



V_{OUT} is bandwidth limited to 20MHz

Figure 9-8. Switch Node and Output Ripple Voltage at Steady State With 3A Resistive Load

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9.2.3 Application Curves (continued)

Typical plots are shown for the following conditions:

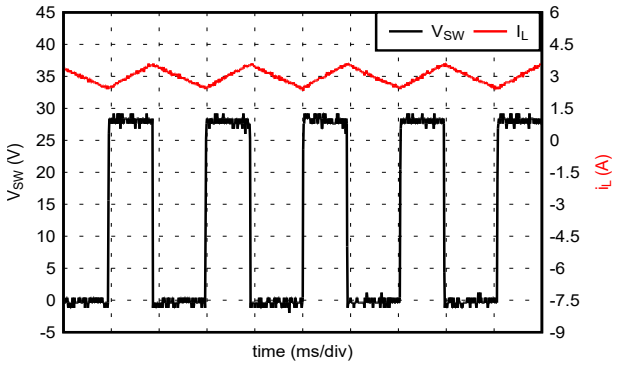
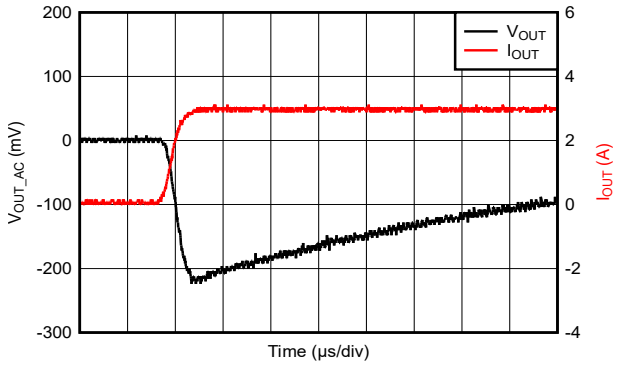
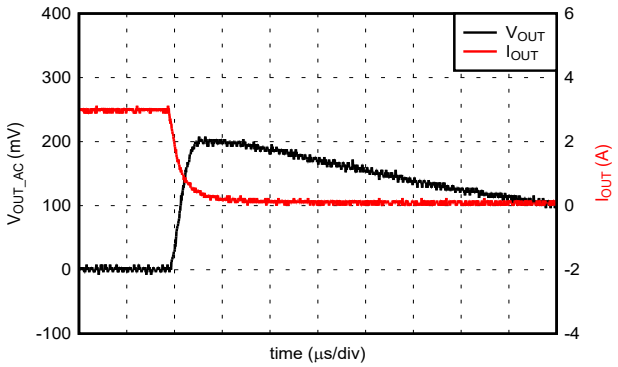


Figure 9-9. Switch Node Voltage and Inductor Current at Steady State With 3A Resistive Load



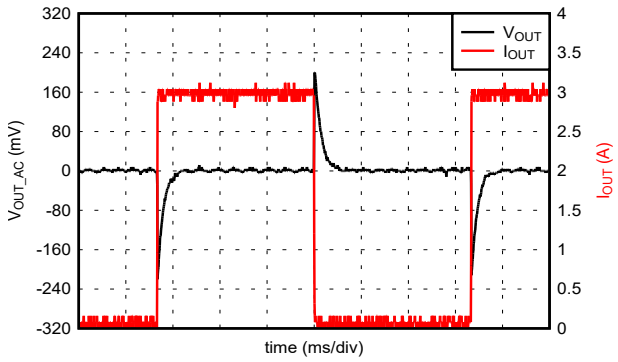
I_{OUT} slew rate of 142mA/µs (using 10% to 90% as the reference current)

Figure 9-10. Output Voltage Load Transient Response From 100mA to 3A (Zoom-in)



I_{OUT} slew rate of 142mA/µs (using 10% to 90% as the reference current)

Figure 9-11. Output Voltage Load Transient Response From 3A to 100mA (Zoom-in)



I_{OUT} slew rate of 142mA/µs (using 10% to 90% as the reference current)

Figure 9-12. Output Voltage Load Transient Response From 3A to 100mA (Zoom-out)

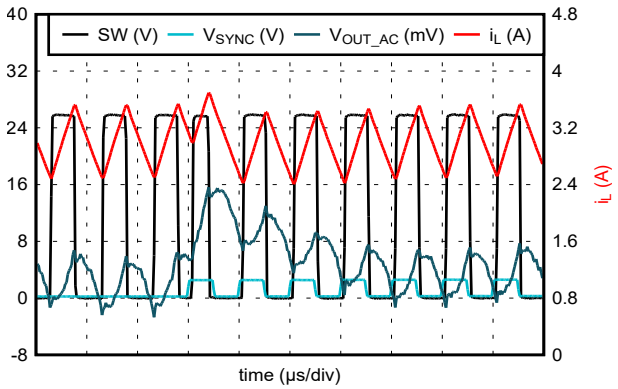


Figure 9-13. Transition From Internal to External Clock at 3A Resistive Load

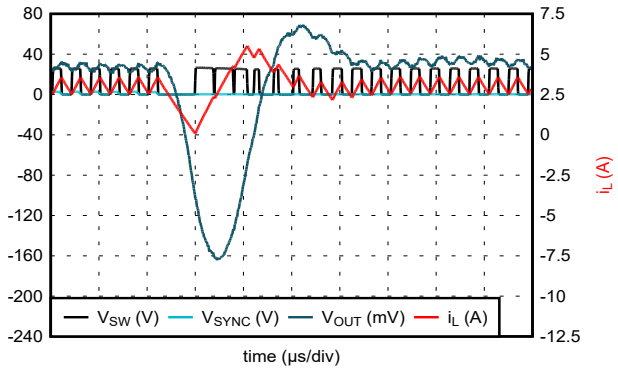
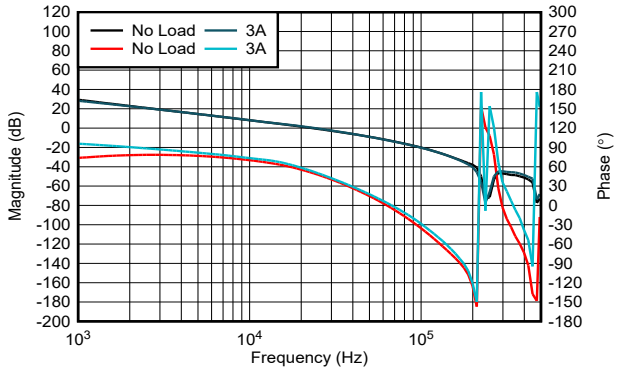


Figure 9-14. Transition From External to Internal Clock at 3A Resistive Load

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9.2.3 Application Curves (continued)

Typical plots are shown for the following conditions:



Load	f_{CO} (kHz)	Phase Margin (°)	Gain Margin (dB)
No Load	23	50	-12
3A (Resistive Load)	24	51	-13

Figure 9-15. Complete Loop Bode Plot at No Load and 3A Resistive Load

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9.2.4 Parallel Operation Compensation

The TPS7H4203 can be paralleled in a primary-secondary mode to achieve increased output current as described in Figure 8-7. The current through each of the N paralleled devices are nominally be 1/N. The TPS7H4203 is designed to inherently support paralleling two devices with out of phase operation to reduce ripple.

In parallel mode, the current mismatch due to error amplifier gm_{EA} differences are minimized since the output of the error amplifiers are all electrically connected by connection of the COMP pins. Therefore, the current mismatch is dominated by the mismatch of the individual power stage gm_{PS} values. This parameter is specified in the Electrical Characteristics table across temperature.

There are two approaches to compensate the TPS7H4203 when in parallel mode. The first is to compensate the primary device and connect all COMP pins together. To do this, follow Section 9.2.2.10 but be sure to use the total output capacitance, C_{OUT}, and total output current, I_{OUT}, of the complete system (not just the output current or output capacitance of a single device). Adjust the R_{COMP} calculation used in step #3 to Equation 40, where N is the number of paralleled devices.

$$R_{COMP_PARALLEL} = \frac{1}{N^2} \times \frac{A_{VM}}{gm_{EA}} \times \frac{V_{OUT}}{V_{REF}} \quad (40)$$

Alternatively, each device may be individually compensated following the steps described in Section 9.2.2.10. In this case, the output capacitance, C_{OUT}, and output current, I_{OUT}, is be the individual C_{OUT} and I_{OUT} of each device (in other words, scale the total C_{OUT} and I_{OUT} by 1/N). The COMP pins should still be tied together but there is no need to change the equation in step #3. The disadvantage of this approach is increased component count, but the advantage is that it may reduce the noise that gets injected into the COMP pin due to the physically close compensation components near each device.

Other items to follow include:

- Only a single feedback network is connected to the VSNS network of the primary device. Therefore, all VSNS nodes must be connected.
- Only a single soft-start capacitor is required. Be aware the soft-start current scales with the number of tied-together SS_TR pins (referred as N).
  - See Equation 11
- Only a single enable signal (or resistor divider) is needed. Connect all EN pins together.
- Connect all PWRGD pins together and use a single pull-up resistor in order to have a wired-OR power good signal.
- Connect the SYNC pins as together, while floating the RT pin of the primary converter. It may also be possible to synchronize to an external clock if desired.

9.2.4.1 Input and Output Capacitance Reduction

One of the benefits of paralleling multiple phases is the reduction in input and output capacitance for steady-state requirements, when compared to a single-phase design with the same total load.

Note

The equations discussed in this section are valid when the phase shift between phases equals 360/N degrees, where N is the number of phases. Importantly, this reduction applies only under steady-state conditions; oftentimes, the input and output capacitance values are dominated by the characteristics of the load transients.

9.2.4.1.1 Input Capacitor Reduction

In a multiphase system, the input RMS current is lower compared to a single-phase system with the same total load (I_{OUT}). This reduction allows for smaller input capacitance while meeting the same input ripple specifications. An additional benefit is reduced self-heating, resulting from the lower current flowing through the equivalent series resistance (ESR) of the capacitors. Figure 9-16 below shows the simplified input current

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waveforms for the primary and secondary (2 devices) operating in parallel, compared to a single-phase configuration (shown in dashed lines). The input RMS current reduction can be calculated using Equation 30. This factor is then applied to the single-phase RMS current, as calculated per the referenced equation. Figure 9-17 shows the $i_{CIN_RMS_PARALLEL_FACTOR}$ plotted against duty cycle.

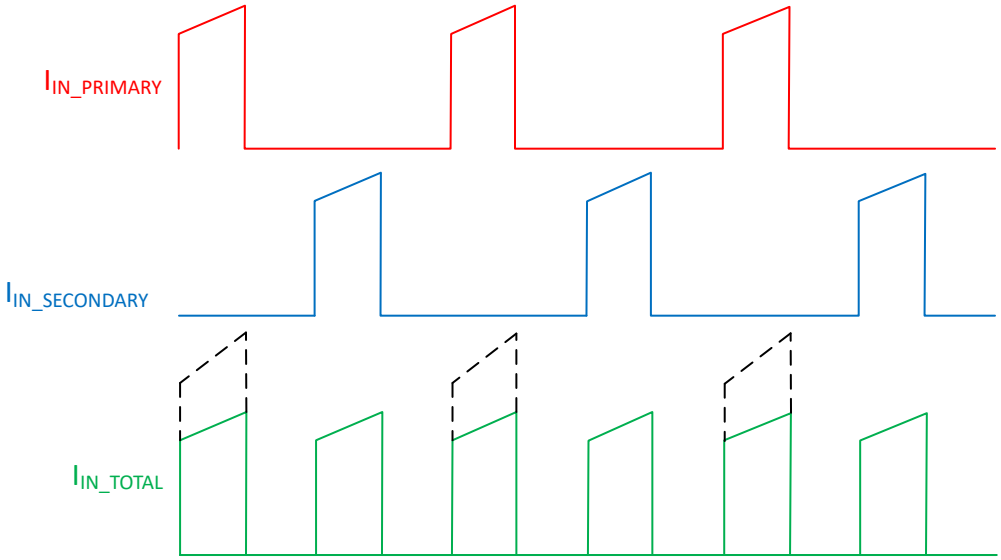


Figure 9-16. Input Current Waveform for SW1 and SW4 in Parallel

$$i_{CIN_RMS_PARALLEL_FACTOR} = \sqrt{\left(D - \frac{m}{N}\right) \times \left(\frac{1+m}{N} - D\right)} \quad (41)$$

Where:

- D is the duty cycle in numerical value (0 to 1).
- N is the number of parallel phases.
- m=floor (N × D)

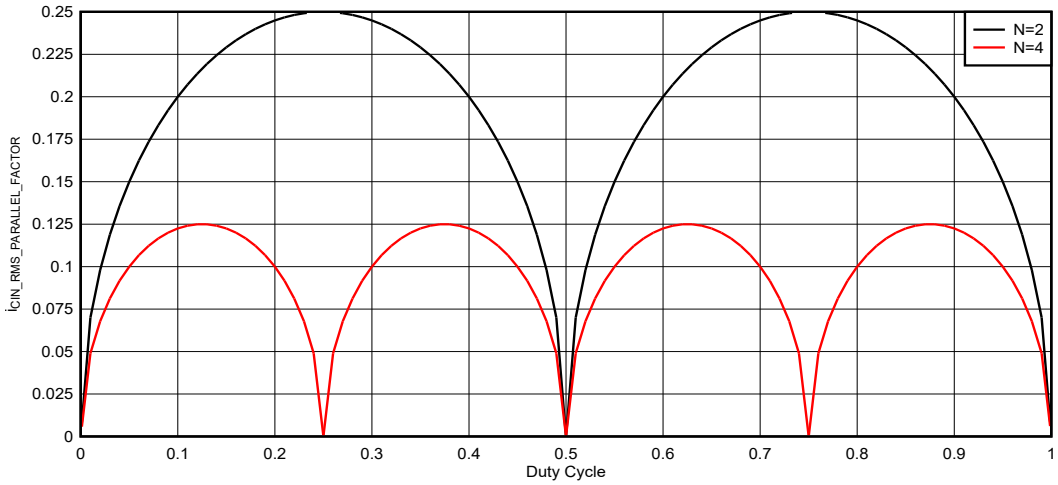


Figure 9-17. $i_{CIN_RMS_PARALLEL_FACTOR}$ vs Duty Cycle

9.2.4.1.2 Output Capacitor Reduction

When phases operate concurrently, each phase charges and discharges the output capacitance at different times based on the active status of that phase. As a result, the total current (the sum of all phase currents) exhibits a smaller peak-to-peak value. Since the AC component of this total current is absorbed by the

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output capacitance (C_{OUT}), the reduced ripple current directly leads to lower output voltage ripple. For a visual representation of this effect, refer to Figure 9-18.

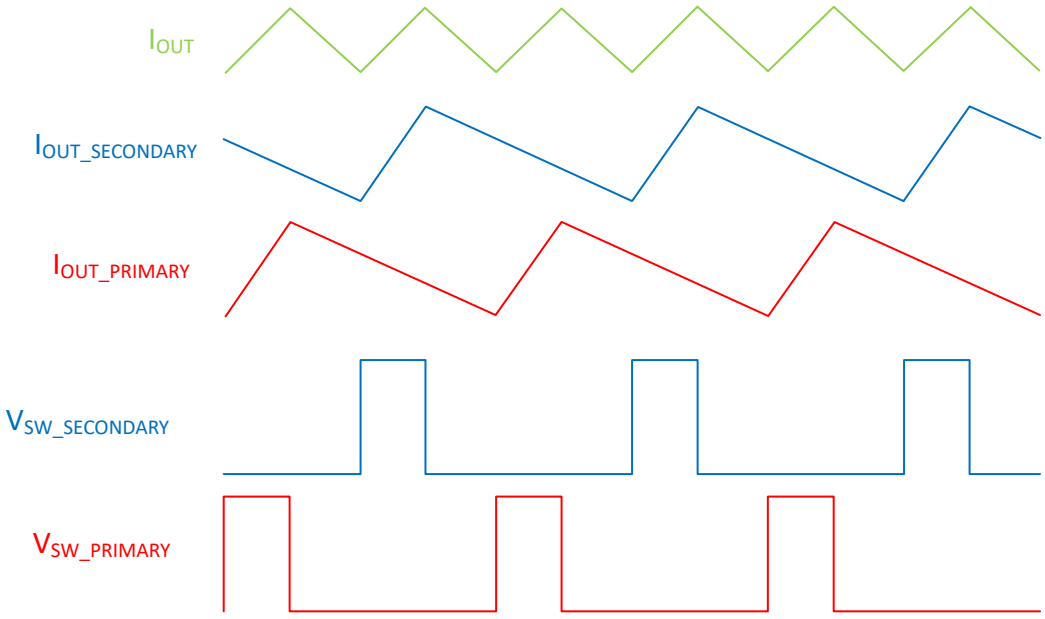


Figure 9-18. Inductor Ripple Currents for Primary and Secondary in Parallel

The reduced ripple output current factor can be calculated using Equation 42. This factor can be seen in Figure 9-19 for 2 and 4 channels (or phases) in parallel. The effective output ripple current is the product of the calculated factor (as per Equation 42) and the single phase ripple current as calculated per Equation 22.

$$\Delta i_{L_PARALLEL_FACTOR} = \frac{N}{D \times (1-D)} \times \left(D - \frac{m}{N}\right) \times \left(\frac{1+m}{N} - D\right) \quad (42)$$

where:

- D is the duty cycle in numerical value (0 to 1).
- N is the number of parallel phases.
- m=floor (N × D)

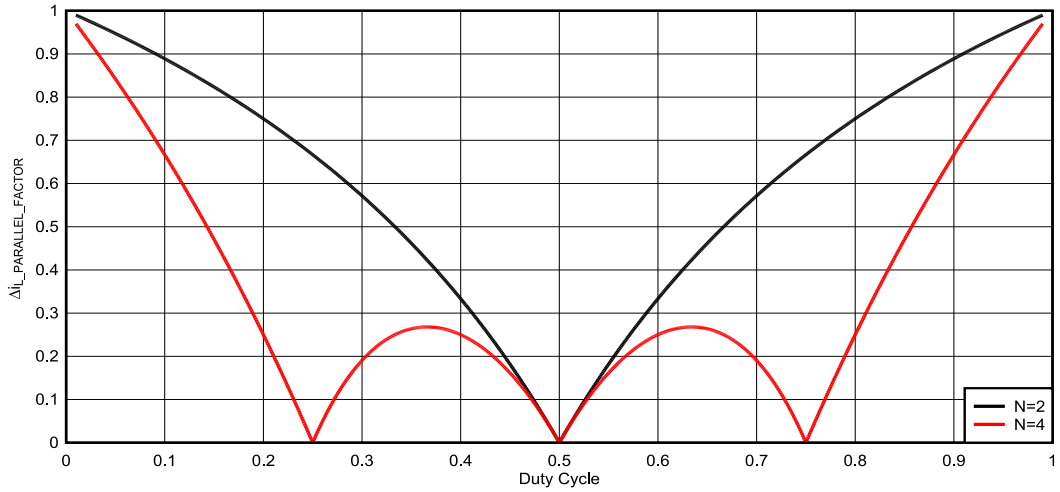


Figure 9-19. $\Delta i_{L_PARALLEL_FACTOR}$ vs Duty Cycle

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9.2.5 Inverting Buck-Boost

The TPS7H4203 can be configured as an inverting buck-boost to create a negative output voltage as shown in Figure 9-20.

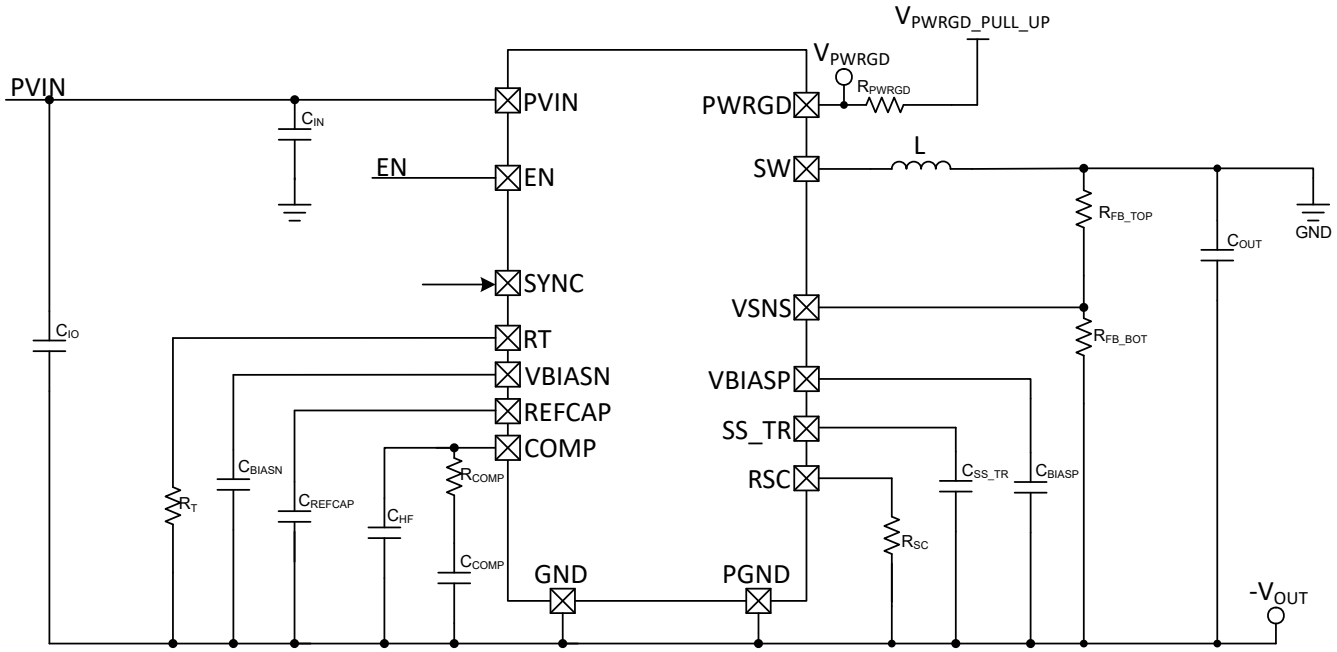


Figure 9-20. Simplified Schematic of Inverting Buck-Boost

Additional considerations for designing an inverting buck-boost are described in the application note, Working With Inverting Buck-Boost Converters. While many details and equations are provided within the application note, a few considerations for the TPS7H4203 are as follows:

- Make sure the recommended maximum input voltage (PVIN) of 38V is followed. This means VIN + |VOUT| ≤ 38V.
- The average inductor current for an inverting buck-boost is greater than the load current (See Equation 43). This can result in higher peak currents than expected when compared to a buck converter. Additionally, this means that the average inductor current must be kept lower than the TPS7H4203 recommended maximum of 3A; therefore, the maximum output current available to the load must always be under 3A. This current needs to be always lower than the MIN value of the high-side current limit (I_{OC}).

$$I_L = I_{OUT} \cdot \left(1 + \frac{|V_{OUT}|}{V_{IN} - \eta}\right) \quad (43)$$

- C_{IO} in the Figure 9-20 is the standard input capacitor that is used in a buck converter. C_{IN} is an input capacitor with respect to system ground which provides a low impedance path at the regulator input.
- Be sure that device logic input pin EN never exceeds the recommended maximum rating of 5.5V. For example, if EN is driven to 5V from an external source and the inverting buck-boost is configured for a –5V output, then EN is stressed to 10V (with respect to the device GND pin) which exceeds the rating of 5.5V. Take care with selecting the input voltage signals to avoid this condition. Alternatively, logic shift the signals so the signals are referenced with respect to -VOUT (which is the device GND pin).

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9.3 Power Supply Recommendations

The TPS7H4203 is designed to operate from an input voltage supply ranging from 10V to 38V. This supply voltage must be well regulated and properly bypassed to maintain correct electrical performance. At a minimum, one 4.7µF (after derating) X7R or better ceramic capacitor must be placed from PVIN to GND. In systems with stringent input ripple specifications, additional local ceramic bypass capacitance may be required. If the TPS7H4203 is located more than several inches from its input power supply, additional bulk capacitance is also recommended. Placed all bypass capacitor as close as possible to the input pins with a low-impedance path to GND. At the output, larger bypass capacitance values will improve the response to radiation-induced transients.

9.4 Layout

9.4.1 Layout Guidelines

- Layout is a critical portion of good power supply design. See *Layout Example* for a PCB layout example.
- It is recommended to include a large topside area filled with ground. This top layer ground area should be connected to the internal ground layers using vias at the input bypass capacitor, the output filter capacitor, and directly under the TPS7H4203 device in order to provide a thermal path from the exposed thermal pad to ground. The topside ground area together with the internal ground plane must provide adequate heat dissipating area.
- It is recommended that the thermal pad under the TPS7H4203 is tied to GND on internal ground layers using vias. The thermal pad does not need to directly connect to ground on the top layer in order to provide noise isolation between the thermal pad ground and the topside PGND, which may be noisy.
- There are several signal paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the performance of the power supply. To help eliminate these problems,bypass the PVIN to ground with a low ESR ceramic bypass capacitor with an X7R dielectric.
- Take care to minimize the loop area formed by the bypass capacitor connections, the PVIN pins, and the ground connections.
- Since the SW connection is the switching node, place the output inductor close to the SW pins and the PCB conductor area minimized to prevent excessive capacitive coupling.
- Use the same power ground for the output filter capacitor and the PVIN input bypass capacitor. Try to minimize this conductor length while maintaining adequate width.
- It is critical to keep the feedback trace away from inductor EMI and other noise sources. Run the feedback trace as far from the inductor, switch (SW) node, and noisy power traces as possible. Avoid routing this trace directly under the output inductor if possible. If not possible, the trace must be routed on another layer with a ground layer separating the trace and inductor.
- Keep the resistive divider used to generate the VSNS voltage as close to the device pin as possible in order to reduce noise pickup.
- The RT and COMP pins are sensitive to noise, place these components as close as possible to the IC pins and routed with minimal trace lengths.
- Make all of the power (high current) traces as short, direct, and thick as possible.
- It may be possible to obtain acceptable performance with alternate PCB layouts.

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9.4.2 Layout Example

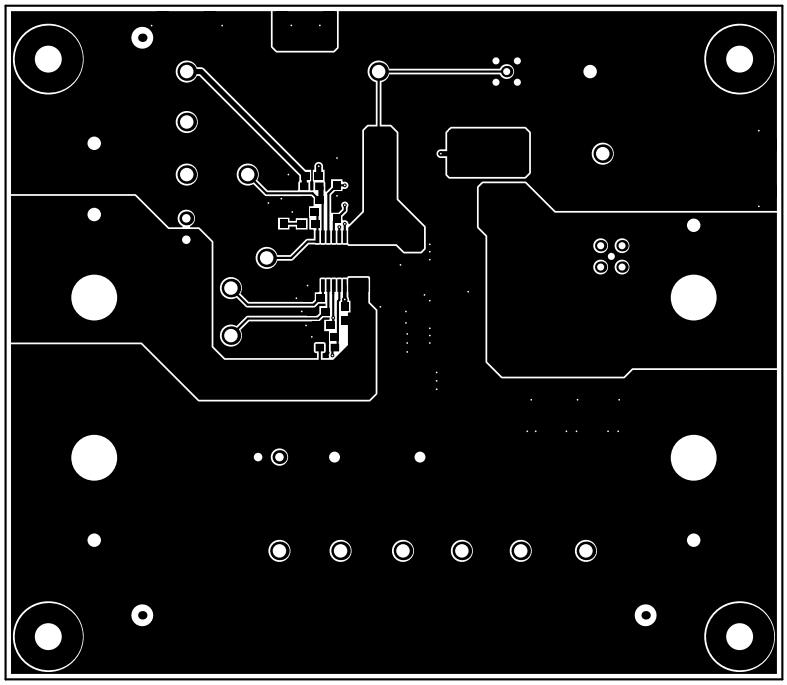


Figure 9-21. PCB Layout Example - Top Layer

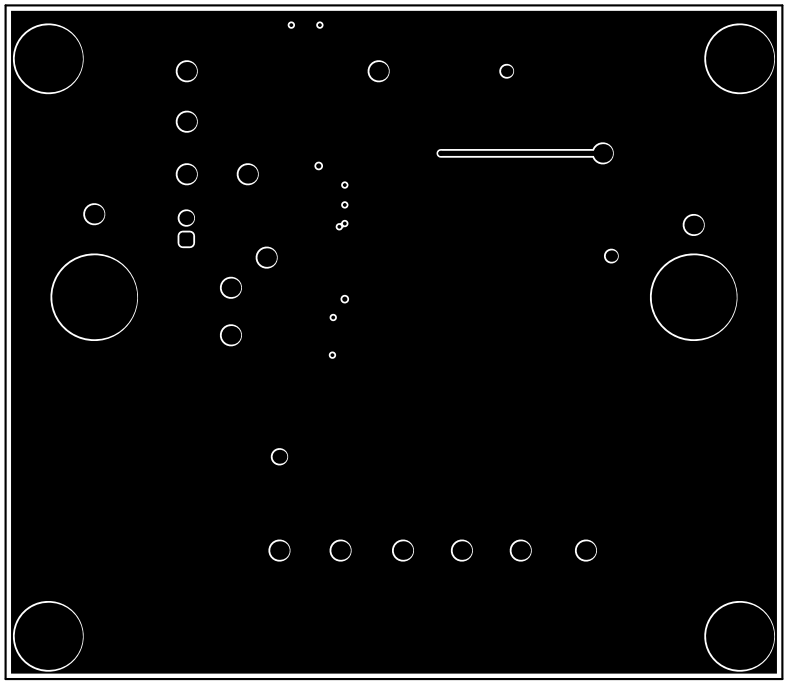


Figure 9-22. PCB Layout Example - Signal Layer 1

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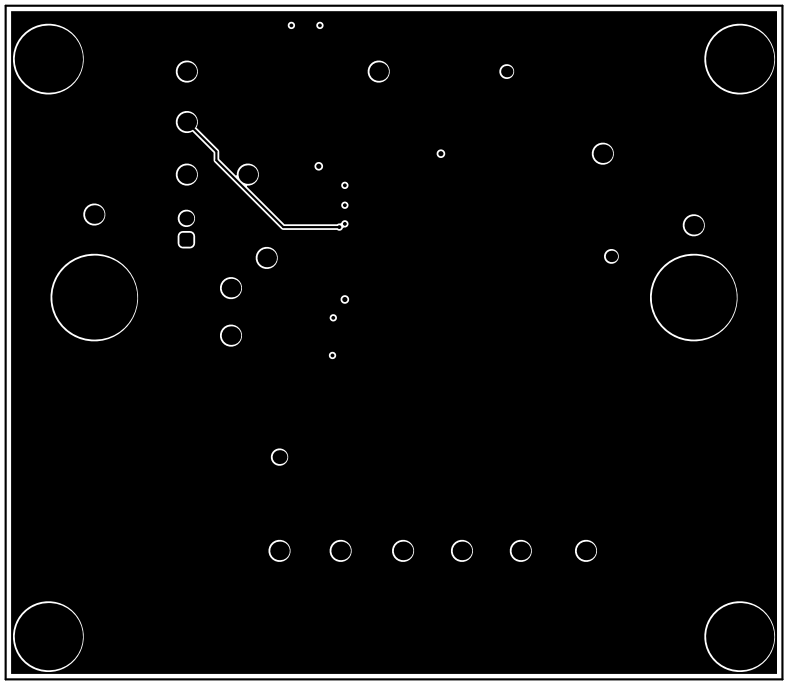


Figure 9-23. PCB Layout Example - Signal Layer 2

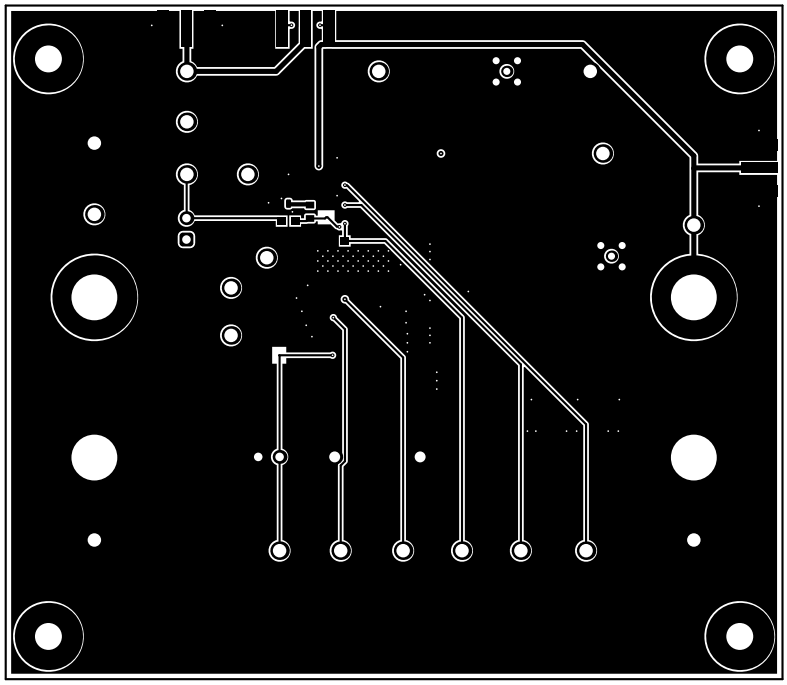


Figure 9-24. PCB Layout Example - Bottom Layer

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10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Third-Party Products Disclaimer

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10.1.2 Related Documentation

- Preliminary TPS7H4203-SEP total ionizing dose (TID) radiation report

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.4 Trademarks

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10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
October 2026	*	Initial Release

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

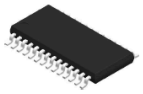
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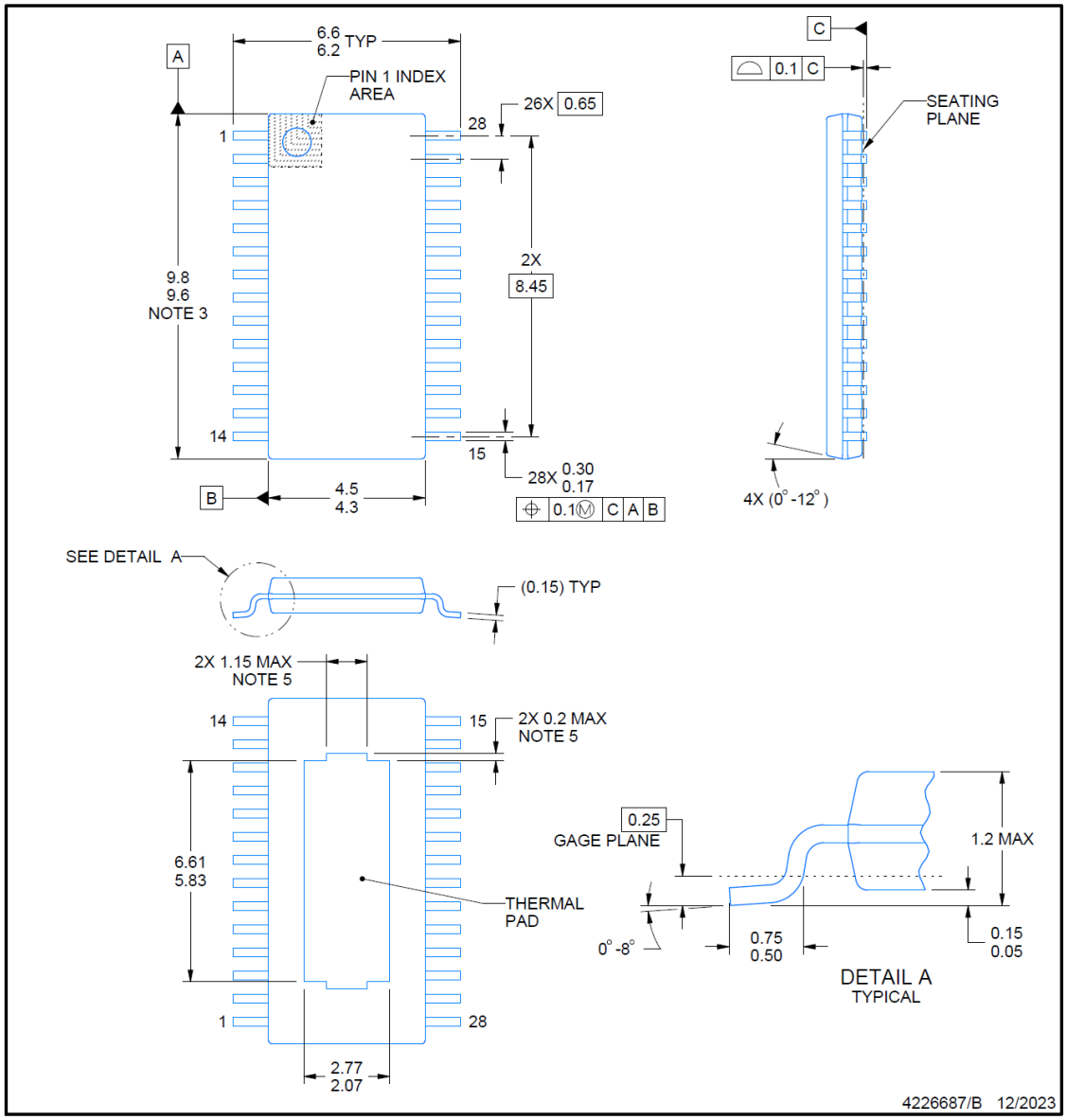
PACKAGE OUTLINE

PWP0028T



PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

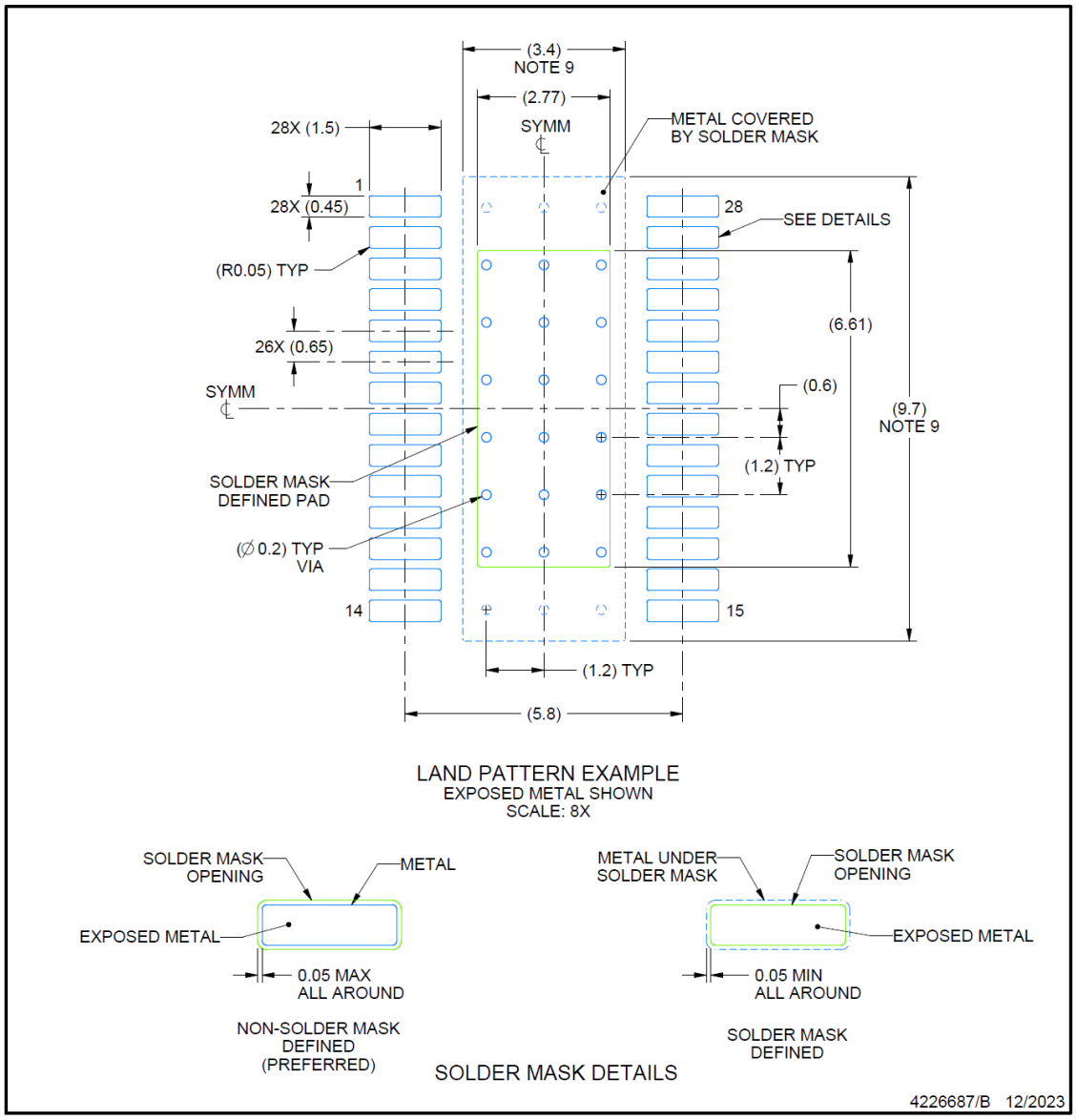
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EXAMPLE BOARD LAYOUT

PWP0028T

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

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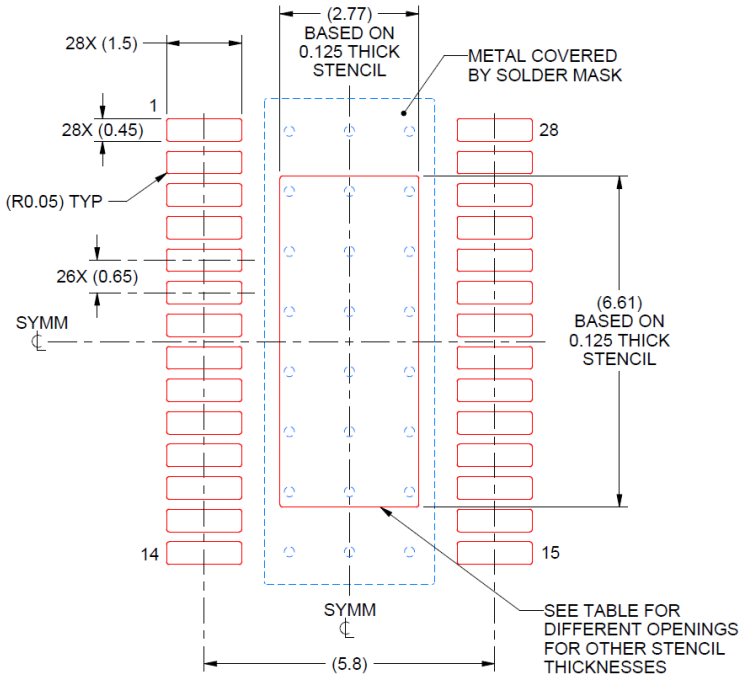
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ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

PWP0028T — **PowerPAD™ TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.10 X 7.39
0.125	2.77 X 6.61 (SHOWN)
0.15	2.53 X 6.03
0.175	2.34 X 5.59

4226687/B 12/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTPS7H4203PWPTSEP	Active	Preproduction	HTSSOP (PWP) | 28	250 | SMALL T&R	-	Call TI	Call TI	-55 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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