

TPS7H5101-SEP Radiation-Tolerant Dual Phase D-CAP+™ Controller

1 Features

- Total ionizing dose (TID) characterized up to 50krad(Si)
- Single-Event Effects (SEE) characterized
 - Single-event latchup (SEL), single-event burnout (SEB), and single-event gate rupture (SEGR) immune up to linear energy transfer (LET) = 43MeV-cm²/mg
 - Single-event functional interrupt (SEFI) and single-event transient (SET) characterized up to LET = 43MeV-cm²/mg
- D-CAP+ control and droop regulation for optimal load response
- Single or dual phase operation with single device
- Support for DrMOS and GaN power stages
- 0.5V to 2.5V nominal output voltage
- ±1% reference voltage accuracy
- Differential remote sensing
- Configurable switching frequency from 200kHz to 800kHz
- PMBus® interface at 100kHz to support:
 - ±10% voltage margining
 - On and off command
 - Packet error checking (PEC) for robust SET performance
- Available in military temperature range (–55°C to 125°C)
- Package is outgas tested per ASTM E595

2 Applications

- Point of load power supplies
- [Communications payload](#)
- [Radar imaging payload](#)

3 Description

The TPS7H5101 is a dual phase D-CAP+ buck controller. The controller is optimized for high current, point of load power delivery due to the advanced control features of the D-CAP+ architecture which support a fast transient response with low output capacitance and high efficiency. The output capacitance can further be minimized through both the use of droop regulation and by utilizing the configurable undershoot reduction (USR) feature.

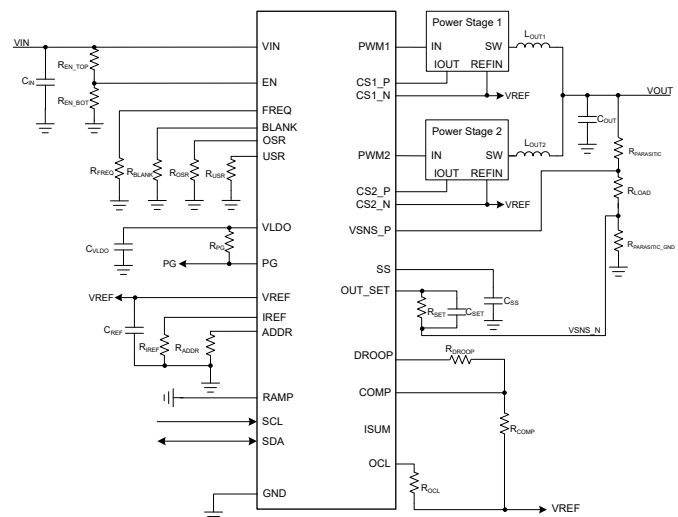
Single or dual phase operation is possible with a single controller, thereby enabling power stage optimization for different current levels.

Multiple configuration options are possible with this controller. PMBus provides the option to enable or disable the controller along with dynamically change the output voltage ±10% (voltage margining). Additional features include differential remote sensing for accurate voltage regulation and configurable compensation for an optimized control loop.

Device Information

PART NUMBER	GRADE ⁽¹⁾	BODY SIZE ⁽²⁾
TPS7H5101MDBTTSEP ⁽³⁾⁽⁴⁾	SEP	30-pin TSSOP 4.40mm × 7.80mm Mass = 99.5mg

- (1) For additional information, view the [Device Comparison Table](#).
- (2) The mass is a nominal value and the body size (length × width) is a nominal value and does not include pins.
- (3) Advance Information.
- (4) TPS7H5101MDBTTSEP is the production part number. Refer to [Device Comparison](#) for additional details regarding pre-production device part numbers.



Simplified Application



Table of Contents

1 Features	1	7.5 Programming.....	32
2 Applications	1	8 Register Map	34
3 Description	1	9 Application and Implementation	36
4 Device Comparison Table	3	9.1 Application Information.....	36
5 Pin Configuration and Functions	4	9.2 Typical Application.....	36
6 Specifications	7	9.3 Power Supply Recommendations.....	42
6.1 Absolute Maximum Ratings.....	7	9.4 Layout.....	42
6.2 ESD Ratings.....	7	10 Device and Documentation Support	45
6.3 Recommended Operating Conditions.....	7	10.1 Documentation Support.....	45
6.4 Thermal Information.....	8	10.2 Receiving Notification of Documentation Updates.....	45
6.5 Electrical Characteristics.....	9	10.3 Support Resources.....	45
6.6 Typical Characteristics.....	12	10.4 Trademarks.....	45
7 Detailed Description	15	10.5 Electrostatic Discharge Caution.....	45
7.1 Overview.....	15	10.6 Glossary.....	45
7.2 Functional Block Diagram.....	15	11 Revision History	45
7.3 Feature Description.....	16	12 Mechanical, Packaging, and Orderable Information	46
7.4 Device Functional Modes.....	31		

4 Device Comparison Table

GENERIC PART NUMBER	RADIATION RATING ⁽¹⁾	GRADE ⁽²⁾	PACKAGE	ORDERABLE PART NUMBER ⁽⁵⁾
TPS7H5101-SEP	TID of 50krad(Si) RLAT, DSEE free to 43MeV- cm ² /mg	Space Enhanced Plastic	30-pin plastic	PTPS7H5101DBBTSEPA ⁽³⁾
				PTPS7H5101DBBTSEPB ⁽⁴⁾

- (1) TID is total ionizing dose and DSEE is destructive single event effects. Additional information is available in the associated TID reports and SEE reports for each product.
- (2) For additional information about part grade, view [part ratings](#).
- (3) Advance information.
- (4) Product preview.
- (5) PTPS7H5101DBBTSEPA is Revision A of the pre-production device, while PTPS7H5101DBBTSEPB is Revision B of the pre-production device. TPS7H5101DBBTSEP is the orderable part number for the production released version of the product.

ORDERABLE PART NUMBER	VIN INTERNAL UVLO RISING THRESHOLD (NOMINAL)	VIN INTERNAL UVLO FALLING THRESHOLD (NOMINAL)
PTPS7H5101DBBTSEPA	7.0V	6.8V
PTPS7H5101DBBTSEPB	3.8V	3.6V

ADVANCE INFORMATION

5 Pin Configuration and Functions

ISUM	1	30	COMP
USR	2	29	DROOP
OSR	3	28	OCL
BLANK	4	27	VREF
FREQ	5	26	CS1_P
RAMP	6	25	CS1_N
OUT_SET	7	24	CS2_P
IREF	8	23	CS2_N
EN	9	22	VSNS_P
VIN	10	21	SS
GND	11	20	VLDO
NC	12	19	NC
ADDR	13	18	PG
SCL	14	17	PWM1
SDA	15	16	PWM2

**Figure 5-1. TPS7H5101-SEP DBT Package, 30-Pin TSSOP
(Top View)**

Table 5-1. Pin Functions

PIN		I/O ⁽¹⁾	DESCRIPTION ⁽²⁾
NAME	TSSOP (30)		
ISUM	1	O	Analog current monitor output. The voltage on this pin is a 1:1 representation of the summed voltages of the CSx_P and CSx_N pins (ISUM). ISUM is a voltage relative to VREF.
USR	2	I	Undershoot reduction. The threshold for activating the undershoot reduction feature can be programmed using a resistor from the pin to GND. The undershoot reduction feature can also be disabled by connecting a resistor greater than 2MΩ to GND, or by floating the pin.
OSR	3	I	Overshoot reduction. A resistor to GND sets the overshoot reduction threshold for the controller. The overshoot reduction feature can also be disabled by connecting a resistor greater than 2MΩ to GND, or by floating the pin.
BLANK	4	I	Blanking time. This is also the minimum PWM off-time. Program the desired blanking time using a resistor to ground on this pin. If this pin is left open, the controller defaults to a blanking time of 40ns (typ).
FREQ	5	I	Frequency set. A resistor to GND is used to set the nominal switching frequency of the controller during normal operation. Note that the frequency varies slightly based on the input voltage, output voltage, and converter loading conditions.
RAMP	6	I	Ramp compensation set. This pin is used to configure the ramp compensation voltage of the controller. The pin can be connected to VLDO, GND, or left floating to select one of three levels for the ramp voltage amplitude.
OUT_SET	7	I	Output voltage set. The output voltage setpoint is configured using this pin, such that $V_{OUT} = I_{REF} \times R_{SET}$. R_{SET} is the resistor connected from OUT_SET to VSNS_N, which is the ground reference at the load. A 470pF capacitor can be connected across R_{SET} for single-event-transient mitigation.
IREF	8	I	Current reference. Add a 169kΩ resistor to ground to generate the internal reference current I_{REF} of approximately 10μA. This reference current is mirrored on the OUT_SET pin and used to program the output voltage.
EN	9	I	Enable. Driving this pin to logic high enables the device given all other enabling conditions have also been met. Driving the pin to logic low disables the device. A resistor divider from VIN to GND can also be used to set the device turn-on level.
VIN	10	I	Input voltage. Voltage supply for the controller and internal circuitry. Connect this pin to the supply voltage of the buck converter power stage to maintain the proper output frequency and on-time of the controller outputs (PWM1 and PWM2).

Table 5-1. Pin Functions (continued)

PIN		I/O ⁽¹⁾	DESCRIPTION ⁽²⁾
NAME	TSSOP (30)		
GND	11	—	Ground. Serves as the return for the internal control circuitry.
NC	12	—	No connect. This pin is not internally connected. This pin can be connected to GND to prevent charge buildup; however, this pin can also be left open or tied to any voltage between GND and VIN
ADDR	13	I	Address. Sets the lower four-bits of the PMBus address using a resistor to GND. Use a 0.1% tolerance resistor or better for address setting. See the Electrical Characteristics table for more details.
SCL	14	I	Serial clock line. Serves as the clock input for the PMBus interface of the controller.
SDA	15	I/O	Serial data line. Transmits the data I/O for the PMBus interface of the controller.
PWM2	16	O	Controller output for the second phase of the multiphase buck. The signal is sent to the second power stage or driver input and is DrMOS compatible. If the second output is not desired to be used, the output can be disabled by connecting CS2_N to VLDO.
PWM1	17	O	Controller output for the first phase of the multiphase buck. The signal is sent to the first power stage or driver input and is DrMOS compatible.
PG	18	O	Power good. Open-drain pin that is pulled up to desired logic level using an external resistor. Used to detect an undervoltage on the output voltage and is asserted when the output voltage is within 10% of the programmed value. PG is deasserted when the output voltage is more than 12% less than the programmed value or during thermal shutdown.
NC	19	—	No connect. This pin is not internally connected. This pin can be connected to GND to prevent charge buildup; however, this pin can also be left open or tied to any voltage between GND and VIN
VLDO	20	O	Linear regulator output capacitor pin. A 1µF capacitor must be placed on this pin for the internal linear regulator. The output voltage is nominally 5V. Do not load this pin with any additional external connections other than where explicitly allowed in the datasheet.
SS	21	I/O	Soft start. An external capacitor connected to this pin controls the output voltage rise time to limit inrush current.
VSNS_P	22	I	Output voltage sense. Connect directly to VOUT sense point at the load to provide remote sense for the controller. Note that although there is no dedicated pin for the VOUT ground sense point at the load, VSNS_N, the negative terminal of the R _{SET} resistor is connected to this point.
CS2_N	23	I	Negative current sense for the second phase of a multiphase buck. Connect to the negative sense output or the VREF of the second power stage. This pin can also be connected to the negative terminal of the current sense resistor or output inductor for inductor current sensing. Differentially route with CS2_P. If PWM2 output is not used, then connect this pin to VLDO to disable the output.
CS2_P	24	I	Positive current sense for the second phase of the multiphase buck. Connect to the sense output current of the second power stage. This pin can also be connected to the positive terminal of the phase current sense resistor or inductor for inductor current sensing. Differentially route with CS2_N on the printed circuit board layout. If PWM2 output is not used, then connect this pin to VLDO.
CS1_N	25	I	Negative current sense for first phase of multiphase buck. Connect to the negative sense output or the VREF of the first power stage. Can also be connected to the negative terminal of the current sense resistor or output inductor for inductor current sensing. Differentially route with CS1_P on the printed circuit board layout.
CS1_P	26	I	Positive current sense for the first phase of the multiphase buck. Connect to the sense output current of the first power stage. Can also be connected to the positive terminal of the phase current sense resistor or inductor for inductor current sensing. Differentially route with CS1_N.
VREF	27	O	Voltage reference output. A 470nF external capacitor is required for the internal bandgap reference. The voltage is nominally 1.7V. Do not connect external circuitry to this pin unless explicitly allowed in the datasheet.
OCL	28	I/O	Overcurrent limit. Use this pin to program the overcurrent detection level for CSx_P – CSx_N on both current sense inputs. If the threshold is exceeded on either phase, the controller enters current limiting mode.
DROOP	29	O	Droop amplifier output. R _{DROOP} (between DROOP and COMP) and R _{COMP} (between COMP and VREF) set the droop gain for the controller. See <i>Droop Control</i> section for more details on how to program the load-line behavior for the controller output.

Table 5-1. Pin Functions (continued)

PIN		I/O ⁽¹⁾	DESCRIPTION ⁽²⁾
NAME	TSSOP (30)		
COMP	30	I	Noninverting input of internal droop amplifier. R_{DROOP} (between DROOP and COMP) and R_{COMP} (between COMP and VREF) set the droop gain for the controller. See <i>Droop Control</i> section for more details on how to program the load-line behavior for the controller output.

(1) I = Input, O = Output, I/O = Input or Output, — = Other

(2) For pins that are allowed to be left open as part of the configuration (USR, OSR, BLANK, RAMP), note that internally the pin is pulled to a known potential and as such the pin is not a floating node in this state.

6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Input voltage	VIN	−0.3	16	V
	PG, SCL, SDA, EN, CS1_N, CS1_P, CS2_N, CS2_P, RAMP, OSR, USR, BLANK	−0.3	7.5	
	ADDR, VSNS_P	−0.3	3.6	
Output voltage	PWM1, PWM2, VLDO	−0.3	7.5	V
	COMP, FREQ, IREF, ISUM, OCL, OUT_SET, SS	−0.3	3.6	
Output voltage	DROOP	−0.3	6.0	V
Output voltage	VREF	−0.3	2.5	V
Sink current	PG	−0.1	5	mA
Input current	SCL, SDA	−0.1	5	mA
T _J	Junction temperature	−55	150	°C
T _{stg}	Storage temperature	−65	150	

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±500	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins ⁽²⁾	±250	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input voltage	VIN (Rev A)	8		15	V
Input voltage	VIN (Rev B)	4.5		15	V
Input voltage	PG, EN	0		7	V
	ADDR	0		3.5	
	VSNS_P	0		2.75	
	SCL, SDA, CS1_N, CS1_P, CS2_N, CS2_P, RAMP, OSR, USR, BLANK	0		5.5	
Output voltage	PWM1, PWM2	0		7	V
	COMP, FREQ, IREF, ISUM, OCL, OUT_SET, REF, SS	0		3.5	
	Configurable output voltage range	0.45		2.75	
Output voltage	OUT_SET	0		2.75	V
Output voltage	VLDO, DROOP	0		5.5	V
Sink current	PG	0		2	mA
Input current	SCL, SDA	0		4	mA
T _J	Junction temperature	−55		125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TP7H5101	UNIT
		DBT (TSSOP)	
		30 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	79.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	15.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	33.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	32.6	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

4.5V ≤ VIN ≤ 15V⁽¹⁾, TA = -55°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY VOLTAGES AND CURRENTS							
I _{Q_VIN}	VIN operating quiescent current	C _{LOAD} = 25 pF for PWMx	No Switching	4.5	7		mA
I _{Q_VIN}	VIN operating quiescent current	C _{LOAD} = 25 pF for PWMx	Max Switching	6	12		mA
I _{Q_VIN}	VIN operating quiescent current	C _{LOAD} = 25 pF for PWMx (single output operation)	Max Switching	6	10		mA
I _{SHDN_VIN}	VIN shutdown supply current	EN = 0V OR disabled through PMBus		1.5	5		mA
ENABLE AND UNDERVOLTAGE LOCKOUT							
V _{EN(rising)}	Enable rising threshold (turn-on)			0.56	0.6	0.64	V
V _{EN(falling)}	Enable falling threshold (turn-off)			0.46	0.5	0.54	
V _{EN(HYS)}	Enable threshold hysteresis			0.1			
t _{EN(delay)}	Enable propagation delay	EN high to PWM1 high, SS pin open		0.08	0.6		ms
t _{UVLO(delay)}	UVLO propagation delay	VIN UVLO good to PWM1 high, SS pin open, EN = 5V		0.6	2		ms
t _{ON(delay)}	PMBus turn-on command propagation delay	Turn-on command stop bit received to PWM1 high, SS pin open		55	120		μs
I _{EN(LKG)}	Enable input leakage current	EN = 7V		5	100		nA
V _{UVLOR_VIN}	VIN internal UVLO rising threshold (Rev A)			6.7	7.0	7.3	V
V _{UVLOF_VIN}	VIN internal UVLO falling threshold (Rev A)			6.5	6.8	7.1	V
V _{UVLOHYST_VIN}	VIN internal UVLO hysteresis (Rev A)			0.2			V
V _{UVLOR_VIN}	VIN internal UVLO rising threshold (Rev B)			3.5	3.8	4.1	V
V _{UVLOF_VIN}	VIN internal UVLO falling threshold (Rev B)			3.3	3.6	3.9	
V _{UVLOHYST_VIN}	VIN internal UVLO hysteresis (Rev B)			0.2			
VOLTAGE REFERENCE							
V _{OUT_SET}	Output set voltage	R _{OUT_SET} = 50kΩ		497.5	502.5	507.5	mV
I _{OUT_SET}	Output set current	169kΩ between IREF and GND		9.90	10.05	10.20	μA
V _{REF}	Reference voltage	C _{REF} = 470nF		1.661	1.68	1.706	V
ERROR AMPLIFIER							
EA _{DC}	Error amplifier total gain	V _{SNS_P} to DROOP		10000			V/V
EA _{ISRC}	Error amplifier source current	100mV input overdrive		450	850	1550	μA
EA _{ISNK}	Error amplifier sink current			450	850	1550	
SOFT START							
I _{SS}	Soft-start current	V _{SS} = 0.3V		1.3	2	2.7	μA
RAMP COMPENSATION							
V _{RAMP}	Compensation ramp amplitude	RAMP = GND		17	20	26	mV
		RAMP = open		34	60	85	
		RAMP = VLDO		89	100	115	
CURRENT SENSE AND OVERCURRENT							
I _{OCL}	Over current limit pin source current			4.5	5	5.5	μA

6.5 Electrical Characteristics (continued)

4.5V ≤ VIN ≤ 15V⁽¹⁾, TA = -55°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V _{OCL}	Over current limit threshold (valley current limit at CSx_P – CSx_N)	R _{OCL} = 4.02kΩ		10	20.1	30	mV
		R _{OCL} = 20kΩ		90	100	110	
		R _{OCL} = 40.2kΩ		180	201	220	
V _{OCL_HYS}	Over current limit hysteresis			20			%
SWITCHING FREQUENCY							
t _{ON}	PWM on-time	VIN = 12V, V _{OUT_SET} = 0.8V	R _{FREQ} = 100kΩ (200kHz)	333			ns
		VIN = 12V, V _{OUT_SET} = 0.8V	R _{FREQ} = 40.2kΩ (500kHz)	133			
		VIN = 12V, V _{OUT_SET} = 0.8V	R _{FREQ} = 25kΩ (800kHz)	83			
		VIN = 6V, V _{OUT_SET} = 0.8V	R _{FREQ} = 40.2kΩ (500kHz)	267			
t _{ON(min)}	Minimum on-time			55			ns
t _{OFF(min)}	Minimum off-time (blanking)	R _{FREQ} = 40.2kΩ (500kHz)	R _{BLANK} = open	40	65	90	ns
			R _{BLANK} = 56.2kΩ	80	110	140	
			R _{BLANK} = 124kΩ	135	160	185	
			R _{BLANK} = 191kΩ	195	210	235	
			R _{BLANK} = 464kΩ	330	400	480	
PWM OUTPUTS							
V _{PWMx(OL)}	PWMx output low	I _{SINK} = 1mA		0.1			V
V _{PWMx(OH)}	PWMx output high	I _{SOURCE} = 1mA		4.2			
V _{PWMx(tri)}	PWMx tri-state	I _{LOAD} = ±500μA		1.58			
t _{PWMx_r}	PWMx rise time	C _{LOAD} = 25pF	10% to 90%	6			ns
t _{PWMx_f}	PWMx fall time		90% to 10%	6			
t _{PWMx_tri}	PWMx tri-state transition time	C _{LOAD} = 25pF, 10% to 1.6V		6			ns
POWER GOOD							
PG _{falling}	Power good falling threshold (fault)	Threshold for PG as percent of V _{OUT_SET}		85%	88%	91%	
PG _{rising}	Power good rising threshold (good)			87%	90%	93%	
IPG(LKG)	Output high leakage	V _{PG} = 7V		50			nA
V _{PG(OL)}	Power good output low	I _{PG(sink)} = 2mA		105			mV
VIN _{MIN_PG}	Minimum VIN for valid PG output	Measured when V _{PG} ≤ 0.5V at 100μA		0.5			V
T _{SD(enter)}	Thermal shutdown enter temperature			165	175	185	°C
T _{SD(exit)}	Thermal shutdown exit temperature			130	140	150	
OVERSHOOT REDUCTION							
V _{OSR}	Overshoot reduction voltage	R _{OSR} = 316kΩ		10	50	95	mV
	Overshoot reduction voltage	R _{OSR} = 75kΩ		135	200	250	
	Overshoot reduction voltage	R _{OSR} = 36.5kΩ		300	400	450	
	Overshoot reduction voltage	R _{OSR} ≥ 2MΩ		OFF			
V _{OSR_H}	Overshoot reduction voltage hysteresis	All settings		20			%

6.5 Electrical Characteristics (continued)

4.5V ≤ VIN ≤ 15V⁽¹⁾, TA = -55°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
UNDERSHOOT REDUCTION								
V _{USR}	Undershoot reduction voltage	R _{USR} = 316kΩ		10	50	100	mV	
		R _{USR} = 154kΩ		40	100	150		
		R _{USR} = 75kΩ		115	200	265		
		R _{USR} ≥ 2MΩ		OFF				
V _{USR_H}	Undershoot reduction voltage hysteresis	All settings		20			%	
PMBus								
f _{SCL}	Clock operating frequency			10		100	kHz	
V _{IL_PMBus}	SCL and SDA low-level input voltage			0.8			V	
V _{IH_PMBus}	SCL and SDA high-level input voltage			1.35			V	
V _{HYS_PMBus}	SCL and SDA hysteresis of Schmitt trigger inputs			80			mV	
V _{OL_PMBus}	SCL and SDA low-level input voltage	I _{OL} = 4mA		0.4			V	
V _{IH_PMBus}	SCL and SDA pin leakage			-10	10		μA	
t _{TIMEOUT}	Detect clock low timeout			25	32	42	ms	
ADDR	Resistance range for setting PMBus address (ADDR = 001 xxxx) ⁽²⁾	Address code of 4 LSB = 0000b		913.1	1500	kΩ		
		Address code of 4 LSB = 0001b		472.4	626			774.6
		Address code of 4 LSB = 0010b		301.6	348			394.1
		Address code of 4 LSB = 0011b		230.0	246			261.5
		Address code of 4 LSB = 0100b		180.9	189			197.1
		Address code of 4 LSB = 0101b		151.3	154			157.6
		Address code of 4 LSB = 0110b		129.1	130			131.7
		Address code of 4 LSB = 0111b		112.0	113			114.0
		Address code of 4 LSB = 1000b		90.4	94.1			98.8
		Address code of 4 LSB = 1010b		74.9	76.8			79.1
		Address code of 4 LSB = 1100b		64.5	64.9			66.2
		Address code of 4 LSB = 1110b			49.9			56.5

(1) Input voltage range is 8V ≤ VIN ≤ 15V for Rev. A of TPS7H5101. Rev. B has an input voltage range of 4.5V ≤ VIN ≤ 15V.

(2) For best results, use 0.1% resistor that correlates to the typical value.

6.6 Typical Characteristics

Typical characteristics shown are for TPS7H5101 with VIN from 8V to 15V, $T_A = -55^\circ\text{C}$, 25°C , and 125°C , unless otherwise noted.

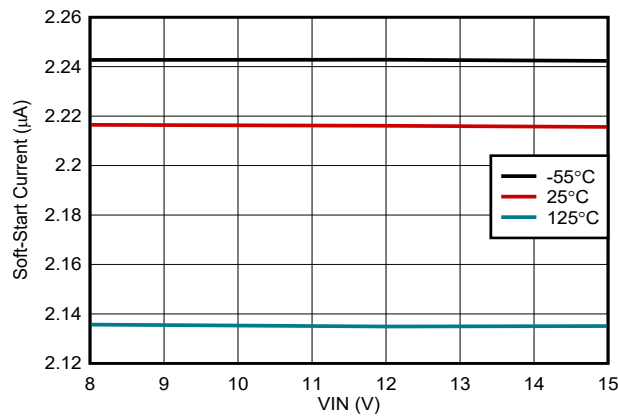
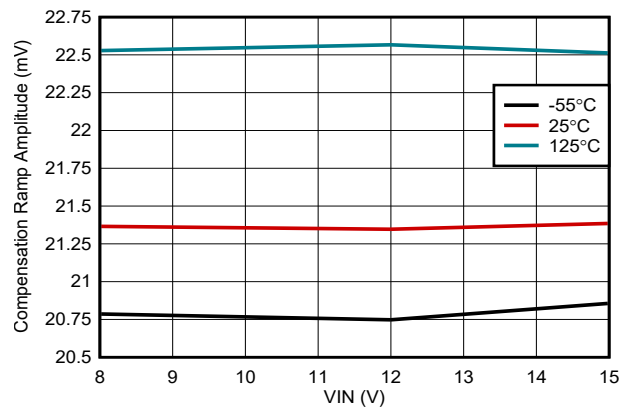
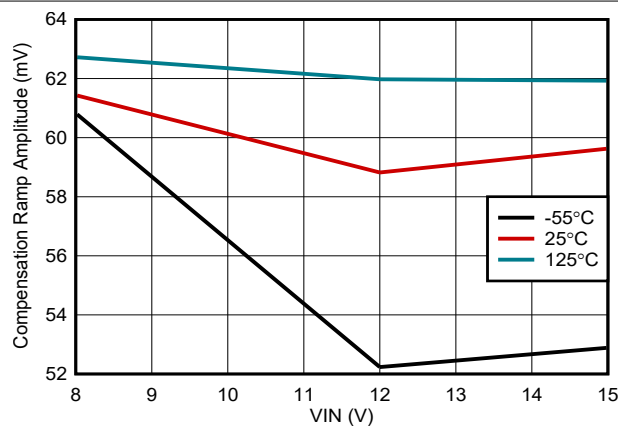


Figure 6-1. Soft-Start Current vs Input Voltage



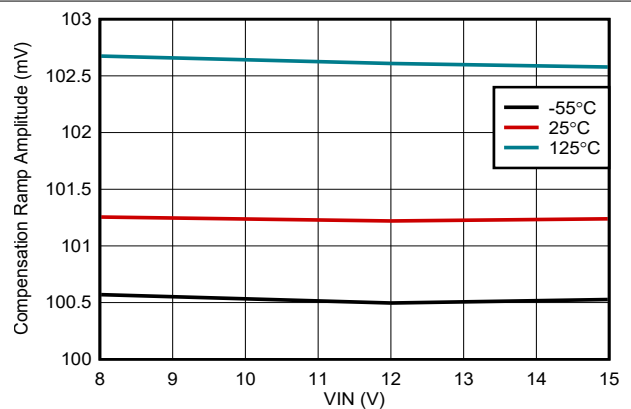
RAMP = GND

Figure 6-2. Compensation Ramp Amplitude vs Input Voltage



RAMP = OPEN

Figure 6-3. Compensation Ramp Amplitude vs Input Voltage



RAMP = VLDO

Figure 6-4. Compensation Ramp Amplitude vs Input Voltage

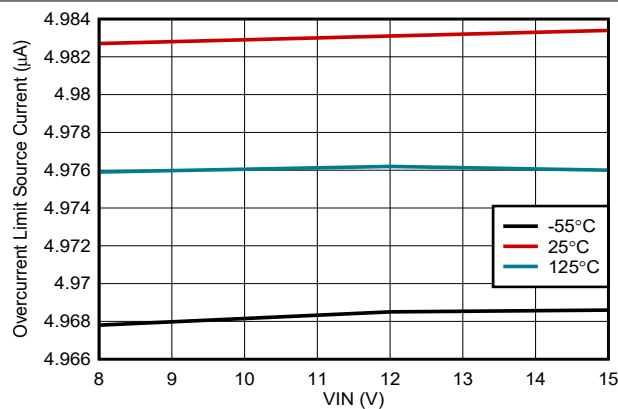
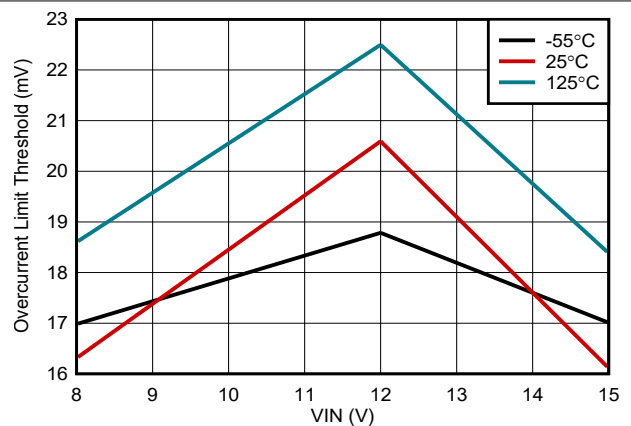


Figure 6-5. Overcurrent Limit Source Current vs Input Voltage



$R_{OCL} = 4.02\text{k}\Omega$

Figure 6-6. Overcurrent Limit Threshold vs Input Voltage

6.6 Typical Characteristics (continued)

Typical characteristics shown are for TPS7H5101 with VIN from 8V to 15V, $T_A = -55^\circ\text{C}$, 25°C , and 125°C , unless otherwise noted.

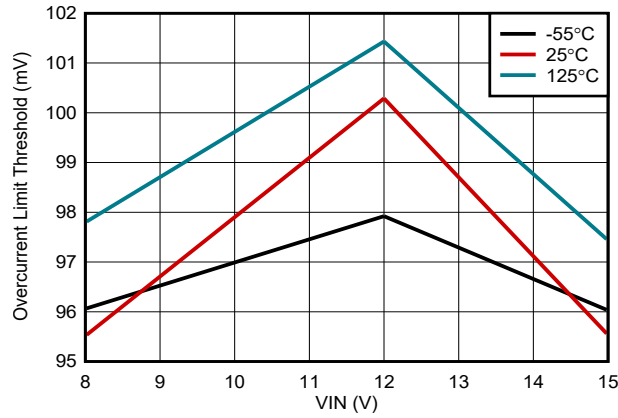


Figure 6-7. Overcurrent Limit Threshold vs Input Voltage

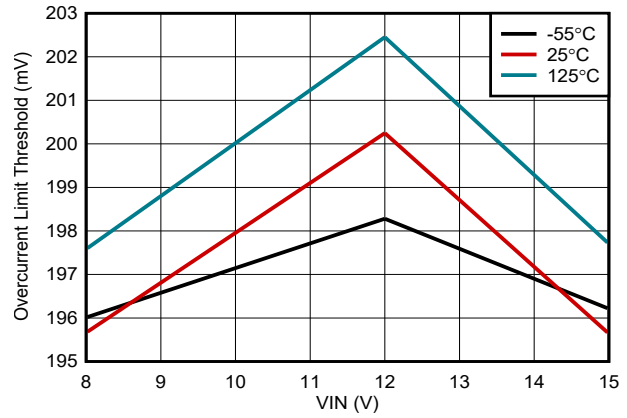


Figure 6-8. Overcurrent Limit Threshold vs Input Voltage

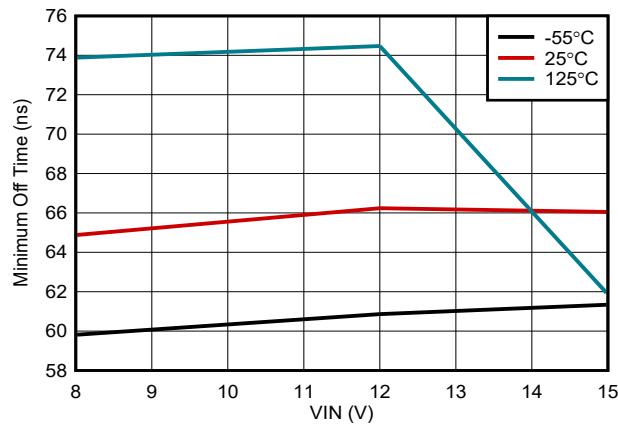


Figure 6-9. Minimum Off Time (Blanking) vs Input Voltage

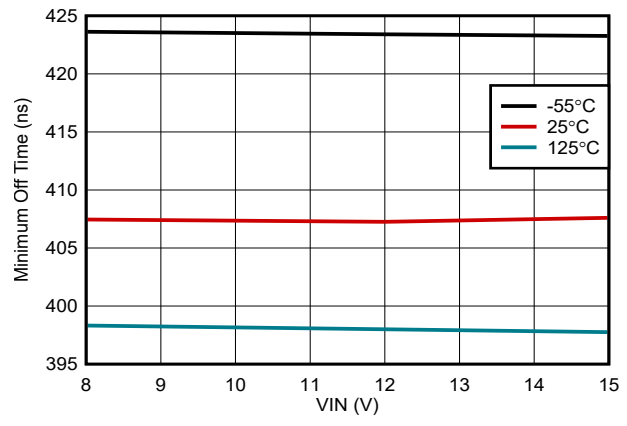


Figure 6-10. Minimum Off Time (Blanking) vs Input Voltage

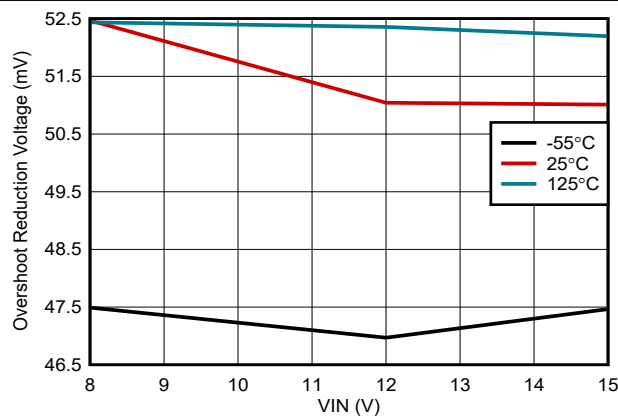


Figure 6-11. Overshoot Reduction Voltage vs Input Voltage

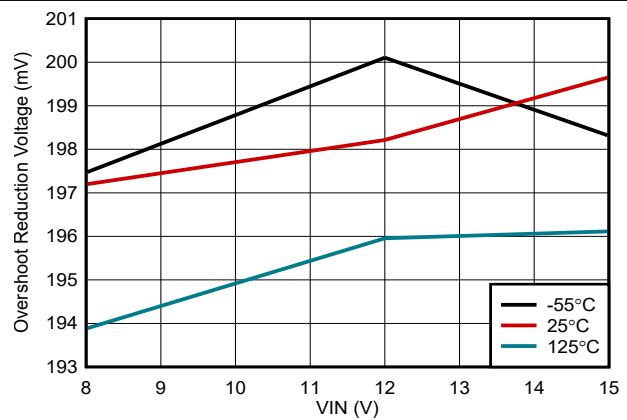


Figure 6-12. Overshoot Reduction Voltage vs Input Voltage

6.6 Typical Characteristics (continued)

Typical characteristics shown are for TPS7H5101 with VIN from 8V to 15V, $T_A = -55^\circ\text{C}$, 25°C , and 125°C , unless otherwise noted.

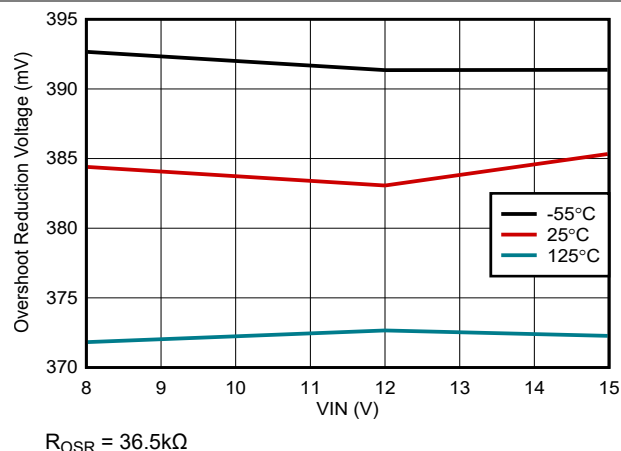


Figure 6-13. Overshoot Reduction Voltage vs Input Voltage

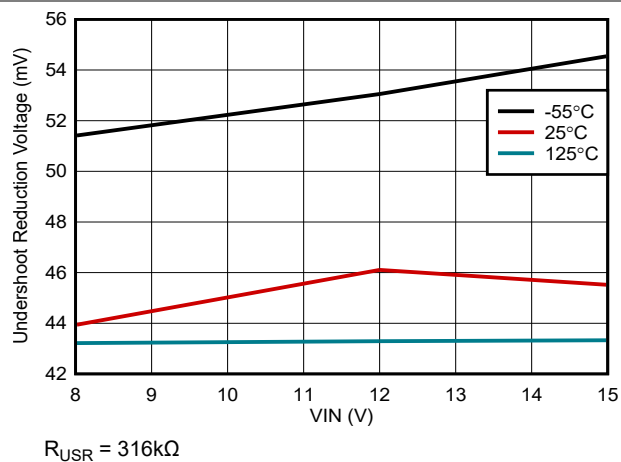


Figure 6-14. Undershoot Reduction Voltage vs Input Voltage

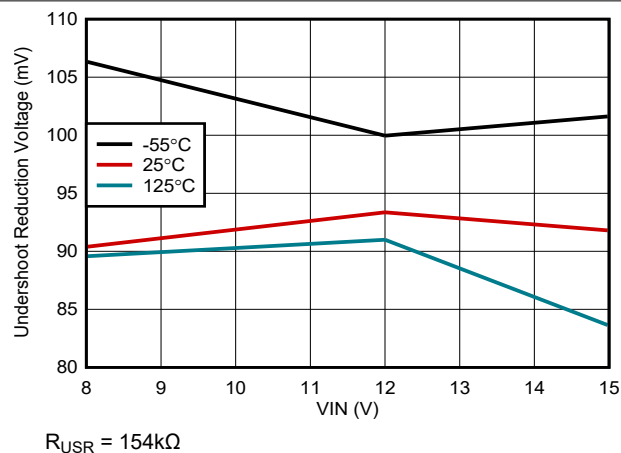


Figure 6-15. Undershoot Reduction Voltage vs Input Voltage

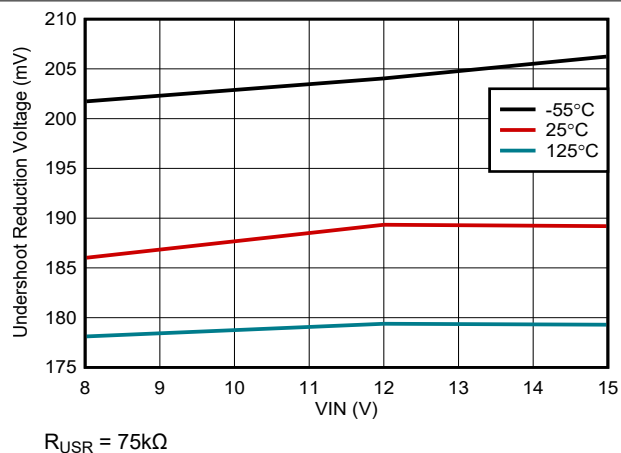


Figure 6-16. Undershoot Reduction Voltage vs Input Voltage

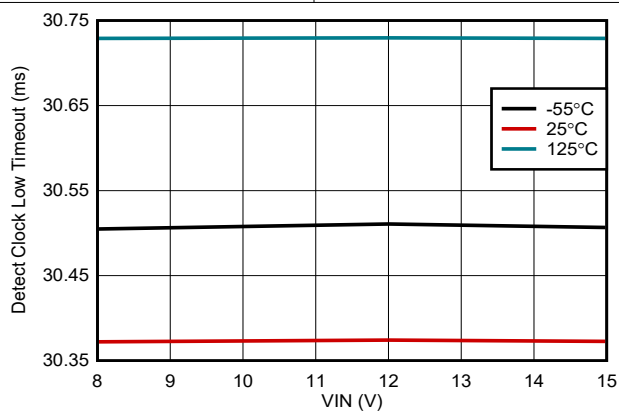


Figure 6-17. Detect Clock Low Timeout vs Input Voltage

7 Detailed Description

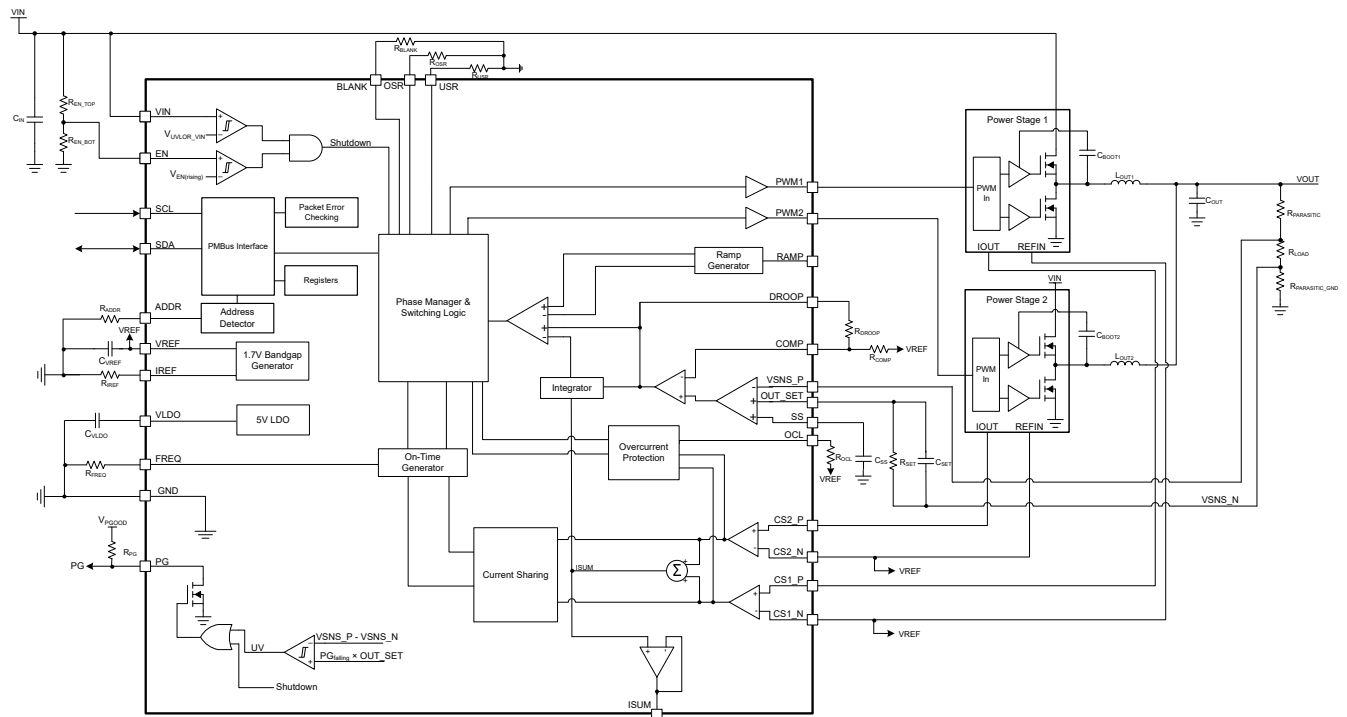
7.1 Overview

The TPS7H5101 is a dual phase D-CAP+ buck controller that utilizes an adaptive on-time control methodology capable of maintaining a pseudo-fixed frequency during the steady state operation that is user programmable. The controller is suitable for high-current, low-voltage point-of-load power delivery typically required for FPGA and ASIC core voltages due to its advanced control features. These features include droop, undershoot reduction, and overshoot reduction, which all support an improved transient response with both low output capacitance and high efficiency.

The controller can support both single and dual phase operation, allowing for power stage optimization depending on the load that is being supplied. In dual phase mode, an internal phase manager is utilized that displaces the output signals of each phase by 180° during steady-state operation. The outputs are never allowed to be commanded on simultaneously except during transient conditions with undershoot reduction enabled, as this aids with the reduction of output voltage deviation. There is also an active current sharing circuit that adjusts the on-time of each phase as needed to maintain approximately equal currents in each phase of the converter.

There are also multiple configuration options for this controller that can be achieved using PMBus. PMBus provides the user the option to enable or disable the controller, as well as dynamically changing the output voltage by a $\pm 10\%$ voltage margin. The controller also utilizes differential remote sensing which is suitable for high accuracy requirements that are often necessary for many of the low voltage and high current power rails.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 D-CAP+

D-CAP+ is a control architecture optimized for high-current, low duty cycle multiphase regulators. It utilizes adaptive on-time control. In this control method, rather than varying the duty cycle to maintain voltage regulation as is the standard with peak current mode control, the high-side FET is turned on for a predetermined amount of time once the control loop triggers the turn-on. However, in contrast to classic constant on-time control, in which the on-time is the same regardless of the operating conditions, adaptive on-time allows for variation based on the input voltage, output voltage, and load to maintain a pseudo-constant frequency during steady state operation.

The controller senses current from the converter using an output from the power stages or inductor sensing, whether using the inductor DCR or a series resistor. The current from each phase is sensed and summed internally to the controller to generate the ISUM signal. The on-time pulses are generated by the controller when the valley of the sensed current waveform ISUM intersects with the error correction signal VDROOP at the output of the droop amplifier. Note that the D-CAP+ method does not require an internal oscillator, but the SW_CLK signal corresponding to the intersection of ISUM and VDROOP is generated each time the on-time pulse is triggered on either phase.

In the case of multiphase operation, the phase manager is used to distribute the SW_CLK signal to the appropriate phase with the proper interleaving of 180°. During single phase operation, ISUM corresponds to the single phase current and SW_CLK generates a pulse on the same phase for each cycle. [Figure 7-1](#) shows the basic waveforms for D-CAP+, in which VDROOP can be seen to contain a component of the output voltage ripple.

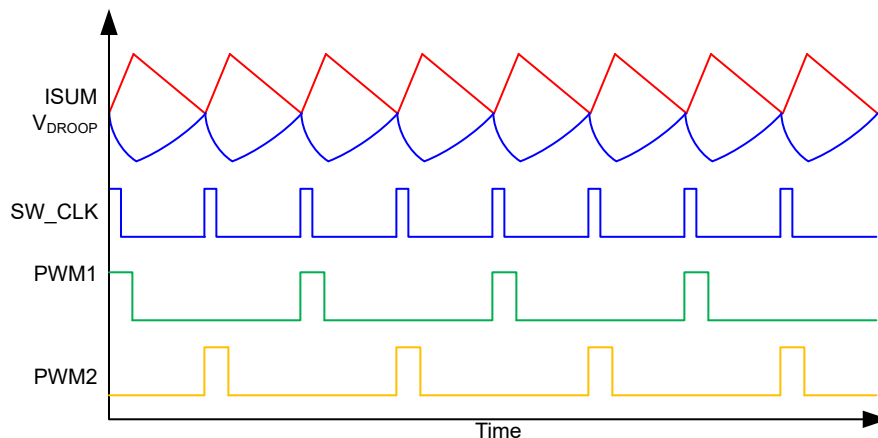


Figure 7-1. D-CAP+ Basic Waveforms

7.3.1.1 Load Transients

The D-CAP+ control method offers exceptional load transient response, which is one of the benefits compared to more classical control methods often utilized for point-of-load converters. During a rapid rising load step, the output voltage of the converter subsequently drops. A rise in the DROOP voltage corresponds to the decrease in the output voltage, and as a result the outputs of the TPS7H5101 start to generate pulses more frequently. The inductor current rises rapidly due to the fast pulse generation until such time when the new load current is reached and the outputs resume switching at the steady-state frequency.

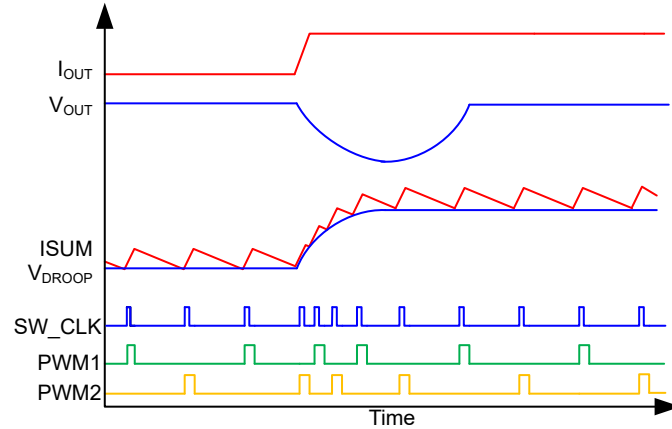


Figure 7-2. Rising Load Step Response

In the event of a rapid load release, the output voltage rises suddenly. A fall in the DROOP voltage corresponds to the increase in the output voltage, and this in turn forces a delay in the output pulses of the TPS7H5101 until the new load current is reached. Afterwards, the steady-state switching at the nominal frequency is resumed.

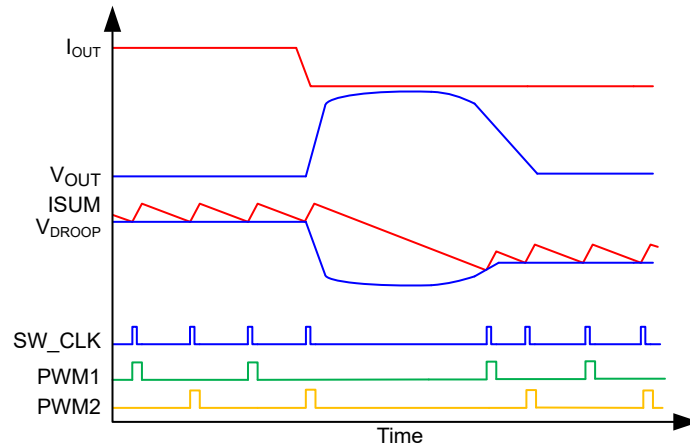


Figure 7-3. Falling Load Step Response

7.3.1.2 On-Time Control

During steady-state, the on-time of the output is determined approximately according to [Equation 1](#):

$$t_{ON} \cong \frac{V_{OUT}}{V_{IN} \times f_{SW}} \quad (1)$$

where:

- V_{OUT} is the converter output voltage
- V_{IN} is the converter input voltage, which must be the same as the controller input voltage
- f_{SW} is the desired nominal switching frequency of the converter as set by R_{FREQ} resistor

Note that for proper operation, V_{IN} of the controller must be connected to the system bus voltage, as it is sensed internally to maintain the frequency and on-time generation. The on-time can also be adjusted by the current sharing circuitry in order to maintain the balance between currents in the different phases of the converter as detailed in [Section 7.3.1.8](#).

7.3.1.3 Switching Frequency

The user can program the desired nominal frequency of the controller during steady-state operation using the R_{FREQ} resistor from $FREQ$ to GND . This set frequency corresponds to the switching frequency of each phase

of the converter, and the effective switching frequency in dual-phase operation as seen by the output capacitors of the buck converter is $2\times$ this programmed value. Note that the actual frequency of the converter during steady-state has slight variations based on the input voltage, output voltage, and load. The frequency also changes during load transients as detailed in [Section 7.3.1.1](#). The equation for selecting R_{FREQ} is shown in [Equation 2](#):

$$R_{FREQ} = \frac{20000}{f_{SW}} \quad (2)$$

where:

- R_{FREQ} is the frequency setting resistor value in $k\Omega$
- f_{SW} is the desired nominal switching frequency in kHz

The following table shows standard resistors used for R_{FREQ} and the controller output frequency to which these correspond.

Table 7-1. Switching Frequency Resistor Selection

R_{FREQ} RESISTOR VALUE ($k\Omega$)	NOMINAL SWITCHING FREQUENCY (kHz)
100	200
40.2	500
24.9	800

Use resistors with 1% tolerance or less for R_{FREQ} selection.

7.3.1.4 Droop Regulation

The TPS7H5101 allows for the user to set droop regulation for the buck converter in which the output voltage setpoint varies based on the load current of the power converter. The output voltage setpoint is lowered as the load current increases, and reduced as the load current decreases. With this feature, the tight AC tolerance specifications that are typical of core voltages of FPGAs and ASICs are more easily met by allowing for more margin between the setpoint and the accuracy limits when load transients occur. Furthermore, the droop regulation also allows for a reduction of output capacitance needed on the converter output.

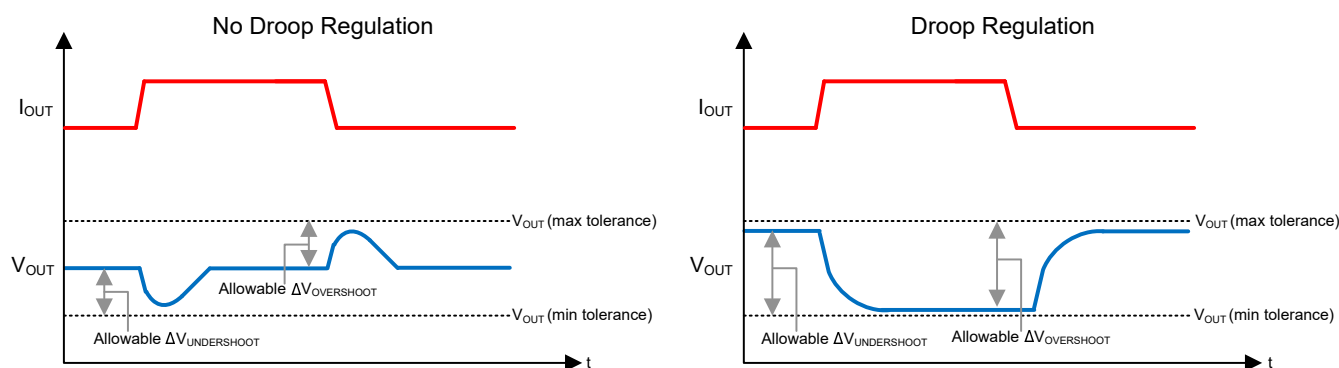


Figure 7-4. Output Voltage Transient Comparison With and Without Droop

The amount of droop that is implemented is dependent on the load-line characteristic R_{LL} that is selected for the converter. The droop can be determined by the following equations:

$$V_{DROOP} = R_{LL} \times I_{OUT} = \frac{R_{CS(eff)} \times A_{CS} \times I_{OUT}}{A_{DROOP}} \quad (3)$$

where:

- R_{LL} is the load line characteristic (as shown in [Figure 7-5](#))
- $R_{CS(eff)}$ is the effective current sense resistance

- A_{CS} is the current sense gain
- I_{OUT} is the load current
- A_{DROOP} is the droop gain

Note that the internal current sense of the TPS7H5101 has a gain of 1, so A_{CS} in Equation 3 can typically be set to 1 for this equation. However, if any external current sense circuitry is used, the gain of that circuit needs to be accounted for with A_{CS} . The parameter $R_{CS(eff)}$ needs to be equal to the current sense resistor or inductor DCR if either of these is used as the primary current sensing input to the controller. When using the TPS7H5101 with the TPS7H6200, value of the $R_{CS(eff)}$ becomes 5mV/A. The droop gain is determined by Equation 4:

$$A_{DROOP} = 1 + \left(\frac{R_{DROOP}}{R_{COMP}} \right) \quad (4)$$

where:

- R_{DROOP} is the resistor connected between the DROOP and COMP pins
- R_{COMP} is the resistor connected between the COMP and VREF pins

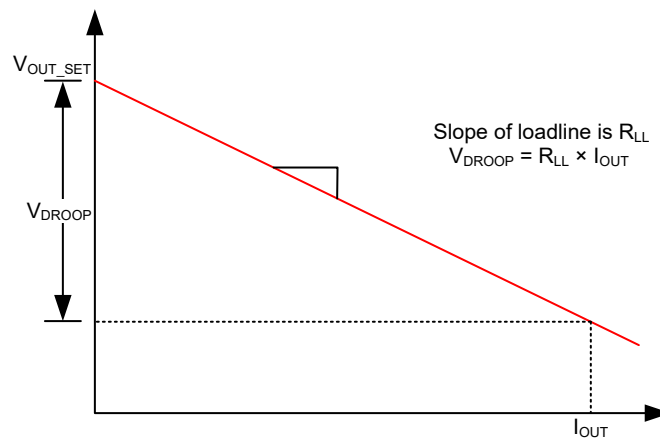


Figure 7-5. Load-Line Regulation

7.3.1.5 Ramp Compensation

If noise is coupled into either the ISUM or VDROOP waveforms, the noise can cause the on-time pulses of the controller to be generated at unexpected times. The result is jitter in the power converter that produces non-idealities in the switching behavior. The noise immunity of these waveforms can be improved by introducing ramp compensation, which in turn helps to reduce the jitter of the power converter.

The TPS7H5101 has three selectable amplitudes that can be chosen for the ramp compensation as shown in Ramp Compensation Configuration. Note that the ramp compensation scales with the selected nominal switching frequency, such that the target amplitude is always reached at the end of the switching cycle. Select the amplitude of the ramp compensation based on the application to best minimize the jitter. The added ramp compensation has the effect of slight reduction of the loop bandwidth, and as such, the ramp height needs to be carefully selected. A higher amplitude more effectively reduces the jitter, but also can worsen the transient response.

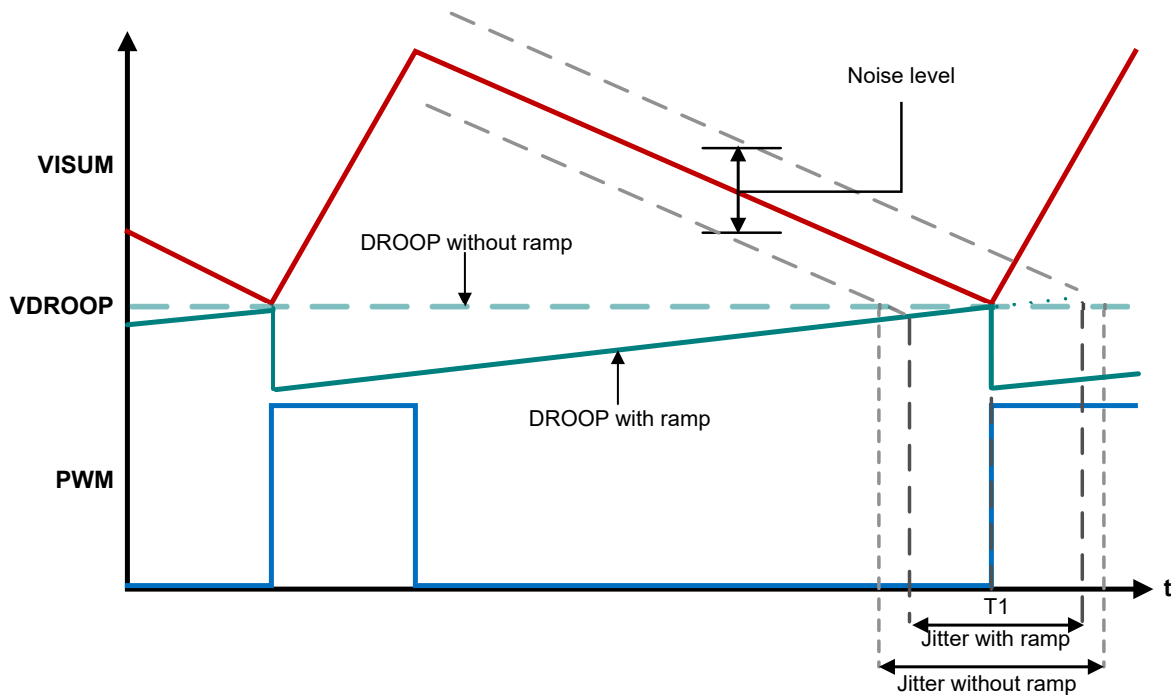


Figure 7-6. Comparison of Ramp Compensation Impact on Operation

Table 7-2. Ramp Compensation Configuration

RAMP PIN CONNECTION	RAMP COMPENSATION AMPLITUDE (mV)
GND	20
Open (floating)	60
VLDO	100

7.3.1.6 Undershoot Reduction (USR)

During a transient load release, the energy in the inductors must be quickly increased to meet the load demand. The undershoot reduction (USR) feature allows for doing this with the TPS7H5101 controller. When the difference between DROOP and ISUM exceeds the desired threshold, then the increase in energy that is needed is supplied by allowing pulse overlapping between the two phases of the controller. As mentioned in [Section 7.3.1](#), during normal operation the phase manager disallows the two outputs from generating on-pulses simultaneously and maintains an 180° displacement between the signals. However, the pulse overlapping during USR allows for more frequent pulse generation which provides the increase in inductor energy needed to meet the load demand and to reduce the undershoot of the output voltage. USR also provides the added benefit of reducing the amount of output capacitance that is needed at the converter output. After the transient is completed, the device resumes operating at the steady-state frequency with the proper phase displacement between PWM1 and PWM2 outputs.

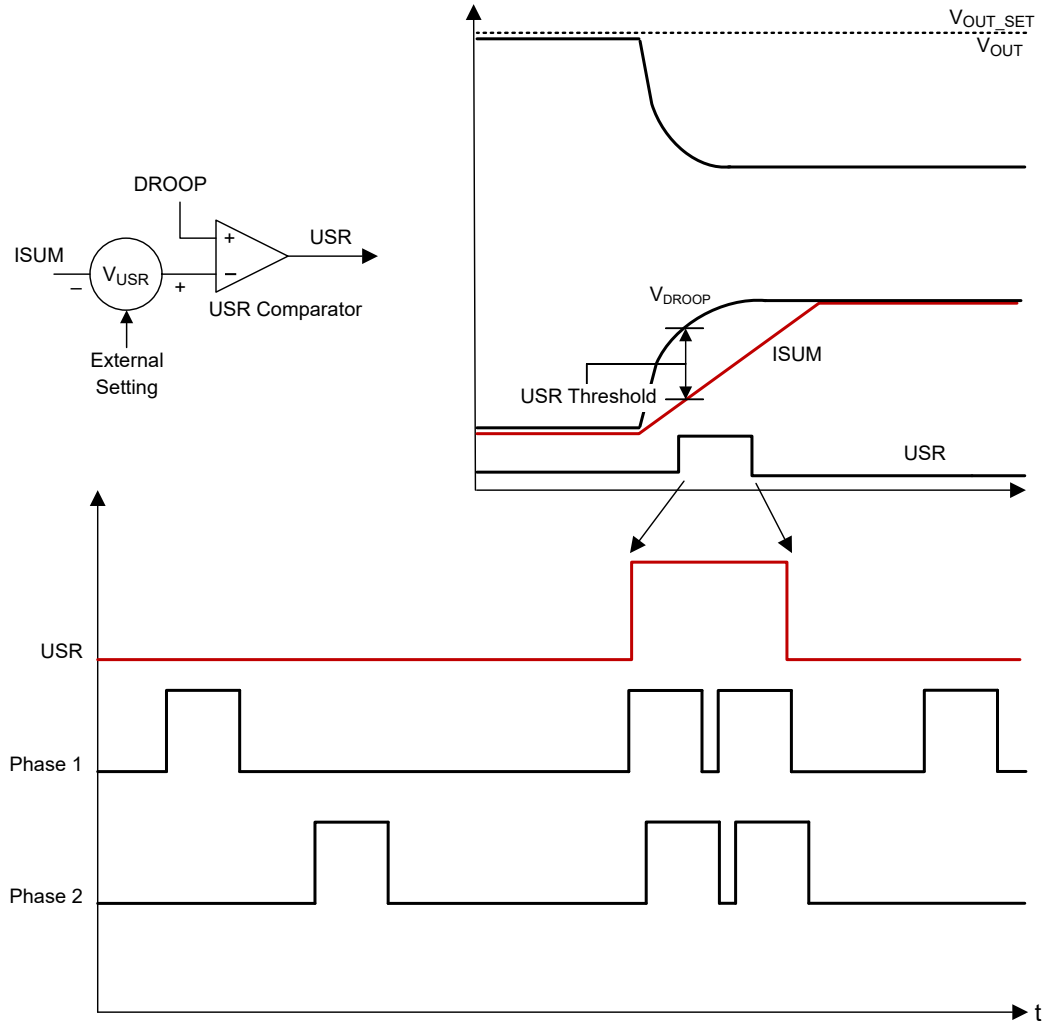


Figure 7-7. Undershoot Reduction

A resistor from the USR pin to GND is used to program the threshold DROOP – ISUM at which undershoot reduction is activated. The USR feature can also be disabled by placing a resistance larger than 2MΩ from USR to GND. If desired, the pin can also be left floating to disable the feature. The equation for selecting R_{USR} is shown in Equation 5.

$$R_{USR} = 18963 \times V_{TH_USR}^{-1.043} \quad (5)$$

where:

- R_{USR} is the resistor between USR and GND in kΩ
- V_{TH_USR} is the desired threshold of DROOP – ISUM at which the undershoot reduction is activated in mV

Undershoot reduction is disabled during the soft-start period of the controller. Furthermore, undershoot reduction is only valid when the controller has both outputs (PWM1 and PWM2) activated and there is no USR functionality if PWM2 is disabled.

7.3.1.7 Overshoot Reduction (OSR)

Since point-of-load synchronous buck converters typically have a low output voltage, responding to overshoot due to a transient load release is a challenge. The TPS7H5101 offers an overshoot reduction (OSR) feature to help minimize the output voltage overshoot during a load release. With the OSR enabled, the low-side gate driver is turned off when the DROOP voltage falls below the ISUM voltage by a predefined threshold. For the TPS7H5101, the outputs are at the tri-state level during this period (See [Section 7.3.2](#) for more details). With the low-side FET off, the energy in the inductor is partially dissipated by the body diode (or through the third quadrant operation for GaN devices). As the overshoot is reduced, the controller resumes normal operation and the low side FET is allowed to turn on again.

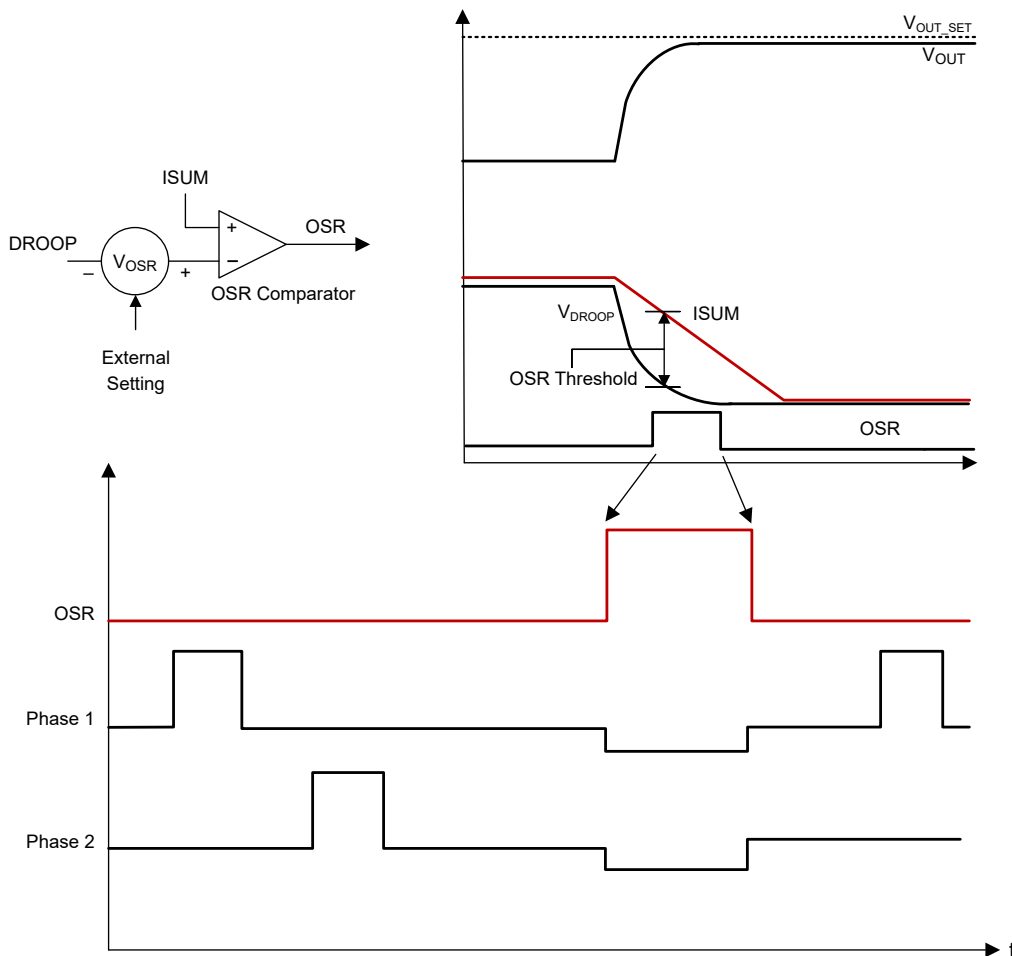


Figure 7-8. Overshoot Reduction

A resistor from the OSR pin to GND is used to program the threshold $ISUM - DROOP$ at which OSR is activated. The OSR feature can also be disabled by placing a resistance larger than $2M\Omega$ from OSR to GND. If desired, the pin can also be left floating to disable OSR. The equation for selecting R_{OSR} is shown in [Equation 6](#).

$$R_{OSR} = 18963 \times V_{TH_OSR}^{-1.043} \quad (6)$$

where:

- R_{OSR} is the resistor between OSR and GND in $k\Omega$
- V_{TH_OSR} is the desired threshold $ISUM - DROOP$ at which the overshoot reduction is activated in mV

7.3.1.8 Current Sensing and Current Sharing

For proper control, the D-CAP+ architecture used by the TPS7H5101 compares ISUM to VDROOP. The ISUM waveform is a summation of the current sense signals that are differentially input to the controller on CSx_P and CSx_N. For dual phase operation, the current is sensed on each phase (CS1_P and CS1_N for the first phase, CS2_P and CS2_N for the second phase). Note that the TPS7H5101 control must detect the valley inductor current of each phase for proper operation, so a sensed current representation of the low-side FET of each phase is required. Thus, the TPS7H5101 can be used either with power stages that implement low-side sensing (such as the TPS7H6200), or by sensing the inductor current directly via DCR or a series sense resistor. In either case, differentially route the current sense signals from the sense points to the CSx_P and CSx_N pins. In the event that only single phase operation is used for the controller, the CS2_P and CS2_N pins can be used to disable PWM2 by tying them to VLDO.

The TPS7H5101 also contains internal circuitry that works to equalize the current in each phase of a multiphase buck implementation. The average current from all phases is determined, and then the on-time of the respective phases can be adjusted to balance the currents. The on-time generating comparator starts a pulse when VDROOP intersects with ISUM. The C_TON capacitor is charged using a current proportional to the power stage input voltage VIN. The on-time pulse is terminated when the voltage at the capacitor matches the on-time reference, which is equal to VOUT_SET.

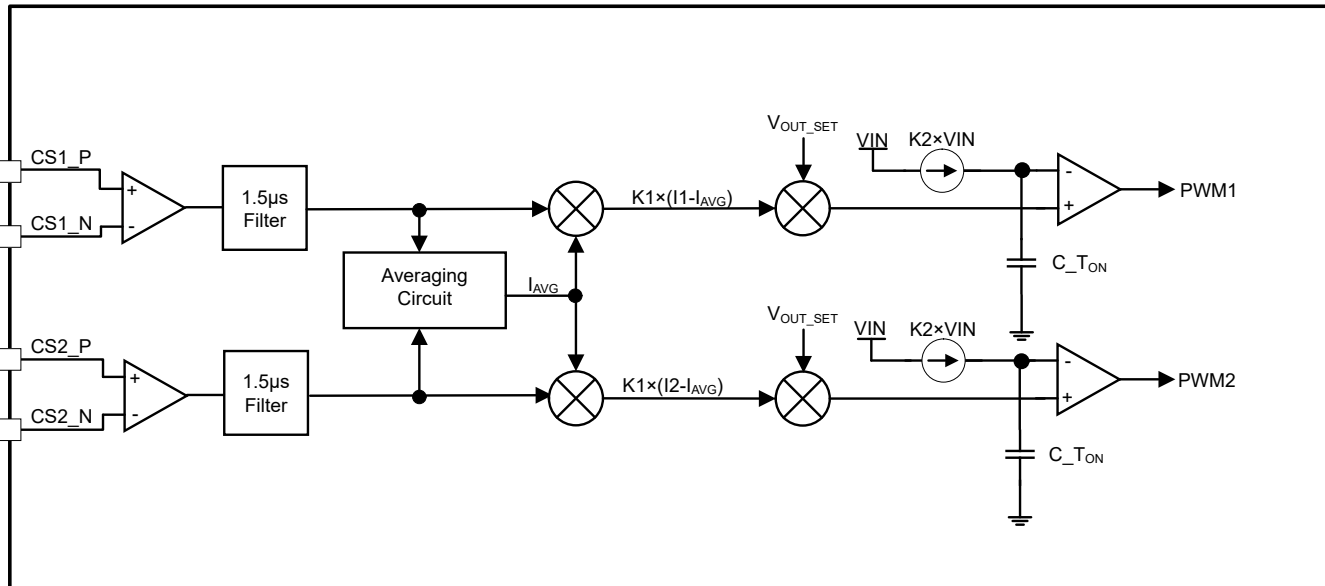


Figure 7-9. TPS7H5101 Current Sharing

The current sharing block diagram is shown in Figure 7-9. If the averaged value of the phase signals are equal, the on-time pulse is terminated at VOUT_SET, and the typical expected pulse width is delivered to the power stage via the controller. However, if $I1 > I_{AVG}$, then an offset is subtracted from the VOUT_SET reference, and the pulse width for the first phase is shortened which reduces the current in that phase. Likewise, if $I1 < I_{AVG}$, the pulse width is lengthened, increasing the current in the phase. The current sharing circuit is critical for maintaining reliable operation of the multiphase converter.

7.3.1.9 Blanking Time (BLANK)

During steady state operation with D-CAP+, the high-side FET is turned on for a set period of time based on the on-time pulse duration that is generated by the controller. During this period, the phase inductor current increases. After the conclusion of the on-time pulse, the high-side FET turns off and the low-side FET is turned on, which causes the phase inductor current to decrease. During this period (1) the control determines when the next on-time pulse is to be generated based on the intersection of ISUM and VDROOP and (2) if an overcurrent has been detected, then the low-side FET is to remain on until the inductor current has falling below a predefined threshold. As such, any ringing on the current waveform that is caused by the low-side turn-on or

the current sense circuitry potentially leads to erroneous operation. This unexpected operation entails triggering the on-pulse at the incorrect time or exiting the overcurrent mode early. The blanking time of the controller is used to mitigate this issue.

The blanking time defines a period during which the pulse generating comparator ignores the current sense input, with the goal of preventing errant triggers of the on-time pulse. The duration is selected to allow for any ringing to dampen. The blanking time is also used to account for the current sense settling time of the power stage, if used. The blanking time is also defined as the minimum off-time, since the blanking equates to the absolute shortest amount of time that the HS FET must remain off after the on-time pulse is terminated. Note that in addition to the blanking at the beginning of the low-side FET turn-on, the comparator also blanks during the entire on-time of the controller output. However, only the blanking during the low-side FET turn-on is programmable. Programmable Blanking Time Example shows the programmable blanking time relative to the PWM pulse and current sense signal for a single phase of the multiphase buck. Note that in this example the current sense signal provided is a representation of the low-side FET current as generated by a power stage in the buck converter. The blanking time accounts for any noise on the current sense signal as well as the propagation delay of the external power stage.

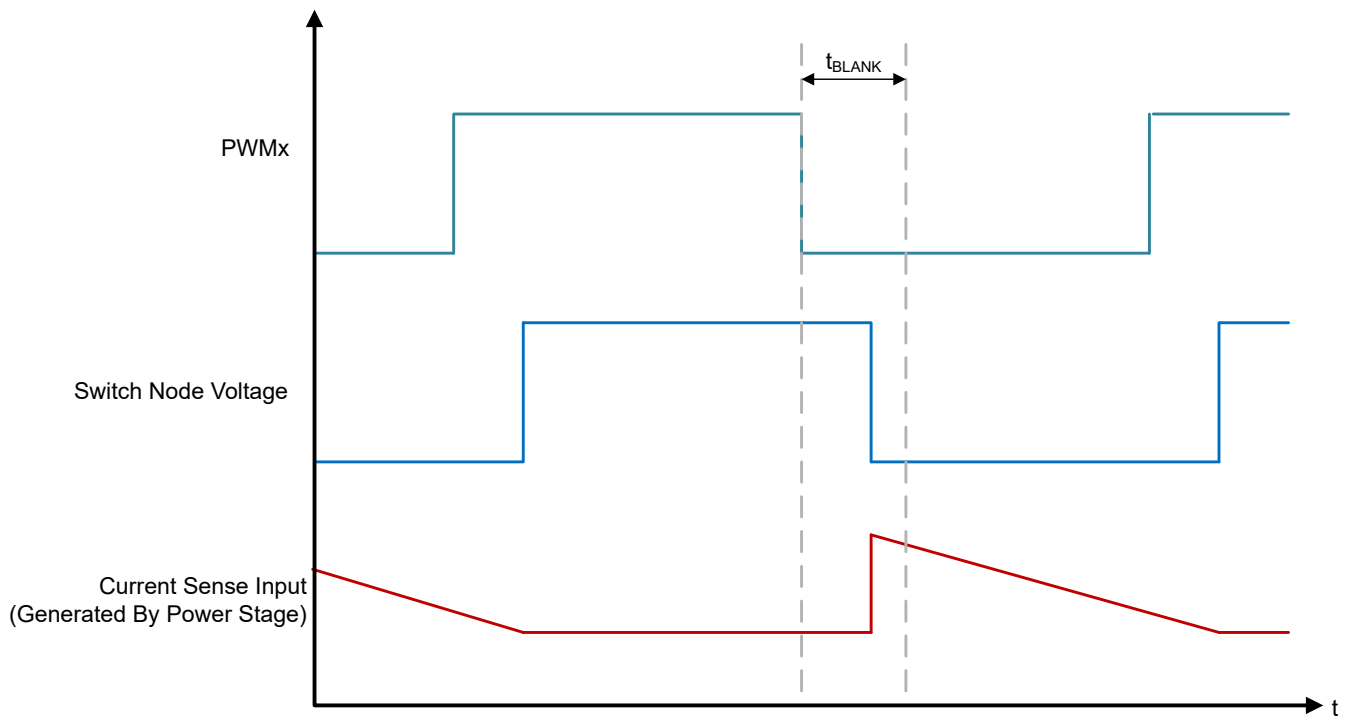


Figure 7-10. Programmable Blanking Time Example

The blanking time at the beginning of the low-side turn-on period of the TPS7H5101 can be set using an external resistor R_{BLANK} from the BLANK pin to GND. Equation 7 can be used to select the resistor based on the desired blanking time.

$$R_{BLANK} = (1.3493 \times t_{BLANK}) - 60.386 \quad (7)$$

where:

- R_{BLANK} is the blanking resistor value in k Ω
- t_{BLANK} is the desired blanking time in ns

7.3.2 PWM Signals

PWM1 and PWM2 pins output the on-time signals to the power stage of the buck converter. The outputs of the controller are 5V logic signals that can be utilized with DrMOS compatible power stages. Each of these output signals is meant to drive a single power stage. The output signals have three distinct states: logic high, logic low, and a tri-state voltage (typically 1.7V). [Table 7-3](#) below describes the expected behavior of the driver or logic stage that corresponds to each PWMx controller output state:

Table 7-3. PWMx Output States

LOGIC LEVEL	POWER STAGE RESPONSE
High	High-side FET is ON and low-side FET is OFF
Low	High-side FET is OFF and low-side FET is ON
Tri-state (mid-level)	Both FETs are OFF

When the controller is disabled, the outputs are in tri-state. Thus, as discussed in [Section 7.3.9.1](#), the first transition during soft-start is from the tri-state to logic high each time the controller is enabled.

PWM2 can be disabled if only single phase operation is required for the controller. To disable the second controller output, CS2_N needs to be connected to VLDO. CS2_P can also be connected to VLDO in this state.

7.3.3 Remote Sensing and Setting VOUT

The TPS7H5101 has the capability for differential remote sensing. However, while the VSNS_P pin serves as the voltage feedback input as referenced to the load, there is no direct pin connection for VSNS_N. Instead, the OUT_SET resistor used to program the output voltage is referenced to VSNS_N, which is the reference point for the load of the buck converter. As such, both VSNS_P and OUT_SET are referenced to this point at the input of the difference amplifier inside the controller.

The remote sensing architecture of the controller is capable of sensing offsets of up to $\pm 100\text{mV}$ between the local GND and remote ground. Optimize the PCB layout such that the ground differentials at the load and controller never exceed this value. Also, differentially route the traces for VSNS_P and VSNS_N from the load to the controller. If remote sensing is not desired to be used, then connect the OUT_SET resistor to the same GND that is utilized by the controller.

A remote sense connection example is shown in [Figure 7-11](#), using a simplified diagram of the TPS7H5101. In this example $R_{\text{PARASITIC}}$ represents the parasitic resistance in the high current path supplying the input voltage for the load. The parasitic resistance is compensated for using the remote sense connection from the load to VSNS_P. $R_{\text{PARASTIC_GND}}$ is the parasitic resistance in the ground path, which is accounted for using the VSNS_N connection to the OUT_SET resistor. Some FPGAs have dedicated remote sense connections, in which case the connections can be made as shown in [Figure 7-12](#). Note that since the remote sense is used to overcome the voltage drop due to parasitic resistances on the printed circuit board as well as the package of the high-current load, the output voltage as measured close to the converter is higher than that at the remote load, which is the actual voltage regulation point.

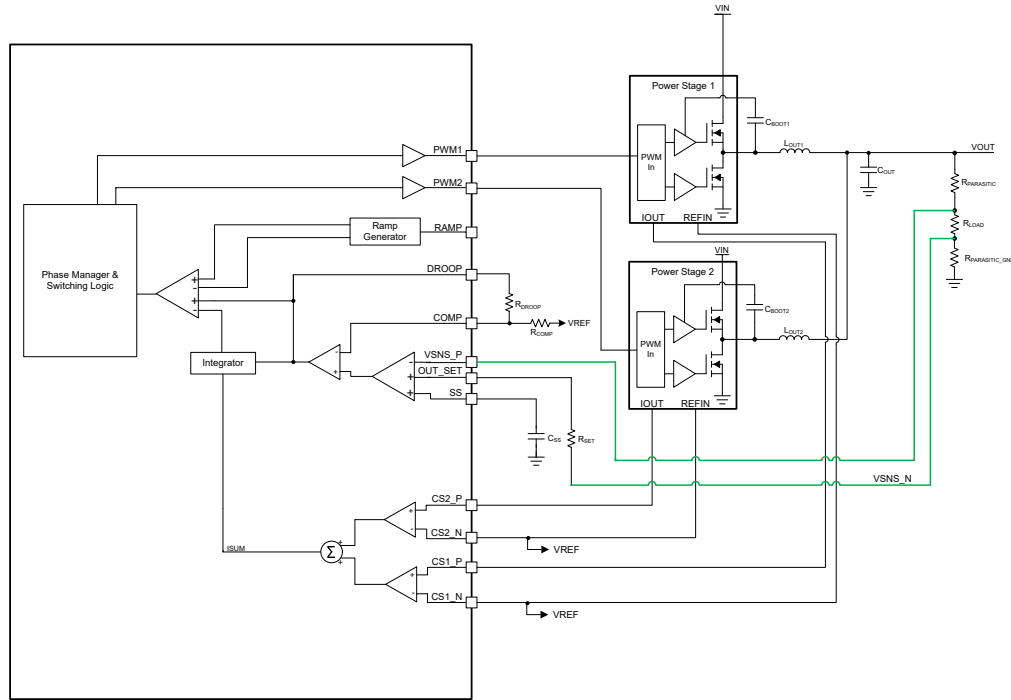


Figure 7-11. Remote Sense Example

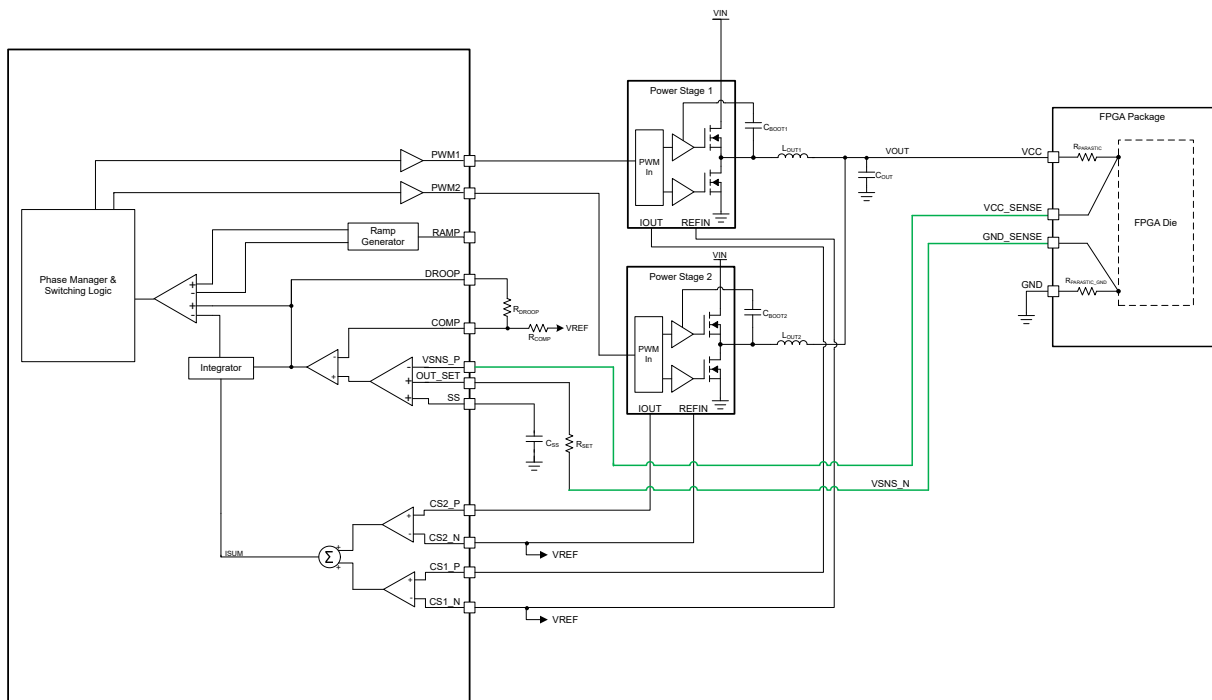


Figure 7-12. FPGA Remote Sense Example

The output voltage of the buck converter utilizing the TPS7H5101 can be set from the nominal range of 0.5V to 2.5V. The output voltage is programmed using the OUT_SET pin of the device. A resistor from OUT_SET to VSNS_N sets the nominal output voltage value. VSNS_N is the remote load reference point, utilized when the controller is configured for differential remote sensing. Equation 9 and Equation 9 can be used to select the resistor for programming the desired output voltage. First set the OUT_SET output current to approximately 10.05µA using the resistor from IREF to GND. Note the IREF current is mirrored on OUT_SET.

$$R_{IREF} = \frac{V_{VREF}}{I_{IREF}} = \frac{1.7V}{10.05\mu A} = 169.2k\Omega \quad (8)$$

Thus, set R_{IREF} to the closest standard resistor value of 169k Ω . With R_{IREF} set to provide 10.05 μ A on the OUT_SET pin, the R_{SET} value can be chosen for the desired output voltage V_{OUT_SET} :

$$R_{SET} = \frac{V_{OUT_SET}}{I_{IREF}} = \frac{V_{OUT_SET}}{10.05\mu A} \quad (9)$$

The converter output voltage V_{OUT} corresponds directly to the V_{OUT_SET} voltage. It is recommended to use 0.1% tolerance resistors for both R_{SET} and R_{IREF} .

7.3.4 Input Voltage (VIN)

The current revision of TPS7H5101 has an input voltage range of 8V to 15V on the VIN pin. The VIN range of the future revision is 4.5V to 15V. VIN provides the voltage needed for the internal control circuitry and logic of the controller. The VIN pin has undervoltage lockout, and the voltage must be above the UVLO rising threshold before the device can be enabled and starts intended operation.

For proper on-time generation and maintaining a pseudo-constant switching frequency during normal operation, connect VIN of the controller to the buck power stage input voltage. As detailed in [Section 7.3.1.2](#) and [Section 7.3.1.8](#), both the on-time and current sharing circuitry require the input voltage from the converter power stage to operate as intended.

Connect a minimum bypass capacitor of at least 1 μ F from VIN to GND in close proximity to the controller.

7.3.5 VLDO

The voltage applied at VIN serves as the input for the internal regulator that generates the VLDO voltage. The VLDO nominal output voltage is 5V. There is also a undervoltage lockout feature on VLDO, which prevents the device from being enabled if the output voltage is too low. A 1 μ F capacitor is recommended from VLDO to GND. Do not externally load VLDO except where deemed acceptable within this document.

7.3.6 Voltage Reference (VREF)

The device generates an internal nominal 1.7V bandgap reference voltage. This voltage is the output of the VREF pin. A 470nF capacitor to ground is required at VREF pin for proper electrical operation as well as to enable robust single event transient (SET) performance of the device.

VREF can also serve as the reference for the current sense inputs when pairing the TPS7H5101 with a power stage such as the TPS7H6200, where VREF is connected to CSx_N. The resistor R_{COMP} (used to set the droop gain) and R_{OCL} (used to set the overcurrent threshold) are also referenced to the VREF pin of the controller.

7.3.7 Enable (EN)

When the voltage at the enable pin is below the enable rising threshold, the device is in shutdown mode and the controller does not produce any output pulses. The device is enabled by bringing the voltage at the pin above this threshold, and after being enabled, the device can be disabled by reducing the voltage below the enable falling threshold. There are several ways in which the device can be enabled externally. A resistor divider from VIN to GND can be used to supply the EN voltage.

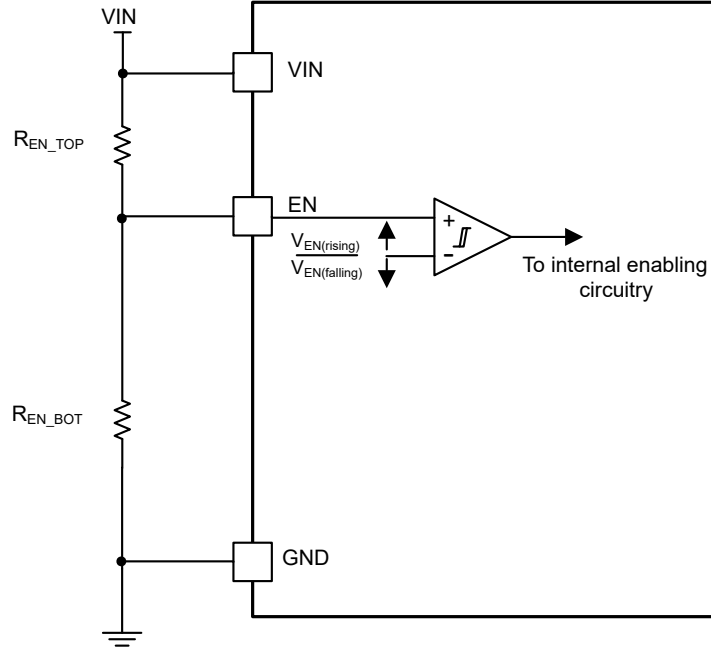


Figure 7-13. Enable Pin Configuration Using Resistor Divider

The resistors can be appropriately sized to turn on the device at the desired input voltage, as shown in [Equation 10](#). This implementation creates an adjustable UVLO that complements the default internal UVLO thresholds on VIN.

$$R_{EN_BOT} = \frac{V_{EN(rising)}}{V_{IN(rising)} - V_{EN(rising)}} \times R_{EN_TOP} \quad (10)$$

where

- $V_{IN(rising)}$ is the input voltage value that causes EN to go high
- $V_{EN(rising)}$ is the rising voltage threshold of the EN pin
- R_{EN_TOP} is the feedback resistor from VIN to EN
- R_{EN_BOT} is the feedback resistor from EN to GND

Likewise, [Equation 11](#) can be used to calculate the $V_{IN(falling)}$ voltage.

$$V_{IN(falling)} = V_{EN(falling)} \times \frac{R_{EN_TOP} + R_{EN_BOT}}{R_{EN_BOT}} \quad (11)$$

where

- $V_{IN(falling)}$ is the input voltage value that causes EN to go low
- $V_{EN(falling)}$ is the falling voltage threshold of the EN pin

Alternatively, the EN pin can be driven directly from a microcontroller or FPGA. The low voltage threshold of the enable pin supports logic levels as low as 1.1V.

As discussed in [Section 7.5](#), the TPS7H5101 can also be enabled and disabled through the PMBus interface. As such, there can be a condition where EN is externally above the necessary threshold for turn-on, but the device remains disabled based on the commanded state via PMBus. The default state for the PMBus enable is “on”, and as such at startup when then the EN pin is driven high the device is enabled without any initial PMBus command.

7.3.8 Power Good (PG)

The power good (PG) pin is an open-drain output that is pulled up through a resistor to a voltage level of 7V or lower. Select the pull-up resistor value to keep the current sunk by PG under 2mA. For most conditions, a 10kΩ resistor is sufficient. Using a larger value minimizes power dissipation, but can allow switching noise to couple into the power good signal as a result of the weaker pull-up capability.

The power good is asserted when VOUT is greater than or equal to 90% (typ) of the programmed value as determined by OUT_SET. If VOUT falls below 88% (typ) of the programmed value, then power good is deasserted. A comparison is made between the sensed feedback voltage VSENSE and OUT_SET, where:

$$VSENSE = VSNS_P - VSNS_N \quad (12)$$

As discussed in [Section 7.3.3](#), VSNS_N is the ground as referenced to the load. VSNS_N also serves as the reference point for OUT_SET when remote sensing is used for the controller. Note that because PG is referenced to local GND, there can be some inaccuracy introduced in the PG assertion points with increased load current. If remote sensing is not desired, then OUT_SET can be referenced to the local ground for the best PG performance.

For the PG state to be considered valid, the input voltage VIN of the controller must be greater than 1V. The full current sinking capability of the PG pin is realized when VIN reaches 7V. Refer to the Electrical Characteristics for additional details.

In addition to an undervoltage on VOUT, the list of conditions that cause PG to be deasserted are:

- VIN goes into UVLO
- The device enters thermal shutdown
- The device is disabled by the EN pin

[Figure 7-14](#) shows the expected power good behavior in response to VOUT conditions.

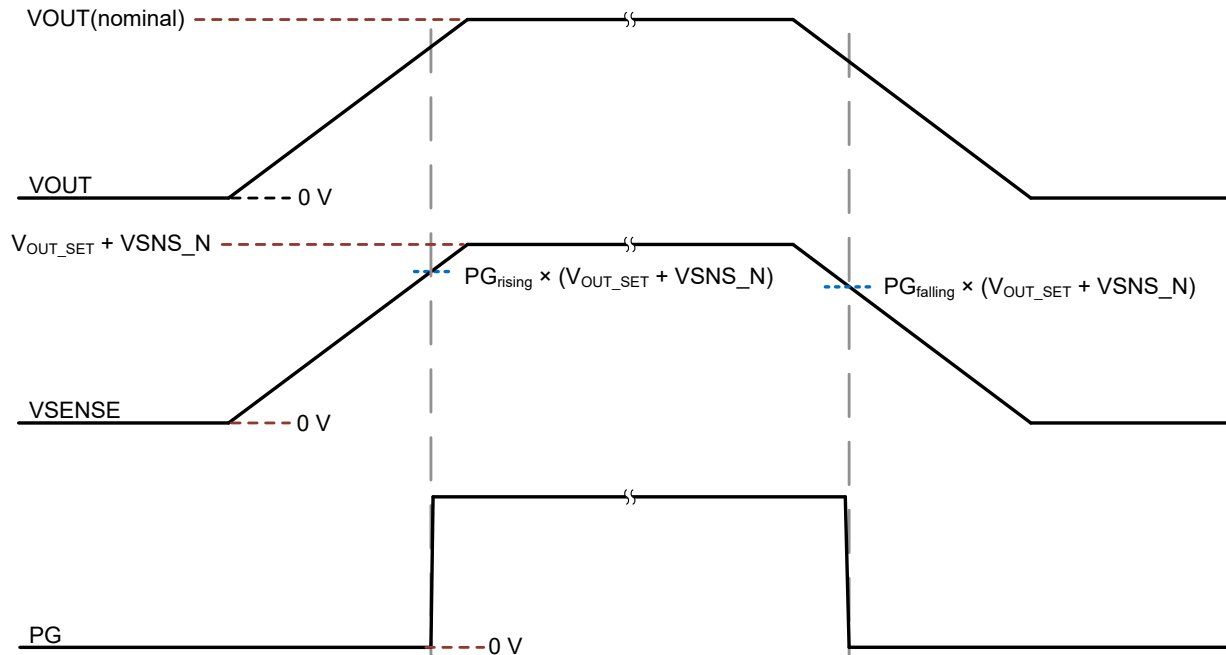


Figure 7-14. Power Good Thresholds

7.3.9 Turn-On Behavior

7.3.9.1 Soft-Start (SS)

A capacitor from the soft-start pin (SS) to GND is used to allow for a controlled rise of the output voltage. This is particularly helpful to prevent excessive inrush current in the converter is caused due to the large output capacitance. The capacitance for the desired soft-start time can be selected as shown in [Equation 13](#):

$$C_{SS} = \frac{t_{SS} \times I_{SS}}{V_{OUT_SET}} \quad (13)$$

where:

- t_{SS} is the desired soft-start time
- V_{OUT_SET} is the output voltage setpoint determined using R_{SET}
- I_{SS} is the soft-start charging current

During soft-start, the controller uses the voltage on the SS pin as the reference until the SS pin voltage exceeds V_{OUT_SET} . After the SS pin voltage is greater than V_{OUT_SET} , the soft-start period is considered complete. To support pre-biased outputs during startup, the TPS7H5101 always sends a pulse to the high-side FET first. As such, it is critical that high-side gate drive circuitry that is used in conjunction with the controller has sufficient voltage before initiating soft-start with the controller.

7.3.10 Current Monitor Output (ISUM)

The current sense signals at CSx_P and CSx_N are summed together internally at ISUM and used by the controller to properly generate the on-time pulses, as described in [Section 7.3.1](#). The signal ISUM is also buffered and output on the ISUM pin to be used as a current monitor. The voltage at ISUM is proportional to the sensed current and also a 1:1 representation of the internal ISUM signal. This analog signal can be used for diagnostics or for other user defined purposes. The ISUM output is capable of driving a capacitive load up to 50pF which is adequate for most modern ADC inputs. The voltage output on the ISUM pin is with respect to VREF.

7.3.11 Overcurrent Protection

The TPS7H5101 uses valley current limiting. Current limiting occurs on a phase-by-phase basis, meaning that if an excessive current is detected on either phase, the controller enters overcurrent protection mode. Likewise, the current limiting occurs on a pulse-by-pulse basis depending on the sensed current value. If the voltage between the CSx_P and CSx_N inputs is above the overcurrent threshold, the controller delays the next on-time pulse until that voltage difference falls below the threshold. During this delay time, the high-side FET is off and the low-side FET is on for the buck converter.

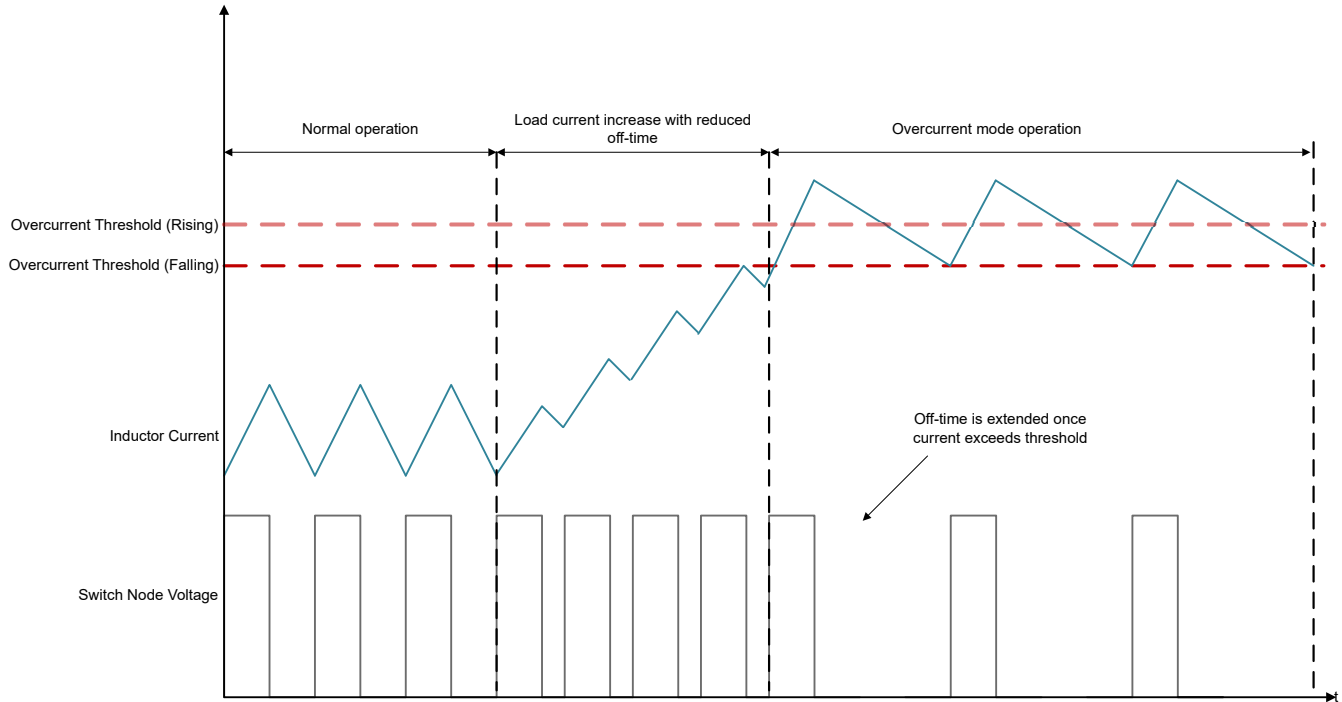


Figure 7-15. Valley Current Limiting Example

The valley current for the buck converter is the load current minus half of the inductor current ripple. The overcurrent threshold, taking into account both any current sense resistor and current sense gain, is based on the calculated valley current for the required overcurrent protection level:

$$V_{CS_OCL} = I_{VALLEY} \times R_{CS(eff)} \times A_{CS} \quad (14)$$

where:

- V_{CS_OCL} is the desired overcurrent threshold voltage as seen by the controller at the CS pins
- I_{VALLEY} is the desired inductor valley current above which the controller is overcurrent
- $R_{CS(eff)}$ is the effective current sense resistance used for sensing the inductor current
- A_{CS} is the current sense gain from the current sensing circuitry, either from the power stage or external to the controller

Using a resistor R_{OCL} from the OCL pin to VREF, set the overcurrent threshold by setting V_{OCL} to equal the intended target as calculated in [Equation 14](#):

$$V_{OCL} = I_{OCL} \times R_{OCL} \approx 5\mu A \times R_{OCL} \quad (15)$$

7.4 Device Functional Modes

The device uses an adaptive on-time with a pseudo-constant frequency current-mode control architecture. As a synchronous buck converter, the device operates in continuous current mode under all load conditions.

7.5 Programming

7.5.1 PMBus General Description

The TPS7H5101 has a simple PMBus interface designed to allow margining the output voltage +10% to -10% and enabling and disabling the device. Additionally, PEC (packet error checking) is included along with fault handling to aid in robust communication.

This PMBus interface supports the following command protocols: Send Byte, Write Byte, and Read Byte. Each of the protocols has a standard version and PEC version to allow for flexibility.

All PMBus transactions utilize the START and STOP commands to frame the data packet and the REPEAT START condition is allowed when necessary. The device can operate in standard mode (100kb/s). The TPS7H5101 device does not stretch pulses on the PMBus when communicating with the controller.

The PMBus is active and ready for transactions a period of 5ms after the input voltage VIN of the TPS7H5101 is above the VIN_{UVLO} threshold of the controller. Sending transactions before this initialization period is completed is not advised as any PMBus actions are potentially perceived as invalid. All registers are reset to default values during initialization. Note that the "ON_OFF" bit of the OPERATION register defaults to the "on" state after the PMBus initialization, regardless of the state of the external enable pin for the controller.

7.5.2 Write Byte

The write format is utilized to send a command code and a byte of data to the target. After the start condition [S], the target chip address is sent, followed by an eighth bit indicating a write. The TPS7H5101 then acknowledges that it is being addressed, and the controller responds with an 8-bit register address byte. The target acknowledges and the controller sends the appropriate 8-bit data byte. Again the target acknowledges and the controller terminates the transfer with the stop condition [P].

7.5.3 Read Byte

After the start condition [S], the target chip address is sent, followed by an eighth bit indicating a write. The TPS7H5101 then acknowledges that it is being addressed, and the controller responds with an 8-bit register address byte. The target acknowledges and the controller sends the repeated start condition [Sr]. Again the target chip address is sent, followed by an eighth bit indicating a read. The target responds with an acknowledge followed by previously addressed 8 bit data byte. The controller then sends a non-acknowledge (NACK) and finally terminates the transfer with the stop condition [P].

7.5.4 Send Byte

The send byte format is utilized to send a single byte of data to the target that contains within it an encoded command. After the start condition [S], the target chip address is sent, followed by an eighth bit indicating a write. The TPS7H5101 then acknowledges that it is being addressed, and the controller responds with an 8-bit data byte. The target acknowledges the controller terminates the transfer with the stop condition [P].

7.5.5 Packet Error Checking (PEC)

Packet Error Checking (PEC) can optionally be utilized to provide error checking on data transmissions. If the TPS7H5101 receiver receives data from the controller that does not match the calculated PEC, the TPS7H5101 performs a NACK the of the PEC byte. Additionally, the command is not acted upon and the CML bit is set in the STATUS_BYTE register.

If the controller provided clock pulses are provided before a STOP, PEC is used. If the STOP is issued without extra clock pulses, PEC is not used. Though the PEC is optional, utilization of this feature is recommended for robust and reliable data transmissions.

7.5.6 Additional Faults

Errors in the PMBus transmission can lead to a fault that is recognized by the TPS7H5101 controller. These faults, which cause the CML bit to be set in the STATUS_BYTE register, include:

- Transmitting or reading too many bits
- Transmitting or reading too few bits
- Too many bytes sent by the TPS7H5101 controller
- Too many bytes read by the TPS7H5101 controller
- An invalid or unsupported PMBus command is sent from the host to the TPS7H5101
- A detect clock low timeout has been initiated by the TPS7H5101 due to another PMBus device holding the SCL line low for a period longer than 32ms (typ).
- A packet error checking (PEC) fail

The CML bit remains set until one of the conditions as described in STATUS_BYTE is met for clearing the register.

7.5.7 PMBus Command Overview

COMMAND	DESCRIPTION	WRITING DATA TYPE	READING DATA TYPE
OPERATION [01h]	Turn controller on and off	Write Byte	Read Byte
CLEAR_FAULTS [03h]	Clear all latched faults	Send Byte	N/A
STATUS_BYTE [78h]	Return status bits	None	Read Byte
MFR_SPECIFIC_C4 [C4h]	Set output voltage margining	Write Byte	Read Byte

7.5.8 PMBus Address Selection

TPS7H5101 allows up to 12 different chip addresses for PMBus communication, with the first three bits fixed as 001. The address selection is defined by the resistor R_{ADDR} from the ADDR pin to GND. The table below lists the target resistor values for each address. Resistors with a 0.1% tolerance or better are recommended for better noise margin and more reliable address detection. The resistor R_{ADDR} needs to be populated for the TPS7H5101 controller.

Table 7-4. Resistor Selection for PMBus Addresses

PMBUS ADDRESS	R_{ADDR} VALUE
0010000	1500k Ω
0010001	626k Ω
0010010	348k Ω
0010011	246k Ω
0010100	189k Ω
0010101	154k Ω
0010110	130k Ω
0010111	113k Ω
0011000	94.1k Ω
0011010	76.8k Ω
0011100	64.9k Ω
0011110	49.9k Ω

8 Register Map

1 OPERATION [01h] (Read/Write byte)

The TPS7H5101 supports only the functions of the OPERATION command shown below.

COMMAND	DEFINITION	DESCRIPTON
OPERATION<7>	ON_OFF	0: turn-off the controller 1: turn-on the controller (default)
OPERATION<6>	–	not supported and don't care
OPERATION<5:4>	–	not supported and don't care
OPERATION<3:2>	–	not supported and don't care
OPERATION<1>	–	not supported and don't care
OPERATION<0>	–	not supported and don't care

Note that the state of the "ON_OFF" bit is "on" by default when the VIN and internal VREF undervoltage lockout thresholds of the TPS7H5101 controller are surpassed.

2 CLEAR_FAULTS [03h] (Send byte)

The CLEAR_FAULTS command is used to clear any fault bits in the STATUS_BYTE register that have been set. This command clears all bits in all status registers. If the fault condition is still present when the bit is cleared, the fault bits immediately set again.

The CLEAR_FAULTS does not cause a unit that has latched off for a fault condition to restart. Units that have been shut down for a fault condition can be restarted with one of the following conditions.

- The output is commanded through the EN pin and/or ON_OFF bit to turn off and then to turn back on.
- VIN power is cycled for the TPS7H5101

If an extended period of time has elapsed since the last PMBus transaction, a CLEAR_FAULTS command needs to be sent prior to the next desired PMBus command. Sending this command clears the STATUS_BYTE register such that the CML bit state pertains only to the subsequent transaction. Sending a CLEAR_FAULTS command after a period of inactivity is also a safeguard against a potential heavy-ion induced bit change.

3 STATUS_BYTE [78h] (Read byte)

The TPS7H5101 does not support all functions of the STATUS_BYTE command. A list of supported functions appears below. A status bit reflects the current state of the converter. Status bit becomes high when the specified condition has occurred and goes low when the specified condition has disappeared. A flag bit is a latched bit that becomes high when the specified condition has occurred and does not go back low when the specified condition has disappeared.

COMMAND	DEFINITION	DESCRIPTON
STATUS<7>	BUSY	Not supported and always 0
STATUS<6>	OFF	Not supported and always 0
STATUS<5>	VOUT_OV	Not supported and always 0
STATUS<4>	IOUT_OC	Not supported and always 0
STATUS<3>	VIN_UV	Not supported and always 0
STATUS<2>	TEMP	Not supported and always 0
STATUS<1>	CML	0: flag indicating no communication, memory, or logic fault has occurred 1: latched flag indicating a communication, memory, or logic fault
STATUS<0>	OTHER	Not supported and always 0

The latched flags of faults can be removed by one of the following conditions:

- The device receives a CLEAR_FAULTS command.
- The output is commanded through the EN pin or ON_OFF bit in the OPERATION command
- VIN power is cycled for the TPS7H5101

If the fault condition remains present when the bit is cleared, the fault bits are immediately set again. The TPS7H5101 does not have an ALERT pin to notify the host of fault conditions. Therefore, the best practice for monitoring the fault conditions from the host is to poll the STATUS_BYTE register when a fault is suspected.

4 MFR_SPECIFIC_C4 (VOUT_MARGIN) [C4h] (Read / Write byte)

This register allows adjustment of the output voltage in 0.67% steps with a total range of +10% and -10.67%.

COMMAND	DEFINITION	DESCRIPTON
VOUT_MARGIN<7:5>	–	Not supported and always 0
VOUT_MARGIN <4:0>	VMARGIN	11111: +10.00% 11110: +9.33% 11101: +8.67% 11100: +8.00% 11011: +7.33% 11010: +6.67% 11001: +6.00% 11000: +5.33% 10111: +4.67% 10110: +4.00% 10101: +3.33% 10100: +2.67% 10011: +2.00% 10010: +1.33% 10001: +0.67% 10000: 0.00% (default) 01111: –0.67% 01110: –1.33% 01101: –2.00% 01100: –2.67% 01011: –3.33% 01010: –4.00% 01001: –4.67% 01000: –5.33% 00111: –6.00% 00110: –6.67% 00101: –7.33% 00100: –8.00% 00011: –8.67% 00010: –9.33% 00001: –10.00% 00000: –10.67%

ADVANCE INFORMATION

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

The TPS7H5101 is a dual phase D-CAP+ buck controller. The TPS7H5101 controller is suitable for high current, point of load power delivery applications in satellites.

Figure 9-1. Typical Application Schematic

9.2.1 Design Requirements

Table 9-1. Design Parameters

DESIGN PARAMETER	DESIGN VALUE
Input voltage	12V ± 5%
Output voltage	0.8V ± 3%
Maximum output current	80A total, 40A per phase
Current sharing accuracy	±30% at full load
Transient response 35A load step at 120A/μs	ΔVOUT = 5%
Output voltage ripple	20mVpp
Nominal switching frequency	500kHz
Inductor	230nH (per phase)
Output capacitance	5mF
Start input voltage (rising VIN)	10V

9.2.2 Detailed Design Procedure

9.2.2.1 Inductor Selection

The key criteria for selecting an inductor value is the tradeoff between transient performance, inductor ripple, and efficiency. A smaller inductor value has better transient performance but higher ripple which contributes to lower overall converter efficiency. Choosing a larger inductor value yields lower ripple and higher efficiency, but hinders the transient response. A good initial target for inductor ripple is 20% to 40%. As such, the initial inductor ripple current can be calculated as follows:

$$I_{PP} = \frac{I_{OUT_MAX}}{n} \times K \quad (16)$$

where:

- I_{PP} is the peak-to-peak inductor ripple current
- I_{OUT_MAX} is the maximum load current
- n is the number of converter phases
- K is the desired ripple percentage, expressed as a decimal

The per-phase inductance can then be calculated as:

$$L = \frac{V_{IN_MAX} - V_{OUT}}{I_{PP}} \times \frac{V_{OUT}}{f_{SW} \times V_{IN_MAX}} \quad (17)$$

where:

- V_{IN_MAX} is the maximum input voltage for the converter
- V_{OUT} is the converter output voltage
- f_{SW} is the nominal converter switching frequency

The final inductor value can be optimized through simulation and testing to attain the desired tradeoff between transient performance and efficiency.

9.2.2.2 Current Limit Threshold

The inductor saturation current rating needs to handle the expected overcurrent in the system. To determine the proper saturation current rating, the valley overcurrent threshold, and the corresponding peak current during that mode, are calculated. Referring to [Equation 14](#), the valley overcurrent protection limit is selected according to [Equation 18](#).

$$I_{VALLEY} = \left(M \times \frac{I_{OUT_MAX}}{n} \right) - \frac{I_{PP}}{2} \quad (18)$$

In this equation:

- M is the desired percentage margin above the maximum load current

After the desired valley current for the overcurrent is determined, the proper value of R_{OCL} needed to program this threshold is determined based on equating Equation 14 and Equation 15. The minimum saturation current rating that is required of the inductor is based on the worst-case peak current seen during the overcurrent condition, as calculated in Equation 19.

$$I_{SAT} = I_{VALLEY} + I_{PP} \quad (19)$$

9.2.2.3 Load-Line Setting

Using the droop regulation capability of the controller, the load-line can be set based on the allowable DC setpoint variance of the target voltage rail. The load line-resistance R_{LL} is determined by:

$$R_{LL} = \frac{V_{OUT_ZL} - V_{OUT_ML}}{I_{OUT_MAX}} \quad (20)$$

where:

- V_{OUT_ZL} is the desired output voltage at zero load
- V_{OUT_ML} is the desired output voltage at maximum load

The droop limits V_{OUT_ZL} and V_{OUT_ML} are selected to allow margin to the minimum and maximum limits for the voltage tolerance specification of the load. Selecting the droop limits with margin also allows for the accounting of factors such as the V_{OUT_SET} tolerance, output voltage ripple, and additional voltage drops that occur in the printed circuit board or voltage sense lines.

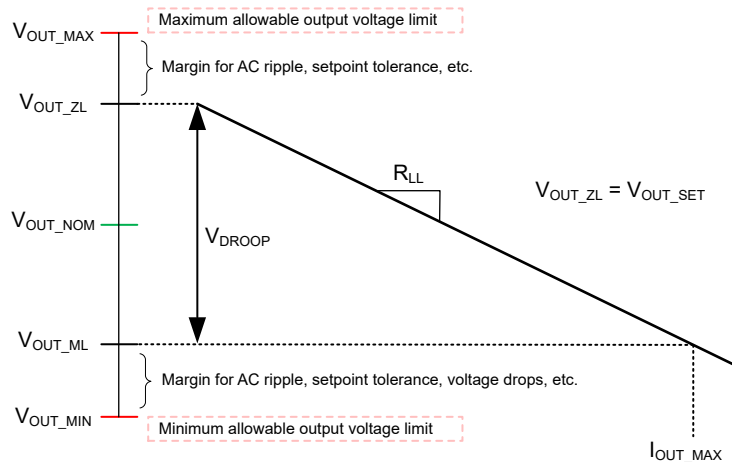


Figure 9-2. Determination of Load-Line Limits

To correspond the nominal output voltage V_{OUT_NOM} with a specific load current I_{OUT_TARGET} , R_{SET} can be adjusted such that V_{OUT_SET} is equal to the zero load output voltage V_{OUT_ZL} . The nominal output voltage is then found based on Equation 21.

$$V_{OUT_NOM} = V_{OUT_SET} - (R_{LL} \times I_{OUT_TARGET}) \quad (21)$$

Once the desired R_{LL} value is determined, then A_{DROOP} is determined from Equation 3 and Equation 4 according to:

$$A_{DROOP} = \frac{R_{CS(eff)} \times A_{CS(eff)}}{R_{LL}} = 1 + \left(\frac{R_{DROOP}}{R_{COMP}} \right) \quad (22)$$

Thus, for a desired load-line, R_{DROOP} can be selected to calculate the necessary R_{COMP} .

$$R_{COMP} = \frac{R_{DROOP}}{A_{DROOP} - 1} \quad (23)$$

9.2.2.4 Output Capacitor Selection

Typically, the allowable voltage deviation during load transients is the determining factor in the amount of output capacitance that is needed for the converter design. During load steps, there is some time required for the inductor to slew to the target current level. In this period, charge is pulled from the output capacitors while the output voltage dips. Likewise, during load releases, charge from the inductor is sent to the output capacitors and the output voltage overshoots. The amount of capacitance required to handle the expected undershoot and overshoot depends on the magnitude of the load step, the amount of inductance selected, and the charge that must be delivered during these periods.

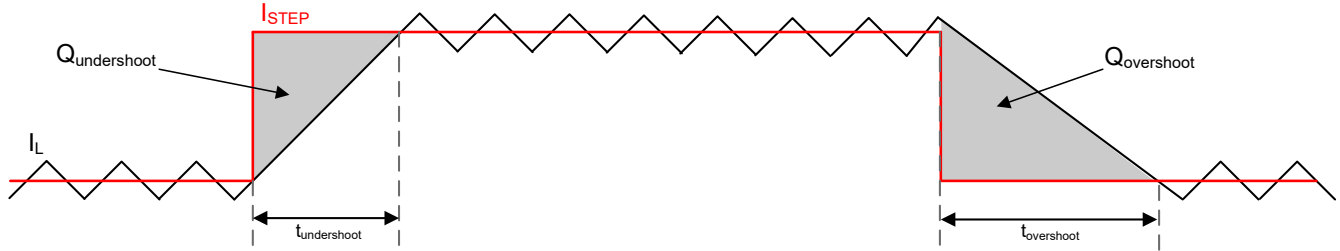


Figure 9-3. Load Transient Waveforms

The periods of overshoot and undershoot, as well as the charge required during those times, are calculated based on Equation 24 to Equation 28:

$$L_{EQ} = \frac{L}{n} \quad (24)$$

$$t_{undershoot} = \frac{L_{EQ} \times I_{STEP}}{V_{IN} - V_{OUT}} \quad (25)$$

$$Q_{undershoot} = \frac{1}{2} \times t_{undershoot} \times I_{STEP} \quad (26)$$

$$t_{overshoot} = \frac{L_{EQ} \times I_{STEP}}{V_{OUT}} \quad (27)$$

$$Q_{overshoot} = \frac{1}{2} \times t_{overshoot} \times I_{STEP} \quad (28)$$

where:

- L_{EQ} is the equivalent inductance which is equal to the per-phase inductance divided by the number of phases
- I_{STEP} is the magnitude of the maximum load step and/or load release that is expected

The calculation of the required capacitance involves dividing the required charge by the allowable output voltage deviation ΔV_{OUT} due to the load transient. The load-line resistance R_{LL} can be considered in this capacitance calculation.

$$C_{undershoot} = \frac{Q_{undershoot}}{\Delta V_{OUT} + (I_{STEP} \times R_{LL})} \quad (29)$$

$$C_{overshoot} = \frac{Q_{overshoot}}{\Delta V_{OUT} + (I_{STEP} \times R_{LL})} \quad (30)$$

If droop regulation is not used, set R_{LL} equal to 0. The user needs to select an output capacitance that is greater than the larger calculated capacitance between $C_{undershoot}$ and $C_{overshoot}$ for the design. A mix of ceramic and bulk capacitance is needed for the best overall performance. The ceramic capacitors keep the output impedance relatively low during the initial period of the transient, allowing the overshoot and undershoot to be minimized

before the control loop of the converter responds. The bulk capacitors can supply sufficient charge to keep the output voltage within the allowable tolerance as the inductor current slews during the transient.

9.2.2.5 Loop Compensation

There are instances where the observed transient behavior of the converter needs improvement and additional compensation can be added. The compensation that is added generally depends on the specific circumstances.

The need for additional loop compensation can be impacted by the amount of output capacitance that is selected for the design. [Section 9.2.2.4](#) details a procedure for initial output capacitor selection. An estimate of the converter crossover frequency can be found according to [Equation 31](#). For D-CAP+ control, the crossover frequency can be up to one-fourth of the nominal switching frequency allowing for much improved transient response.

$$f_c = \frac{1}{2\pi \times C_{OUT}} \times \frac{A_{DROOP}}{R_{CS} \times A_{CS}} \quad (31)$$

When a low amount of output capacitance is used, such as when the area on the printed circuit board is limited, there is a potential for a combination of high bandwidth with poor phase margin. Furthermore, if the load line is shallow or droop regulation is not used, poor phase margin can result and additional compensation is potentially needed for improvement. In each of the aforementioned cases, a series resistor-capacitor combination can be added across R_{DROOP} (between DROOP to COMP) for improved transient behavior. This RC adds a zero to the overall loop transfer function with a frequency given by [Equation 32](#).

$$f_z = \frac{1}{2\pi \times C_{DC} \times (R_{DC} + (R_{COMP} \parallel R_{DROOP}))} \quad (32)$$

The additional zero can be used to improve phase margin, with the RC acting to reduce the gain A_{DROOP} from an AC perspective and subsequently, the converter bandwidth.

For cases where the output capacitance selected is sufficiently high to meet the transient requirements but there is still a need to increase the overall bandwidth, a series resistor-capacitor combination can be added in parallel with R_{COMP} (from COMP to VREF). The RC acts to increase the gain A_{DROOP} and the converter bandwidth. In this configuration, the RC adds a pole and zero to the loop transfer function with the frequencies depicted in [Equation 33](#) and [Equation 34](#).

$$f_z = \frac{1}{2\pi \times C_{CR} \times (R_{CR} + (R_{COMP} \parallel R_{DROOP}))} \quad (33)$$

$$f_p = \frac{1}{2\pi \times R_{CR} \times C_{CR}} \quad (34)$$

In all cases, the RC values are fine tuned to attain the desired transient response. For the printed circuit board layout, the user can add placeholders for an RC both across R_{COMP} and R_{DROOP} in the event that an improved transient response is needed. An additional placeholder for a small capacitor from COMP to DROOP can also be added for mitigation of potential noise issues.

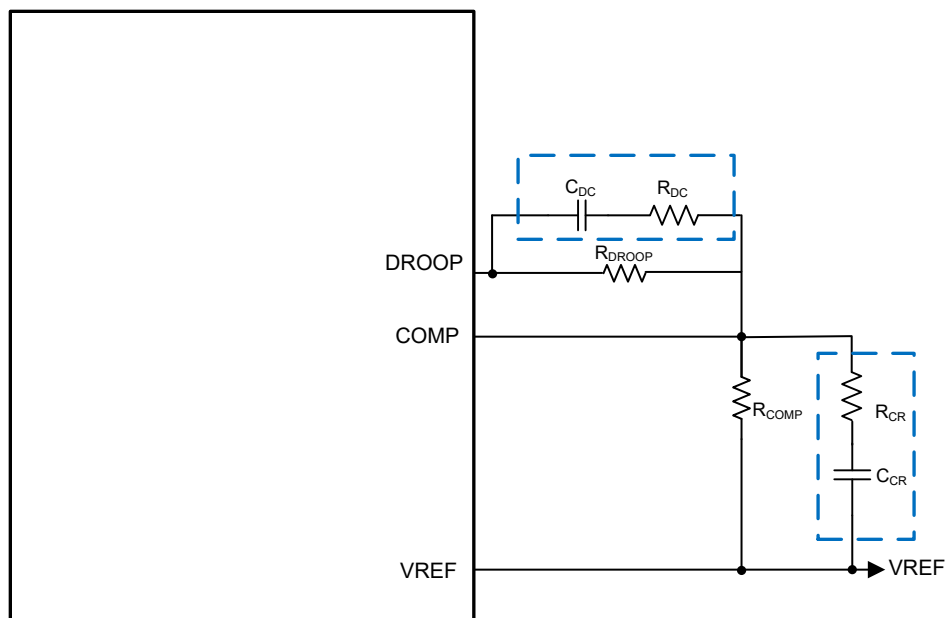


Figure 9-4. Compensation Component Placement Options for TPS7H5101

9.2.3 Application Curve

Typical plots are shown for the following conditions:

- VIN (TPS7H5101) = PVIN (TPS7H6200) = 12V
- VOUT = 0.8V
- IOUT = 20A
- Switching frequency = 500kHz (nominal)

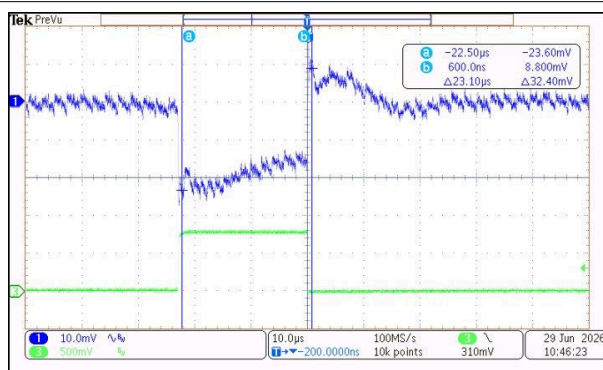


Figure 9-5. VOUT Response to 20A to 57A Load Step With Slew Rate of 150A/μs

9.3 Power Supply Recommendations

The TPS7H5101 is designed to operate from an input supply voltage of 4.5V to 15V. This voltage is applied to the VIN pin of the device. The input voltage supply for the controller needs to be well regulated and properly bypassed for best electrical performance. A minimum input bypass capacitor of 1µF from VIN to GND is needed for best performance, but additional capacitance can be used to improve the noise performance of the controller. Place these capacitors as close to the controller as possible with a low impedance path to GND.

The TPS7H5101 uses an adaptive on-time architecture, which adjusts the on-time of the output pulses based on several factors, including the input voltage. As such, to maintain a relatively constant switching frequency during steady-state operation, the controller input voltage at VIN needs to be the same as input voltage of the buck converter power stage. If using the TPS7H5101 in conjunction with the TPS7H6200 power stage, PVIN of the power stage and VIN of the controller are the same. Both the on-time and current sharing circuitry of the controller require the input from the power stage to operate as intended.

Sufficient bulk and decoupling capacitors are required near the power stage voltage connection to the FETs to minimize overall impedance and improve converter efficiency. Refer to the *Power Supply Recommendations* and *Layout Guidelines* for the TPS7H6200 for additional details.

9.4 Layout

9.4.1 Layout Guidelines

- Place the bypass capacitors for VIN of the controller as close to the device as possible.
- When using the TPS7H5101 with the TPS7H6200 power stage, differentially route the power stage current sense pins IOUTx and REFINx signals to the CS_Px and CS_Nx pins of the controller. Place these sense traces on a quiet layer of the printed circuit board. Also, route the traces and place any associated vias away from the switch node and PWM signals for the power stage.
- The REFIN signals from the power stage are connected to both VREF and CS_N signals of the controller. These connections can be made near the controller. For best results, avoid connecting REFIN signals to a plane or copper pour for VREF and differentially route the sense signals as previously detailed.
- If the TPS7H6200 is not used or if current sensing is performed using the inductor DCR or discrete sense resistor, utilize Kelvin connections from the pads of the resistor or inductor back to the current sense pins (CS_P and CS_N) of the controller. These signals also need to be differentially routed.
- Place the OUT_SET resistor as close to the controller as possible. Likewise, if using a 470pF capacitor from OUT_SET to VSNS_P for noise and single event transient mitigation, the capacitor also needs to be placed in close proximity to the device.
- Differentially route VSNS_P and VSNS_N remote sense lines routed from the load. Connect the VSNS_P trace to the point on the printed circuit board at which the voltage needs to be regulated and routed back to the controller. For best results, do not connect VSNS_P directly to the copper plane used for the high current output voltage. Likewise, do not directly connected VSNS_N to the ground plane at the controller. Route the VSNS_N trace from the load to the OUT_SET resistor. Avoid routing the sense traces across the switch node of the power stage.
- Allow high current traces to have sufficient conductor width and via count to minimize voltage drop across the printed circuit board. Utilize pours and planes for these connections where possible to decrease resistance and inductance of the path.
- If using external compensation components between COMP and DROOP, and/or between COMP and VREF, plan to place these components as close to the device as possible.
- Place the PMBus address setting resistor close to the device, away from the SCL line and PWM signals as best possible.
- Prioritize component placement near the controller in the following order, from highest to lowest priority:
 - VIN bypass capacitors
 - OUT_SET resistor and capacitor
 - DROOP, COMP, and VREF compensation components
 - PMBus address setting resistor
 - OCL, BLANK, OSR, and USR resistors

- Minimize high current and high di/dt loop areas in the layout, which include the input capacitor loop, the main current loop, and the gate drive loops. Minimize the switch node area as best possible to mitigate noise coupling issues.
- Separate analog ground for the controller from the power ground on the printed circuit board to isolate the high-frequency switching noise in the power stage from the controller circuitry. Connect the grounds at a single point to maintain the quiet analog reference for the controller.

9.4.2 Layout Example

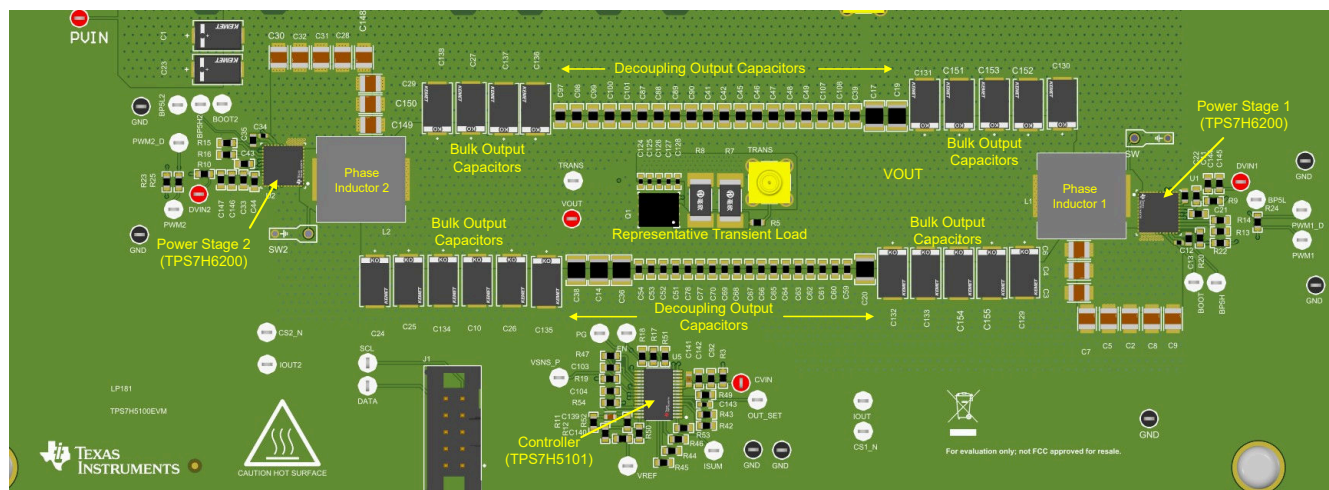


Figure 9-6. 3D Layout Example With TPS7H5101 in Dual Phase Setup With TPS7H6200

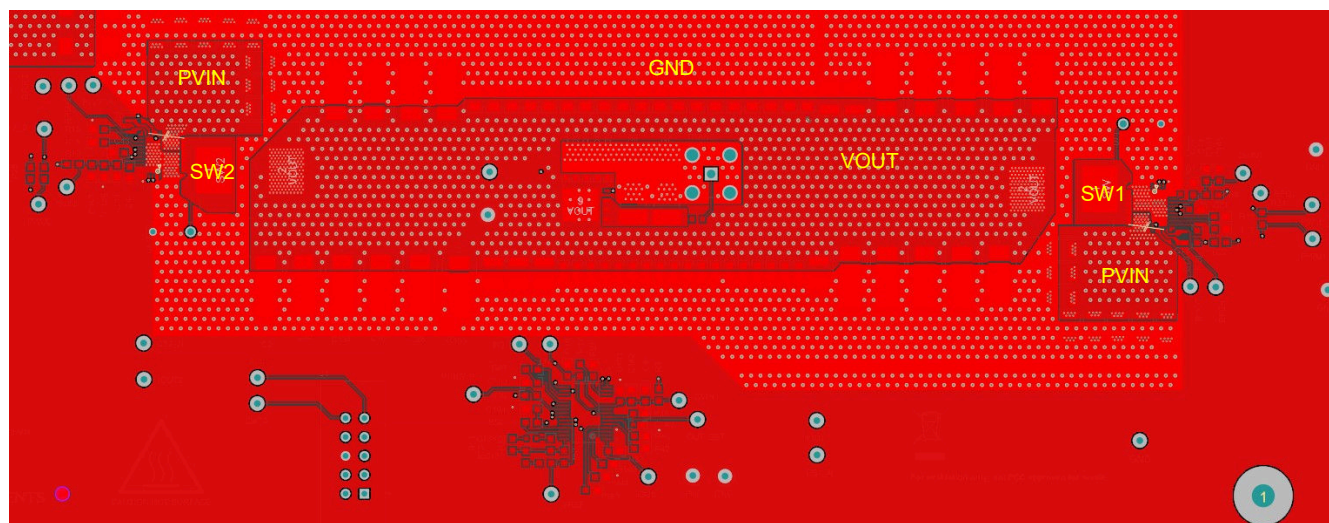


Figure 9-7. 2D Layout Example With TPS7H5101 and TPS7H6200 - Top Layer View

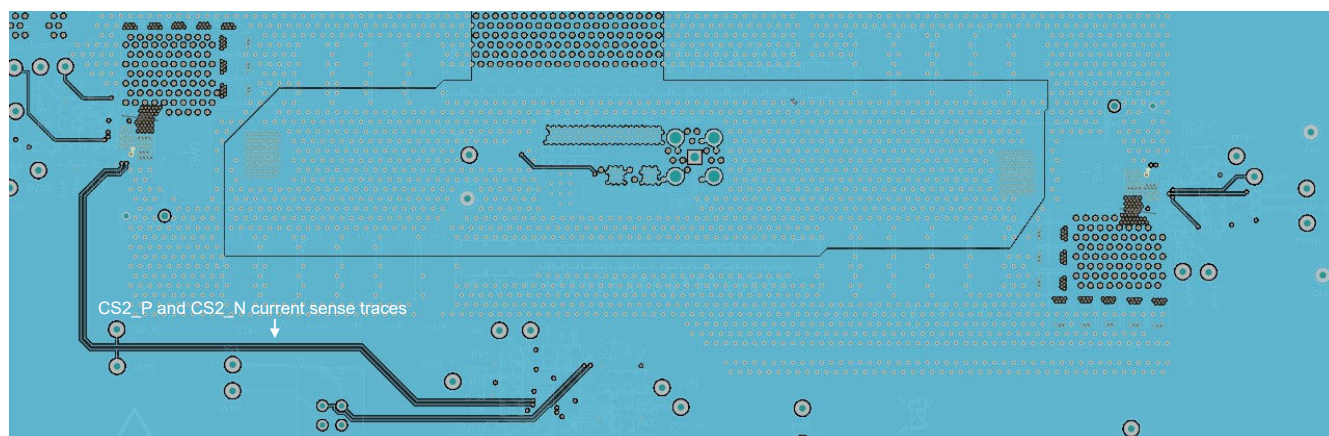


Figure 9-8. Example of Differential Current Sense Routing From Power Stage to TPS7H5101

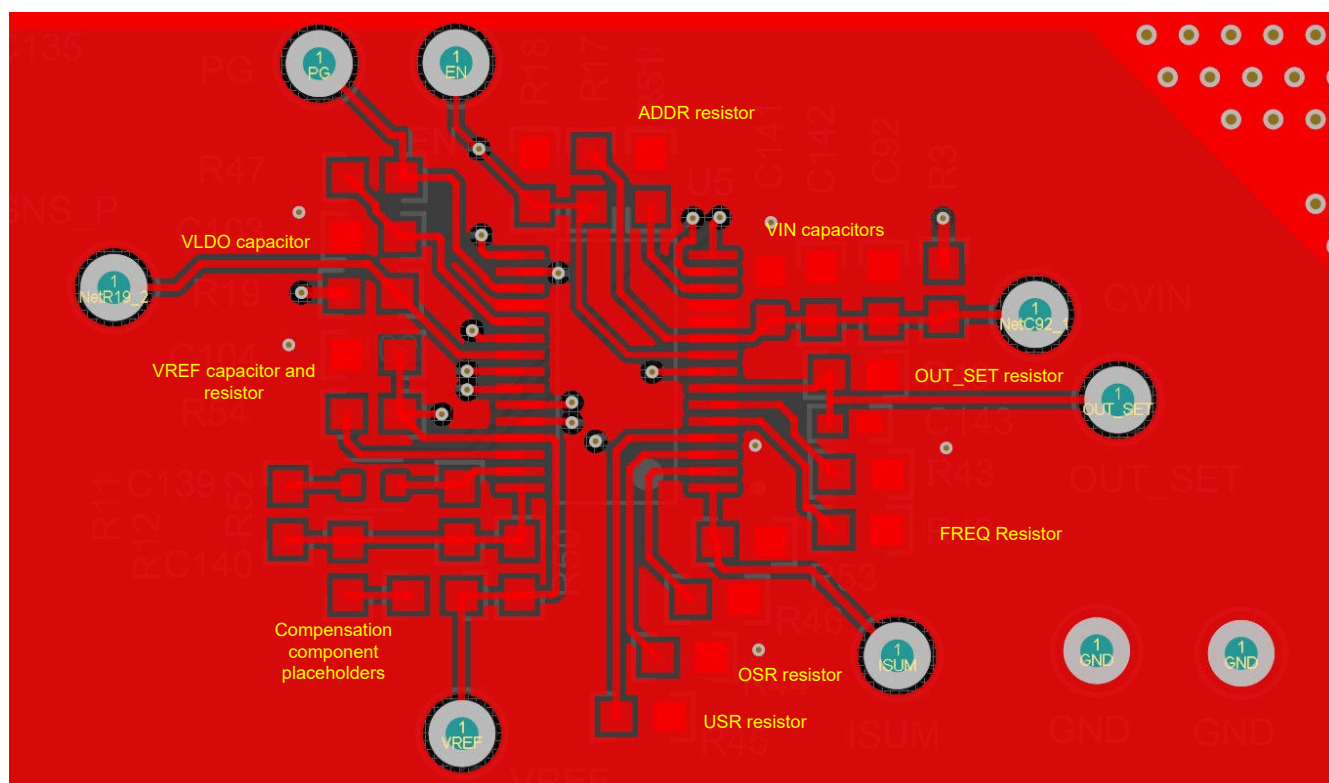


Figure 9-9. Top Layer View of TPS7H5101 and Component Placement

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

10.1.2 Related Documentation

- [An Introduction to the D-CAP+ Modulator and Its Real World Performance](#)
- [D-CAP+ Control for Multiphase, Step-Down Voltage Regulators for Powering Microprocessors](#)

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

10.4 Trademarks

D-CAP+™ and TI E2E™ are trademarks of Texas Instruments.

PMBus® is a registered trademark of System Management Interface Forum, Inc..

All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2026	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

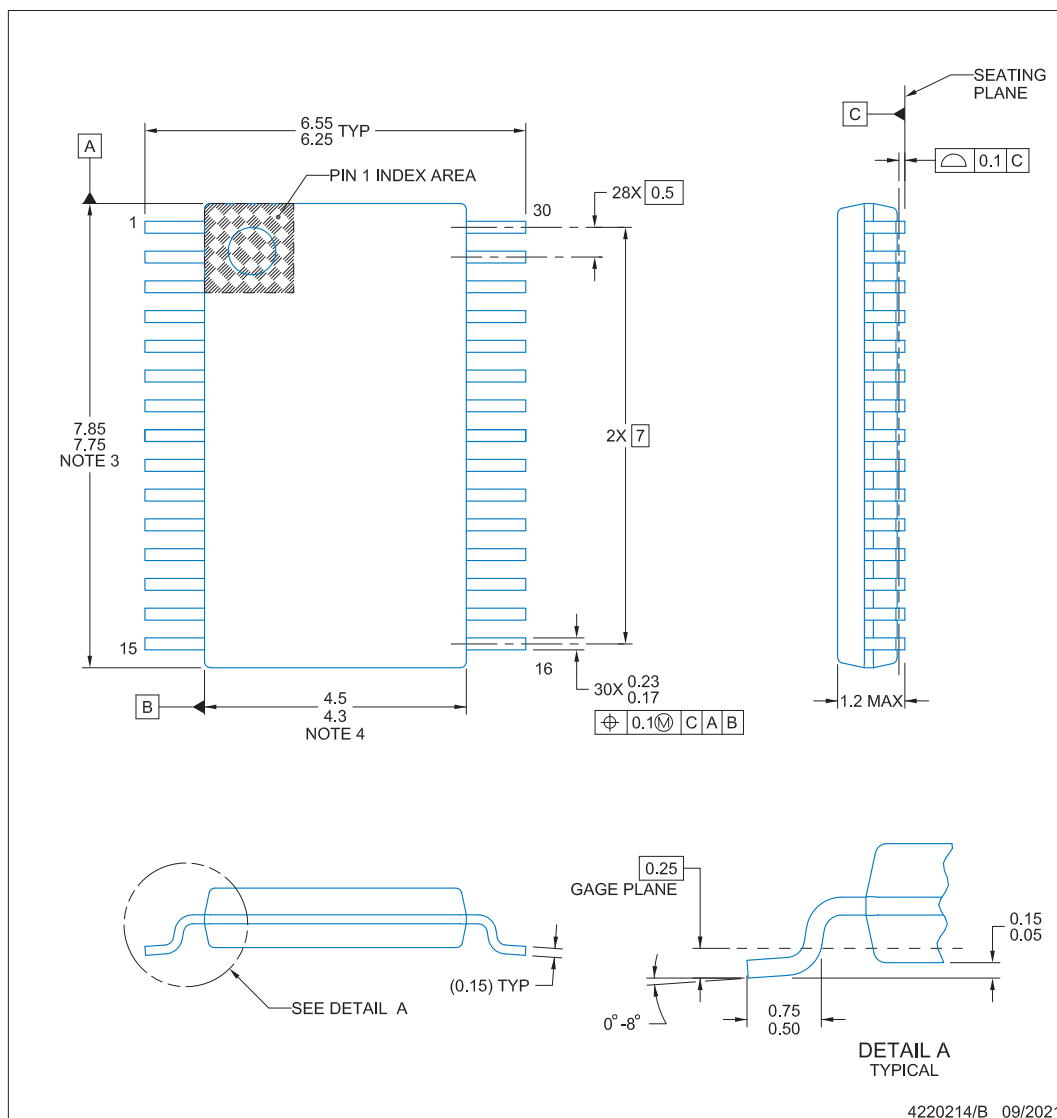
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this datasheet, refer to the left-side navigation.

PACKAGE OUTLINE

DBT0030A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



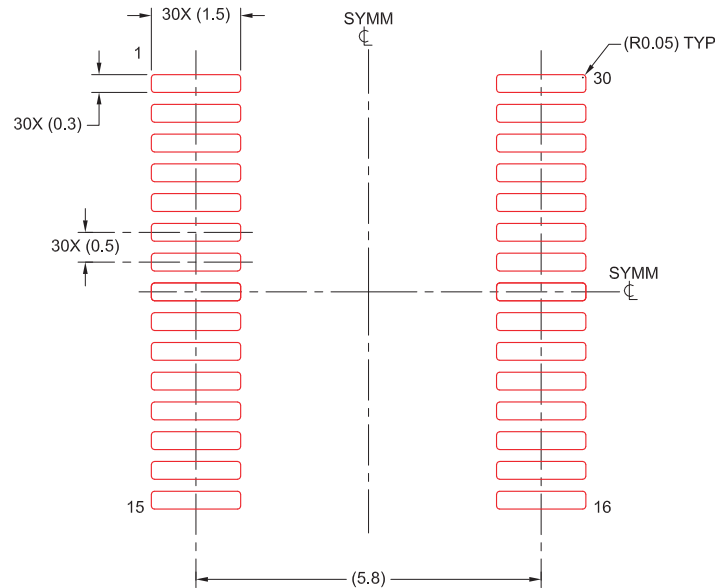
ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

DBT0030A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220214/B 09/2021

NOTES: (continued)

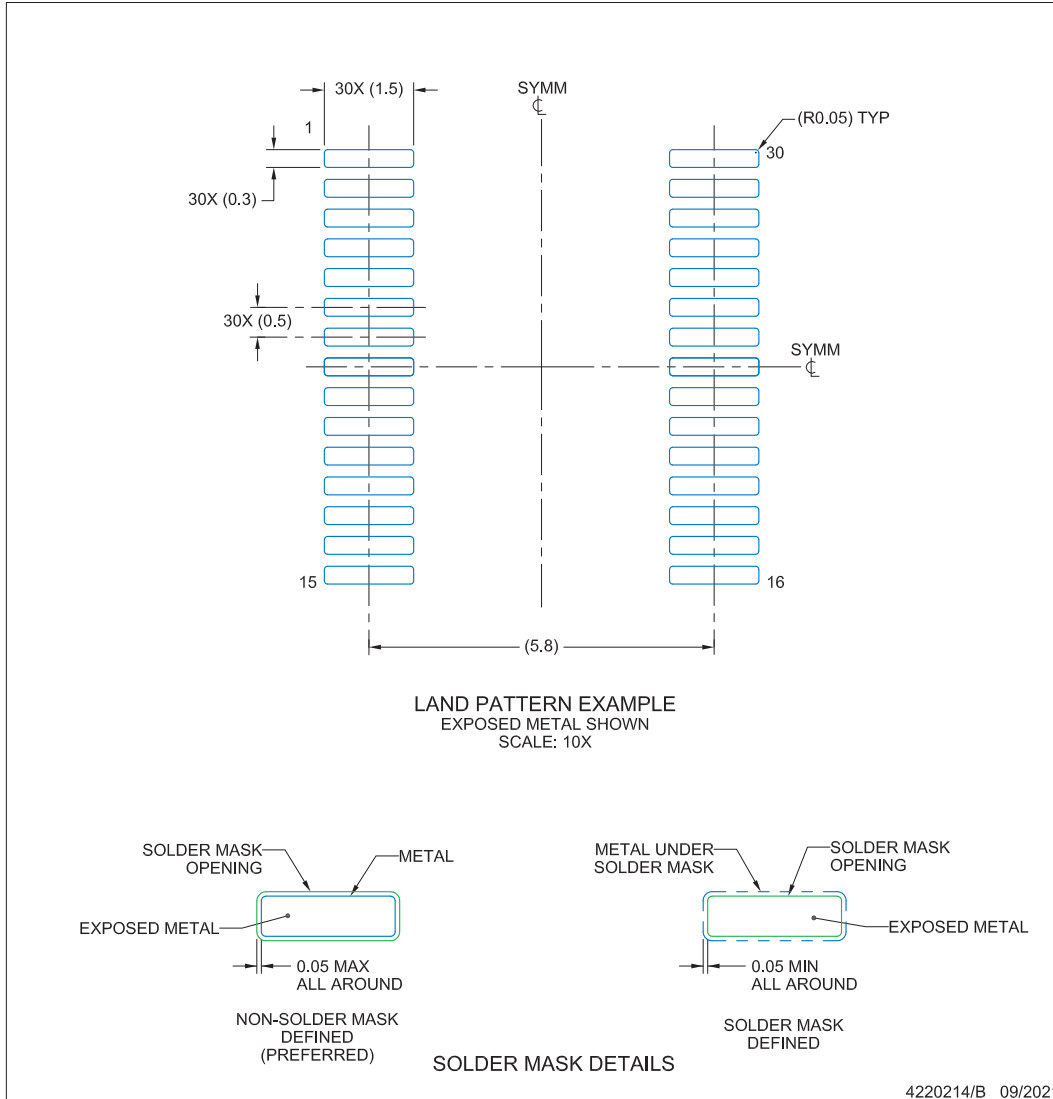
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

EXAMPLE BOARD LAYOUT

DBT0030A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTPS7H5101DBTTSEPA	Active	Preproduction	TSSOP (DBT) 30	250 SMALL T&R	-	Call TI	Call TI	-55 to 125	

- (1) **Status:** For more details on status, see our [product life cycle](#).
- (2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- (3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- (4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025