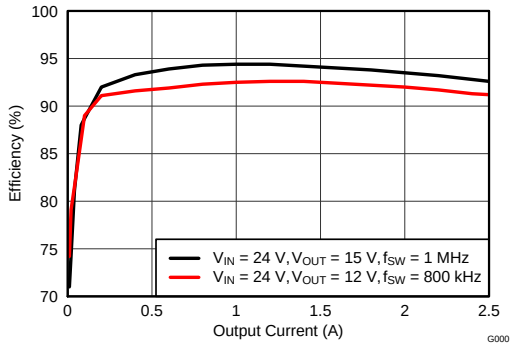
TPS84250 7-V to 50-V Input, 2.5-A Step-Down, Integrated Power Solution

1 FEATURES

- Complete Integrated Power Solution Allows Small Footprint, Low-Profile Design
- Wide Input-Voltage Range from 7 V to 50 V
- Output Adjustable from 2.5 V to 15 V
- 65-V Surge Capability
- Efficiencies Up to 96%
- Adjustable Switching Frequency (300 kHz to 1 MHz)
- Synchronizes to an External Clock
- Adjustable Slow Start
- Output Voltage Sequencing and Tracking
- Power-Good Output
- Programmable Undervoltage Lockout (UVLO)
- Output Overcurrent Protection
- Overyemperature Protection
- Prebias Output Start-Up
- Operating Temperature Range: –40°C to +85°C
- Enhanced Thermal Performance: 14°C/W
- Meets EN55022 Class B Emissions
- For Design Help Visit http://www.ti.com/TPS84250

2 APPLICATIONS

- Industrial and Motor Controls
- Automated Test Equipment
- Medical and Imaging Equipment
- High Density Power Systems

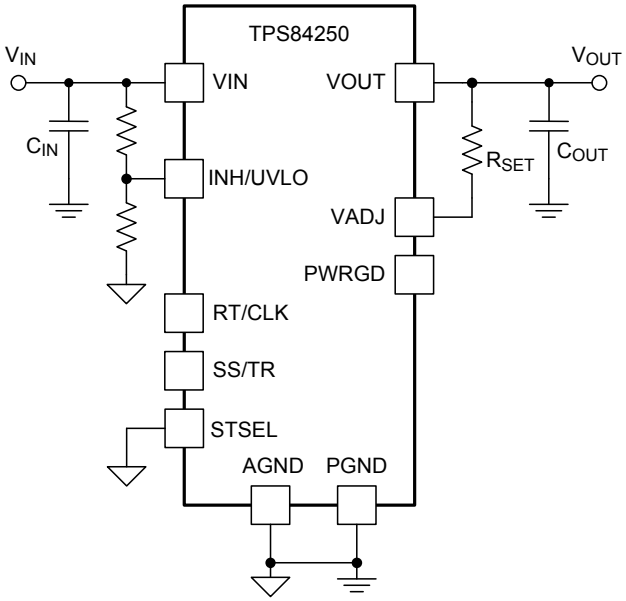


3 DESCRIPTION

The TPS84250 is an easy-to-use integrated power solution that combines a 2.5-A DC/DC converter with an inductor and passives into a low profile, QFN package. This total power solution allows as few as five external components and eliminates the loop compensation and magnetics part selection process.

The small 9 mm × 11 mm × 2.8 mm, QFN package is easy to solder onto a printed circuit board and allows a compact point-of-load design with greater than 90% efficiency and excellent power dissipation capability. The TPS84250 offers the flexibility and the feature-set of a discrete point-of-load design and is ideal for powering a wide range of ICs and systems. Advanced packaging technology affords a robust and reliable power solution compatible with standard QFN mounting and testing techniques.

SIMPLIFIED APPLICATION



9 mm × 11 mm × 2.8 mm

Table 1. ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this datasheet, or see the TI website at www.ti.com.

4 Specifications

4.1 ABSOLUTE MAXIMUM RATINGS(1)

over operating temperature range (unless otherwise noted)		MIN	MAX	UNIT
Input Voltage	VIN	–0.3	65	V
	INH/UVLO	–0.3	5	V
	VADJ	–0.3	3	V
	PWRGD	–0.3	6	V
	SS/TR	–0.3	3	V
	STSEL	–0.3	3	V
	RT/CLK	–0.3	3.6	V
Output Voltage	PH	–0.6	65	V
	PH 10ns Transient	–2	65	V
	VOUT	–0.6	V_{IN}	V
V_{DIFF} (GND to exposed thermal pad)			±200	mV
Source Current	RT/CLK		100	µA
	INH/UVLO		100	µA
Sink Current	SS/TRK		200	µA
	PWRGD		10	mA
Operating Junction Temperature		–40	105(2)	°C
Storage Temperature		–65	150	°C
Peak Reflow Case Temperature(3)(4)			250	°C
Maximum Number of Reflows Allowed(3)(4)			3	
Mechanical Shock	Mil-STD-883D, Method 2002.3, 1 msec, 1/2 sine, mounted		1500	G
Mechanical Vibration	Mil-STD-883D, Method 2007.2, 20-2000Hz		20	

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) See the temperature derating curves in the Typical Characteristics section for thermal information.
(3) For soldering specifications, refer to the *Soldering Requirements for BQFN Packages* application note.
(4) Devices with a date code prior to week 14 2018 (1814) have a peak reflow case temperature of 240°C with a maximum of one reflow.

4.2 RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)		MIN	MAX	UNIT
V_{IN}	Input Voltage	7	50	V
V_{OUT}	Output Voltage	2.5	15	V
f_{SW}	Switching Frequency	400	1000	kHz
T_A	Operating Ambient Temperature	-40	85	°C

4.3 PACKAGE SPECIFICATIONS

TPS84250		UNIT
Weight		0.9 grams
Flammability	Meets UL 94 V-O	
MTBF Calculated reliability	Per Bellcore TR-332, 50% stress, T_A = 40°C, ground benign	31.7 MHrs

4.4 ELECTRICAL CHARACTERISTICS

-40°C ≤ T_A ≤ +85°C, V_{IN} = 24 V, V_{OUT} = 5.0 V, I_{OUT} = 2.5 A, R_T = Open
C_{IN} = 2 x 2.2 µF ceramic, C_{OUT} = 2 x 47 µF ceramic (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{OUT}	Output current	Over input voltage and output voltage range		0		2.5	A
V_{IN}	Input voltage range	Over output current range		7.0 (1)		50 (2)	V
UVLO	VIN Undervoltage lockout	No hysteresis, Rising and Falling			2.5		V
$V_{OUT(adj)}$	Output voltage adjust range	Over output current range		2.5 (3)		15	V
V_{OUT}	Set-point voltage tolerance	T_A = 25°C; I_{OUT} = 100 mA				±2.0% (4)	
	Temperature variation	-40°C ≤ T_A ≤ +85°C			±0.5%	±1.0%	
	Line regulation	Over input voltage range			±0.1%		
	Load regulation	Over output current range			±0.4%		
	Total output voltage variation	Includes set-point, line, load, and temperature variation				±3.0% (4)	
η	Efficiency	V_{IN} = 24 V, I_{OUT} = 1.5 A	V_{OUT} = 12 V, f_{SW} = 800 kHz		93 %		
			V_{OUT} = 5.0 V, f_{SW} = 500 kHz		84 %		
			V_{OUT} = 3.3 V, f_{SW} = 400 kHz		79 %		
		V_{IN} = 48 V, I_{OUT} = 1.5 A	V_{OUT} = 12 V, f_{SW} = 800 kHz		87 %		
			V_{OUT} = 5.0 V, f_{SW} = 500 kHz		79 %		
			V_{OUT} = 3.3 V, f_{SW} = 400 kHz		74 %		
	Output voltage ripple	20 MHz bandwith, 0.25 A ≤ I_{OUT} ≤ 2.5 A, VOUT ≥ 3.3V			1% (3)		V_{OUT}
I_{LIM}	Current limit threshold				5.1		A
	Transient response	1.0 A/µs load step from 50 to 100% $I_{OUT(max)}$	Recovery time		400		µs
			VOUT over/undershoot		90		mV
V_{INH}	Inhibit threshold voltage	No hysteresis		1.15	1.25	1.36 (5)	V
I_{INH}	INH Input current	V_{INH} < 1.15 V			-0.9		µA
		V_{INH} > 1.36 V			-3.8		µA
$I_{I(stby)}$	Input standby current	INH pin to AGND			1.3	4	µA
Power Good	PWRGD Thresholds	V_{OUT} rising	Good		94%		
			Fault		109%		
		V_{OUT} falling	Fault		91%		
			Good		106%		
	PWRGD Low Voltage	I(PWRGD) = 3.5 mA			0.2		V
f_{SW}	Switching frequency	RT/CLK pin OPEN		300	400	500	kHz
f_{CLK}	Synchronization frequency	CLK Control		300		1000	kHz
V_{CLK-H}	CLK High-Level Threshold				1.9	2.2	V
V_{CLK-L}	CLK Low-Level Threshold			0.5	0.7		V
D_{CLK}	CLK Duty cycle			25%	50%	75%	
	Thermal Shutdown	Thermal shutdown			180		°C
		Thermal shutdown hysteresis			15		°C
C_{IN}	External input capacitance		Ceramic	4.4 (6)	10		µF
			Non-ceramic		22		
C_{OUT}	External output capacitance			100 (7)		430	µF

(1) For output voltages ≤ 12 V, the minimum input voltage is 7 V or (V_{OUT}+ 3 V), whichever is greater. For output voltages > 12 V, the minimum input voltage is (1.33 x V_{OUT}). See Figure 27 for more details.
(2) The maximum input voltage is 50 V or (15 x V_{OUT}), whichever is less.
(3) Output voltages < 3.3 V are subject to reduced $V_{IN(max)}$ specifications and higher ripple magnitudes.
(4) The stated limit of the set-point voltage tolerance includes the tolerance of both the internal voltage reference and the internal adjustment resistor. The overall output voltage tolerance is affected by the tolerance of the external R_{SET} resistor.
(5) Value when no voltage divider is present at the INH/UVLO pin.
(6) A minimum of 4.4µF of ceramic external capacitance is required across the input (VIN and PGND connected) for proper operation. Locate the capacitor close to the device. See Table 3 for more details.
(7) The required capacitance must include at least 2 x 47µF ceramic capacitors (or 4 x 22µF). Locate the capacitance close to the device. Adding additional capacitance close to the load improves the response of the regulator to load transients. See Table 3 for more details.

4.5 THERMAL INFORMATION

THERMAL METRIC[1]		TPS84250 RKG 41 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance[2]	14	°C/W
ψ_{JT}	Junction-to-top characterization parameter[3]	3.3	
ψ_{JB}	Junction-to-board characterization parameter[4]	6.8	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.
(2) The junction-to-ambient thermal resistance, θ_{JA}, applies to devices soldered directly to a 100 mm x 100 mm double-sided, 4-layer PCB with 1 oz. copper and natural convection cooling. Additional airflow reduces θ_{JA}.
(3) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7). $T_J = \psi_{JT} * Pdis + T_T$; where Pdis is the power dissipated in the device and T_T is the temperature of the top of the device.
(4) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7). $T_J = \psi_{JB} * Pdis + T_B$; where Pdis is the power dissipated in the device and T_B is the temperature of the board 1mm from the device.

5 DEVICE INFORMATION

FUNCTIONAL BLOCK DIAGRAM

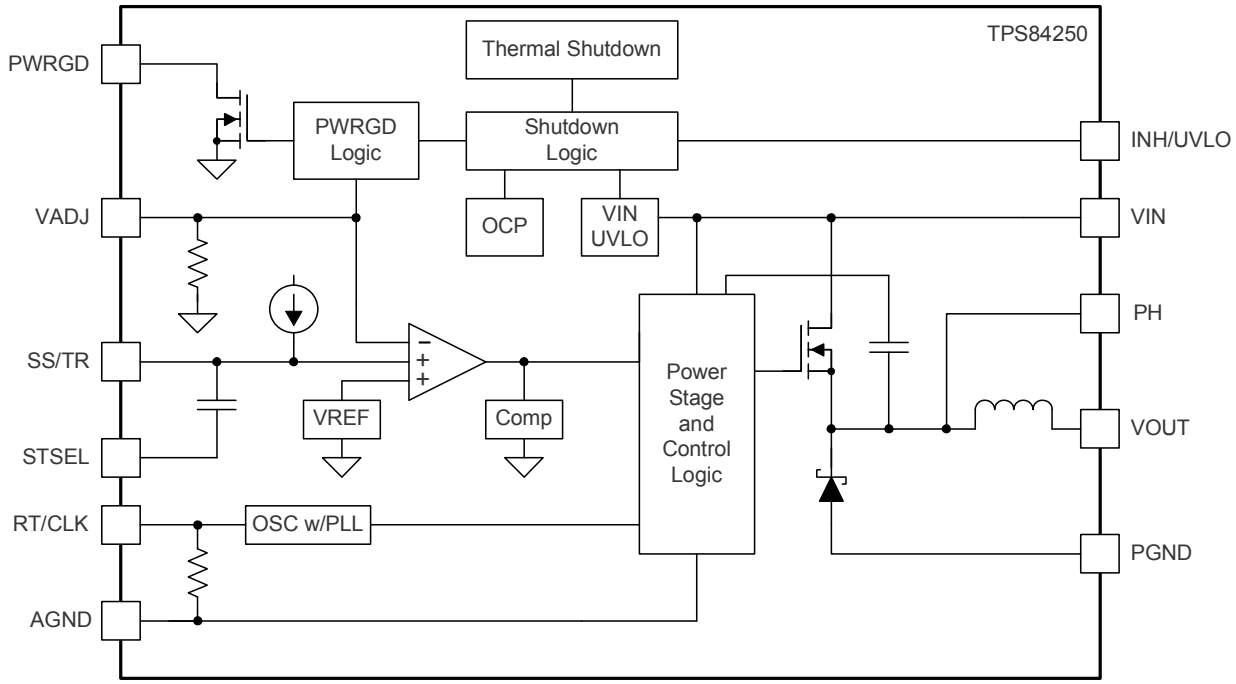
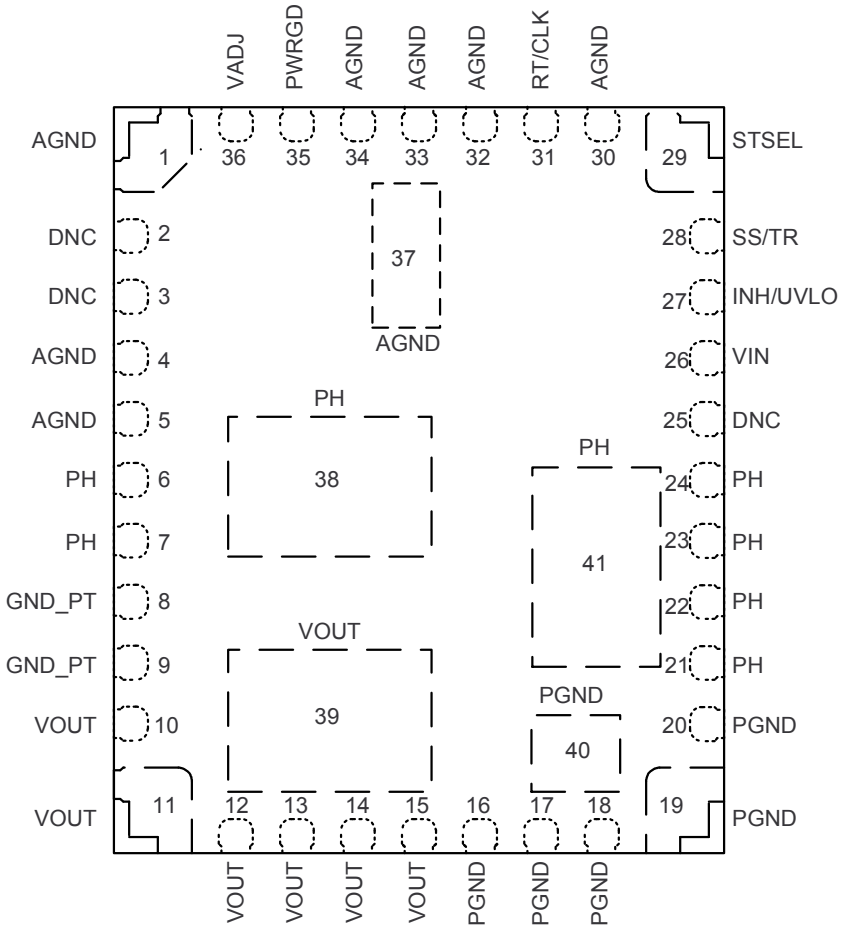


Table 2. PIN DESCRIPTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
AGND	1	These pins are connected to the internal analog ground (AGND) of the device. This node should be treated as the zero volt ground reference for the analog control circuitry. Pad 37 should be connected to PCB ground planes using multiple vias for good thermal performance. Not all pins are connected together internally. All pins must be connected together externally with a copper plane or pour directly under the module. Connect AGND to PGND at a single point (GND_PT; pins 8 & 9). See Layout Recommendations.
	4	
	5	
	30	
	32	
	33	
	34	
	37	
DNC	2	Do Not Connect. Do not connect these pins to AGND, to another DNC pin, or to any other voltage. These pins are connected to internal circuitry. Each pin must be soldered to an isolated pad.
	3	
	25	
PH	6	Phase switch node. Do not place any external component on these pins or tie them to a pin of another function.
	7	
	21	
	22	
	23	
	24	
	38	
	41	
GND_PT	8	Ground Point. Connect AGND to PGND at these pins as shown in the Layout Considerations. These pins are not connected to internal circuitry, and are not connected to one another.
	9	
VOUT	10	Output voltage. These pins are connected to the internal output inductor. Connect these pins to the output load and connect external bypass capacitors between these pins and PGND. Connect a resistor from these pins to VADJ to set the output voltage.
	11	
	12	
	13	
	14	
	15	
	39	
PGND	16	This is the return current path for the power stage of the device. Connect these pins to the load and to the bypass capacitors associated with VIN and VOUT. Pad 40 should be connected to PCB ground planes using multiple vias for good thermal performance.
	17	
	18	
	19	
	20	
	40	
VIN	26	Input voltage. This pin supplies all power to the converter. Connect this pin to the input supply and connect bypass capacitors between this pin and PGND.
INH/UVLO	27	Inhibit and UVLO adjust pin. Use an open drain or open collector logic device to ground this pin to control the INH function. A resistor divider between this pin, AGND, and VIN sets the UVLO voltage.
SS/TR	28	Slow-start and tracking pin. Connecting an external capacitor to this pin adjusts the output voltage rise time. A voltage applied to this pin allows for tracking and sequencing control.
STSEL	29	Slow-start or track feature select. Connect this pin to AGND to enable the internal SS capacitor. Leave this pin open to enable the TR feature.
RT/CLK	31	This pin is connected to an internal frequency setting resistor which sets the default switching frequency. An external resistor can be connected from this pin to AGND to increase the frequency. This pin can also be used to synchronize to an external clock.
PWRGD	35	Power Good flag pin. This open drain output asserts low if the output voltage is more than approximately ±6% out of regulation. A pull-up resistor is required.
VADJ	36	Connecting a resistor between this pin and VOUT sets the output voltage.

RKG PACKAGE
(TOP VIEW)



6 TYPICAL CHARACTERISTICS (VIN = 12 V) (1) (2)

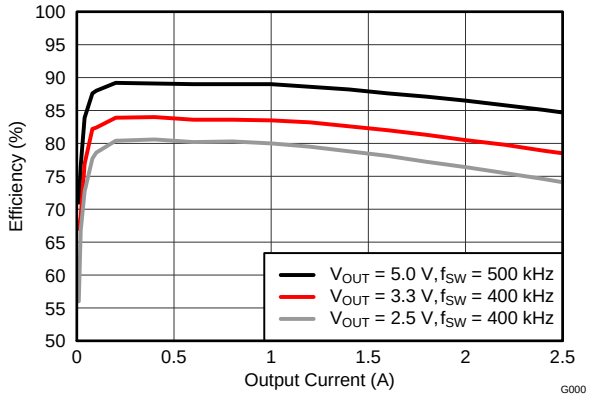


Figure 1. Efficiency vs. Output Current

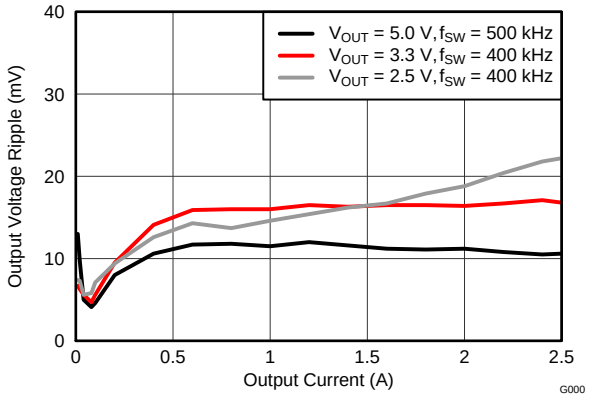


Figure 2. Voltage Ripple vs. Output Current

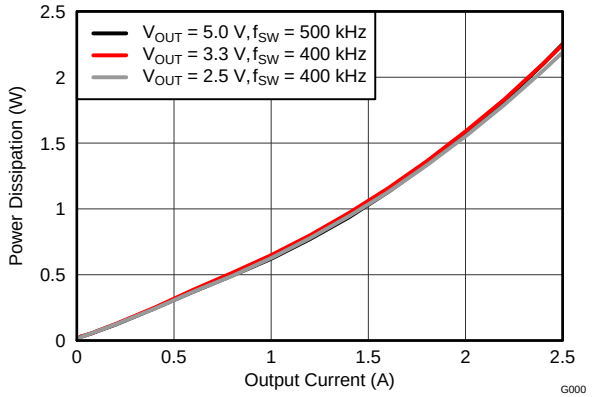


Figure 3. Power Dissipation vs. Output Current

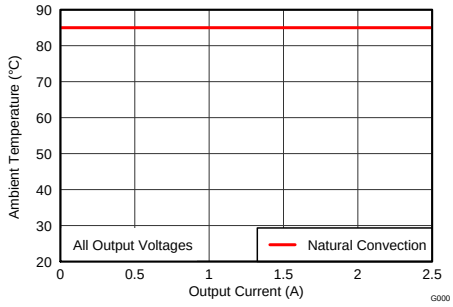


Figure 4. Safe Operating Area

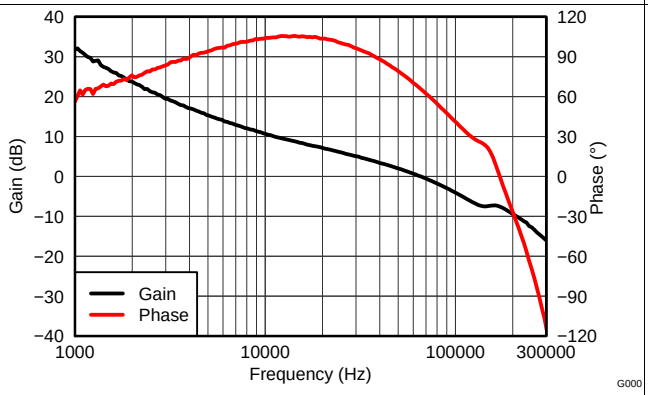


Figure 5. V_{OUT}= 5 V, I_{OUT}= 2 A, C_{OUT1}= 44 µF ceramic, C_{OUT2}= 56 µF electrolytic, f_{SW}= 500 kHz

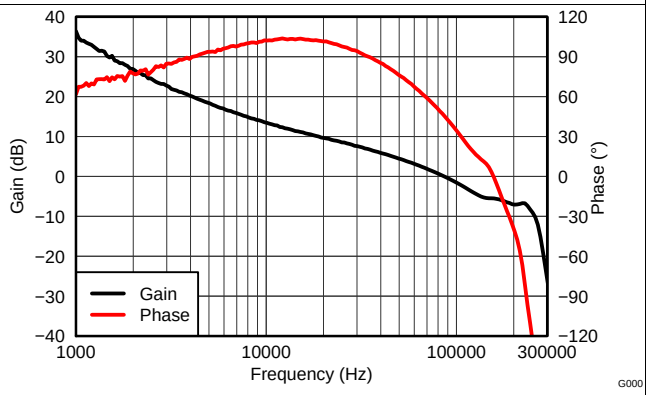


Figure 6. V_{OUT}= 3.3 V, I_{OUT}= 2 A, C_{OUT1}= 44 µF ceramic, C_{OUT2}= 56 µF electrolytic, f_{SW}= 400 kHz

(1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 1, Figure 2, and Figure 3.

(2) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to devices soldered directly to a 100 mm × 100 mm double-sided PCB with 1 oz. copper. Applies to Figure 4.

7 TYPICAL CHARACTERISTICS (VIN = 24 V) (1) (2) (3)

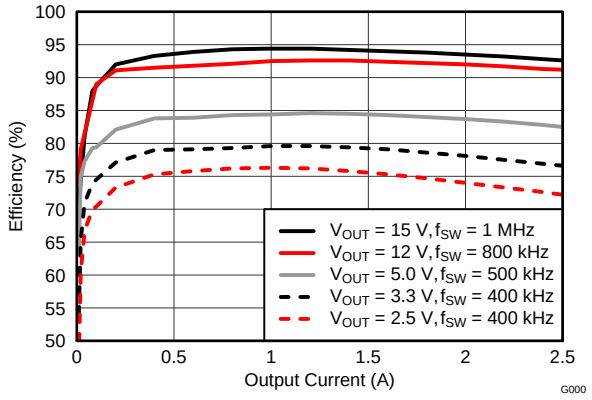


Figure 7. Efficiency vs. Output Current

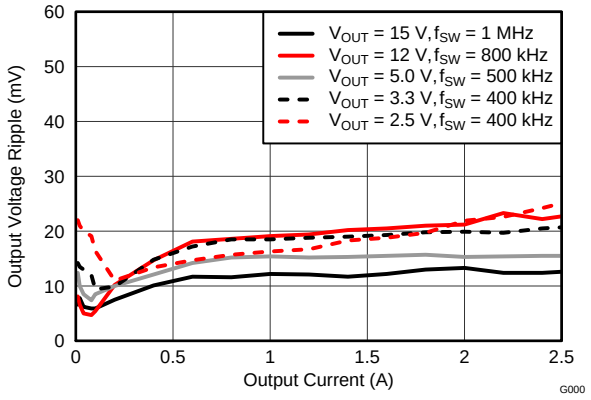


Figure 8. Voltage Ripple vs. Output Current

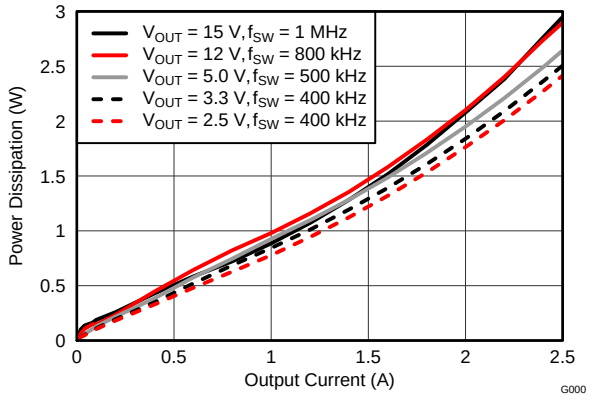


Figure 9. Power Dissipation vs. Output Current

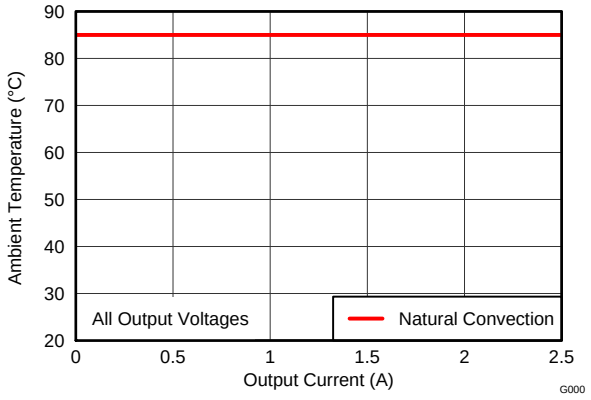


Figure 10. Safe Operating Area

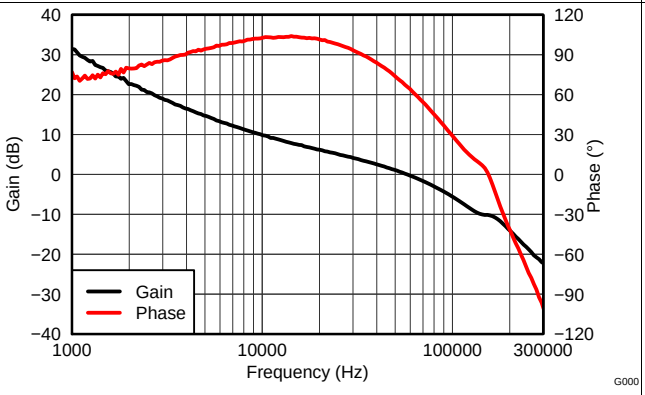


Figure 11. V_{OUT}= 5 V, I_{OUT}= 2 A, C_{OUT1}= 44 µF ceramic, C_{OUT2}= 56 µF electrolytic, f_{SW}= 500 kHz

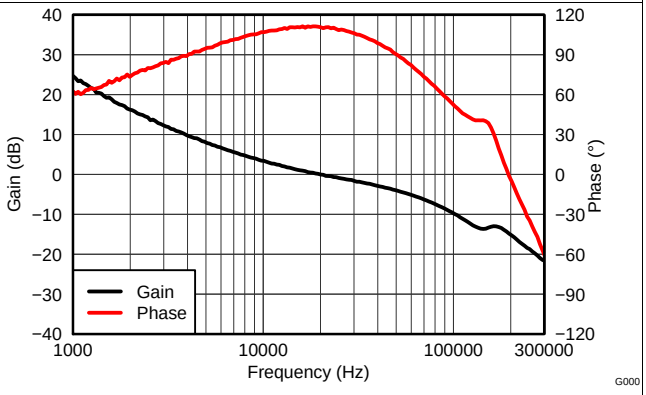


Figure 12. V_{OUT}= 12 V, I_{OUT}= 2 A, C_{OUT1}= 44 µF ceramic, C_{OUT2}= 56 µF electrolytic, f_{SW}= 800 kHz

(1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 7, Figure 8, and Figure 9.
(2) At light load the output voltage ripple may increase due to pulse skipping. See Light-Load Behavior for more information. Applies to Figure 8.
(3) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to devices soldered directly to a 100 mm × 100 mm double-sided PCB with 1 oz. copper. Applies to Figure 10.

8 TYPICAL CHARACTERISTICS (VIN = 36 V) (1) (2) (3)

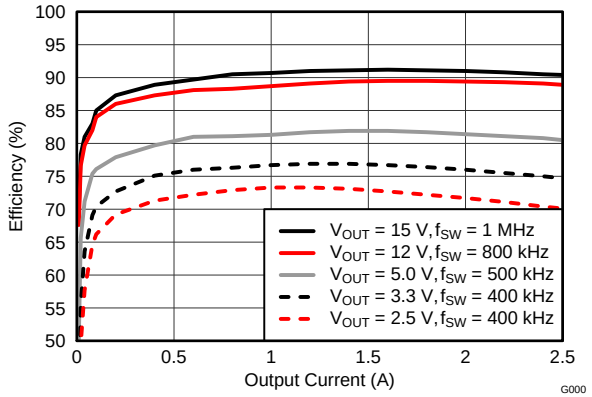


Figure 13. Efficiency vs. Output Current

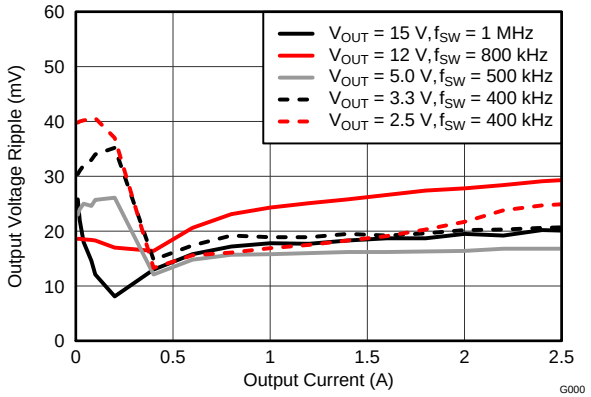


Figure 14. Voltage Ripple vs. Output Current

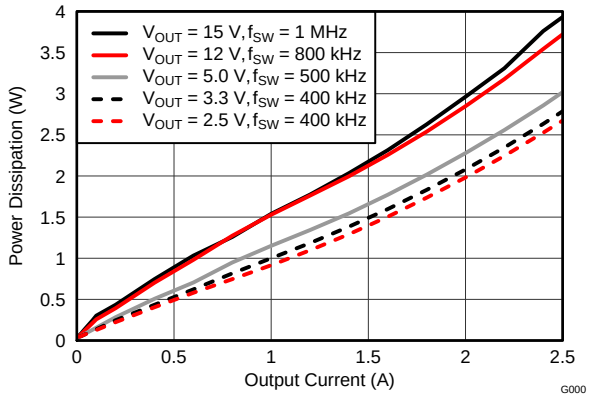


Figure 15. Power Dissipation vs. Output Current

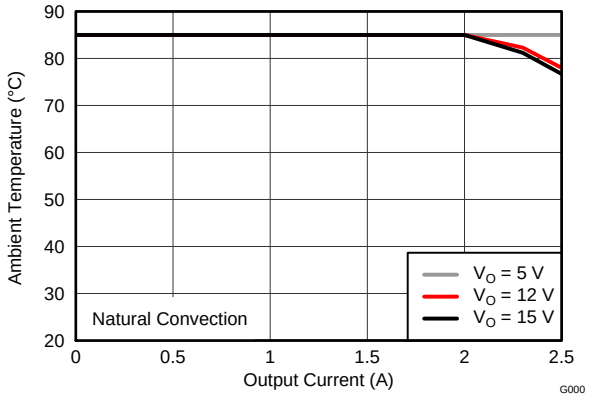


Figure 16. Safe Operating Area

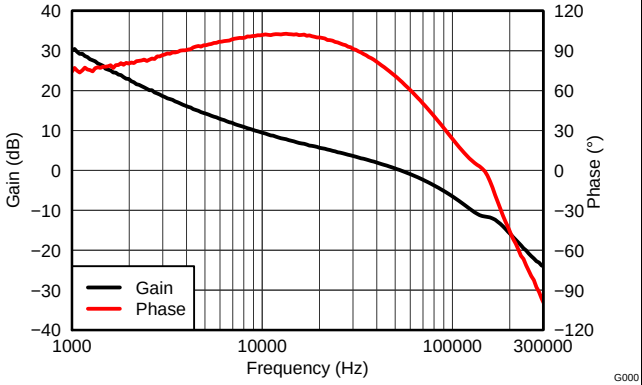


Figure 17. V_{OUT}= 5 V, I_{OUT}= 2 A, C_{OUT1}= 44 µF ceramic, C_{OUT2}= 56 µF electrolytic, f_{SW}= 500 kHz

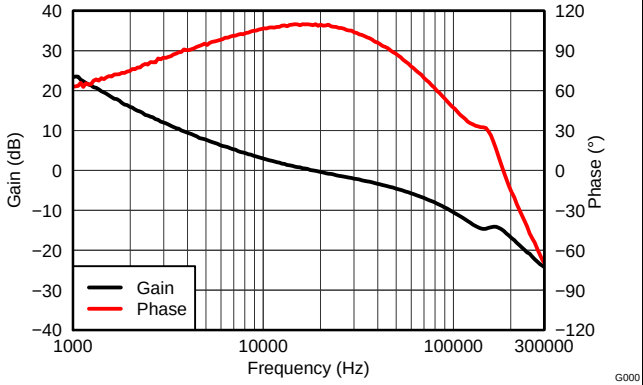


Figure 18. V_{OUT}= 12 V, I_{OUT}= 2 A, C_{OUT1}= 44 µF ceramic, C_{OUT2}= 56 µF electrolytic, f_{SW}= 800 kHz

(1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 13, Figure 14, and Figure 15.

(2) At light load the output voltage ripple may increase due to pulse skipping. See Light-Load Behavior for more information. Applies to Figure 14.

(3) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to devices soldered directly to a 100 mm × 100 mm double-sided PCB with 1 oz. copper. Applies to Figure 16.

9 TYPICAL CHARACTERISTICS (VIN = 48 V) (1) (2) (3)

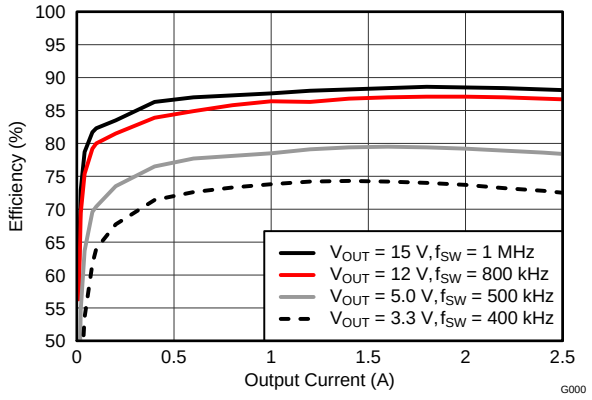


Figure 19. Efficiency vs. Output Current

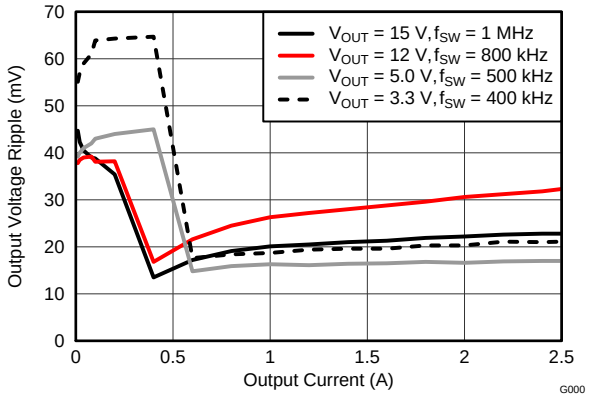


Figure 20. Voltage Ripple vs. Output Current

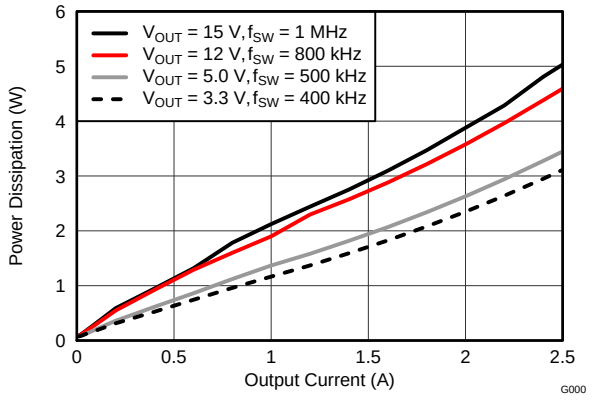


Figure 21. Power Dissipation vs. Output Current

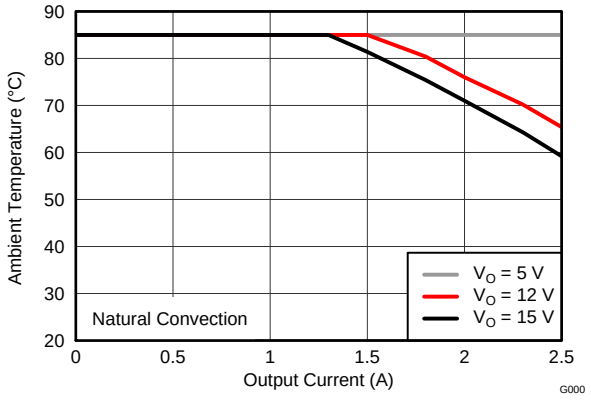


Figure 22. Safe Operating Area

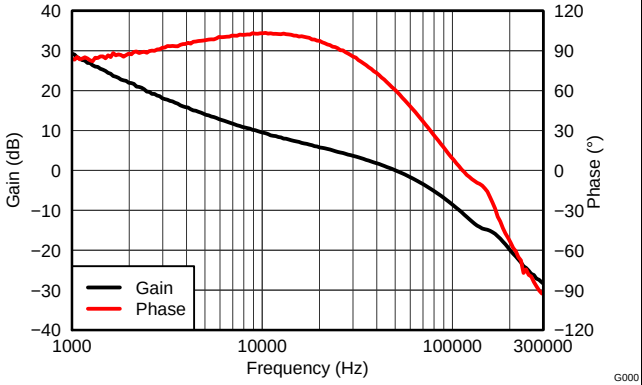


Figure 23. V_{OUT}= 5 V, I_{OUT}= 2 A, C_{OUT1}= 44 µF ceramic, C_{OUT2}= 56 µF electrolytic, f_{SW}= 500 kHz

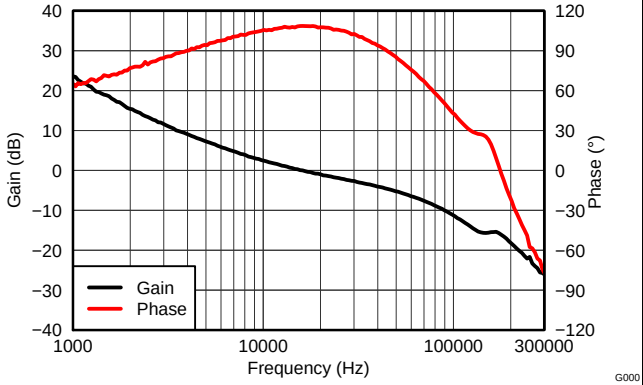


Figure 24. V_{OUT}= 12 V, I_{OUT}= 2 A, C_{OUT1}= 44 µF ceramic, C_{OUT2}= 56 µF electrolytic, f_{SW}= 800 kHz

(1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 19, Figure 20, and Figure 21.
(2) At light load the output voltage ripple may increase due to pulse skipping. See Light-Load Behavior for more information. Applies to Figure 20.
(3) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to devices soldered directly to a 100 mm × 100 mm double-sided PCB with 1 oz. copper. Applies to Figure 22.

10 CAPACITOR RECOMMENDATIONS FOR THE TPS84250 POWER SUPPLY

10.1 Capacitor Technologies

10.1.1 Electrolytic, Polymer-Electrolytic Capacitors

When using electrolytic capacitors, high-quality, computer-grade electrolytic capacitors are recommended. Polymer-electrolytic type capacitors are recommended for applications where the ambient operating temperature is less than 0°C. The Sanyo OS-CON capacitor series is suggested due to the lower ESR, higher rated surge, power dissipation, ripple current capability, and small package size. Aluminum electrolytic capacitors provide adequate decoupling over the frequency range of 2 kHz to 150 kHz, and are suitable when ambient temperatures are above 0°C.

10.1.2 Ceramic Capacitors

The performance of aluminum electrolytic capacitors is less effective than ceramic capacitors above 150 kHz. Multilayer ceramic capacitors have a low ESR and a resonant frequency higher than the bandwidth of the regulator. They can be used to reduce the reflected ripple current at the input as well as improve the transient response of the output.

10.1.3 Tantalum, Polymer-Tantalum Capacitors

Polymer-tantalum type capacitors are recommended for applications where the ambient operating temperature is less than 0°C. The Sanyo POSCAP series and Kemet T530 capacitor series are recommended rather than many other tantalum types due to their lower ESR, higher rated surge, power dissipation, ripple current capability, and small package size. Tantalum capacitors that have no stated ESR or surge current rating are not recommended for power applications.

10.2 Input Capacitor

The TPS84250 requires a minimum input capacitance of 4.4 µF of ceramic type. The voltage rating of input capacitors must be greater than the maximum input voltage. The ripple current rating of the capacitor must be at least 450 mArms. Table 3 includes a preferred list of capacitors by vendor.

10.3 Output Capacitor

The output capacitance of the TPS84250 can be comprised of either all ceramic capacitors, or a combination of ceramic and bulk capacitors. The required output capacitance must include at least 100 µF of ceramic type (or 2 x 47 µF). When adding additional non-ceramic bulk capacitors, low-ESR devices like the ones recommended in Table 3 are required. Additional capacitance above the minimum is determined by actual transient deviation requirements. Table 3 includes a preferred list of capacitors by vendor.

Table 3. Recommended Input/Output Capacitors(1)

VENDOR	SERIES	PART NUMBER	CAPACITOR CHARACTERISTICS		
			WORKING VOLTAGE (V)	CAPACITANCE (µF)	ESR (2) (mΩ)
Murata	X5R	GRM31CR61H225KA88L	50	4.7	2
TDK	X5R	C3216X5R1H475K	50	4.7	2
Murata	X5R	GRM32ER61E226K	16	22	2
TDK	X5R	C3225X5R0J476K	6.3	47	2
Murata	X5R	GRM32ER60J476M	6.3	47	2
Sanyo	POSCAP	16TQC68M	16	68	50
Sanyo	POSCAP	6TPE100MI	6.3	100	25
Kemet	T530	T530D227M006ATE006	6.3	220	6

(1) **Capacitor Supplier Verification, RoHS, Lead-free and Material Details**
Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in this table.
(2) Maximum ESR @ 100 kHz, 25°C.

11 APPLICATION INFORMATION

11.1 TPS84250 OPERATION

The TPS84250 can operate over a wide input voltage range of 7V to 50V and produce output voltages from 2.5V to 15V. The performance of the device varies over this wide operating range, and there are some important considerations when operated near the boundary limits. This section offers guidance in selecting the optimum components depending on the application and operating conditions.

The user must select three primary parameters when designing with the TPS84250.

- Output Voltage
- UVLO Threshold
- Switching Frequency

The adjustment of each of these parameters can be made using just one or two resistors. Figure 25 below shows a typical TPS84250 schematic with the key parameter-setting resistors labeled.

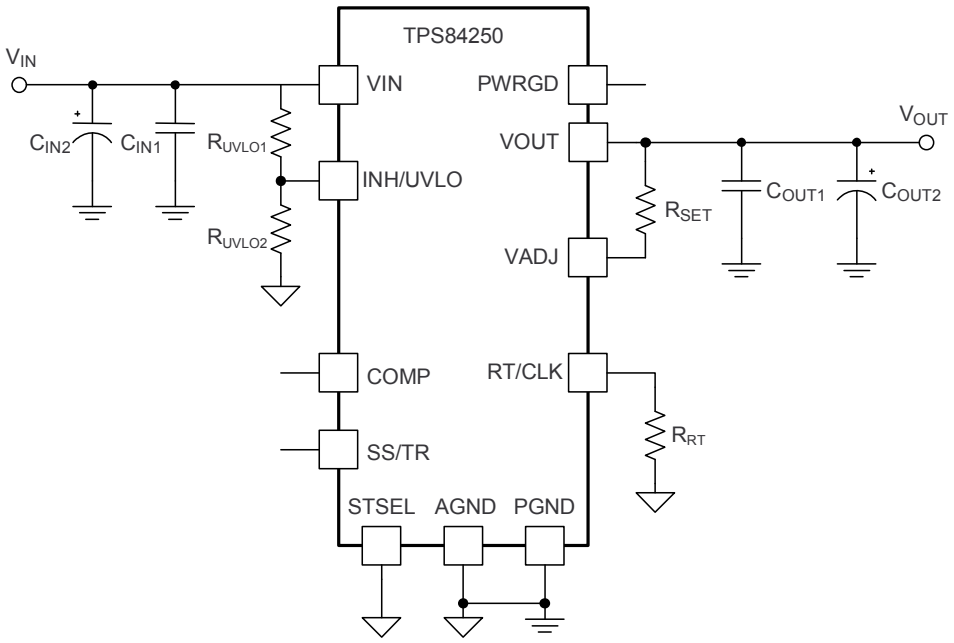


Figure 25. TPS84250 Typical Schematic

11.2 ADJUSTING THE OUTPUT VOLTAGE

The TPS84250 is designed to provide output voltages from 2.5V to 15V. The output voltage is determined by the value of R_{SET}, which must be connected between the VOUT node and the VADJ pin (Pin 36). For output voltages greater than 5.0V, improved operating performance can be obtained by increasing the operating frequency. This adjustment requires the addition of R_{RT} between RT/CLK (Pin 31) and AGND (Pin 30). See the Switching Frequency section for more details. Table 4 gives the standard external R_{SET} resistor for a number of common bus voltages and also includes the recommended R_{RT} resistor for output voltages above 5.0V.

Table 4. Standard R_{SET} Resistor Values for Common Output Voltages

RESISTORS	OUTPUT VOLTAGE V_{OUT} (V)					
	2.5	3.3	5.0	8.0	12.0	15.0
R_{SET} (kΩ)	21.5	31.6	52.3	90.9	140	178
R_{RT} (kΩ)	open	open	1100	549	267	178

For other output voltages the value of R_{SET} can be calculated using the following formula, or simply selected from the range of values given in Table 5.

$$R_{SET} = 10 \times \left(\frac{V_{OUT}}{0.798} - 1 \right) (k\Omega) \quad (1)$$

Table 5. Standard R_{SET} and R_{RT} Resistor Values

V_{OUT} (V)	R_{SET} (kΩ)	R_{RT}(kΩ)	f_{SW}(kHz)	V_{OUT} (V)	R_{SET} (kΩ)	R_{RT}(kΩ)	f_{SW}(kHz)
2.5	21.5	open	400	9.0	102	365	700
3.0	27.4	open	400	9.5	110	365	700
3.3	31.6	open	400	10.0	115	365	700
3.5	34.0	open	400	10.5	121	267	800
4.0	40.2	open	400	11.0	127	267	800
4.5	46.4	open	400	11.5	133	267	800
5.0	52.3	1100	500	12.0	140	267	800
5.5	48.7	1100	500	12.5	147	215	900
6.0	64.9	1100	500	13.0	154	215	900
6.5	71.5	1100	500	13.5	158	215	900
7.0	78.7	549	600	14.0	165	178	1000
7.5	84.5	549	600	14.5	174	178	1000
8.0	90.9	549	600	15.0	178	178	1000
8.5	97.6	365	700				

11.3 Input Voltage

The TPS84250 operates over the input voltage range of 7 V to 50 V. For reliable start-up and operation at light loads, the minimum input voltage depends on the output voltage. For output voltages ≤ 12V, the minimum input voltage is 7V or (VOUT + 3V), whichever is greater. For output voltages > 12V, the minimum input voltage is (1.33 x VOUT).

The maximum input voltage is (15 x VOUT) or 50 V, whichever is less.

While the device can safely handle input surge voltages up to 65 V, sustained operation at input voltages above 50 V is not recommended.

See the Undervoltage Lockout (UVLO) Threshold section of this datasheet for more information.

11.4 Undervoltage Lockout (UVLO) Threshold

At turn-on, the V_{ON} UVLO threshold determines the input voltage level where the device begins power conversion. During the power-down sequence, the V_{OFF} UVLO threshold determines the input voltage where power conversion ceases. The turn-on and turn-off thresholds are set by two resistors, R_{UVLO1} and R_{UVLO2} as shown in Figure 26.

The V_{ON} UVLO threshold must be set to at least (VOUT + 3 V) or 7 V whichever is greater to insure proper start-up and reduce current surges on the host input supply as the voltage rises. If possible, it is recommended to set the UVLO threshold to appproximantely 80 to 85% of the minimum expected input voltage.

Use Equation 2 and Equation 3 to calculate the values of R_{UVLO1} and R_{UVLO2}. V_{ON} is the voltage threshold during power-up when the input voltage is rising. V_{OFF} is the voltage threshold during power-down when the input voltage is decreasing. V_{OFF} should be selected to be at least 500mV less than V_{ON}. Table 6 lists standard resistor values for R_{UVLO1} and R_{UVLO2} for adjusting the V_{ON} UVLO threshold for several input voltages.

$$R_{UVLO1} = \frac{(V_{ON} - V_{OFF})}{2.9 \times 10^{-3}} \ (k\Omega) \tag{2}$$

$$R_{UVLO2} = \frac{1.25}{\left(\frac{(V_{ON} - 1.25)}{R_{UVLO1}}\right) + 0.9 \times 10^{-3}} \ (k\Omega) \tag{3}$$

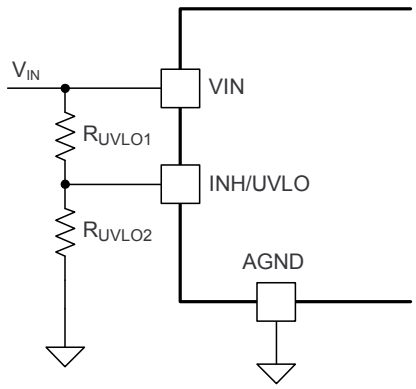


Figure 26. Adjustable VIN UVLO

Table 6. Standard Resistor Values to set V_{ON} UVLO Threshold

V_{ON} THRESHOLD (V)	6.5	10.0	15.0	20.0	25.0	30.0	35.0	40.0	45.0
R_{UVLO1} (kΩ)	174	174	174	174	174	174	174	174	174
R_{UVLO2} (kΩ)	40.2	24.3	15.8	11.5	9.09	7.50	6.34	5.62	4.99

11.5 Power Good (PWRGD)

The PWRGD pin is an open drain output. Once the output voltage is between 94% and 106% of the set voltage, the PWRGD pin pull-down is released and the pin floats. The recommended pull-up resistor value is between 10 kΩ and 100 kΩ to a voltage source that is 5.5 V or less. The PWRGD pin is in a defined state once VIN is greater than 1.0 V, but with reduced current sinking capability. The PWRGD pin achieves full current sinking capability once the VIN pin is above 4.5V. The PWRGD pin is pulled low when the output voltage is lower than 91% or greater than 109% of the nominal set voltage. Also, the PWRGD pin is pulled low if the input UVLO or thermal shutdown is asserted, the INH pin is pulled low, or the SS/TR pin is below 1.4 V.

11.6 Switching Frequency

Nominal switching frequency of the TPS84250 is set from the factory at 400 kHz. This switching frequency is optimum for output voltages below 5.0 V. For output voltages 5.0V and above, better operating performance can be obtained raising the operating frequency. This is easily done by adding a resistor, R_{RT} in , from the RT/CLK pin (Pin 31) to the AGND pin (Pin 30). Raising the operating frequency reduces output voltage ripple, lowers the load current threshold where pulse skipping begins, and improves transient response.

The recommended switching frequency for all output voltages is listed in Table 5.

For the maximum recommended output voltage value of 15 V, the switching frequency computes to 1000 kHz or 1 MHz. Operation above 1 MHz is not recommended. Use Table 7 below to select the value of the timing resistor for the given values of switching frequencies.

Table 7. Standard Resistor Values to set the Switching Frequency

f_{SW} (kHz)	400	500	600	700	800	900	1000
R_{RT}(kΩ)	OPEN	1100	549	365	267	215	178

It is also possible to synchronize the switching frequency to an external clock signal. See the Synchronization (CLK) section for further details.

While it is possible to set the operating frequency higher than 400 kHz when using the device at output voltages of 5 V or less, minimum duty cycle and pulse skipping issues restrict the maximum recommended input voltage under these conditions. The recommended operating conditions for the TPS84250 can be summarized by Figure 27. The graph shows the maximum input voltage vs. output voltage restriction for several operating frequencies. The lower boundary of the graph shows the minimum input voltage as a function of the output voltage.

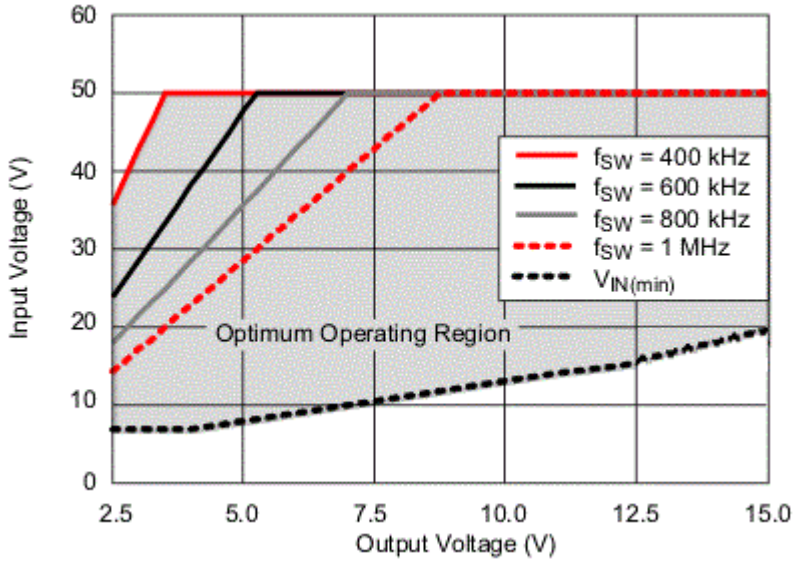


Figure 27. Optimum Operating Range with Switching Frequency

11.7 Application Schematics

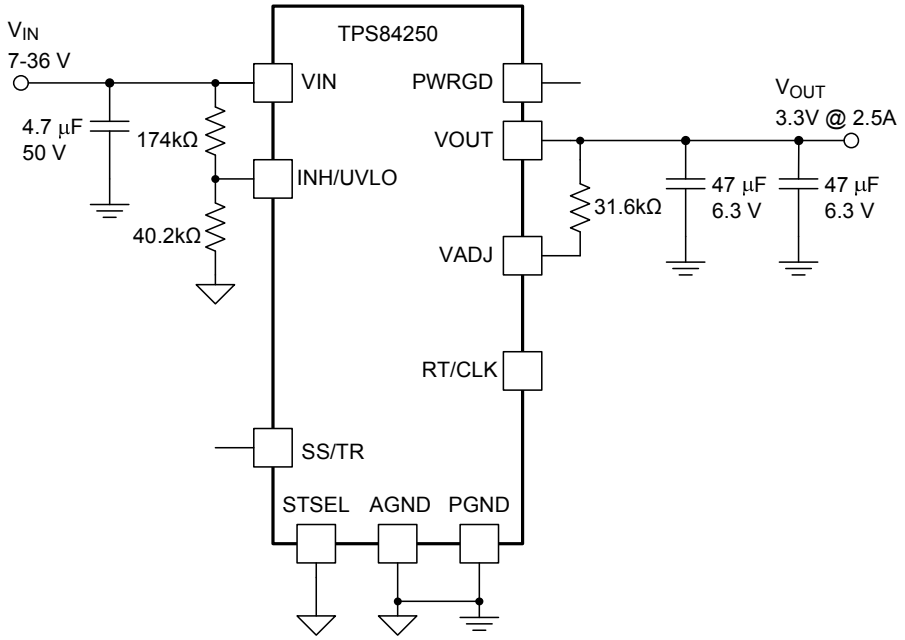


Figure 28. Typical Schematic
VIN = 7 V to 36 V, VOUT = 3.3 V

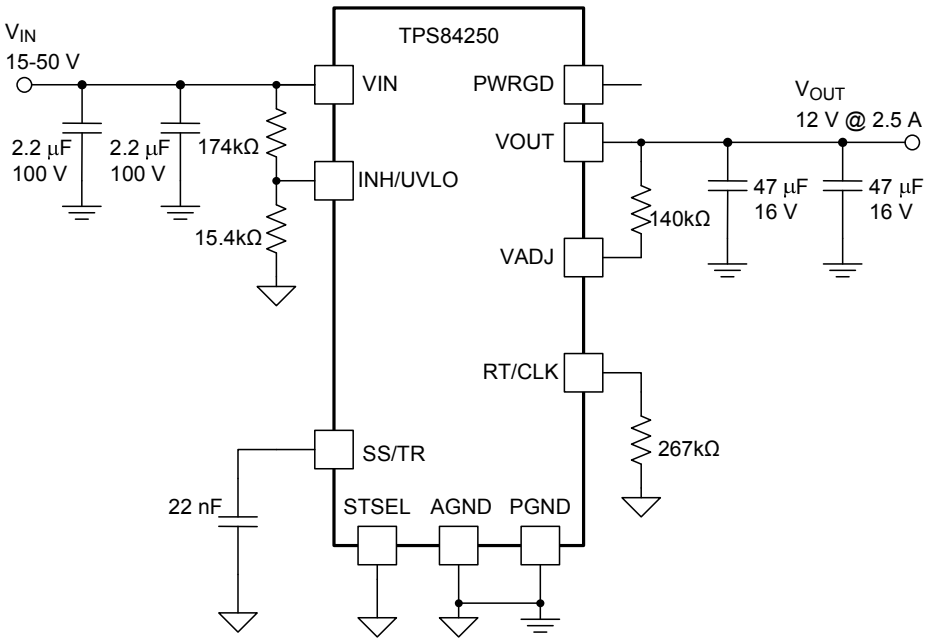


Figure 29. Typical Schematic
VIN = 15 V to 50 V, VOUT = 12 V

Application Schematics (continued)

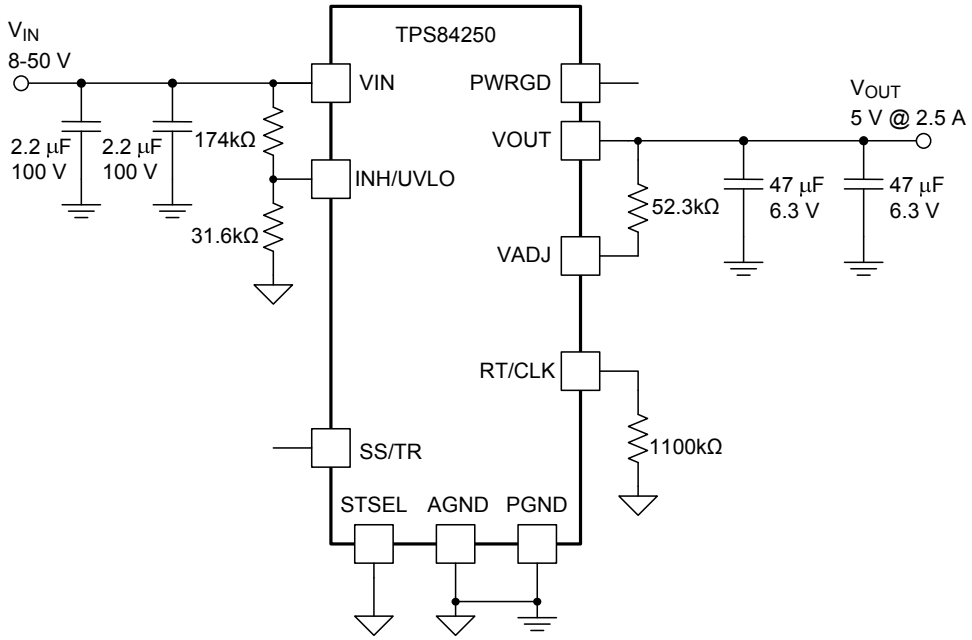


Figure 30. Typical Schematic
VIN = 8 V to 50 V, VOUT = 5 V

11.8 Power-Up Characteristics

When configured as shown in the front page schematic, the TPS84250 produces a regulated output voltage following the application of a valid input voltage. During the power-up, internal soft-start circuitry slows the rate that the output voltage rises, thereby limiting the amount of in-rush current that can be drawn from the input source. The soft-start circuitry introduces a short time delay from the point that a valid input voltage is recognized. Figure 31 shows the start-up waveforms for a TPS84250, operating from a 24-V input and the output voltage adjusted to 5 V. The waveform were measured with a 2-A constant current load.

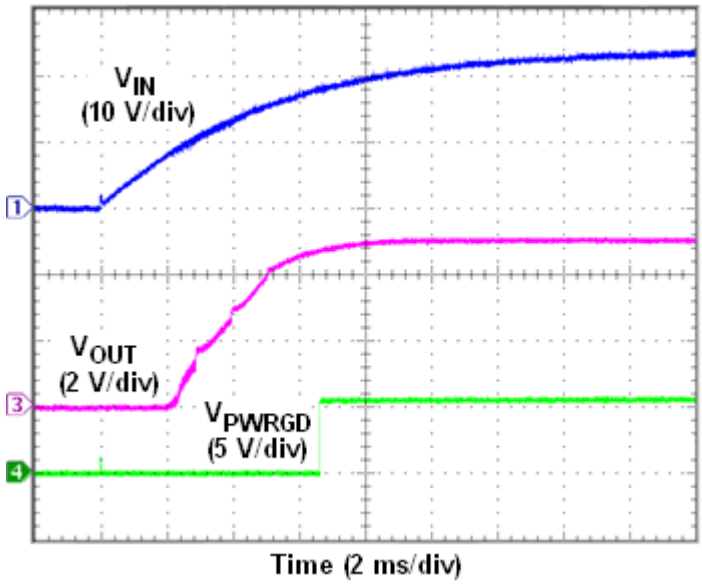


Figure 31. Start-Up Sequence

11.9 Output On/Off Inhibit (INH)

The INH pin provides electrical on/off control of the device. Once the INH pin voltage exceeds the threshold voltage, the device starts operation. If the INH pin voltage is pulled below the threshold voltage, the regulator stops switching and enters low quiescent current state.

The INH pin has an internal pull-up current source, allowing the user to float the INH pin for enabling the device. If an application requires controlling the INH pin, use an open drain/collector device, or a suitable logic gate to interface with the pin.

Figure 32 shows the typical application of the inhibit function. The Inhibit control has its own internal pull-up to VIN potential. An open-collector or open-drain device is recommended to control this input.

Turning Q1 on applies a low voltage to the inhibit control (INH) pin and disables the output of the supply, shown in Figure 33. If Q1 is turned off, the supply executes a soft-start power-up sequence, as shown in Figure 34. A regulated output voltage is produced within 5 ms. The waveforms were measured with a 2-A constant current load.

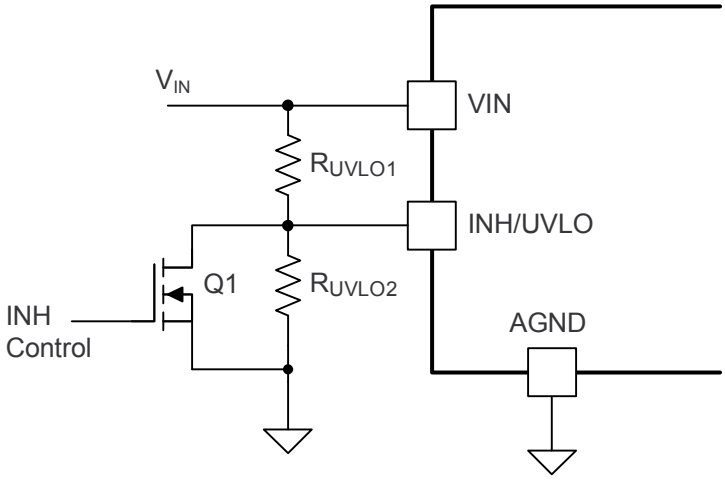


Figure 32. Typical Inhibit Control

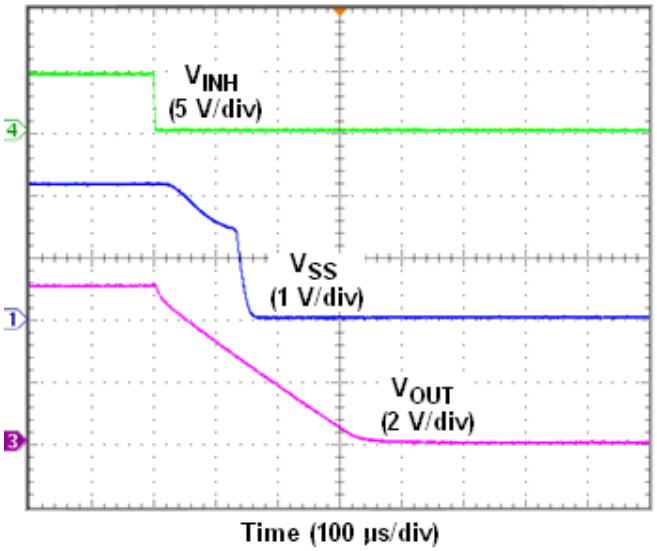


Figure 33. Inhibit Turn-Off

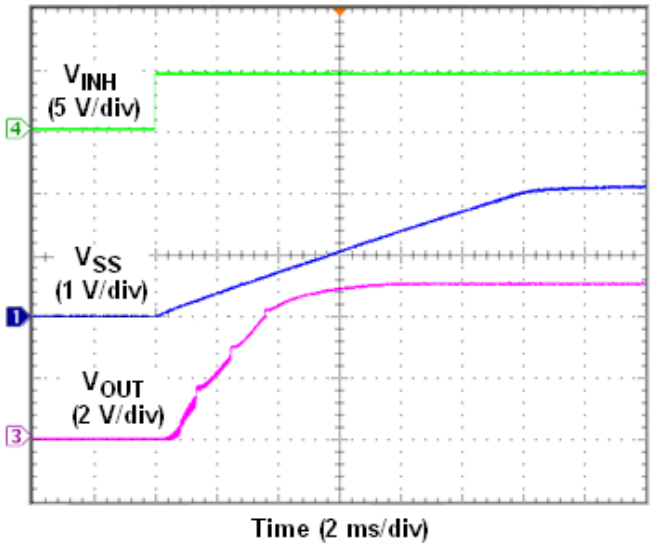


Figure 34. Inhibit Turn-On

11.10 Slow Start (SS/TR)

For outputs voltages of 5V or less, the slow start capacitance built into the TPS84250 is sufficient to provide for a turn-on ramp rate that does not induce large surge currents while charging the output capacitors. Connecting the STSEL pin (Pin 29) to AGND while leaving SS pin (Pin 28) open enables the internal SS capacitor with a slow start interval of approximately 5 ms. For output voltages greater than 5V, additional slow start capacitance is recommended. For 12V to 15V output voltages, a 22nF capacitor should be connected between the SS/TR pin (Pin 28) and AGND, while connecting the STSEL pin (Pin 29) to AGND as well. Figure 35 shows an additional SS capacitor connected to the SS pin and the STSEL pin connected to AGND. See Table 8 below for SS capacitor values and timing interval.

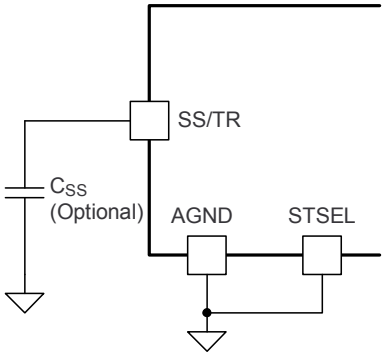


Figure 35. Slow Start Capacitor (C_{SS}) and STSEL Connection

Table 8. Slow Start Capacitor Values and Slow Start Time

C_{SS} (nF)	open	4.7	10	15	22
SS Time (msec)	5	7	10	13	17

11.11 Overcurrent Protection

For protection against load faults, the TPS84250 incorporates cycle-by-cycle current limiting. During an overcurrent condition the output current is limited and the output voltage is reduced, as shown in Figure 36. As the output voltage drops more than 8% below the set point, the PWRGD signal is pulled low. If the output voltage drops more than 25%, the switching frequency is reduced to reduce power dissipation within the device. When the overcurrent condition is removed, the output voltage returns to the established voltage.

The TPS84250 is not designed to endure a sustained short circuit condition. The use of an output fuse, voltage supervisor circuit, or other overcurrent protection circuit is recommended. A recommended overcurrent protection circuit is shown in Figure 37. This circuit uses the PWRGD signal as an indication of an overcurrent condition. As PWRGD remains low, the 555 timer operates as a low frequency oscillator, driving the INH/UVLO pin low for approximately 400ms, halting the power conversion of the device. After the inhibit interval, the INH/UVLO pin is released and the TPS84250 restarts. If the overcurrent condition is removed, the PWRGD signal goes high, resetting the oscillator and power conversion resumes, otherwise the inhibit cycle repeats.

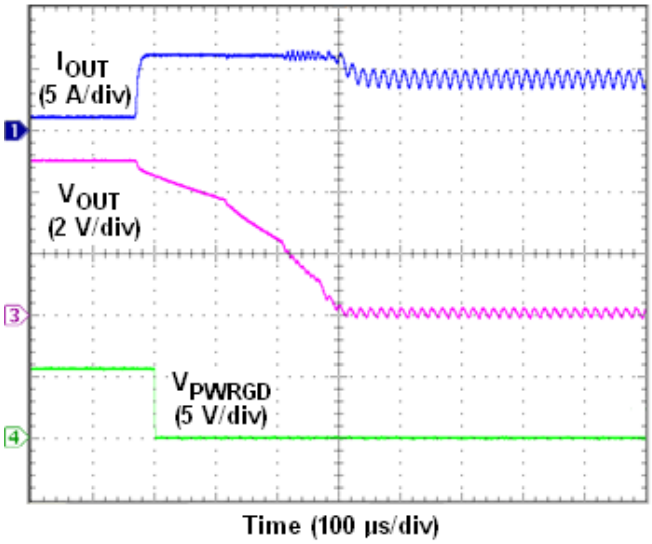


Figure 36. Overcurrent Limiting

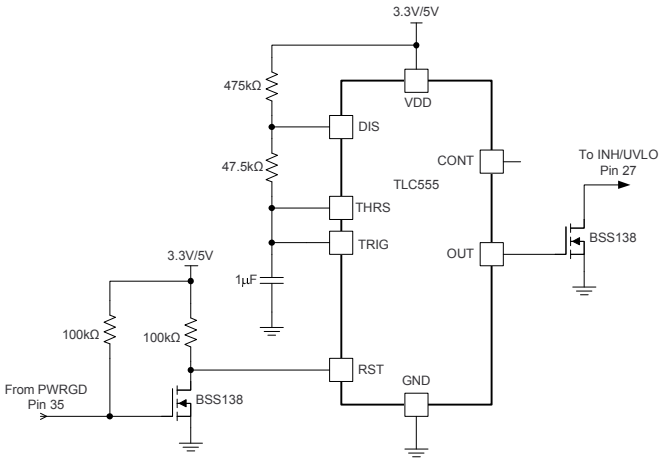


Figure 37. Over-Current Protection Circuit

11.12 Light-Load Behavior

The TPS84250 is a non-synchronous converter. One of the characteristics of a non-synchronous converter is that as the load current on the output is decreased, a point is reached where the energy delivered by a single switching pulse is more than the load can absorb. This causes the output voltage to rise slightly. This rise in output voltage is sensed by the feedback loop and the device responds by skipping one or more switching cycles until the output voltages falls back to the set point. At very light loads or no load, many switching cycles are skipped. The observed effect during this pulse skipping mode of operation is an increase in the peak to peak ripple voltage, and a decrease in the ripple frequency. The load current where pulse skipping begins is a function of the input voltage, the output voltage, and the switching frequency. A plot of the pulse skipping threshold current as a function of input voltage is given in Figure 38 for a number of popular output voltage and switching frequency combinations.

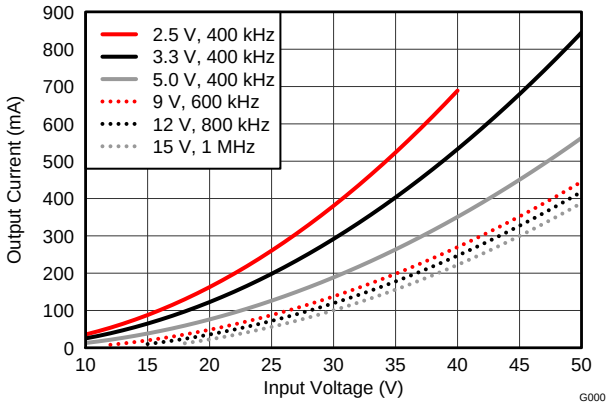


Figure 38. Pulse Skipping Threshold

11.13 Synchronization (CLK)

An internal phase locked loop (PLL) allows synchronization between 400 kHz and 1 MHz, and to easily switch from RT mode to CLK mode. To implement the synchronization feature, connect a square wave clock signal to the RT/CLK pin with a duty cycle between 20% to 80%. The clock signal amplitude must transition lower than 0.8 V and higher than 2.0 V. The start of the switching cycle is synchronized to the falling edge of RT/CLK pin. In applications where both RT mode and CLK mode are needed, the device can be configured as shown in Figure 39.

Before the external clock is present, the device works in RT mode where the switching frequency is set by the R_{RT} resistor. When the external clock is present, the CLK mode overrides the RT mode. The first time the CLK pin is pulled above the RT/CLK high threshold (2.0 V), the device switches from RT mode to CLK mode and the RT/CLK pin becomes high impedance as the PLL starts to lock onto the frequency of the external clock. It is not recommended to switch from CLK mode back to RT mode because the internal switching frequency drops to 100 kHz first before returning to the switching frequency set by the R_{RT} resistor .

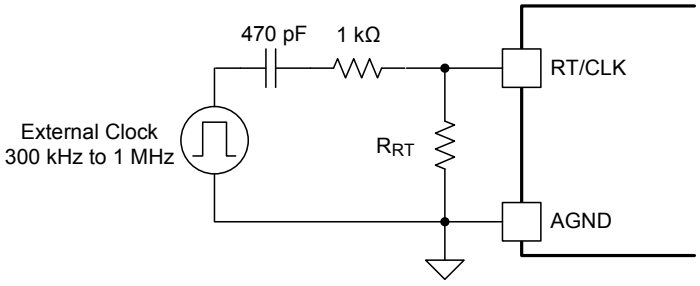


Figure 39. CLK/RT Configuration

11.14 Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 180°C typically. The device reinitiates the power up sequence when the junction temperature drops below 165°C typically.

11.15 Layout Considerations

To achieve optimal electrical and thermal performance, an optimized PCB layout is required. Figure 40 and Figure 41 show two layers of a typical PCB layout. Some considerations for an optimized layout are:

- Use large copper areas for power planes (VIN, VOUT, and PGND) to minimize conduction loss and thermal stress.
- Place ceramic input and output capacitors close to the module pins to minimize high frequency noise.
- Locate additional output capacitors between the ceramic capacitor and the load.
- Place a dedicated AGND copper area beneath the TPS84250.
- Isolate the PH copper area from the VOUT copper area using the PGND copper area.
- Connect the AGND and PGND copper area at one point; at pins 8 & 9.
- Place R_{SET}, R_{RT}, and C_{SS} as close as possible to their respective pins.
- Use multiple vias to connect the power planes to internal layers.
- Use a dedicated sense line to connect R_{SET} to VOUT near the load for best regulation.

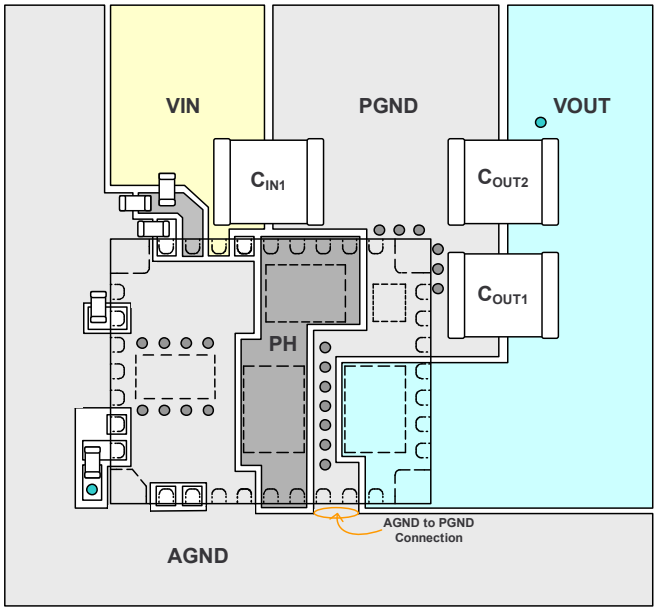


Figure 40. Typical Top-Layer Recommended Layout

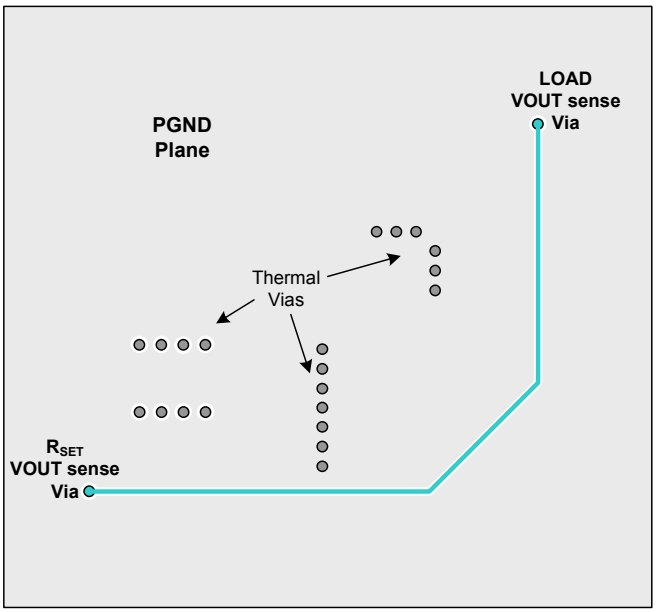


Figure 41. Typical PGND-Layer Recommended Layout

11.16 EMI

The TPS84250 is compliant with EN55022 Class B radiated emissions. Figure 42 and Figure 43 show typical examples of radiated emissions plots for the TPS84250 operating from 24 V and 12 V respectively. Both graphs include the plots of the antenna in the horizontal and vertical positions.

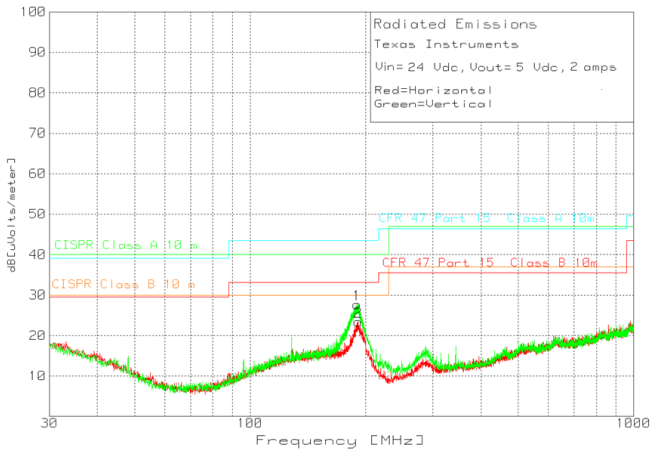


Figure 42. Radiated Emissions 24-V Input, 5-V Output, 2-A Load (EN55022 Class B)

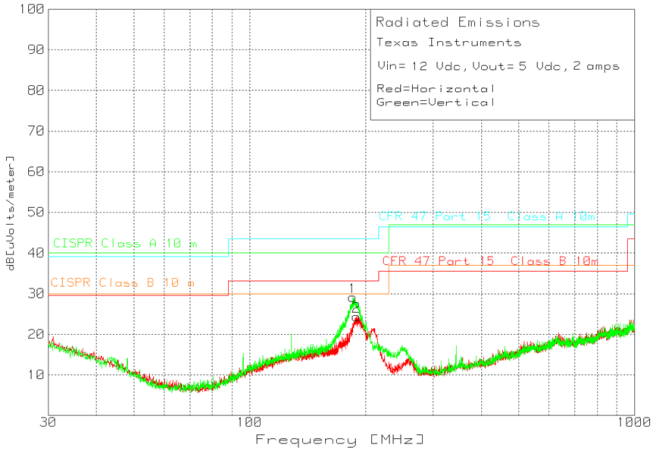


Figure 43. Radiated Emissions 12-V Input, 5-V Output, 2-A Load (EN55022 Class B)

12 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (June 2017) to Revision C **Page**

- Added top navigator icon for TI reference design 1
- Increased the peak reflow temperature and maximum number of reflows to JEDEC specification for improved manufacturability. 2

Changes from Revision A (June 2013) to Revision B **Page**

- Added peak reflow and maximum number of reflows information 2
- Added *Mechanical, Packaging, and Orderable Information* section..... 26

Changes from Original (August 2012) to Revision A **Page**

- Changed describing pins 8 & 9 not connected together internally. 6

13 Device and Documentation Support

13.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.5 Glossary

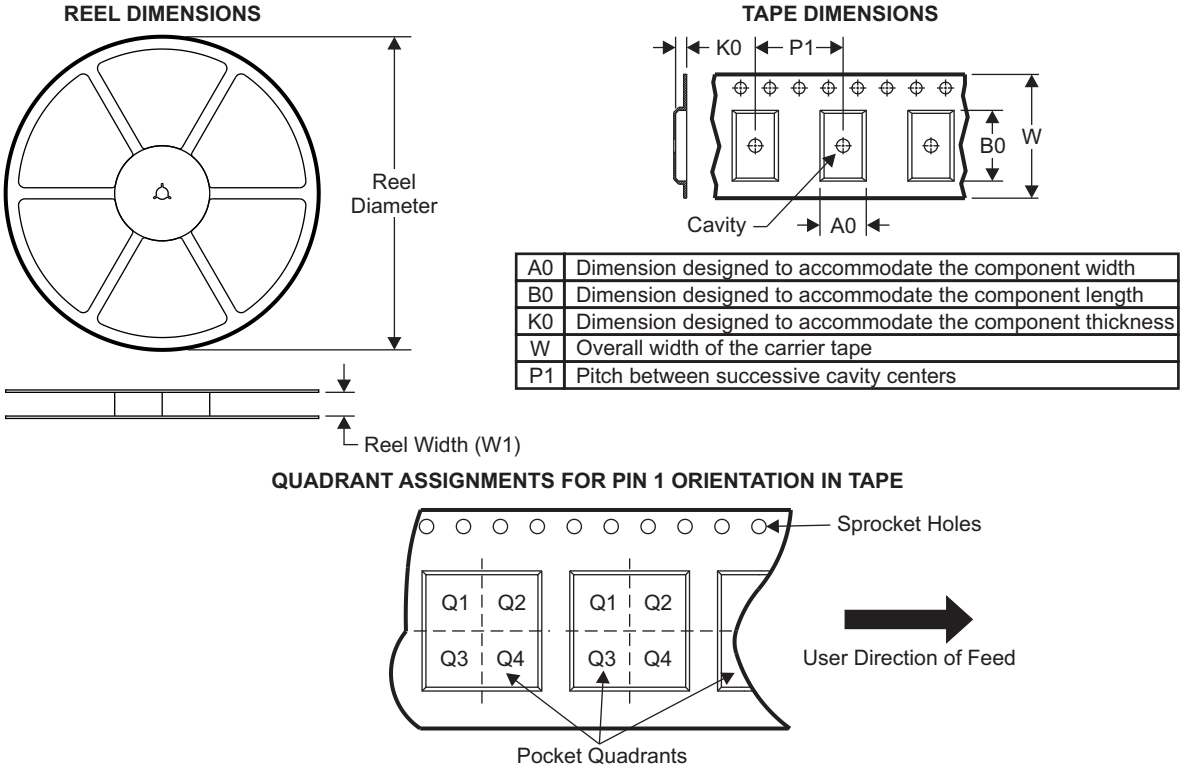
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

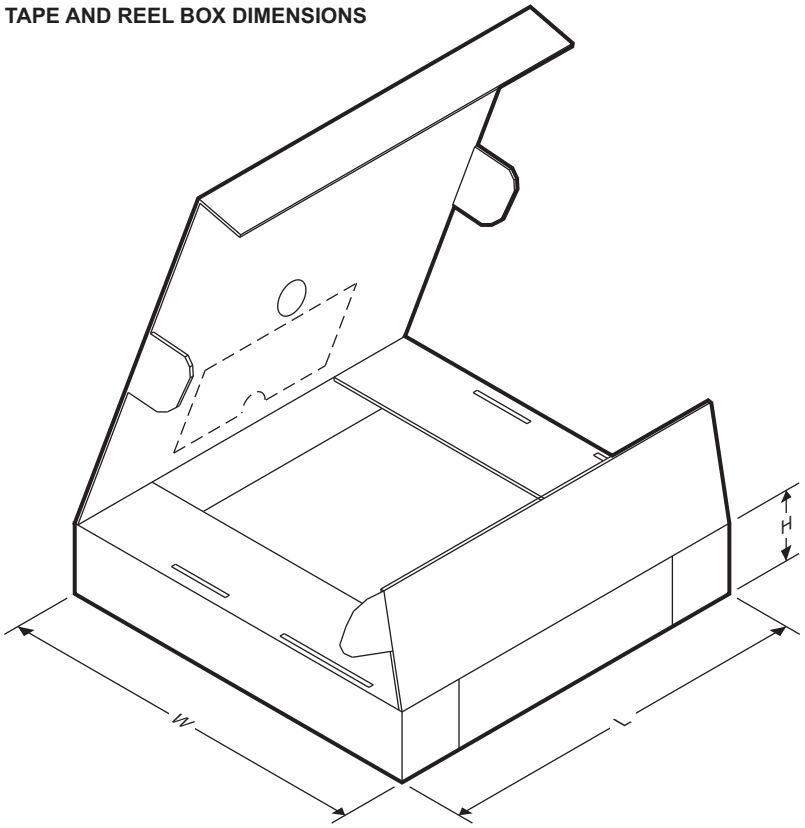
14.1 Tape and Reel Information



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS84250RKGR	B1QFN	RKG	41	500	330.0	24.4	9.35	11.35	3.1	16.0	24.0	Q1
TPS84250RKGT	B1QFN	RKG	41	250	330.0	24.4	9.35	11.35	3.1	16.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS84250RKGR	B1QFN	RKG	41	500	383.0	353.0	58.0
TPS84250RKGT	B1QFN	RKG	41	250	383.0	353.0	58.0

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS84250RKGR	Active	Production	B1QFN (RKG) | 41	500 | LARGE T&R	Exempt	NIPDAU	Level-3-250C-168 HR	-40 to 85	(54260, TPS84250)
TPS84250RKGR.A	Active	Production	B1QFN (RKG) | 41	500 | LARGE T&R	Exempt	NIPDAU	Level-3-250C-168 HR	-40 to 85	(54260, TPS84250)
TPS84250RKGRG4	Active	Production	B1QFN (RKG) | 41	500 | LARGE T&R	No	NIPDAU	Level-3-250C-168 HR	-40 to 85	TPS84250
TPS84250RKGRG4.A	Active	Production	B1QFN (RKG) | 41	500 | LARGE T&R	No	NIPDAU	Level-3-250C-168 HR	-40 to 85	TPS84250
TPS84250RKGRG4.B	Active	Production	B1QFN (RKG) | 41	500 | LARGE T&R	No	NIPDAU	Level-3-250C-168 HR	-40 to 85	TPS84250
TPS84250RKGT	Active	Production	B1QFN (RKG) | 41	250 | SMALL T&R	Exempt	NIPDAU	Level-3-250C-168 HR	-40 to 85	(54260, TPS84250)
TPS84250RKGT.A	Active	Production	B1QFN (RKG) | 41	250 | SMALL T&R	Exempt	NIPDAU	Level-3-250C-168 HR	-40 to 85	(54260, TPS84250)

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

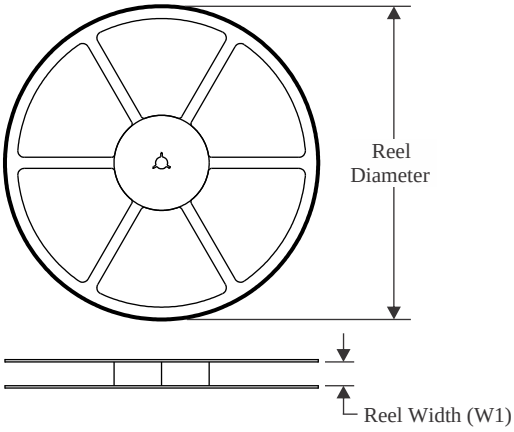
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

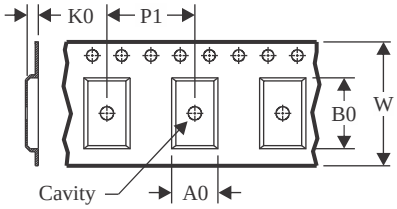
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

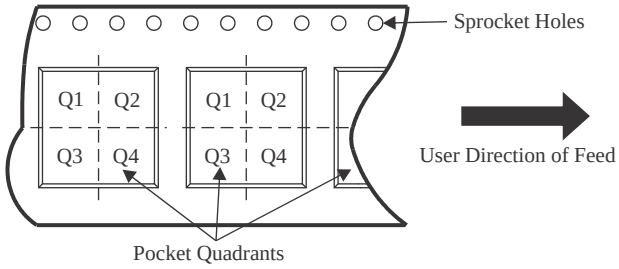


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

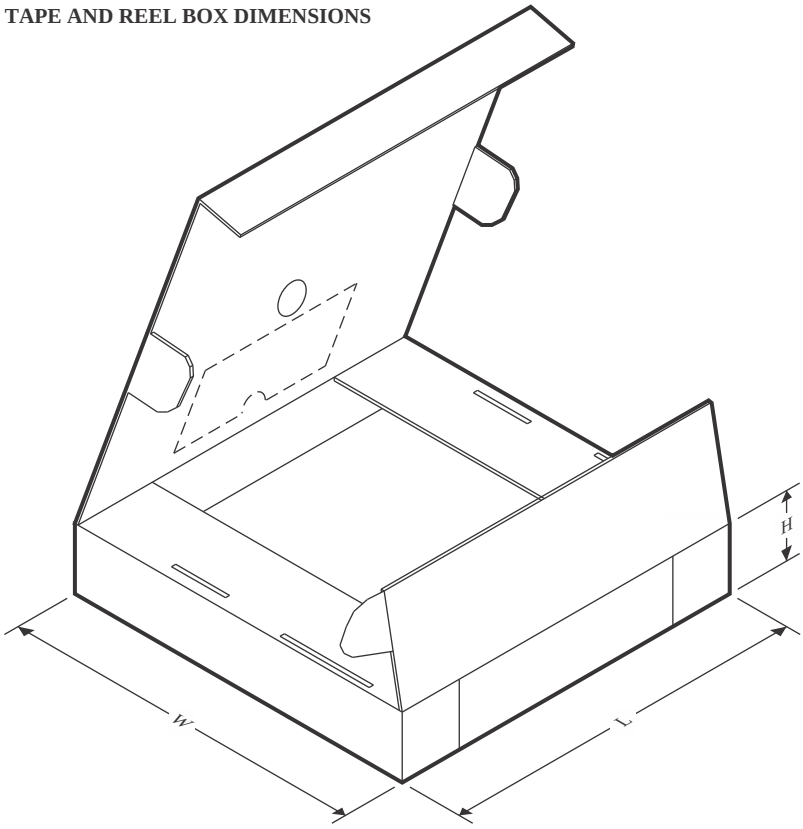
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS84250RKGR	B1QFN	RKG	41	500	330.0	24.4	9.35	11.35	3.1	16.0	24.0	Q1
TPS84250RKGRG4	B1QFN	RKG	41	500	330.0	24.4	9.35	11.35	3.1	16.0	24.0	Q1
TPS84250RKGT	B1QFN	RKG	41	250	330.0	24.4	9.35	11.35	3.1	16.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

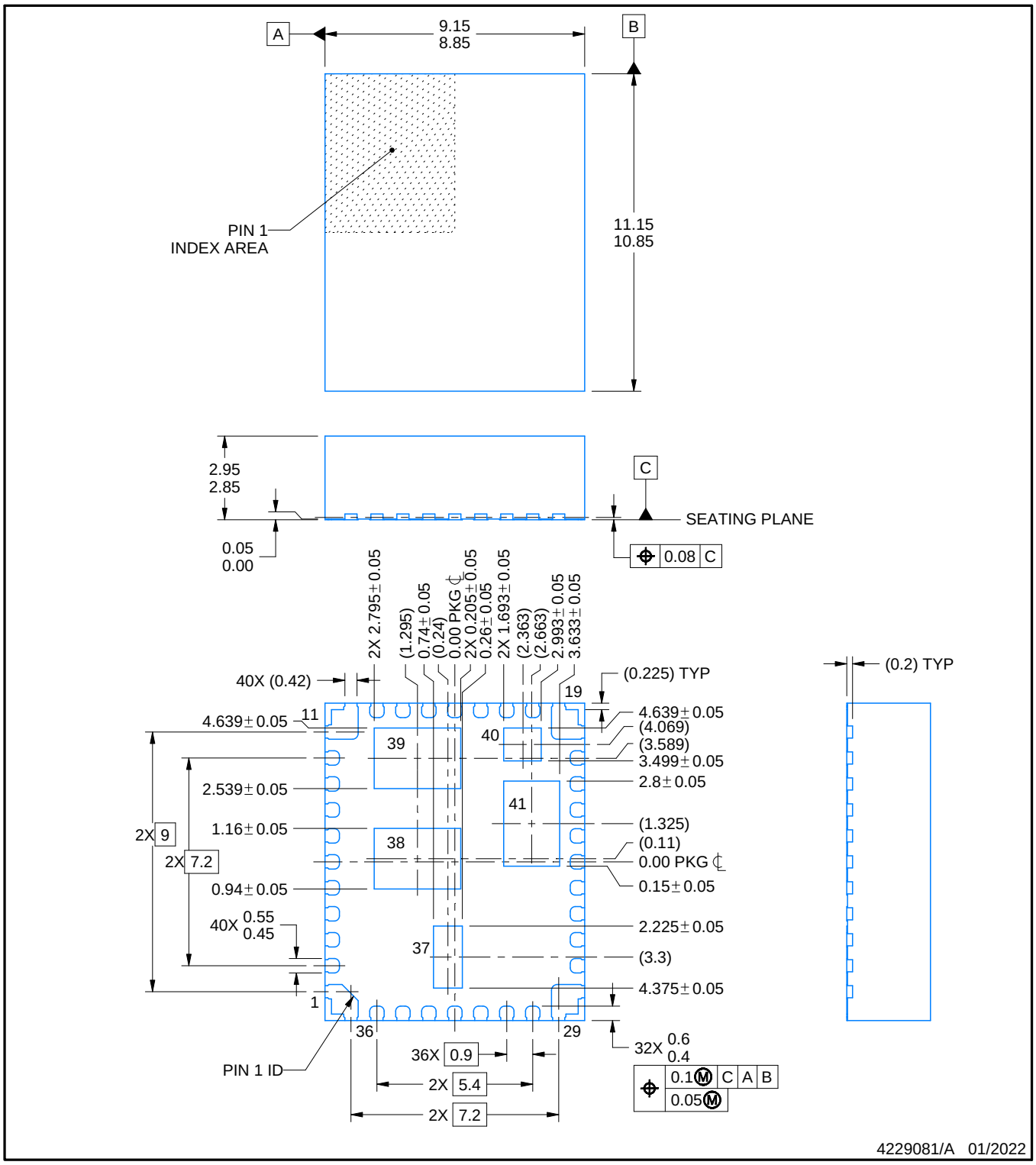
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS84250RKGR	B1QFN	RKG	41	500	383.0	353.0	58.0
TPS84250RKGRG4	B1QFN	RKG	41	500	383.0	353.0	58.0
TPS84250RKGT	B1QFN	RKG	41	250	383.0	353.0	58.0

PACKAGE OUTLINE

RKG0041A

B1QFN - 2.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

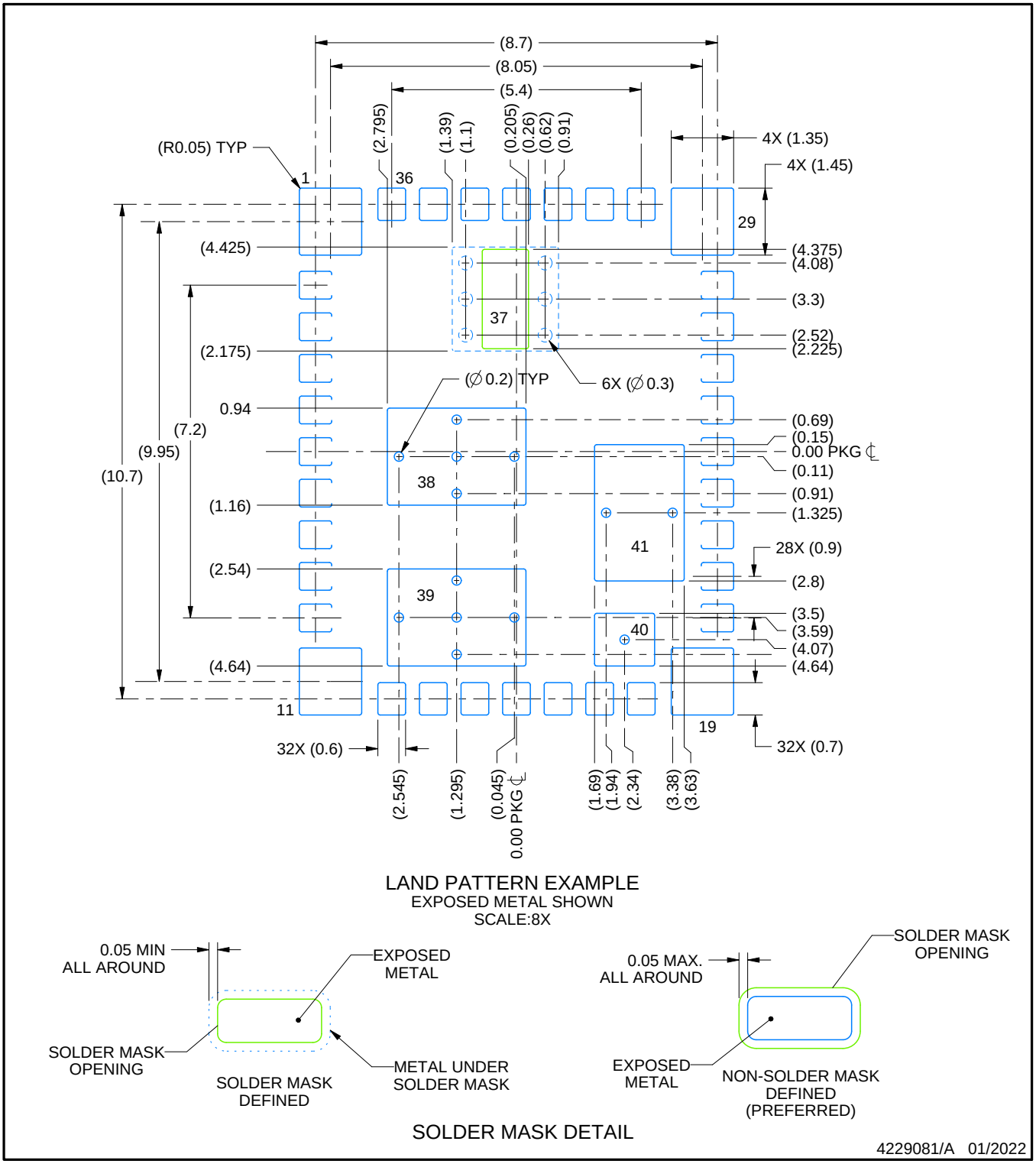
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pads must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RKG0041A

B1QFN - 2.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

SOLDER MASK DETAIL

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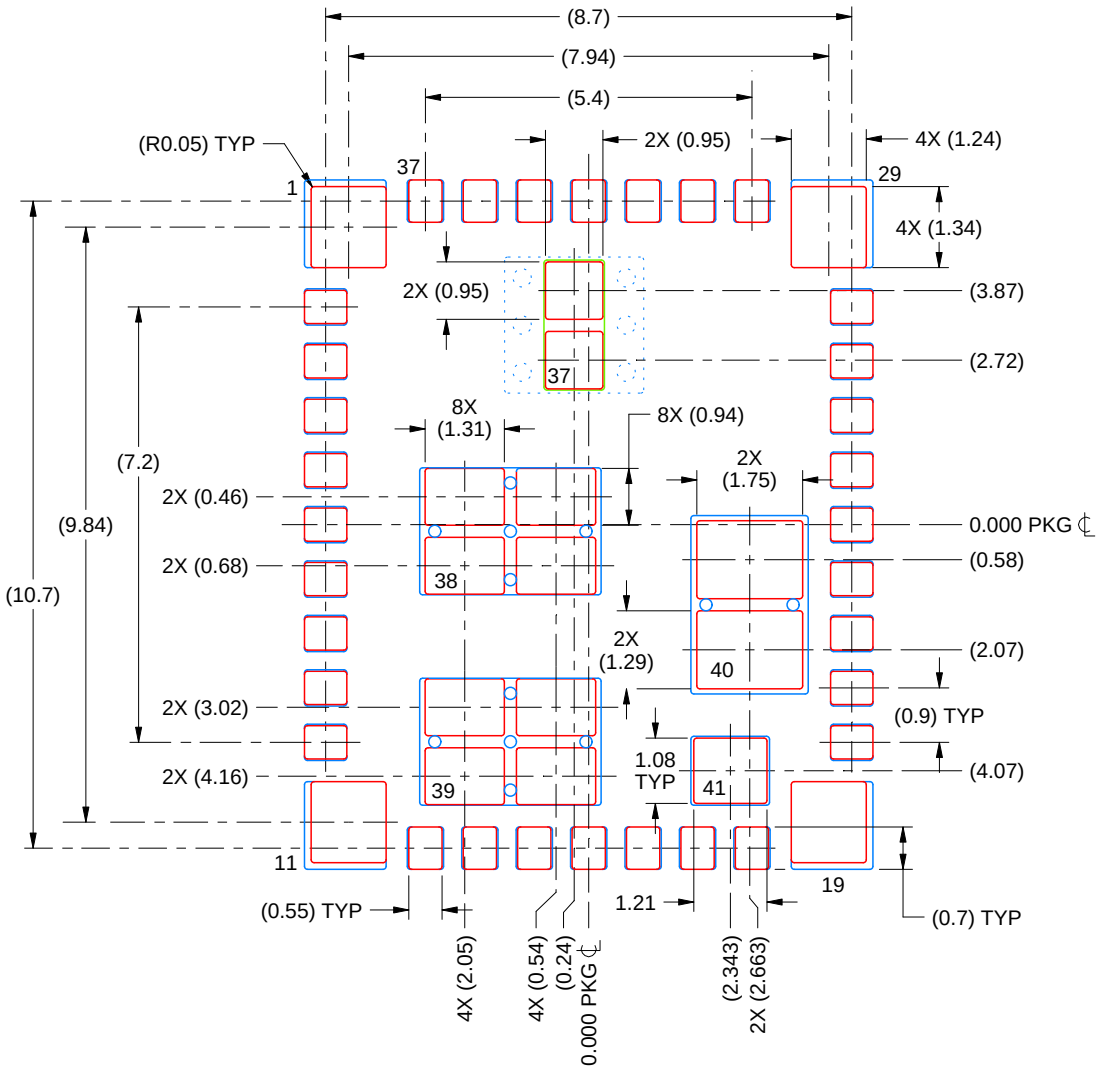
NOTES: (continued)

4. This package designed to be soldered to a thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE

BASED ON 0.1 mm STENCIL THICKNESS

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Last updated 10/2025