# TPS92310 Off-Line Primary Side Sensing Controller With PFC

**Check for Samples: TPS92310**

## FEATURES

- **Regulates LED Current Without Secondary Side Sensing**
- **Adaptive ON-Time Control With Inherent PFC**
- **Critical-Conduction-Mode (CRM) With Zero-Current Detection (ZCD) for Valley Switching**
- **Programmable Switch Turn ON Delay**
- **Programmable Constant ON-Time (COT) and Peak Current Control**
- **Over-Temperature Protection**

## APPLICATIONS

- **LED Lamps: A19 (E26/27, E14), PAR30/38, GU10**
- **Solid State Lighting**

## DESCRIPTION

The TPS92310 is an off-line controller specifically designed to drive high power LEDs for lighting applications. With the primary side sensing, constant on-time and quasi-resonant switching techniques, the TPS92310 application circuit gives high Power Factor, good EMI performance and high system efficiency. Also, using this device, low external component count application solutions can be designed easily. Power Factor Correction is inherent if the TPS92310 is operated in the constant on-time mode with an adaptive algorithm. The control algorithm of TPS92310 adjusts the on-time with reference to the primary side inductor peak current and secondary side inductor discharge time dynamically, the response time of which is set by an external capacitor. Also, minimized EMI and switching loss is achieved with quasi-resonant switching. Other supervisory features of the TPS92310 include cycle-by-cycle primary side inductor current limit, VCC under-voltage lockout, output over-voltage protection and thermal shutdown. The TPS92310 is available in the VSSOP-10 package.

### Typical Application

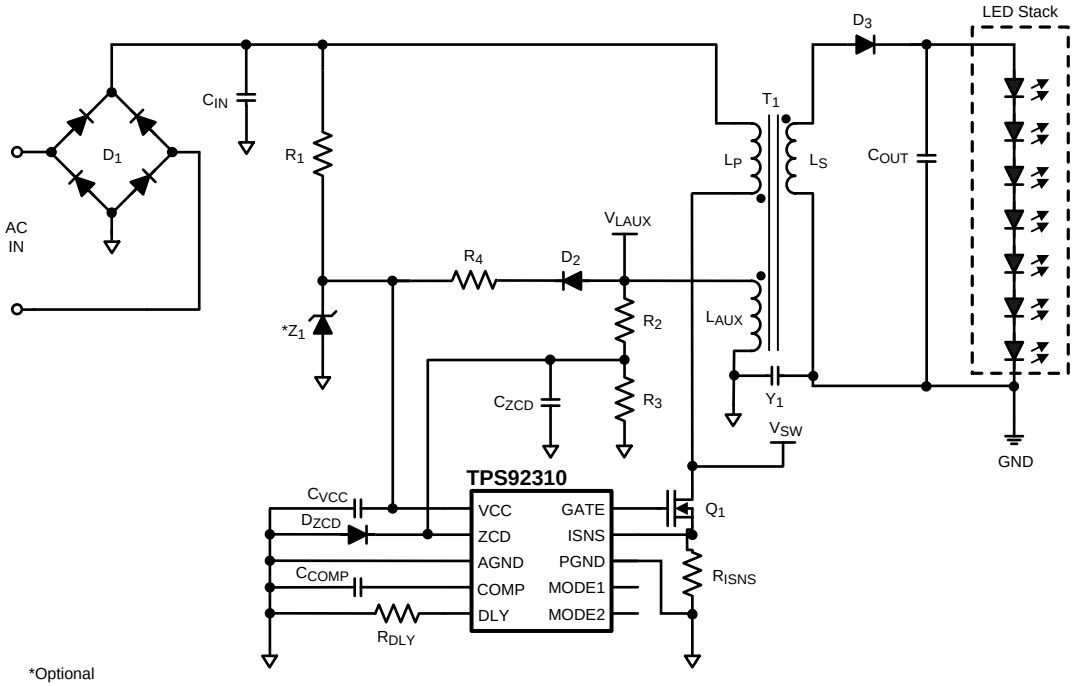



**Figure 1.**

## Connection Diagram

**Top View**

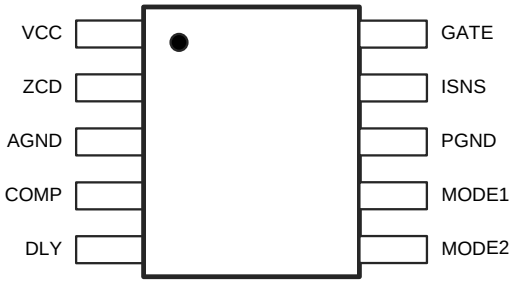



**Figure 2. 10-Pin VSSOP**

### Pin Descriptions

| Pin | Name | Description | Application Information |
|---|---|---|---|
| 1 | VCC | Power supply input | This pin provides power to the internal control circuitry and gate driver. Connect a 10µF capacitor from this pin to ground. |
| 2 | ZCD | Zero crossing detection input | The pin senses the voltage of the auxiliary winding for zero current detection. |
| 3 | AGND | Small signal ground | Signal ground. |
| 4 | COMP | Compensation network | Output of the error amplifier. Connect a capacitor from this pin to ground to set the frequency response of the LED current regulation loop. |
| 5 | DLY | Delay control input | Connect a resistor from this pin to ground to set the delay between switching ON and OFF periods. |
| 6 | MODE2 | Mode selection input 2 | Select operating mode for isolated or non-isolated mode. |
| 7 | MODE1 | Mode selection input 1 | Select operating mode for peak current mode or constant ON time. |
| 8 | PGND | Power ground | Power ground. This pin must be connected to the AGND pin externally for normal operation. This pin has no internal connection to PGND. |
| 9 | ISNS | Current sense voltage feedback | Switch current sensing input. |
| 10 | GATE | Gate driver output | Gate driving signal to the external switching MOSFET. |

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings(1)(2)

| | |
|---|---|
| VCC to GND | -0.3V to 40V |
| DLY, COMP, ZCD to GND | -0.3V to 7V |
| ISNS to GND | -0.3V to 7V |
| GATE to GND | -0.3V to 12V (5ns, –5V) |
| MODE1 to GND | -0.3V to 7V |
| MODE2 to GND | -0.3V to 7V |
| ESD Rating, HBM (3) | ±2 kV |
| Machine Model | 200V |
| Storage Temperature Range | -65°C to +125°C |
| Junction Temperature | +150°C |

(1) Absolute maximum ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is intended to be functional, but device parameter specifications may not be ensured. For ensured specifications and test conditions, see the Electrical Characteristics. All voltages are with respect to the potential at the GND pin, unless otherwise specified.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Human Body Model, applicable std. JESD22-A114-C.

## Operating Conditions

| | |
|---|---|
| Supply Voltage range VCC | 13V to 36V |
| Junction Temperature ($T_J$) | -40°C to +125°C |
| Thermal Resistance ($\theta_{JA}$) (1) | 120°C/W |

(1) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design. In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A-MAX}$) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application ($P_{D-MAX}$), and the junction-to ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (R_{\theta JA} \times P_{D-MAX})$.

## Electrical Characteristics

$V_{CC}$ = 18V unless otherwise indicated. Typicals and limits appearing in plain type apply for $T_A = T_J$ = +25°C. Limits appearing in **boldface** type apply over the full Operating Temperature Range. Data sheet minimum and maximum specification limits are specified by design, test or statistical analysis.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **SUPPLY VOLTAGE INPUT (VCC)** | | | | | | |
| $V_{CC-UVLO}$ | VCC Turn on threshold | | 23.4 / **23** | 25.6 | 27.8 / **29** | V |
| | VCCTurn off threshold | | 11.1 / **10.4** | 13 | 14.7 **/ 15.7** | V |
| | Hysteresis | | | 12.6 | | |
| $I_{STARTUP}$ | Startup Current | $V_{CC}$=$V_{CC-UVLO}$–3.0V | **10** | 12.5 | **14.75** | µA |
| $I_{VCC}$ | Operating supply current | Not switching | **0.9** | 1.2 | **1.5** | mA |
| | | 65kHz switching, $C_{LOAD}$ = 1nF | | 2 | | mA |
| **ZERO CROSS DETECT (ZCD)** | | | | | | |
| $I_{ZCD}$ | ZCD bias current | $V_{ZCD}$= 5V | | 0.1 | 1 | µA |
| $V_{ZCD-OVP}$ | ZCD over-voltage threshold | | **4.1** | 4.3 | **4.5** | V |
| $T_{OVP}$ | Over voltage de-bounce time | | | 3 | | cycle |
| $V_{ZCD-ARM}$ | ZCD Arming threshold | $V_{ZCD}$ = Increasing | **1.16** | 1.24 | **1.3** | V |
| $V_{ZCD-TRIG}$ | ZCD Trigger threshold | $V_{ZCD}$ = Decreasing | **0.48** | 0.6 | **0.77** | V |
| $V_{ZCD-HYS}$ | ZCD Hysteresis | $V_{ZCD-ARM}$-$V_{ZCD-TRIG}$ | | 0.64 | | V |

## Electrical Characteristics (continued)

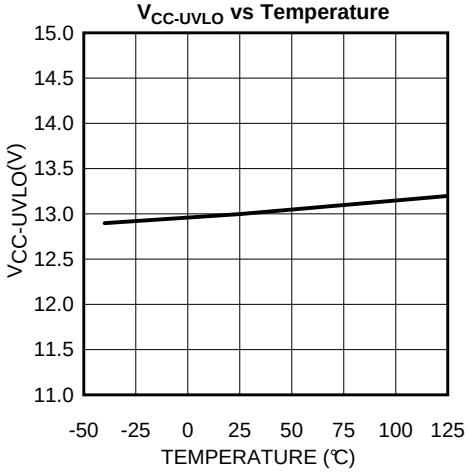
$V_{CC}$ = 18V unless otherwise indicated. Typicals and limits appearing in plain type apply for $T_A = T_J$ = +25°C. Limits appearing in **boldface** type apply over the full Operating Temperature Range. Data sheet minimum and maximum specification limits are specified by design, test or statistical analysis.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **COMPENSATION (COMP)** | | | | | | |
| $I_{COMP-SOURCE}$ | Internal reference current for primary side current regulation | $V_{COMP}$ = 2.0V, $V_{ISNS}$ = 0V, Measure at COMP pin | | 27 | | µA |
| $gm_{ISNS}$ | ISNS error amp transconductance | Δ $V_{ISNS}$ to Δ $I_{COMP}$ @ $V_{COMP}$ = 2.5V | | 100 | | µmho |
| $V_{COMP}$ | COMP operating range | | 2.0 | | 3.5 | V |
| **DELAY CONTROL (DLY)** | | | | | | |
| $V_{DLY}$ | DLY pin internal reference voltage | | **1.21** | 1.23 | **1.26** | V |
| $I_{DLY-MAX}$ | DLY source current | $V_{DLY}$= 0V | **250** | | | µA |
| **CURRENT SENSE (ISNS)** | | | | | | |
| $V_{ISNS-OCP}$ | Over Current Detection Threshold | Non isolation mode | 0.59 | 0.64 | 0.68 | V |
| $V_{ISNS-OCP}$ | Over Current Detection Threshold | Isolation mode | 3.2 | 3.4 | 3.6 | V |
| $I_{ISNS}$ | Current Sense Bias Current | $V_{ISNS}$= 5V | -1 | | 1 | µA |
| $T_{OCP}$ | Over current Detection Propagation Delay | Measure GATE pulse width at $V_{ISNS}$ = 5V | | 210 | | ns |
| **GATE DRIVER (GATE)** | | | | | | |
| $V_{GATE-H}$ | GATE high drive voltage | $I_{GATE}$ = 50mA source | **8** | 9.4 | **11.86** | V |
| $V_{GATE-L}$ | GATE low drive voltage | $I_{GATE}$ = 50mA sink | **28** | 80 | **167** | mV |
| $T_{ON-MIN}$ | Minimum ON time | | **360** | 540 | **720** | ns |
| $T_{OFF-MAX}$ | Maximum OFF time | ZCD = GND | **50** | 72 | **94** | µs |
| $t_{GATE-RISE}$ | Rise time | $C_{LOAD}$ = 1nF | | 110 | | ns |
| $t_{GATE-FALL}$ | Fall time | $C_{LOAD}$ = 1nF | | 20 | | ns |
| **THERMAL SHUTDOWN** | | | | | | |
| TSD | Thermal shutdown temperature (1) | | | 165 | | °C |
| | Thermal Shutdown hysteresis | | | 20 | | °C |

(1) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at $T_J$ = 165°C (typ.) and disengages at $T_J$ = 145°C (typ).

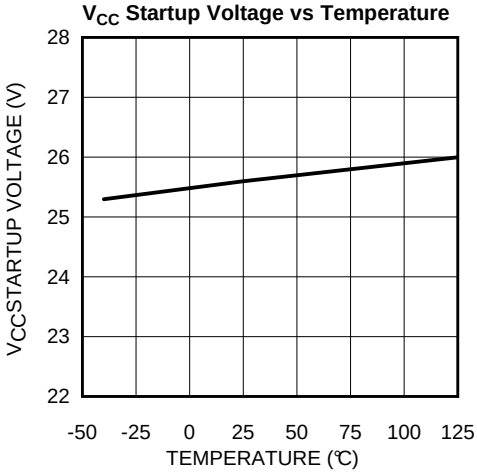
## Typical Performance Characteristics

All curves taken at $V_{CC}$=18V with configuration in typical application for driving seven power LEDs with $I_{LED}$=350mA shown in this datasheet. $T_A$=25°C, unless otherwise specified.



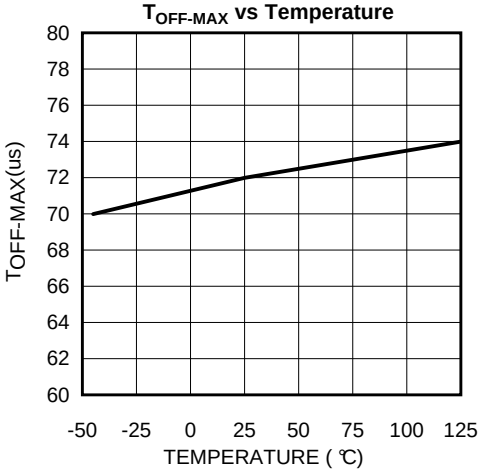

**$V_{CC-UVLO}$ vs Temperature**

**Figure 3.**



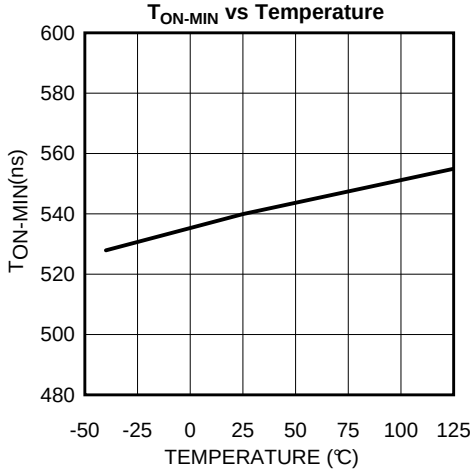

**$V_{CC}$ Startup Voltage vs Temperature**

**Figure 4.**



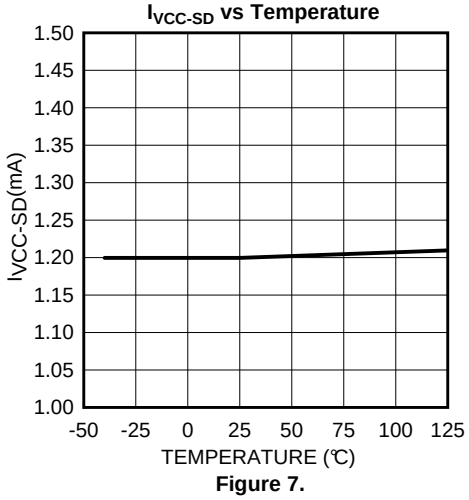

**$T_{OFF-MAX}$ vs Temperature**

**Figure 5.**



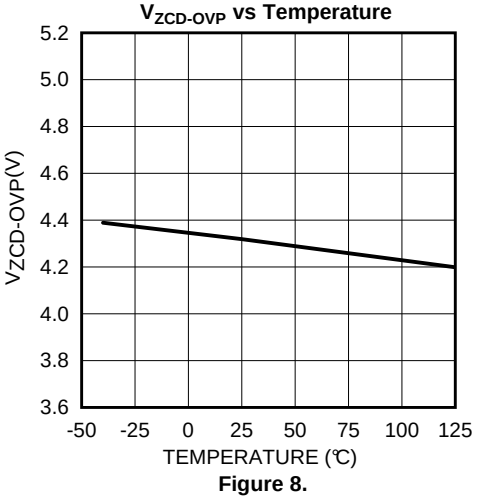

**$T_{ON-MIN}$ vs Temperature**

**Figure 6.**




**$I_{VCC-SD}$ vs Temperature**

**Figure 7.**




**$V_{ZCD-OVP}$ vs Temperature**

**Figure 8.**

## Typical Performance Characteristics (continued)

All curves taken at $V_{CC}$=18V with configuration in typical application for driving seven power LEDs with $I_{LED}$=350mA shown in this datasheet. $T_A$=25°C, unless otherwise specified.

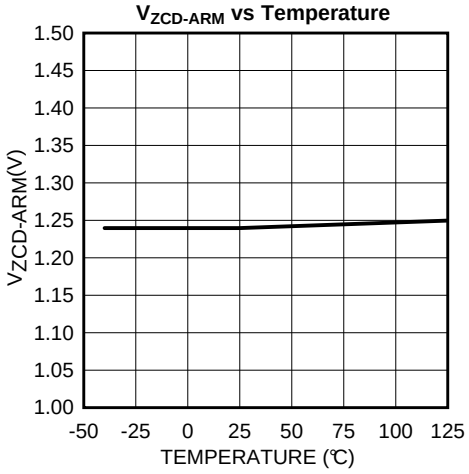



**Figure 9.**

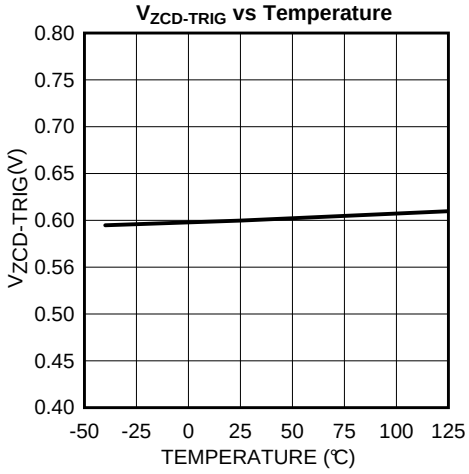



**Figure 10.**

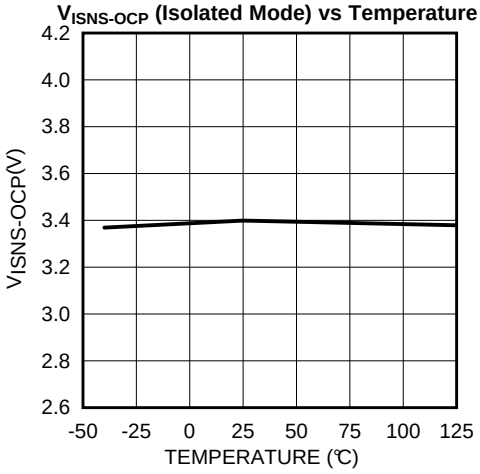



**Figure 11.**

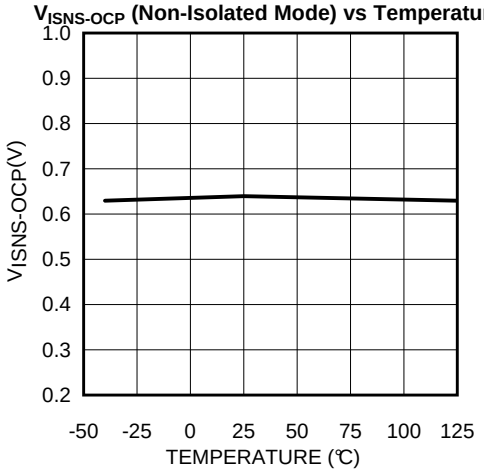



**Figure 12.**

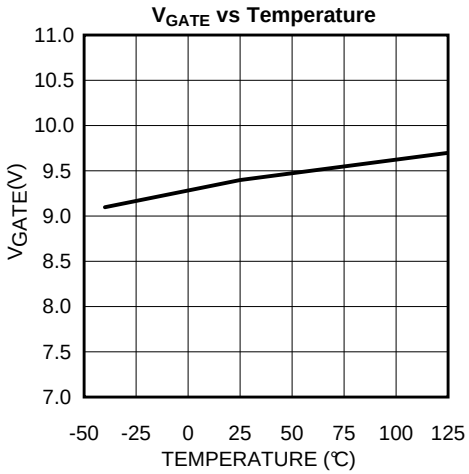



**Figure 13.**

## SIMPLIFIED INTERNAL BLOCK DIAGRAM

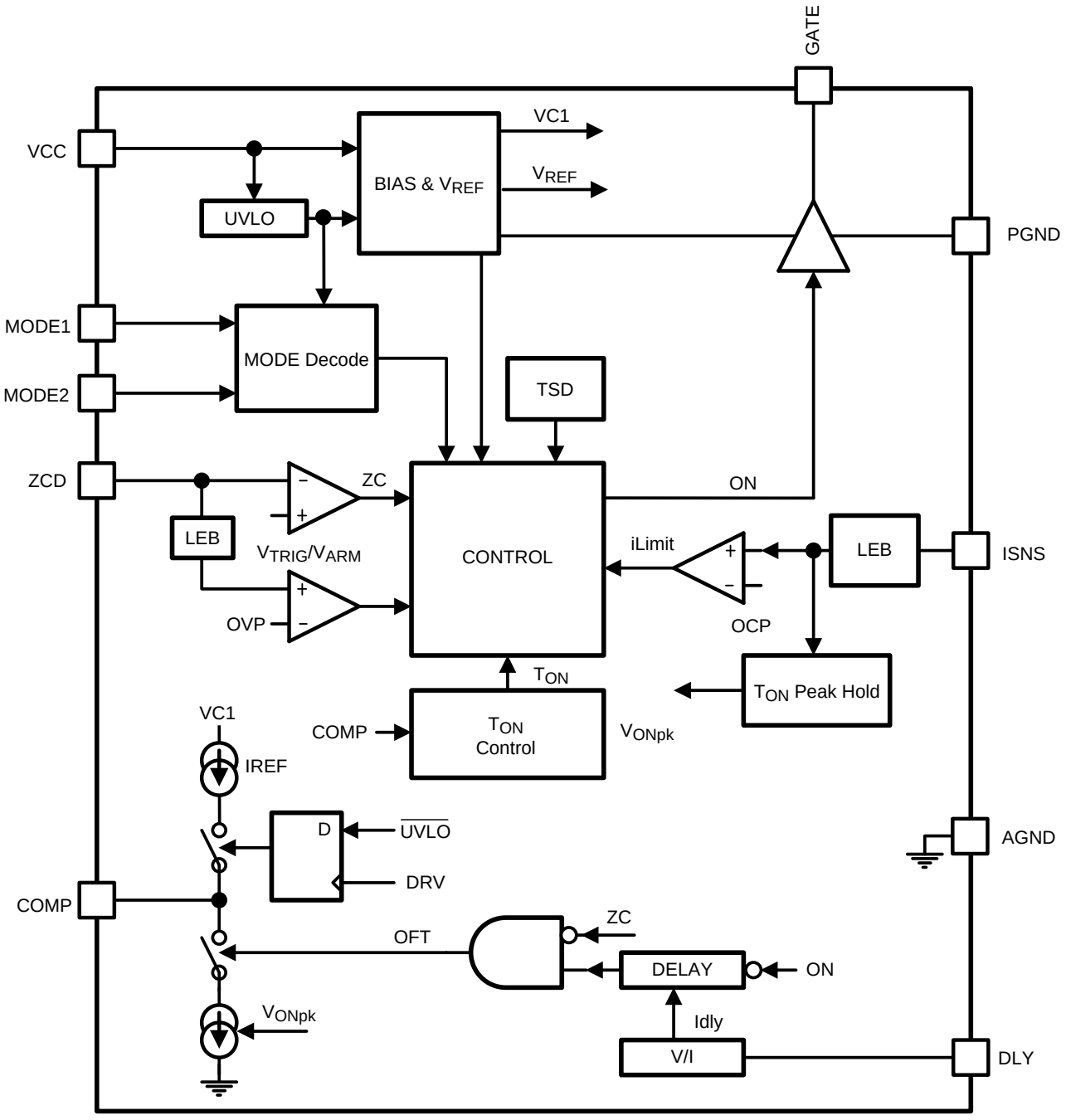



**Figure 14. Simplified Block Diagram**

## Application Information

The TPS92310 is an off-line controller specifically designed to drive LEDs with inherent Power Factor Correction (PFC). This device operates in Critical Conduction Mode (CRM) with adaptive Constant ON-Time control, so that high power factor can be achieved naturally. The TPS92310 can be used in isolated and non-isolated off-line applications that cover most requirements for LED lighting applications. A typical application schematic is shown in Figure 1. On the primary side, the off-line flyback converter consists of a transformer which includes three windings $L_P$, $L_S$ and $L_{AUX}$, an external MOSFET $Q_1$ and inductor current sensing resistor $R_{ISNS}$. On the output side, the $L_S$ winding, the output diode $D_3$, the output capacitor $C_{OUT}$ and a LED string connected as the load. Additionally, an auxiliary supply circuit to power the TPS92310 after start-up with $L_{AUX}$ output is implemented. The $L_{AUX}$ output voltage, $V_{LAUX}$ is also used to detect the zero crossing point due to the end of a complete switching cycle. During the on-period, $Q_1$ is turned on, the AC line input is rectified by the input bridge rectifier $D_1$ and input capacitor $C_{IN}$ and current flows through $L_P$, $Q_1$ and $R_{ISNS}$ to ground, input energy is stored in the primary inductor $L_P$. Simultaneously, the ISNS pin of the device monitors the voltage of the current sensing resistor $R_{ISNS}$ to perform the cycle-by-cycle inductor current limit function. While the MOSFET $Q_1$ turned off, current flow in $L_P$ ceased and the energy stored during the on cycle is released to output and auxiliary circuits. The current in the secondary winding $L_S$ charges the output capacitor $C_{OUT}$ through $D_3$ and supplies the LED load, the $C_{OUT}$ also responsible to supply current to LED load during subsequent on-period. The current flows through $L_{AUX}$ powers the TPS92310 through $D_2$ and $C_{VCC}$ in steady state operation. The voltage across $L_{AUX}$, $V_{LAUX}$ is fed back to the ZCD pin through a resistor divider network formed by $R_2$ and $R_3$ to perform zero crossing detection of $V_{LAUX}$, which determines the end of the off-period of a switching cycle. The next on-period of a new cycle will be initiated after an inserted delay of 2 x $t_{DLY}$, the $t_{DLY}$ is programmable by a single resistor connecting the DLY pin and ground. The setting of the delay time, $t_{DLY}$ will be described in separate paragraph.

During steady state operation, the duration of the on-period $t_{ON}$ can be determined with two different modes: the Constant On-Time (COT) mode and the Peak Current Mode (PCM), which are configured by setting the MODE1 and MODE2 pins. For the COT mode, $t_{ON}$ is generated by comparing an internal fixed saw-tooth wave with the voltage on the COMP pin, $V_{COMP}$. Since $V_{COMP}$ is slow varying, $t_{ON}$ is nearly constant within an AC line cycle. For the PCM, the on-period is terminated when the voltage of the ISNS pin, $V_{ISNS}$ reaches a threshold determined by $V_{COMP}$. Since the instantaneous input voltage (AC voltage) varies, $t_{ON}$ varies accordingly within an AC line cycle. The duration of the off-period $t_{OFF}$ is determined by the rate of discharging of $L_S$, which is governed by $I_{LS-PEAK}$ and $V_{LED}$. Also, $I_{LS-PEAK}$ equals to n × $I_{LP-PEAK}$ where n is the turn ratio of $L_P$ and $L_S$. Figure 15 shows the typical waveforms in normal operation.

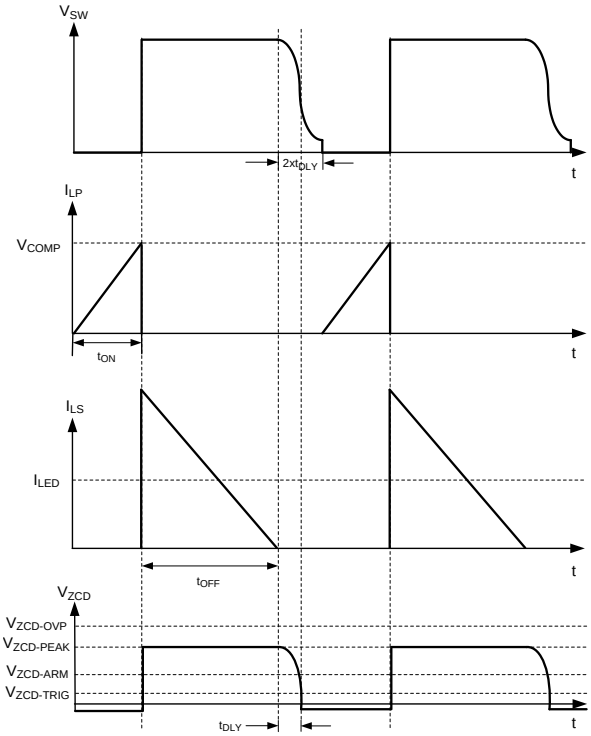



**Figure 15. Primary and Secondary Side Current Waveforms**

## Startup Bias and UVLO

During startup, the TPS92310 is in the startup state. It is powered from the AC line through $R_1$ and $D_1$ (Figure 1). In the startup state, most of the internal circuits of the TPS92310 shut down so that the quiescent current is minimized. When $V_{CC}$ (voltage on the VCC pin) reaches the rising threshold of the $V_{CC-UVLO}$ (typically 25.6V), the TPS92310 is in the low frequency state, where $t_{ON}$ and $t_{OFF}$ are fixed to 1.5µs and 72µs. When $V_{ZCD–PEAK}$ is higher than $V_{ZCD-ARM}$, the TPS92310 enters normal operation.

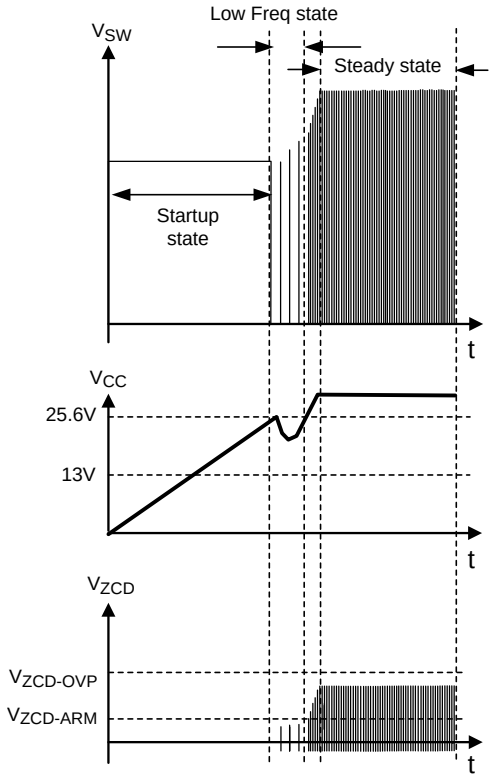



**Figure 16. Start up Bias Waveforms**

## Mode Decoder

The TPS92310 can operate in the Peak Current Mode (PCM) or Constant On-Time (COT) mode if an isolated topology is used. The TPS92310 can also use a non-isolated topology. In this case, only the COT mode can be selected. The COT mode gives a high power factor. The PCM can achieve a lower output current ripple. The COT mode using a non-isolated topology can achieve a higher efficiency and good load regulation. The above modes can be selected by setting the MODE1 and MODE2 pins according to Table 1. For normal operation of the TPS92310, the MODE1 and MODE2 pins cannot be connect to ground at the same time. And these pin were biased by an internal 1µA pull up, forcing any voltage into these pins are not allowed. The MODE decoder status will latch-in only when $V_{CC}$ voltage reaches the $V_{CC-UVLO}$ turn on threshold during start-up.

**Table 1. MODE Configuration**

| MODE1 | MODE2 | Mode of operation |
|---|---|---|
| OPEN | OPEN | COT mode using isolated topology |
| GND | OPEN | PCM using isolated topology |
| OPEN | GND | COT mode using non-isolated topology |
| GND | GND | Reserved |

## Zero Crossing Detection

To minimized the switching loss of the external MOSFET, a zero crossing detection circuit is embedded in the TPS92310. $V_{LAUX}$ is AC voltage coupled from $V_{SW}$ by means of the transformer, with the lower part of the waveform clipped by $D_{ZCD}$. $V_{LAUX}$ is fed back to the ZCD pin to detect a zero crossing point through a resistor divider network which consists of $R_2$ and $R_3$. The next turn on time of $Q_1$ is selected $V_{SW}$ is the minimum, an instant corresponding to a small delay after the zero crossing occurs. (Figure 17) The actual delay time depends on the drain capacitance of the $Q_1$ and the primary inductance of the transformer ($L_P$). Such delay time is set by a single external resistor as described in Delay Setting section.

During the off-period at steady state, $V_{ZCD}$ reaches its maximum $V_{ZCD-PEAK}$ (Figure 14), which is scalable by the turn ratio of the transformer and the resistor divider network $R_2$ and $R_3$. It is recommended that $V_{ZCD-PEAK}$ is set to 3V during normal operation.

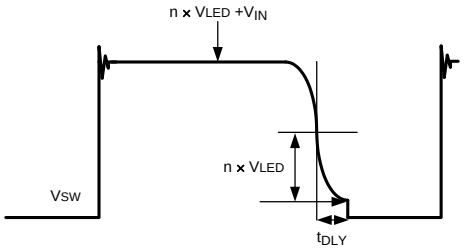



**Figure 17. Switching Node Waveforms**

## Delay Time Setting

In order to reduce EMI and switching loss, the TPS92310 can insert a delay between the off-period and the on-period. The delay time is set by a single resistor which connects across the DLY pin and ground, and their relationship is shown in Figure 18. The optimal delay time depends on the resonance frequency between $L_P$ and the drain to source capacitance of $Q_1$ ($C_{DS}$). Circuit designers should optimize the delay time according to the following equation.

$$f_{SW} = \frac{1}{2\pi\sqrt{L_P C_{DS}}} \quad (1)$$

$$t_{DLY} = \frac{\pi\sqrt{L_P C_{DS}}}{2} \quad (2)$$

After determining the delay time, $t_{DLY}$ can be implemented by setting $R_{DLY}$ according to the following equation:

$$R_{DLY} = K_{DLY}(t_{DLY} - 105ns) \quad (3)$$

where $K_{DLY}$ = 32MΩ/ns is a constant.

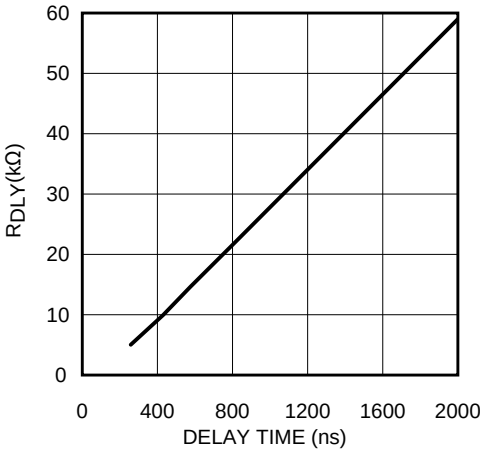



**Figure 18. Delay Time Setting**

## Protection Features

### Output Open Circuit Protection

If the LED string is disconnected, $V_{LED}$ increases and thus $V_{ZCD-PEAK}$ increases. When $V_{ZCD-PEAK}$ is larger than $V_{ZCD-OVP}$ for 3 continues switching cycles, the Over Voltage Protection (OVP) feature is triggered such that the TPS92310 becomes Over-Voltage (OV) state. In this case, the switching of $Q_1$ is stopped, and $V_{CC}$ decreases owing to the power consumption of the internal circuits of the TPS92310. When $V_{CC}$ drops below the falling threshold of $V_{CC-UVLO}$, the TPS92310 restarts, and re-enter into startup state (Figure 20).

### Output Short Circuit Protection

If the LED string is shorted, $V_{ZCD-PEAK}$drops. If $V_{ZCD-PEAK}$ drops below $V_{ZCD-TRIG}$, the TPS92310 will under low frequency operation. In this case, the power supplied from $L_{AUX}$ is not enough to maintain $V_{CC}$, then $V_{CC}$ decreases. If the short is removed during low frequency state, the TPS92310 will restore to steady state. If the short sustains till VCC drops below the falling threshold of $V_{CC-UVLO}$, the TPS92310 restarts, and becomes startup state again. (Figure 19)

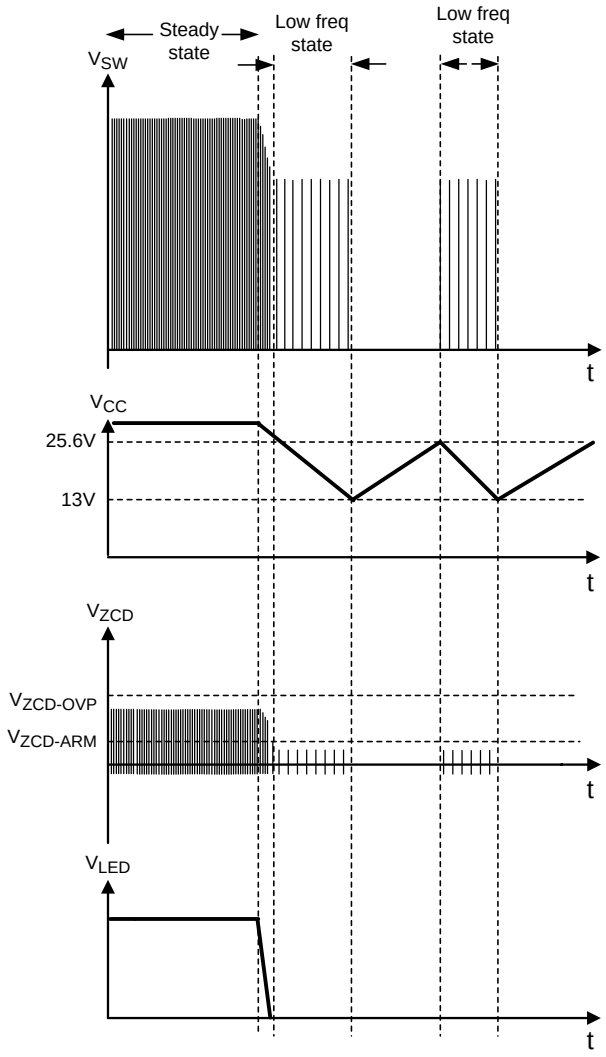



**Figure 19. Output Short Circuit waveforms**

### Over Current Protection

The Over Current Protection (OCP) limits the drain current of the external MOSFET Q1 and prevent inductor / transformer saturation. When $V_{ISNS}$ reaches a threshold, the OCP is triggered and the output of the GATE pin is low immediately. The threshold is typically 3.4V and 0.64V when the TPS92310 is using an isolated topology and a non-isolated topology respectively.

### Thermal Protection

Thermal protection is implemented by an internal thermal shutdown circuit, which activates at 160°C (typically) to shut down the TPS92310. In this case, the GATE pin outputs low to turn off the external MOSFET, and hence no power from the VAUX winding to $V_{CC}$. Capacitor $C_{VCC}$ will discharge until UVLO. When the junction temperature of the TPS92310 falls back below 130°C, the TPS92310 resumes normal operation.

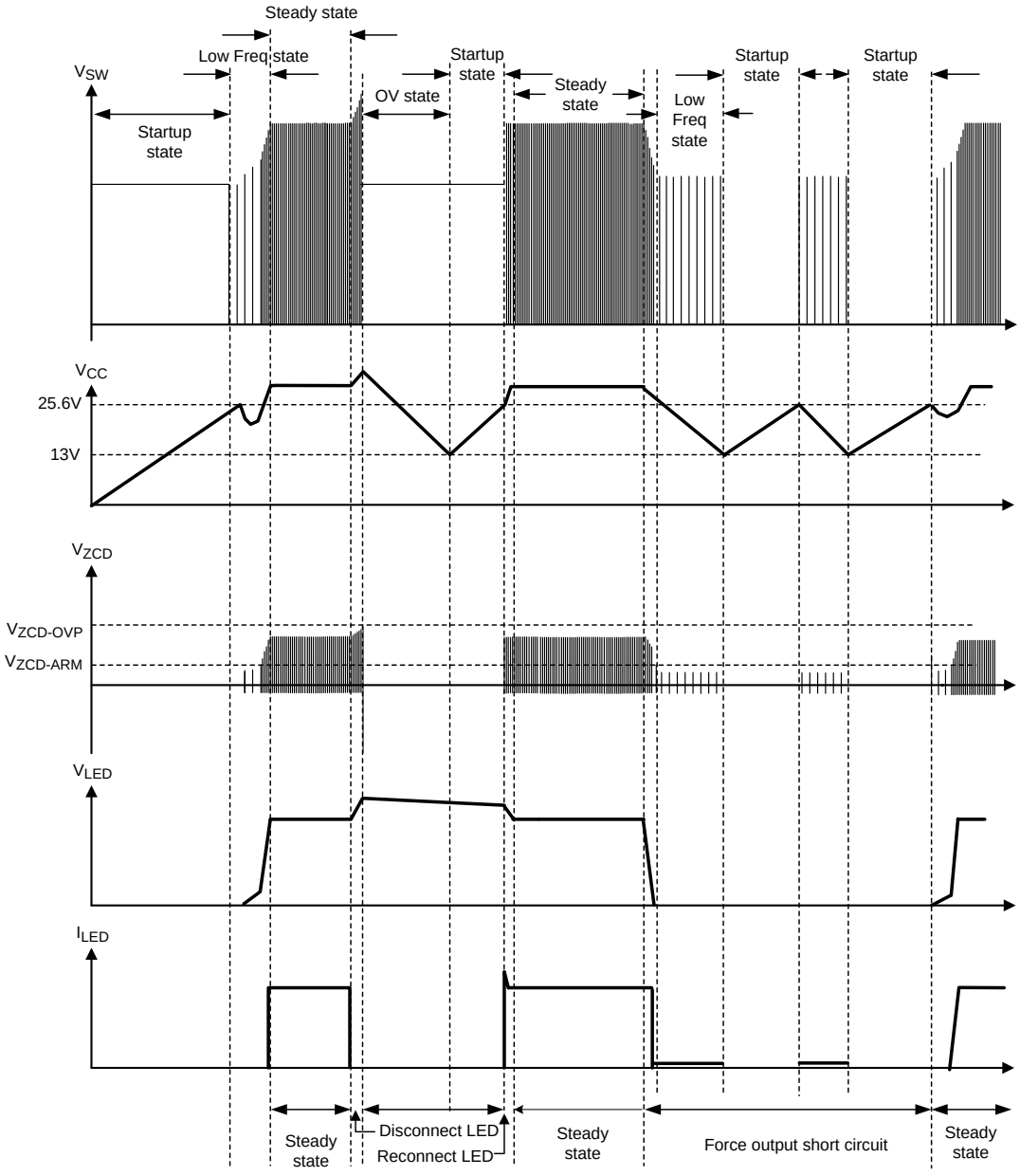



**Figure 20. Auto Restart Operation**

## Design Example

The following design example illustrates the procedures to calculate the external component values for the TPS92310 isolated single stage fly-back LED driver with PFC.

### Design Specifications:

Input voltage range, $V_{AC\_RMS}$ = 85VAC – 132VAC

Nominal input voltage, $V_{AC\_RMS(NOM)}$ = 110VAC

Number of LED in serial =7

LED current, $I_{LED}$ = 350mA

Forward voltage drop of single LED = 3.0V

Forward voltage of LED stack, $V_{LED}$ = 21V

### Key operating Parameters:

Converter minimum switching frequency, $f_{SW}$ = 75kHz

Output rectifier maximum reverse voltage, $V_{D3(MAX)}$ = 100V

Power MOSFET rating, $V_{Q1(MAX)}$ = 800V (2.5A/3.8Ω)

Power MOSFET Output Capacitance, $C_{DS}$ = 37pF (estimated)

Nominal output power, $P_{OUT}$ = 8W

### Start Up Bias resistor

During start up, the $V_{CC}$ will be powered by the rectified line voltage through external resistor, $R_1$. The $V_{CC}$ start up current, $I_{VCC(SU)}$ must set in the range $I_{VCC(MIN)} > I_{VCC(SU)} > I_{STARTUP(MAX)}$ to ensure proper restart operation during OVP fault. In this example, a value of 0.55mA is suggested. The resistance of $R_1$ can be calculated by dividing the nominal input voltage in RMS by the start up current suggested.

So, $R_1$ = 110V/0.55mA = 200KΩ is recommended.

### Transformer Turn Ratio

The transformer winding turn ratio, n is governed by the MOSFET Q1 maximum rated voltage, ($V_{Q3(MAX)}$), highest line input peak voltage ($V_{AC\text{-}PEAK}$) and output diode maximum reverse voltage rating ($V_{D3(MAX)}$). The output diode rating limits the lower bound of the turn ratio and the MOSFET rating provide the upper bound of the turn ratio. The transformer turn ratio must be selected in between the bounds. If the maximum reverse voltage of D3 ($V_{D3(MAX)}$) is 100V. the minimum transformer turn ratio can be calculated with the equation in below.

$$n > \frac{V_{AC\text{-}PEAK}}{\left(V_{D3(MAX)} - V_{LED}\right)}$$

$$n > \frac{132 \times \sqrt{2}}{100-30} = 2.33 \quad (4)$$

In operation, the voltage at the switching node, $V_{SW}$ must be small than the MOSFET maximum rated voltage $V_{Q1(MAX)}$ , For reason of safety, 10% safety margin is recommended. Hence, 90% of $V_{Q1(MAX)}$ is used in the following equation.

$$n < \frac{V_{Q1(MAX)} \times 0.9 - V_{AC\text{-}PEAK} - V_{os}}{V_{LED(MAX)}} \quad (5)$$

$$n < \frac{600 \times 0.9 - 132\sqrt{2} - 50}{30} = 12.1 \quad (6)$$

where $V_{OS}$ is the maximum switching node overshoot voltage allowed, in this example, 50V is assumed. As a rule of thumb, lower turn ratio of transformer can provide a better line regulation and lower secondly side peak current. In here, turn ratio n = 3.8 is recommended.

### Switching Frequency Selection

TPS92310 can operate at high switching frequency in the range of 60kHz to 150kHz. In most off-line applications, with considering of efficiency degradation and EMC requirements, the recommended switching frequency range will be 60kHz to 80kHz. In this design example, switching frequency at 75kHz is selected.

### Switching On Time

The maximum power switch on-time, $t_{ON}$ depends on the low line condition of $85V_{AC}$. At $85V_{AC}$ the switching frequency was chosen at 75kHz. This transformer design will follow the formulae as shown below.

$$t_{ON}=\frac{1}{f_{sw}\left(\frac{V_{AC\_MIN\_PEAK}}{n x V_{LED}}+1\right)}$$

$$t_{ON}=\frac{1}{75000\left(\frac{85\sqrt{2}}{3.8 \text{ x } 21}+1\right)}=5.3\,\mu s \quad (7)$$

### Transformer Primary Inductance

The primary inductance, $L_P$ of the transformer is related to the minimum operating switching frequency $f_{SW}$, converter output power $P_{OUT}$, system efficiency η and minimum input line voltage $V_{AC\_RMS(MIN)}$. For CRM operation, the output power, $P_{OUT}$ can be described by the equation in below.

$$P_{OUT}=\eta x\frac{1}{2}L_P x I_{LP\text{-}PEAK}{}^2 x f_{SW} \quad (8)$$

By re-arranging terms, the transformer primary inductance required in this design example can be calculated with the equation follows:

$$L_P=\frac{\eta x V_{AC\_RMS(MIN)}{}^2 t_{ON}{}^2}{2 x P_{OUT} x \frac{1}{f_{sw}}} \quad (9)$$

The converter minimum switching frequency is 75kHz, $t_{ON}$ is 5.3µs, $V_{AC\_RMS(MIN)}$ = 85V and $P_{OUT}$ = 8W, assume the system efficiency, η = 85%. Then,

$$L_P=\frac{0.85 x (85)^2 x (5.3\,\mu)^2}{2x8x13.3\,\mu}=0.81mH \quad (10)$$

From the calculation in above, the inductance of the primary winding required is 0.81mH.

### Calculate The Current Sensing Resistor

After the primary inductance and transformer turn ratio is determined, the current sensing resistor, $R_{ISNS}$ can be calculated.

The resistance for $R_{ISNS}$ is governed by the output current and transformer turn ratio, the equation in below can be used.

$$R_{ISNS}= n \text{ x } \left(\frac{V_{REF}}{I_{LED}}\right) \quad (11)$$

where $V_{REF}$ is fixed to 0.14V internally.

Transformer turn ratio, $N_P$ : $N_S$ is 3.8 : 1 and $I_{LED}$ = 0.35A

$$R_{ISNS}=3.8\times\frac{0.14}{0.35}=1.52\,\Omega \quad (12)$$

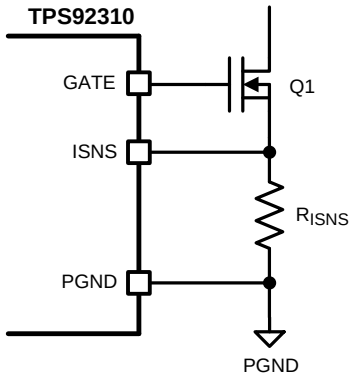



**Figure 21. $R_{ISNS}$ Resistor Interface**

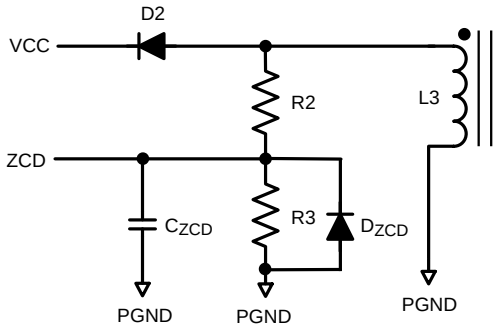



**Figure 22. Auxiliary Winding Interface to ZCD**

### Auxiliary Winding Interface To ZCD

In Figure 22, R2 and R3 forms a resistor divider which sets the thresholds for over voltage protection of $V_{LED}$, $V_{ZCD-OVP}$, and $V_{ZCD-PEAK}$. Before the calculation, we need to set the voltage of the auxiliary winding, $V_{LAUX}$ at open circuit.

For example :

Assume the nominal forward voltage of LED stack ($V_{LED}$) is 21V.

To avoid false triggering $ZCD_{OVP}$ voltage threshold at normal operation, select $ZCD_{OVP}$ voltage at 1.3 times of the $V_{LED}$ is typical in most applications. In case the transformer leakage is higher, the $ZCD_{OVP}$ threshold can be set to 1.5 times of the $V_{LED}$.

In this design example, open circuit AUX winding OVP voltage threshold is set to 30V. Assume the current through the AUX winding is 0.4mA typical.

As a result, R2 is 66kΩ and R3 is 11kΩ. Also, for suppressing high frequency noise at the ZCD pin, a 15pF capacitor connects the ZCD pin to ground is recommended.

### Auxiliary Winding $V_{cc}$ Diode Selection

The $V_{CC}$ diode $D_2$ provides the supply current to the controller, low temperature coefficient , low reverse leakage and ultra fast diode is recommended.

### Compensation Capacitor And Delay Timer Resistor Selection

To achieve PFC function with a constant on time flyback converter, a low frequency response loop is required. In most applications, a 2.2µF $C_{COMP}$ capacitor is suitable for compensation.

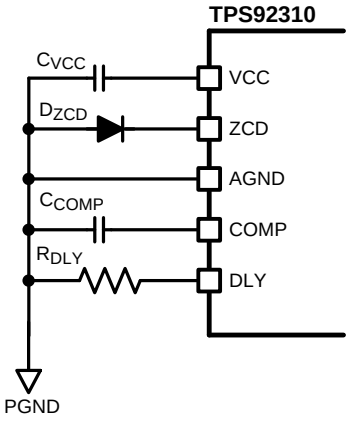



**Figure 23. Compensation and DLY Timer connection**

The resistor $R_{DLY}$ connecting the DLY pin to ground is used to set the delay time between the ZCD trigger to gate turn on. The delay time required can be calculated with the parasitic capacitance at the drain of MOSFET to ground and primary inductance of the transformer. Equation in below can be used to find the delay time and Figure 18 can help to find the resistance once the delay time is calculated

$$t_{DLY} = \frac{\pi\sqrt{L_P C_{DS}}}{2} \quad (13)$$

For example, using a transformer with primary inductance $L_P$ = 1mH, and power MOSFET drain to ground capacitor $C_{DS}$=37pF, the $t_{DLY}$ can be calculated by the upper equation. As a result, $t_{DLY}$=302ns and $R_{DLY}$ is 6.31kΩ. The delay time may need to change according to the primary inductance of the transformer. The typical level of output current will shift if inappropriate delay time is chosen.

### Output Flywheel Diode Selection

To increase the overall efficiency of the system, a low forward voltage schottky diode with appropriate rating should be used.

### Primary Side Snubber Design

The leakage inductance can induce a high voltage spike when power MOSFET is turned off. Figure 24 illustrate the operation waveform. A voltage clamp circuit is required to protect the MOSFET. The voltage of snubber clamp ($V_{SN}$) must be higher than the sum of over shoot voltage ($V_{OS}$), LED open load voltage multiplied by the transformer turn ratio (n). In this examples, the $V_{OS}$ is 50V and LED maximum voltage, $V_{LED(MAX)}$ is 30V, transformer turn ratio is 3.8. The snubber voltage required can be calculated with following equations.

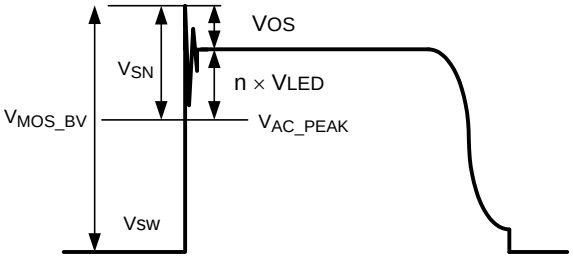



**Figure 24. Snubber Waveform**

$$V_{SN} > V_{OS} + V_{LED(MAX)} \times n \quad (14)$$

where n is the turn ratio of the transformer.

$$V_{SN} > 50V + 30V \times 3.8 = 154V \quad (15)$$

At the same time, sum of the snubber clamp voltage and $V_{AC}$ peak voltage ($V_{AC\_PEAK}$) must be smaller than the MOSFET breakdown voltage ($V_{MOS\_BV}$). By re-arranging terms, equation in below can be used.

$$V_{SN} < V_{MOS\_BV} - V_{AC}\sqrt{2}$$
$$V_{SN} < 800 - 132 \times \sqrt{2} = 614V \quad (16)$$

In here, snubber clamp voltage, $V_{SN}$ = 250V is recommended.

### Output Capacitor

The capacitance of the output capacitor is determined by the equivalent series resistance (ESR) of the LED, $R_{LED}$ and the ripple current allowed for the application. The equation in below can be used to calculate the required capacitance.

$$C_{OUT} = \frac{\sqrt{\left(2\frac{I_{LED}}{\Delta I_{LED}}\right)^2 - 1}}{4 \times \pi \times f_{AC} \times R_{LED}} \quad (17)$$

Assume the ESR of the LED stack contains 7 LEDs and is 2.6Ω, AC line frequency $f_{AC}$ is 60Hz.

In this example, LED current $I_{LED}$ is 350mA and output ripple current is 30% of $I_{LED}$:

$$C_{OUT} = \frac{\sqrt{\left(\frac{2 \times 0.35}{0.3 \times 0.35}\right)^2 - 1}}{4 \times \pi \times 60 \times 7 \times 2.6} \quad (18)$$

Then, $C_{OUT}$ = 480µF.

In here, a 470µF output capacitor with 10µF ceramic capacitor in parallel is suggested.

## PCB Layout Considerations

The performance of any switching power supplies depend as much upon the layout of the PCB as the component selection. Good layout practices are important when constructing the PCB. The layout must be as neat and compact as possible, and all external components must be as close as possible to their associated pins. High current return paths and signal return paths must be separated and connect together at single ground point. All high current connections must be as short and direct as possible with thick traces. The gate pin of the switching MOSFET should be connected close to the GATE pin with short and thick trace to reduce potential electro-magnetic interference. For off-line applications, one more consideration is the safety requirements. The clearance and creepage to high voltage traces must be complied to all applicable safety regulations.

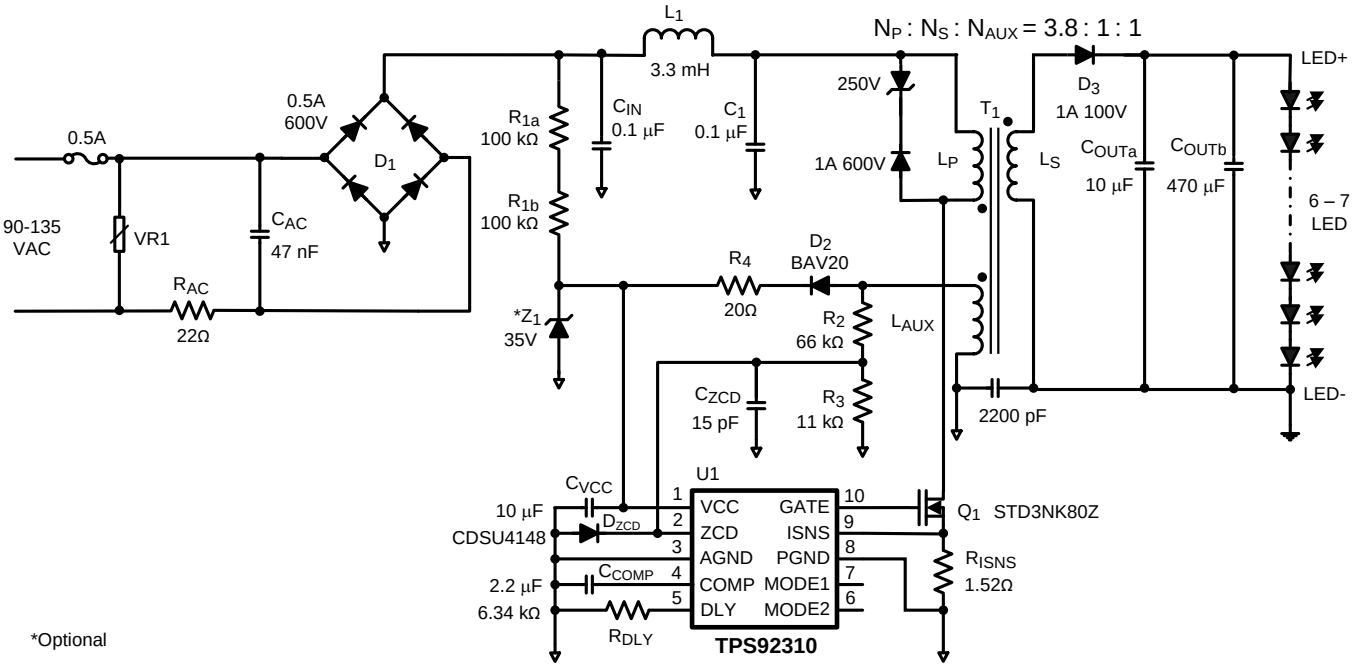



**Figure 25. Isolated topology schematic**

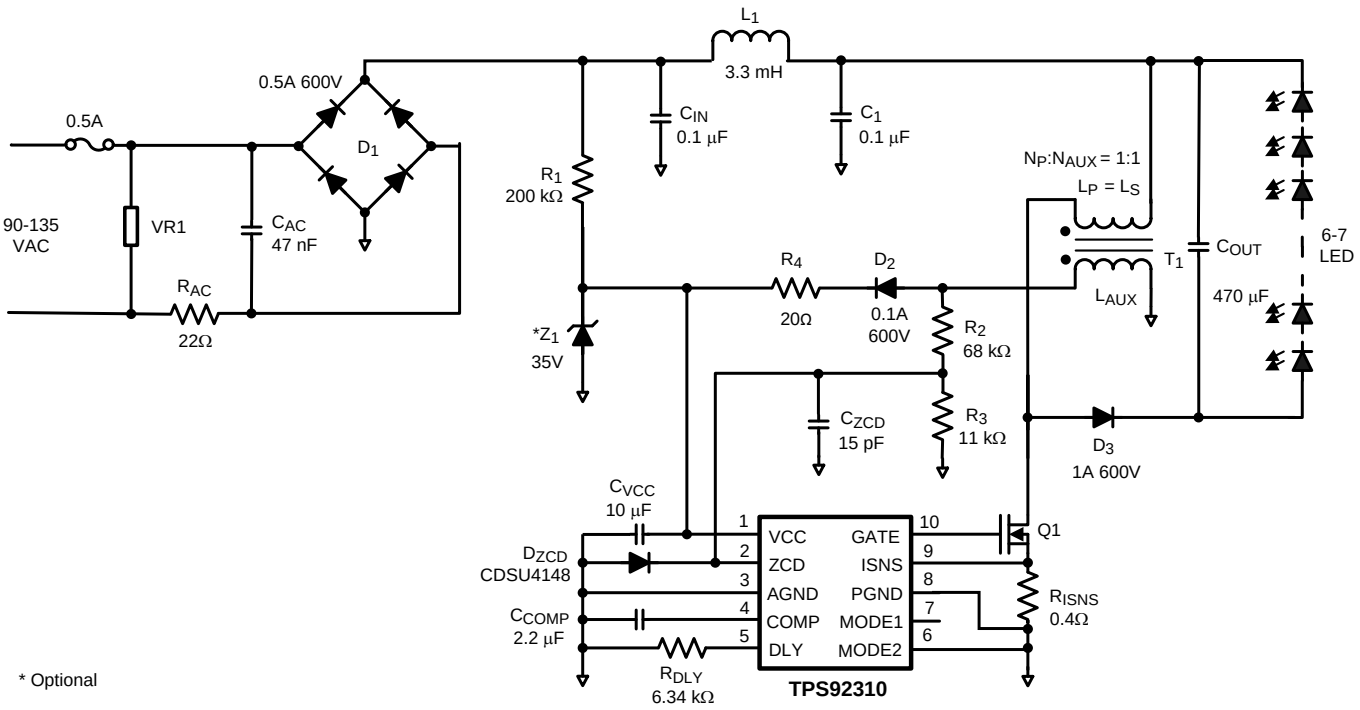



**Figure 26. Non-isolated topology schematic**

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS92310DGS/NOPB | Active | Production | VSSOP (DGS) \| 10 | 1000 \| SMALL T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | SL1B |
| TPS92310DGS/NOPB.A | Active | Production | VSSOP (DGS) \| 10 | 1000 \| SMALL T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | SL1B |
| TPS92310DGSR/NOPB | Active | Production | VSSOP (DGS) \| 10 | 3500 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | SL1B |
| TPS92310DGSR/NOPB.A | Active | Production | VSSOP (DGS) \| 10 | 3500 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | SL1B |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

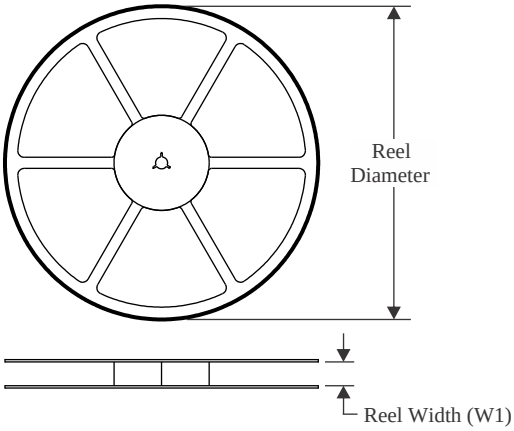
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

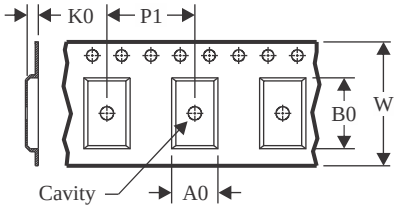
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

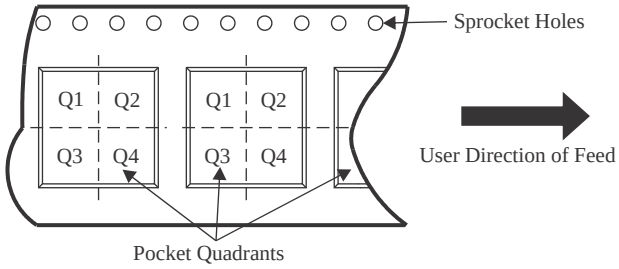



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

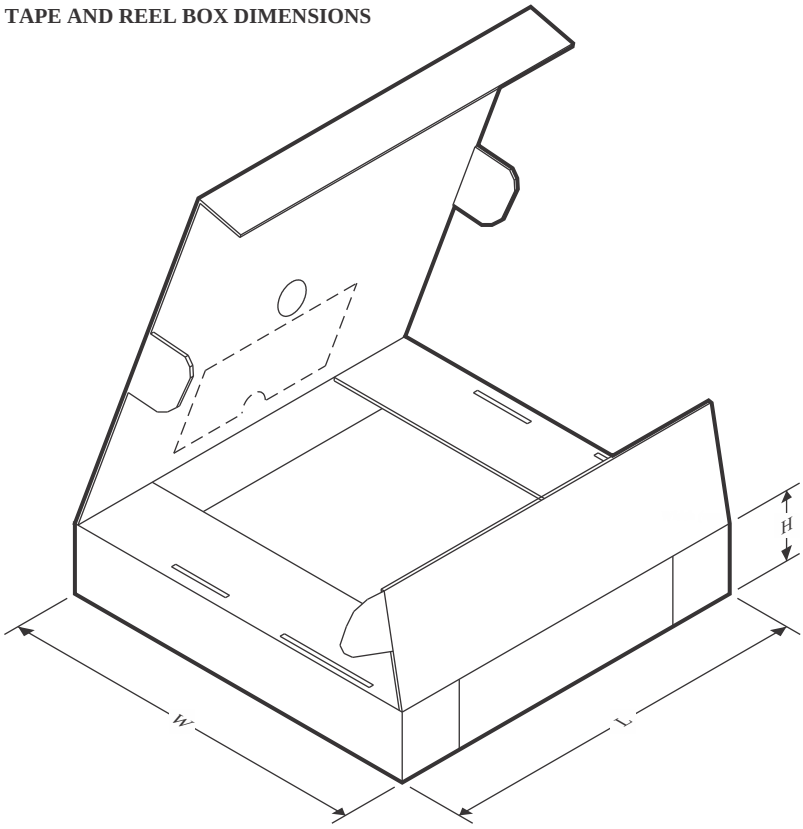
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS92310DGS/NOPB | VSSOP | DGS | 10 | 1000 | 177.8 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TPS92310DGSR/NOPB | VSSOP | DGS | 10 | 3500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

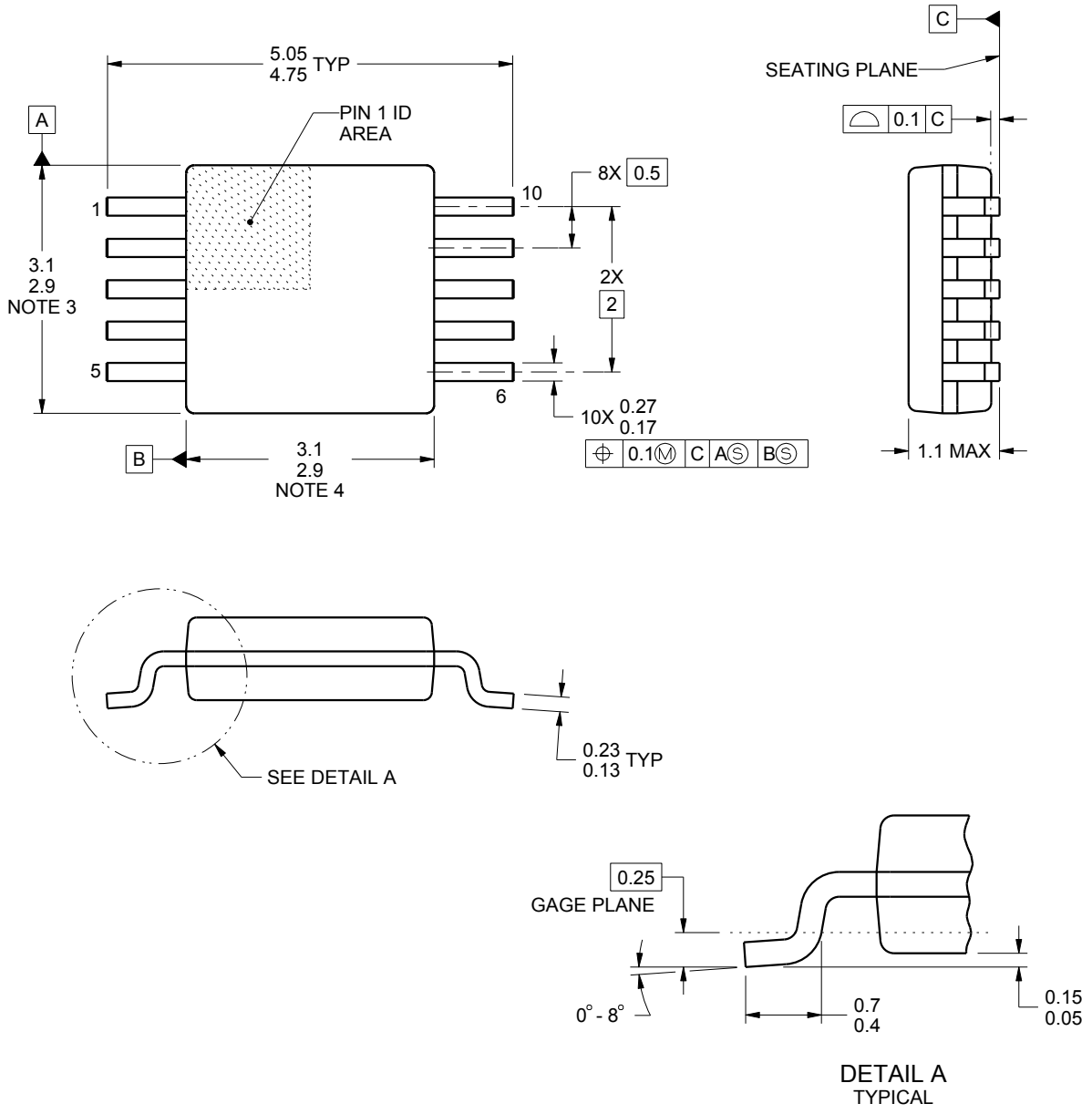
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS92310DGS/NOPB | VSSOP | DGS | 10 | 1000 | 208.0 | 191.0 | 35.0 |
| TPS92310DGSR/NOPB | VSSOP | DGS | 10 | 3500 | 367.0 | 367.0 | 35.0 |

# PACKAGE OUTLINE

## DGS0010A

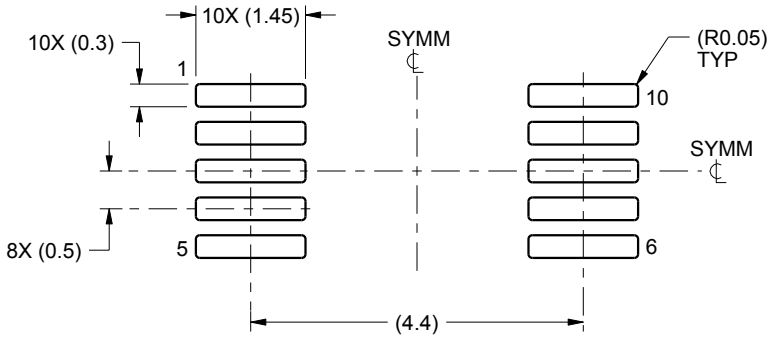
## VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

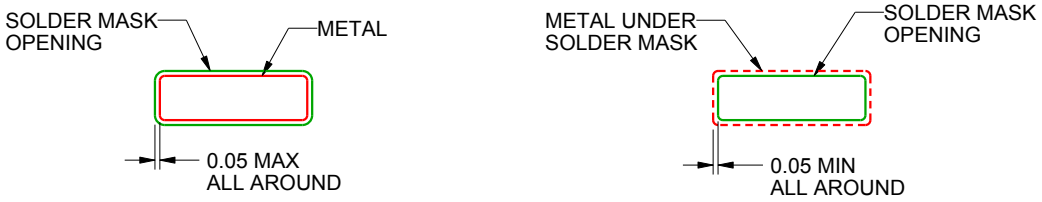



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.




LAND PATTERN EXAMPLE
SCALE:10X

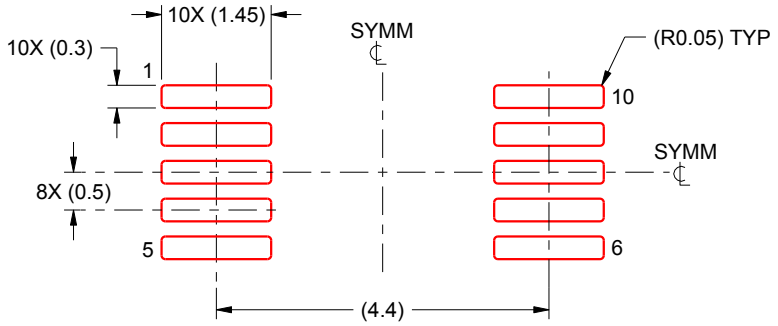



SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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