

# TPS92401 4-Channel 5A LED Dot-Controller with Integrated PWM Shunt FETs, SPI Interface and Adaptive Configuration

## 1 Features

- 4.5V to 65V wide input range
- LED common anode or cathode connection
- 4 integrated PWM shunt FETs
  - 5A FET max continuous current
  - Internal 32MHz oscillator for PWM generator
  - Programmable 16-bit, >20kHz PWM dimming
- SPI interface and adaptive configuration
  - Up to 5MHz SPI clock for data transfer
  - Star and daisy chain connection
  - Stacking up to 4 devices for 16-LED string
- Enhanced EMI performance
  - Programmable PWM slew rate
  - Programmable PWM edge shift
  - Internal charge pump with spread spectrum
- Full protection features
  - LED open detection and protection
  - LED short detection
  - Shunt FET open detection
  - Programmable LED open voltage
  - Thermal warning
- Optional power save mode
  - PWM output to control LED drivers
  - Low power standby mode
- Package: VQFN-36

## 2 Applications

- Stage and Photography Lighting
- Surgical Lighting
- Machine Vision and IP Camera LED Array
- Cold/Warm WLED Lighting
- 3D Printing
- Industrial Transportation

## 3 Description

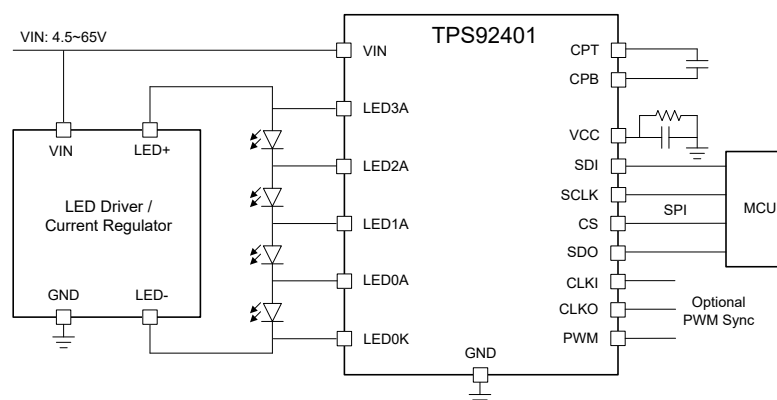
The TPS92401 LED dot-controller device enables 4-channel individual lighting solutions by providing up to 5A pixel-level LED dimming control with 4.5V to 65V wide input range. The device includes a string of 4 series-connected integrated shunt FETs, each of which providing PWM dimming for an individual LED. The shunt FET string allows the device to support constant current regulators with either common-anode or common-cathode LEDs.

The TPS92401 has an internal oscillator for a system clock to enable integrated PWM generator up to 16-bit with programmable PWM frequency up to 60kHz. The serial peripheral interface (SPI) enables high speed data transmission and supports both daisy chain and star connections. The SPI and optimized pinout allow multiple devices connected in stacking configuration for single-layer PCBs.

The TPS92401 incorporates registers for programming PWM pulse width, slew rate, edge shift and open voltage of each individual LED in the string and for reporting LED open, LED short, shunt FET open and thermal warning. The internal charge pump incorporates spread spectrum feature to enhance EMI performance. The TPS92401 also provides PWM dimming control of constant current regulators and enables multi-channel power save to significantly increase dimming efficiency especially in low brightness condition.

### Package Information

| PART NUMBER         | PACKAGE   | BODY SIZE (NOM) |
|---------------------|-----------|-----------------|
| TPS92401, TPS92401M | VQFN (36) | 6.00mm × 5.00mm |



**Simplified Application**



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## 4 Device and Documentation Support

### 4.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 4.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 4.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

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### 4.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 4.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE          | REVISION | NOTES           |
|---------------|----------|-----------------|
| November 2024 | *        | Initial release |

## 6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

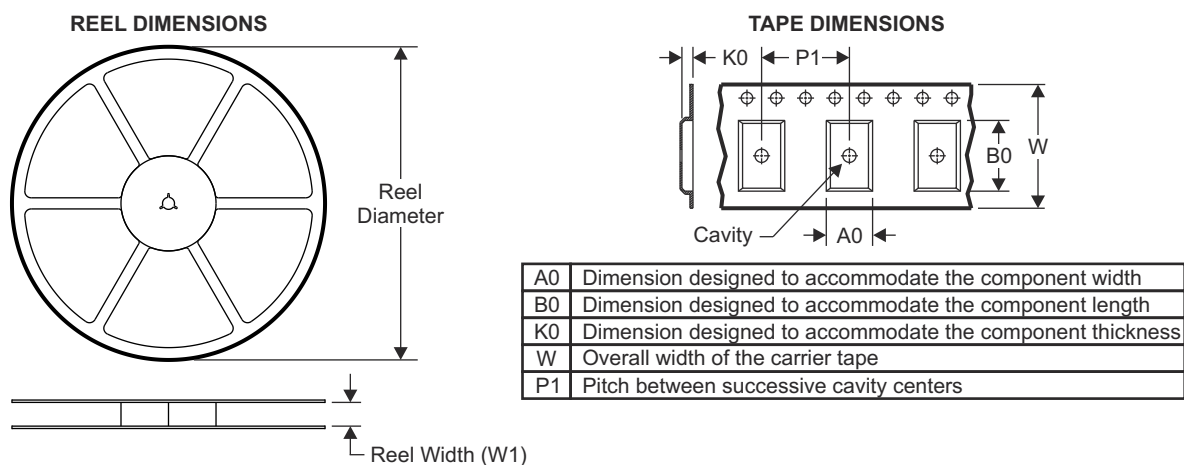
## 6.1 Package Option Addendum

### Packaging Information

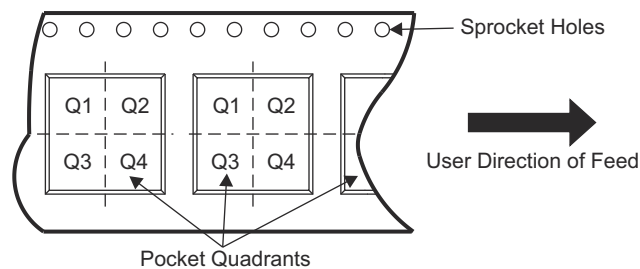
| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup>   | Lead/Ball Finish <sup>(4)</sup> | MSL Peak Temp <sup>(3)</sup> | Op Temp (°C) | Device Marking <sup>(5) (6)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|---------------------------|---------------------------------|------------------------------|--------------|-----------------------------------|
| TPS92401RRVR     | ACTIVE                | VQFN         | RRV             | 36   | 3000        | Green (RoHS and no Sb/Br) | Cu NiPdAu                       | LEVEL1-260C-UNLIM            | -40 to 85    | 92401                             |
| TPS92401MRRVR    | ACTIVE                | VQFN         | RRV             | 36   | 3000        | Green (RoHS and no Sb/Br) | Cu NiPdAu                       | LEVEL1-260C-UNLIM            | -55 to 125   | 92401M                            |

- (1) The marketing status values are defined as follows:  
**ACTIVE:** Product device recommended for new designs.  
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.  
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.  
**PRE\_PROD** Unannounced device, not in production, not available for mass market, nor on the web, samples not available.  
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.  
**OBSOLETE:** TI has discontinued the production of the device.
- (2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.  
**TBD:** The Pb-Free/Green conversion plan has not been defined.  
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.  
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.  
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)
- (3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device
- (6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.  
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## 6.2 Tape and Reel Information

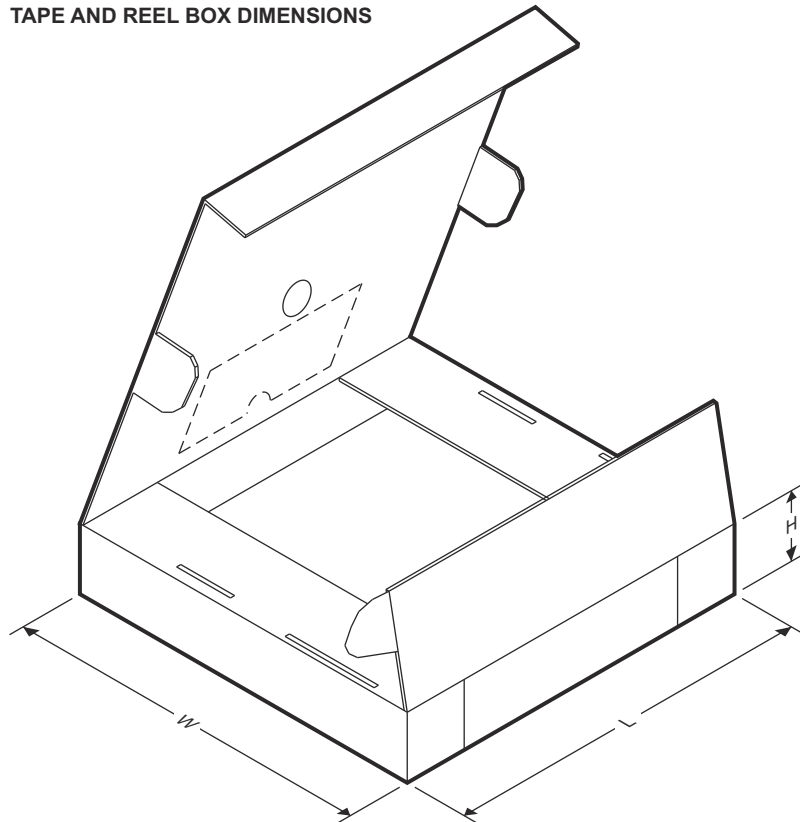


### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS92401RRVR  | VQFN         | RRV             | 36   | 3000 | 330.0              | 12.4               | 5.3     | 6.3     | 1.15    | 8.0     | 12.0   | Q1            |
| TPS92401MRRVR | VQFN         | RRV             | 36   | 3000 | 330.0              | 12.4               | 5.3     | 6.3     | 1.15    | 8.0     | 12.0   | Q1            |

# TAPE AND REEL BOX DIMENSIONS



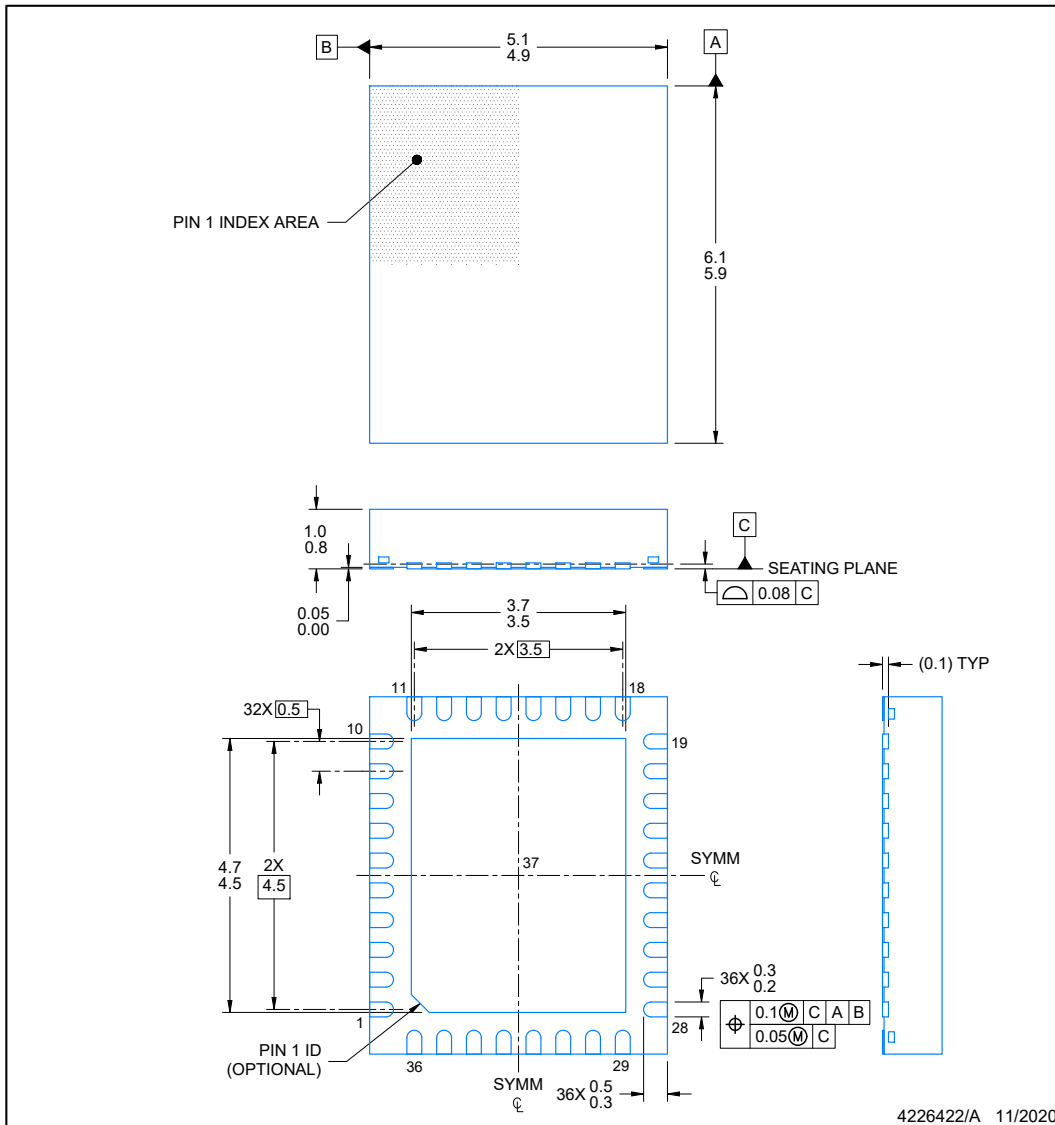
| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS92401RRVR  | VQFN         | RRV             | 36   | 3000 | 360.0       | 360.0      | 36.0        |
| TPS92401MRRVR | VQFN         | RRV             | 36   | 3000 | 360.0       | 360.0      | 36.0        |

# PACKAGE OUTLINE

## RRV0036A

### VQFN - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD

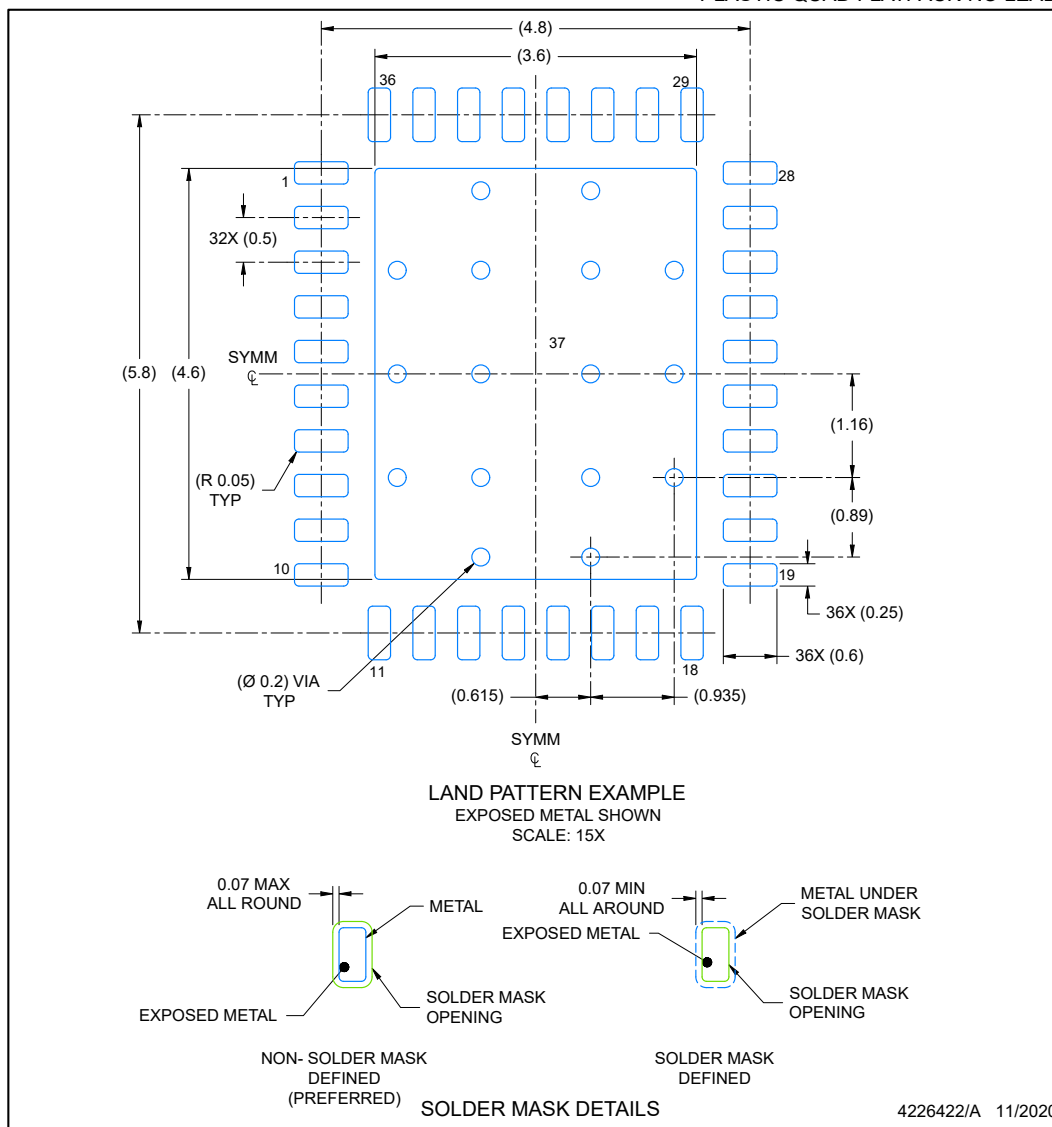


## EXAMPLE BOARD LAYOUT

**VQFN - 1 mm max height**

RRV0036A

PLASTIC QUAD FLATPACK-NO LEAD



NOTES: (continued)

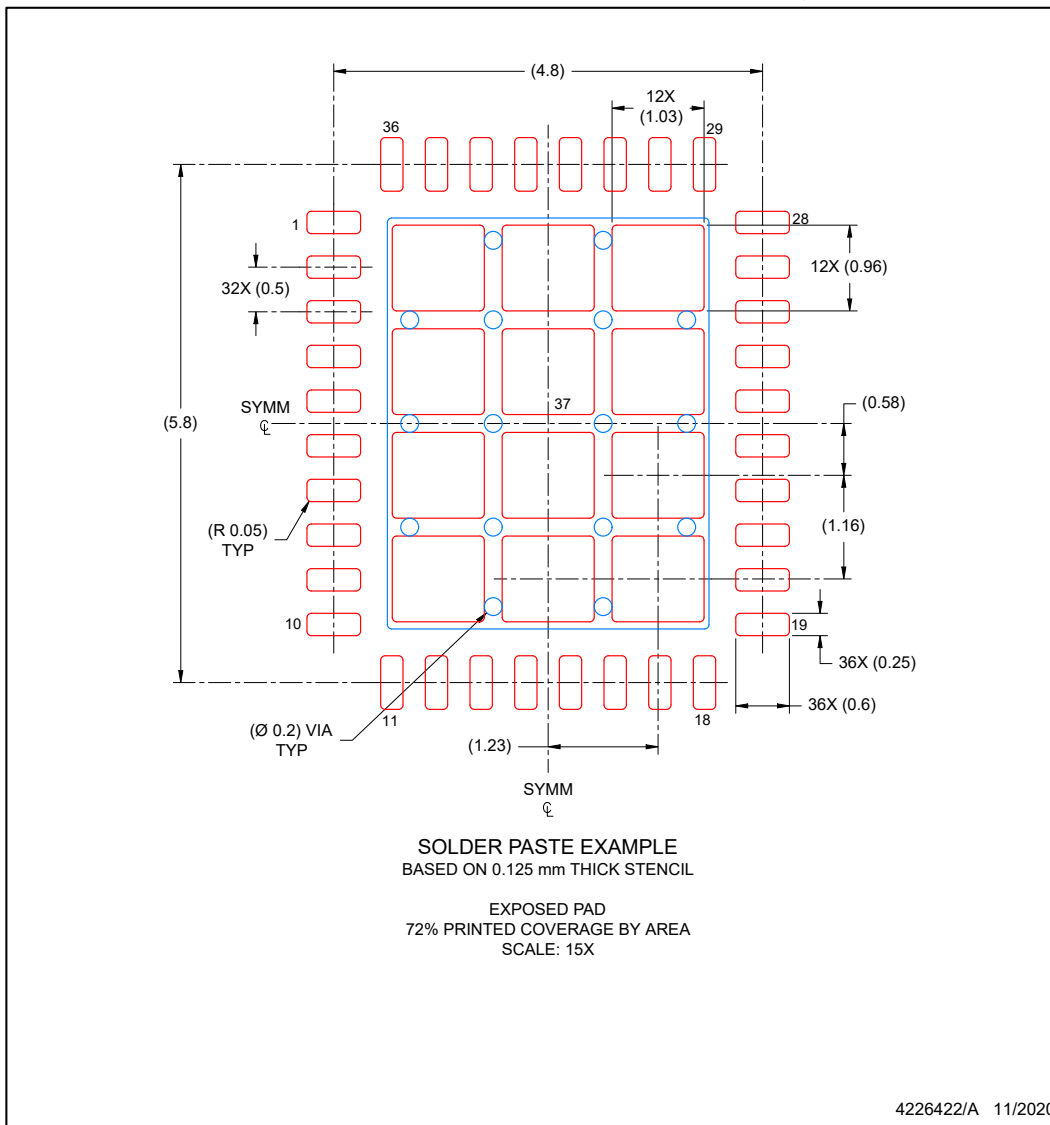
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

## EXAMPLE STENCIL DESIGN

**RRV0036A**

**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK-NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## PACKAGING INFORMATION

| Orderable part number         | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C)      | Part marking<br>(6) |
|-------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|-------------------|---------------------|
| <a href="#">TPS92401MRRVR</a> | Active        | Production           | VQFN (RRV)   36 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85         | 92401M              |
| TPS92401MRRVR.A               | Active        | Production           | VQFN (RRV)   36 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | See TPS92401MRRVR | 92401M              |
| <a href="#">TPS92401RRVR</a>  | Active        | Production           | VQFN (RRV)   36 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85         | 92401               |
| TPS92401RRVR.A                | Active        | Production           | VQFN (RRV)   36 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | See TPS92401RRVR  | 92401               |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

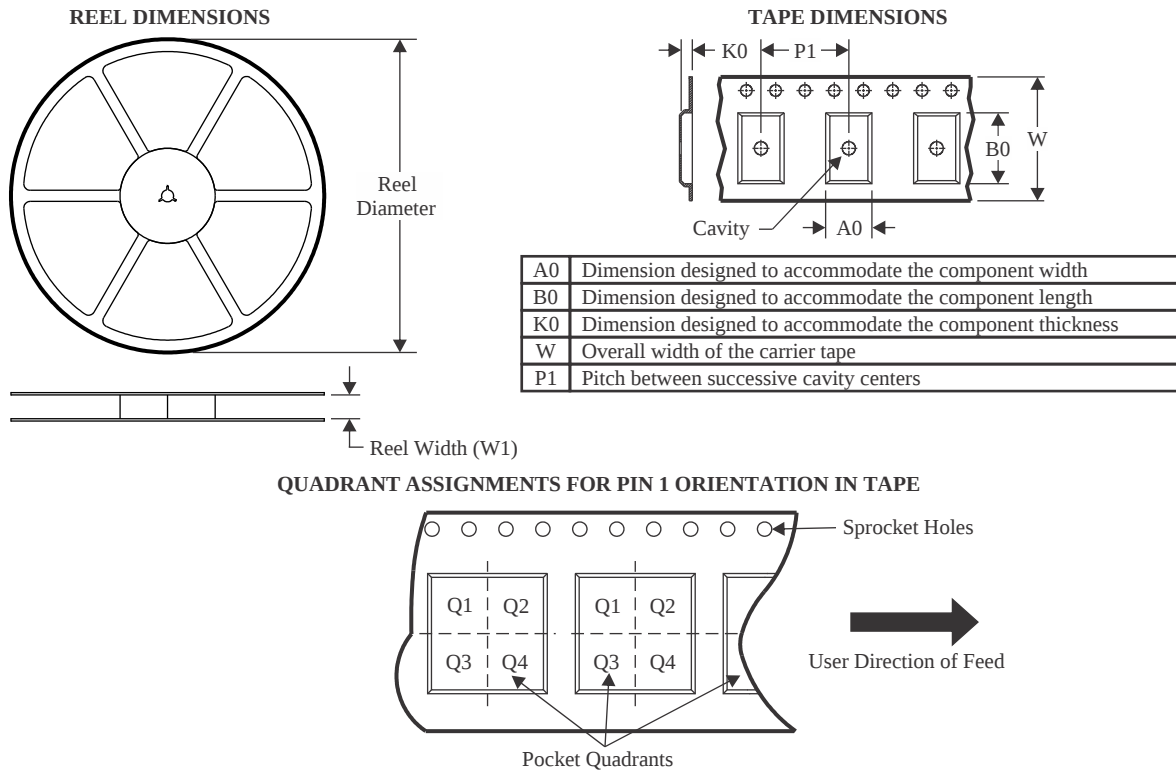
<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS92401MRRVR | VQFN         | RRV             | 36   | 3000 | 330.0              | 12.4               | 5.3     | 6.3     | 1.15    | 8.0     | 12.0   | Q1            |
| TPS92401RRVR  | VQFN         | RRV             | 36   | 3000 | 330.0              | 12.4               | 5.3     | 6.3     | 1.15    | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS92401MRRVR | VQFN         | RRV             | 36   | 3000 | 360.0       | 360.0      | 36.0        |
| TPS92401RRVR  | VQFN         | RRV             | 36   | 3000 | 360.0       | 360.0      | 36.0        |

## GENERIC PACKAGE VIEW

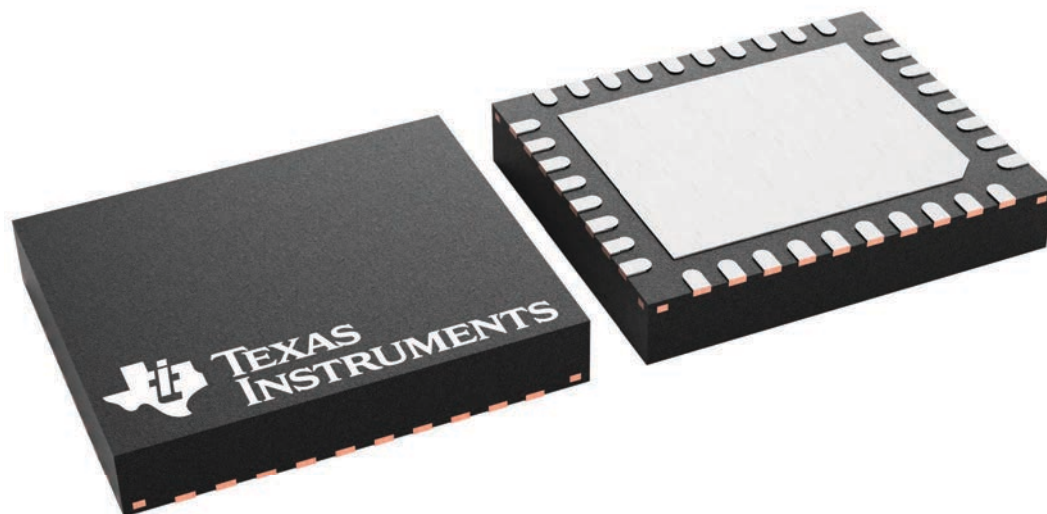
**RRV 36**

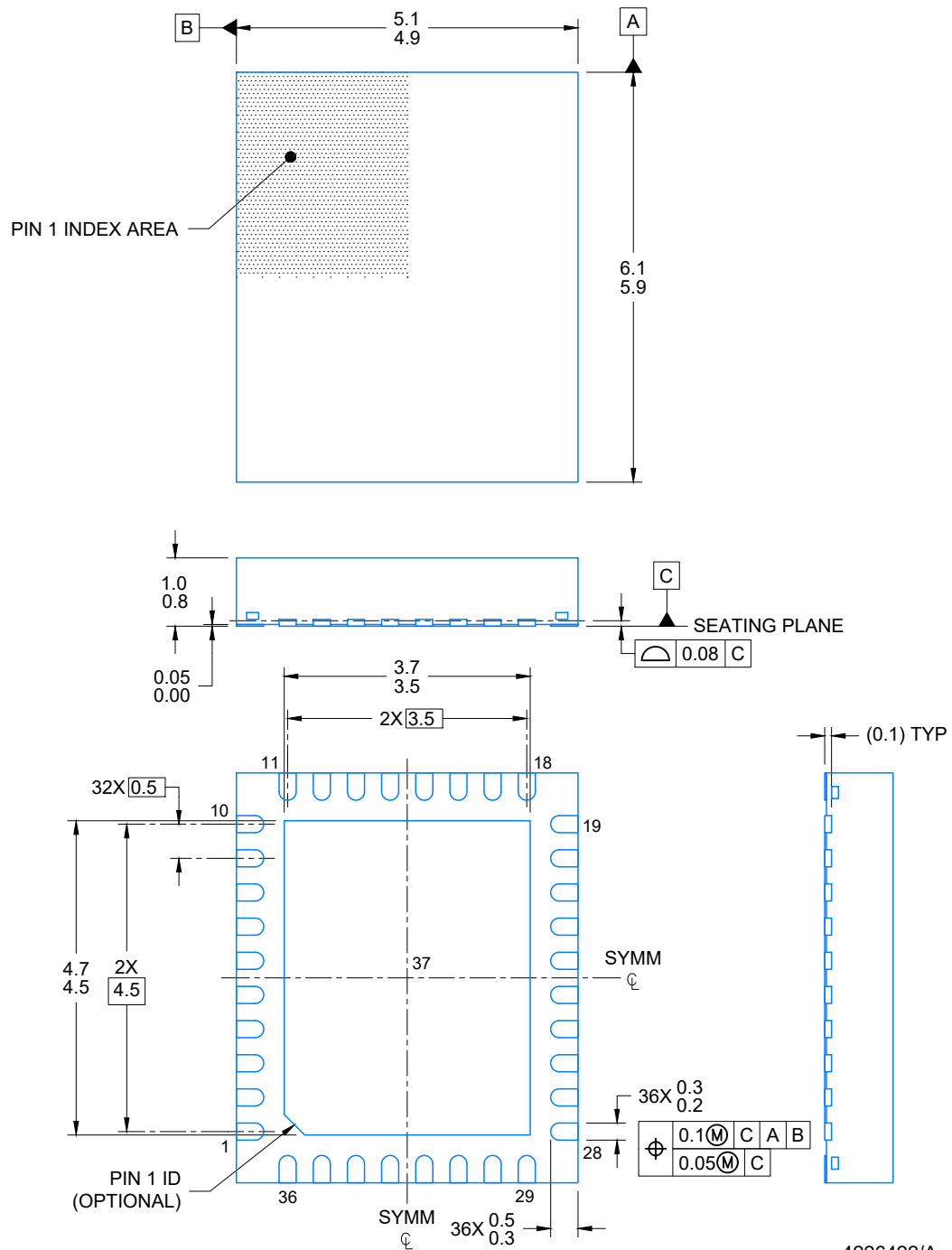
**VQFN - 1 mm max height**

5 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

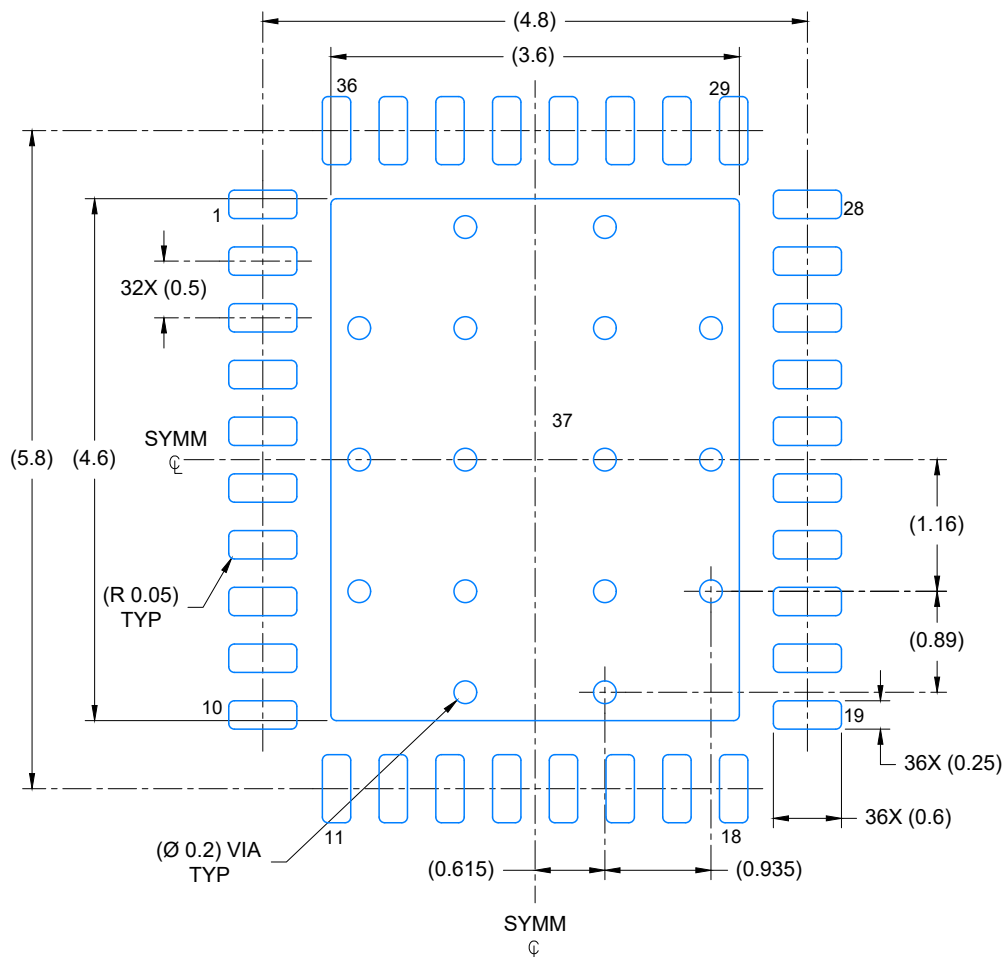




4226422/A 11/2020

NOTES:

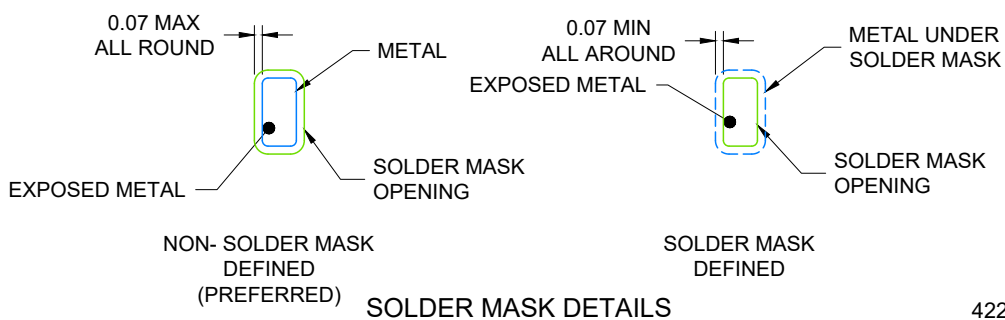
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



## LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN

SCALE: 15X

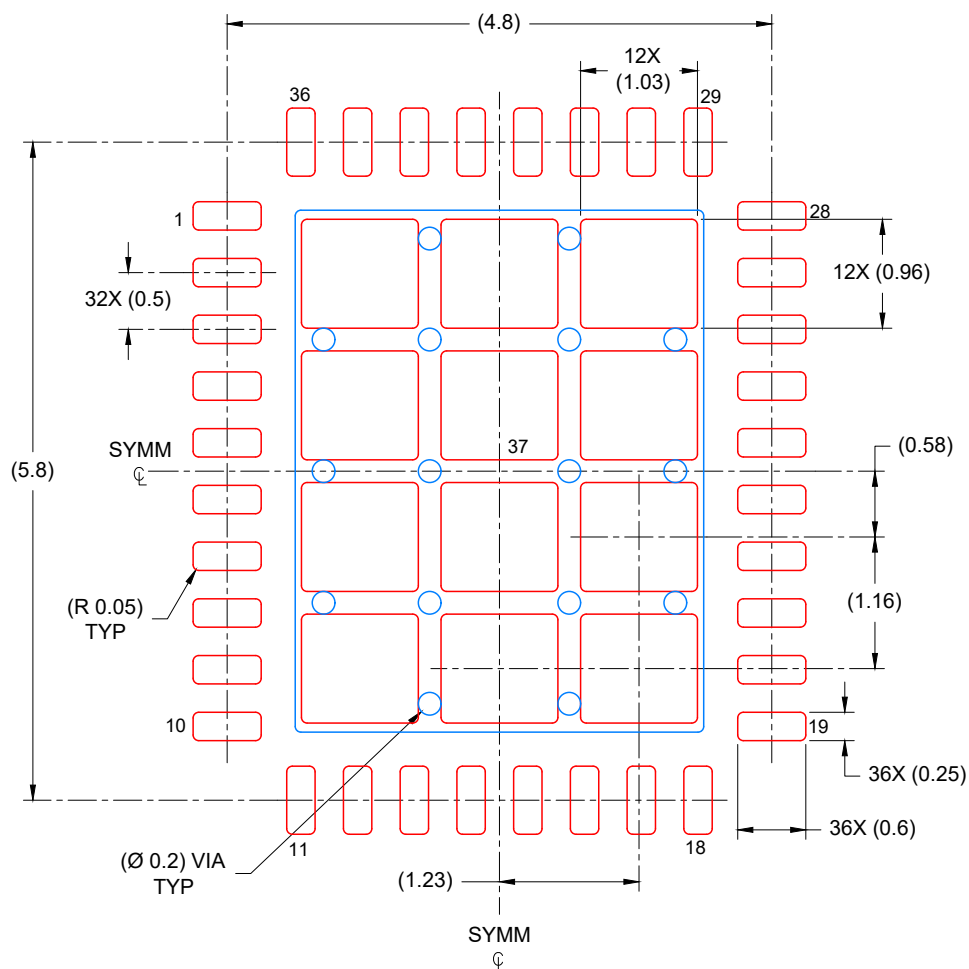


## SOLDER MASK DETAILS

4226422/A 11/2020

## NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE  
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
 72% PRINTED COVERAGE BY AREA  
 SCALE: 15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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