TPS92690 N-Channel Controller for Dimmable LED Drives With Low-Side Current Sense

1 Features

- Input Voltage Range from 4.5 to 75 V
- Adjustable Current Sense (50 to 500 mV)
- Low-Side Current Sensing
- 2-Ω MOSFET Gate Driver
- Input Undervoltage Protection
- Output Overvoltage Protection
- Cycle-by-Cycle Current Limit
- PWM Dimming Input
- Programmable Oscillator Frequency
- External Synchronization Capability
- Slope Compensation
- Programmable Soft-Start Function
- HTSSOP (PWP), 16-Pin, Exposed Pad Package

2 Applications

- LED Drivers
- Constant Current Regulator: Boost, Cuk, Flyback, and SEPIC

3 Description

The TPS92690 device is a high-voltage, low-side NFET controller with an adjustable output current sense resistor voltage. Ideal for LED drivers, it contains all of the features needed to implement current regulators based on boost, SEPIC, flyback, and Cuk topologies.

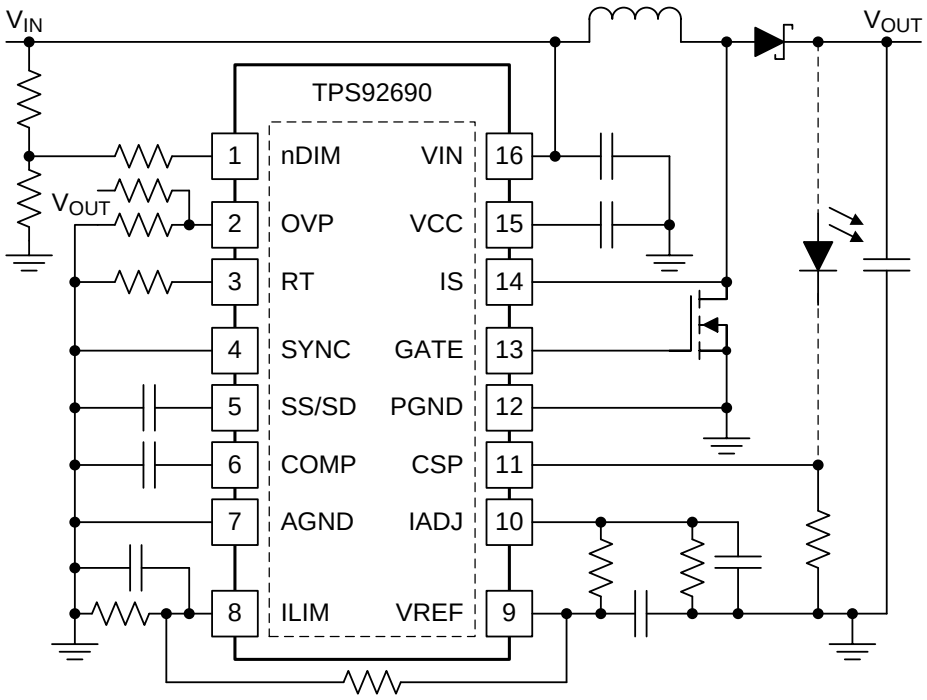
Output current regulation is based on peak current-mode control supervised by a control loop. This methodology eases the design of loop compensation while providing inherent input voltage feed-forward compensation. The TPS92690 device includes a high-voltage start-up regulator that operates over a wide input range between 4.5 and 75 V. The PWM controller is designed for high-speed capability including an oscillator frequency range up to 2 MHz. The TPS92690 device includes an error amplifier, precision reference, cycle-by-cycle current limit, and thermal shutdown.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS92690	HTSSOP (16)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Application



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

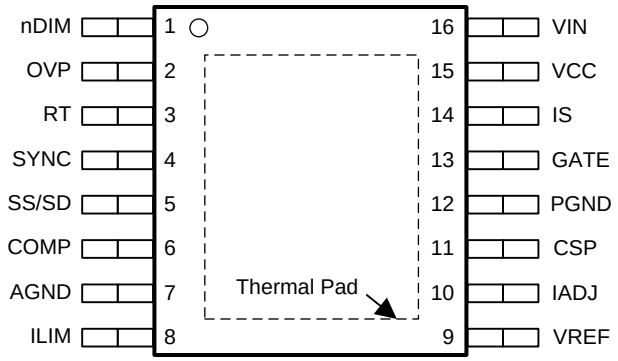
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (December 2012) to Revision A	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Separated data sheet from TPS92690-Q1. For the TPS92690-Q1 data sheet, see SLVSCU0 on www.ti.com.	1

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5 Pin Configuration and Functions

PWP Package
16-Pin HTSSOP With PowerPAD
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
AGND	7	GND	Connect to PGND through DAP exposed thermal pad for proper ground return path.
COMP	6	I	Connect ceramic capacitor to GND to set loop compensation.
CSP	11	I	Connect to positive terminal of sense resistor in series with LED stack.
GATE	13	O	Connect to main N-channel MOSFET gate of switching converter.
IADJ	10	I	Connect resistor divider from VREF to set error amplifier reference voltage.
ILIM	8	I	Connect resistor divider from VREF to set current limit threshold voltage at IS pin.
IS	14	I	Connect to drain of main N-channel MOSFET or to source of MOSFET if sense resistor is used for improved accuracy.
nDIM	1	I	Connect resistor divider from VIN to set UVLO threshold and hysteresis. Connect through diode or MOSFET to PWM dim concurrently.
OVP	2	I	Connect resistor divider from output voltage to set OVP threshold and hysteresis.
PGND	12	GND	Connect to AGND through the exposed thermal pad for proper ground return path.
RT	3	O	Connect resistor to AGND to set base switching frequency.
SS/SD	5	I	Connect capacitor to AGND to set soft-start delay. Pull pin below 75 mV for low-power shutdown.
SYNC	4	I	Connect external PWM signal to set switching frequency. Must be higher than base frequency set at RT pin. Can also connect series resistor and capacitor to drain of main MOSFET and capacitor to AGND to implement zero-crossing detection for quasi-resonant topologies. In either case, a falling edge on SYNC triggers a new on-time at GATE. If tied to ground, internal oscillator is used.
VCC	15	O	Bypass with 2.2-µF ceramic capacitor to provide bias supply for controller.
VIN	16	I	Connect to input supply of converter. Bypass with 100-nF ceramic capacitor to AGND as close to the device as possible.
VREF	9	O	Connect to the IADJ pin directly or through resistor divider. Bypass with 100-nF ceramic capacitor to AGND.
Thermal Pad		GND	

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6 Specifications

6.1 Absolute Maximum Ratings

All voltages are with respect to GND, –40°C < T_J = T_A< 125°C, all currents are positive into and negative out of the specified terminal (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage	VIN	–0.3	76	V
Input voltage	nDIM, OVP	–0.3	76	V
	IS(2)	–0.3	76	
	CSP, IADJ, SS/SD, ILIM	–0.3	6	
Output voltage	VCC, GATE(3)	–0.3	14	V
	COMP, RT, VREF	–0.3	6	
Continuous input current	IS		–1	mA
	GATE	–1	1	
	SYNC		1	
Output current	VREF		–1	mA
Operating junction temperature, T_J(4)			150	°C
Storage Temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The IS pin can sustain –2 V for 100 ns without damage.
(3) the GATE pin can sustain –2.5 V for 100 ns. The VCC pin can sustain –2.5 V for 100 ns.
(4) Maximum junction temperature is internally limited.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VIN	Input voltage	4.5	12	75	V
T_J	Operating junction temperature	–40	25	125	°C
$V_{IADJ(max)}$	Maximum operating IADJ voltage	0		5	V

6.4 Thermal Information

THERMAL METRIC(1)		TPS92690 PWP (TSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	39.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	23.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	17.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

–40°C < T_J = T_A < 125°C, V_{IN} = 14 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STARTUP REGULATOR (VCC)						
VCC_{REG}	VCC regulation voltage	I_{CC} = 0 mA	6.35	6.9	7.45	V
ICC_{LIM}	VCC current limit	V_{VCC} = 0 V	–20	–30		mA
I_Q	Quiescent current			2	3	mA
I_{SD}	Shutdown current	$V_{SS/SD}$ = 0 V		45	65	µA
VCC_{UV}	VCC UVLO threshold	V_{VCC} rising		4.1	4.50	V
		V_{VCC} falling	3.61	4.01		
VCC_{HYS}	VCC UVLO hysteresis			83		mV
REFERENCE VOLTAGE OUTPUT						
VREF	Reference voltage	No load	2.4	2.45	2.5	V
ERROR AMPLIFIER						
	CSP input bias current		–0.6	0	0.6	µA
	COMP sink current		17.1	28.5	39.9	µA
	COMP source current	V_{IADJ} = 5 V	–12.6	–16.8	–21	µA
g_M	Transconductance	V_{IADJ} = 1 V, 0 V ≤ V_{CSP} ≤ 0.8 V		33		µA/V
	Transconductance bandwidth	–6dB		1		MHz
	IADJ pin input impedance			1		MΩ
V_{CSP}	Error amplifier reference voltage	Precise value implied in offset		V_{IADJ}/10		V
	Error amplifier input offset voltage	V_{VCC} = 4.5 V, 1 V ≤ V_{COMP} ≤ 1.4 V, T_A = 25°C	–1.5	0	1.5	mV
		V_{VCC} > 6 V, 1 V ≤ V_{COMP} ≤ 3 V, V_{IADJ} ≤ 1.25 V, T_A = 25°C	–1.8	0	1.8	
		V_{VCC} > 6 V, 1 V ≤ V_{COMP} ≤3 V, V_{IADJ} > 1.25 V, T_A = 25°C (% of)	–1.44	0	1.44	V_{CSP}%
PWM COMPARATOR and SLOPE COMPENSATION						
D_{MAX}	Maximum duty cycle	Internal oscillator only	90%	94.4%		
	IS to PWM offset voltage	No slope added	950	1100	1250	mV
		D = D_{MAX} (maximum slope added)		125		
I_{OFF}	IS source current	No slope added		–11.9		µA
I_{OFF} + I_{SL}		D = D_{MAX} (maximum slope added)		–60		µA
CURRENT LIMIT						
	ILIM delay to output			60	100	ns
$t_{ON(min)}$	Leading edge blanking time			200	300	ns
	Current limit off-timer			38		µs
	ILIM offset voltage	D = 50%	–19	–5.6	5	mV
LOW POWER SHUTDOWN and SOFTSTART						
V_{SD}	Shutdown threshold voltage	$V_{SS/SD}$ falling	30	86		mV
V_{SDH}	Shutdown hysteresis			24		mV
I_{SS}	SS/SD current source	$V_{SS/SD}$ > (V_{SD} + V_{SDH})		–10.8		µA
		$V_{SS/SD}$ < V_{SD}		–1.1		µA
OSCILLATOR and EXTERNAL SYNCHRONIZATION						
f_{SW}	Switching frequency	R_{RT} = 121 kΩ	312	350	389	kHz
		R_{RT} = 100 kΩ	372	418	464	
		R_{RT} = 84.5 kΩ	436	490	544	
	SYNC threshold voltage (falling edge triggers on-time)	Rising		2.05	2.36	V
		Falling	0.95	1.31		

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Electrical Characteristics (continued)

–40°C < T_J = T_A < 125°C, V_{IN} = 14 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYNC Clamp Voltage		Positive		6.2		V
		Negative		–0.5		
OVERVOLTAGE PROTECTION						
OVP OVLO threshold		Rising		1.23	1.282	V
		Falling	1.144	1.19		
OVP hysteresis source current		OVP active (high)	–14	–21.5	–28	µA
PWM DIMMING INPUT and UVLO						
nDIM/UVLO threshold		Rising		1.23	1.285	V
		Falling	1.14	1.19		
nDIM hysteresis current			–14	–21.6	–28	µA
GATE DRIVER						
GATE sourcing resistance		GATE = High		2.4	6	Ω
GATE sinking resistance		GATE = Low		1	5	Ω
Peak GATE current		Source		–0.47		A
		Sink		1.1		A
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown temperature			175		°C
$T_{SD(hys)}$	Thermal shutdown hysteresis			25		°C

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6.6 Typical Characteristics

Unless otherwise noted, –40°C ≤ T_A = T_J ≤ 125°C, V_{VIN} = 14 V, C_{BYP} = 2.2 µF, C_{COMP} = 0.1 µF

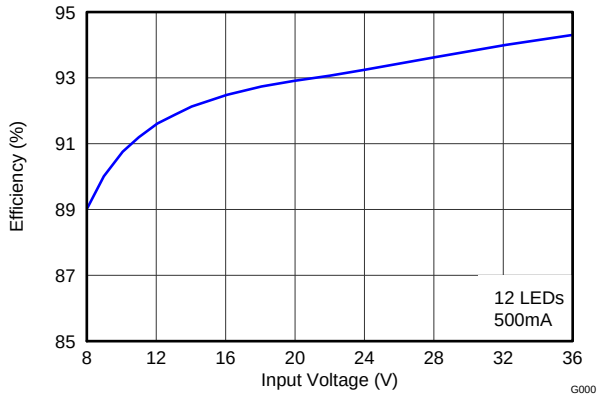


Figure 1. Boost Efficiency vs Input Voltage

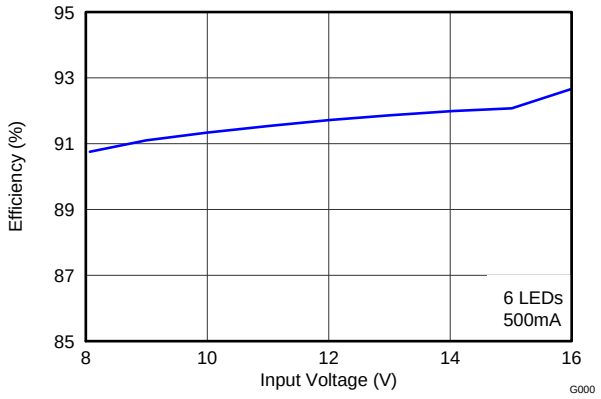


Figure 2. Boost Efficiency vs Input Voltage

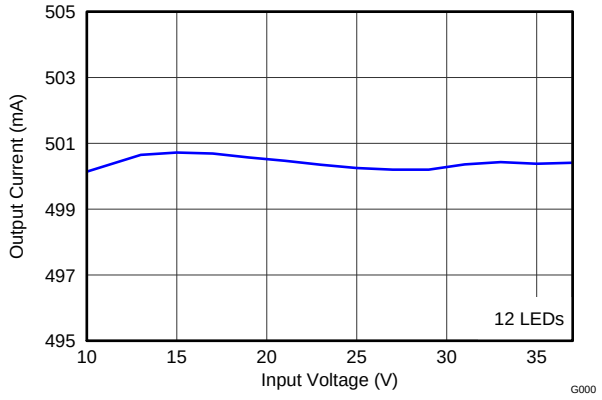


Figure 3. Boost Line Regulation

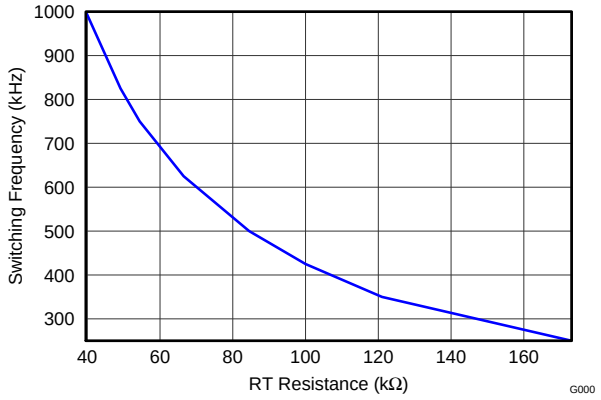


Figure 4. Switching Frequency vs RT Resistance

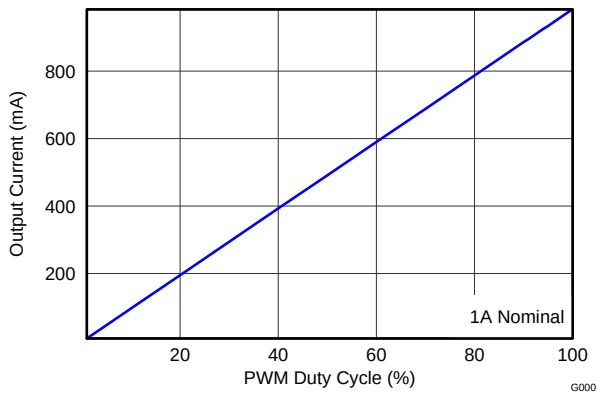


Figure 5. 160-Hz Boost PWM Dimming

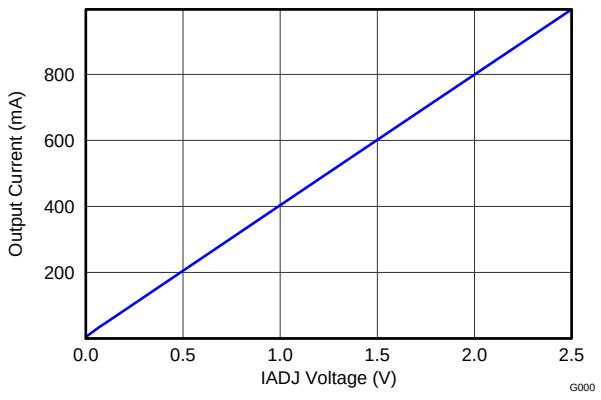


Figure 6. IADJ Analog Dimming (R_{CS} = 0.25 Ω)

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Typical Characteristics (continued)

Unless otherwise noted, –40°C ≤ T_A = T_J ≤ 125°C, V_{VIN} = 14 V, C_{BYP} = 2.2 µF, C_{COMP} = 0.1 µF

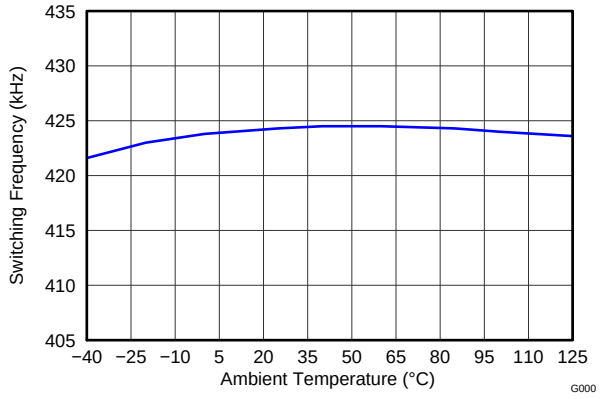


Figure 7. Switching Frequency vs Ambient Temperature (R_T = 100 kΩ)

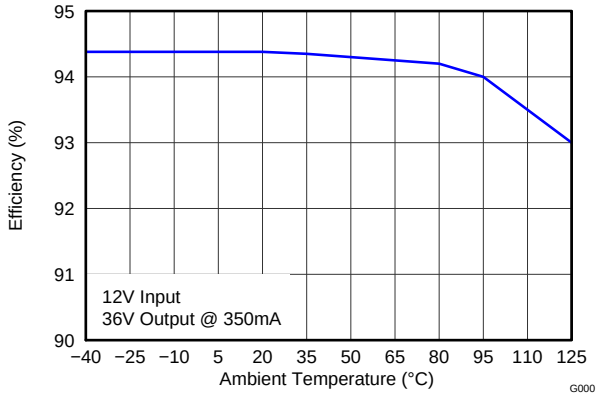


Figure 8. Efficiency vs Ambient Temperature

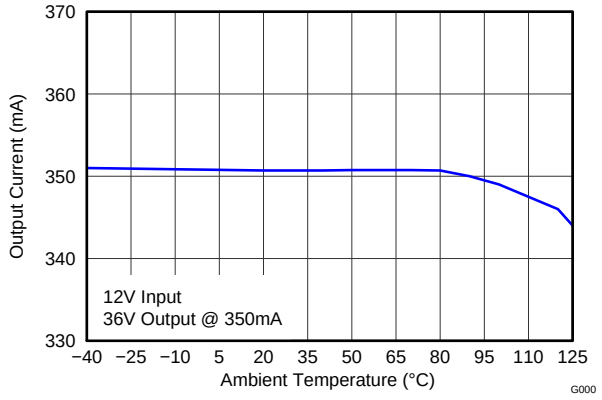


Figure 9. Output Current vs Ambient Temperature

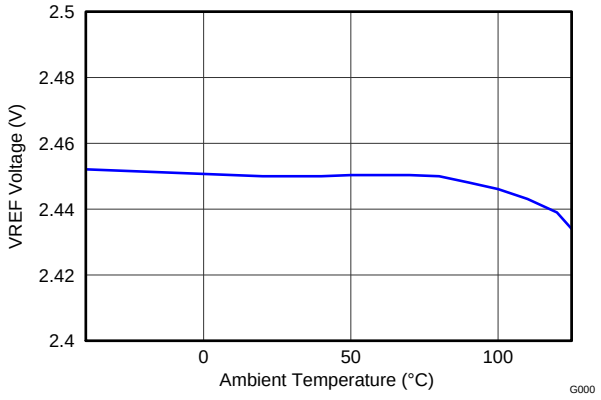


Figure 10. VREF Voltage vs Ambient Temperature

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7 Detailed Description

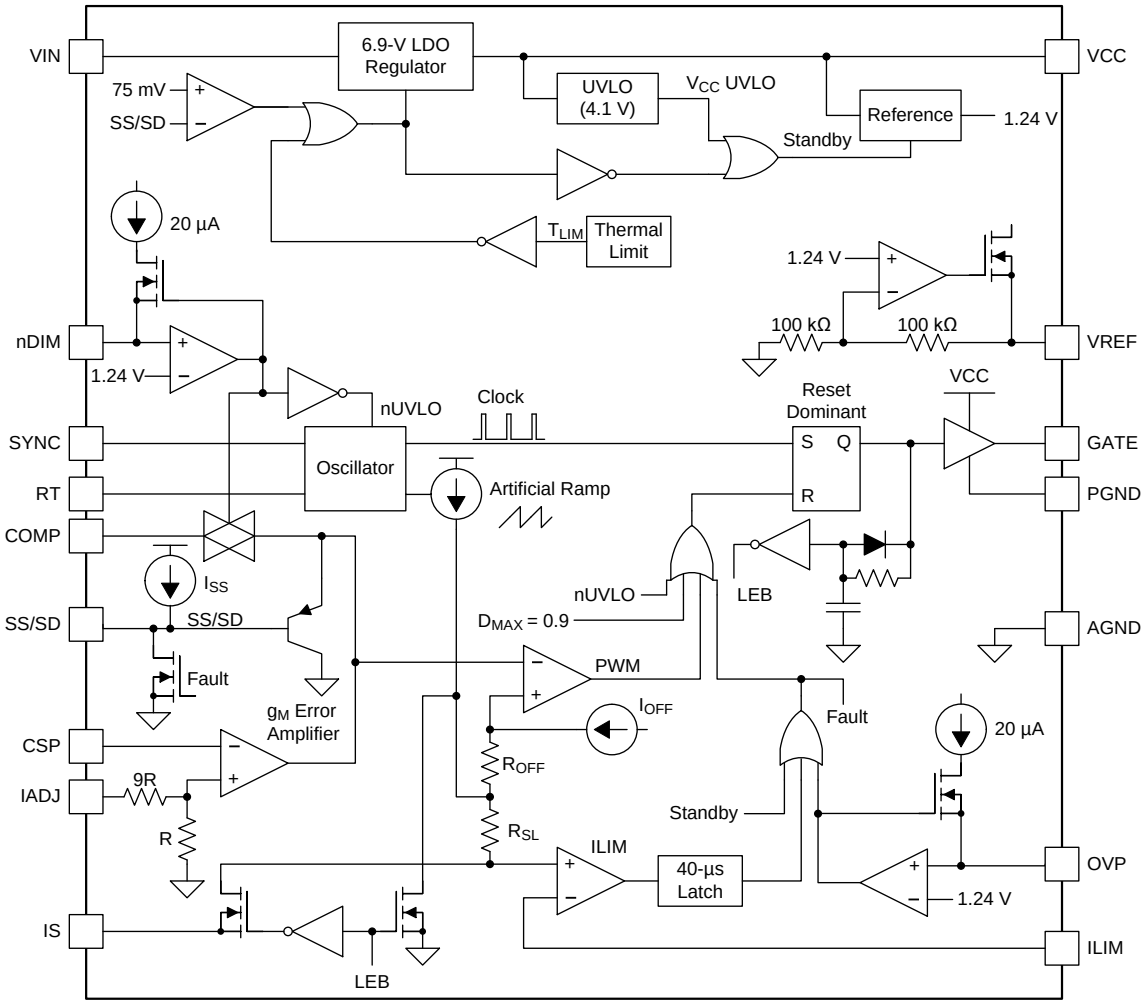
7.1 Overview

The TPS92690 device is an N-channel MOSFET (NFET) controller for boost, SEPIC, Cuk, and flyback current regulators which are ideal for driving LED loads. The controller has wide input voltage range allowing for regulation of a variety of LED loads. The low-side current sense, with low adjustable threshold voltage, provides an excellent method for regulating output current while maintaining high system efficiency.

The TPS92690 device uses peak current mode control providing good noise immunity and an inherent cycle-by-cycle current limit. The adjustable current sense threshold provides a way to analog dim the LED current, which can also be used to implement thermal foldback. The dual function nDIM pin provides a PWM dimming input that controls the main GATE output for PWM dimming the LED current also.

When designing, the maximum attainable LED current is not internally limited because the TPS92690 device is a controller. Instead it is a function of the system operating point, component choices, and switching frequency allowing the TPS92690 device to easily provide constant currents up to 5 A. This simple controller contains all the features necessary to implement a high efficiency versatile LED driver.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Current Regulators

Current regulators can be designed to accomplish different functions: boost, buck-boost, and flyback. The TPS92690 device is designed to drive a ground referenced N-channel FET and sense a ground referenced LED load. This control architecture is perfect for driving boost, SEPIC, flyback, or Cuk topologies. It does not work with a floating buck or buck-boost topology since the LED current sense amplifier is ground referenced.

Looking at the boost design in the *Typical Boost Application*, the basic operation of a current regulator can be analyzed. During the time that the N-channel FET (Q1) is turned on (t_{ON}), the input voltage source stores energy in the inductor (L1) while the output capacitor (C_O) provides energy to the LED load. When Q1 is turned off (t_{OFF}), the re-circulating diode (D1) becomes forward biased and L1 provides energy to both C_O and the LED load. Figure 11 shows the inductor current ($i_L(t)$) waveform for a regulator operating in CCM.

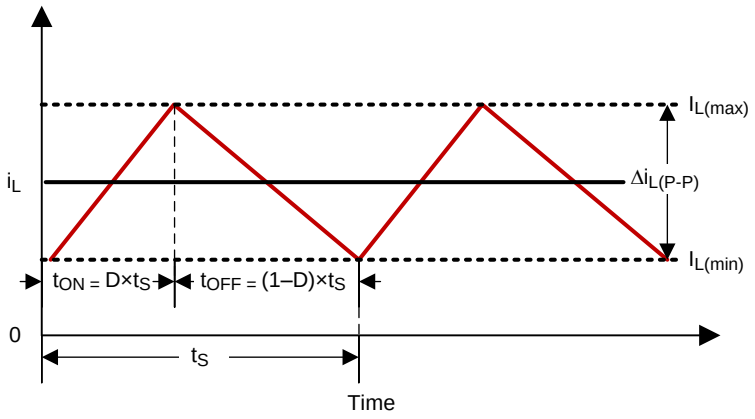


Figure 11. Basic CCM Inductor Current Waveform

The average output LED current (I_{LED}) is proportional to the average inductor current (I_L), therefore if I_L is tightly controlled, I_{LED} is well regulated. As the system changes input voltage or output voltage, the ideal duty cycle (D) is varied to regulate I_L and ultimately I_{LED}. For any current regulator, D is a function of the conversion ratio:

Use Equation 1 to calculate the duty cycle for an application using the boost topology.

$$D = \frac{V_O - V_{IN}}{V_O} \tag{1}$$

Use Equation 2 to calculate the duty cycle for an application using the buck-boost (SEPIC/Cuk) topology.

$$D = \frac{V_O}{V_O + V_{IN}} \tag{2}$$

Use Equation 3 to calculate the duty cycle for an application using the flyback topology.

$$D = \frac{nV_O}{nV_O + V_{IN}} \tag{3}$$

where

- n is the primary to secondary turns ratio of the coupled inductor, n:1

7.3.2 Peak Current Mode Control

Peak current mode control is used by the TPS92690 device to regulate the average LED current through an array of HBLEDs. This method of control uses a series resistor in the LED path to sense LED current and can use either a series resistor in the MOSFET path or the MOSFET $R_{DS(on)}$ for both cycle-by-cycle current limit and input voltage feed forward. The controller has a fixed switching frequency set by an internal programmable oscillator therefore slope compensation is added to mitigate current mode instability. A detailed explanation of this control method is presented in the following sections.

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Feature Description (continued)

7.3.3 Switching Frequency and Synchronization

The switching frequency of the TPS92690 device is programmed using an external resistor (R_T) connected from the RT pin to GND. This switching frequency is defined as shown in Equation 4.

$$f_{SW} = \frac{1}{2.29 \times 10^{-11} \times R_T + 80 \times 10^{-9}} \quad (4)$$

The *Typical Characteristics* shows a graph of switching frequency versus timing resistance on R_T. For maximum operational range and best efficiency, TI recommends a switching frequency of 1 MHz or lower. It is possible to reduce the solution size in applications with switching frequencies as high as 2 MHz in some situations. Higher frequencies require an increased gate-drive current and that can result in higher AC losses, both of which result in decreased efficiency. It is also possible that the minimum on-time (leading edge blanking time) limits the minimum operational duty cycle and reduces the input voltage range for a given output voltage.

Alternatively, an external PWM signal can be applied to the SYNC pin to synchronize the device to an external clock. If the PWM signal frequency applied is higher than the base frequency set by the timing (R_T) resistor, the internal oscillator is bypassed and the switching frequency is equal to the synchronized frequency. The PWM signal should have an amplitude between 2.5 and 5 V. The device triggers a switch-on time on the falling edge of the PWM signal and operates correctly regardless of the duty cycle of the applied signal.

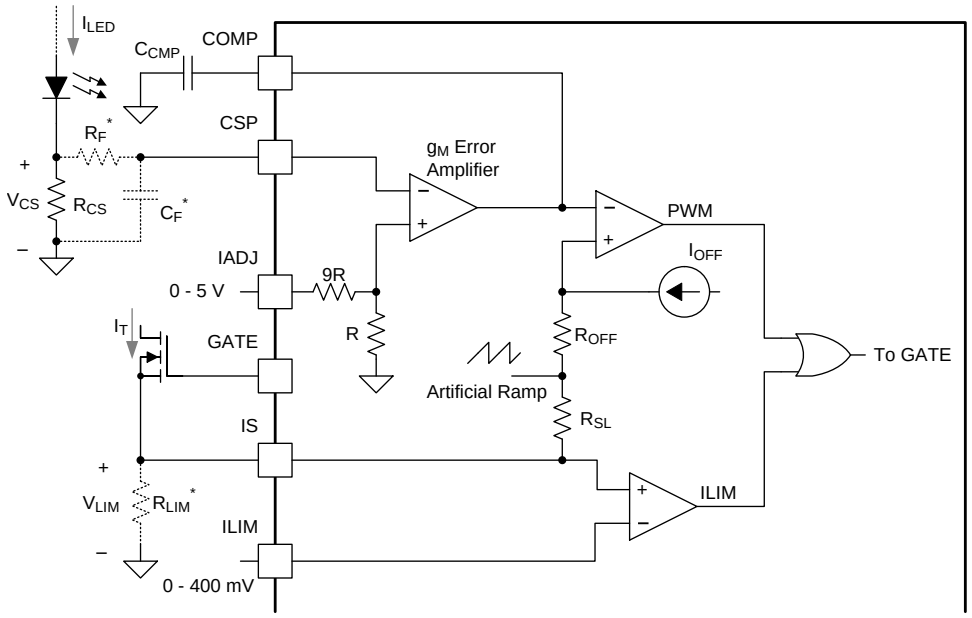


Figure 12. Current Sense and Control Circuitry (* optional)

7.3.4 Current Sense and Current Limit

The TPS92690 device implements peak current mode control using the circuit shown in Figure 12. The peak detection is accomplished with a comparator that monitors the main MOSFET current, comparing it with the COMP pin. When the IS pin voltage (plus the DC level shift and the ramp discussed later) exceeds the COMP pin voltage, the MOSFET is turned off. The MOSFET is turned back on when the oscillator starts a new on-time and the cycle repeats.

The IS pin incorporates a cycle-by-cycle overcurrent protection function. Current limit is accomplished by a redundant internal current sense comparator. If the voltage at the current sense comparator input (IS) exceeds the voltage at the ILIM pin, the MOSFET is turned off and the COMP pin is pulled to ground and discharged. The MOSFET turns back on after either the 43-µs current limit timeout has passed or after the COMP pin is recharged, whichever is longer. The IS input pin has an internal N-channel MOSFET which pulls it down at the conclusion of every cycle. The discharge device remains on an additional 216 ns (typical) after the beginning of a new cycle to blank the leading edge spike on the current sense signal. This blanking time also results in a minimum switch-on time of 216 ns which determines a minimum duty cycle dependent upon switching frequency.

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Feature Description (continued)

IS sensing can be done in one of two ways. The most accurate current sensing is accomplished by using a resistor, R_{LIM}. This adds a component that dissipates additional power but the result is higher accuracy and no limitation on the maximum MOSFET drain voltage. For applications that have a maximum MOSFET drain voltage below 75 V MOSFET $R_{DS(on)}$ sensing can be used by connecting the IS pin directly to the drain of the MOSFET and eliminating R_{LIM}. This results in higher efficiency but the accuracy depends on the accuracy of the MOSFET $R_{DS(on)}$. Care must be taken to use the maximum expected $R_{DS(on)}$ when setting the current limit threshold at the ILIM pin.

7.3.5 Average LED Current

The COMP pin voltage is dynamically adjusted, via the internal error amplifier, to maintain the desired regulation. A sense resistor in series with the LEDs sets the average LED current regulation. The voltage across the sense resistor (V_{CS}) is regulated to the IADJ voltage divided by 10.

The IADJ pin can be set to any value up to 2.45 V by connecting it to VREF through a resistor divider for static output current settings. IADJ can also be used to change the regulation point if connected to a controlled voltage source up to 5 V or potentiometer to provide analog dimming. It is also possible to configure the IADJ pin for thermal foldback functions.

$$I_{LED} = \frac{V_{CS}}{R_{CS}} \tag{5}$$

$$V_{CS} = \frac{V_{IADJ}}{10} \tag{6}$$

The TPS92690 device maintains high accuracy at any level of V_{CS}. However, the accuracy remains better with higher levels as offsets and other errors become a smaller percentage of the overall V_{CS} voltage. Power losses are also higher with higher V_{CS} voltages. A good tradeoff for accuracy and efficiency is to set the maximum V_{CS} voltage to between 100 and 250 mV.

In some applications, such as standard boost or flyback topologies, the output capacitor can be connected from the output directly to ground. In these cases the CS pin can be directly connected to R_{CS}. In other applications an additional filter may be desired on the CS pin (R_F and C_F). Use these filters with topologies where the current through R_{CS} is not continuous such as in the Cuk configuration. Another example would be a boost regulator where PWM dimming is required and the output capacitor is connected directly across the LEDs. In these cases it is recommended to add a 47-Ω resistor for R_F and a 47-nF capacitor for C_F to achieve the best accuracy and line regulation.

7.3.6 Precision Reference (VREF)

The TPS92690 device includes a precision 2.45-V reference. This can be used in conjunction with a resistor divider to set voltage levels for the ILIM pin and the IADJ pin to set the maximum current limit and LED current. It can also be used with high impedance external circuitry requiring a reference. To set the current limit (I_{CL}) using VREF you can use the following equations:

$$I_{CL} = \frac{V_{LIM}}{R_{LIM}} \tag{7}$$

$$V_{LIM} = V_{ILIM} = VREF \times \frac{R_{LIM1}}{R_{LIM1} + R_{LIM2}} \tag{8}$$

When $R_{DS(on)}$ sensing is being used substitute R_{LIM} in the above equation with $R_{DS(on)}$. A small amount of capacitance (C_{LIM}) can be placed from the ILIM pin to ground for filtering if desired. If so, a value between 47 pF and 100 nF should be used but this value should not exceed the value of C_{CMP} to avoid false triggering of the current limit. To set the IADJ voltage level using VREF use the following equation:

$$V_{IADJ} = VREF \times \frac{R_{ADJ1}}{R_{ADJ1} + R_{ADJ2}} \tag{9}$$

If desired, place a small capacitor (C_{ADJ}) from the IADJ pin to ground for additional filtering. A value between 47 pF and 100 nF should be sufficient.

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Feature Description (continued)

7.3.7 Low-Level Analog Dimming

The IADJ pin can be driven as low as 0 V. The device encounters a minimum on-time at some level, depending on the switching frequency. When the voltage on the IADJ pin falls beyond this point, the device begins to skip pulses to maintain average output current regulation. Depending on external components and regulator bandwidth this skipping may or may not result in visible flicker. If flicker is present below this level higher inductor and/or output capacitor values may help and a lower COMP pin capacitor value may help. In many cases this level occurs at very low LED current and it is more desirable to simply limit the low level on the IADJ pin as shown in Figure 13.

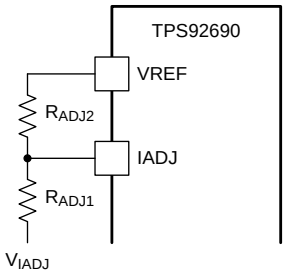


Figure 13. Limiting Minimum IADJ Voltage

The resulting IADJ voltage can be found using the following equation:

$$V_{IADJ} = (VREF - V_{ADJ}) \times \frac{R_{ADJ1}}{R_{ADJ1} + R_{ADJ2}} \quad (10)$$

7.3.8 Soft-Start and Shutdown

The TPS92690 device can be placed into low power shutdown by grounding the SS/SD pin (any voltage below 86 mV). During low power shutdown, the device limits the quiescent current to approximately 40 µA, typical.

The SS/SD pin also has a 10-µA current source (or 1 µA when below the 86-mV shutdown threshold), which charges a capacitor from SS/SD to GND to soft-start the converter. The SS/SD pin is attached through a PNP transistor to COMP therefore it controls the speed at which COMP rises at startup. When VCC_{UV} is below the falling threshold, SS/SD is pulled down to reset the capacitor voltage to zero. Then when VCC_{UV} rising threshold is exceeded, the pin is released and charges via the 10-µA current source.

7.3.9 VCC Regulator and Start-Up

The TPS92690 device includes a high voltage, low dropout bias regulator. When power is applied, or SS/SD is released, the regulator is enabled and sources current into an external capacitor (C_{BYP}) connected to the VCC pin. The recommended bypass capacitance for the VCC regulator is 2.2 to 3.3 µF. This capacitor should be rated for 10 V or greater and an X7R dielectric ceramic is recommended. The output of the VCC regulator is monitored by an internal UVLO circuit that protects the device from attempting to operate with insufficient supply voltage and the supply is also internally current limited. VCC may also be driven externally to increase the GATE voltage and reduce the $R_{DS(on)}$ of the external switching MOSFET. The maximum voltage on this pin is 14 V and should not exceed the VIN voltage. The bypass capacitor voltage rating may need to be increased accordingly.

The start-up time of the device to full output current depends on the value of C_{BYP}, C_{SS} (soft-start capacitor), C_{CMP}, and C_O (output capacitor) as shown in Figure 14:

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Feature Description (continued)

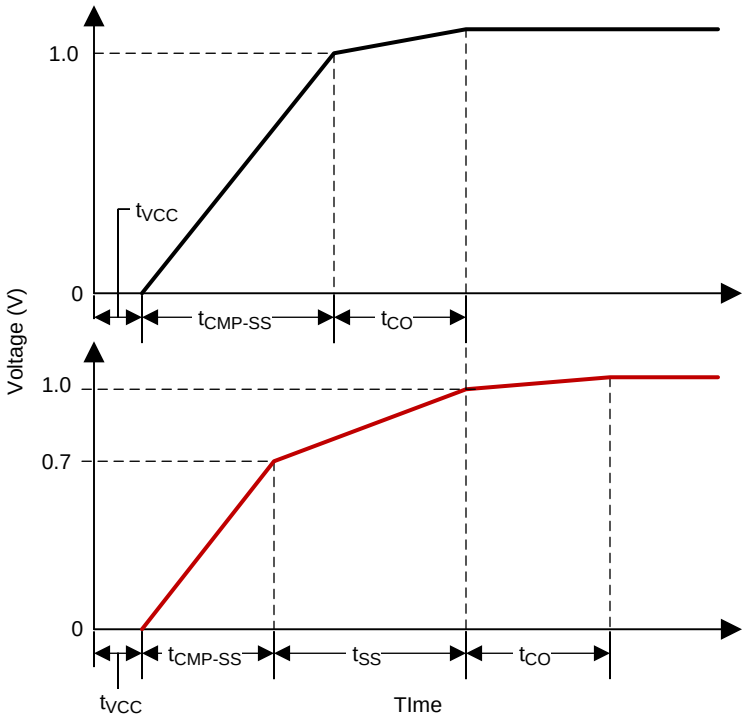


Figure 14. Start-up Waveforms

First, C_{BYP} is charged to be above the VCC UVLO threshold of 4.1 V. The C_{BYP} charging time (t_{VCC}) can be estimated as:

$$t_{VCC} = \frac{4.1V \times C_{BYP}}{30mA} \quad (11)$$

Assuming there is no C_{SS} (top trace), or if C_{SS} is less than 40% of C_{CMP}, C_{CMP} is then charged to 1V over the charging time (t_{CMP}) which can be estimated as:

$$t_{CMP} = \frac{1V \times C_{CMP}}{V_{CS} \times 35\mu S} \quad (12)$$

Once C_{CMP} = 1 V, the device starts switching to charge C_O until the LED current is in regulation. The C_O charging time (t_{CO}) can be roughly estimated as:

$$t_{CO} = \frac{C_O \times V_O}{I_{LED}} \quad (13)$$

If C_{SS} is greater than 40% of C_{CMP} (bottom trace), the compensation capacitor only charges to 0.7 V over a smaller C_{CMP} charging time (t_{CMP-SS}) which can be estimated as:

$$t_{CMP-SS} = \frac{0.7V \times C_{CMP}}{V_{CS} \times 35\mu S} \quad (14)$$

Then COMP clamps to SS, forcing COMP to rise (the last 300 mV before switching begins) according to the C_{SS} charging time (t_{SS}) which can be estimated as:

$$t_{SS} = \frac{0.3V \times C_{SS}}{11\mu A} \quad (15)$$

The system start-up time t_{SU} (for C_{SS} < 0.4 C_{CMP}) or t_{SU-SS} (for C_{SS} > 0.4 C_{CMP}) is defined as:

$$t_{SU} = t_{VCC} + t_{CMP} + t_{CO} \quad (16)$$

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Feature Description (continued)

$$t_{SU-SS} = t_{VCC} + t_{CMP-SS} + t_{SS} + t_{CO} \quad (17)$$

As a general rule of thumb, standard smooth startup operation can be achieved with C_{SS} = C_{CMP}. If SD/SS is being driven by an external source the equations above may need to be modified depending on the current sourcing capability of the external source.

7.3.10 Overvoltage Protection (OVP)

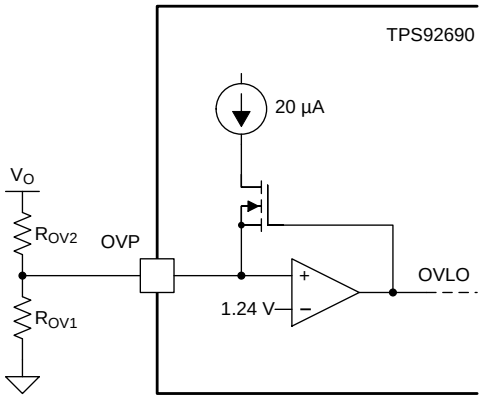


Figure 15. Overvoltage Protection Circuitry

The TPS92690 device includes a dedicated OVP pin which can be used for either input or output over-voltage protection. This pin features a precision 1.24-V threshold with 20 µA (typical) of hysteresis current as shown in Figure 15. When the OVP threshold is exceeded, the GATE pin is immediately pulled low and a 20-µA current source provides hysteresis to the lower threshold of the OVP hysteretic band.

The over-voltage turn-off threshold ($V_{TURN-OFF}$) and the hysteresis (V_{HYSO}) are defined by:

$$V_{TURN-OFF} = 1.24V \times \frac{R_{OV1} \times R_{OV2}}{R_{OV1}} \quad (18)$$

$$V_{HYSO} = 20\mu A \times R_{OV2} \quad (19)$$

7.3.11 Input Undervoltage Lockout (UVLO)

The nDIM pin is a dual function input that features an accurate 1.24-V threshold with programmable hysteresis as shown in Figure 16. This pin functions as both the PWM dimming input for the LEDs and as a VIN UVLO. When the pin voltage rises and exceeds the 1.24-V threshold, 20 µA (typical) of current is driven out of the nDIM pin into the resistor divider providing programmable hysteresis.

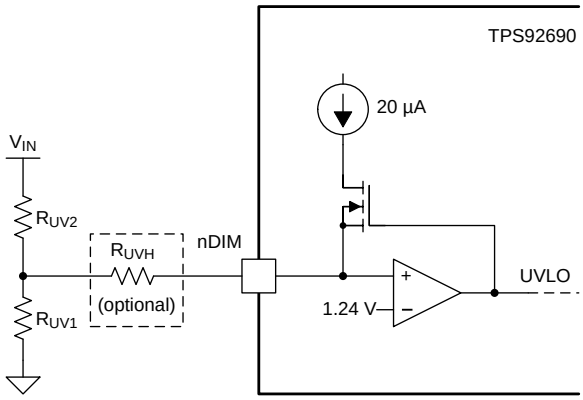


Figure 16. UVLO Circuit

Feature Description (continued)

When using the nDIM pin for UVLO and PWM dimming concurrently, the UVLO circuit can have an extra resistor to set the hysteresis. This allows the standard resistor divider to have smaller values minimizing PWM delays due to a pull-down MOSFET at the nDIM pin (see *PWM Dimming*). In general, at least 3 V of hysteresis is preferable when PWM dimming if operating near the UVLO threshold. The turn-on threshold ($V_{TURN-ON}$) is defined as follows:

$$V_{TURN-ON} = 1.24V \times \frac{R_{UV1} \times R_{UV2}}{R_{UV1}} \quad (20)$$

The hysteresis (V_{HYS}) is defined as follows:

UVLO Only

$$V_{HYS} = 20\mu A \times R_{UV2} \quad (21)$$

PWM Dimming and UVLO

$$V_{HYS} = 20\mu A \times \left(R_{UV2} + \frac{R_{UVH} \times (R_{UV1} + R_{UV2})}{R_{UV1}} \right) \quad (22)$$

7.3.12 PWM Dimming

The active low nDIM pin can be driven with a PWM signal which controls the main N-channel FET. The brightness of the LEDs can be varied by modulating the duty cycle of this signal. LED brightness is approximately proportional to the PWM signal duty cycle (that is, 30% nDIM high duty cycle equals about 30% LED brightness). This function can be ignored if PWM dimming is not required by using nDIM solely as a VIN UVLO input as described in the *Input Undervoltage Lockout (UVLO)* section or by tying it directly to VCC or VIN when UVLO is not required.

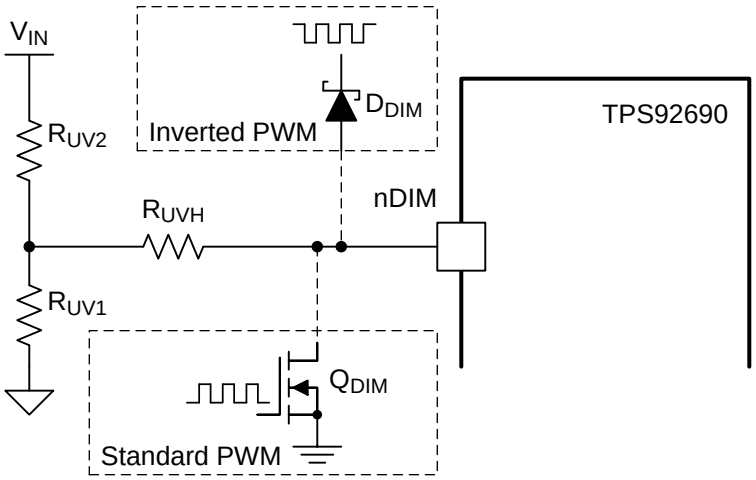


Figure 17. PWM Dimming Circuit

When using a MOSFET (QDIM), connect the drain to the nDIM pin and the source to GND. Apply an external logic-level PWM signal to the gate of Q_{DIM}. Brightness is proportional to the negative duty cycle of the PWM signal. When using a Schottky diode (D_{DIM}), connect the anode to the nDIM pin. Apply an external logic-level PWM signal to the cathode of the diode and brightness is proportional to the positive duty cycle of the PWM signal.

7.3.13 Control Loop Compensation

Compensating the TPS92690 device is relatively simple for most applications. To prevent subharmonic oscillations due to current mode control, a minimum inductor value should be chosen. This minimum value can be approximated with the following equation:

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Feature Description (continued)

$$L_{min} = \frac{V_O \times 425 \times 10^3}{2 \times f_{SW}} (\mu H) \quad (23)$$

Compensating the control loop simply requires a capacitor from the COMP pin to ground. Most LED driver applications do not require high bandwidth response since there are no significant output transients and generally limited, low bandwidth input transients. The high output impedance (R_O) of the error amplifier (typically 200MΩ) enables a low bandwidth system where standard poles and zeros, including the right half plane zero in many cases, can be neglected. In this case the bandwidth of the system generally becomes the bandwidth of the error amplifier. TI recommends a C_{CMP} value of 1 to 100 nF, which results in the following dominant pole and crossover frequency:

$$f_{P1} = \frac{1}{2\pi \times R_O \times C_{CMP}} \quad (24)$$

$$f_C = \frac{g_m}{2\pi \times C_{CMP}} \quad (25)$$

A 1-nF capacitor results in a bandwidth of approximately 5.2 kHz while a 100-nF capacitor results in a bandwidth of approximately 52 Hz. Larger values are recommended for most applications unless higher bandwidth is required. Larger values are also recommended for applications requiring PWM dimming as it allows the COMP pin to hold its level more accurately during the LED current off time. In applications where the duty cycle (D) exceeds 0.5 ($V_{IN} < V_O / 2$ for a boost regulator) the location of the right half plane zero should be calculated to ensure stability using the following equation:

$$f_{RHPZ} = \frac{r_D \times D'^2}{2\pi \times D \times L1} \quad (26)$$

Where D and D' are calculated using the minimum input voltage. The crossover frequency, f_C, should be a decade below f_{RHPZ} for maximum stability. C_{CMP} should be adjusted accordingly if required.

7.3.14 Thermal Shutdown

The TPS92690 device includes thermal shutdown protection. If the die temperature reaches approximately 175°C the device shuts down (GATE pin low). If the die temperature is allowed to cool until it reaches approximately 150°C the device resumes normal operation.

7.4 Device Functional Modes

This device has no additional functional modes

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8 Application and Implementation

NOTE

Information in the following applications sections is not included in the TI component specification, and TI does not warrant its accuracy or completeness. TI customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Inductor

The inductor (L1) is the main energy storage device in a switching regulator. Depending on the topology, energy is stored in the inductor and transferred to the load in different ways (as an example, boost operation is detailed in the *Current Regulators* section). The size of the inductor, the voltage across it, and the length of the switching subinterval (t_{ON} or t_{OFF}) determines the inductor current ripple ($\Delta i_{L\text{-}PP}$). In the design process, L1 is chosen to provide a desired $\Delta i_{L\text{-}PP}$. For a Cuk regulator the second inductor (L2) has a direct connection to the load, which is good for a current regulator. This requires little to no output capacitance therefore $\Delta i_{L\text{-}PP}$ is basically equal to the LED ripple current $\Delta i_{LED\text{-}PP}$ since the inductor ripple in L2 is equal to that in L1. However, for boost and other buck-boost regulators, there is always an output capacitor which reduces $\Delta i_{LED\text{-}PP}$, therefore the inductor ripple can be larger than in the Cuk regulator case where output capacitance is minimal or completely absent.

In general, $\Delta i_{LED\text{-}PP}$ is recommended by manufacturers to be less than 40% of the average LED current (I_{LED}). Therefore, for the Cuk regulator with no output capacitance, $\Delta i_{LED\text{-}PP}$ should also be less than 40% of I_{LED} unless a large output capacitor is used. For the boost and other buck-boost topologies, $\Delta i_{L\text{-}PP}$ can be much higher depending on the output capacitance value. However, $\Delta i_{L\text{-}PP}$ is suggested to be less than 100% of the average inductor current (i_L) to limit the RMS inductor current. $\Delta i_{L\text{-}PP}$ is defined as:

$$\Delta i_{L-PP} = \frac{V_{IN} \times D}{L \times f_{SW}} \tag{27}$$

Be sure to observe the minimum inductor value from the *Control Loop Compensation* section. L1 is also suggested to have an RMS current rating at least 25% higher than the calculated minimum allowable RMS inductor current ($I_{L\text{-}RMS}$).

8.1.2 LED Dynamic Resistance

When the load is a string of LEDs, the output load resistance is the LED string dynamic resistance plus R_{CS}. LEDs are PN junction diodes, and their dynamic resistance shifts as their forward current changes. Dividing the forward voltage of a single LED (V_{LED}) by the forward current (I_{LED}) can lead to an incorrect calculation of the dynamic resistance of a single LED (r_{LED}). The result can be 5 to 10 times higher than the true r_{LED} value.

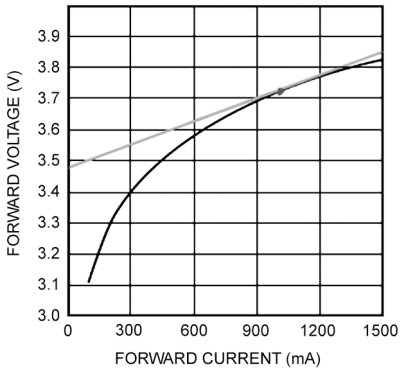


Figure 18. Dynamic Resistance

Obtaining r_{LED} is accomplished by referring to the manufacturer LED I-V characteristic. It can be calculated as the slope at the nominal operating point as shown in Figure 18. For any application with more than 2 series LEDs, R_{CS} can be neglected allowing r_D to be approximated as the number of LEDs multiplied by r_{LED}.

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Application Information (continued)

8.1.3 Output Capacitor

For boost, SEPIC, and flyback regulators, the output capacitor (C_O) provides energy to the load when the recirculating diode (D1) is reverse biased during the first switching subinterval. An output capacitor in a Cuk topology simply reduces the LED current ripple (Δi_{LED-PP}) below the inductor current ripple (Δi_{L-PP}). In all cases, C_O is sized to provide a desired Δi_{LED-PP}. As mentioned in *Inductor*, Δi_{LED-PP} is recommended by manufacturers to be <40% of the average LED current (I_{LED}).

C_O should be carefully chosen to account for derating due to temperature and operating voltage. It must also have the necessary RMS current rating. Ceramic capacitors are the best choice due to their high ripple current rating, long lifetime, and good temperature performance. An X7R dielectric rating is suggested.

8.1.4 Input Capacitor

The input capacitor (C_{IN}) only needs to provide the ripple current due to the direct connection to the inductor. C_{IN} is selected given the maximum input voltage ripple (ΔV_{IN-PP}) which can be tolerated. ΔV_{IN-PP} is suggested to be less than 10% of the input voltage (V_{IN}). An input capacitance at least 100% greater than the calculated C_{IN} value is recommended to account for derating due to temperature and operating voltage. When PWM dimming, even more capacitance can be helpful to minimize the large current draw from the input voltage source during the rising transition of the LED current waveform.

The chosen input capacitors must also have the necessary RMS current rating. Ceramic capacitors are again the best choice due to their high ripple current rating, long lifetime, and good temperature performance. An X7R dielectric rating is suggested.

For most applications, it is recommended to bypass the VIN pin with an 0.1-µF ceramic capacitor placed as close as possible to the pin. In situations where the bulk input capacitance may be far from the TPS92690 device, a 10-Ω series resistor can be placed between the bulk input capacitance and the bypass capacitor, creating a 150-kHz filter to eliminate undesired high frequency noise.

8.1.5 MOSFET Selection

The TPS92690 device requires an external N-channel FET (Q1) as the main power MOSFET for the switching regulator. Q1 is recommended to have a voltage rating at least 15% higher than the maximum transistor voltage to ensure safe operation during the ringing of the switch node. In practice, all switching regulators have some ringing at the switch node due to the diode parasitic capacitance and the lead inductance. The current rating is recommended to be at least 10% higher than the average transistor current. The power rating is then verified by calculating the power loss given the average transistor current and the N-channel FET on-resistance ($R_{DS(on)}$).

In general, the N-channel FET should be chosen to minimize total gate charge (Q_g) when f_{SW} is high and minimize $R_{DS(on)}$ otherwise. This minimizes the dominant power losses in the system. Frequently, higher current N-channel FETs in larger packages are chosen for better thermal performance.

8.1.6 Recirculating Diode

A recirculating diode (D1) is required to carry the inductor current during t_{OFF}. The most efficient choice for D1 is a Schottky diode due to low forward voltage drop and near-zero reverse recovery time. Similar to Q1, D1 is recommended to have a voltage rating at least 15% higher than the maximum transistor voltage to ensure safe operation during the ringing of the switch node and a current rating at least 10% higher than the average diode current. The power rating is verified by calculating the power loss through the diode. This is accomplished by checking the typical diode forward voltage from the I-V curve on the product datasheet and multiplying by the average diode current. In general, higher current diodes have a lower forward voltage and come in better performing packages minimizing both power losses and temperature rise.

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8.2 Typical Applications

8.2.1 Basic Topology Schematics

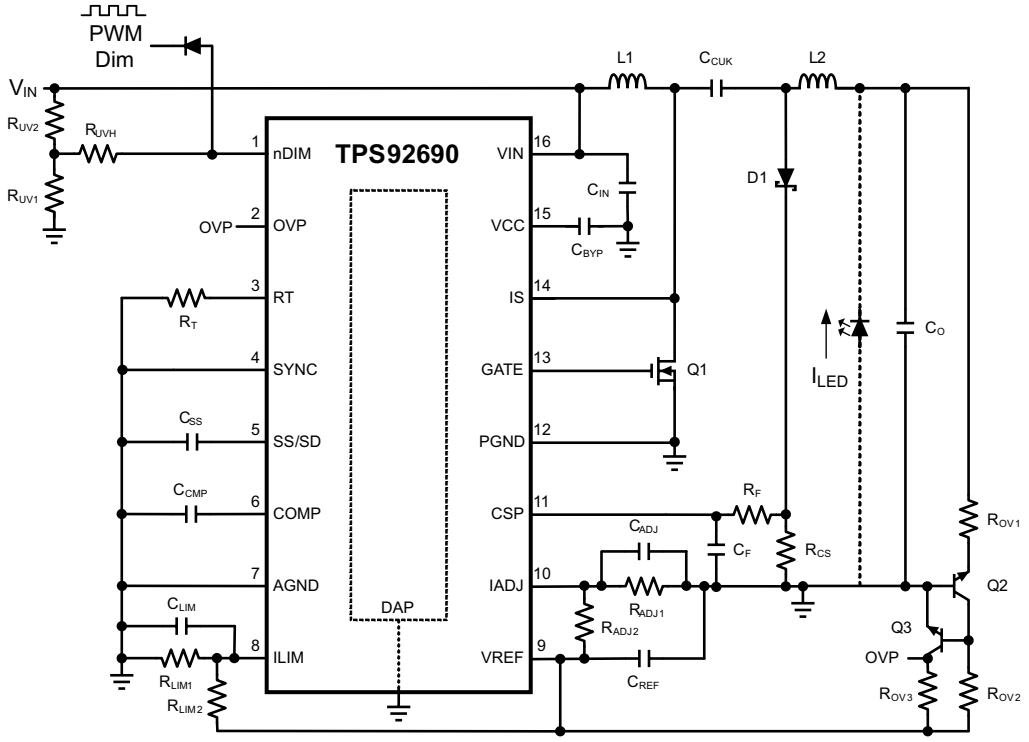


Figure 19. CUK Topology (Buck-Boost)

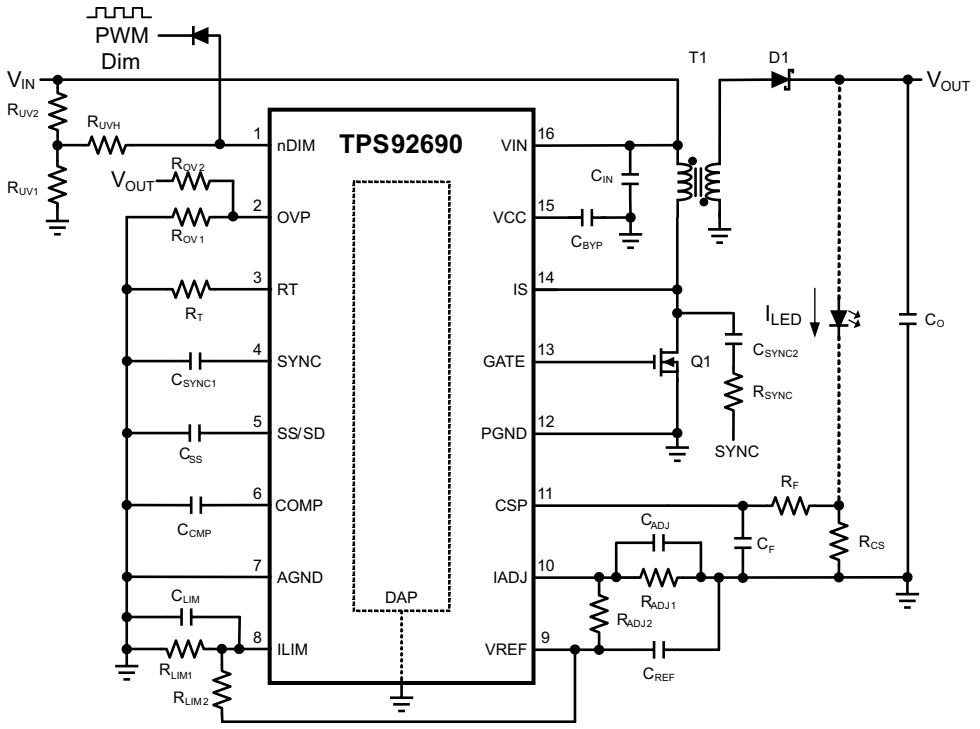


Figure 20. Quasi-Resonant Flyback Topology

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Typical Applications (continued)

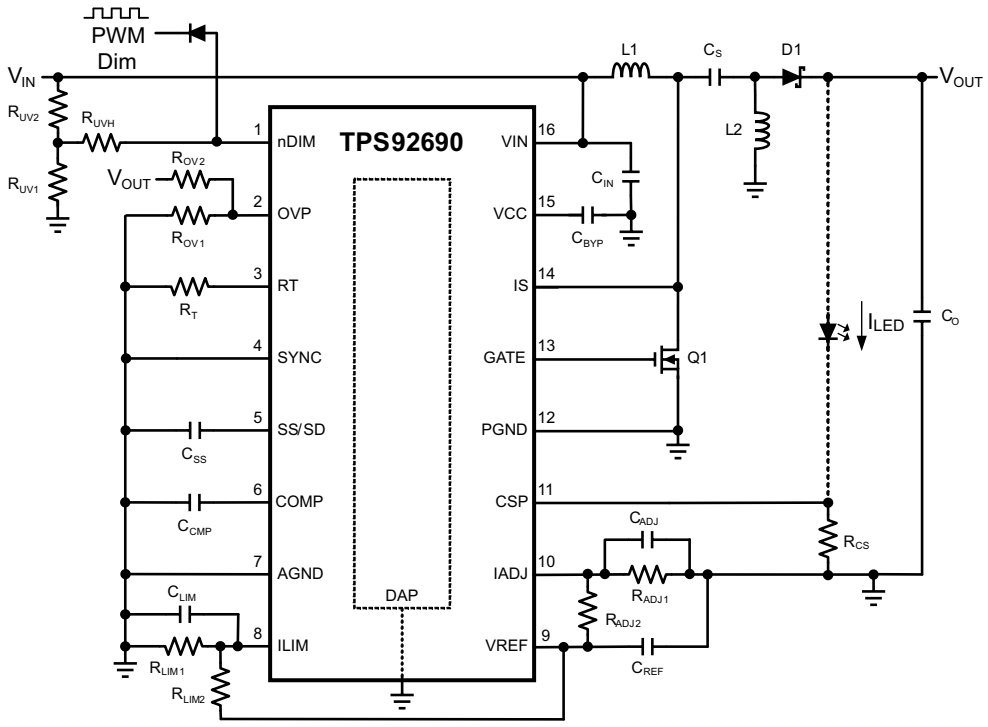


Figure 21. SEPIC Topology (Buck-Boost)

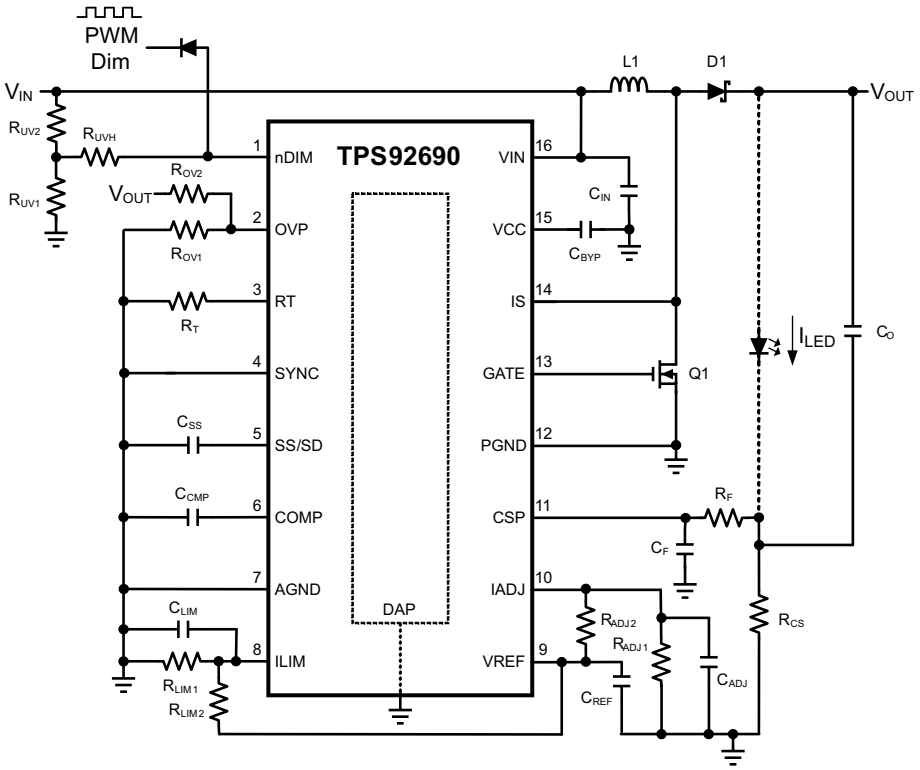


Figure 22. Boost Topology With PWM Dimming

Typical Applications (continued)

8.2.1.1 Design Requirements

N = 10

V_{LED} = 3.5 V

r_{LED} = 500 mΩ

V_{IN} = 12 V

V_{IN-MIN} = 8 V

V_{IN-MAX} = 19 V

f_{SW} = 420 kHz

V_{CS} = 50 mV

I_{LED} = 500 mA

Δi_{L-PP} < 650 mA

Δi_{LED-PP} < 50 mA

Δv_{IN-PP} = 50 mV

V_{LIM} = 100 mV

I_{LIM} = 5 A

$V_{TURN-ON}$ = 7.8 V

V_{HYS} = 2 V

$V_{TURN-OFF}$ = 40 V

V_{HYSO} = 5 V

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Operating Point

Solve for V_O and r_D:

$$V_O = N \times V_{LED} = 10 \times 3.5V = 35V \quad (28)$$

$$r_D = N \times r_{LED} = 10 \times 0.5\ \Omega = 5\ \Omega \quad (29)$$

Solve for D, D_{MAX}, and D_{MIN}:

$$D = \frac{V_O - V_{IN}}{V_O} = \frac{23}{35} = 0.657 \quad (30)$$

$$D_{MIN} = \frac{V_O - V_{IN(max)}}{V_O} = \frac{16}{35} = 0.457 \quad (31)$$

$$D_{MAX} = \frac{V_O - V_{IN(min)}}{V_O} = \frac{27}{35} = 0.771 \quad (32)$$

8.2.1.2.2 Switching Frequency

Solve for R_T:

$$R_T = \frac{1 - 80 \times 10^{-9}}{2.29 \times 10^{-11} \times 420kHz} = 103.9k\Omega \quad (33)$$

A close standard resistor is 105 kΩ resulting in f_{SW} = 402 kHz. Choose ***R_T = 105 kΩ***.

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Typical Applications (continued)

8.2.1.2.3 Average LED Current

Solve for R_{CS} using our desired 50-mV sense voltage:

$$R_{CS} = \frac{V_{CS}}{I_{LED}} = \frac{50\ mV}{500\ mA} = 0.1\Omega \tag{34}$$

Solve for V_{IADJ}:

$$V_{IADJ} = 10 \times V_{CS} = 10 \times 50mV = 500mV \tag{35}$$

A resistor divider can be used from the reference pin (VREF) to IADJ, select ***R_{IAD2} = 100 kΩ*** and solve for R_{IAD1}:

$$R_{ADj1} = \frac{R_{ADj2} \times V_{IADj}}{V_{REF} - V_{IADI}} = \frac{100\ k\Omega \times 0.5\ V}{2.5\ V - 0.5\ V} = 25\ k\Omega \tag{36}$$

The closest standard value is to choose ***R_{ADJ1} = 25.5 kΩ***.

8.2.1.2.4 Inductor Ripple Current

Solve for the minimum value of L1 for stability:

$$L1_{min} = \frac{V_O \times 425 \times 10^3}{2 \times f_{SW}} = \frac{35V \times 425 \times 10^3}{2 \times 420kHz} = 17.7\mu H \tag{37}$$

The inductor value required to meet the ripple current requirements is:

$$L = \frac{V_{IN} \times D}{\Delta i_{L-PP} \times f_{SW}} = \frac{12\ V \times 0.657}{650\ mA \times 420\ kHz} = 28.9\ \mu H \tag{38}$$

The closest standard inductor is 33 µH therefore Δi_{L-PP} is:

$$\Delta i_{L-PP} = \frac{V_{IN} \times D}{L \times f_{SW}} = \frac{12V \times 0.657}{33\mu H \times 420kHz} = 640mA \tag{39}$$

Determine minimum allowable RMS current rating:

$$I_{L-RMS} = \frac{I_{LED}}{D'} \sqrt{1 + \frac{1}{12} \times \left(\frac{\Delta I_{L-PP} \times D'}{I_{LED}} \right)^2} = \frac{500\ mA}{0.343} \sqrt{1 + \frac{1}{12} \times \left(\frac{640\ mA \times 0.343}{500\ mA} \right)^2} = 1.47\ A \tag{40}$$

The chosen component is ***L1 = 33 µH***.

8.2.1.2.5 Output Capacitance

Solve for C_O:

$$C_O = \frac{I_{LED} \times D}{r_D \times \Delta i_{LED-PP} \times f_{SW}} = \frac{500mA \times 0.657}{5\Omega \times 50mA \times 420kHz} = 3.13\mu F \tag{41}$$

Add some capacitance to account for voltage de-rating and temperature and choose ***C_O = 4.7 µF***.

Determine minimum allowable RMS current rating:

$$I_{CO-RMS} = I_{LED} \times \sqrt{\frac{D_{MAX}}{1 - D_{MAX}}} = 500\ mA \times \sqrt{\frac{0.771}{0.229}} = 0.92\ A \tag{42}$$

Since this is a PWM dimming application the output capacitor should be placed directly across the LED string and not connected to ground. So the CS pin should have additional filtering in the form of ***R_F = 47 Ω*** and ***C_F = 47 nF***.

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Typical Applications (continued)

8.2.1.2.6 Peak Current Limit

Solve for R_{LIM}:

$$R_{LIM} = \frac{V_{LIM}}{I_{LIM}} = \frac{100mV}{5A} = 0.02\Omega \quad (43)$$

The closest standard resistor is 0.02 Ω; therefore, choose ***R_{LIM} = 0.02 Ω***.

Assume ***R_{LIM2} = 100 kΩ*** and calculate R_{LIM1}:

$$R_{LIM1} = \frac{R_{LIM2} \times V_{LIM}}{V_{REF} - V_{LIM}} = \frac{100\ k\Omega \times 0.1\ V}{2.5\ V - 0.1\ V} = 4.17\ k\Omega \quad (44)$$

The closest standard value is ***R_{LIM1} = 4.22 kΩ***

8.2.1.2.7 Loop Compensation

Check the frequency of the output pole:

$$f_{pCo} = \frac{1}{2\pi \times r_D \times C_O} = \frac{1}{2\pi \times 5\ \Omega \times 4.7\ \mu F} = 6.77\ kHz \quad (45)$$

Check the frequency of the RHP zero:

$$f_{RHPZ} = \frac{r_D \times (1 - D_{MAX})^2}{2\pi \times D_{MAX} \times L1} = \frac{5\Omega \times (1 - 0.771)^2}{2\pi \times 0.771 \times 33\mu H} = 1.64kHz \quad (46)$$

The lower of the two is the RHP zero at 1.64 kHz, so the maximum crossover frequency should be 164 Hz or less. Calculate the minimum COMP capacitor value:

$$C_{CMP\,(min)} = \frac{g_m}{2\pi \times f_C} = \frac{33\mu A/V}{2\pi \times 164Hz} = 32nF \quad (47)$$

To ensure stability over all conditions add some margin and choose ***C_{CMP} = 47 nF***.

8.2.1.2.8 Input Capacitance

Solve for the minimum C_{IN}:

$$C_{IN} = \frac{\Delta i_{L-PP}}{8 \times \Delta V_{IN-PP} \times f_{SW}} = \frac{640mA}{8 \times 50mV \times 420kHz} = 3.8\mu F \quad (48)$$

To minimize power supply interaction a 200% larger capacitance or more should be used particularly with PWM dimming, therefore the actual $\Delta v_{IN\text{-}PP}$ is much lower. Choose ***C_{IN} = 10 µF***.

Determine minimum allowable RMS current rating:

$$I_{CIN-RMS} = \frac{\Delta i_{L-PP}}{\sqrt{12}} = \frac{640\ mA}{\sqrt{12}} = 185\ mA \quad (49)$$

8.2.1.2.9 NFET

Determine minimum Q1 voltage rating and current rating:

$$V_{T-MAX} = V_O = 35\ V \quad (50)$$

$$I_{T-MAX} = \frac{D_{MAX}}{1 - D_{MAX}} \times I_{LED} = \frac{0.771}{1 - 0.771} \times 500mA = 1.68A \quad (51)$$

The RMS current rating used in conjunction with the chosen FET $R_{DS\text{-}ON}$ to calculate power dissipation is:

$$I_{T-RMS} = \frac{I_{LED}}{D'} \times \sqrt{D} = \frac{500\ mA}{1 - 0.657} \times \sqrt{0.657} = 1.18\ A \quad (52)$$

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Typical Applications (continued)

8.2.1.2.10 Diode

Determine minimum D1 voltage rating and current rating:

$$V_{RD-MAX} = V_O = 35V \quad (53)$$

$$I_{D-MAX} = I_{LED} = 500mA \quad (54)$$

8.2.1.2.11 Input UVLO

Since this is a PWM dimming application R_{UVH} will be used. Start by picking ***R_{UV2}* = 10 kΩ** and solve for R_{UV1}:

$$R_{UV1} = \frac{1.24V \times R_{UV2}}{V_{TURN\ -ON} - 1.24V} = \frac{1.24V \times 10k\Omega}{7.8V - 1.24V} = 1.89k\Omega \quad (55)$$

The closest standard resistor is 1.89 kΩ so choose ***R_{UV1}* = 1.89 kΩ**.

Solve for R_{UVH} given the hysteresis requirements:

$$R_{UVH} = \frac{R_{UV1} \times (V_{HYS} - 20\mu A \times R_{UV2})}{20\mu A \times (R_{UV1} + R_{UV2})} = \frac{1.89k\Omega \times (2V - 20\mu A \times 10k\Omega)}{20\mu A \times (10k\Omega \times 1.89k\Omega)} = 14.3k\Omega \quad (56)$$

The closest standard resistor is 14.3 kΩ so choose ***R_{UVH}* = 14.3 kΩ**.

8.2.1.2.12 Output OVLO

Solve for R_{OV2}:

$$R_{OV2} = \frac{V_{HYSO}}{20\mu A} = \frac{5V}{20\mu A} = 250k\Omega \quad (57)$$

The closest standard resistor is 249 kΩ; therefore, choose ***R_{UV2}* = 249 kΩ**. Solve for R_{OV1}:

$$R_{OV1} = \frac{1.24V \times R_{OV2}}{V_{TURN\ -OFF} - 1.24V} = \frac{1.24V \times 249k\Omega}{40V - 1.24V} = 8k\Omega \quad (58)$$

Choose the nearest standard resistor value of ***R_{OV1}* = 8.06 kΩ**.

8.2.1.3 Application Curve

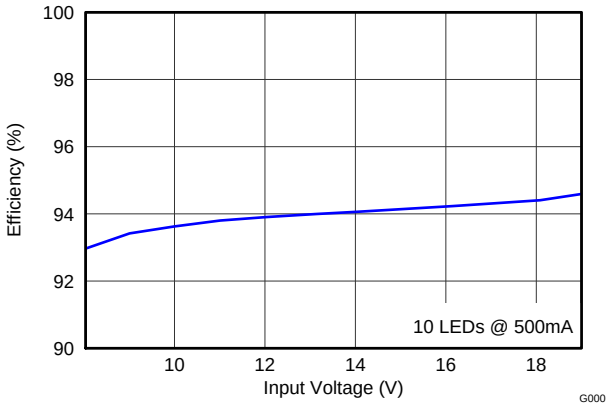


Figure 23. Efficiency vs Input Voltage

Typical Applications (continued)

8.2.2 Simplified Application

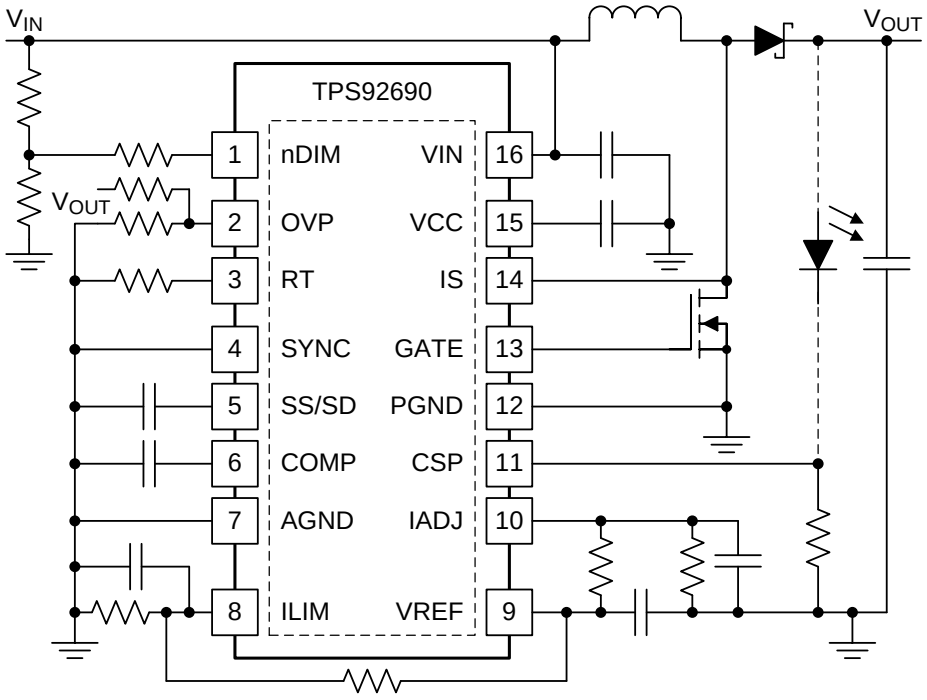


Figure 24. Simplified Application Schematic

8.2.2.1 Design Requirements

Number of series LEDs: N

Single LED forward voltage: V_{LED}

Single LED dynamic resistance: r_{LED}

Nominal input voltage: V_{IN}

Input voltage range: V_{IN-MAX}, V_{IN-MIN}

Switching frequency: f_{SW}

Current sense voltage: V_{CS}

Average LED current: I_{LED}

Inductor current ripple: Δi_{L-PP}

LED current ripple: Δi_{LED-PP}

Peak current limit: I_{LIM}

Input voltage ripple: Δv_{IN-PP}

Output OVLO characteristics: $V_{TURN-OFF}$, V_{HYSO}

Input UVLO characteristics: $V_{TURN-ON}$, V_{HYS}

Total start-up time: t_{TSU}

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Typical Applications (continued)

8.2.2.2 Detailed Design Procedure

8.2.2.2.1 Operating Point

Given the number of series LEDs (N), the forward voltage (V_{LED}) and dynamic resistance (r_{LED}) for a single LED, solve for the nominal output voltage (V_O) and the nominal LED string dynamic resistance (r_D):

$$V_O = N \times V_{LED} \tag{59}$$

$$r_D = N \times r_{LED} \tag{60}$$

Solve for the ideal nominal duty cycle (D):

Boost

$$D = \frac{V_O - V_{IN}}{V_O} \tag{61}$$

Buck-Boost

$$D = \frac{V_O}{V_O + V_{IN}} \tag{62}$$

Using the same equations, find the minimum duty cycle (D_{MIN}) using maximum input voltage (V_{IN-MAX}) and the maximum duty cycle (D_{MAX}) using the minimum input voltage (V_{IN-MIN}). Also, remember that D' = 1 - D.

8.2.2.2.2 Switching Frequency

Set the switching frequency (f_{SW}) by solving for R_T:

$$R_T = \frac{1 - 80 \times 10^{-9}}{2.29 \times 10^{-11} \times f_{SW}} \tag{63}$$

8.2.2.2.3 Average LED Current

For all topologies, set the average LED current (I_{LED}) knowing the desired current sense voltage (V_{CS}) and solving for R_{CS}:

$$V_{CS} = \frac{V_{IADJ}}{10} \tag{64}$$

$$R_{CS} = \frac{V_{CS}}{I_{LED}} \tag{65}$$

If the calculated R_{CS} is too far from a desired standard value, then V_{CS} will have to be adjusted to obtain a standard value.

Setup the IADJ voltage by assuming R_{ADJ2} = 100 kΩ and solving for R_{ADJ1}:

$$R_{ADJ1} = \frac{R_{ADJ2} \times V_{IADJ}}{V_{REF} - V_{IADJ}} \tag{66}$$

If the calculated R_{ADJ1} is too far from a desired standard value, then R_{ADJ2} can be adjusted to obtain a standard value.

8.2.2.2.4 Inductor Ripple Current

Find the minimum inductor value and calculate the nominal inductor ripple current (Δi_{L-PP}) by solving for the appropriate inductor (L1):

8.2.2.2.4.1 Minimum Inductor Value

$$L1_{min} = \frac{V_0 \times 425 \times 10^3}{2 \times f_{SW}} \ (\mu H) \tag{67}$$

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Typical Applications (continued)

8.2.2.2.4.2 Inductor Ripple Current

$$\Delta i_{L-PP} = \frac{V_{IN} \times D}{L \times f_{SW}} \quad (68)$$

If the inductor ripple current is too high given the chosen value increase L1 to get the required inductor current ripple. For buck-boost applications replace V_O with V_{IN} + V_O when solving for L1.

The minimum allowable inductor RMS current rating ($I_{L\text{-}RMS}$) can be calculated as:

8.2.2.2.4.3 RMS Inductor Current

$$I_{L\text{-}RMS} = \frac{I_{LED}}{D'} \times \sqrt{1 + \frac{1}{12} \times \left(\frac{\Delta I_{L\text{-}PP} \times D'}{I_{LED}} \right)^2} \quad (69)$$

8.2.2.2.5 LED Ripple Current

Set the nominal LED ripple current ($\Delta i_{LED\text{-}PP}$), by solving for the output capacitance (C_O):

8.2.2.2.5.1 Output Capacitor

$$C_O = \frac{I_{LED} \times D}{r_D \times \Delta i_{LED\text{-}PP} \times f_{SW}} \quad (70)$$

To set the worst case LED ripple current, use D_{MAX} when solving for C_O.

The minimum allowable RMS output capacitor current rating ($I_{CO\text{-}RMS}$) can be approximated:

8.2.2.2.5.2 Output Capacitor RMS Current

$$I_{CO\text{-}RMS} = I_{LED} \times \sqrt{\frac{D_{MAX}}{1\text{-}D_{MAX}}} \quad (71)$$

8.2.2.2.6 Peak Current Limit

Set the peak current limit (I_{LIM}) by setting the ILIM pin voltage and solving for the transistor path sense resistor (R_{LIM}):

$$V_{LIM} = V_{REF} \times \frac{R_{LIM1}}{R_{LIM1} + R_{LIM2}} \quad (72)$$

$$R_{LIM} = \frac{V_{LIM}}{I_{LIM}} \quad (73)$$

8.2.2.2.7 Loop Compensation

Using a simple first order peak current mode control model, neglecting any output capacitor ESR dynamics, the necessary loop compensation can be determined.

A maximum bandwidth (f_C) of 10 kHz is recommended and the COMP pin capacitor can be calculated using:

8.2.2.2.7.1 Compensation Capacitor

$$C_{CMP} = \frac{g_m}{2\pi \times f_C} \quad (74)$$

Check the location of the right-half plane zero and the output pole and make sure the crossover frequency is at least a decade below the lowest of the two using the following equations:

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Typical Applications (continued)

8.2.2.2.7.2 RHP Zero

$$f_{RHPZ} = \frac{r_D \times D'^2}{2\pi \times D \times L1} \quad (75)$$

8.2.2.2.7.3 Output Capacitor Pole

$$f_{pCo} = \frac{1}{2\pi \times r_D \times C_O} \quad (76)$$

If the input voltage range is wide use the maximum duty cycle (D_{MAX}) corresponding to the minimum input voltage to calculate the RHP zero. In general smaller CCMP values will provide greater bandwidth but the bandwidth may be limited by the location of the RHP zero or output pole. For PWM dimming applications the largest capacitor value that will fit the applications requirements is suggested.

8.2.2.2.8 Input Capacitance

Set the nominal input voltage ripple (Δv_{IN-PP}) by solving for the required capacitance (C_{IN}):

Boost

$$C_{IN} = \frac{\Delta i_{L-PP}}{8 \times \Delta V_{IN-PP} \times f_{SW}} \quad (77)$$

Buck-Boost

$$C_{IN} = \frac{I_{LED} \times D}{\Delta V_{IN-PP} \times f_{SW}} \quad (78)$$

Use D_{MAX} to set the worst case input voltage ripple.

The minimum allowable RMS input current rating ($I_{CIN-RMS}$) can be approximated:

Boost

$$I_{CIN-RMS} = \frac{\Delta i_{L-PP}}{\sqrt{12}} \quad (79)$$

Buck-Boost

$$I_{CIN-RMS} = I_{LED} \times \sqrt{\frac{D_{MAX}}{1-D_{MAX}}} \quad (80)$$

8.2.2.2.9 NFET

The NFET voltage rating should be at least 15% higher than the maximum NFET drain-to-source voltage (V_{T-MAX}):

Boost

$$V_{T-MAX} = V_O \quad (81)$$

Buck-Bosst

$$V_{T-MAX} = V_{IN-MAX} + V_O \quad (82)$$

The current rating should be at least 10% higher than the maximum average NFET current (I_{T-MAX}):

8.2.2.2.9.1 Maximum Average NFET Current

$$I_{T-MAX} = \frac{D_{MAX}}{1 - D_{MAX}} \times I_{LED} \quad (83)$$

Approximate the nominal RMS transistor current (I_{T-RMS}) :

Typical Applications (continued)

8.2.2.2.9.2 RMS Transistor Current

$$I_{T\text{-}RMS} = \frac{I_{LED}}{D'} \times \sqrt{D} \quad (84)$$

Given an NFET with on-resistance ($R_{DS\text{-}ON}$), solve for the nominal power dissipation (P_T):

$$P_T = I_{T\text{-}RMS}^{2} \times R_{DSON} \quad (85)$$

8.2.2.2.10 Diode

The Schottky diode voltage rating should be at least 15% higher than the maximum blocking voltage ($V_{RD\text{-}MAX}$):

Boost

$$V_{RD\text{-}MAX} = V_O \quad (86)$$

Buck-Boost

$$V_{RD\text{-}MAX} = V_{IN\text{-}MAX} + V_O \quad (87)$$

The current rating should be at least 10% higher than the maximum average diode current ($I_{D\text{-}MAX}$):

8.2.2.2.10.1 Maximum Average Diode Current

$$I_{D\text{-}MAX} = I_{LED} \quad (88)$$

Replace D_{MAX} with D in the $I_{D\text{-}MAX}$ equation to solve for the average diode current (I_D). Given a diode with forward voltage (V_{FD}), solve for the nominal power dissipation (P_D):

$$P_D = I_D \times V_{FD} \quad (89)$$

8.2.2.2.11 Output OVLO

The output OVLO is programmed with the turn-off threshold voltage ($V_{TURN\text{-}OFF}$) and the desired hysteresis (V_{HYSO}). To set V_{HYSO}, solve for R_{OV2}:

$$R_{OV2} = \frac{V_{HYSO}}{20\,\mu A} \quad (90)$$

To set $V_{TURN\text{-}OFF}$, solve for R_{OV1}:

$$R_{OV1} = \frac{1.24V \times R_{OV2}}{V_{TURN\text{-}OFF} - 1.24V} \quad (91)$$

8.2.2.2.12 Input UVLO

For all topologies, input UVLO is programmed with the turn-on threshold voltage ($V_{TURN\text{-}ON}$) and the desired hysteresis (V_{HYS}).

Method 1: If no PWM dimming is required, a two resistor network can be used. To set V_{HYS}, solve for R_{UV2}:

$$R_{UV2} = \frac{V_{HYS}}{20\,\mu A} \quad (92)$$

To set $V_{TURN\text{-}ON}$, solve for R_{UV1}:

$$R_{UV1} = \frac{1.24V \times R_{UV2}}{V_{TURN\text{-}ON} - 1.24V} \quad (93)$$

Method 2: If PWM dimming is required, a three resistor network is suggested. To set $V_{TURN\text{-}ON}$, assume R_{UV2} = 10 kΩ and solve for R_{UV1} as in Method 1. To set V_{HYS}, solve for R_{UVH}:

$$R_{UVH} = \frac{R_{UV1} \times (V_{HYS} - 20\,\mu A \times R_{UV2})}{20\,\mu A \times (R_{UV1} + R_{UV2})} \quad (94)$$

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Typical Applications (continued)

8.2.2.2.13 Soft-Start

For all topologies, if soft-start is desired, find the start-up time without C_{SS} (t_{SU}):

$$t_{SU} = t_{VCC} + t_{CMP} + t_{CO} \quad (95)$$

Then, if the desired total start-up time (t_{TSU}) is larger than t_{SU}, solve for the base start-up time ($t_{SU\text{-}SS\text{-}BASE}$), assuming that a C_{SS} greater than 40% of C_{CMP} will be used:

$$t_{SU\text{-}SS\text{-}BASE} = 168\Omega \times C_{BYP} + 28\,k\Omega \times C_{CMP} + \frac{V_O}{I_{LED}} \times C_O \quad (96)$$

Then solve for C_{SS}:

$$C_{SS} = \frac{10\,\mu A}{0.2V} \times (t_{TSU} - t_{SU\text{-}SS\text{-}BASE}) \quad (97)$$

8.2.2.2.14 PWM Dimming Method

PWM dimming can be performed several ways:

Method 1: Connect the dimming MosFET (Q_3) with the drain to the nDIM pin and the source to GND. Apply an external PWM signal to the gate of Q_{DIM}. A pull down resistor may be necessary to properly turn off Q_3.

Method 2: Connect the anode of a Schottky diode to the nDIM pin. Apply an external inverted PWM signal to the cathode of the same diode.

8.2.2.2.15 Analog Dimming Method

Analog dimming can be performed several ways:

Method 1: Place a potentiometer in place of R_{IADJ1}.

Method 2: Connect a controlled voltage source to the IADJ pin to control the current sense voltage (V_{CS}).

9 Power Supply Recommendations

9.1 Bench Supply Current Limit

It is important to set the output current limit of your input supply to an appropriate value to avoid delays in your converter analysis and optimization. If not set high enough, current limit can be tripped during start up or when your converter output power is increased, causing a foldback or shut-down condition. It is a common oversight when powering up a converter for the first time.

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10 Layout

10.1 Layout Guidelines

The performance of any switching regulator depends as much upon the layout of the PCB as the component selection. Following a few simple guidelines maximizes noise rejection and minimizes the generation of EMI within the circuit.

Discontinuous currents are the most likely to generate EMI, therefore care should be taken when routing these paths. In the boost regulator, the discontinuous current flows through the output capacitor (C_O), D1, Q1, and R_{LIM} (if used). These loops should be kept as small as possible and the connections between all the components should be short and thick to minimize parasitic inductance. In particular, the switch node (where L1, D1 and Q1 connect) should be just large enough to connect the components. To minimize excessive heating, large copper pours can be placed adjacent to the short current path of the switch node.

The RT, COMP, CSP, IS, IADJ, ILIM, and SYNC pins are all high-impedance inputs which couple external noise easily. Therefore, the loops containing these nodes should be minimized whenever possible.

In some applications the LED or LED array can be far away (several inches or more) from the TPS92690, or on a separate PCB connected by a wiring harness. When an output capacitor is used and the LED array is large or separated from the rest of the regulator, the output capacitor should be placed close to the LEDs to reduce the effects of parasitic inductance on the AC impedance of the capacitor.

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10.2 Layout Example

Note critical paths and component placement:

Minimize power loop containing discontinuous currents

Minimize signal current loops (components close to IC)

- Ground plane under IC for signal routing helps minimize noise coupling

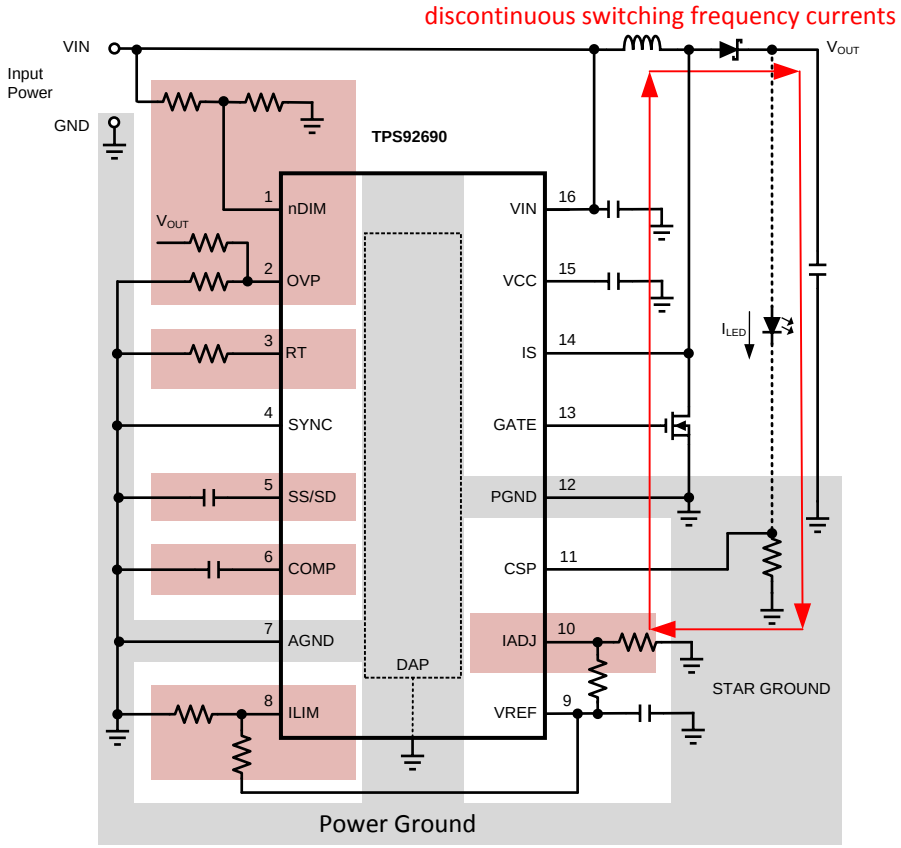


Figure 25. Layout Recommendation

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS92690PWP/NOPB	Active	Production	HTSSOP (PWP) | 16	92 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	TP92690 PWP
TPS92690PWP/NOPB.A	Active	Production	HTSSOP (PWP) | 16	92 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	TP92690 PWP
TPS92690PWP/NOPB.B	Active	Production	HTSSOP (PWP) | 16	92 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	TP92690 PWP
TPS92690PWPR/NOPB	Active	Production	HTSSOP (PWP) | 16	2500 | LARGE T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 125	TP92690 PWP
TPS92690PWPR/NOPB.A	Active	Production	HTSSOP (PWP) | 16	2500 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	TP92690 PWP
TPS92690PWPR/NOPB.B	Active	Production	HTSSOP (PWP) | 16	2500 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	TP92690 PWP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS92690 :

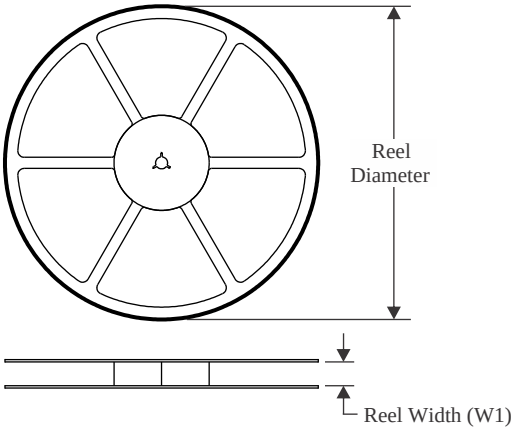
- Automotive : TPS92690-Q1

NOTE: Qualified Version Definitions:

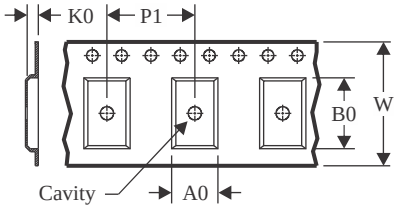
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

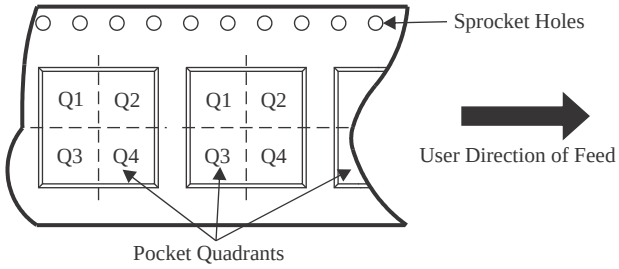


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

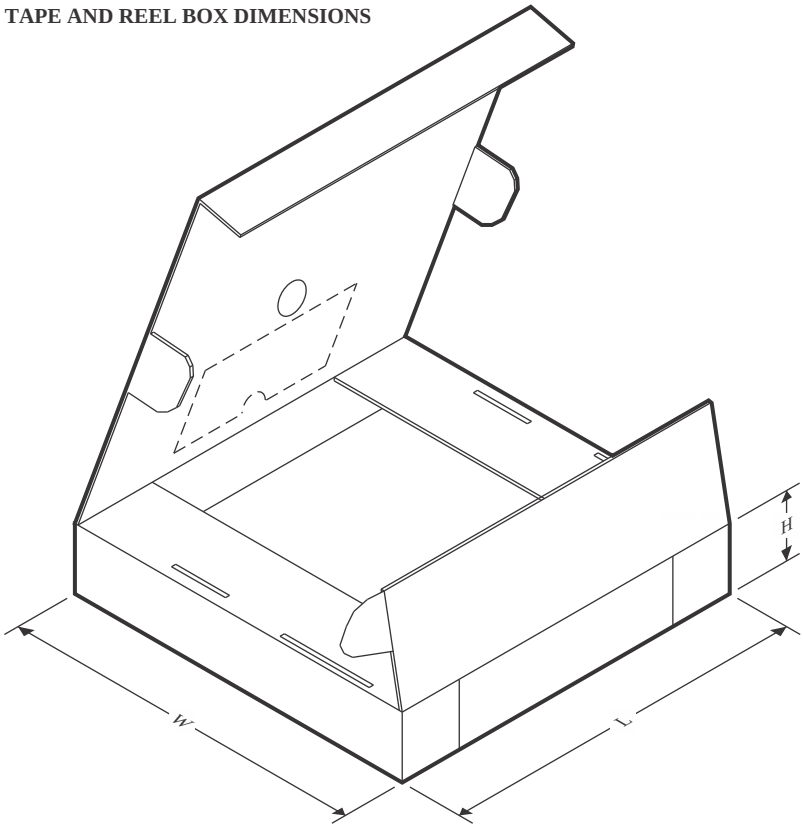
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS92690PWPR/NOPB	HTSSOP	PWP	16	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

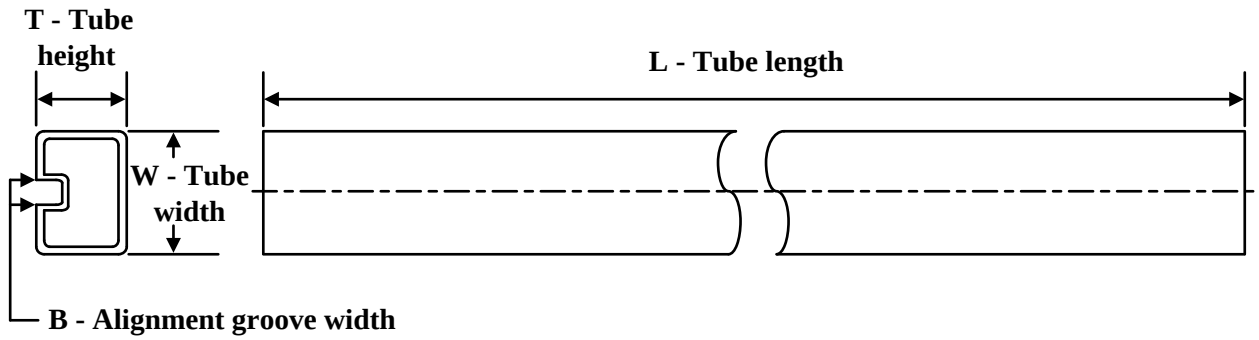
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS92690PWPR/NOPB	HTSSOP	PWP	16	2500	367.0	367.0	35.0

TUBE

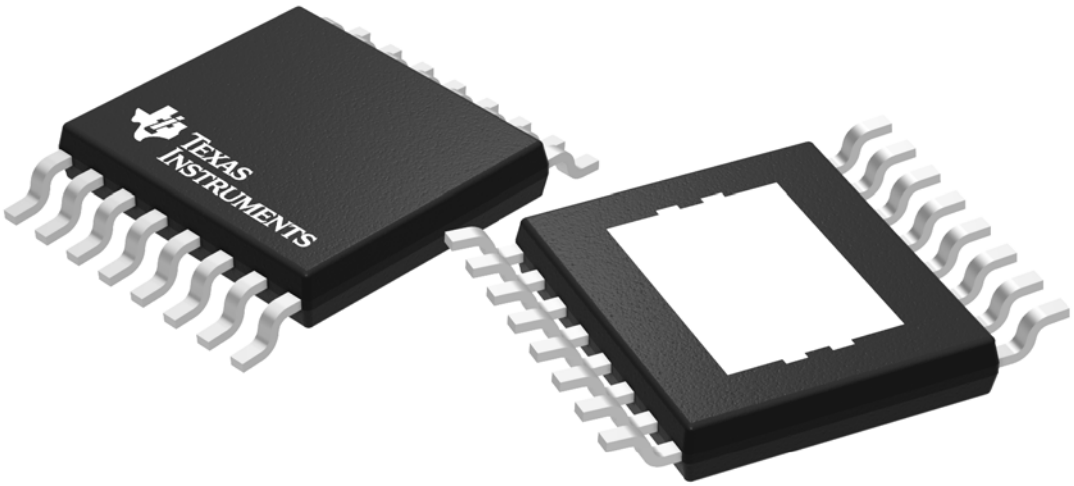


*All dimensions are nominal

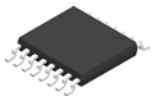
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS92690PWP/NOPB	PWP	HTSSOP	16	92	495	8	2514.6	4.06
TPS92690PWP/NOPB.A	PWP	HTSSOP	16	92	495	8	2514.6	4.06
TPS92690PWP/NOPB.B	PWP	HTSSOP	16	92	495	8	2514.6	4.06

PWP 16 PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

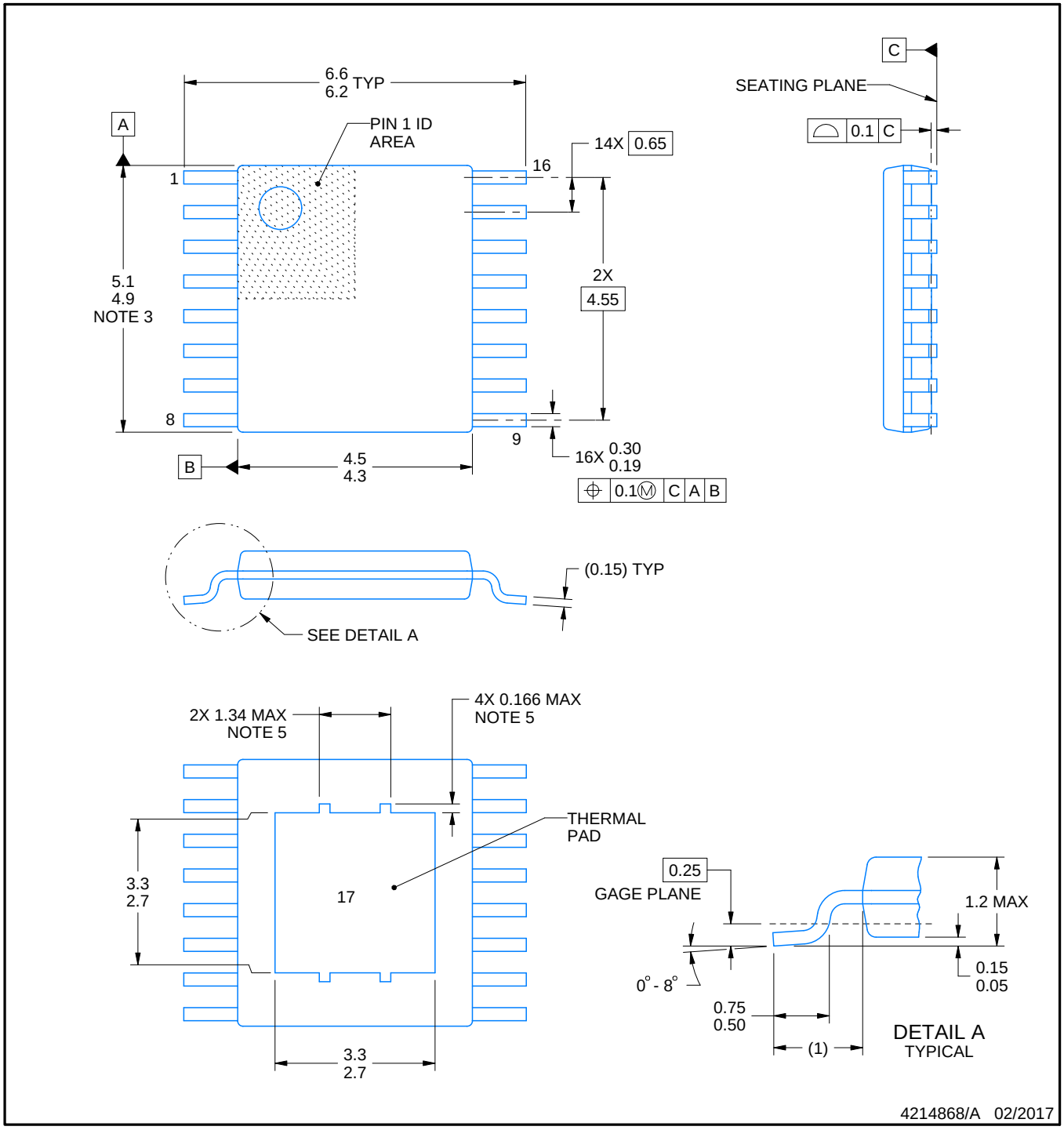


PACKAGE OUTLINE

PWP0016A

PowerPAD ™ HTSSOP - 1.2 mm max height

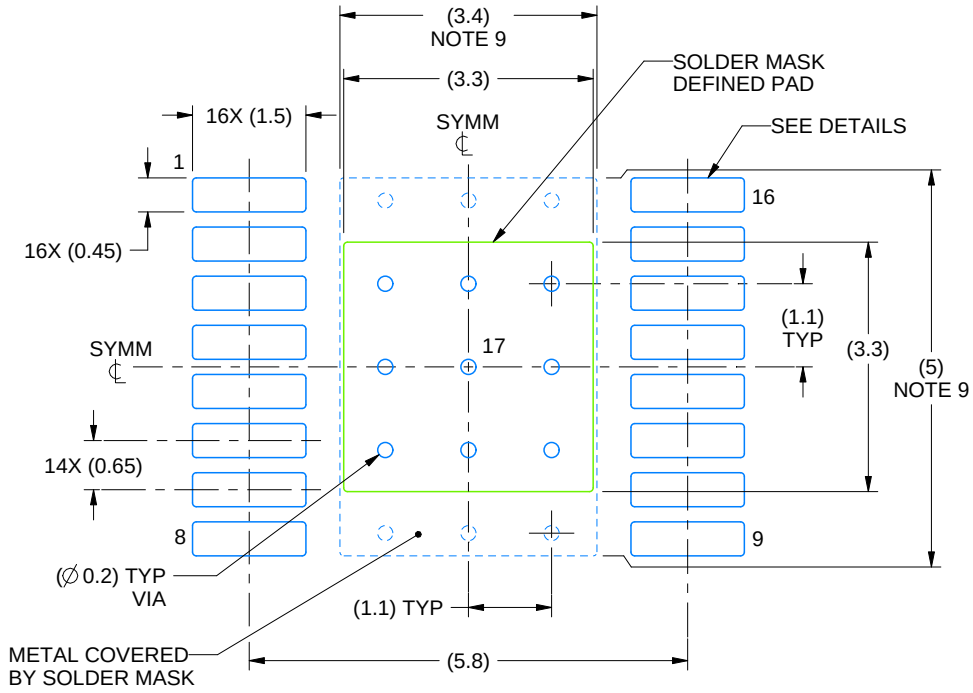
PLASTIC SMALL OUTLINE



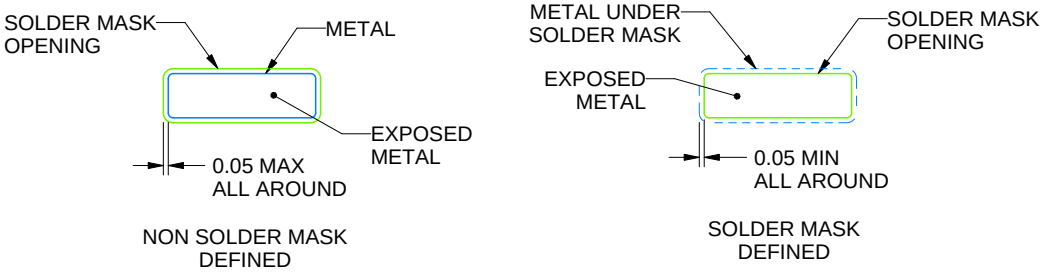
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:10X

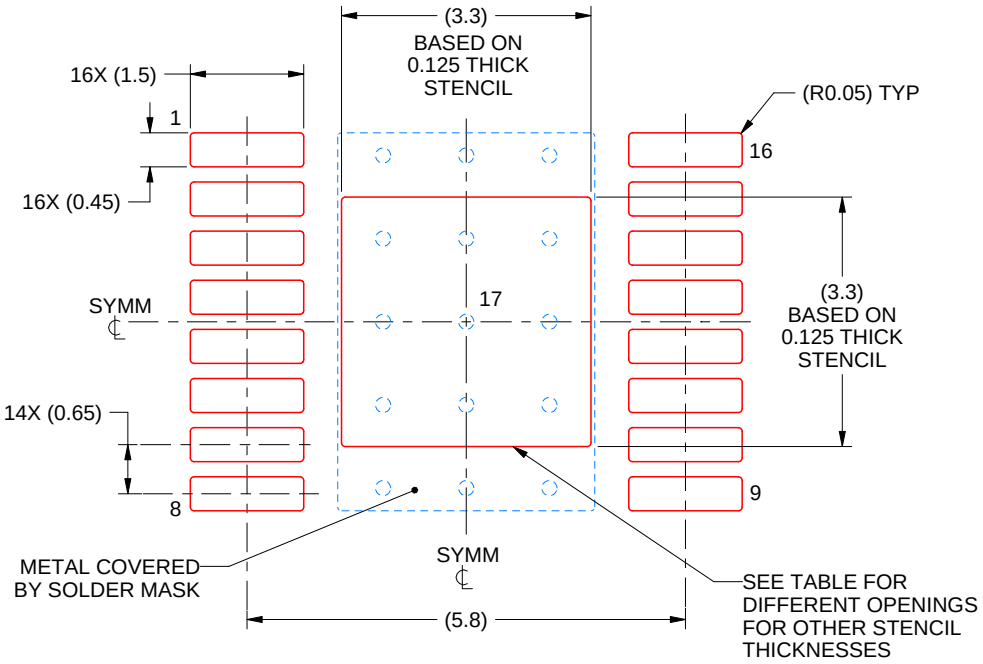


SOLDER MASK DETAILS
PADS 1-16

4214868/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.69 X 3.69
0.125	3.3 X 3.3 (SHOWN)
0.15	3.01 X 3.01
0.175	2.79 X 2.79

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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