TPSI3052A-Q1 Automotive Reinforced Isolated Switch Driver With Integrated 17V Gate Supply

1 Features

- No isolated secondary supply required
- Drives external power transistors or SCRs
- 5kV$_{RMS}$ reinforced isolation
- 17V gate drive with 1.5/2.5A peak source and sink current
- Up to 40mW supply for external auxiliary circuitry
- Supports AC or DC switching
- Drop-in replacement for existing TPSI305x devices using 3-wire mode
- Automatic power transfer regulation
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- AEC Q-100 qualified for automotive applications:
  - Temperature grade 1: –40 to +125°C, T$_A$
- Safety-Related Certifications
  - 7071V$_{PK}$ reinforced isolation per DIN EN IEC 60747-17 (VDE 0884-17)
  - 5kV$_{RMS}$ isolation for 1 minute per UL 1577

2 Applications

- Solid state relay (SSR)
- Battery management system
- On-board charger
- Hybrid, electric, and powertrain system
- Building automation
- Factory automation and control

3 Description

The TPSI3052A-Q1 is a fully integrated, isolated switch driver, which when combined with an external power switch, forms a complete isolated solid state relay (SSR). With a nominal gate drive voltage of 17V with 1.5/2.5A peak source and sink current, a large variety of external power switches can be selected to meet a wide range of applications. The TPSI3052A-Q1 generates its own secondary bias supply from the power received from its primary side, so an isolated secondary supply bias is not required. Additionally, the TPSI3052A-Q1 can optionally supply power to external supporting circuitry for various application needs.

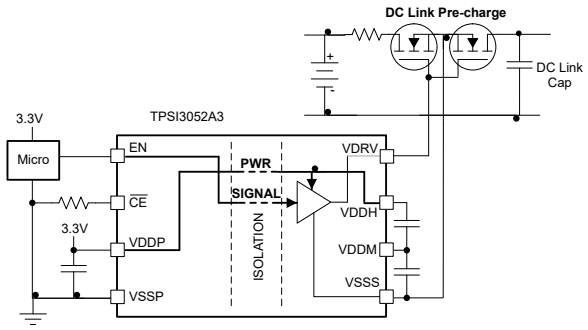
Available in three-wire mode only, the TPSI3052A-Q1 features low emissions technology, allowing the device to pass [CISPR25 Class 5 emission in many applications]. The power transfer of the TPSI3052A-Q1 is automatically controlled by bidirectional communication between the primary and secondary side. This allows the device to transfer only as much power as needed, further lowering emissions in many applications.

The secondary side provides a regulated, floating supply rail of 17V for driving a large variety of power switches with no need for a secondary bias supply. The application can drive single power switches for DC applications or dual back-to-back power switches for AC applications, as well as various types of SCR. The TPSI3052A-Q1 integrated isolation protection is extremely robust with much higher reliability, lower power consumption, and increased temperature ranges than traditional mechanical relays and optocouplers.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPSI3052A-Q1	SOIC 8-pin (DWZ)	7.50mm × 5.85mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



TPSI3052A-Q1 Simplified Schematic

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4 Device Comparison

Table 4-1. Device Comparison Table

VARIANT	DESCRIPTION
TPSI3052A3	3.3V Input Voltage
TPSI3052A5	5.0V Input Voltage

5 Pin Configuration and Functions

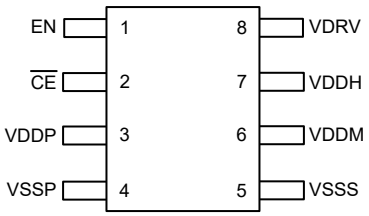

Figure 5-1. TPSI3052A-Q1, TPSI3052A-Q1 8-Pin SOIC Top View

Table 5-1. Pin Functions

PIN		I/O	TYPE[1]	DESCRIPTION
NO.	NAME			
1	EN	I	—	Driver enable, active high
2	CEbar	I	—	Chip enable, active low
3	VDDP	—	P	Power supply for primary side
4	VSSP	—	GND	Ground supply for primary side
5	VSSS	—	GND	Ground supply for secondary side
6	VDDM	—	P	Generated mid supply
7	VDDH	—	P	Generated high supply
8	VDRV	O	—	Active high driver output

(1) P = power, GND = ground, NC = no connect

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER(1)		MIN	MAX	UNIT
Primary side supply(2)	VDDP, EN, $\overline{CE}$	–0.3	6	V
Secondary side supply(3)	VDRV	–0.3	20	V
	VDDH	–0.3	20	V
	VDDM	–0.3	6	V
	VDDH-VDDM	–0.3	14	V
Junction temperature, T_J	Junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to VSSP.
(3) All voltage values are with respect to VSSS.

6.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDDP	Primary side supply voltage, A5(1)	4.5		5.5	V
	Primary side supply voltage, A3(1)	3.0		3.6	V
EN	Enable VDRV, A5(1)	0		5.5	V
	Enable VDRV, A3(1)	0		3.6	V
$\overline{CE}$	Chip enable, A5(1)	0		5.5	V
	Chip enable, A3(1)	0		3.6	V
C_{VDDP}	Decoupling capacitance on VDDP and VSSP(3)	1		20	µF
C_{DIV1} (2)	Decoupling capacitance across VDDH and VDDM(3)	0.003		15	µF
C_{DIV2} (2)	Decoupling capacitance across VDDM and VSSS(3)	0.1		40	µF
Q_{TOTAL}	Total charge to be driven by VDRV.			2500	nC
I_{AUX}	Auxiliary current sourced from VDDM.	0		8	mA
T_A	Ambient operating temperature	–40		125	°C
T_J	Operating junction temperature	–40		150	°C

(1) All voltage values are with respect to VSSP.
(2) C_{DIV1} and C_{DIV2} should be of same type and tolerance. C_{DIV2} capacitance value should be at least three times the capacitance value of C_{DIV1} i.e. $C_{DIV2} \geq 3 \times C_{DIV1}$.
(3) All capacitance values are absolute. Derating should be applied where necessary.

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6.3 Thermal Information

THERMAL METRIC[1] [2]		DEVICE DWZ (SOIC) 8 PINS	UNIT
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	89.3	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	40.3	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	45.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	44.4	°C/W

(1) Estimate only.
(2) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

6.4 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation, VDDP.	T_A = 25°C, V_{VDDP} = 5.0V, f_{EN} = 1kHz square wave, C_{VDRV} = 1nF			250	mW

6.5 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
CREEPAGE AND TRACKING				
CLR	External clearance[1]	Shortest terminal-to-terminal distance through air	≥ 8	mm
CPG	External creepage[1]	Shortest terminal-to-terminal distance across the package surface	≥ 8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	> 120	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 600V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000V_{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1697	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave)	1200	V_{RMS}
		DC voltage	1697	V_{DC}
C_{IO}	Barrier capacitance, input to output[2]	V_{IO} = 0.4 × sin (2πft), f = 1MHz	3	pF
R_{IO}	Insulation resistance, input to output[2]	V_{IO} = 500V, T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500V at T_S =150°C	> 10^9	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed-circuit board are used to help increase these specifications.
(2) All pins on each side of the barrier tied together creating a two-pin device.

6.6 Safety Limiting Values

PARAMETER(1) (2)		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 82.5°C/W, V_{VDDP} = 5.5V, T_J = 150°C, T_A = 25°C			275	mA
P_S	Safety input, output, or total power	$R_{\theta JA}$ =82.5°C/W, T_J = 150°C, T_A = 25°C			1.52	W
T_S	Maximum safety temperature				150	°C

(1) Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

(2) The safety-limiting constraint is the maximum junction temperature specified in the datasheet. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the Section 6.3 table is that of a device installed on a high-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

6.7 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted). Typicals at T_A = 25°C. C_{VDDP} = 1µF, C_{DIV1} = 47nF, C_{DIV2} = 220nF, C_{VDRV} = 1nF. $\overline{CE}$ pull down = 20kΩ

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
COMMON						
CMTI	Common-mode transient immunity, static.	$\|V_{CM}\|$ = 1000V, V_{EN} = 0V or V_{EN} = 5V.	100			V/ns
TSD	Temperature shutdown	V_{VDDP} = 5V		173		°C
TSDH	Temperature shutdown hysteresis	V_{VDDP} = 5V		32		°C
SUPPLY						
I_{VDDP_STBY}	VDDP current in standby	V_{VDDP} = 5V, EN = 0V, CE = 0V. Measure average current.		20	45	µA
$I_{VDDP\_LOW\_3V3}$	VDDP average current in steady state	V_{VDDP} = EN = 3.3V, $\overline{CE}$ = 0V. I_{VDDM} = I_{VDDH} = 0mA, 25°C V_{VDDH} in steady state, measure I_{VDDP}.		7		mA
$I_{VDDP\_LOW\_5V}$	VDDP average current in steady state	V_{VDDP} = EN= 5V, $\overline{CE}$ = 0V. I_{VDDM} = I_{VDDH} = 0mA, 25°C V_{VDDH} in steady state, measure I_{VDDP}.		8.5		mA
$I_{VDDP\_HIGH\_3V3}$	VDDP average current in steady state	V_{VDDP} = EN= 3.3V, $\overline{CE}$ = 0V. VDDM shorted to VSSS, measure I_{VDDP}.		32		mA
$I_{VDDP\_HIGH\_5V}$	VDDP average current in steady state	V_{VDDP} = 5V, EN = 5V, $\overline{CE}$ = 0V. VDDM shorted to VSSS, measure I_{VDDP}.		43		mA
V_{VDDH}	VDDH output voltage	V_{VDDP} = 3.3V, 5V EN = 3.3V, 5V, $\overline{CE}$ = 0V	16	17	18	V
P_{OUT_VDDM}	Maximum power transfer to VDDM	A3 Devices V_{VDDP} = 3.3V, EN = 0V, $\overline{CE}$ = 0V.	TBD	TBD		mW
		A5 Devices V_{VDDP} = 5V, EN = 0V, $\overline{CE}$ = 0V.	TBD	TBD		mW
P_{OUT_VDDH}	Maximum power transfer to VDDH.	A3 Devices V_{VDDP} = 3.3V, EN = 0V, $\overline{CE}$ = 0V.	TBD	TBD		mW
		A5 Devices V_{VDDP} = 5V, EN = 0V, $\overline{CE}$ = 0V.	TBD	TBD		mW

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6.7 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted). Typicals at T_A = 25°C. C_{VDDP} = 1µF, C_{DIV1} = 47nF, C_{DIV2} = 220nF, C_{VDRV} = 1nF. $\overline{CE}$ pull down = 20kΩ

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{VDDM_IAUX}	Average VDDM voltage when sourcing external current.	For A5: V_{VDDP} = 5V, EN = 0V, steady state. Source I_{AUX} = 5mA from VDD For A3: V_{VDDP} = 3.3V, EN = 0V, steady state. Source I_{AUX} = 2.5mA from VDD Measure V_{VDDM}. C_{DIV2} = 1µF	4.7		5.5	V
SUPERVISORY						
$V_{VDDP\_UV\_R}$	VDDP undervoltage threshold rising	A3 Devices	2.71	2.82	2.92	V
		A5 Devices	3.9	4.1	4.35	V
$V_{VDDP\_UV\_F}$	VDDP undervoltage threshold falling	A3 Devices	2.67	2.76	2.87	V
		A5 Devices	3.8	3.9	4.25	V
$V_{VDDP\_UV\_HYS}$	VDDP undervoltage threshold hysteresis	A3 Devices		110		mV
		A5 Devices		150		mV
$V_{VDDH\_UV\_R}$	VDDH undervoltage threshold rising	VDDH rising.	11.9	13	14.2	V
$V_{VDDH\_UV\_F}$	VDDH undervoltage threshold falling.	VDDH falling.	9.6	10.4	11.5	V
$V_{VDDH\_UV\_HYS}$	VDDH undervoltage threshold hysteresis.			2.8		V
$V_{VDDM\_UV\_R}$	VDDM undervoltage threshold rising	VDDM rising.	3.4	3.7	3.9	V
$V_{VDDM\_UV\_F}$	VDDM undervoltage threshold falling.	VDDM falling.	3.1	3.4	3.7	V
$V_{VDDM\_UV\_HYS}$	VDDM undervoltage threshold hysteresis.			0.5		V
DRIVER						
V_{VDRV_H}	VDRV output voltage driven high	V_{VDDP} = 5V, EN = 5V. V_{VDDH} in steady state	16	17	18	V
V_{VDRV_L}	VDRV output voltage driven low	V_{VDDP} = 5V, EN = 0V, V_{VDDH} in steady state, VDRV sinking 10mA.			0.1	V
I_{VDRV_PEAK}	VDRV peak output current during rise	V_{VDDP} = 5V, EN = 0V → 5V, V_{VDDH} in steady state, measure peak current.		1.5		A
	VDRV peak output current during fall	V_{VDDP} = 5V, EN = 5V → 0V, V_{VDDH} in steady state, measure peak current.		2.5		A
R_{DSON_VDRV}	Driver on resistance in low state.	V_{VDDH} in steady state		1.5		Ω
	Driver on resistance in high state.	V_{VDDH} in steady state		3.5		Ω
V_{ACT_CLAMP}	Active clamp voltage when engaged.	V_{VDDP} = 0V. Sink I_{VDRV} = 300mA. Measure VDRV.		1.9	2.5	V

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6.7 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted). Typicals at T_A = 25°C. C_{VDDP} = 1µF, C_{DIV1} = 47nF, C_{DIV2} = 220nF, C_{VDRV} = 1nF. $\overline{CE}$ pull down = 20kΩ

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IT\_+(EN)}$	Input threshold voltage rising on EN.	A3 Devices	1.4	1.6	1.9	V
$V_{IT\_-(EN)}$	Input threshold voltage falling on EN.		1.1	1.2	1.5	V
$V_{IT\_HYS(EN)}$	Input threshold voltage hysteresis on EN.			0.4		V
DIGITAL INPUT/OUTPUT						
$V_{IT\_+(EN)}$	Input threshold voltage rising on EN.	A5 Devices	2.3	2.5	2.7	V
$V_{IT\_-(EN)}$	Input threshold voltage falling on EN.		1.7	1.9	2.0	V
$V_{IT\_HYS(EN)}$	Input threshold voltage hysteresis on EN.			0.5		V
$V_{IT\_+(\overline{CE})}$	Input threshold voltage rising on $\overline{CE}$.	A3 Devices	1.4	1.6	1.9	V
$V_{IT\_+(\overline{CE})}$	Input threshold voltage rising on $\overline{CE}$.		1.1	1.2	1.4	V
$V_{IT\_HYS(\overline{CE})}$	Input threshold voltage hysteresis on CE.			0.4		V
$V_{IT\_+(\overline{CE})}$	Input threshold voltage rising on $\overline{CE}$.	A5 Devices	2.3	2.5	2.7	V
$V_{IT\_-(\overline{CE})}$	Input threshold voltage falling on $\overline{CE}$.		1.7	1.9	2.0	V
$V_{IT\_HYS(\overline{CE})}$	Input threshold voltage hysteresis on CE.			0.5		V
$R_{EN\_PULLDOWN}$	Internal resistor pull-down on EN.	V_{VDDP} = 5V	340	500	670	kΩ
$R_{\overline{CE}\_PULLDOWN}$	Internal resistor pull-down on $\overline{CE}$.	V_{VDDP} = 5V	340	500	670	kΩ

6.8 Switching Characteristics

over operating free-air temperature range (unless otherwise noted). Typicals at T_A = 25°C. C_{VDDP} = 1µF, C_{DIV1} = 47nF, C_{DIV2} = 220nF, C_{VDRV} = 1nF. 20kΩ pull-down from $\overline{CE}$ to VSSP

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER and DRIVER						
$t_{LO\_\overline{CE}}$	Low time of $\overline{CE}$.	V_{VDDH}, V_{VDDM} = steady state.	5			µs
t_{LO_EN}	Low time of EN.	V_{VDDH}, V_{VDDM} = steady state.	5			µs
t_{HI_EN}	High time of EN.	V_{VDDH}, V_{VDDM} = steady state.	5			µs
t_{PER_EN}	Period of EN.	V_{VDDH}, V_{VDDM} = steady state.	10			µs
t_{LH_VDDH}	Propagation delay time from VDDP rising to VDDH at 50% level.	EN = 0V, V_{VDDP} = 0V → 5V at 1V/µs, V_{VDDH} = 7.5V.		120		µs
t_{LH_VDRV}	Propagation delay time from EN rising to VDRV at 90% level	V_{VDDP} = 5V, V_{VDDH}, V_{VDDM} = steady state, EN = 0V → 5V, V_{VDRV} = 13.5V.		3	4.5	µs
t_{HL_VDRV}	Propagation delay time from EN falling to VDRV at 10% level	V_{VDDP} = 5V, V_{VDDH}, V_{VDDM} = steady state, EN = 5V → 0V, V_{VDRV} = 1.5V.		2.5	3.0	µs

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6.8 Switching Characteristics (continued)

over operating free-air temperature range (unless otherwise noted). Typicals at T_A = 25°C. C_{VDDP} = 1µF, C_{DIV1} = 47nF, C_{DIV2} = 220nF, C_{VDRV} = 1nF. 20kΩ pull-down from $\overline{CE}$ to VSSP

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{HL\_VDRV\_PD}$	Propagation delay time from VDDP falling to VDRV at 10% level. Timeout mechanism due to loss of power on primary supply.	EN = 5V, V_{VDDP} = 5V → 0V at -1V/µs, V_{VDRV} = 1.5V.		140	210	µs
$t_{LH\_VDRV\_\overline{CE}\_33V}$	Propagation delay time from $\overline{CE}$ falling to VDRV at 10% level	V_{VDDP} = EN = 3.3V, VDDH and VDDM fully discharged. V_{VDRV} = 1.5V. $\overline{CE}$ 3.3V -> 0V		275		µs
$t_{LH\_VDRV\_\overline{CE}\_5V}$	Propagation delay time from $\overline{CE}$ falling to VDRV at 10% level	V_{VDDP} = EN = 5V, VDDH and VDDM fully discharged. V_{VDRV} = 1.5V. $\overline{CE}$ 5V -> 0V		200		µs
$t_{HL\_VDRV\_\overline{CE}}$	Propagation delay time from $\overline{CE}$ rising to VDRV at 10% level	V_{VDDP} = 5V, V_{VDDH}, V_{VDDM} = steady state, EN = 5V, $\overline{CE}$= 0V → 5V, V_{VDRV} = 1.5V.		2.5	3	µs
t_{R_VDRV}	VDRV rise time from EN rising to VDRV from 15% to 85% level	V_{VDDP} = 5V, V_{VDDH}, V_{VDDM} = steady state, EN = 0V → 5V, V_{VDRV} = 2.25V to 12.75V.		15		ns
t_{F_VDRV}	VDRV fall time from EN falling to VDRV from 85% to 15% level	V_{VDDP} = xV, V_{VDDH}, V_{VDDM} = steady state, EN = xV → 0V, V_{VDRV} = 12.75V to 2.25V.		10		ns

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6.9 Insulation Characteristic Curves

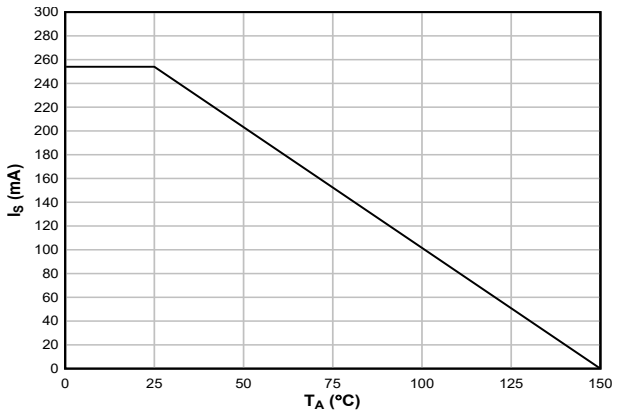


Figure 6-1. Thermal Derating Curve for Limiting Current per VDE and IEC, Three-Wire Mode

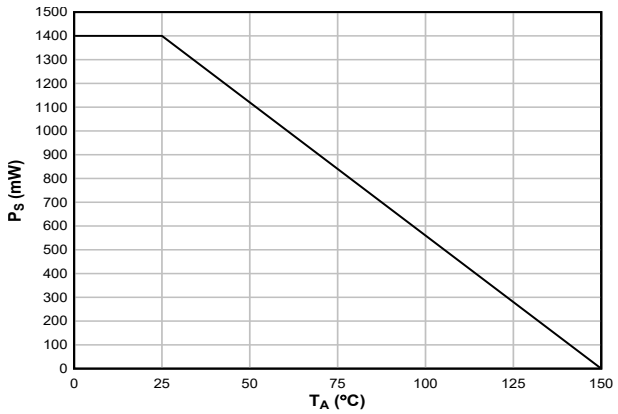


Figure 6-2. Thermal Derating Curve for Limiting Power per VDE and IEC

ADVANCE INFORMATION

7 Parameter Measurement Information

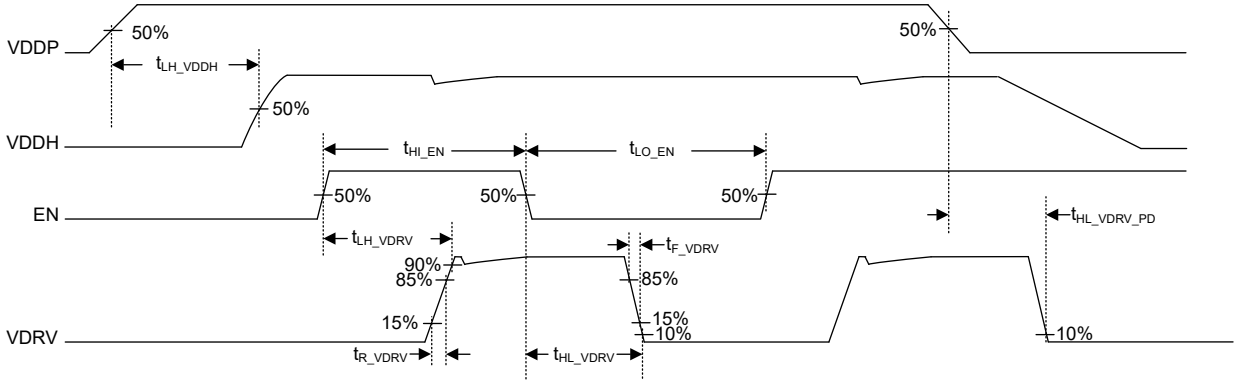


Figure 7-1. Three-Wire Mode Timing, Standard Enable

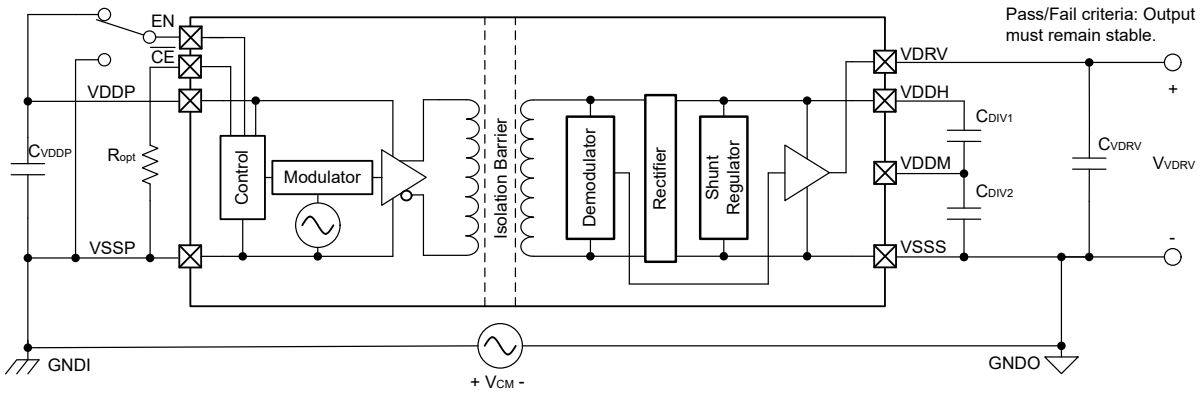


Figure 7-2. Common-Mode Transient Immunity Test Circuit

ADVANCE INFORMATION

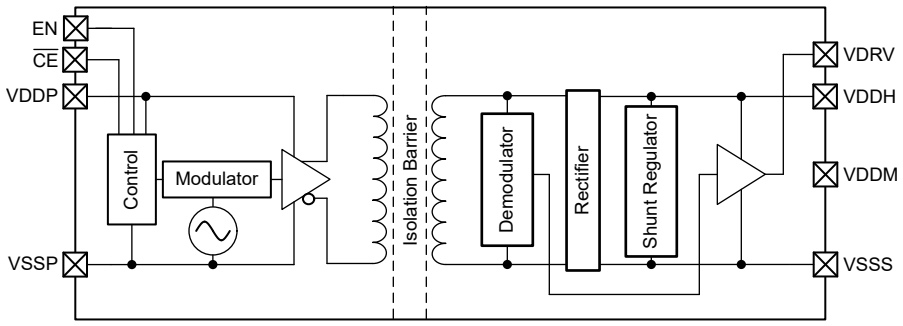
8 Detailed Description

8.1 Overview

The TPSI3052A-Q1 is a fully integrated, reinforced isolated power switch driver, which when combined with an external power switch, forms a complete isolated Solid State Relay (SSR). With a nominal gate drive voltage of 17V and 1.5/3.0A peak source and sink current, select from a large variety of external power switches to meet a wide range of applications. The TPSI3052A-Q1 generates its own secondary supply from the power received from its primary side, so no isolated secondary bias supply is required.

The *Functional Block Diagram* shows the primary side that includes a transmitter that drives an alternating current into the primary winding of an integrated transformer when the chip is enabled. The transmitter operates at high frequency to optimally drive the transformer to its peak efficiency. In addition, the transmitter uses several techniques to greatly improve EMI performance over the TPSI3052-Q1, allowing many applications to achieve CISPR 25 - Class 5. During transmission, data information transfers to the secondary side alongside with the power. On the secondary side, the voltage induced on the secondary winding of the transformer is rectified, and the shunt regulator regulates the output voltage level of VDDH. Lastly, the demodulator decodes the received data information and drives VDRV high or low based on the logic state of the EN pin.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Transmission of the Enable State

The TPSI3052A-Q1 uses a modulation scheme to transmit the switch enable state information across the isolation barrier. The transmitter modulates the EN signal with an internally generated, high-frequency carrier (89MHz typical), and differentially drives the primary winding of the isolation transformer. The receiver on the secondary side demodulates the received signal and asserts VDRV high or low based on the data received.

8.3.2 Power Transmission

The TPSI3052A-Q1 does not use an external isolated supply for power. The secondary side power is obtained by the transferring of the primary side input power across the isolation transformer. The modulation scheme uses several techniques to improve EMI performance over previous devices, assisting applications in meeting the CISPR 25 Class 5 standards. These techniques include optimized spread spectrum, precision switching, automatic power transfer level and a center frequency of 65MHz optimized for the CISPR 25 standard.

8.3.3 Gate Driver

The TPSI3052A-Q1 has an integrated gate driver that provides a nominal 17V gate voltage with 1.5/2.5A peak source and sink current sufficient for driving many power transistors or Silicon-Controlled Rectifiers (SCR). When driving external power transistors, TI recommends bypass capacitors (C_{DIV2} = 3 * C_{DIV1}) from VDDH to VDDM and VDDM to VSSS of 20 times the equivalent gate capacitance.

The gate driver also includes an active clamp keep off circuit. This feature helps to keep the driver output, VDRV, low if power be lost on the secondary supply rails, for example, power loss on the VDDP supply prevents power

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transfer. If power is lost, the active clamp keep off circuit tries to clamp the voltage of VDRV to under 2,V relative to VSSS.

8.3.4 VDDP, VDDH, and VDDM Undervoltage Lockout (UVLO)

TPSI3052A-Q1 implements an internal UVLO protection feature for both input and output power supplies, VDDP, VDDH, and VDDM. When VDDP is lower than the UVLO threshold voltage, power ceases to be transferred to the VDDM and VDDH rails. Over time the VDDH and VDDM rails begins to discharge. If enough charge is available on VDDP, the device tries to signal VDRV to assert low. If not enough charge is available on VDDP, a timeout mechanism establishes VDRV asserts low after reaching the timeout. When either VDDH or VDDM are lower than the respective UVLO thresholds, VDRV asserts low regardless of the EN state. The UVLO protection blocks feature hysteresis, which helps to improve the noise immunity of the power supply. During turn-on and turn-off, the driver sources and sinks a peak transient current, which can result in voltage drop of the VDDH, VDDM power supplies. The internal UVLO protection block ignores the associated noise during these normal switching transients.

8.3.5 Power Supply, CE, and EN Sequencing

TPSI3052A-Q1 has an active low chip enable, CE. When CE is asserted low and VDDP is present, the device enters its active mode of operation and power transfer occurs from the primary side to the secondary side. When CE is asserted high while VDDP is present, the device enters standby and no power transfer occurs from primary side to the secondary side and VDRV is asserted low. Over time, VDDH and VDDM fully discharge depending on the amount of loading present on these rails.

During power up, the DC/DC converter is initially disabled. Once VDDP reaches $V_{VDDP\_UV\_R}$ and CE is determined to below, the DC/DC converter is enabled, transferring power at the maximum rate to quickly charge up the VDDM and VDDH. For this brief period, the current VDDP is I_{VDDP_High}.

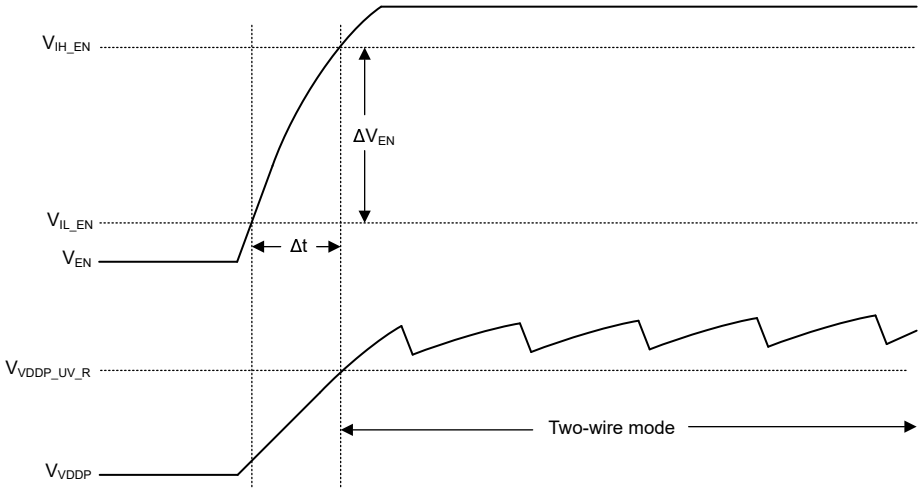

Figure 8-1. Sequencing

In most applications, the same voltage rail and source supply the EN and VDDP. It is recommended that V_{EN} remain below V_{IL_EN} until V_{VDDP} reaches $V_{VDDP\_UV\_R}$. It is also possible in some applications to connect EN directly to the VDDP supply. Figure 8-1 shows these two scenarios.

8.3.6 Thermal Shutdown

The device contains an integrated temperature sensor to monitor its local temperature. When the sensor reaches its threshold, it automatically ceases power transfer from the primary side to the secondary side. In addition, if power is still present on VDDP, the driver is automatically asserted low. The power transfer is disabled until the local temperature reduces enough to re-engage.

8.4 Device Functional Modes

Table 8-1 summarizes the functional modes for the TPSI3052A-Q1 and TPSI3052A-Q1.

Table 8-1. TPSI3052A-Q1, TPSI3052A-Q1 Device Functional Modes

VDDP(1)	VDDH	EN(1)	nCE(1)	VDRV	COMMENTS
Powered up(2)	Powered up(3)	L	L	L	TPSI3052A-Q1 normal operation: VDRV output state assumes logic state of EN logic state.
		H	L	H	
		L	L	L	TPSI3052A-Q1 normal operation (three-wire mode only): rising edge of EN causes VDRV to be singly pulsed high. EN must be asserted low first to assert another pulse.
		L → H	L	L → H → L	
Powered up(2)	X	X	H	L	Disabled operation: VDRV output disabled, no power transfers to VDDH, keep off circuitry applied.
Powered down(4)	Powered down(5)	X(6)	X	L	Disabled operation: VDRV output disabled, keep off circuitry applied.
Powered up(2)	Powered down(5)	X(6)	X	L	Disabled operation: VDRV output disabled, keep off circuitry applied.
Powered down(4)	Powered up(3)	X(6)	X	L	Disabled operation: when VDDP is powered down, output driver is disabled automatically after timeout, keep off circuitry applied.

(1) Refer to Power Supply, CE, and EN Sequencing for additional information.
(2) V_{VDDP} ≥ VDDP undervoltage lockout rising threshold, $V_{VDDP\_UV\_R}$.
(3) V_{VDDH} ≥ VDDH undervoltage lockout rising threshold, $V_{VDDH\_UV\_R}$.
(4) V_{VDDP} < VDDP undervoltage lockout falling threshold, $V_{VDDP\_UV\_F}$.
(5) V_{VDDH} < VDDH undervoltage lockout falling threshold, $V_{VDDH\_UV\_F}$.
(6) X: do not care.

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPSI3052A-Q1 is a fully integrated, isolated switch driver with integrated bias, which when combined with an external power switch, forms a complete isolated solid-state relay solution. With a nominal gate drive voltage of 17V with 1.5/3.0A peak source and sink current, select from a large variety of external power switches such as MOSFETs, IGBTs, or SCRs to meet a wide range of applications. The TPSI3052A-Q1 generates its own secondary bias supply from the power received from its primary side, so no isolated secondary supply bias is required.

The secondary side provides a regulated, floating supply rail of 17V for driving a large variety of power switches with no need for a secondary bias supply. The TPSI3052A-Q1 can support driving single power switch, dual back-to-back, parallel power switches for a variety of AC or DC applications. The TPSI3052A-Q1 integrated isolation protection is extremely robust with much higher reliability, lower power consumption, and increased temperature ranges than those found using traditional mechanical relays and optocouplers.

9.2 Typical Application

The circuits in Figure 9-1 a typical application for driving silicon based MOSFETs in three-wire mode.

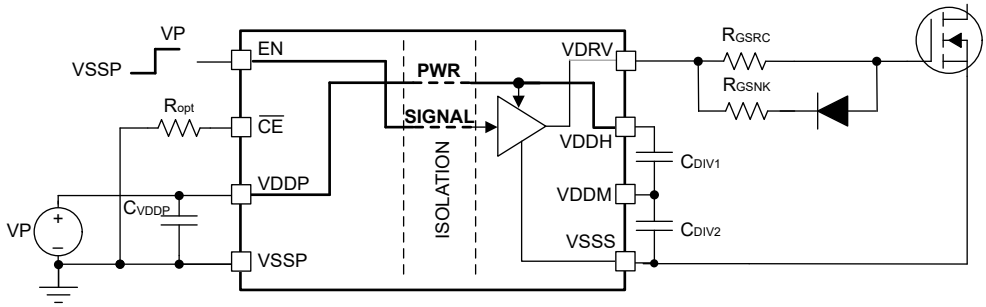

Figure 9-1. TPSI3052A-Q1 Three-Wire Mode Driving MOSFETs

9.2.1 Design Requirements

Table 9-1 lists the design requirements of the TPSI3052A-Q1 gate driver.

Table 9-1. TPSI3052A-Q1 Design Requirements

DESIGN PARAMETERS	
Total gate capacitance	100nC
FET turn-on time	1µs
Propagation delay	< 4µs
Switching frequency	10kHz
Supply voltage (VDDP)	5V ± 5%

9.2.2 Detailed Design Procedure

9.2.2.1 C_{DIV1}, C_{DIV2} Capacitance

The C_{DIV1} and C_{DIV2} capacitances required depends on the amount of drop that the VDDH rail tolerates during switching of the external load. The charge stored on the CDIV1 and CDIV2 capacitances provides the current

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to the load during switching. During switching, charge sharing occurs and the voltage on VDDH drops. At a minimum, TI recommends that the total capacitance the series combination of C_{DIV1} and C_{DIV2} forms size to at least 30 times the total gate capacitance to be switched. This sizing results in an approximate 0.5V drop of the VDDH supply rail that supplies power to the VDRV signal. Use Equation 1 and Equation 2 to calculate the amount of capacitance required for a specified voltage drop.

C_{DIV1} and C_{DIV2} must be of the same type and tolerance.

$$C_{DIV1} = \left(\frac{n+1}{n}\right) \times \frac{Q_{LOAD}}{\Delta V},\ n \geq 3.0 \quad (1)$$

$$C_{DIV2} = n \times C_{DIV1},\ n \geq 3.0 \quad (2)$$

where

- n is a real number greater than or equal to 3.0.
- C_{DIV1} is the external capacitance from VDDH to VDDM.
- C_{DIV2} is the external capacitance from VDDM to VSSS.
- Q_{LOAD} is the total charge of the load from VDRV to VSSS.
- ΔV is the voltage drop on VDDH when switching the load.

Note

C_{DIV1} and C_{DIV2} represent absolute capacitances and components selected must be adjusted for tolerances and any derating necessary to achieve the required capacitances.

Larger values of ΔV are useable in the application, but excessive droop can cause the VDDH undervoltage lockout falling threshold ($V_{VDDH\_UVLO\_F}$) to be reached and cause VDRV to be asserted low. Note that as the series combination of C_{DIV1} and C_{DIV2} capacitances increases relative to Q_{LOAD}, the VDDH supply voltage drop decreases, but the initial charging of the VDDH supply voltage during power up increases.

For this design, assuming n = 3 and ΔV≅ 0.5V, then

$$C_{DIV1} = \left(\frac{3+1}{3}\right) \times \frac{120\ nC}{0.5\ V} = 320\ nF \quad (3)$$

$$C_{DIV2} = 3 \times 320\ nF = 960\ nF \quad (4)$$

For this design, C_{DIV1} = 330nF and C_{DIV2} = 1µF standard capacitor values were selected.

9.2.2.2 C_{VDDP} Capacitance

This design requires three-wire mode to meet the design requirements. For three-wire mode, increasing the amount of capacitance, C_{VDDP}, improves the ripple on the VDDP supply. This design uses 1µF in parallel with 100nF.

9.2.2.3 Gate Driver Output Resistor

Use the optional external gate driver resistors, R_{GSRC} and R_{GSNK}, to:

1. Limit ringing caused by parasitic inductances and capacitances
2. Limit ringing caused by high voltage switching dv/dt, high current switching di/dt, and body-diode reverse recovery
3. Fine-tune gate drive strength for sourcing and sinking
4. Reduce electromagnetic interference (EMI)

The TPSI3052A-Q1 has a pullup structure with a P-channel MOSFET with a peak source current of 1.5A. Therefore, predict the peak source current with:

$$I_{O+} \cong \min\left(1.5A,\ \frac{V_{VDDH}}{R_{DSON\_VDRV} + R_{GSRC} + R_{GFET\_INT}}\right) \quad (5)$$

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where

- R_{GSRC}: external turn-on resistance.
- R_{DSON_VDRV}: TPSI3052A-Q1 driver on resistance in high state. See *Electrical Characteristics*.
- V_{VDDH}: VDDH voltage. Assumed 15.1V in this example.
- R_{GFET_INT}: external power transistor internal gate resistance, found in the power transistor datasheet. Assume 0Ω for this example.
- I_{O+}: peak source current. The minimum value between 1.5A, the gate driver peak source current, and the calculated value based on the gate drive loop resistance.

For this example, R_{DSON_VDRV} = 2.5Ω, R_{GSRC} = 10Ω, and R_{GFET_INT} = 0Ω results in:

$$I_{O+} \cong min\left(1.5\ A, \frac{15.1\ V}{2.5\ \Omega + 10\ \Omega + 0\ \Omega}\right) = 1.21\ A \quad (6)$$

Similarly, the TPSI3052A-Q1 has a pulldown structure with an N-channel MOSFET with a peak sink current of 3.0A. Therefore, assuming R_{GFET_INT} = 0Ω, predict the peak sink current with:

$$I_{O-} \cong \min\left[3.0\ A, (V_{VDDH} \times (R_{GSRC} + R_{GSNK}) - R_{GSRC} \times V_F) \times \frac{1}{R_{GSRC} \times R_{GSNK} + R_{DSON\_VDRV} \times (R_{GSRC} + R_{GSNK})}\right] \quad (7)$$

where

- R_{GSRC}: external turn-on resistance.
- R_{GSNK}: external turn-off resistance.
- R_{DSON_VDRV}: TPSI3052A-Q1 driver on resistance in low state. See *Electrical Characteristics*.
- V_{VDDH}: VDDH voltage. Assumed 15.1V in this example.
- V_F: diode forward voltage drop. Assumed 0.7V in this example.
- I_{O-}: peak sink current. The minimum value between 3.0A, the gate driver peak sink current, and the calculated value based on the gate drive loop resistance.

For this example, assuming R_{DSON_VDRV} = 1.7Ω, R_{GSRC} = 10Ω, R_{GSNK} = 5.0Ω, and R_{GFET_INT} = 0Ω, results in:

$$I_{O-} \cong min\left[3.0\ A, (15.1\ V \times (10\ \Omega + 5\ \Omega) - 10\Omega \times 0.7\ V) \times \frac{1}{10\ \Omega \times 5\ \Omega + 1.7\ \Omega \times (10\Omega + 5\ \Omega)}\right] = 2.91\ A \quad (8)$$

Importantly, the estimated peak current is also influenced by PCB layout and load capacitance. Parasitic inductance in the gate driver loop can slow down the peak gate drive current and introduce overshoot and undershoot. Therefore, TI strongly recommends to minimize the gate driver loop.

9.2.2.4 Start-up Time and Recovery Time

As described in the Section 9.2.2.1, the start-up time of the fully discharged VDDH rail depends on the amount of capacitance present on the VDDH supply. The rate at which this capacitance charges depends on the amount of power transferred from the primary side to the secondary side. The amount of power transferred to the secondary supply (VDDH), is automatically regulated. When the device initially starts up, it supplies the maximum amount of power, then reduces once the VDDH and VDDM voltages have reached nominal levels, thereby minimizing the overall start-up and recovery times.

9.2.2.5 Supplying Auxiliary Current, I_{AUX} From VDDM

The TPSI3052A-Q1 can provide power from VDDM to support external auxiliary circuitry as shown in Figure 9-2. In this case, the required transfer power must include the additional power the auxiliary circuitry on the VDDM rail consumes. Unlike previous devices, the power transfer is automatically regulated and R_{PXFR} is not longer needed.

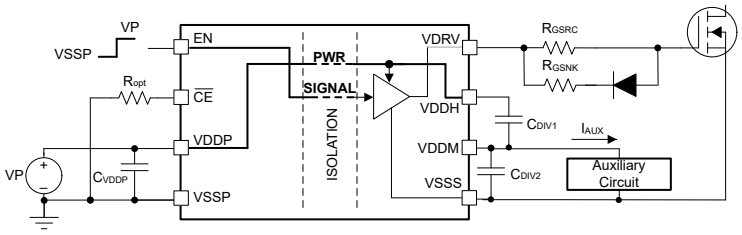

Figure 9-2. Supplying Auxiliary Power From VDDM

9.2.2.6 VDDM Ripple Voltage

Note that when supplying power from VDDM, that is when I_{AUX} > 0mA, additional voltage ripple is present on the VDDM rail. This ripple can be reduced by applying additional capacitance from VDDM to VSSS.

9.2.3 Application Curves

9.2.4 Insulation Lifetime

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; See Figure 9-3 for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60Hz overtemperature. For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million (ppm). Even though the expected minimum insulation lifetime is 20 years at the specified working isolation voltage, VDE reinforced certification requires additional safety margin of 20% for working voltage and 87.5% for lifetime which translates into minimum required insulation lifetime of 37.5 years at a working voltage that is 20% higher than the specified value.

Figure 9-4 shows the intrinsic capability of the isolation barrier to withstand high voltage stress over its lifetime. Based on the TDDB data, the intrinsic capability of the insulation is 1000V_{RMS} with a lifetime of 1184 years.

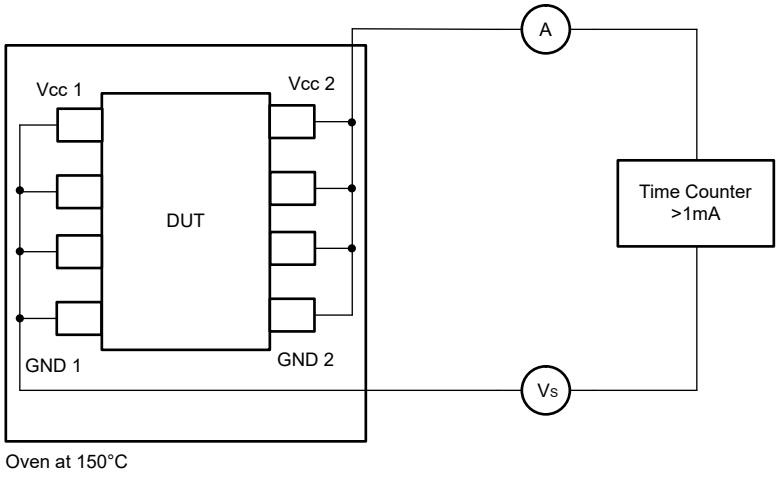

Figure 9-3. Test Setup for Insulation Lifetime Measurement

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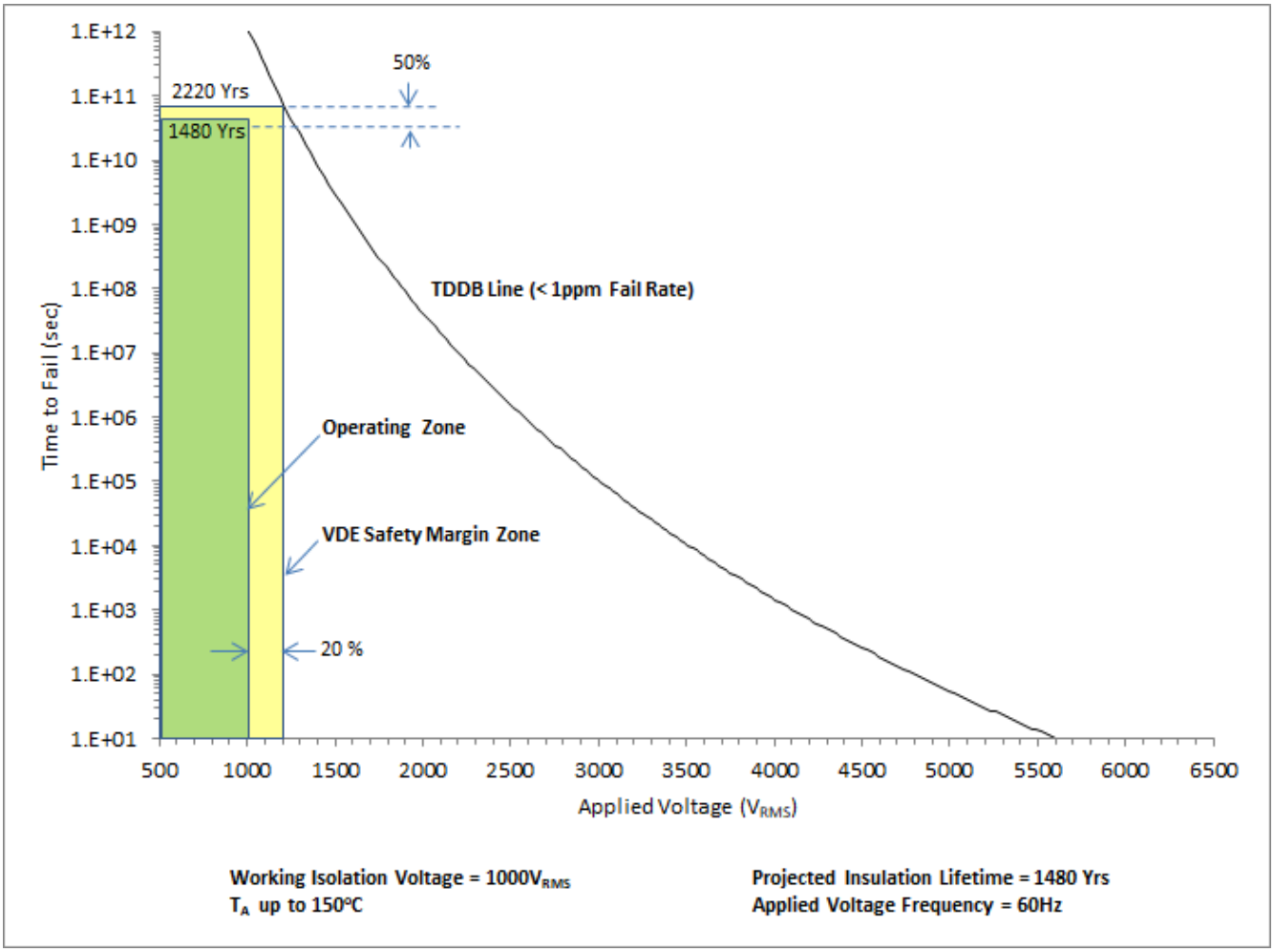

Figure 9-4. Insulation Lifetime Projection Data

9.3 Power Supply Recommendations

To help establish a reliable supply voltage, TI recommends that the C_{VDDP} capacitance from VDDP to VSSP consists of a 0.1µF bypass capacitor for high-frequency decoupling in parallel with a 1µF for low-frequency decoupling. Connect low-ESR and low-ESL capacitors close to the device between the VDDP and VSSP pins.

9.4 Layout

9.4.1 Layout Guidelines

Designers must pay close attention to PCB layout to achieve peak performance for the TPSI3052A-Q1. Some key guidelines are:

- Component placement:
  - Place the driver as close as possible to the power semiconductor to reduce the parasitic inductance of the gate loop on the PCB traces.
  - Connect low-ESR and low-ESL capacitors close to the device between the VDDH and VDDM pins and the VDDM and VSSS pins to bypass noise and to support high peak currents when turning on the external power transistor.
  - Connect low-ESR and low-ESL capacitors close to the device between the VDDP and VSSP pins.
- Grounding considerations:
  - Limit the high peak currents that charge and discharge the transistor gates to a minimal physical area. This limitation decreases the loop inductance and minimizes noise on the gate terminals of the transistors. Place the gate driver as close as possible to the transistors.

  - Connect the driver VSSS to the Kelvin connection of MOSFET source or IGBT emitter. If the power device does not have a split Kelvin source or emitter, connect the VSSS pin as close as possible to the source or emitter terminal of the power device package to separate the gate loop from the high power switching loop.
- High-voltage considerations:
  - To establish isolation performance between the primary and secondary side, avoid placing any PCB traces or copper below the driver device. TI recommends a PCB cutout or groove to prevent contamination that can compromise the isolation performance.
- Thermal considerations:
  - Proper PCB layout can help dissipate heat from the device to the PCB and minimize junction-to-board thermal impedance (θ_{JB}).
  - If the system has multiple layers, TI also recommends connecting the VDDH and VSSS pins to internal ground or power planes through multiple vias of adequate size. Locate these vias close to the IC pins to maximize thermal conductivity. However, keep in mind that no traces or coppers from different high voltage planes are overlapping.

9.4.2 Layout Example

Figure 9-5 shows a PCB layout example with the signals and key components labeled.

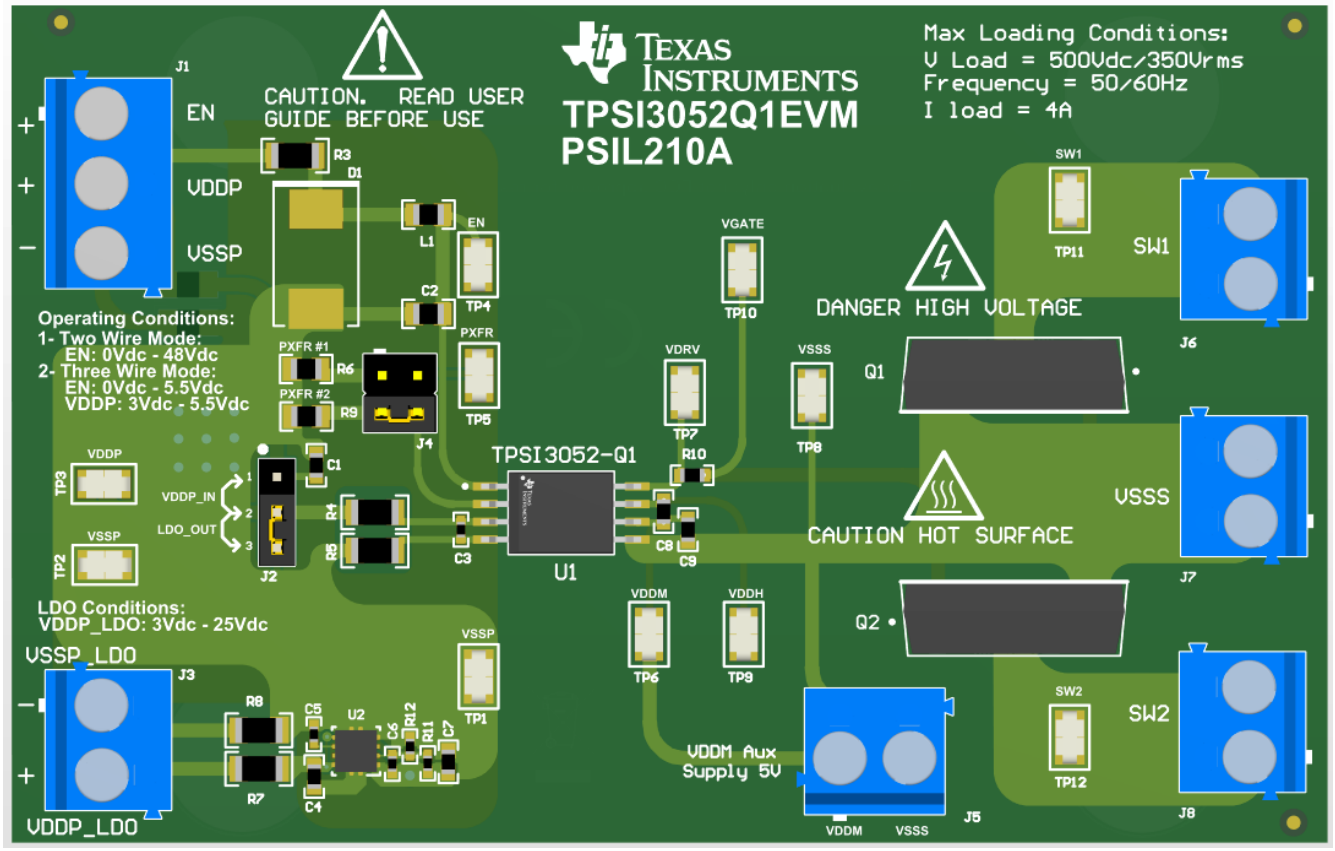

Figure 9-5. 3D PCB View

Figure 9-6 and Figure 9-7 show the top and bottom layer traces and copper.

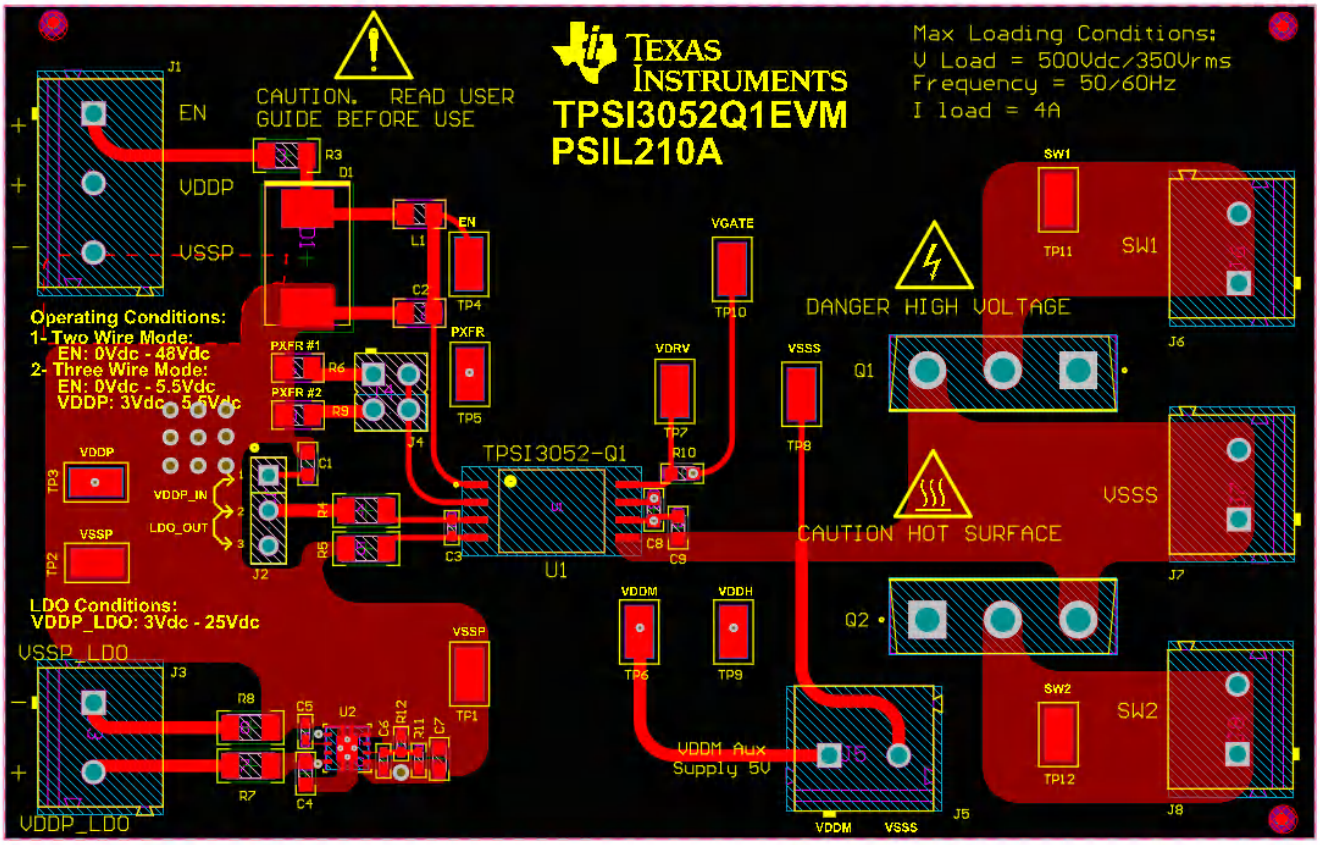

Figure 9-6. Top Layer

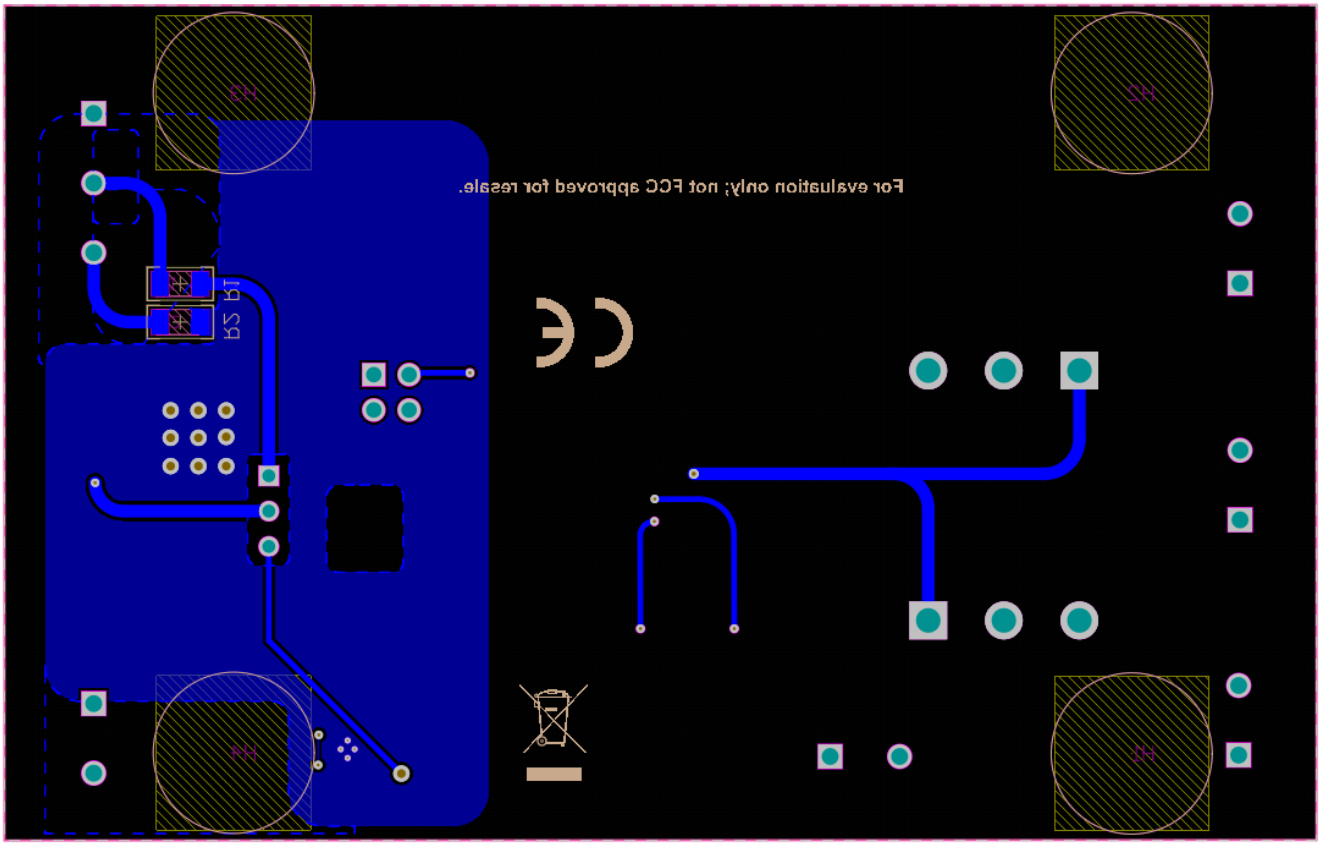

Figure 9-7. Bottom Layer

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10 Device and Documentation Support

10.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 10-1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPSI3052A-Q1	Click here	Click here	Click here	Click here	Click here
TPSI3052A-Q1	Click here	Click here	Click here	Click here	Click here

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
July 2026	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTPSI3052A3QDWZRQ1	Active	Preproduction	SO-MOD (DWZ) | 8	1000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PTPSI3052A5QDWZRQ1	Active	Preproduction	SO-MOD (DWZ) | 8	1000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

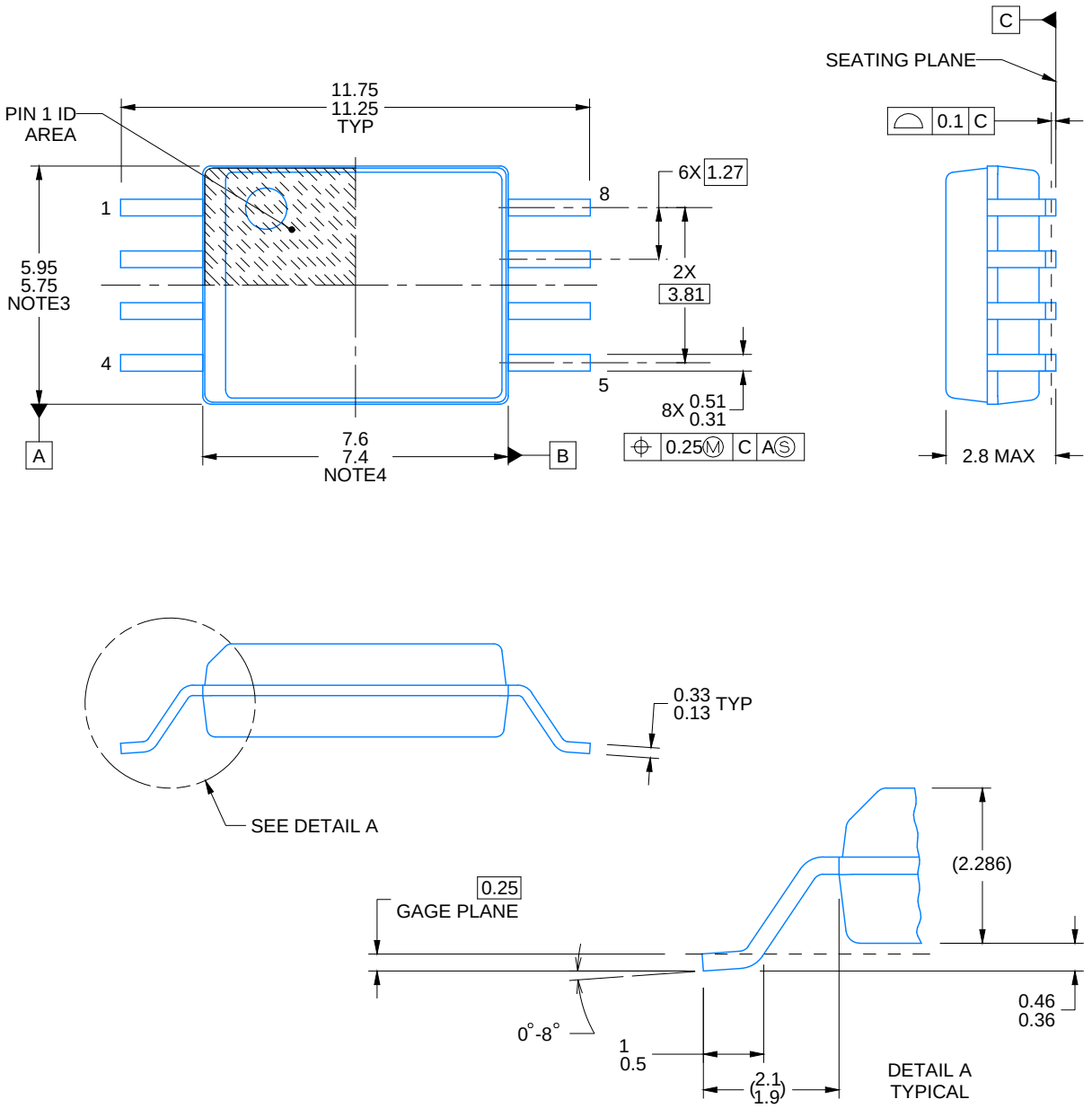
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

PACKAGE OUTLINE

DWZ0008A

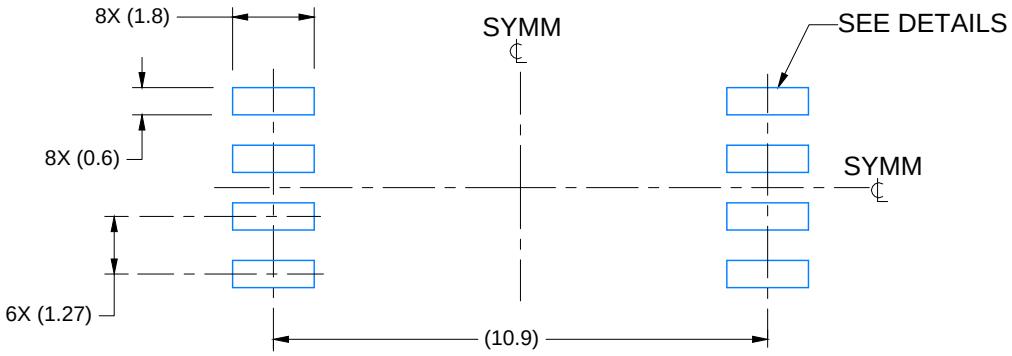
SOIC - 2.8 mm max height

SMALL OUTLINE PACKAGE

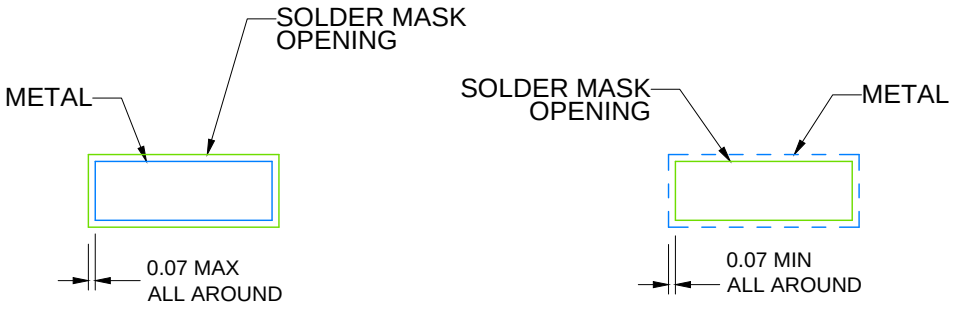


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Ref. JEDEC registration MS-013



LAND PATTERN EXAMPLE
9.1 mm NOMINAL CLEARANCE/CREEPAGE
SCALE: 6X



NON SOLDER MASK
DEFINED

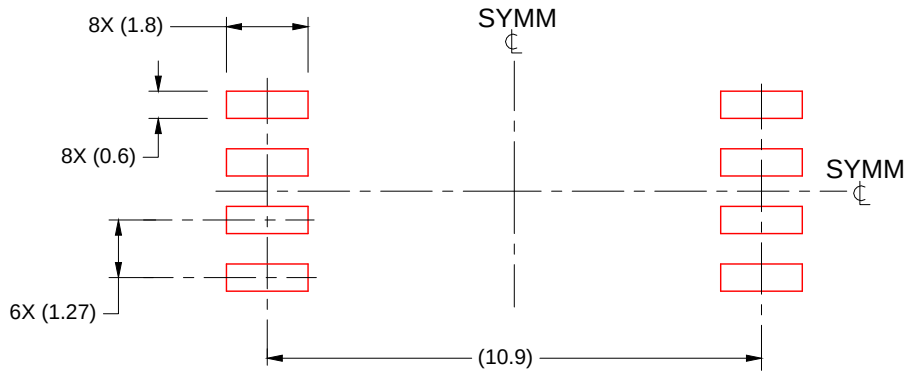
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4226306/A 09/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 6X

4226306/A 09/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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