TPSI8830 80V, 30mΩ, 3A, Solid-State Relay With Overcurrent Protection, Load Diagnostics, and Functional Isolation

1 Features

- Integrated back-back MOSFETs with ± 80V Operation
  - R_{ON} = 30mΩ (T_J = 25°C)
  - I_{OFF} = 1µA at 60V (T_J = 105°C)
- Power path overcurrent protection with fault signal across isolation
  - Version A: 4A
  - Version B: 6A
- Wide supply range: 3.0V to 5.5V
- Configurable fault retry timer (TMR)
- Low on-state primary side supply current (VDD)
  - 5mA ON state VDD current
- Wide temperature range:–40 to 125°C
- Functional isolation:
  - 200V_{RMS}, 250V_{DC} working voltage
  - 570V_{RMS}, 800V_{DC} transient voltage (60s)
- SSOP 14-pin (DFP) package with 8mm of creepage and clearance
- Functional Safety Capable
  - Documentation available to aid in ISO 26262 and IEC 61508 system design

2 Applications

- Solid state relay
- Thermostats
- PLC - digital output modules

3 Description

The TPSI8830 is an isolated solid-state relay designed for industrial applications. The TPSI8830 uses TI's high reliability capacitive isolation technology in combination with internal back-to-back MOSFETs to form a completely integrated option requiring no secondary side power supply. The TPSI8830 improves system reliability as TI's capacitive isolation technology does not suffer from mechanical wear-out or photo degradation failure modes common in mechanical relay and photo relay components.

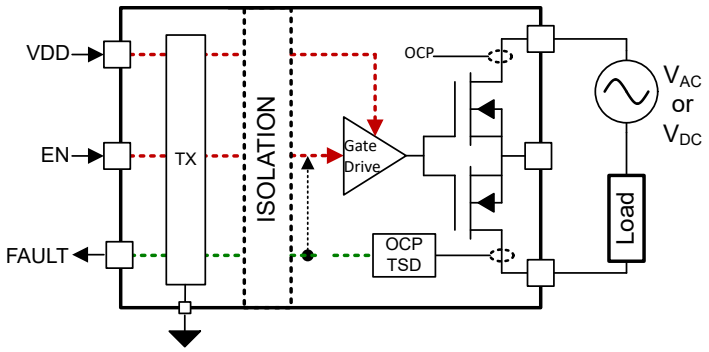
The primary side of the device is powered by only 5mA of input current and incorporates a fail-safe EN pin preventing any possibility of back powering the VDD supply. In most applications, the VDD pin of the device must connect to a system supply from 3.0V to 5.5V and the EN pin of the device must be driven by a GPIO output with logic HI from 1.8V to 5.5V. In other applications, the VDD and EN pins can be driven together directly from the system supply or from a GPIO output.

The secondary side consists of back-to-back MOSFETs with a standoff voltage of ±80V from S1 to S2. The TPSI8830 integrates bidirectional overcurrent protection to prevent damage due to output miswiring or short to ground.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPSI8830	DFP (SOIC, 14)	5.4mm × 10.5mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Diagram

ADVANCE INFORMATION

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Table of Contents

4 Device Comparison Table

over operating free-air temperature range (unless otherwise noted)

Device	Variant	Operating Voltage	Rdson	OCP	Fault Response
TPSI8830	TPSI8830A	-80 to 80V	30mΩ	4A	Programmable
	TPSI8830B	-80 to 80V	30mΩ	6A	Programmable
	TPSI8830AZ	-80 to 80V	30mΩ	4A	Programmable
	TPSI8830BZ	-80 to 80V	30mΩ	6A	Programmable

ADVANCE INFORMATION

ADVANCE INFORMATION

5 Pin Configuration and Functions

Figure 5-1. TPSI88xx DFP Package, 14-Pin SOIC (Top View)

Table 5-1. Pin Functions

PIN NO.	PIN NAME	TYPE(1)	DESCRIPTION
1	GND	GND	Ground supply for primary side
2	VDD	P	Power supply for primary side
3	NC	NC	No connect
4	$\overline{\text{FAULT}}$	I	Open drain global fault output. Referred to FLT, or fault pin.
5	EN	I	Switch Enable
6	TMR	I	Connect to capacitor to set retry time. Short to ground to configure fault to Latch-off.
7	NC	NC	No connect
8	GND	GND	Ground supply for primary side
9	S2	P	Switch Input
11	SM	P	Internally connected, connect to SM
12	SM	P	Common Source Connection
13	SM	P	Common Source Connection
14	SM	P	Internally connected, connect to SM
16	S1	P	Switch Input

(1) P = power, I = input, O = output, GND = ground, NC = no connect

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		MIN	MAX	UNIT
V_{VDD}	Primary side supply voltage(2)	–0.3	6	V
V_{FAULT}	$\overline{FAULT}$ pin voltage	–0.3	6	V
V_{TMR}	TMR pin voltage	–0.3	6	V
V_{EN}	Enable Voltage(2)	–0.3	6	V
$V_{S1,S2}$	Switch input voltage	-87	87	V
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C
Transient Isolation Voltage	AC Voltage, t = 60s		500	V_{RMS}
	DC Voltage, t = 60s		800	V_{DC}

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Voltage values are with respect to GND.

6.2 ESD Ratings

				VALUE	UNIT
HBM	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 2	All pins	±TBD	V
HBM_{Prim}	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 2	Primary Side Pins No. 1-8	±2000	V
HBM_{Sec}		Human body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 1C	Secondary Side Pins No. 9-16	±2000	V
CDM	Electrostatic discharge	Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4	All pins	±TBD	V

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$V_{S1,S2}$	Switch input voltage		-80		80	V
V_{VDD}	Primary side supply voltage		3.0		5.5	V
V_{FAULT}	$\overline{FAULT}$ pin voltage		0		5.5	V
V_{TMR}	TMR pin Voltage		0		5.5	V
V_{EN}	Enable Voltage		0		5.5	V
$I_{S1,S2}$	Switch current, S1/S2				4	A
V_{IOWM}	Functional Isolation Working Voltage	AC Voltage (Sine Wave)			200	V_{RMS}
		DC Voltage			250	V_{DC}
T_A	Ambient temperature		-40		125	°C
C_L	Capacitive Load	80V			1.5	uF

ADVANCE INFORMATION

6.4 Thermal Information

THERMAL METRIC (1)		DEVICE SOIC 14 PINS	UNIT
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	TBD	°C/W
$R_{\Theta JA, EVM, 60S}$	Junction-to-ambient thermal resistance(2) (3)	TBD	°C/W
$R_{\Theta JA, EVM, 5S}$	Junction-to-ambient thermal resistance(2) (4)	TBD	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	TBD	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	TBD	°C/W
ψ_{JT}	Junction-to-top characterization parameter	TBD	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	TBD	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.
(2) EVM PCB dimensions are 74.25mm × 43mm × 1mm. 4 layer PCB with 2oz Cu on layers 1,4 and 1oz Cu on layer 2,3.
(3) Performance of EVM with power applied for 60s.
(4) Performance of EVM with power applied for 5s.

6.5 Electrical Characteristics

Unless otherwise noted, all minimum/maximum specifications are over recommended operating conditions. All typical values are measured at T_A = 25°C, V_{VDD} = 3.0V to 5.5V, V_{EN} = 5V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PRIMARY SIDE SUPPLY (VDD)						
V_{UVLO}	VDD undervoltage threshold	VDD rising	2.7	2.9	3.0	V
		VDD falling	2.6	2.8	2.9	V
		Hysteresis	100	120	130	mV
I_{VDD_ON}	VDD current, 3.3V, device powered on	V_{VDD} = 3.3V, V_{EN} = V_{VDD} V T_J = 25°C		5	6.2	mA
		V_{VDD} = 3.3V, V_{EN} = V_{VDD} –40°C ≤ T_J ≤ 150°C		5	6.5	
	VDD current, 5.5V device powered on	V_{VDD} = 5.5V, V_{EN} = V_{VDD}, T_J = 25°C		4.5	5.2	
		V_{VDD} = 5.5V, V_{EN} = V_{VDD} , –40°C ≤ T_J ≤ 150°C		4.5	6.5	
I_{VDD_OFF}	VDD current, device powered off	V_{EN} = 0V T_J = 25°C		6	10	µA
		V_{EN} = 0V T_J = 85°C		6.3	11	
		V_{EN} = 0V T_J = 105°C		7.6	15	
		V_{EN} = 0V T_J = 125°C			30	
FET CHARACTERISTICS 30mΩ						

Unless otherwise noted, all minimum/maximum specifications are over recommended operating conditions. All typical values are measured at T_A = 25°C, V_{VDD} = 3.0V to 5.5V, V_{EN} = 5V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{DSON}	On resistance Connection A	I_O = 100mA, T_J = 25°C		30	35	mΩ
		I_O = 100mA, T_J = 85°C		43	50	
		I_O = 100mA, T_J = 105°C		45	50	
		I_O = 100mA, T_J = 125°C		45	55	
		I_O = 100mA, –40°C ≤ T_J ≤ 150°C			60	
	On Resistance, Connection B	I_O = 100mA, T_J = 25°C		8	10	mΩ
		I_O = 100mA, T_J = 85°C		10	12	
		I_O = 100mA, T_J = 105°C		10	15	
		I_O = 100mA, T_J = 125°C		12	15	
		I_O = 100mA, –40°C ≤ T_J ≤ 150°C			15	
	On resistance Connection C	I_O = 100mA, T_J = 25°C		15	20	mΩ
		I_O = 100mA, T_J = 85°C		20	25	
		I_O = 100mA, T_J = 105°C		22	25	
		I_O = 100mA, T_J = 125°C		25	30	
		I_O = 100mA, –40°C ≤ T_J ≤ 150°C			30	
I_{OFF_S1S2}	Off leakage, 80V, Both Directions, Connection A	V_{S1S2} = ±80V, T_J = 25°C			0.1	µA
		V_{S1S2} = ±80V, T_J = 85°C			3	
		V_{S1S2} = ±80V, T_J = 105°C			5	
		V_{S1S2} = ±80V, T_J = 125°C			15	
		V_{S1S2} = ±80V, –40°C ≤ T_J ≤ 150°C			50	
	Off leakage, 60V, Both Directions, Connection A	V_{S1S2} = ±60V, T_J = 25°C			0.1	
		V_{S1S2} = ±60V, T_J = 85°C			1	
		V_{S1S2} = ±60V, T_J = 105°C			3	
		V_{S1S2} = ±60V, T_J = 125°C			10	
		V_{S1S2} = ±60V, –40°C ≤ T_J ≤ 150°C			40	
	Off leakage, 24V, Both Directions, Connection A	V_{S1S2} = ±24V, T_J = 25°C			0.1	
		V_{S1S2} = ±24V, T_J = 85°C			1	
		V_{S1S2} = ±24V, T_J = 105°C			1.5	
		V_{S1S2} = ±24V, T_J = 125°C			6	
		V_{S1S2} = ±24V, –40°C ≤ T_J ≤ 150°C			25	

ADVANCE INFORMATION

ADVANCE INFORMATION

Unless otherwise noted, all minimum/maximum specifications are over recommended operating conditions. All typical values are measured at T_A = 25°C, V_{VDD} = 3.0V to 5.5V, V_{EN} = 5V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OFF_S1S2}	Off leakage, 80V, Connection B, C	V_{S1S2} = +80V, T_J = 25°C			0.1	µA
		V_{S1S2} = +80V, T_J = 85°C			4	
		V_{S1S2} = +80V, T_J = 105°C			10	
		V_{S1S2} = +80V, T_J = 125°C			30	
		V_{S1S2} = +80V, –40°C ≤ T_J ≤ 150°C			100	
	Off leakage, 60V, Connection B, C	V_{S1S2} = +60V, T_J = 25°C			0.2	
		V_{S1S2} = +60V, T_J = 85°C			2	
		V_{S1S2} = +60V, T_J = 105°C			6	
		V_{S1S2} = +60V, T_J = 125°C			20	
		V_{S1S2} = +60V, –40°C ≤ T_J ≤ 150°C			80	
	Off leakage, 24V, Connection B, C	V_{S1S2} = +24V, T_J = 25°C			0.2	
		V_{S1S2} = +24V, T_J = 85°C			1	
		V_{S1S2} = +24V, T_J = 105°C			3	
		V_{S1S2} = +24V, T_J = 125°C			12	
		V_{S1S2} = +24V, –40°C ≤ T_J ≤ 150°C			50	
C_{OSS}	S1, S2 capacitance	$V_{S1,S2}$ = 0V, SM float, F = 1MHz		75		pF
PROTECTION 30mΩ (TSD, OCP)						
I_{OCP}	Over Current Protection Threshold	Device Version A, Configuration A, V = ±80V	4			A
I_{OCP}	Over Current Protection Threshold	Device Version B, Configuration A, V = ±80V	6			A
t_{OCP}	Over-Current Protection Response Time	Current Slew Rate = 3A/µs		8		µs
C_{Load}	Load capacitance without a false trip due to high inrush current.	V = 80V			1.5	µF
T_{SD}	Thermal Shutdown			170		°C
ZERO CROSS						
Z_{th}	Zero Cross Detection Threshold	Freq = 60Hz V_S = 24VAC, I_{Load} = 1A_{RMS} Switch is ON when I_{S1} = 50mA	-2.4		2.4	V
Z_{Tpd}	Zero Cross Detection to turn on time				1000	us
LOGIC-LEVEL INPUT (EN)						
V_{IL}	Input logic low voltage		0.0		0.65	V
V_{IH}	Input logic high voltage		0.95		5.5	V
V_{HYS}	Input logic hysteresis		100	250	300	mV
I_{IL}	Input logic low current	V_{EN} = 0V	–0.1		0.1	µA
		V_{EN} = 0.8V	0.5	0.85	2.25	µA
I_{IH}	Input logic high current	V_{EN} = 5V	4	5.5	8	µA
I_{VDD_FS}	VDD fail-safe current	V_{EN} = 5V, V_{VDD} = 0V	–0.1	0	0.1	µA
R_{PD}	Pulldown resistance	V_{EN} = 0.6V		1000		kΩ
OPEN-DRAIN OUTPUTS($\overline{FAULT}$)						
V_{OL_FLT}	Output Low Voltage	$I_{\overline{FAULT}}$ = 1mA		0.5		V
I_{OFF_FLT}	Off-state Leakage	$V_{\overline{FAULT}}$ = 5V	5e-05	1e-4	5	µA

6.6 Switching Characteristics

Unless otherwise noted, all minimum/maximum specifications are over recommended operating conditions. All typical values are measured at T_A = 25°C, V_{VDD} = 5V, V_{EN} = 5V.

MODE	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SWITCHING CHARACTERISTICS							
EN switching	t_{PD_ON}	Input HI to Output voltage falling propagation delay	V_{S1S2} = 24V R_L = 48Ω		115	200	µs
	t_F	Output fall time			40	TBD	
	t_{PD_OFF}	Input LO to Output voltage rising propagation delay			20	50	
Fault Indication	T_{FAULT}	Time between fault detected and FAULT asserting from OCP or TSD				500	µs
	T_{RETRY}	Time between fault detected and enable auto-retry time	TMR = 100pF		100		µs
			TMR = 1nF		1		ms
			TMR = 10nF		10		ms
			TMR = 100nF		100		ms
			TMR = 1uF		1		s
			TMR = GND		Latch-Off		

ADVANCE INFORMATION

7 Parameter Measurement Information

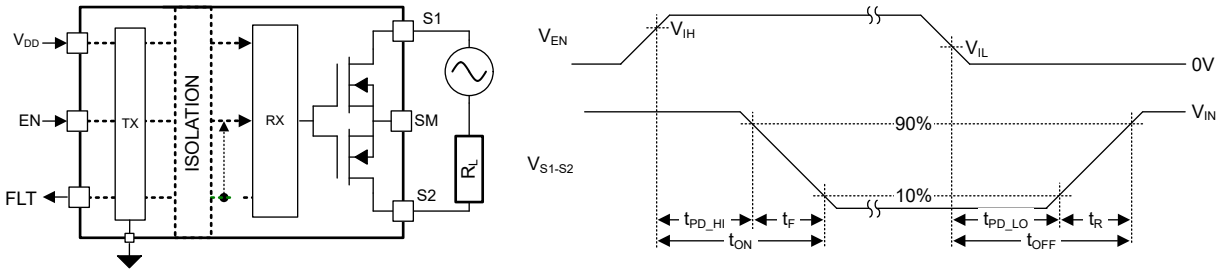

Figure 7-1. Timing Diagram

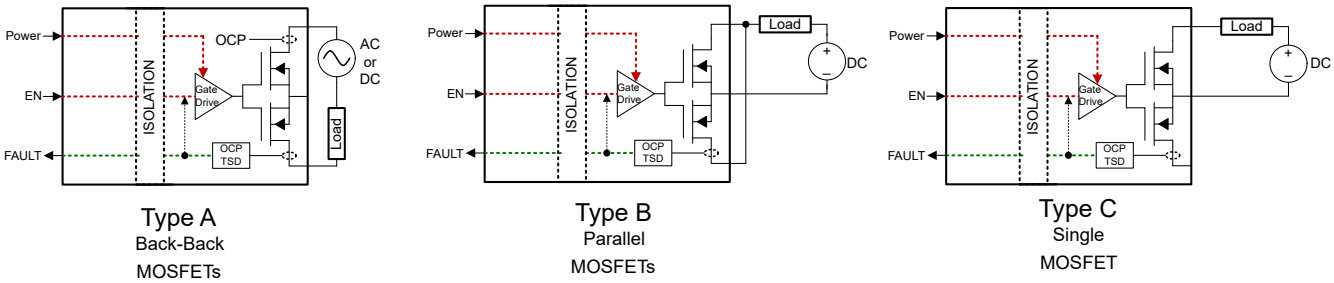

Figure 7-2. Connection Diagrams

8 Detailed Description

8.1 Overview

The TPSI8830 is an isolated solid-state relay designed for high voltage industrial applications. TI's high reliability capacitive isolation technology in combination with back-to-back MOSFETs form a completely integrated option requiring no secondary side power supply.

As seen in the *Functional Block Diagram*, the primary side consists of a driver which delivers power and enable logic information to each of the internal MOSFETs on the secondary side. When the enable pin is brought HI and the VDD voltage is above the UVLO threshold, the oscillator starts and the driver sends power and a logic HI across the isolation barrier. When the enable pin is brought LO or the VDD voltage falls below the UVLO threshold, the driver is disabled.

TPSI8830 integrates overcurrent protection which detects when the current flowing through the MOSFET has increased beyond I_{OCP} at which point it disables the MOSFETs and sends a signal back to the primary side across isolation to let the MCU know that the MOSFETs have been disabled. Configure TPSI8830 to latch-off the power path or auto-retry by using the TMR pin.

The MOSFETS in TPSI8830 are configurable in a back-back configuration to provide bidirectional off-state blocking. Alternatively, parallel the MOSFETS to help minimize power dissipation at the trade-off of bidirectional off-state blocking.

8.2 Functional Block Diagram

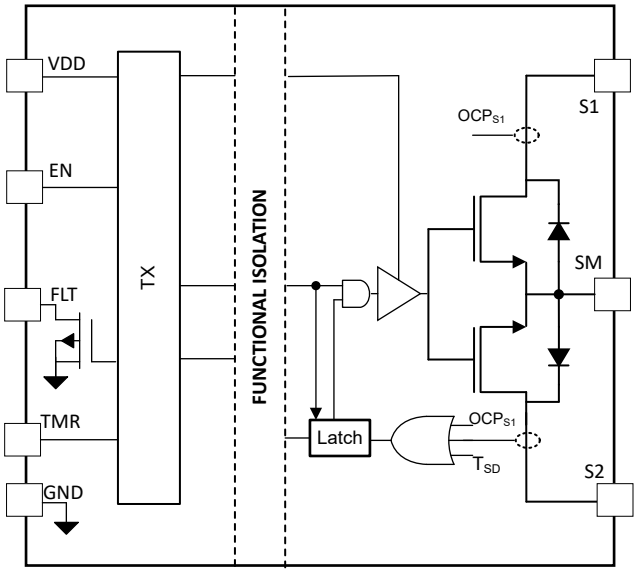

Figure 8-1. TPSI88xx Block Diagram

8.3 Feature Description

8.3.1 Configurable Fault Response Timer (TMR)

TPSI8830 integrates a configurable fault response timer. When the pin is shorted, the device latches-off the power path in the event of a fault such as overcurrent protection or thermal shutdown.

8.3.1.1 Fault Latch-OFF

When the TMR pin is shorted to ground, the device behaves in latch-off behavior. This provides the system the flexibility to re-enable the device once faults are cleared and prevents the device from re-enabling into a fault state. This behavior requires the MCU to reset the device through EN pin or power cycle the VDD pin.

ADVANCE INFORMATION

8.3.1.2 Fault Auto-Retry

When the TMR pin open or a capacitor is connected to primary side ground, the device auto-retries when a fault is present. The capacitor size connected to the pin determines the retry time (T_{RETRY}). The device continues to auto-retry until the fault is cleared, at which point it resumes normal operation.

8.3.2 Over-Current Protection (OCP)

When the current across S1S2 exceeds the I_{OCP} threshold, the device disables the power path within t_{OCP}. This establishes that the device does not get damaged due to the high di/dt created by an external short or miswire. After the OCP is tripped, the $\overline{FAULT}$ pin is asserted low. The fault response behavior follows the TMR pin configuration described in the previous section.

8.3.3 Thermal Shutdown

When the junction temperature rises up beyond T_{ABS_R} the device disables the power path and send a fault signal back to the primary side. After the thermal shutdown is triggered, the $\overline{FAULT}$ pin is asserted low. The device follows the behavior programmed by TMR (Latch-off or auto-retry). A TVS or other clamping circuit is recommended to absorb any inductive energy from the load when the device shuts down.

8.3.4 Zero-Cross Turn On

The zero cross detection feature is offered on devices with the Z suffix and is targeted for AC systems.

When the device is enabled, it delays turn-on until the voltage between S1 and S2 drops to zero. This minimizes stress on the device, especially when driving large capacitive loads. Without this feature, the inrush current can cause an unwanted trip of the overcurrent protection.

When the device is disabled using the EN pin, TSD event, or OCP event, the device shuts down immediately and does not wait for the voltage between S1 and S2 to drop to zero. When driving inductive loads, this immediate shut-off causes a voltage spike. A TVS or other clamping circuit is recommended to absorb any inductive energy from the load when the device shuts down.

8.4 Device Functional Modes

Table 8-1. Device Functional Modes

VDD	EN	S1S2 State	I_{S1S2}	$\overline{FAULT}$	COMMENTS
Powered Up(1)	L	OFF	X	Hi-Z	VDD current is in OFF state range.
	H	ON	$<I_{OCP}$ $T_j < T_{SD}$	Hi-Z	VDD current is in ON state range.
	H	OFF	$>I_{OCP}$, $T_j < T_{SD}$	Low-Z	Over-Current Detected and power path disabled
	H	OFF	$<I_{OCP}$, $T_j > T_{SD}$	Low-Z	Over Temperature detected and power path disabled
Powered Down(2)	L	OFF	X	Hi-Z	VDD current is in OFF state range.
	H	OFF	X	Hi-Z	Primary side analog is powered on, VDD current is between OFF state and ON state ranges.

(1) VDD ≥ VDD undervoltage rising threshold.
(2) VDD ≤ VDD undervoltage falling threshold.

ADVANCE INFORMATION

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The integrated back-to-back MOSFETs and inter-gated functional isolation of the TPSI8830 allow the device to switch AC or DC loads and replace traditional mechanical relay and photo relays. In this application, the device is configured to switch 24VAC loads in a home thermostat.

9.2 Typical Application

9.2.1 Thermostat

Figure 9-1 shows the a typical application of TPSI8830 being used as an output relay for a smart thermostat, replacing mechanical relays or photo-relays. A variety of different loads are connectable, including relays, contactors, and solenoids.

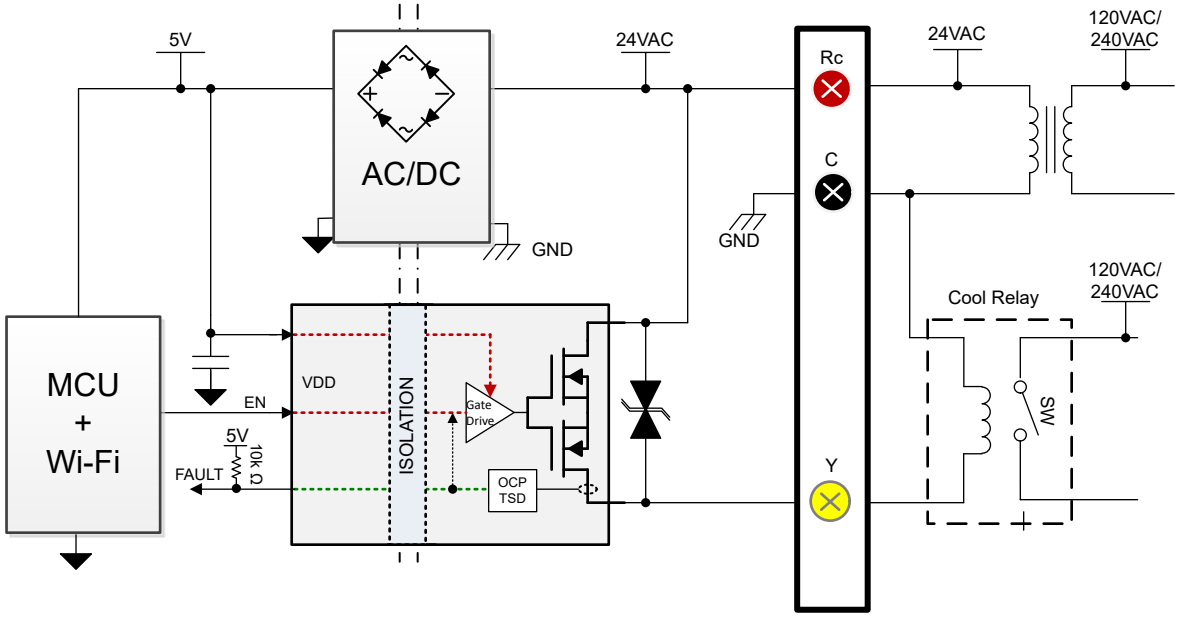

Figure 9-1. Typical Thermostat block diagram

Galvanic isolation is required to control the 24VAC loads from the low voltage MCU, as they do not share the same ground. The 24VAC transformer powering the thermostat provides isolation to protect the user from the mains voltage. Typically this isolation operates with less than 100V across it at any time. The TPSI8830 provides an integrated isolation barrier that can withstand 200VAC for the lifetime of the device, and surges up to 800VDC for 60 seconds.

The TPSI8830 features a low on-resistance of 30mΩ, minimizing self-heating within the thermostat housing even at higher currents, confirming the temperature sensor remains as close to ambient temperature as possible.

ADVANCE INFORMATION

9.2.2 System Level Testing

The TPSI8830 is designed to support the different industrial standards IEC-61000-4X in conjunction with an external bidirectional TVS placed across the S1 and S2 terminals. Size this TVS according to the class required.

The TPSI8830 uses TI's low EMI driver technology in combination with SSM (Spread Spectrum Modulation) to minimize radiated emissions. To establish good EMC performance, TI recommends placing a 0402 100nF capacitor between pins 1 and 2, as close as manufacturing rules allow. An additional system capacitance of 1µF or more on the VDD rail is also recommended. With these EMC considerations, the TPSI8830 can pass CISPR 32 Class B.

9.2.3 Design Requirements

Table 9-1. Typical Design Parameters For TPSI8830

PARAMETER	VALUE
Nominal S1S2 Voltage	24VAC ±10%
Primary side supply (V_{VDD})	5V ±10%
Nominal load current	187mA
Load inductance	340mH

9.2.4 Detailed Design Procedure

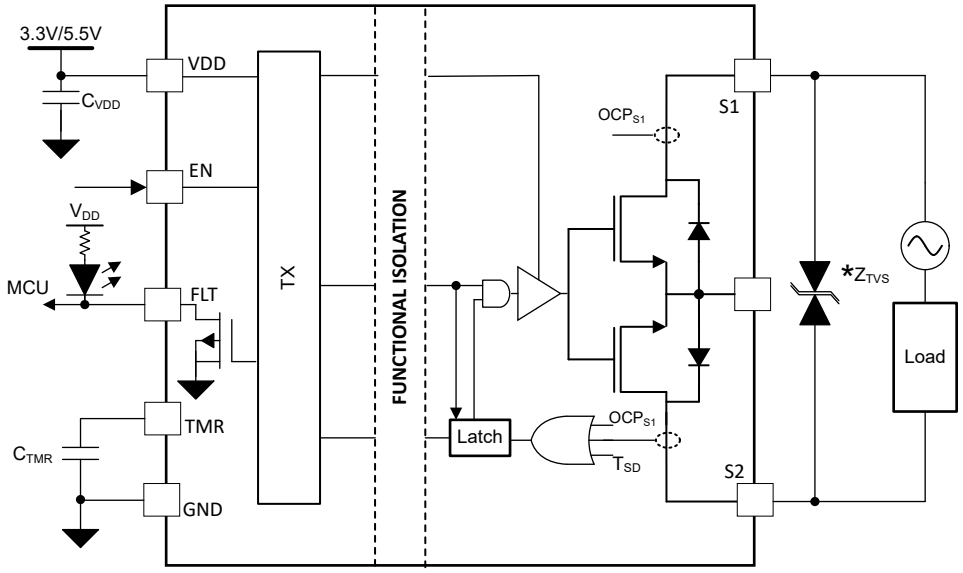

Figure 9-2. Typical Application Diagram

When the TPSI8830 turns on, an inrush current flows through the device for a short duration. Selecting the variant with the desired minimum OCP threshold establishes a false trip does not occur during the initial inrush.

When the switch is turned off, inductive loads causes a voltage spike. The avalanche capability of the device's integrated MOSFETs is limited, and they can only survive a few tens of millijoules of total avalanche energy. It is therefore recommended to place a TVS diode, MOV, or other clamping circuit across the S1 and S2 terminals when driving large inductive loads. The device or clamping circuit must dissipate the energy stored in the load at peak current during each cycle.

During a fault condition, such as a short circuit, the TPSI8830 or an external clamping circuit must dissipate the energy stored in the system's inductance (such as long wires or the magnetizing inductance of a 24VAC transformer). If the device is configured to use the auto retry functionality with the TMR pin, select an appropriate

retry time to establish that heat that dissipated during avalanche did not damage the clamping circuit nor the TPSI8830.

9.3 Power Supply Recommendations

To establish a reliable supply voltage, TI recommends placing a minimum of 100nF ceramic capacitor between the VDD pin and the GND pin of the TPSI8830. Place the capacitor as close a manufacturing rules allow to the VDD pin of the device. An additional system capacitance of 1µF or more on the VDD rail is also recommended.

9.4 Layout

9.4.1 Layout Guidelines

PCB designers must take a few items into consideration when placing the TPSI8830 on the circuit board.

Place the TVS or other clamping circuit recommended close to the device to minimize the inductance between the device and the clamping circuit. In space constrained applications, placing the clamp on the same circuit board as the TPSI8830, near the field-side connector, is acceptable.

To establish good EMC performance, TI recommends placing a 0402 100nF capacitor between pins 1 and 2, as close as manufacturing rules allow.

9.4.1.1 EMI Considerations

The TPSI8830 employs spread-spectrum modulation (SSM) and TI's low EMI driver technology. Additional system design considerations are not required to meet the EMI performance needs if the layout and power supply recommendations are followed.

9.4.2 Layout Example

Figure 9-3 shows a PCB layout example with the signals and components labeled.

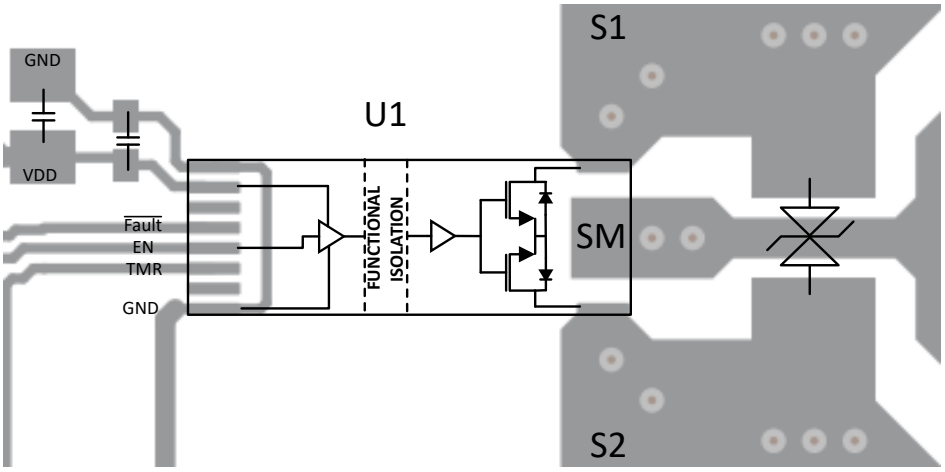

Figure 9-3. TPSI8830 Layout Example

ADVANCE INFORMATION

ADVANCE INFORMATION

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Third-Party Products Disclaimer

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10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
May 2026	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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