12-Channel 1:2 MUX/DEMUX Switch with Integrated 4-Channel Sideband Signal Switching for DVI/HDMI and DisplayPort (DP) Applications

Check for Samples: TS3DV621

FEATURES

- **Switch Type: 2:1 or 1:2**
- **Data Rate Compatibility**
  - **HDMI v1.4**
  - **DVI 1.0**
  - **DisplayPort 1.1a**
- **Bandwidth (-3dB) – 2.2 GHz**
- **R_{ON} – 8 Ω**
- **C_{ON} – 5.6 pF**
- **V_{CC} Range – 3.0V–3.6 V**
- **I/O Voltage Range – 0–5 V**
- **Bit-to-Bit Skew – 6 ps Typical**
- **Propagation Delay – 40 ps Typical**
- **Special Features**
  - **Dedicated Enable Logic Supports Hi-Z Mode**
  - **I_{OFF} Protection Prevents Current Leakage in Powered Down State (V_{CC} = 0 V)**
- **ESD Performance**
  - **2kV Human Body Model (A114B, Class II)**
  - **1kV Charged Device Model (C101)**
- **42-pin QFN Package (9 x 3.5 mm, 0.5 mm Pitch)**

APPLICATIONS

- **DVI/HDMI/DisplayPort Signal Switching**
- **General Purpose TMDS/LVDS Signal Switching**

DESCRIPTION

The TS3DV621 is a 1:2 or 2:1 bi-directional multiplexer/demultiplexer with a integrated 4 side-band control channel (DDC, AUX, CEC, or HPD) signal switcher. Operating from a 3 to 3.6V supply, the TS3DV621 offers low and flat ON-state resistance as well as low I/O capacitance, which allows the TS3DV621 to achieve a typical bandwidth of 2.2 GHz. The device provides the high bandwidth necessary for HDMI, DVI, and DisplayPort applications. The TS3DV621 expands the high-speed physical link interface from a single HDMI port to two HDMI ports (A or B port) or vise-versa. It can also be used for DisplayPort (DP) source/sink applications. The integrated side-band control channels allow 5V signals to pass through, making the TS3DV621 suitable for HDMI applications.

The most common application for the TS3DV621 is the sink application. In this case, there are two possible sources (DVD, set-top box, or game console) that are routed to one receiver. The unselected port is in the high-impedance mode, such that the receiver receives information from only one source. HDCP encryption is passed through the switch for the receiver to decode.

ORDERING INFORMATION

For package and ordering information, see the Package Option Addendum at the end of this document.

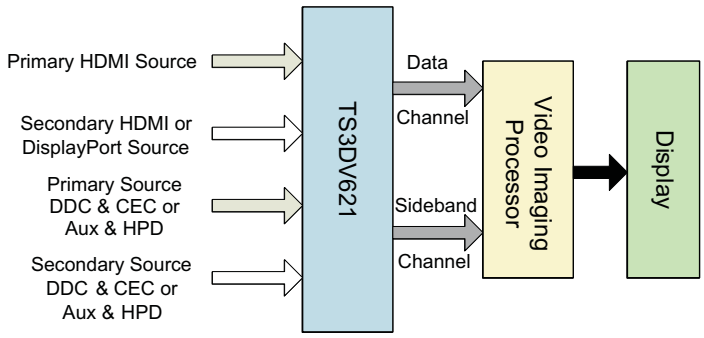
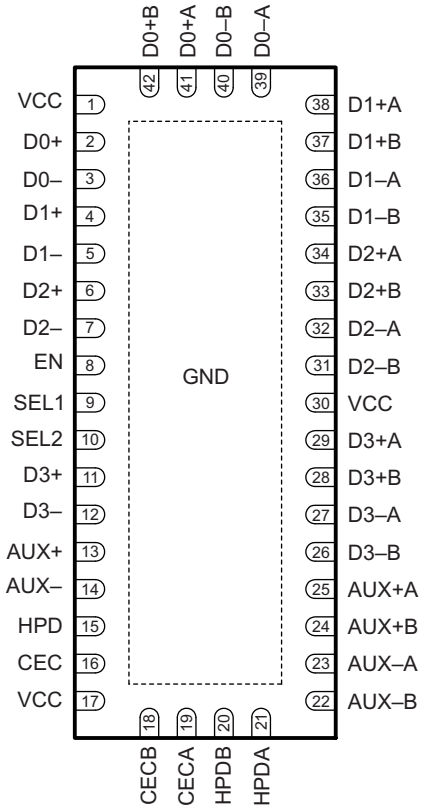


Figure 1. Multiplexing Dual Video Input Source (HDMI/DisplayPort)

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN FUNCTIONS



PIN		I/O TYPE	DESCRIPTION
NAME	NO.		
VCC	1,17, 30	Power	Supply Voltage
GND	PowerPad	Ground	Ground
EN	8	I	Enable Input
SEL1	9	I	Select Input 1
SEL2	10	I	Select Input 2
D0+A	41	I/O	Port A, Lane 0, +ve signal
D0-A	39	I/O	Port A, Lane 0, -ve signal
D1+A	38	I/O	Port A, Lane 1, +ve signal
D1-A	36	I/O	Port A, Lane 1, -ve signal
D2+A	34	I/O	Port A, Lane 2, +ve signal
D2-A	32	I/O	Port A, Lane 2, -ve signal
D3+A	29	I/O	Port A, Lane 3, +ve signal
D3-A	27	I/O	Port A, Lane 3, -ve signal
D0+B	42	I/O	Port B, Lane 0, +ve signal
D0-B	40	I/O	Port B, Lane 0, -ve signal
D1+B	37	I/O	Port B, Lane 1, +ve signal
D1-B	35	I/O	Port B, Lane 1, -ve signal
D2+B	33	I/O	Port B, Lane 2, +ve signal
D2-B	31	I/O	Port B, Lane 2, -ve signal
D3+B	28	I/O	Port B, Lane 3, +ve signal
D3-B	26	I/O	Port B, Lane 3, -ve signal
D0+	2	I/O	Common Port, Lane 0, +ve signal
D0–	3	I/O	Common Port, Lane 0, -ve signal
D1+	4	I/O	Common Port, Lane 1, +ve signal
D1–	5	I/O	Common Port, Lane 1, -ve signal
D2+	6	I/O	Common Port, Lane 2, +ve signal
D2–	7	I/O	Common Port, Lane 2, -ve signal
D3+	11	I/O	Common Port, Lane 3, +ve signal
D3-	12	I/O	Common Port, Lane 3, -ve signal
AUX+A	25	I/O	+ve AUX Channel for Port A
AUX-A	23	I/O	-ve AUX Channel for Port A
HPDA	21	I/O	Port A HPD
CECA	19	I/O	Port A CEC
AUX+B	24	I/O	+ve AUX Channel for Port B
AUX-B	22	I/O	-ve AUX Channel for Port B
HPDB	20	I/O	Port B HPD
CECB	18	I/O	Port B CEC
AUX+	13	I/O	+ve AUX Channel for Common Port
AUX–	14	I/O	-ve AUX Channel for Common Port
HPD	15	I/O	HPD for Common Port
CEC	16	I/O	CEC for Common Port

LOGIC DIAGRAM

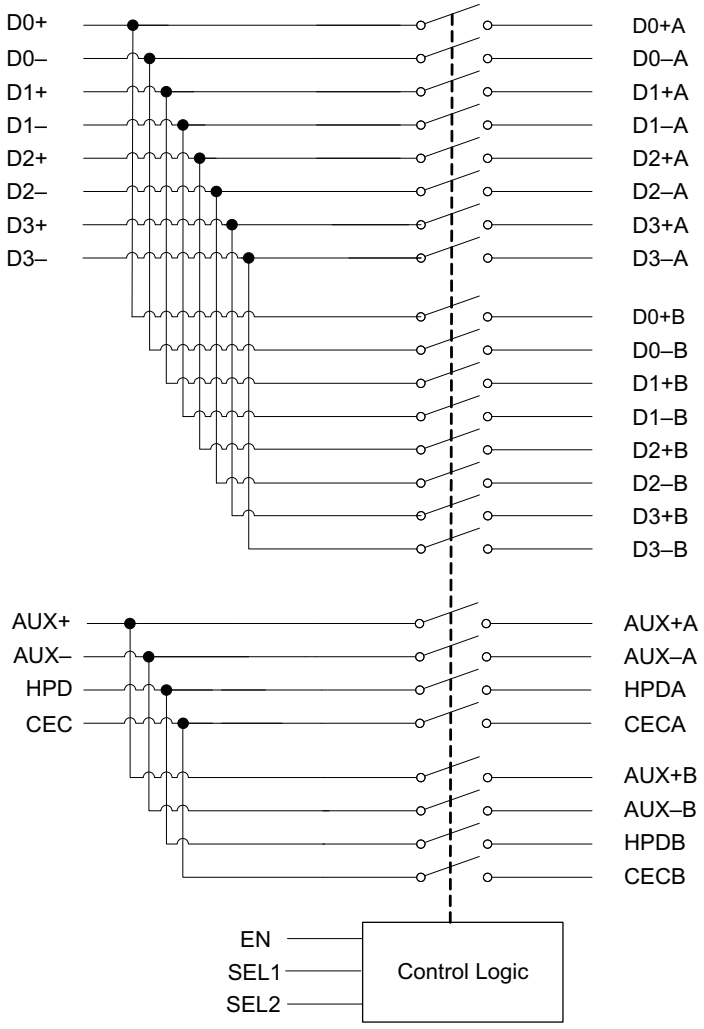


Table 1. FUNCTION TABLE

EN	SEL1	SEL2	FUNCTION
L	X	X	All I/O = High Impedance
H	L(1)	L(1)	Output port A = Input Output Port B = High Impedance
H	H(1)	H(1)	Output Port A = High Impedance Output Port B = Input

(1) Tie SEL1 and SEL2 together for easy output control

APPLICATION EXAMPLES

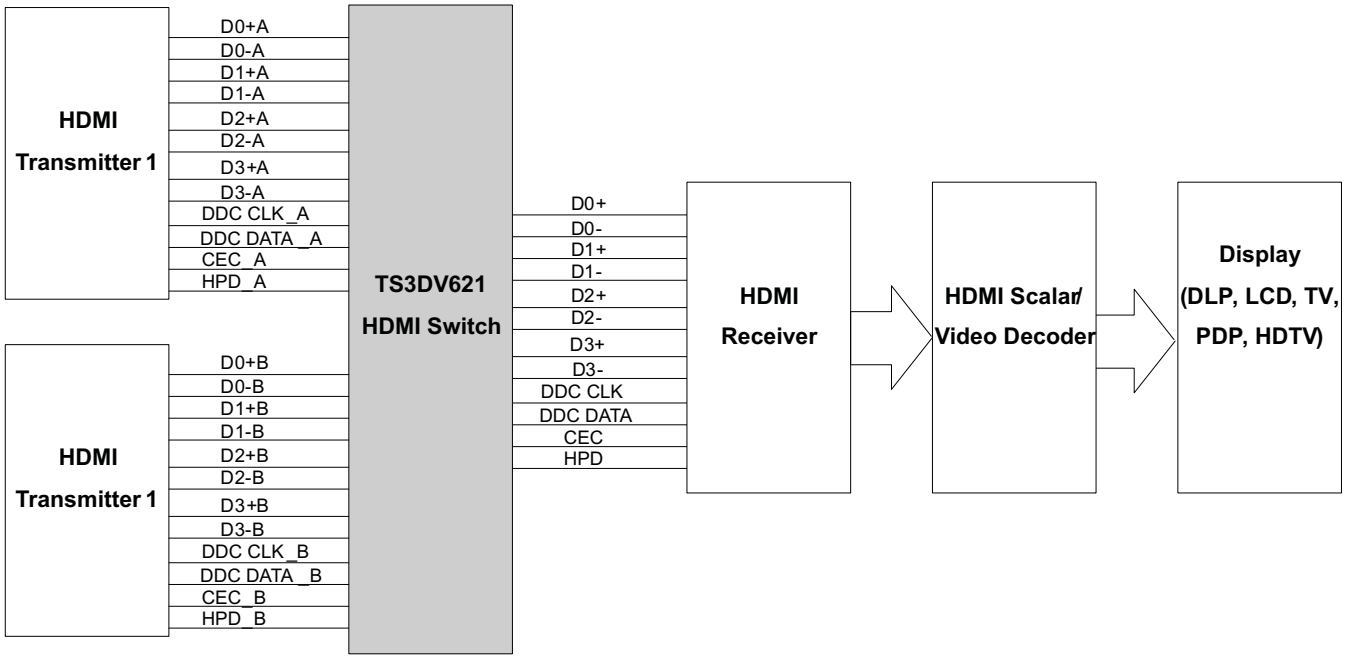


Figure 2. Dual HDMI Source Application

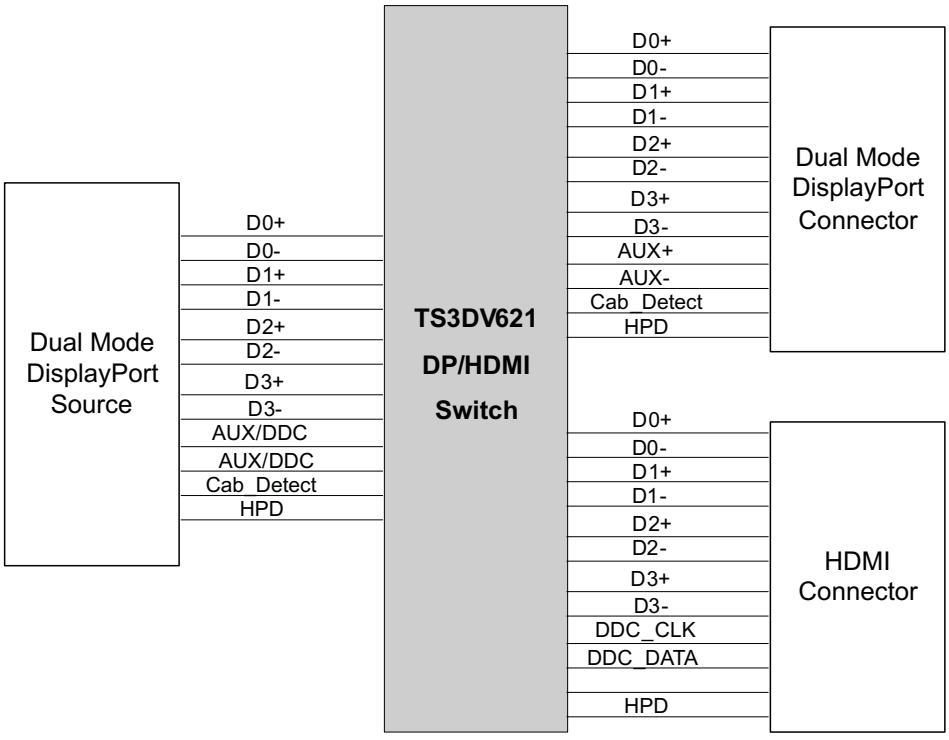


Figure 3. Dual-Mode DisplayPort Application

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	4.6	V
$V_{I/O}$	Analog voltage range(2)(3)(4)	All I/O	–0.5	7	V
V_{IN}	Digital input voltage range(2)(3)	SEL1, SEL2	–0.5	7	V
$I_{I/OK}$	Analog port diode current	$V_{I/O} < 0$		–50	mA
I_{IK}	Digital input clamp current	$V_{IN} < 0$		–50	mA
$I_{I/O}$	On-state switch current(5)	All I/O	–128	128	mA
I_{DD} I_{GND}	Continuous current through V_{DD} or GND		–100	100	mA
θ_{JA}	Package thermal impedance(6)	RUA package		31.8	°C/W
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
(5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.
(6) The package thermal impedance is calculated in accordance with JESD 51-7

RECOMMENDED OPERATING CONDITIONS(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		3	3.6	V
V_{IH}	High-level control input voltage	SEL1, SEL2	2	5.5	V
V_{IL}	Low-level control input voltage	SEL1, SEL2	0	0.8	V
V_{IN}	Input voltage	SEL1, SEL2	0	5.5	V
$V_{I/O}$	Input/Output voltage		0	5.5	V
T_A	Operating free-air temperature		–40	85	°C

(1) All unused control inputs of the device must be held at VDD or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS

PARAMETER			TEST CONDITIONS(1)	MIN	TYP(2)	MAX	UNIT
V_{IK}	Digital input clamp voltage	SEL1,SEL2	V_{CC} = 3.6 V, I_{IN} = -18 mA	– 1. 2	– 0. 8		V
R_{ON}	On-state resistance	All I/O	V_{CC} = 3 V, 1.5 V ≤ $V_{I/O}$ ≤ V_{CC}, $I_{I/O}$ = –40 mA		8	12	Ω
$R_{ON(flat)}$ (3)	On-state resistance flatness	All I/O	V_{CC} = 3 V, VI/O = 1.5 V and V_{CC}, $I_{I/O}$ = –40mA		1.5		Ω
ΔR_{ON} (4)	On-state resistance match between channels	All I/O	V_{CC} = 3 V, 1.5 V ≤ $V_{I/O}$ ≤ V_{CC}, $I_{I/O}$ = –40mA		0.4	1	Ω
I_{IH}	Digital input high leakage current	SEL1,SEL2	V_{CC} = 3.6 V , V_{IN} = V_{DD}			±1	µA
I_{IL}	Digital input low leakage current	SEL1,SEL2	V_{CC} = 3.6 V, V_{IN} = GND			±1	µA
I_{OFF}	Leakage under power off conditions	All outputs	V_{CC} = 0 V, $V_{I/O}$ = 0 to 3.6 V, V_{IN} = 0 to 5.5V			±1	µA
C_{IN}	Digital input capacitance	SEL1,SEL2	f = 1 MHz, V_{IN} = 0 V		2.6	3.2	pF
C_{OFF}	Switch OFF capacitance	All I/O	f = 1 MHz, $V_{I/O}$ = 0 V, Output is open, Switch is OFF		2		pF
C_{ON}	Switch ON capacitance	All I/O	f = 1 MHz, $V_{I/O}$ = 0 V, Output is open, Switch is ON		5.6		pF
I_{CC}	VCC supply current		V_{CC} = 3.6 V, $I_{I/O}$ = 0, V_{IN} = V_{DD} or GND		300	400	µA

(1) V_I, V_O, I_I, and I_O refer to I/O pins, V_{IN} refers to the control inputs
(2) All typical values are at V_{CC} = 3.3V (unless otherwise noted), T_A = 25°C
(3) $R_{ON(FLAT)}$ is the difference of R_{ON} in a given channel at specified voltages.
(4) ΔR_{ON} is the difference of R_{ON} from center port to any other ports.

SWITCHING CHARACTERISTICS

Over recommended operation free-air temperature range, V_{CC} = 3.3 V ± 0.3 V, R_L = 200 Ω, C_L = 4 pF (unless otherwise noted) (see and)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP(1)	MAX	UNIT
t_{pd} (2)	All I/O input side	All I/O output side		40		ps
t_{PZH}, t_{PZL}	SEL1, SEL2	All I/O	2		7	ns
t_{PHZ}, t_{PLZ}	SEL1, SEL2	All I/O	2		5	ns
$t_{sk(o)}$ (3)	All I/O input side	All I/O output side		6	30	ps
$t_{sk(p)}$ (4)				6	30	ps

(1) All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.
(2) The propagation delay is the calculated RC time constant of the typical ON-State resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).
(3) Output skew between center port and any other channel.
(4) Skew between opposite transitions of the same output $|t_{PHL} – t_{PLH}|$

DYNAMIC CHARACTERISTICS

Over recommended operation free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TYP(1)	UNIT
XTALK	R_L = 50 Ω, f = 250 MHz (Figure 11)	–43	dB
OIRR	R_L = 50 Ω, f = 250 MHz (Figure 12)	–42	dB
BW	R_L = 50 Ω, Switch ON (Figure 10)	2.2	GHz

(1) All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

OPERATING CHARACTERISTICS

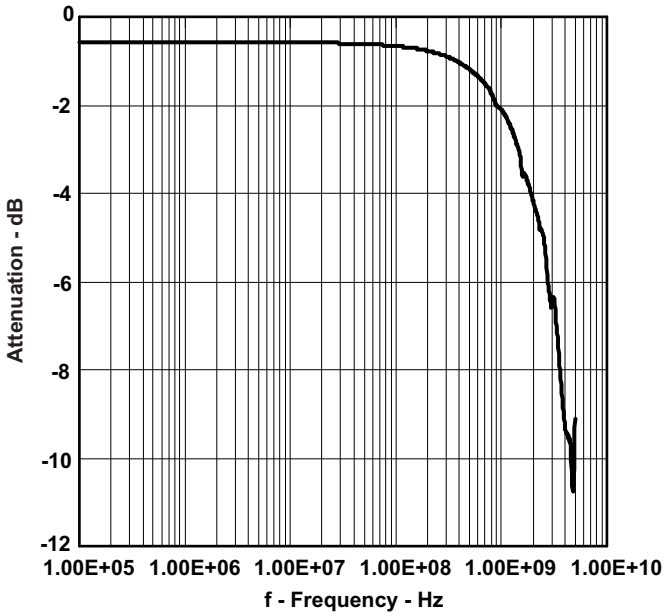


Figure 4. Gain vs Frequency

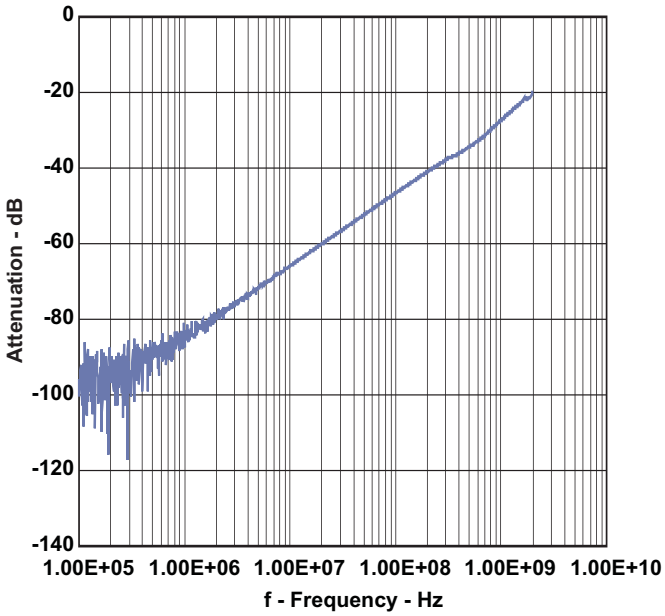


Figure 5. Off Isolation vs Frequency

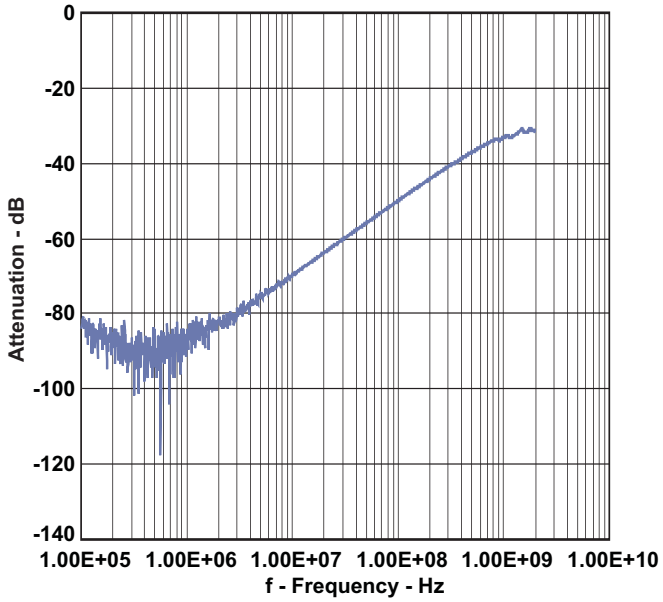


Figure 6. Crosstalk vs Frequency

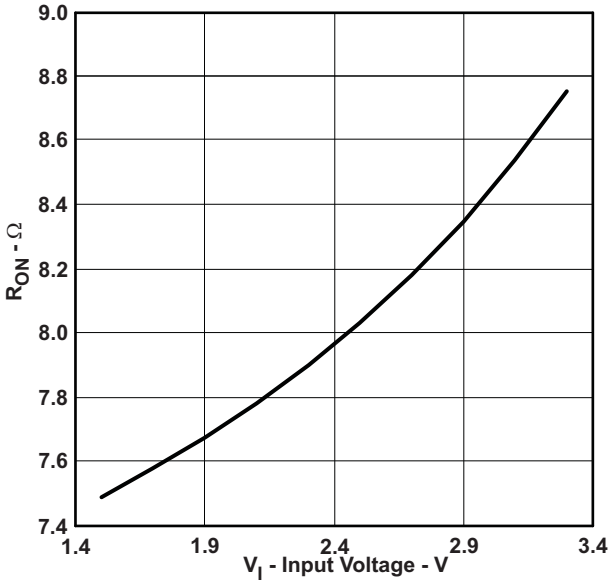
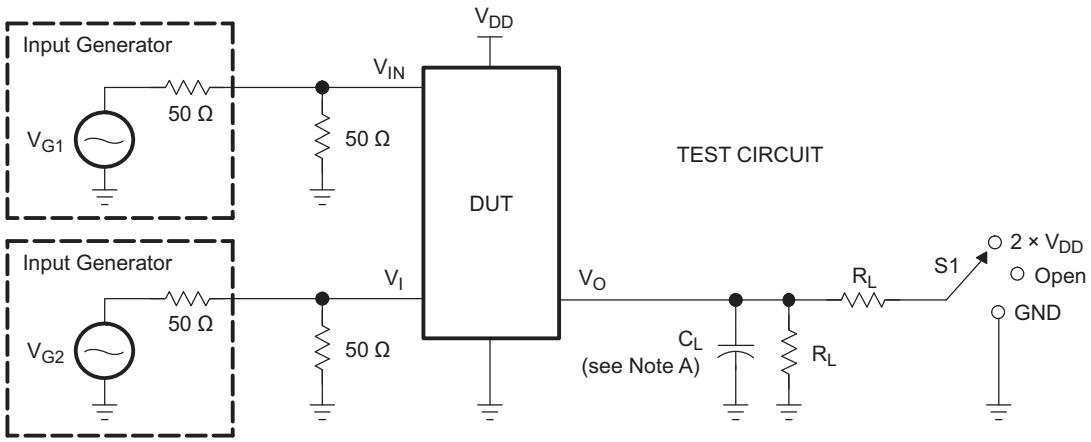


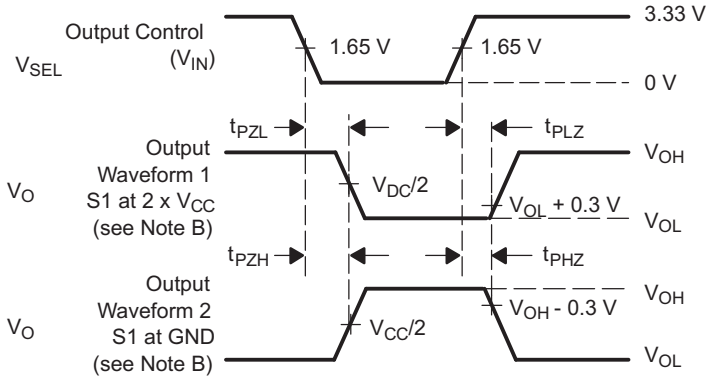
Figure 7. R_{ON} vs V_{IN}

PARAMETER MEASUREMENT INFORMATION

Enable and Disable Times



TEST	V_{DD}	S1	R_L	V_{in}	C_L	V_Δ
t_{PLZ}/t_{PZL}	3.3 V ± 0.3 V	2 × V_{DD}	200 Ω	GND	4 pF	0.3 V
t_{PHZ}/t_{PZH}	3.3 V ± 0.3 V	GND	200 Ω	V_{DD}	4 pF	0.3 V



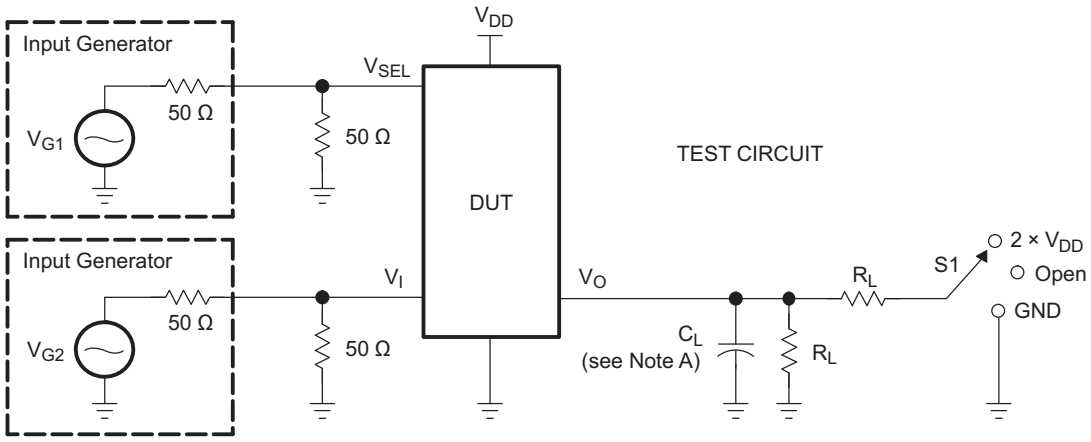
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics:PRR ≤10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.

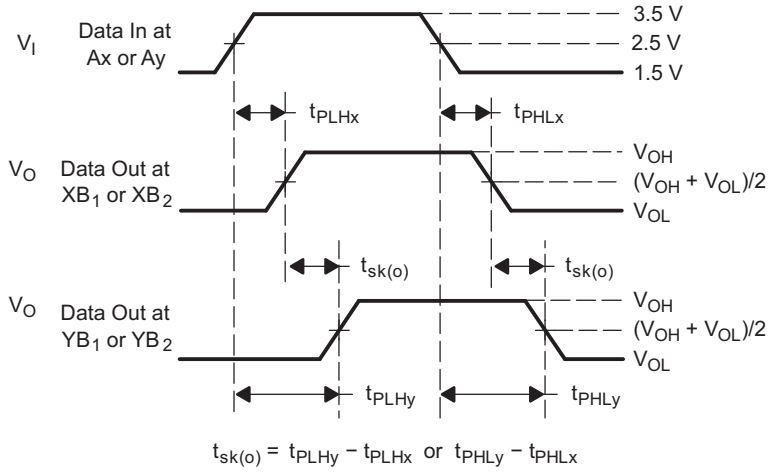
Figure 8. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

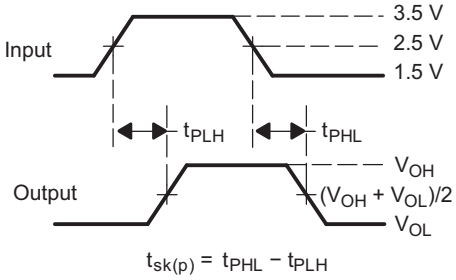
Skew



TEST	V_{CC}	S1	R_L	V_{in}	C_L
$t_{sk(o)}$	3.3 V ± 0.3 V	Open	200 Ω	V_{CC} or GND	4 pF
$t_{sk(p)}$	3.3 V ± 0.3V	Open	200 Ω	V_{CC} or GND	4 pF



VOLTAGE WAVEFORMS
OUTPUT SKEW ($t_{sk(o)}$)



VOLTAGE WAVEFORMS
PULSE SKEW [$t_{sk(p)}$]

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.

Figure 9. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

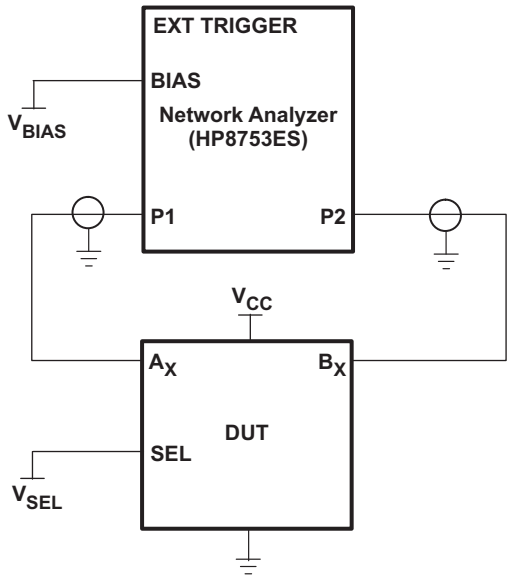


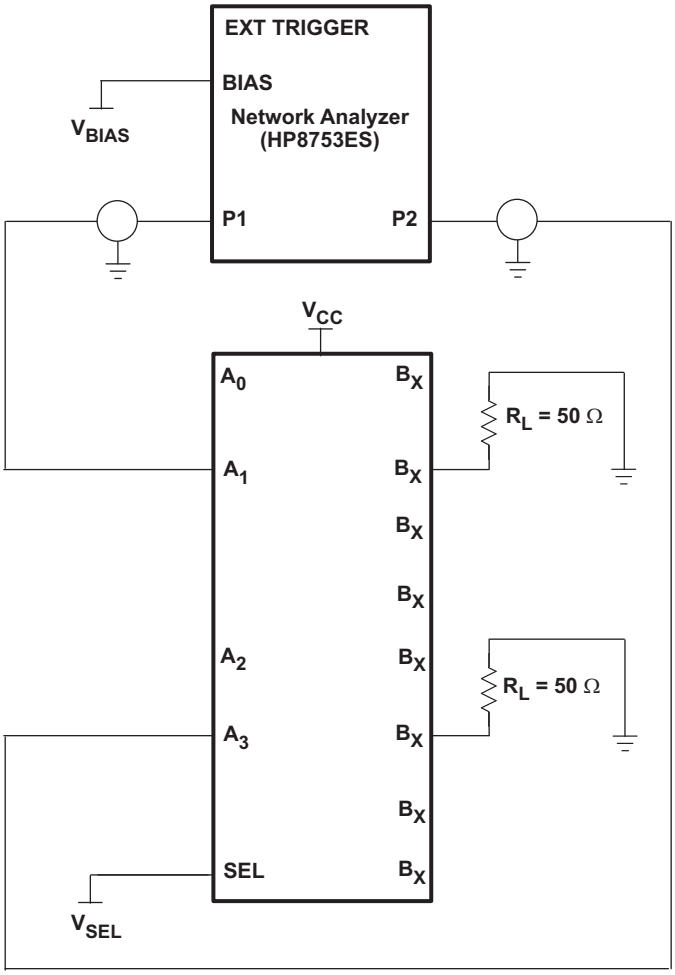
Figure 10. Test Circuit for Frequency Response (BW)

Frequency response is measured at the output of the ON channel. For example, when V_{SEL} = 0 and A_0 is the input, the output is measured at B0. All unused analog I/O ports are left open.

HP8753ES Setup

Average = 4
RBW = 3 kHz
V_{BIAS} = 0.35 V
ST = 2 s
P1 = 0 dBM

PARAMETER MEASUREMENT INFORMATION (continued)



A. C_L includes probe and jig capacitance.
B. A 50 W termination resistor is needed to match the loading of the network analyzer.

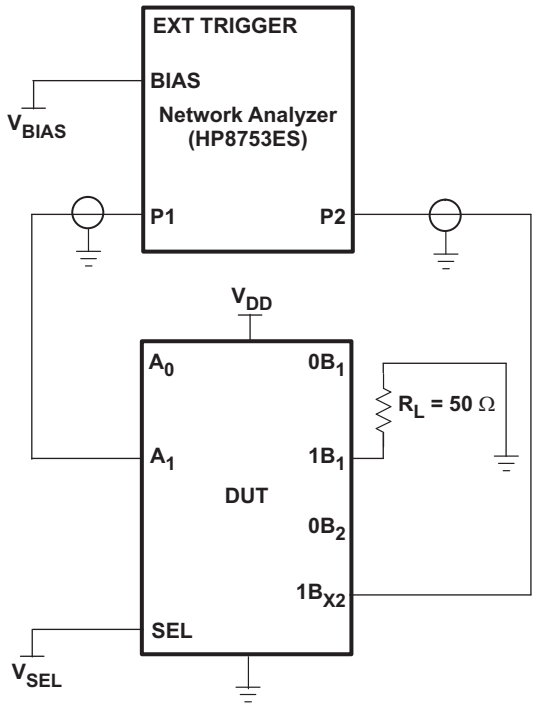
Figure 11. Test Circuit for Crosstalk (X_{TALK})

Crosstalk is measured at the output of the nonadjacent ON channel. For example, when V_{SEL} = 0 and A_1 is the input, the output is measured at A_3. All unused analog input (A) ports are connected to GND, and output (B) ports are left open.

HP8753ES Setup

Average = 4
RBW = 3 kHz
V_{BIAS} = 0.35 V
ST = 2 s
P1 = 0 dBM

PARAMETER MEASUREMENT INFORMATION (continued)



A. C_L includes probe and jig capacitance.
B. A 50 W termination resistor is needed to match the loading of the network analyzer.

Figure 12. Test Circuit for OFF Isolation (O_{IRR})

OFF isolation is measured at the output of the OFF channel. For example, when V_{SEL} = GND and A_1 is the input, the output is measured at $1B_2$. All unused analog input (A) ports are connected to ground, and output (B) ports are left open.

HP8753ES Setup

Average = 4
RBW = 3 kHz
V_{BIAS} = 0.35 V
ST = 2 s
P1 = 0 dBM

REVISION HISTORY

Changes from Original (January 2012) to Revision A	Page
• Changed C_{ON} value in FEATURES from 5.6 pF to 4 pF.	1
• Deleted LEVEL-SHIFTING REQUIREMENT FOR DUAL-MODE DP/HDMI APPLICATION section from document.	4
• Added C_{ON} TYP value to the ELECTRICAL CHARACTERISTICS table.	6

Changes from Revision A (February 2012) to Revision B	Page
• Changed C_{ON} value from 4 pF to 5.6 pF.	1
• Changed C_{ON} TYP value to the ELECTRICAL CHARACTERISTICS table.	6

Changes from Revision B (May 2012) to Revision C	Page
• Updated APPLICATIONS.	1

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TS3DV621RUAR	Active	Production	WQFN (RUA) | 42	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SD621
TS3DV621RUAR.B	Active	Production	WQFN (RUA) | 42	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SD621
TS3DV621RUARG4	Active	Production	WQFN (RUA) | 42	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SD621
TS3DV621RUARG4.B	Active	Production	WQFN (RUA) | 42	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SD621

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

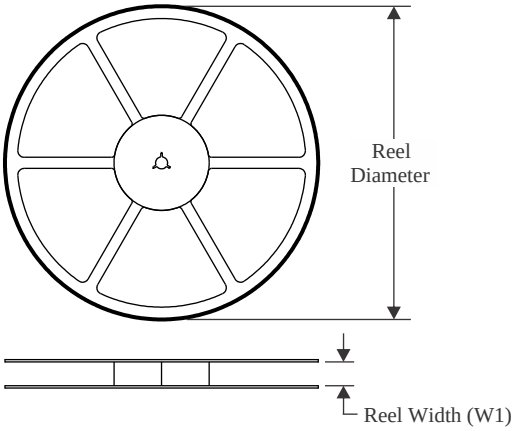
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

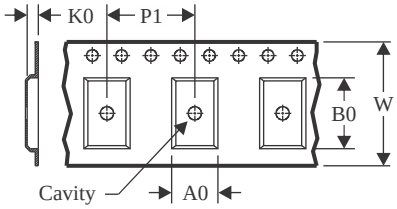
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

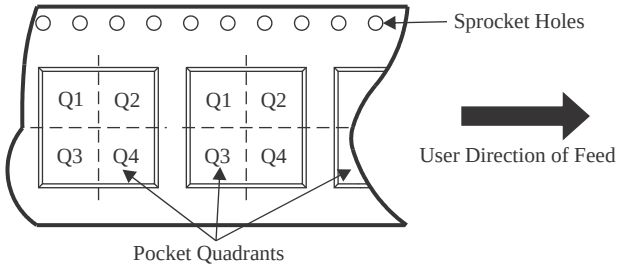


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

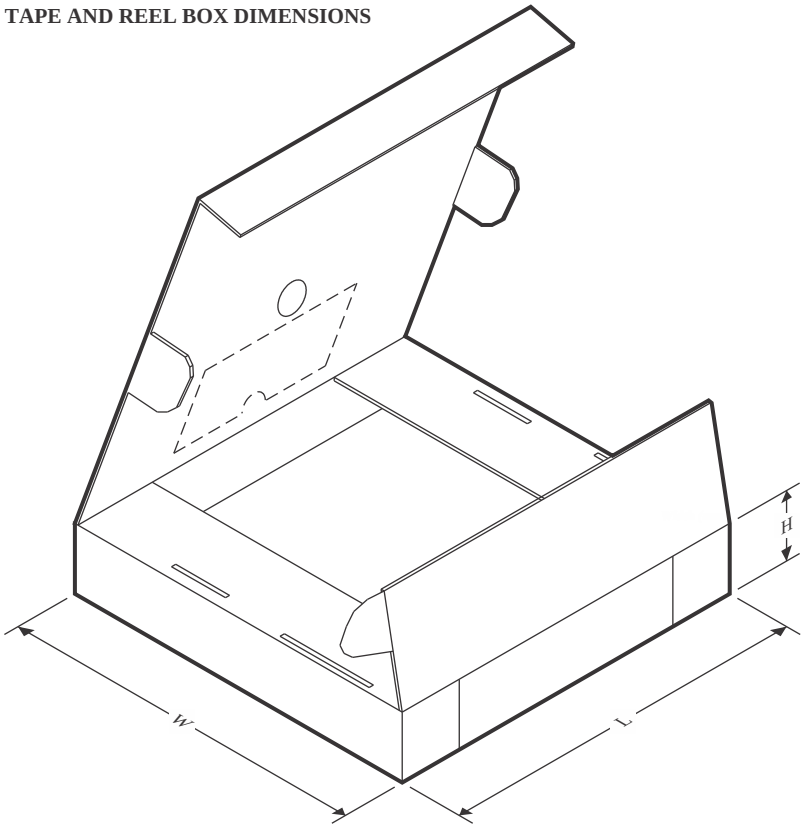
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3DV621RUAR	WQFN	RUA	42	3000	330.0	16.4	3.8	9.3	1.0	8.0	16.0	Q1
TS3DV621RUARG4	WQFN	RUA	42	3000	330.0	16.4	3.8	9.3	1.0	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3DV621RUAR	WQFN	RUA	42	3000	358.0	335.0	35.0
TS3DV621RUARG4	WQFN	RUA	42	3000	358.0	335.0	35.0

GENERIC PACKAGE VIEW

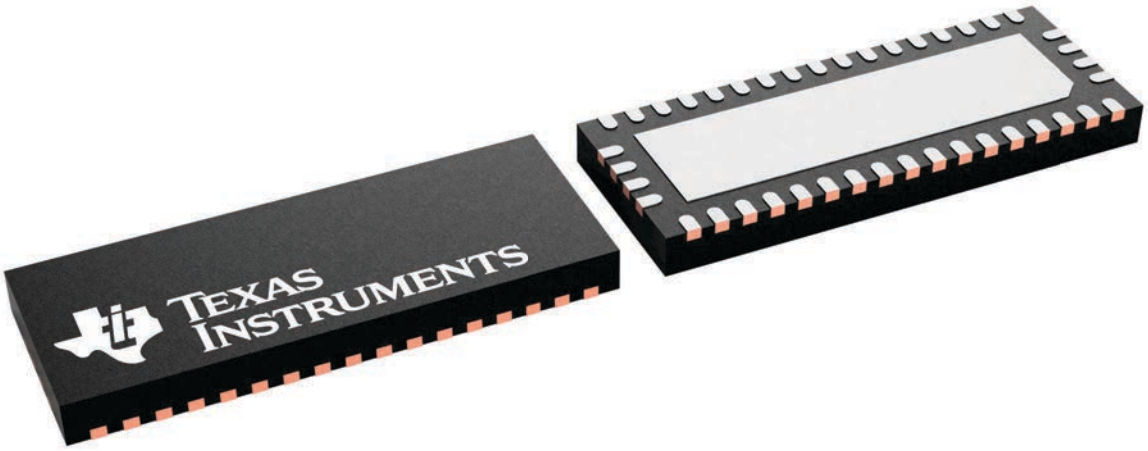
RUA 42

WQFN - 0.8 mm max height

9 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

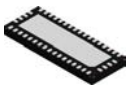
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4226504/A

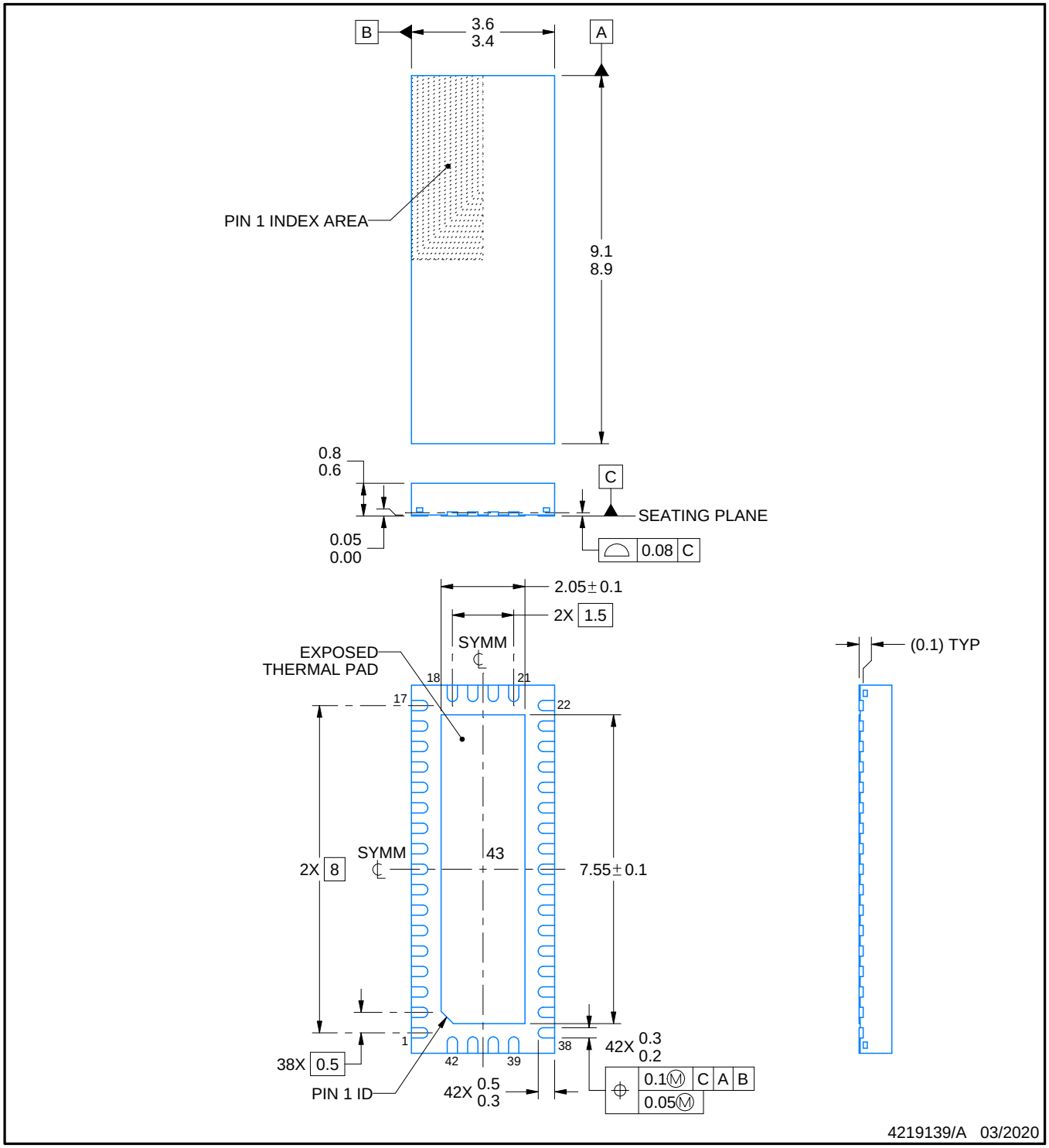
PACKAGE OUTLINE

RUA0042A



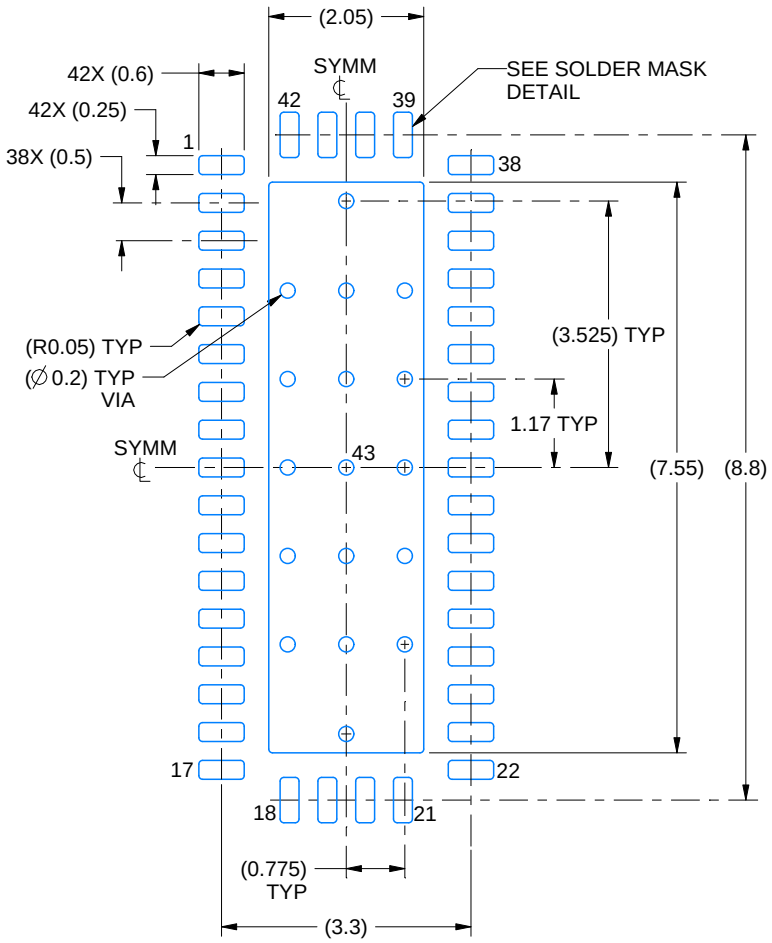
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

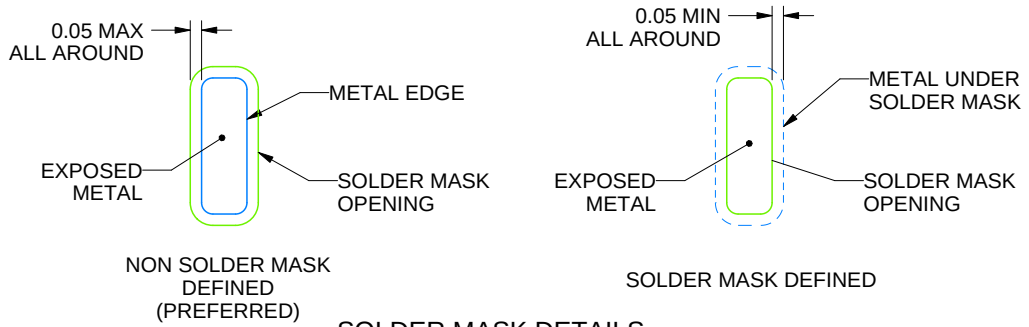


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

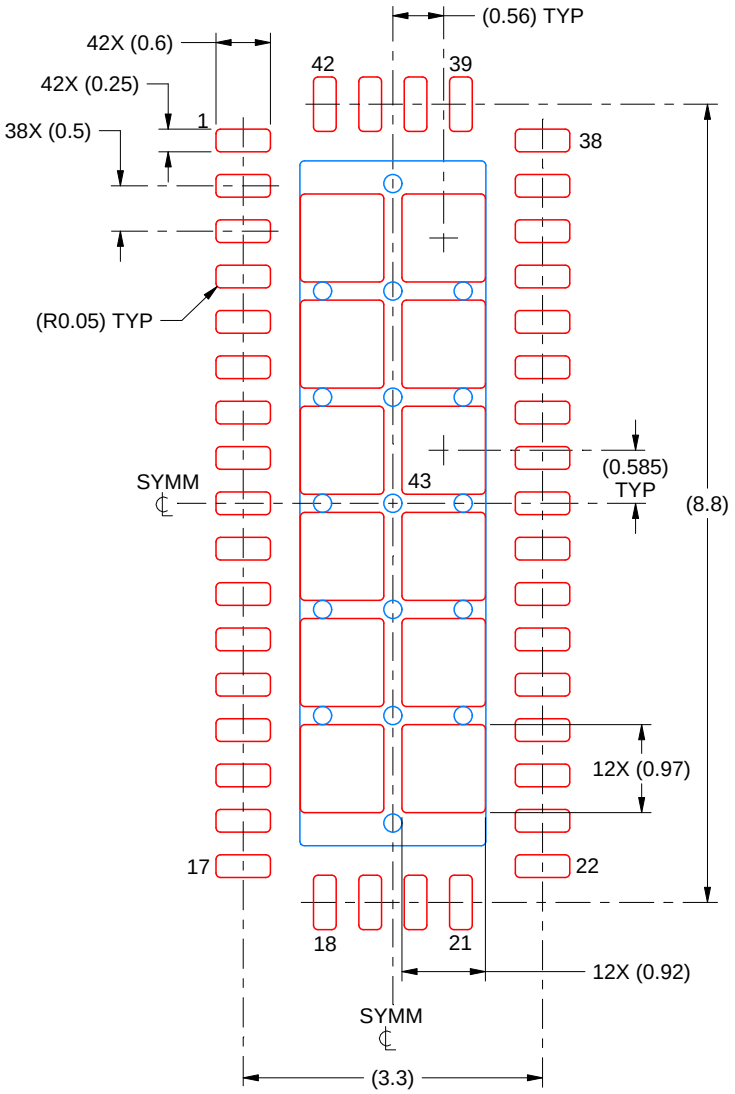
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RUA0042A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 12X

EXPOSED PAD 43
69% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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