TS3USB3031 2-Channel, 1:3, USB 2.0 High-Speed (480Mbps) and Mobile High-Definition Link (MHL) or Mobility Display Port (MyDP) Switch

1 Features

- V_{CC} range: 2.5V to 4.3V
- Mobile high-definition link (MHL) or mobility display port (MyDP) switch:
  - Bandwidth (–3dB): 6.5GHz
  - R_{ON} (typical): 5.5Ω
  - C_{ON} (typical): 1.3pF
- USB switches (2 sets):
  - Bandwidth (–3dB): 6.5GHz
  - R_{ON} (typical): 4.5Ω
  - C_{ON} (typical): 1pF
- Current consumption: 28µA (typical)
- Special features:
  - I_{OFF} protection prevents current leakage in powered-down state (V_{CC} = 0V)
  - 1.8V compatible control inputs (SEL)
  - Overvoltage tolerance (OVT) on all I/O pins up to 5.5V without external components
- ESD performance:
  - 2kV human-body model (A114B, class II)
  - 1kV charged-device model (C101)
- Package:
  - 12-pin VQFN package (1.8mm × 1.8mm, 0.4mm pitch)

2 Applications

- Smart phones
- Tablets
- Mobile phones
- Portable instrumentation
- Digital cameras USB 2.0 MHL

3 Description

The TS3USB3031 device is a 2-channel, 1:3 multiplexer that includes a high-speed Mobile High-Definition Link (MHL), Mobility Display Port (MyDP) switch, and USB 2.0 High-Speed (480Mbps) switches in the same package. These configurations allow the system designer to save board space and eliminate multiple connectors buy using a common USB or Mico-USB connector for MHL/MyDP signals and two sets of USB data. The MHL/MyDP path supports the latest MHL Rev. 3.0 specification.

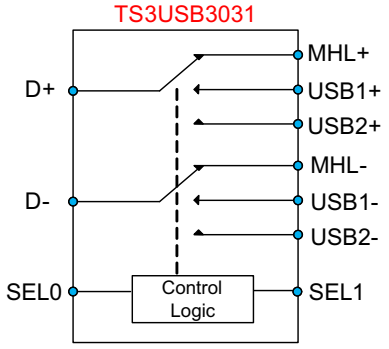
The TS3USB3031 has a V_{CC} range of 2.5V to 4.3V and supports overvoltage tolerance (OVT) feature, which allows the I/O pins to withstand overvoltage conditions (up to 5.5V). The power-off protection feature forces all I/O pins to be in high impedance mode when power is not present, allowing full isolation of the signals lines under such condition without excessive leakage current. The select pins of TS3USB3031 are compatible with 1.8V control voltage, allowing them to be directly interfaced with the General Purpose I/O (GPIO) from a mobile processor with out needing additional voltage level shifting circuitry.

The TS3USB3031 is available in a small 1.8mm × 1.8mm 12-pin VQFN package designed for mobile applications.

Package Information

PART NUMBER	PACKAGE(1)	PACAKGE SIZE(2)
TS3USB3031	RMG (VQFN, 12)	1.8mm × 1.8mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Switch Diagram

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4 Pin Configuration and Functions

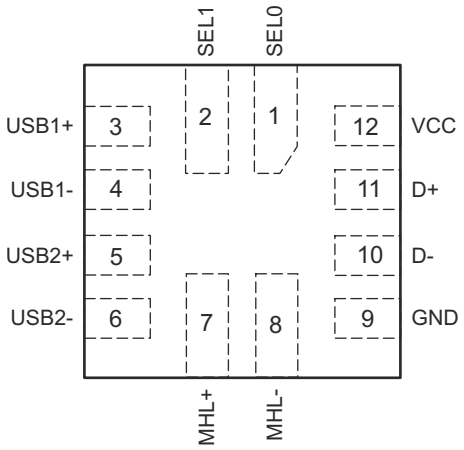


Figure 4-1. RMG Package, 12-Pin VQFN (Top View)

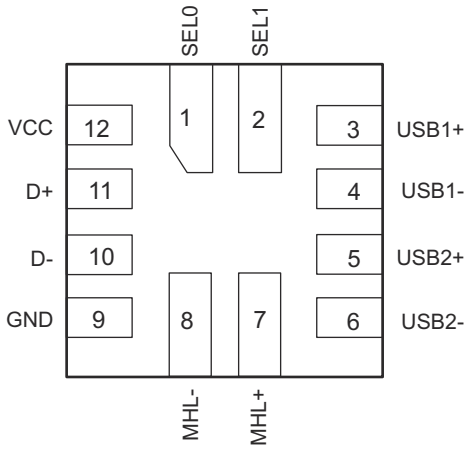


Figure 4-2. RMG Package, 12-Pin VQFN (Bottom View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
SEL0	1	I	Digital control Input
SEL1	2	I	Digital control Input
USB1+	3	I/O	Differential signal path 1
USB1–	4	I/O	Differential signal path 1
USB2+	5	I/O	Differential signal path 2
USB2–	6	I/O	Differential signal path 2
MHL+	7	I/O	Differential signal path 3
MHL–	8	I/O	Differential signal path 3
GND	9	G	Ground
D–	10	I/O	Common Differential signal path
D+	11	I/O	Common Differential signal path
VCC	12	P	Power Supply

(1) G = Ground, I = Input, O = Output, P = Power

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage(3)	–0.3	5.5	V
$V_{I/O}$	Input/Output DC voltage(3)	–0.3	5.5	V
I_K	Input/Output port diode current (VI/O < 0)	–50		mA
V_I	Digital input voltage (SEL0, SEL1)	–0.3	5.5	
I_{IK}	Digital logic input clamp current (VI < 0)(3)	–50		mA
$I_{I/O}$	Continuous switch DC output current (USB and MHL)		60	mA
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to ground, unless otherwise specified.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±1000 V may actually have higher performance.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.5	4.3	V
$V_{I/O\ (USB)}$, $V_{I/O\ (MHL)}$	Analog voltage	0	3.6	V
V_I	Digital input voltage (SEL0, SEL1)	0	V_{CC}	V
$T_{RAMP\ (VCC)}$	Power supply ramp time requirement (VCC)	100	1000	µs/V
$I_{I/O,\ PEAK}$	Peak switch DC output current (1-ms duration pulse at <10% duty cycle)		150	mA
T_A	Operating free-air temperature	–40	85	°C

5.4 Thermal Information

THERMAL METRIC(1)		TS3USB3031 RMG (VQFN) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	160.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	95.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	91.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	91.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

T_A = –40°C to 85°C, typical values are at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MHL SWITCH						
R_{ON}	ON-state resistance	V_{CC} = 2.5 V, $V_{I/O}$ = 1.5V, I_{ON} = –8 mA (see Figure 6-1)		5.5	7	Ω
ΔR_{ON}	ON-state resistance match between + and – paths	V_{CC} = 2.5 V, $V_{I/O}$ = 1.5 V, I_{ON} = –8 mA		0.1		Ω
$R_{ON\ (FLAT)}$	ON-state resistance flatness	V_{CC} = 2.5 V, $V_{I/O}$ = 1.5 V to 3.3 V, I_{ON} = –8 mA		1		Ω
I_{OZ}	OFF leakage current	V_{CC} = 4.3 V, Switch OFF, $V_{MHL+/MHL–}$ = 1.5 V to 3.3 V, $V_{D+/D–}$= 0 V (see Figure 6-2)	–2		2	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0 V, Power off, $V_{MHL+/MHL–}$ = 1.5 V to 3.3 V, $V_{D+/D–}$= NC	–10		10	µA
I_{ON}	ON leakage current	V_{CC} = 4.3 V, Switch ON, $V_{MHL+/MHL–}$ = 1.5 V to 3.3 V, $V_{D+/D–}$= NC	–2		2	µA
USB SWITCH (USB1 and USB2)						
R_{ON}	ON-state resistance	V_{CC} = 2.5 V, $V_{I/O}$ = 0.4 V, I_{ON} = –8 mA (see Figure 6-1)		4.5	6	Ω
ΔR_{ON}	ON-state resistance match between + and – paths	V_{CC} = 2.5 V, $V_{I/O}$ = 0.4 V, I_{ON} = –8 mA		0.1		Ω
$R_{ON\ (FLAT)}$	ON-state resistance flatness	V_{CC} = 2.5 V, $V_{I/O}$ = 0 V to 0.4 V, I_{ON} = –8 mA		1		Ω
I_{OZ}	OFF leakage current	V_{CC} = 4.3 V, Switch OFF, $V_{USB+/USB–}$ = 0 V to 0.4 V, $V_{D+/D–}$= 0 V (see Figure 6-2)	–2		2	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0 V, Switch ON or OFF, $V_{USB+/USB–}$ = 0 V to 0.4 V, $V_{D+/D–}$= NC	–10		10	µA
I_{ON}	ON leakage current	V_{CC} = 4.3 V, Switch ON, $V_{USB+/USB–}$ = 0 V to 0.4 V, $V_{D+/D–}$= NC	–2		2	µA
DIGITAL CONTROL INPUTS (SEL)						
V_{IH}	Input logic high	V_{CC} = 2.5 V to 4.3 V	1.3			V
V_{IL}	Input logic low	V_{CC} = 2.5 V to 4.3 V			0.6	V
I_{IN}	Input leakage current	V_{CC} = 4.3 V, $V_{I/O}$ = 0 V to 3.6 V, V_{IN} = 0 V to 4.3 V	–10		10	µA

5.6 Dynamic Characteristics

T_A = –40°C to 85°C, Typical values are at V_{CC} = 3.3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd}	Propagation delay	R_L = 50 Ω, CL = 5 pF, V_{CC} = 2.5 V to 4.3 V, $V_{I/O(USB)}$ = 0.4 V, $V_{I/O(MHL)}$ = 3.3 V		50		ps
t_{switch}	Switching time between USB/MHL channels in active modes	R_L = 50 Ω, CL = 5 pF, V_{CC} = 2.5 V to 4.3 V, $V_{I/O(USB)}$ = 0.4 V, $V_{I/O(MHL)}$ = 3.3 V			400	ns
t_{ON}	Switch turnon time (from disabled to active mode)	R_L = 50 Ω, CL = 5 pF, V_{CC} = 2.5 V to 4.3 V, $V_{I/O(USB)}$ = 0.4 V, $V_{I/O(MHL)}$ = 3.3 V			100	µs
t_{OFF}	Switch turnoff time (from active to disabled mode)	R_L = 50 Ω, CL = 5 pF, V_{CC} = 2.5 V to 4.3 V, $V_{I/O(USB)}$ = 0.4 V, $V_{I/O(MHL)}$ = 3.3 V			100	µs
$C_{ON(MHL)}$	MHL path, ON capacitance	V_{CC} = 3.3 V, $V_{I/O}$ = 0 V or 3.3 V, f = 240 MHz, Switch ON		1.3		pF
$C_{ON(USB)}$	USB1 and USB2 paths, ON capacitance	V_{CC} = 3.3 V, $V_{I/O}$ = 0 V or 3.3 V, f = 240 MHz, Switch ON		1		pF
$C_{OFF(MHL)}$	MHL path, OFF capacitance	V_{CC} = 3.3 V, $V_{I/O}$ = 0 V or 3.3 V, f = 240 MHz, Switch OFF		1		pF
$C_{OFF(USB)}$	USB1 and USB2 paths, OFF capacitance	V_{CC} = 3.3 V, $V_{I/O}$ = 0 V or 3.3 V, f = 240 MHz, Switch OFF		0.8		pF
C_I	Digital input capacitance	V_{CC} = 3.3 V, V_I = 0 V or 2 V		2.2		pF
$O_{ISO\ (MHL)}$	MHL path, OFF isolation	V_S = –10 dBm, V_{DC_BIAS} = 2.4 V, RT = 50 Ω, f = 240 MHz (see Figure 6-3), Switch OFF		–38		dB
$O_{ISO\ (USB)}$	USB path, OFF isolation	V_S = –10 dBm, V_{DC_BIAS} = 0.2 V RT = 50 Ω, f = 240 MHz (see Figure 6-3), Switch OFF		–38		dB

T_A = –40°C to 85°C, Typical values are at V_{CC} = 3.3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$X_{TALK\ (MHL)}$	MHL channel crosstalk	V_S = –10 dBm, V_{DC_BIAS} = 2.4 V, RT = 50 Ω, f = 240 MHz (see Figure 6-4), Switch ON		–41		dB
$X_{TALK\ (USB)}$	USB channel crosstalk	V_S = –10 dBm, V_{DC_BIAS} = 0.2 V, RT = 50 Ω, f = 240 MHz (see Figure 6-4), Switch ON		–38		dB
$BW_{(MHL)}$	MHL path, –3-dB bandwidth	V_{CC} = 2.5 V to 4.3 V, R_L = 50 Ω (see Figure 6-5), Switch ON		6.5		GHz
$BW_{(USB)}$	USB path, –3-dB bandwidth	V_{CC} = 2.5 V to 4.3 V, R_L = 50Ω (See Figure 6-5), Switch ON		6.5		GHz
SUPPLY						
V_{CC}	Power supply voltage		2.5		4.3	V
I_{CC}	Positive supply current	V_{CC} = 4.3 V, V_{IN} = V_{CC} or GND, $V_{I/O}$ = 0 V, Switch ON or OFF		28	40	µA

5.7 Typical Characteristics

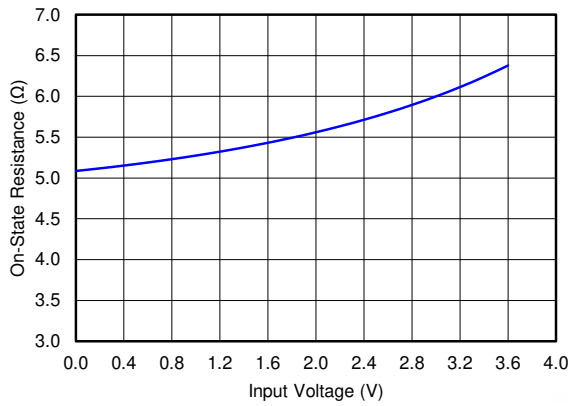


Figure 5-1. ON-Resistance vs $V_{I/O}$ for MHL Switch

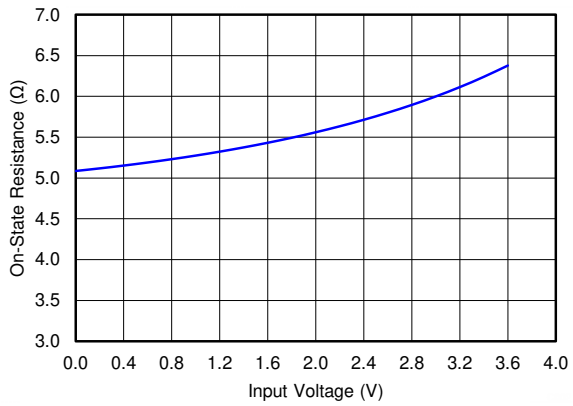


Figure 5-2. ON-Resistance vs $V_{I/O}$ for USB Switch

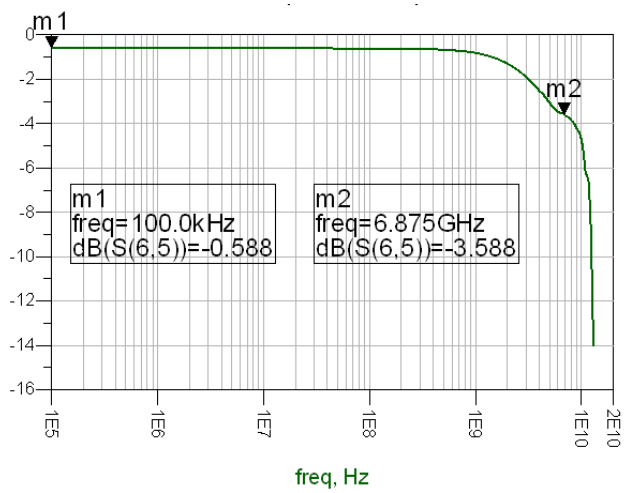


Figure 5-3. Bandwidth for MHL Switch

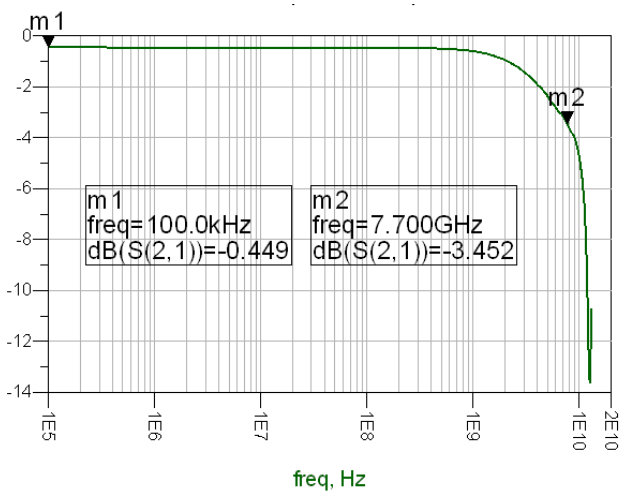


Figure 5-4. Bandwidth for USB Switch

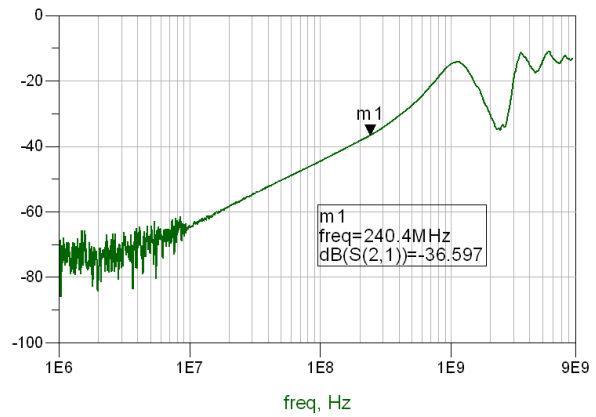


Figure 5-5. OFF Isolation vs Frequency for MHL Path

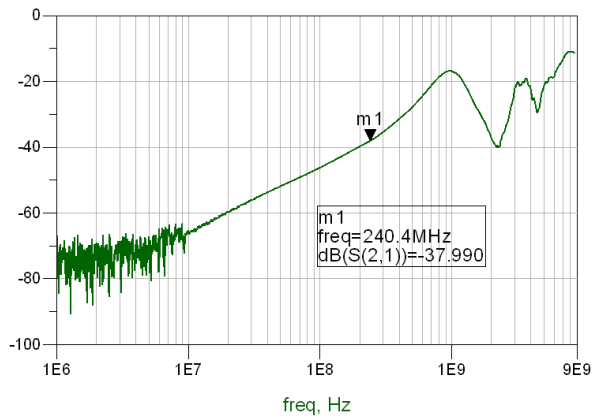


Figure 5-6. OFF Isolation vs Frequency for USB Path

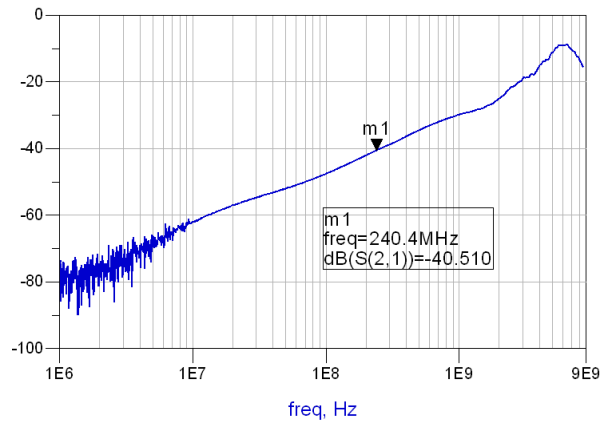


Figure 5-7. Cross Talk vs Frequency for MHL Path

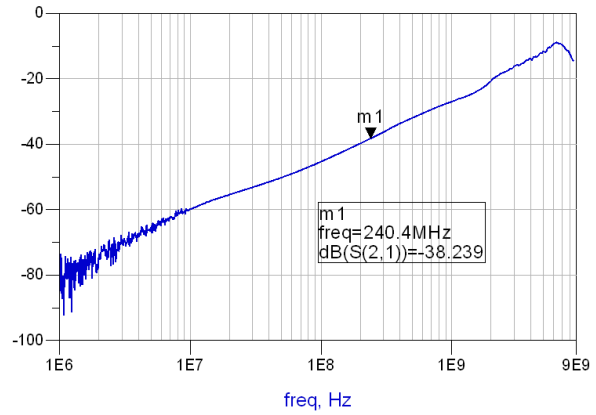


Figure 5-8. Cross Talk vs Frequency for USB Path

Parameter Measurement Information

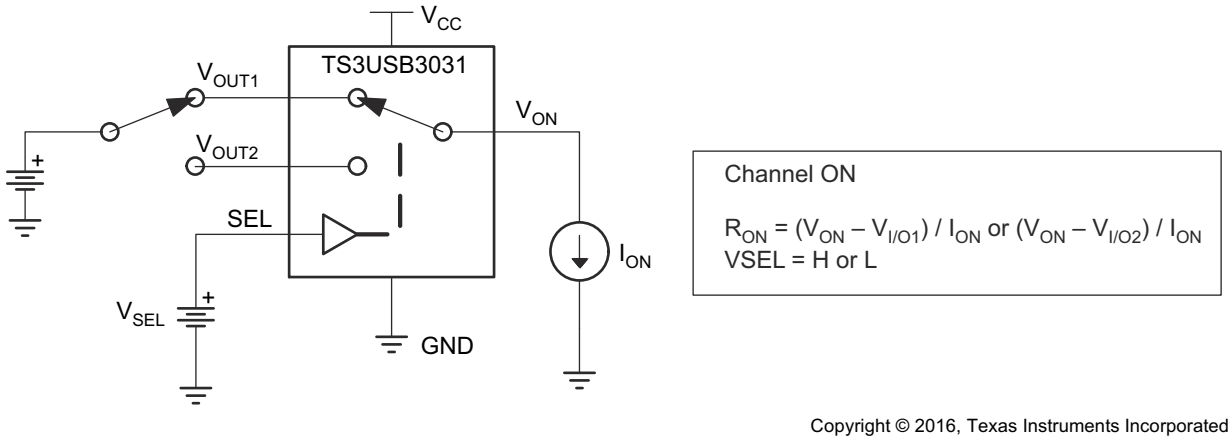


Figure 6-1. ON-State Resistance (R_{ON})

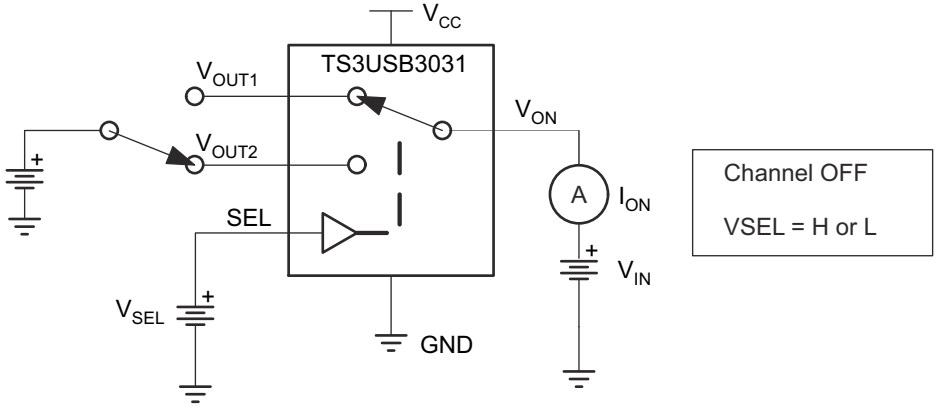


Figure 6-2. OFF Leakage Current (I_{OZ})

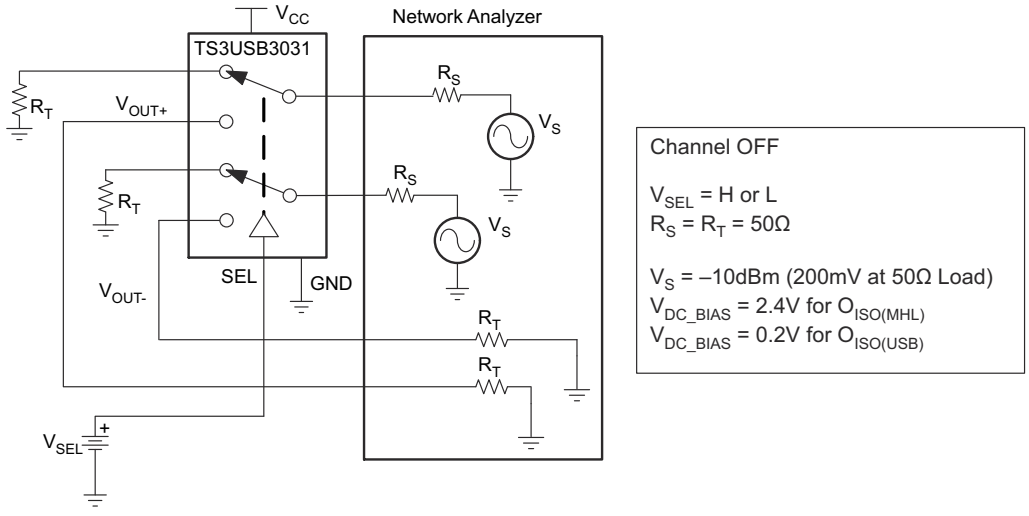


Figure 6-3. Differential Off-Isolation (O_{ISO})

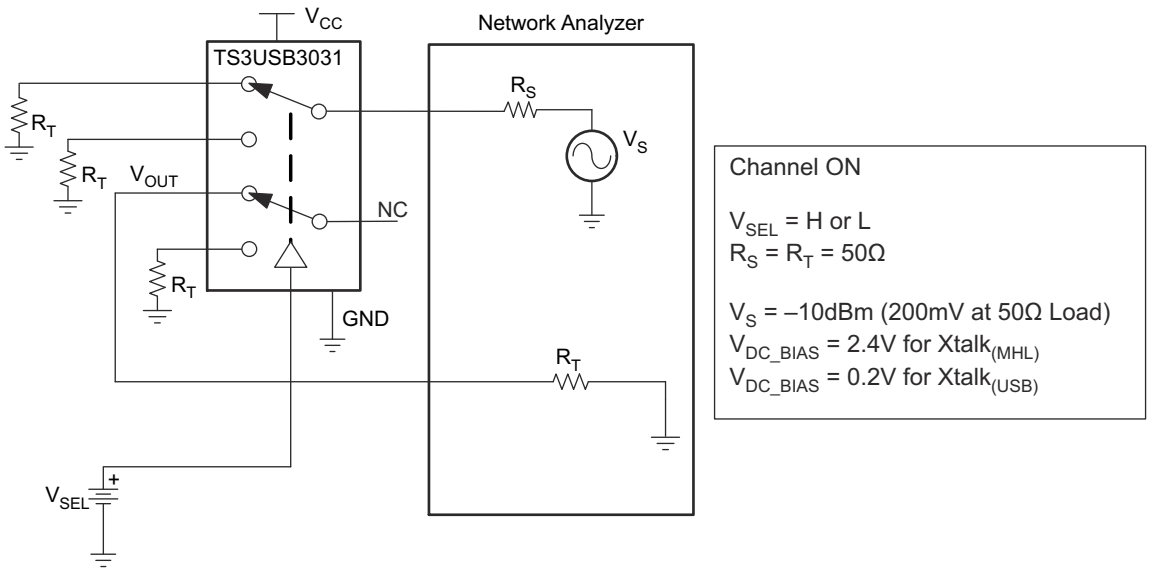


Figure 6-4. Crosstalk (Xtalk)

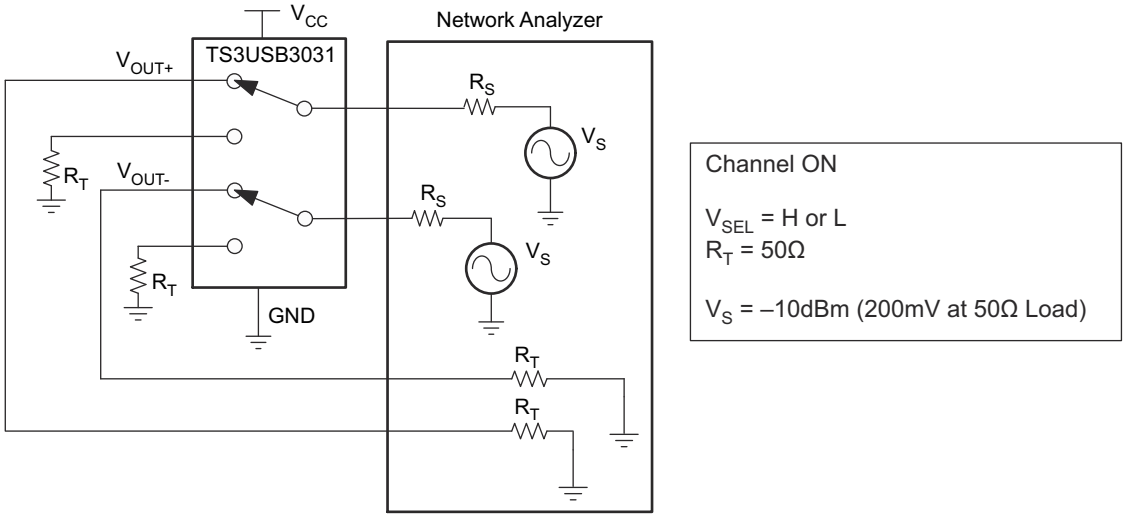


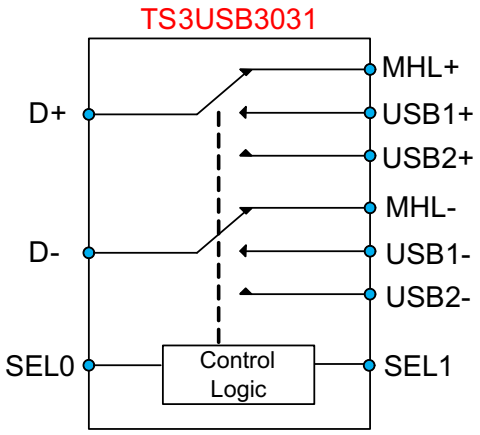
Figure 6-5. Differential Bandwidth (BW)

6 Detailed Description

6.1 Overview

The TS3USB3031 device is a 2-channel, 1:3 multiplexer that includes a high-speed Mobile High-Definition Link (MHL) or Mobility Display Port (MyDP) switch and USB 2.0 High-Speed (480 Mbps) switches in the same package. This device is used in many high-speed differential 1:3 mux applications.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 I_{OFF} Protection

I_{OFF} protection prevents current leakage through the device when V_{cc} = 0 V This allows signals to be present on the D± and USB/MHL± pins before the device is powered up without damaging the device or system.

6.3.2 1.8-V Compatible Logic

The TS3USB3031 device supports 1.8-V logic irrespective to the supply voltage applied to the IC.

6.3.3 Overvoltage Tolerant (OVT)

The D± and USB/MHL± pins of the device can support signals up to 5.5 V without damaging the device. This protects the TS3USB3031 in case the VBUS pin of the USB connector is shorted to the signal path without additional components added.

6.4 Device Functional Modes

Table 6-1 lists the functional modes of the TS3USB3031.

Table 6-1. Function Table

SEL1	SEL0	SWITCH STATUS
Low	Low	D+/D– connected to USB1+/USB1–
Low	High	D+/D– connected to USB2+/USB2–
High	Low	D+/D– connected to MHL+/MHL–
High	High	USB and MHL switches in High-Z

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TS3USB3031 is a passive, bidirectional, 2-channel 1:3 switch that can be used in many high speed 1:3 switching applications. This device was designed originally for USB 2.0 and Mobile High-Definition Link applications but can be used for general signal switching applications such as I^2C, UART, LVDS, and so forth.

7.2 Typical Application

Figure 7-1 represents a typical application of the TS3USB3031 MHL switch. The TS3USB3031 is used to switch signals between the two sets of USB paths, which go to either the baseband or application processor, and the MHL path, which goes to the HDMI to MHL bridge. The TS3USB3031 has internal 6-MΩ pulldown resistors on SEL0 and SEL1. The pulldown on SEL0 and SEL1 ensure the USB1 channel is selected by default. The TS5A3157 is a separate SPDT switch that is used to switch between the MHL CBUS and the USB ID line that is required for USB OTG (USB On-The-Go) application.

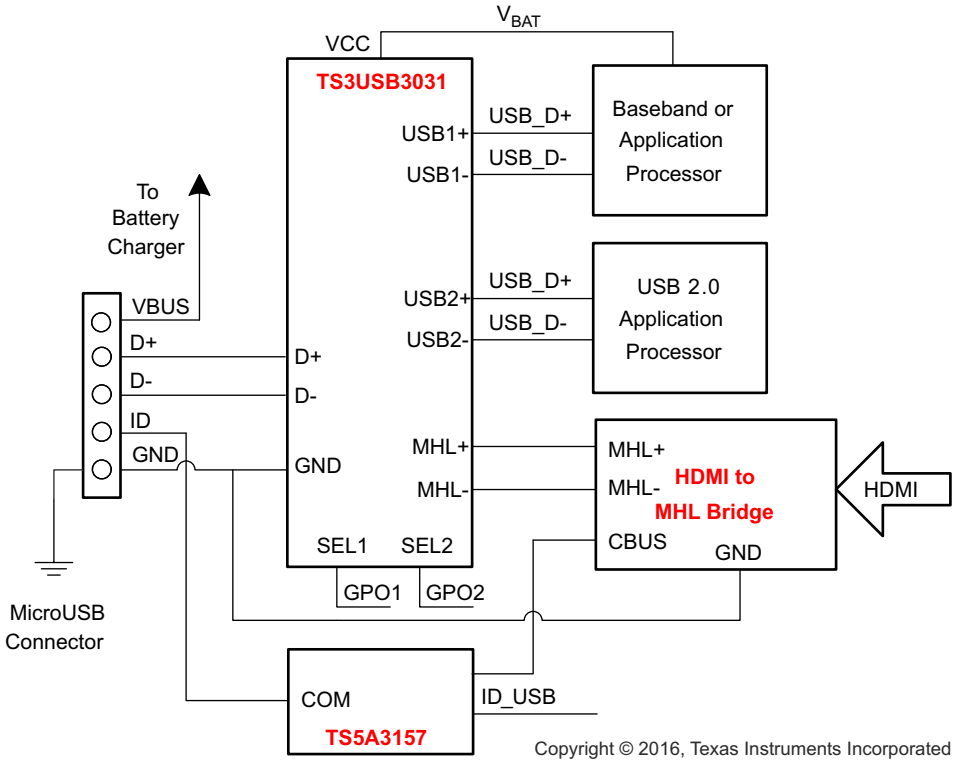


Figure 7-1. Typical TS3USB3031 Application

7.2.1 Design Requirements

Design requirements of the MHL and USB 1.0,1.1, and 2.0 standards must be followed.

The TS3USB3031 has internal 6-MΩ pulldown resistors on SEL0 and SEL1 so no external resistors are required on the logic pins. The pulldown on SEL0 and SEL1 ensure the USB1 channel is selected by default.

The TS5A3157 is a separate SPDT switch that is used to switch between the CBUS of the MHL and the USB ID line that is required for USB OTG (USB On-The-Go) application.

7.2.2 Detailed Design Procedure

The TS3USB3031 can be properly operated without any external components. However, TI recommends that unused signal I/O pins must be connected to ground through a 50-Ω resistor to prevent signal reflections back into the device.

7.2.3 Application Curves

7.2.3.1 MHL Eye Pattern

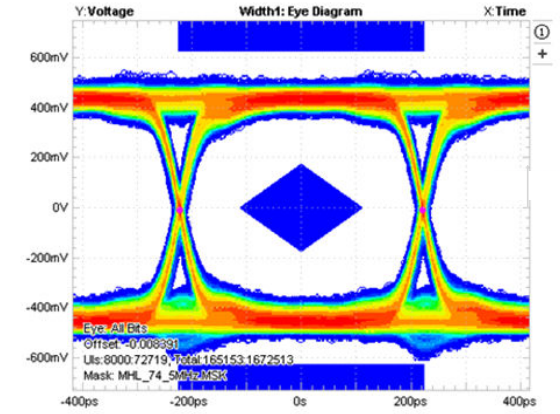


Figure 7-2. Eye Pattern Error Histogram: 2.25 Gbps With No Device

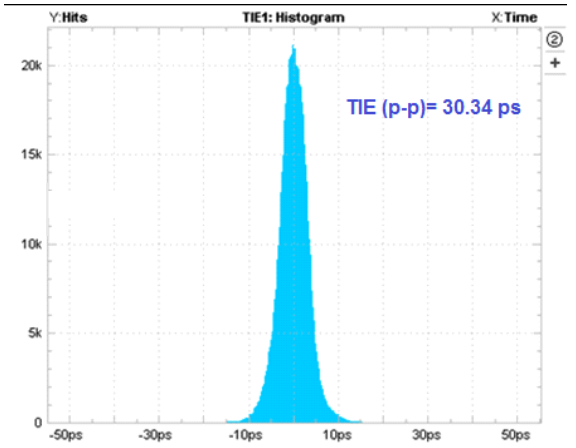


Figure 7-3. Time Interval Error Histogram: 2.25 Gbps With No Device

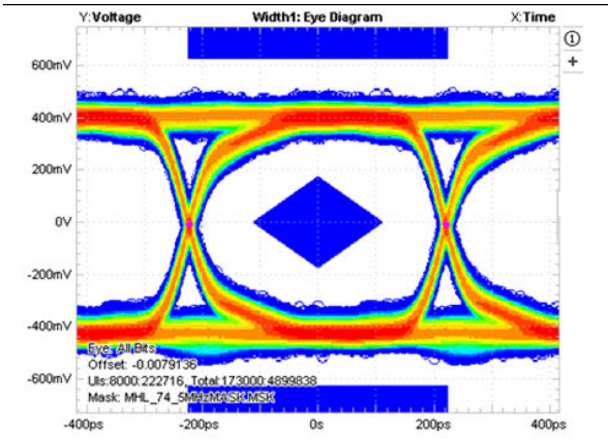


Figure 7-4. Eye Pattern Error Histogram: 2.25 Gbps With TS3USB3031 (Added Jitter = 5.04 ps)

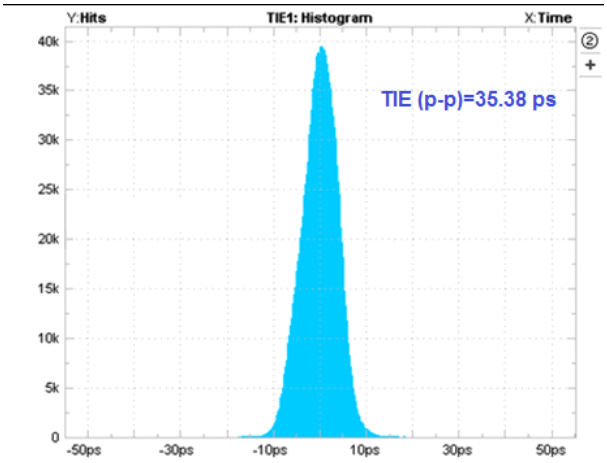


Figure 7-5. Time Interval Error Histogram: 2.25 Gbps With TS3USB3031 (Added Jitter = 5.04 ps)

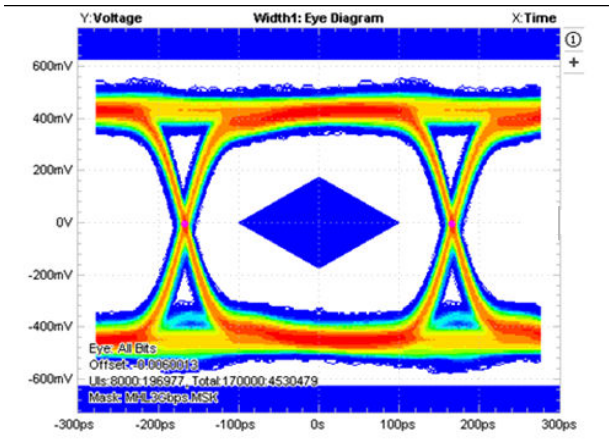


Figure 7-6. Eye Pattern Error Histogram: 3.0 Gbps With No Device

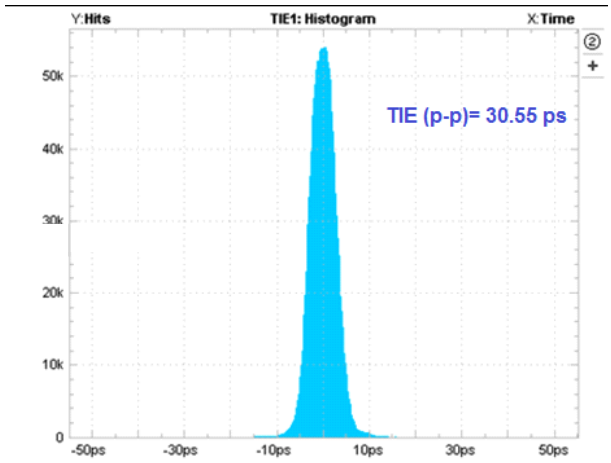


Figure 7-7. Time Interval Error Histogram: 3.0 Gbps With No Device

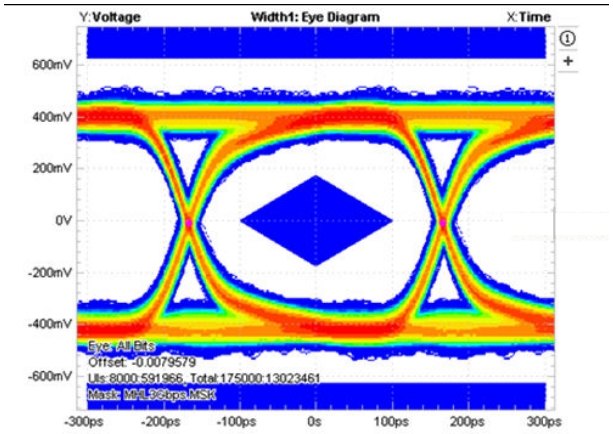


Figure 7-8. Eye Pattern Error Histogram: 3.0 Gbps With TS3USB3031 (Added Jitter = 2.57 ps)

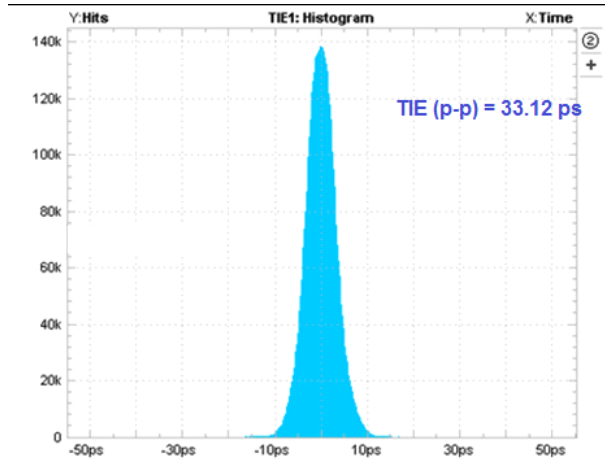


Figure 7-9. Time Interval Error Histogram: 3.0 Gbps With TS3USB3031 (Added Jitter = 2.57 ps)

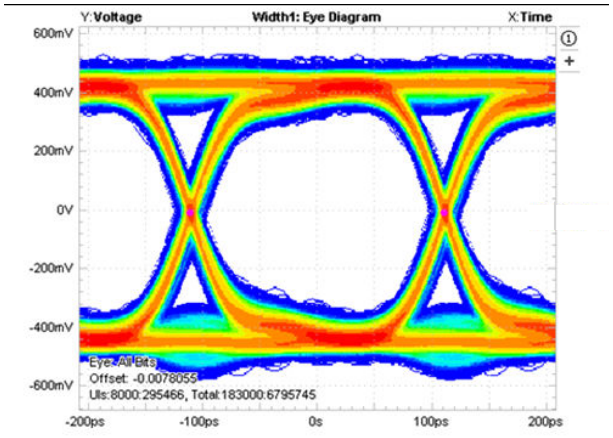


Figure 7-10. Eye Pattern Error Histogram: 4.5 Gbps With No Device

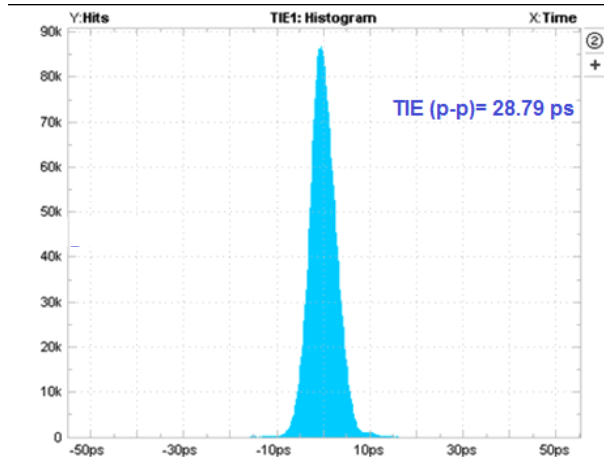


Figure 7-11. Time Interval Error Histogram: 4.5 Gbps With No Device

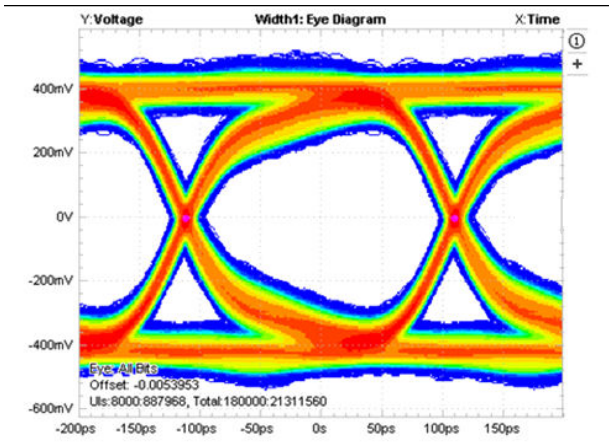


Figure 7-12. Eye Pattern Error Histogram: 4.5 Gbps With TS3USB3031 (Added Jitter = 1.13 ps)

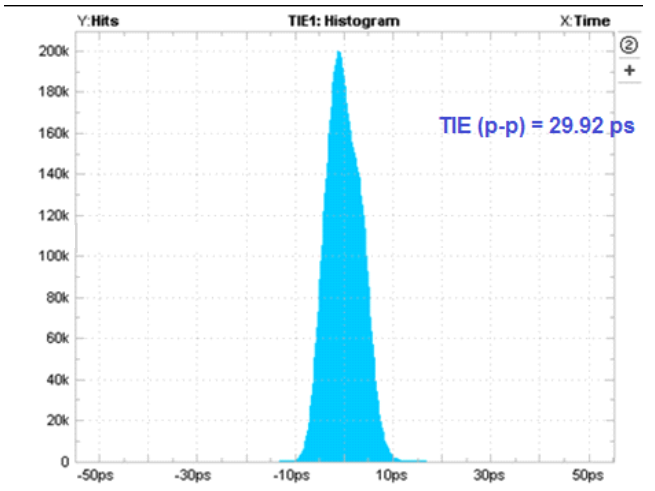


Figure 7-13. Time Interval Error Histogram: 4.5 Gbps With TS3USB3031 (Added Jitter = 1.13 ps)

7.2.3.2 USB EYE Pattern

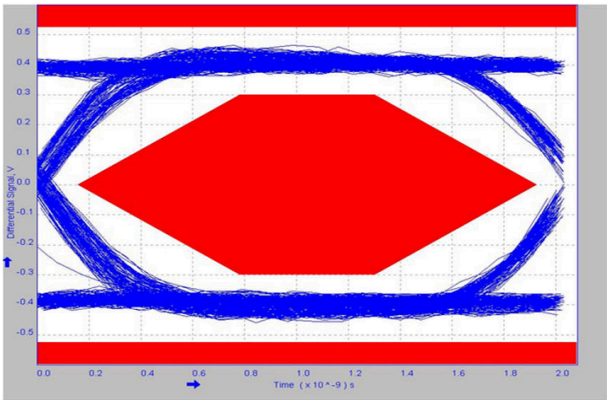


Figure 7-14. 480-Mbps USB 2.0 Eye Pattern With No Device

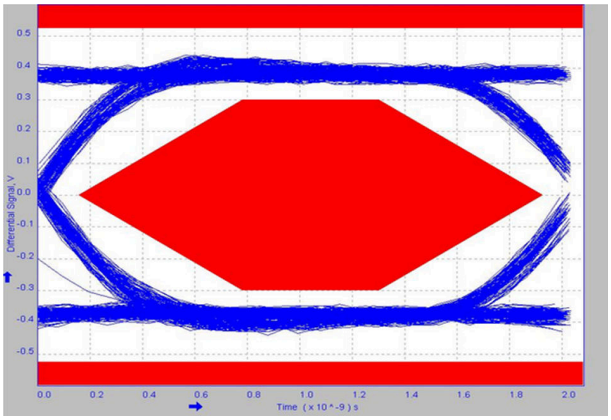


Figure 7-15. 480-Mbps USB 2.0 Eye Pattern for USB Switch

7.3 Power Supply Recommendations

Power to the device is supplied through the V_{CC} pin. TI recommends placing a bypass capacitor as close as possible to the supply pin V_{CC} to help smooth out lower frequency noise to provide better load regulation across the frequency spectrum.

This device does not require any power sequencing with respect to other devices in the system due to the power off isolation feature. The power off isolation feature allows signals to be present on the signal path pins before the device is powered up without damaging the device.

7.4 Layout

7.4.1 Layout Guidelines

Place supply bypass capacitors as close to the V_{CC} pin as possible and avoid placing the bypass caps near the D+ and D– traces.

The high-speed D+ and D– traces must always be of equal length and must be no more than four inches; otherwise, the eye diagram performance may degrade. A high-speed USB connection is made through a shielded, twisted pair cable with a differential characteristic impedance. In the layout, the impedance of D+ and D– traces must match the cable characteristic differential impedance for optimal performance.

Route the high-speed USB signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around the via to minimize the capacitance. Each via introduces discontinuities in the transmission line of the signal and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.

When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities.

Do not route USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices, or ICs that use or duplicate clock signals.

Avoid stubs on the high-speed USB signals because the stubs cause signal reflections. If a stub is unavoidable, then the stub must be less than 200 mm.

Route all high-speed USB signal traces over continuous GND planes, with no interruptions.

Avoid crossing over anti-etch, commonly found with plane splits.

Due to high frequencies associated with the USB, a printed circuit board with at least four layers is recommended: two signal layers separated by a ground layer and a power layer. The majority of signal traces must run on a single layer, preferably top layer. Immediately next to this layer must be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies. For more information on layout guidelines, see *High Speed Layout Guidelines* and *USB 2.0 Board Design and Layout Guidelines*.

7.4.2 Layout Example

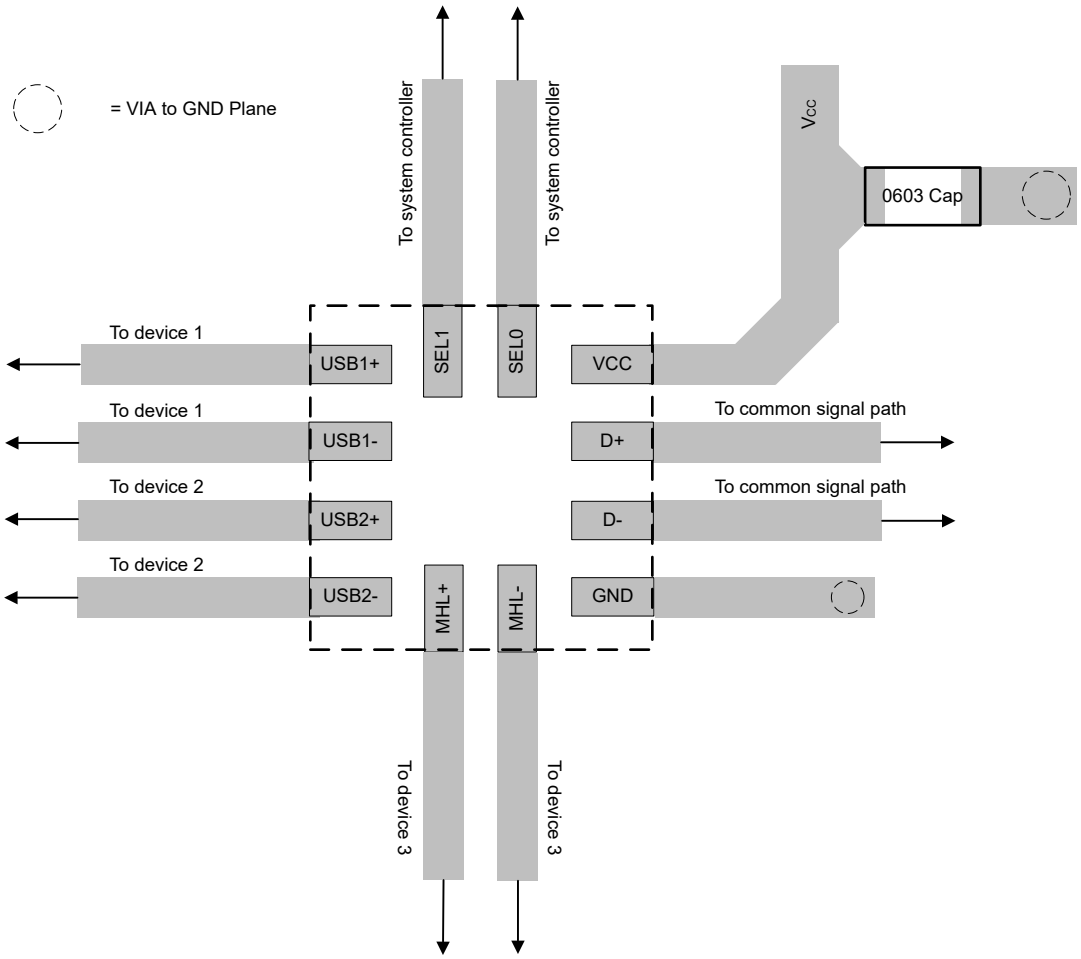


Figure 7-16. Layout Recommendation

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *High Speed Layout Guidelines*
- Texas Instruments, *USB 2.0 Board Design and Layout Guidelines*

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

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8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (March 2017) to Revision D (August 2024)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Changed pitch dimension from 0.5mm to 0.4mm	1
• Changed the *480-Mbps USB 2.0 Eye Pattern for USB Switch* graph.	14
• Changed SEL2 pin name to SEL0 in the *Layout Example* image to keep consistency across the data sheet	16

Changes from Revision B (December 2016) to Revision C (March 2017)	Page
• Changed Feature From: 1.8-V Compatible Control Inputs (SEL, $\overline{OE}$) To: 1.8-V Compatible Control Inputs (SEL)	1
• Changed second pin D+ To: D- in the *Switch Diagram*	1
• Changed DIGITAL CONTROL INPUTS (SEL, $\overline{OE}$) To: DIGITAL CONTROL INPUTS (SEL) in the *Electrical Characteristics* table	5
• Changed second pin D+ To: D- in the *Functional Block Diagram*	10

- Deleted sentence: "The internal pulldown resistor on OE enables the switch when power is applied to VCC" from the *Design Requirements* section..... 12

Changes from Revision A (September 2013) to Revision B (December 2016) **Page**

- Added *Applications* list, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section..... 1
- Deleted *Ordering Information* table; see *Package Option Addendum* at the end of the data sheet..... 1
- Moved Peak switch DC output current parameter From: *Absolute Maximum Ratings* To: *Recommended Operating Conditions* 4

Changes from Revision * (June 2013) to Revision A (September 2013) **Page**

- Added TYPICAL CHARACTERISTICS section..... 6

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3USB3031RMGR	ACTIVE	WQFN	RMG	12	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DY	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

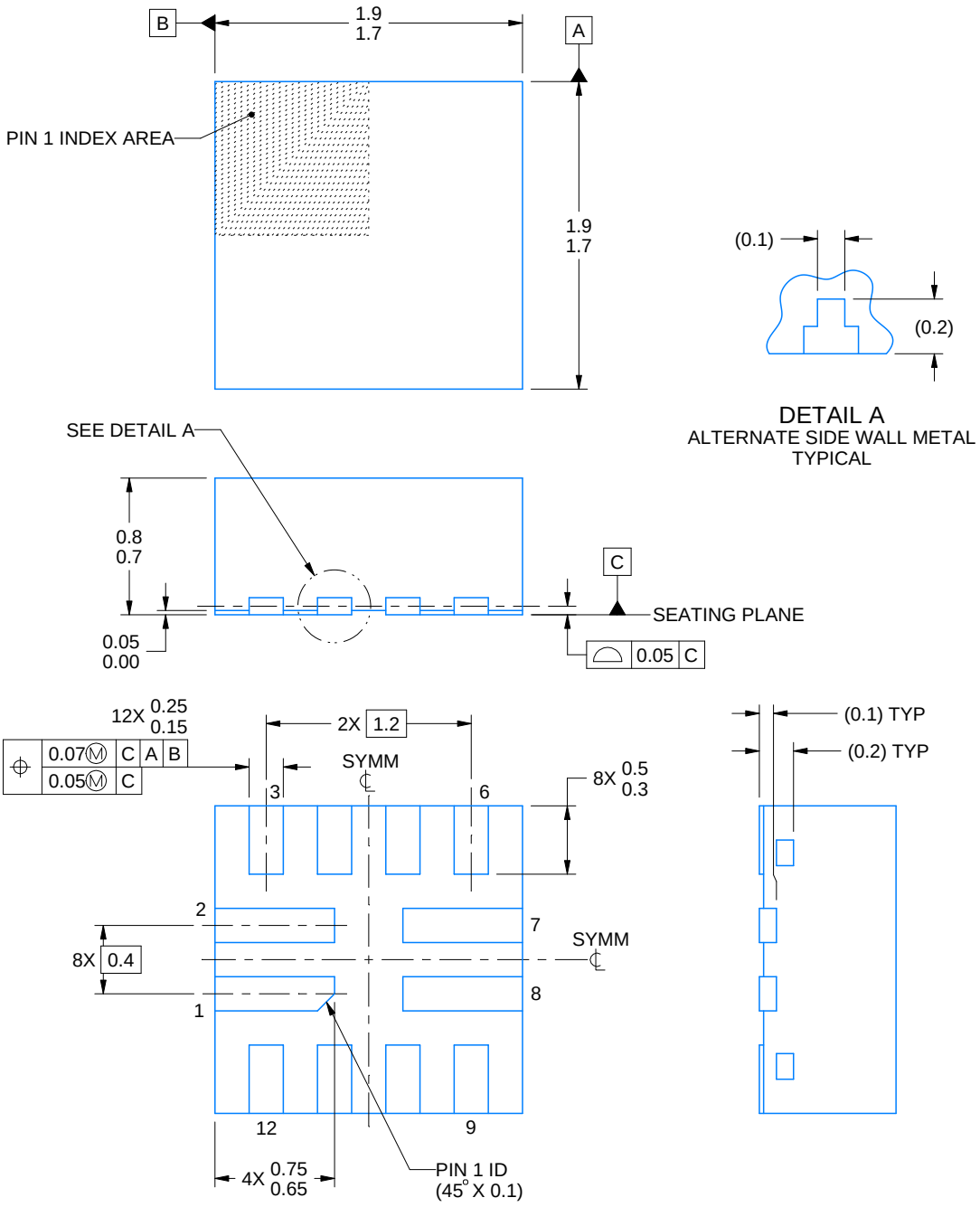
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

RMG0012A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



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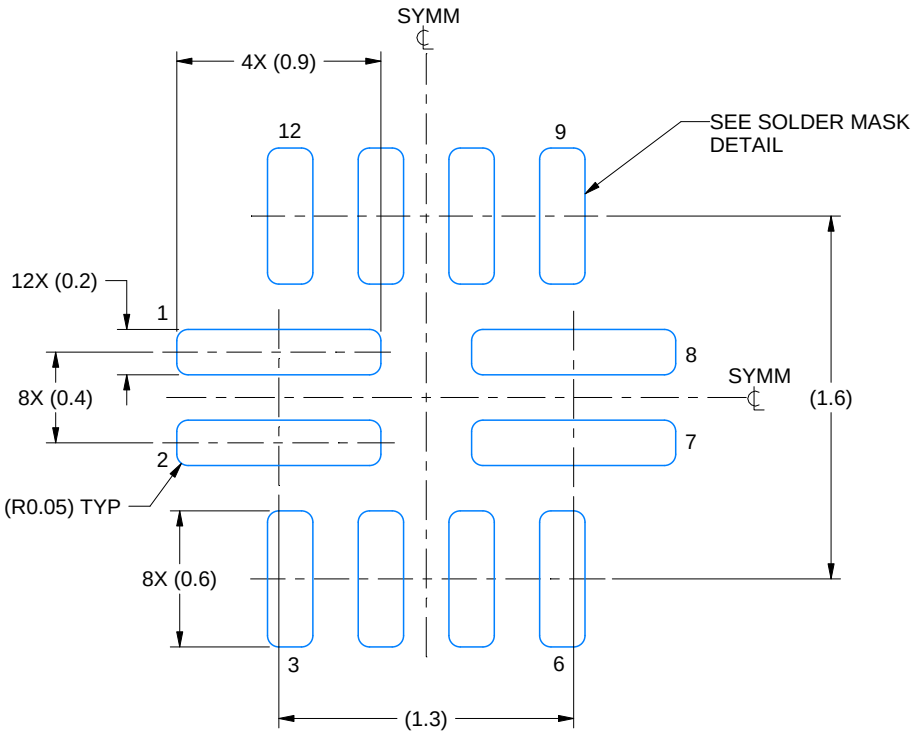
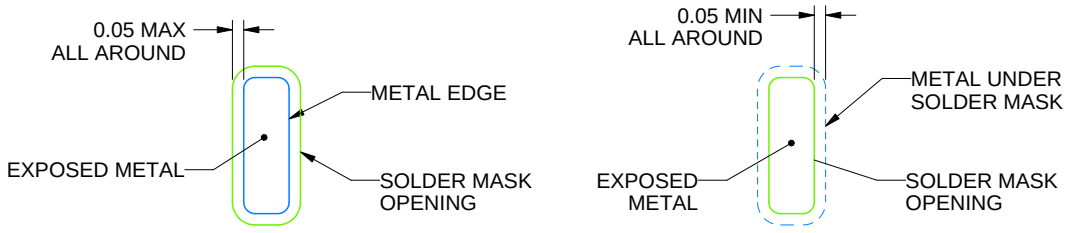
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X



NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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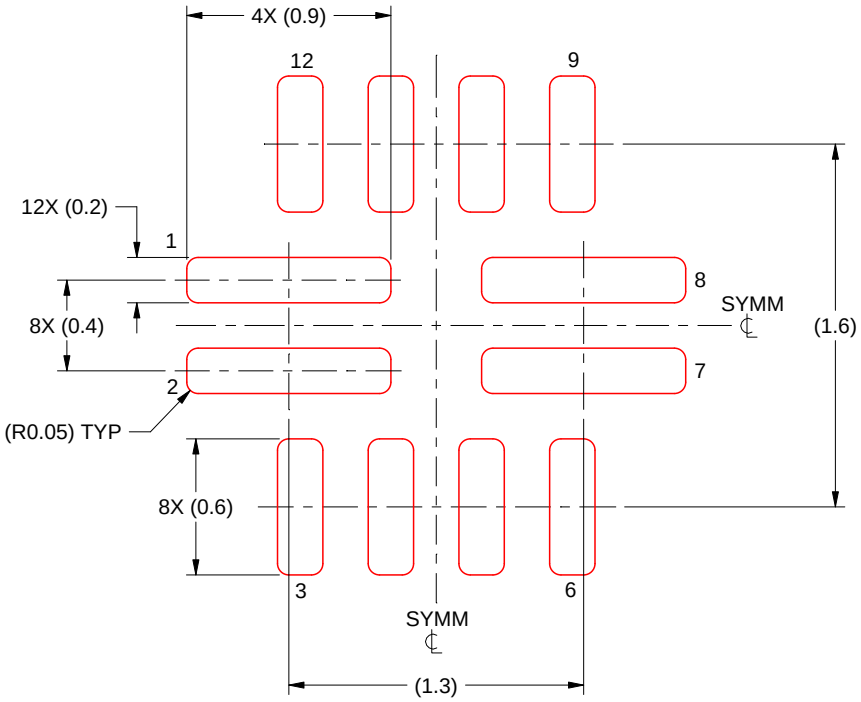
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 30X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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