TS5A3157 10Ω SPDT Analog Switch

1 Features

- Low ON-State Resistance (10Ω)
- Control Inputs are 5V Tolerant
- Low Charge Injection
- Excellent ON-State Resistance Matching
- Low Total Harmonic Distortion (THD)
- 1.65V to 5.5V Single-Supply Operation
- Latch-up Performance Exceeds 100mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22:
  - 2000V Human-Body Model (A114-B, Class II)
  - 1000V Charged-Device Model (C101)

2 Applications

- Sample-and-Hold Circuits
- Battery-Powered Equipment
- Audio and video signal routing
- Communication Circuits

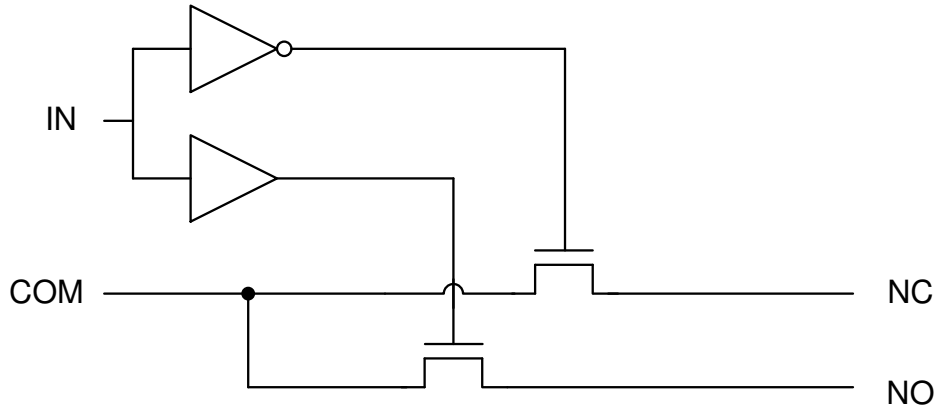
3 Description

The TS5A3157 device is a single-pole double-throw (SPDT) analog switch that is designed to operate from 1.65V to 5.5V. This device handles both digital and analog signals. Signals up to V_+ can be transmitted in either direction.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TS5A3157	DBV (SOT-23, 6)	2.9mm × 2.8mm
	DCK (SC70, 6)	2mm × 1.5mm
	YZP (DSBGA, 6)	1.75mm × 1.25mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Functional Block Diagram

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

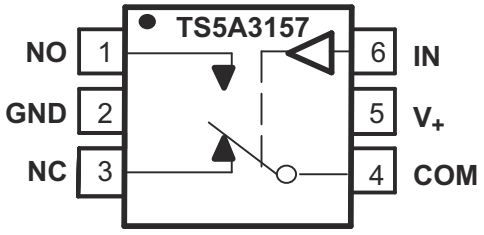

Figure 4-1. DBV and DCK Packages, 6-Pin SOT-23 and SC-70 (Top View)

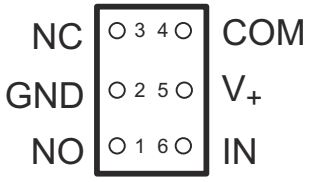

Figure 4-2. YZP Package, 6-Pin DSBGA (Bottom View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
1	NO	I/O	Normally open switch port
2	GND	—	Ground
3	NC	I/O	Normally closed switch port
4	COM	I/O	Common switch port
5	V+	—	Power supply
6	IN	I	Switch select. High = COM connected to NO; Low = COM connected to NC.

(1) I = input, O = output

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(2) (1)

		MIN	MAX	UNIT
V_+	(YZP Only) Supply voltage(3)	-0.5	6.5	V
V_+	Supply voltage(3)	-0.5	6	V
V_{NO} V_{NC} V_{COM}	Analog voltage(3) (4) (5)	-0.5	V_+ + 0.5V	V
I_K	Analog port diode current V_{NO}, V_{NC}, V_{COM} < 0 or V_{NO}, V_{NC}, V_{COM} > V_+	-50	50	mA
I_{NO} I_{NC} I_{COM}	On-state switch current V_{NO}, V_{NC}, V_{COM} = 0 to V_+	-50	50	mA
V_I	Digital input voltage(3) (4)	-0.5	6	V
I_{IK}	Digital input clamp current V_+< 0	-50		mA
I_+	Continuous current through V_+	-100	100	mA
I_{GND}	Continuous current through GND	-100	100	mA
T_{stg}	Storage temperature	-65	150	C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to ground unless otherwise specified.
(4) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(5) This value is limited to 5.5 V maximum.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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5.3 Thermal Information

THERMAL METRIC(1)		TS5A3157			UNIT
		DBV (SOT-23)	DCK (SC70)	YZP (DSBGA)	
		6 PINS	6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	258.2	286.4	132	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	182.8	224.6	n/a	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	142.8	143.7	n/a	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	118.4	124.5	n/a	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	142.2	142.8	n/a	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	NOM	MAX	UNIT
$V_{I/O}$	Switch input or output voltage (Max of V_{CC})		0		V_+	V
V_+	Supply voltage		1.65		5.5	V
V_I	Control input voltage		0		5.5	V
T_A	Operating Temperature		-40		85	°C

(1) All unused inputs of the device must be held at VCC or GND to ensure proper device operation. See the TI application report, Implications of Slow or Floating CMOS Inputs (SCBA004)

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5.5 Electrical Characteristics

T_A = -40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS				MIN	TYP	MAX	UNIT
TS5A3157									
		V_+ V	**$V_{I/O}$ V**	**$I_{C\ OM}$ mA**	**T_A**				
r_{ON} (YZP Only)	ON-state switch resistance	1.65 V	0 ≤ (V_{NO} or V_{NC}) ≤ V_+	$I_{C\ OM}$ = -4 mA	25°C		140	160	Ω
					Full			160	
		2.3 V		$I_{C\ OM}$ = -8 mA	25°C		35	45	
					Full			50	
		3 V		$I_{C\ OM}$ = -24 mA	25°C		12	20	
					Full			20	
		4.5 V		$I_{C\ OM}$ = -30 mA	25°C		5.5	10	
					Full			12	
r_{ON}	ON-state switch resistance	1.65 V	0 ≤ (V_{NO} or V_{NC}) ≤ V_+	$I_{C\ OM}$ = -4 mA	25°C		140	180	Ω
					Full			180	
		2.3 V		$I_{C\ OM}$ = -8 mA	25°C		35	45	
					Full			50	
		3 V		$I_{C\ OM}$ = -24 mA	25°C		12	20	
					Full			20	
		4.5 V		$I_{C\ OM}$ = -30 mA	25°C		5.5	12	
					Full			15	
Δr_{ON}	Maximum ON resistance between any two channels	1.65 V	V_{NO} or V_{NC} = 1.16 V	$I_{C\ OM}$ = -4 mA	25°C		0.5	0.6	Ω
					Full			0.75	
		2.3 V	V_{NO} or V_{NC} = 1.6 V	$I_{C\ OM}$ = -8 mA	25°C		0.3	0.5	
					Full			0.7	
		3 V	V_{NO} or V_{NC} = 2.1 V	$I_{C\ OM}$ = -24 mA	25°C		0.2	0.4	
					Full			0.4	
		4.5 V	V_{NO} or V_{NC} = 3.15 V	$I_{C\ OM}$ = -30 mA	25°C		0.15	0.2	
					Full			0.3	
$r_{on(flat)}$ (YZP Only)	ON resistance flatness	1.65 V	0 ≤ (V_{NO} or V_{NC}) ≤ V_+	$I_{C\ OM}$ = -4 mA	25°C		125	130	Ω
					Full			140	
		2.3 V		$I_{C\ OM}$ = -8 mA	25°C		30	40	
					Full			40	
		3 V		$I_{C\ OM}$ = -24 mA	25°C		9	11	
					Full			12	
		4.5 V		$I_{C\ OM}$ = -30 mA	25°C		4	5	
					Full			6	
$r_{on(flat)}$	ON resistance flatness	1.65 V	0 ≤ (V_{NO} or V_{NC}) ≤ V_+	$I_{C\ OM}$ = -4 mA	25°C		125	160	Ω
					Full			180	
		2.3 V		$I_{C\ OM}$ = -8 mA	25°C		30	50	
					Full			60	
		3 V		$I_{C\ OM}$ = -24 mA	25°C		8	13	
					Full			14	
		4.5 V		$I_{C\ OM}$ = -30 mA	25°C		4	5	
					Full			6	

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T_A = -40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS				MIN	TYP	MAX	UNIT
$I_{NO(OFF)}$, $I_{NC(OFF)}$	NO, NC OFF leakage current	1.65 to 5.5 V	V_{NO} ≥ 0 V_{NC} ≥ 0 V_{COM} ≤ V_+		25°C		±0.05	±0.1	µA
					Full			±0.2	
$I_{NO(ON)}$, $I_{NC(ON)}$	NO, NC ON leakage current	1.65 to 5.5 V	V_{NO} = V_+ or GND V_{NC} = V_+ or GND V_{COM} = Open		25°C		±0.05	±0.1	µA
					Full			±0.2	
$I_{COM(ON)}$	COM ON leakage current	5.5 V	V_{NO} = Open V_{NC} = Open V_{COM} = Open		25°C		±0.05	±0.1	µA
					Full			±0.2	
V_{IH}	Input logic high				Full	V_+ × 0.7		5.5	V
V_{IL}	Input logic low				Full	0		V_+ × 0.3	V
I_{IH}	Input leakage current	1.65 to 5.5 V	5.5V or 0		25°C		0.05	±0.1	µA
					Full			±1	
I_+	Supply current	5.5	V_I = V_+ or GND Switch ON or OFF		25°C		2.5	5	µA
					Full			10	
C_I	Digital input capacitance	5	V_I = V_+ or GND		25°C		2.8		pF
$C_{NO(OFF)}$, $C_{NC(OFF)}$	NO, NC OFF capacitance	5	V_{NO} or V_{NC} = V_+ or GND Switch OFF	V_{NO} or V_{NC} = V_+ or GND Switch OFF	25°C		5.5		pF
$C_{NO(ON)}$, $C_{NC(ON)}$	NO, NC ON capacitance	5	V_{NO} or V_{NC} = V_+ or GND Switch ON		25°C		17.5		pF
$C_{COM(ON)}$	COM ON capacitance	5	V_{NO} or V_{NC} = V_+ or GND Switch ON		25°C		17.5		pF

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

5.6 Switching Characteristics

T_A = -40 to +85°C

Parameter		V_{CC}	T_A	MIN	NOM	MAX	UNIT
t_{ON}	R_L = 300Ω, C_L = 50pF, V_{load} = V_{CC}	1.8 V ± 0.15 V	25°C	5	11	24	ns
			Full	5		24	
		2.5 V ± 0.2 V	25°C	3.5	8	13.5	
			Full	3.5		14	
		3.3 V ± 0.3 V	25°C	3.5	7	9.5	
			Full	1.5		10.5	
		5 V ± 0.5 V	25°C	1	6	8.5	
			Full	1		9.5	
t_{OFF}	R_L = 300Ω, C_L = 50pF, V_{load} = V_{CC}, V_Δ = 0.3V	1.8 V ± 0.15 V	25°C	3	6	11	ns
			Full	3		13	
		2.5 V ± 0.2 V	25°C	1	3.5	7.5	
			Full	1		7.5	
		3.3 V ± 0.3 V	25°C	1	3.5	6.5	
			Full	1		7.5	
		5 V ± 0.5 V	25°C	1	3.5	6.5	
			Full	1		7.5	

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T_A = -40 to +85℃

Parameter		V_{CC}	T_A	MIN	NOM	MAX	UNIT
T_{B-M}	Break before make time	1.8 V ± 0.15 V	25°C	2	5.5	9	ns
			Full	2		12	
		2.5 V ± 0.2 V	25°C	2	5	7	
			Full	2		7.5	
		3.3 V ± 0.3 V	25°C	1	3	6	
			Full	1		6	
		5 V ± 0.5 V	25°C	1	2	5	
			Full	1		5	

5.7 (YZP Only)Switching Characteristics

T_A = -40 to +85℃

Parameter		V_{CC}	T_A	MIN	NOM	MAX	UNIT
t_{ON}	R_L = 300Ω, C_L = 50pF, V_{load} = V_{CC}	1.8 V ± 0.15 V	25°C	5	15	24	ns
			Full	7		24	
		2.5 V ± 0.2 V	25°C	5	8	13.5	
			Full	3.5		14	
		3.3 V ± 0.3 V	25°C	3.5	7	9.5	
			Full	1.5		10.5	
		5 V ± 0.5 V	25°C	1	6	8.5	
			Full	1		9.5	
t_{OFF}	R_L = 300Ω, C_L = 50pF, V_{load} = V_{CC}, V_Δ = 0.3V	1.8 V ± 0.15 V	25°C	1	3.5	6.5	ns
			Full	1		7.5	
		2.5 V ± 0.2 V	25°C	1	3.5	6.5	
			Full	1		7.5	
		3.3 V ± 0.3 V	25°C	1	3.5	6.5	
			Full	1		7.5	
		5 V ± 0.5 V	25°C	1	3.5	6.5	
			Full	1		7.5	
T_{B-M}	Break before make time	1.8 V ± 0.15 V	25°C	5.5	7.5	9	ns
			Full	5.2		12	
		2.5 V ± 0.2 V	25°C	3.5	5	7	
			Full	3		7.5	
		3.3 V ± 0.3 V	25°C	2.5	3	5	
			Full	2		5	
		5 V ± 0.5 V	25°C	1.8	2	3	
			Full	1.8		3.5	

5.8 Analog Channel Specifications

over operating free-air temperature range (unless otherwise noted)

Parameter	TEST CONDITIONS	v_{cc}	MIN	NOM	MAX	UNIT
Frequency response (switch on)[(1)]	R_L = 50 Ω, f_{in} = sine wave	1.65 V		300		MHz
		2.3 V		300		
		3 V		300		
		4.5 V		300		

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over operating free-air temperature range (unless otherwise noted)

Parameter	TEST CONDITIONS	v_{cc}	MIN	NOM	MAX	UNIT
Crosstalk (between switches) (YZP Only)(2)	R_L = 50 Ω, f_{in} = 10 MHz (sine wave)	1.65 V		-66		dB
		2.3 V		-66		
		3 V		-66		
		4.5 V		-66		
Crosstalk (between switches)(2)	R_L = 50 Ω, f_{in} = 10 MHz (sine wave)	1.65 V		-60		dB
		2.3 V		-60		
		3 V		-60		
		4.5 V		-60		
Feed through attenuation (switch off) (YZP Only)(2)	C_L = 5 pF, R_L = 50 Ω, f_{in} = 10 MHz (sine wave)	1.65 V		-65		dB
		2.3 V		-65		
		3 V		-65		
		4.5 V		-65		
Feed through attenuation (switch off)(2)	C_L = 5 pF, R_L = 50 Ω, f_{in} = 10 MHz (sine wave)	1.65 V		-57		dB
		2.3 V		-57		
		3 V		-57		
		4.5 V		-57		
Charge injection	C_L = 0.1 nF, R_L = 1 MΩ	1.65 V		1		pC
		2.3 V		2		
		3.3 V		3		
		5 V		7		
Total harmonic distortion (YZP Only)	V_I = 1.4 V_{p-p}, Vbias = Vcc/2, R_L = 10kΩ, f_{in} = 600 Hz to 20kHz (sine wave)	1.65 V		0.015		%
Total harmonic distortion	V_I = 1.4 V_{p-p}, Vbias = Vcc/2, R_L = 10kΩ, f_{in} = 600 Hz to 20kHz (sine wave)	1.65 V		0.5		%
	V_I = 2.0 V_{p-p}, Vbias = Vcc/2, R_L = 10kΩ, f_{in} = 600 Hz to 20kHz (sine wave)	2.3 V		0.025		
	V_I = 2.5 V_{p-p}, Vbias = Vcc/2, R_L = 10kΩ, f_{in} = 600 Hz to 20kHz (sine wave)	3 V		0.015		
	V_I = 4.0 V_{p-p}, Vbias = Vcc/2, R_L = 10kΩ, f_{in} = 600 Hz to 20kHz (sine wave)	4.5 V		0.01		

(1) Set fin to 0 dBm and provide a bias of 0.4 V. Increase fin frequency until the gain is 3 dB below the insertion loss.
(2) Set fin to 0 dBm and provide a bias of 0.4 V.

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6 Parameter Measurement Information

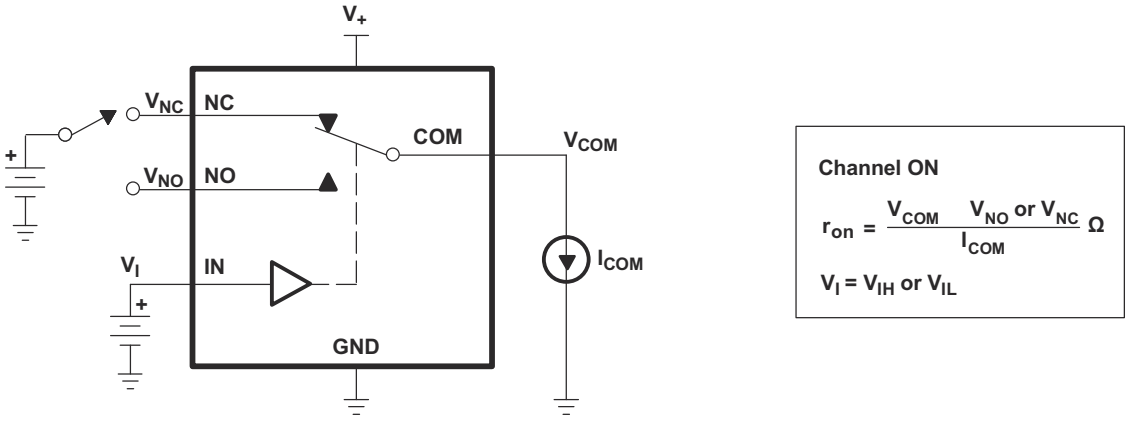

Figure 6-1. ON-State Resistance (r_{on})

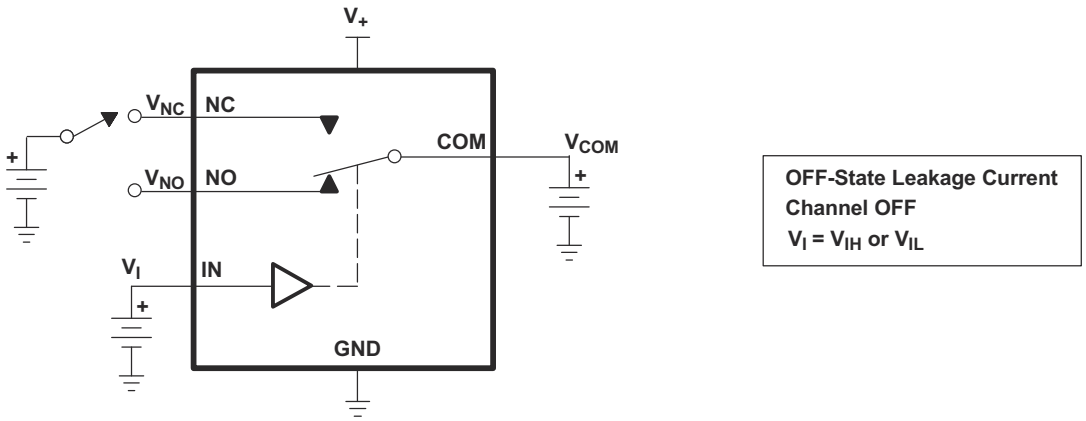

Figure 6-2. OFF-State Leakage Current ($I_{NC(OFF)}$, $I_{NO(OFF)}$)

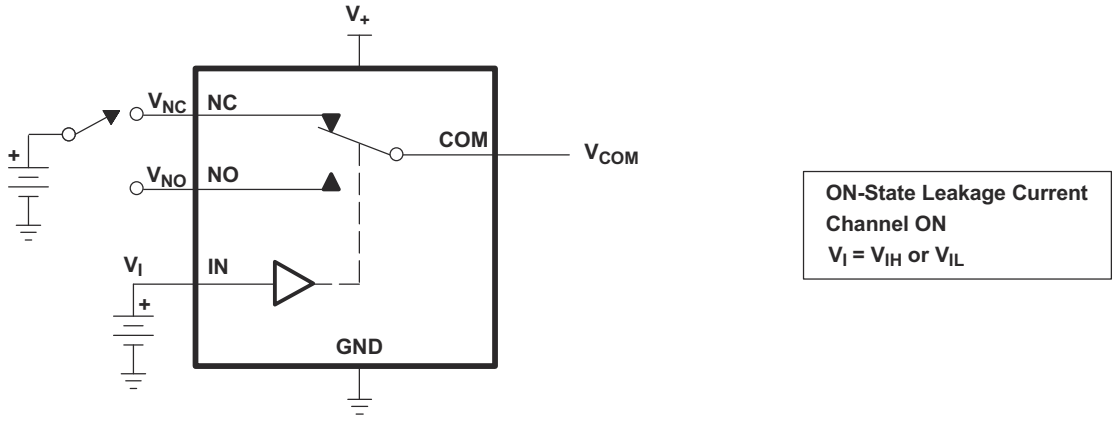

Figure 6-3. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NC(ON)}$, $I_{NO(ON)}$)

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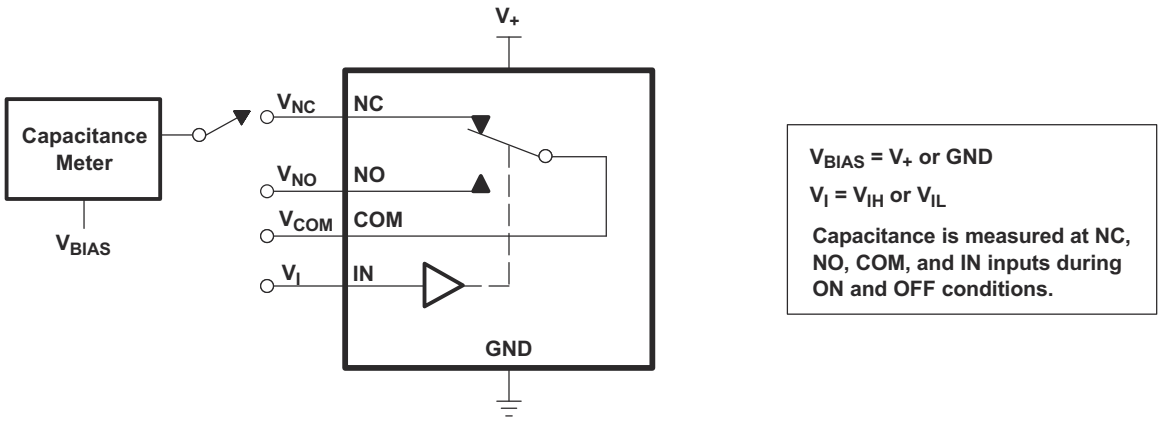
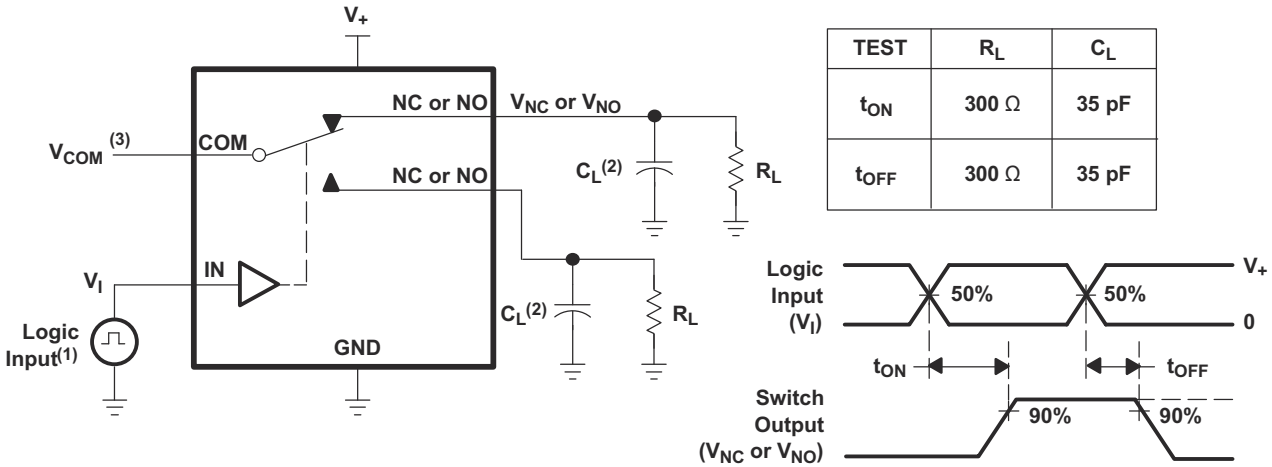


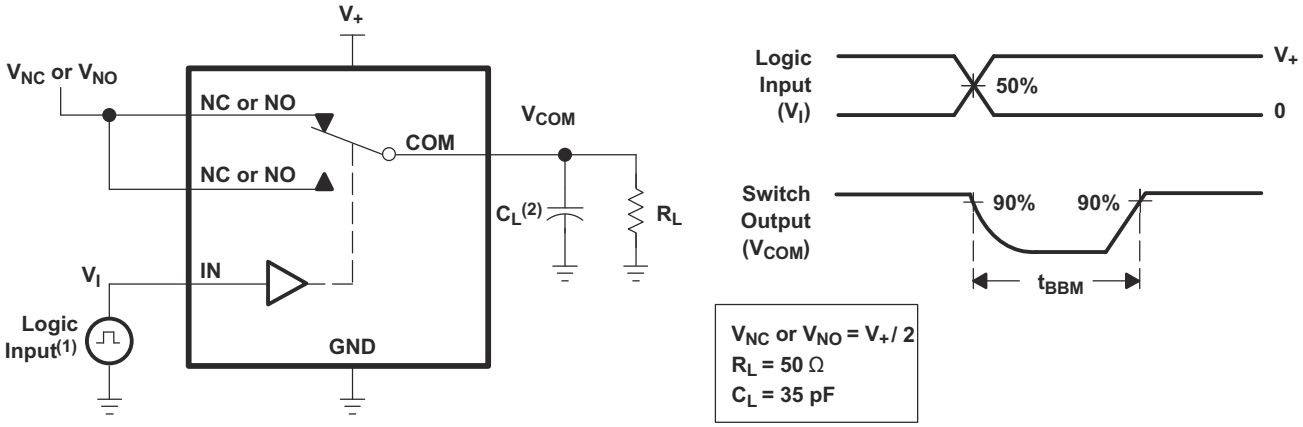
Figure 6-4. Capacitance (C_I, $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NO(OFF)}$, $C_{NC(ON)}$, $C_{NO(ON)}$)



TEST	R_L	C_L
t_{ON}	300 Ω	35 pF
t_{OFF}	300 Ω	35 pF

A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10MHz, Z_O = 50Ω, t_r < 5ns, t_f < 5ns.
B. C_L includes probe and jig capacitance.
C. See Electrical Characteristics for V_{COM}.

Figure 6-5. Turnon (t_{ON}) and Turnoff Time (t_{OFF})



A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.
B. C_L includes probe and jig capacitance.

Figure 6-6. Break-Before-Make Time (t_{BBM})

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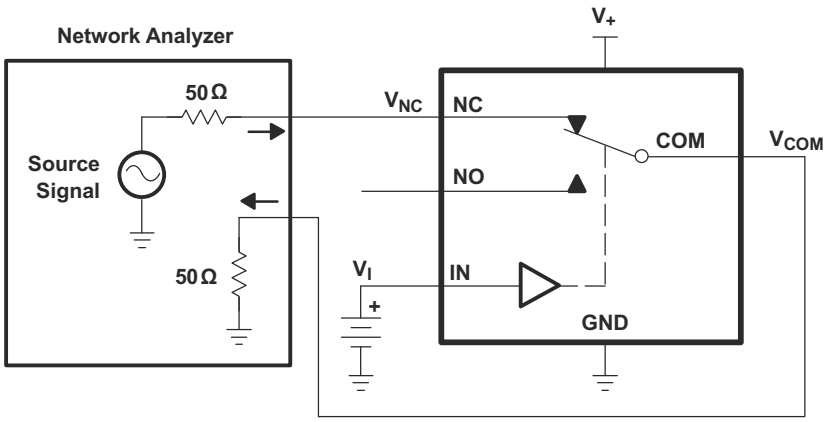


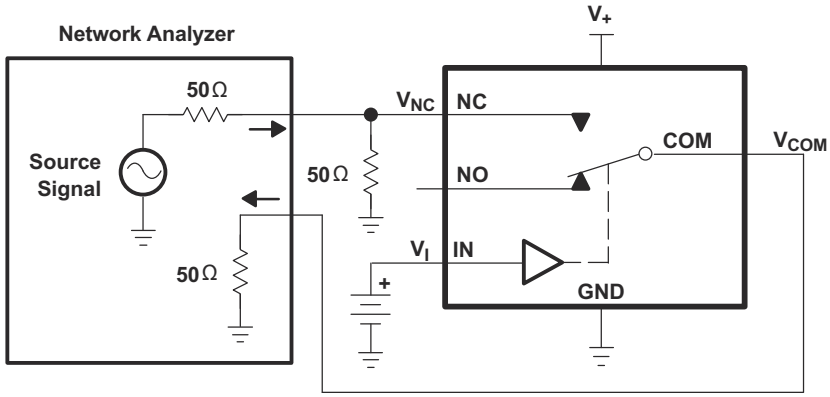
Channel ON: NC to COM
$V_I = V_+$ or GND

Network Analyzer Setup

Source Power = 0 dBm (632-mV P-P at 50-Ω load)

DC Bias = 350 mV

Figure 6-7. Bandwidth (BW)



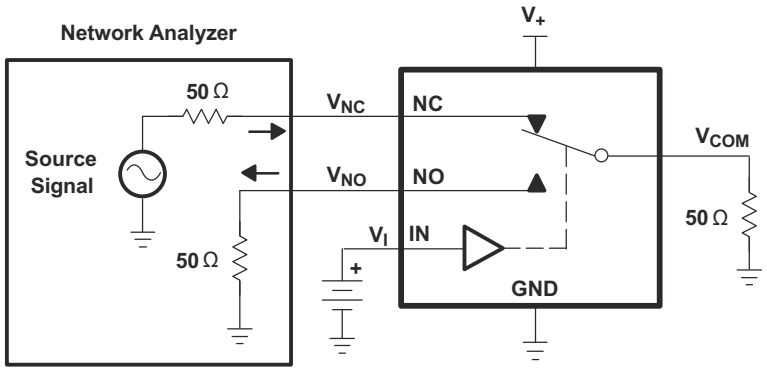
Channel OFF: NC to COM
$V_I = V_+$ or GND

Network Analyzer Setup

Source Power = 0 dBm (632-mV P-P at 50-Ω load)

DC Bias = 350 mV

Figure 6-8. OFF Isolation (O_{ISO})



Channel ON: NC to COM
Channel OFF: NO to COM
$V_I = V_+$ or GND

Network Analyzer Setup

Source Power = 0 dBm (632-mV P-P at 50-Ω load)

DC Bias = 350 mV

Figure 6-9. Crosstalk (X_{TALK})

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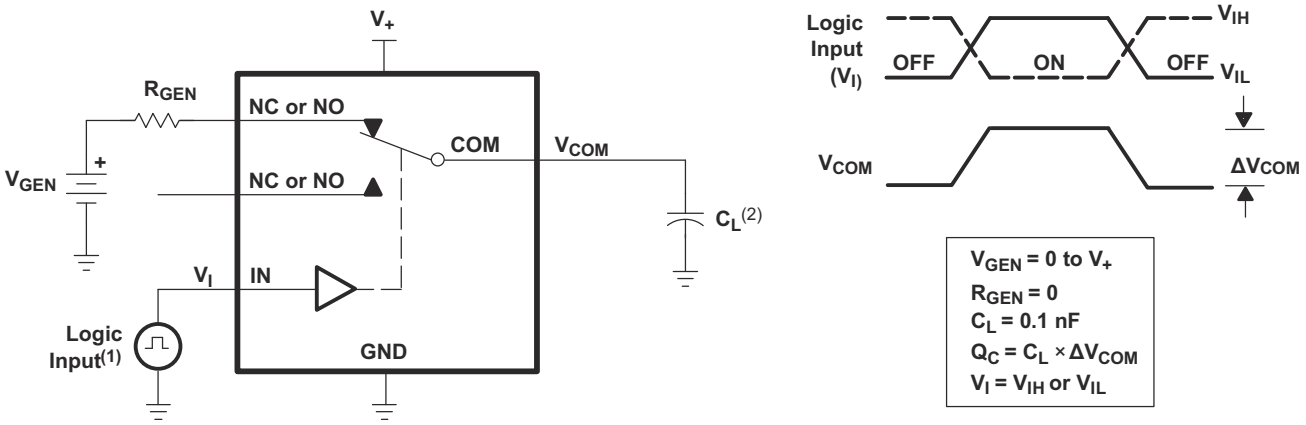
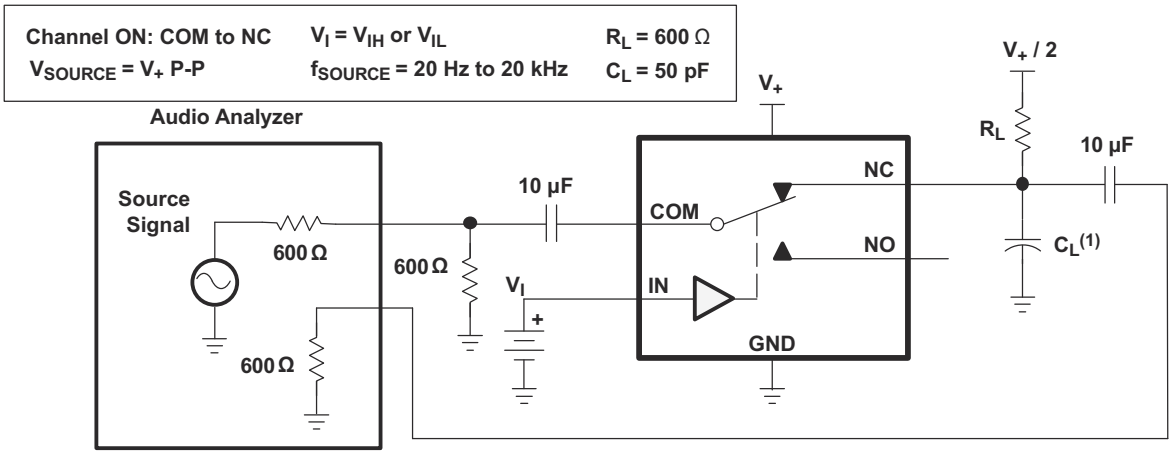


A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.
B. C_L includes probe and jig capacitance.

Figure 6-10. Charge Injection (Q_C)



A. C_L includes probe and jig capacitance.

Figure 6-11. Total Harmonic Distortion (THD)

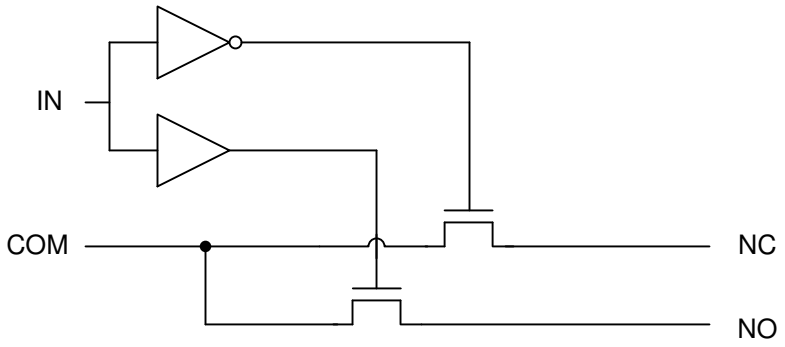
7 Detailed Description

7.1 Overview

The TS5A3157 is a single-pole-double-throw (SPDT) solid-state analog switch. The TS5A3157, like all analog switches, is bidirectional. When powered on, each COM pin is connected to the NC pin. For this device, NC stands for *normally closed* and NO stands for *normally open*. If IN is low, COM is connected to NC. If IN is high, COM is connected to NO.

The TS5A3157 is a break-before-make switch. This means that during switching, a connection is broken before a new connection is established. The NC and NO pins are never connected to each other.

7.2 Functional Block Diagram



7.3 Feature Description

The low ON-state resistance, ON-state resistance matching, and charge injection in the TS5A3157 make this switch an excellent choice for analog signals that require minimal distortion. In addition, the low THD allows audio signals to be preserved more clearly as they pass through the device.

The 1.65V to 5.5V operation allows compatibility with more logic levels, and the bidirectional I/Os can pass analog signals from 0V to V_+ with low distortion. The control inputs are 5V tolerant, allowing control signals to be present without V_{CC}.

7.4 Device Functional Modes

Table 7-1. Function Table

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TS5A3157 can be used in a variety of customer systems. The TS5A3157 can be used anywhere multiple analog or digital signals must be selected to pass across a single line.

8.2 Typical Application

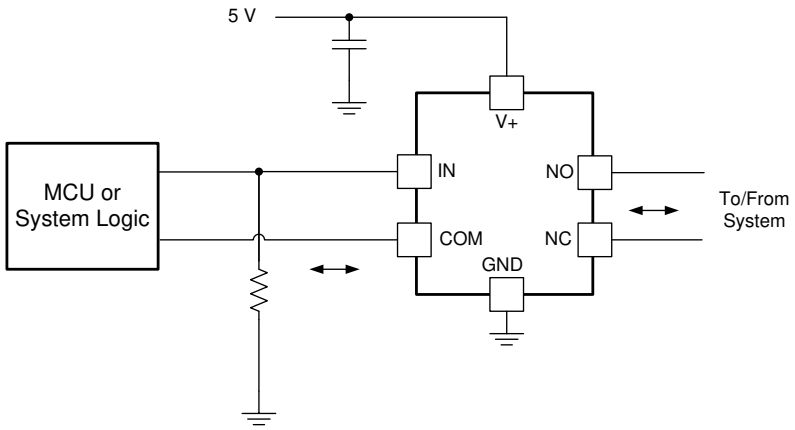

Figure 8-1. System Schematic for TS5A3157

8.2.1 Design Requirements

In this particular application, V_+ was 1.8V, although V_+ is allowed to be any voltage specified in *Section 5.4*. A decoupling capacitor is recommended on the V+ pin. See *Section 8.3* for more details.

8.2.2 Detailed Design Procedure

In this application, IN is, by default, pulled low to GND. Choose the resistor size based on the current driving strength of the GPIO, the desired power consumption, and the switching frequency (if applicable). If the GPIO is open-drain, use pullup resistors instead.

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8.2.3 Application Curve

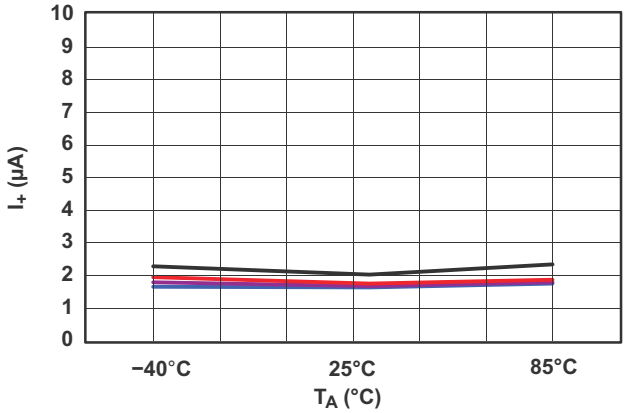

Figure 8-2. Power-Supply Current vs Temperature (V_+ = 5V)

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Section 5.4*.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1µF bypass capacitor is recommended. If there are multiple pins labeled V_{CC}, then a 0.01µF or 0.022µF capacitor is recommended for each V_{CC} because the VCC pins will be tied together internally. For devices with dual supply pins operating at different voltages, for example V_{CC} and V_{DD}, a 0.1µF bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1µF and 1µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self–inductance of the trace — resulting in the reflection. It is a given that not all PCB traces can be straight, and so they will have to turn corners. Below figure shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

Unused switch I/Os, such as NO, NC, and COM, can be left floating or tied to GND. However, the IN pin must be driven high or low. Due to partial transistor turnon when control inputs are at threshold levels, floating control inputs can cause increased I_{CC} or unknown switch selection states.

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8.4.2 Layout Example

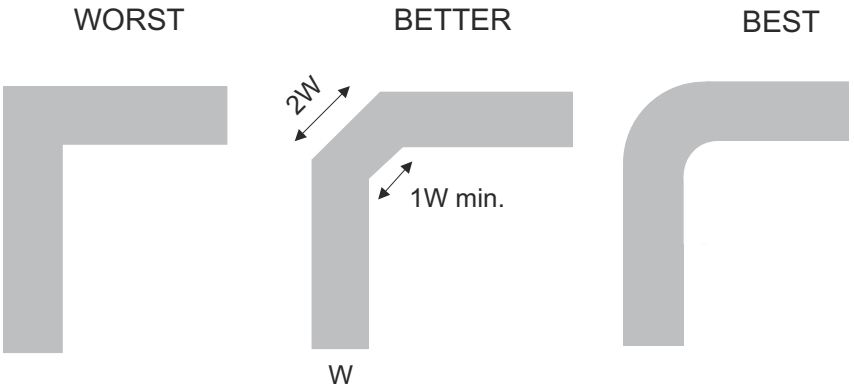

Figure 8-3. Trace Example

9 Device and Documentation Support

9.1 Device Support

9.1.1 Device Nomenclature

Table 9-1. Parameter Description

SYMBOL	DESCRIPTION
V_{COM}	Voltage at COM
V_{NC}	Voltage at NC
V_{NO}	Voltage at NO
r_{on}	Resistance between COM and NC or COM and NO ports when the channel is ON
Δr_{on}	Difference of r_{on} between channels in a specific device
$r_{on(flat)}$	Difference between the maximum and minimum value of r_{on} in a channel over the specified range of conditions
$I_{NC(OFF)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state
$I_{NO(OFF)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state
$I_{NC(ON)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) open
$I_{NO(ON)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open
$I_{COM(ON)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NO or COM to NC) in the ON state and the output (NC or NO) open
V_{IH}	Minimum input voltage for logic high for the control input (IN)
V_{IL}	Maximum input voltage for logic low for the control input (IN)
V_I	Voltage at the control input (IN)
I_{IH}, I_{IL}	Leakage current measured at the control input (IN)
t_{ON}	Turn-on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM, NC, or NO) signal when the switch is turning ON.
t_{OFF}	Turn-off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM, NC, or NO) signal when the switch is turning OFF.
t_{BBM}	Break-before-make time. This parameter is measured under the specified range of conditions and by the propagation delay between the output of two adjacent analog channels (NC and NO) when the control signal changes state.
Q_C	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NC, NO, or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_{COM}$, C_L is the load capacitance and ΔV_{COM} is the change in analog output voltage.
$C_{NC(OFF)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is OFF
$C_{NO(OFF)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is OFF
$C_{NC(ON)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is ON
$C_{NO(ON)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is ON
$C_{COM(ON)}$	Capacitance at the COM port when the corresponding channel (COM to NC or COM to NO) is ON
C_I	Capacitance of control input (IN)
O_{ISO}	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM or NO to COM) in the OFF state.
X_{TALK}	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NC to NO or NO to NC). This is measured in a specific frequency and in dB.
BW	Bandwidth of the switch. This is the frequency where the gain of an ON channel is –3 dB below the DC gain.
THD	Total harmonic distortion describes the signal distortion caused by the analog switch. This is defined as the ratio of root mean square (RMS) value of the second, third, and higher harmonic to the absolute magnitude of fundamental harmonic.
I_+	Static power-supply current with the control (IN) pin at V_+ or GND

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9.2 Documentation Support

9.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs*

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (May 2025) to Revision D (July 2025)	Page
• Separated relevant DBV and DCK specifications from other packages	4

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Changes from Revision B (May 2015) to Revision C (May 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated the *Package Information* table to include package lead size	1
• Updated Ron and flatness values	6
• Included all voltage ranges into the same table and updated conditions accordingly	6
• Updated enable timing for 1.8V, and 2.5V	7
• Updated disable timing for 1.8V, and 2.5V	7
• Updated bbm timing for 1.8V, 2.5V, 3.3V, and 5V	7

Changes from Revision A (September 2004) to Revision B (May 2015)	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Removed *Ordering Information* table.	1

Changes from Revision * (August 2004) to Revision A (September 2004)	Page
• Updated document to new TI data sheet format - no specification changes.	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TS5A3157DBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(3HVH, JC5R)
TS5A3157DBVR.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(3HVH, JC5R)
TS5A3157DBVR.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(3HVH, JC5R)
TS5A3157DCKR	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(3HWH, JC5, JCF, J CJ, JCR)
TS5A3157DCKR.A	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(3HWH, JC5, JCF, J CJ, JCR)
TS5A3157DCKR.B	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(3HWH, JC5, JCF, J CJ, JCR)
TS5A3157YZPR	Active	Production	DSBGA (YZP) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	JCN
TS5A3157YZPR.B	Active	Production	DSBGA (YZP) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	JCN

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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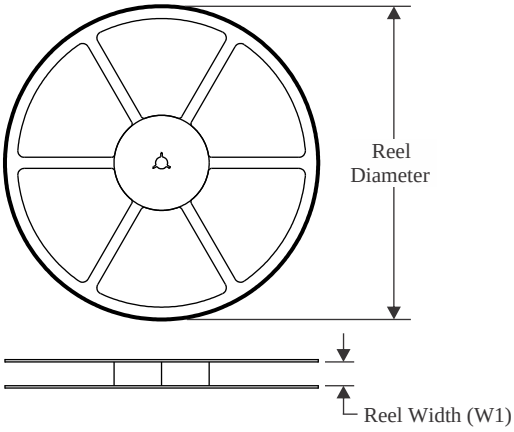
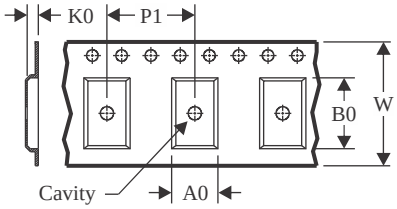
TAPE AND REEL INFORMATION

REEL DIMENSIONS

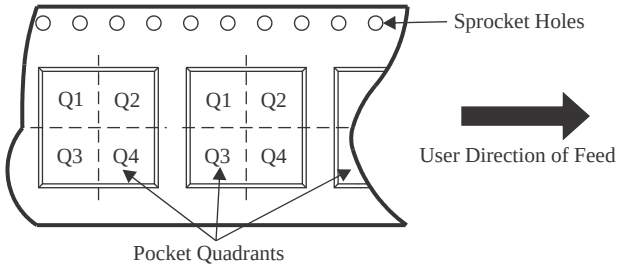


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

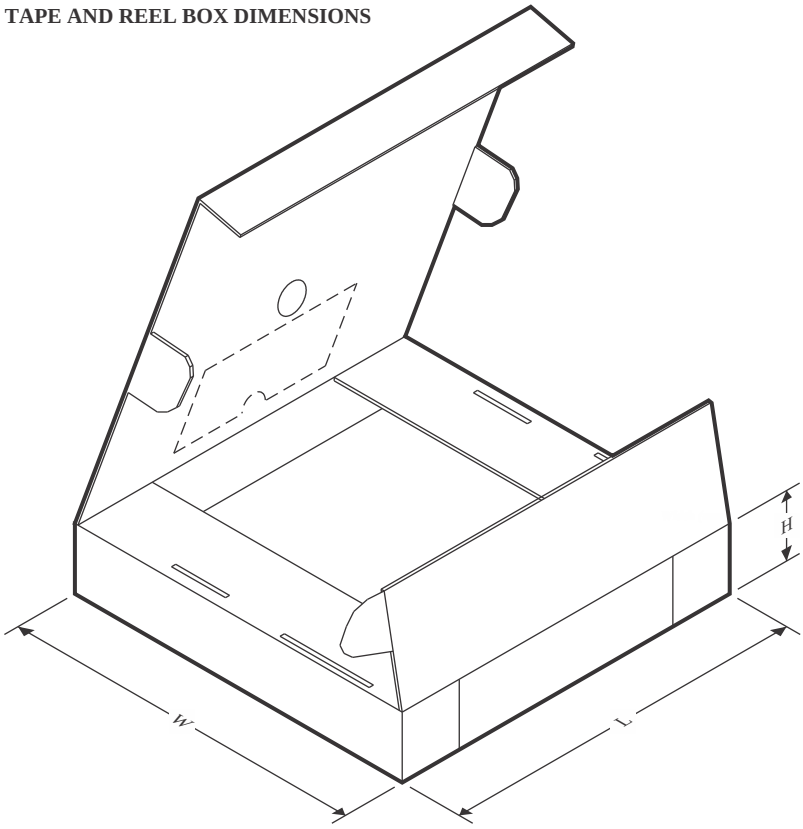
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A3157DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TS5A3157DCKR	SC70	DCK	6	3000	180.0	8.4	2.3	2.55	1.2	4.0	8.0	Q3
TS5A3157DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TS5A3157YZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

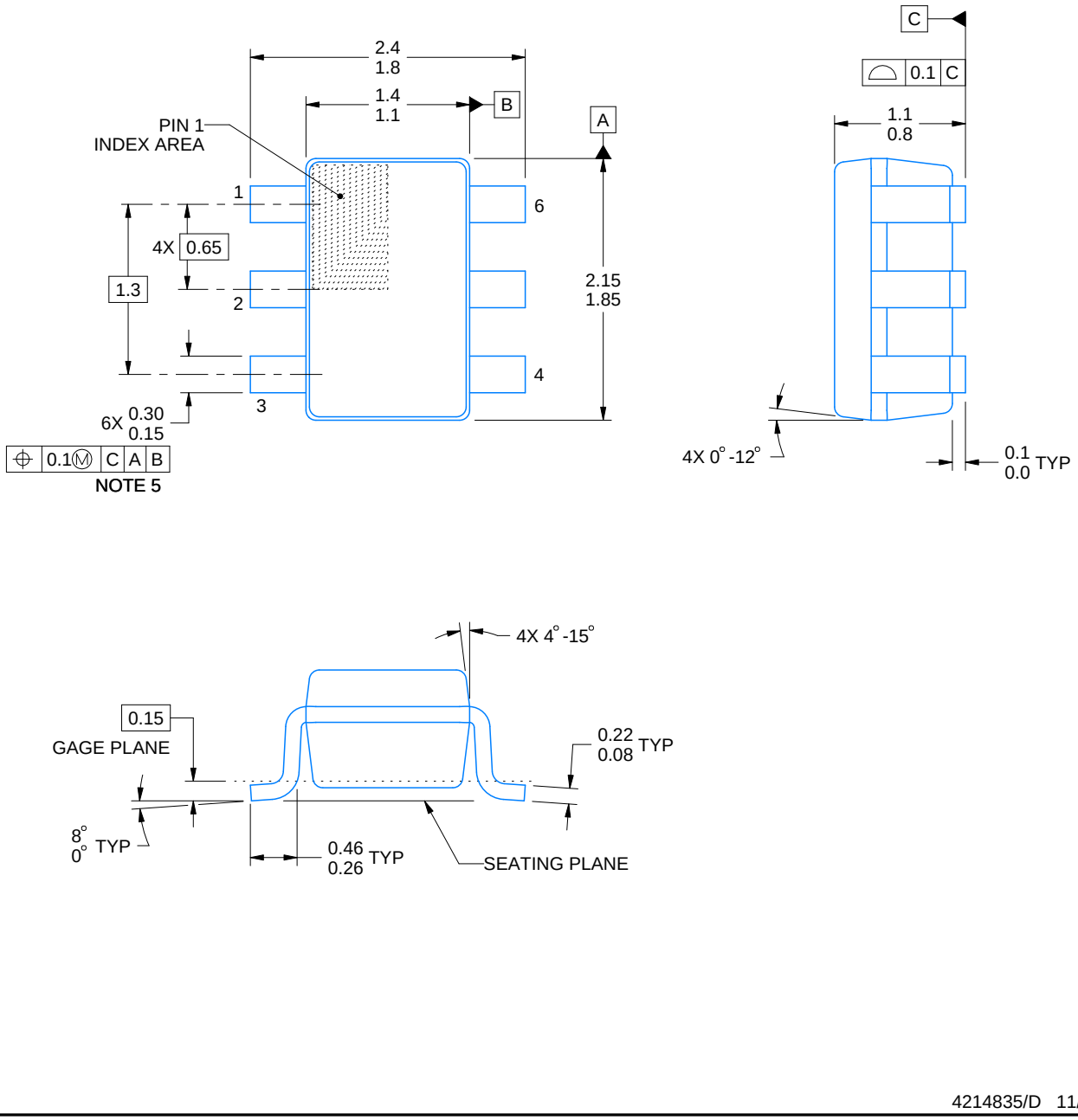
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A3157DBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
TS5A3157DCKR	SC70	DCK	6	3000	210.0	185.0	35.0
TS5A3157DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
TS5A3157YZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0

PACKAGE OUTLINE

DCK0006A

SOT - 1.1 max height

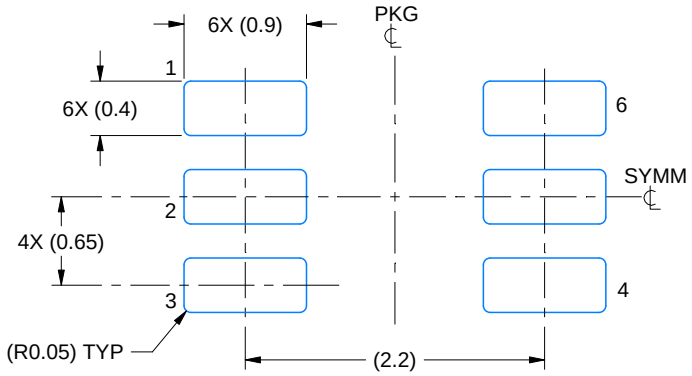
SMALL OUTLINE TRANSISTOR



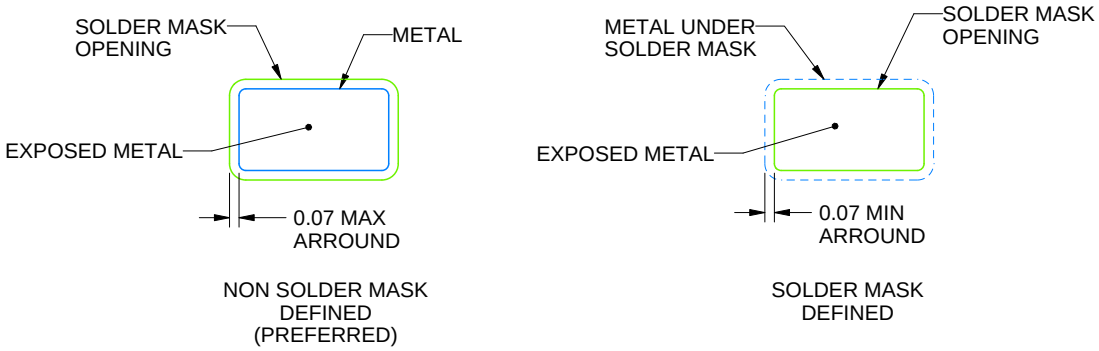
4214835/D 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

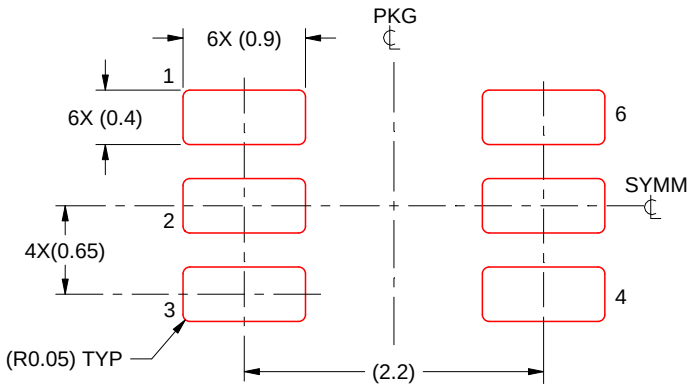


SOLDER MASK DETAILS

4214835/D 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214835/D 11/2024

NOTES: (continued)

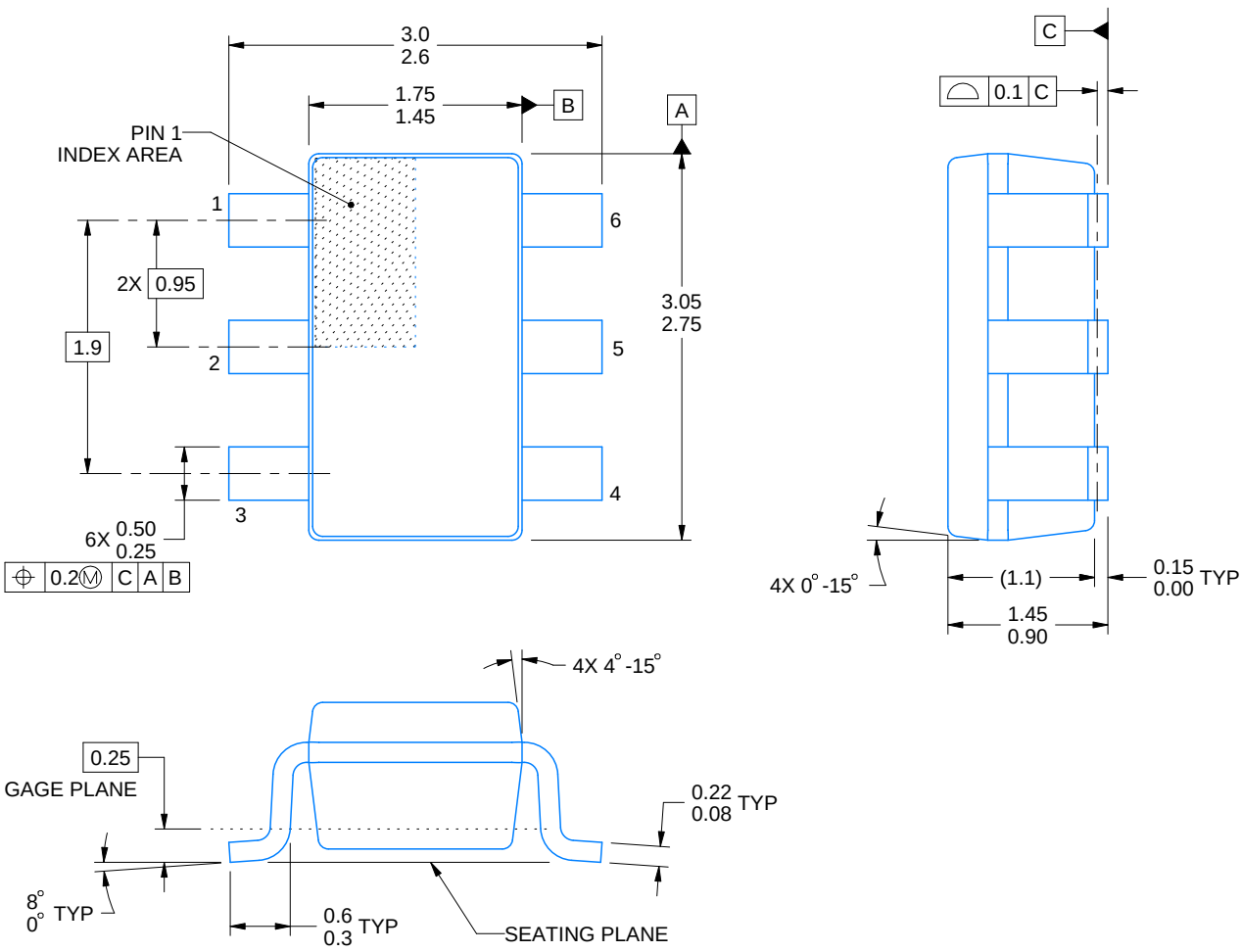
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

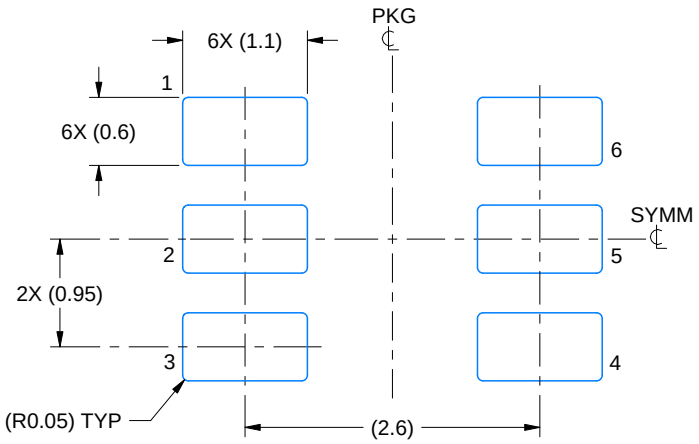
SMALL OUTLINE TRANSISTOR



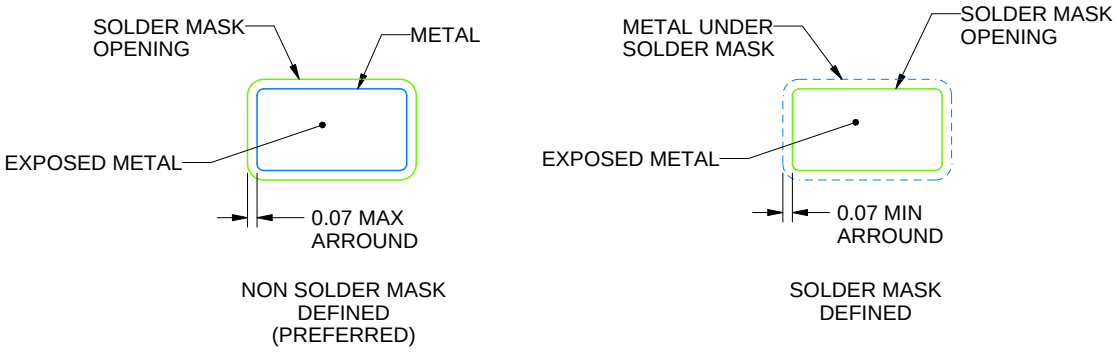
4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

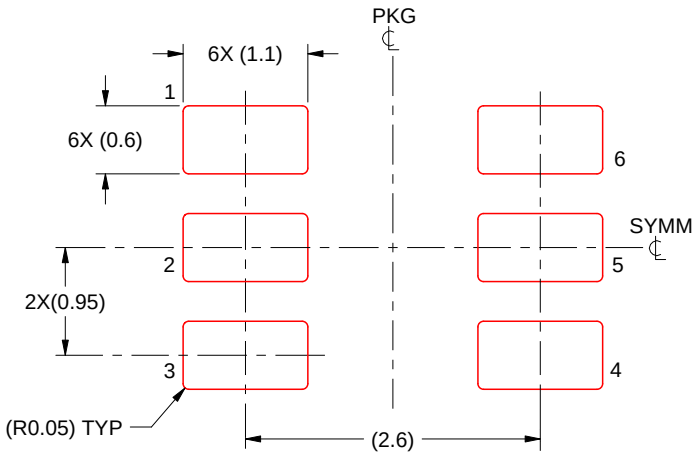


SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

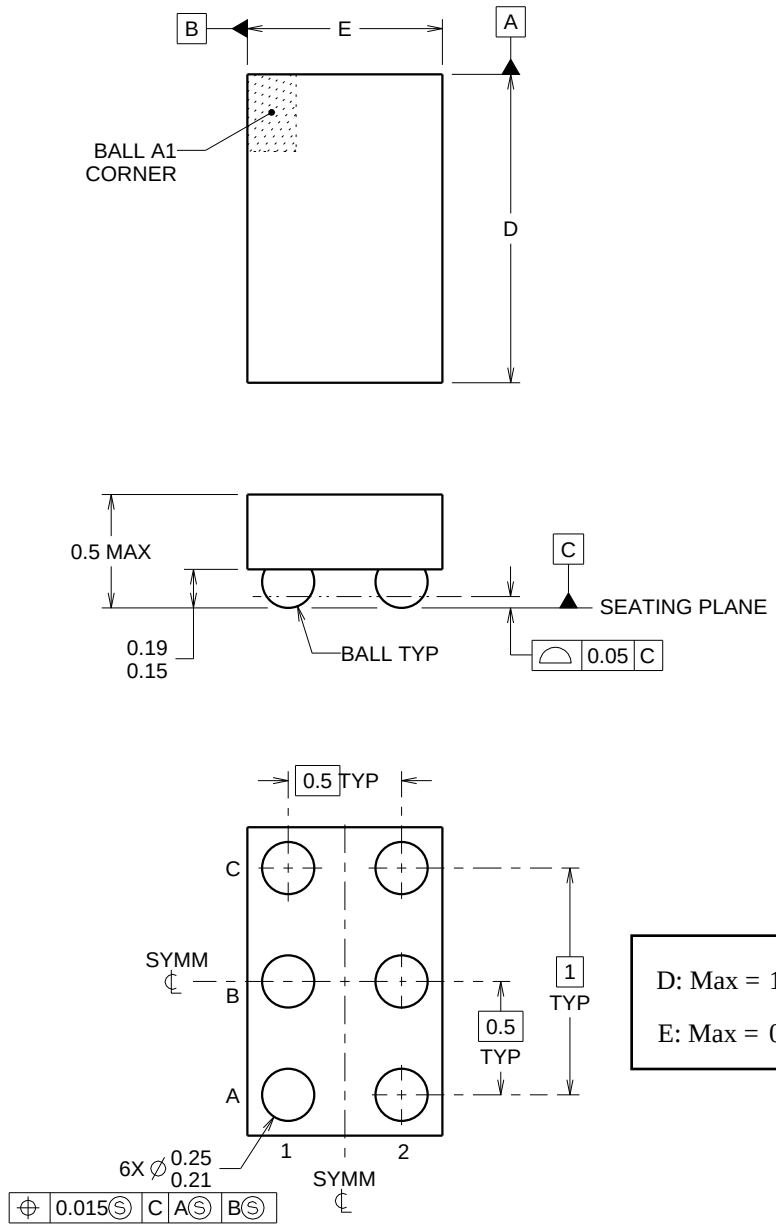
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 1.418 mm, Min =1.358 mm

E: Max = 0.918 mm, Min =0.858 mm

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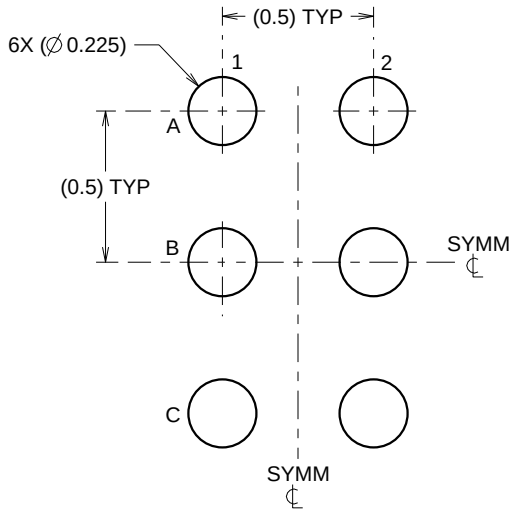
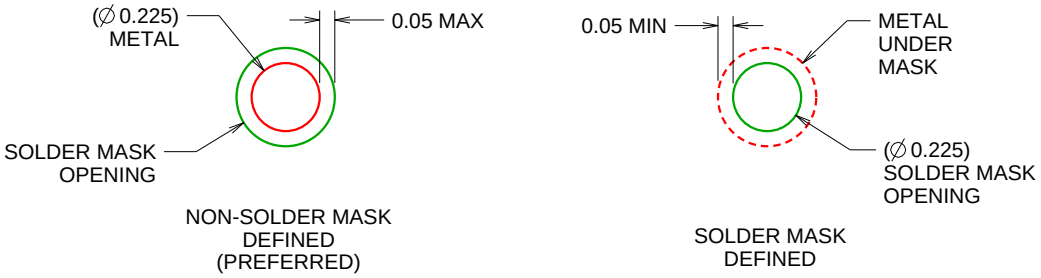
NOTES:

NanoFree Is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

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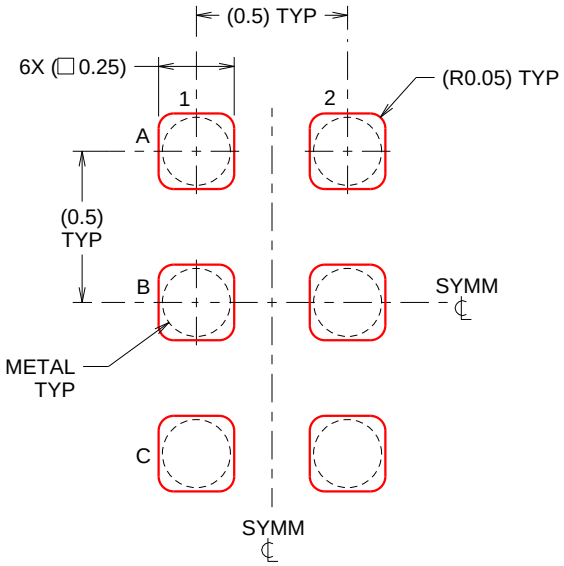
NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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