# 5V, 5-BITS VIDEO EXCHANGE SWITCH FOR DUAL VGA SOURCE TO SINK -2V UNDERSHOOT PROTECTION WITH LOW ON-STATE RESISTANCE

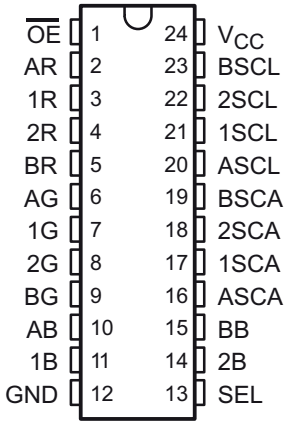
**Check for Samples: TS5V522C**

## FEATURES

- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **High Bandwidth, 380MHZ (typ) RGB Switching**
- **Low ON-State Resistance (ron) Characteristics (ron =3 Ω Typical)**
- **Low Input/Output Capacitance Minimizes Loading and Signal Distortion (CIO(OFF) = 8pF Typical)**
- **Undershoot Clamp Diodes on Data and Control Inputs.**
- **Low Power Consumption (Icc = 3uA Max.)**
- **Vcc Operation Range from 4V to 5.5V**
- **Data I/Os Support 0 to 5-V Signaling Levels (0.8V, 1.2V, 1.5V, 1.8V, 2.5V, 3.3V, 4V)**
- **Allow to pull up resistor up to 5V on the I/O**
- **$I_{off}$ Supports Live Insertion, Partial Power Down Mode, and Back Drive Protection**
- **Latch-Up Performance Exceeds 100Ma Per JESD 78, Class II.**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

## APPLICATIONS

- **Digital and Analog Signal Interface**
- **Audio and Video Signal Interface**
- **High Speed Signal Bus Exchange**
- **Bus Isolation, Interleaving**
- **Notebook Computer Graphics Control**




## DESCRIPTION

The TS5V522C is high bandwidth analog switches offering a 2:2 dual-graphics crossover solution for VGA signal switching. The device is designed for switching between 2 VGA sources to either of the two destinations within a laptop computer. The TS5V522C integrates 5 very high-frequency 380Mhz (typ) SPDT switches for RGB signals, 2 pairs of level-translating buffer for the HSYNC and VSYNC lines, and integrated ESD protection. The 5 crossover switches can be controlled by either 5V or 3.3V TTL control signals.

The TS5V522C would bypass the VGA analog signal to destination with less distortions. DDC Channel (SCA, SCL) may require to +5Vopen drain level at the VGA connector and it may require a pull up resistor on the destination side. Active undershoot-protection circuitry on the data ports of the TS5V522C provide protection for undershoots up to -2V by sensing an undershoot event and ensuring that the switch remains in the proper off state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pull up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ORDERING INFORMATION(1)

| $T_A$ | PACKAGE(2) | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| –40°C to 85°C | SSOP (QSOP) – DBQ | Tape and Reel | TS5V522CDBQR | TS5V522C |
| | TSSOP – PW | Tape and Reel | TS5V522CPWR | TE522C |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

## Table 1. FUNCTION TABLE

| CONTROL | | INPUT/OUTPUTS | | FUNCTIONS | |
|---|---|---|---|---|---|
| $\overline{OE}$ | SEL | 1 X | 2 X | | |
| L | L | A X | B X | 1X port = AX port<br>2x port = BX port | |
| L | H | B X | A X | 1X port = BX port<br>2x port = AX port | |
| H | X | Z | Z | Disconnect | |

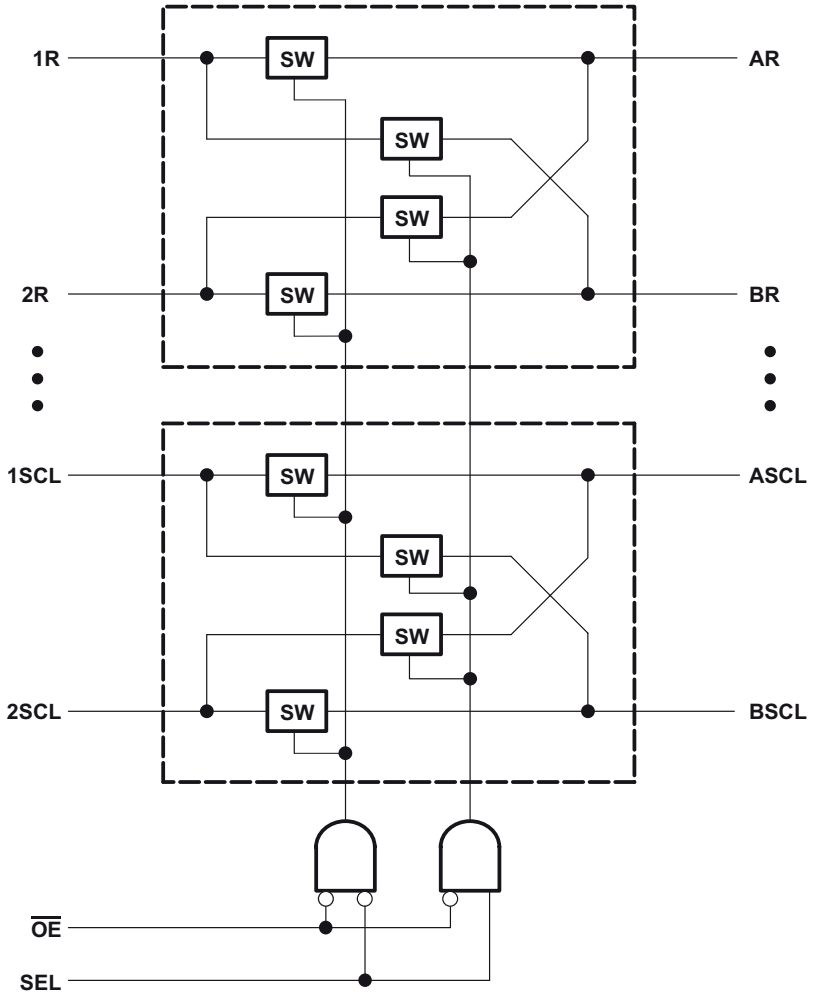
## Table 2. PIN DESCRIPTION

| PIN NAME | DESCRIPTION |
|---|---|
| xR, xG, xB | Analog Video I/Os |
| xSCL, xSCA | Analog sync I/Os |
| $\overline{OE}$ | Enable pin |
| $\overline{EN}$ | Input select |

## PARAMETER DEFINITIONS

| PARAMETER | DESCRIPTION |
|---|---|
| $r_{ON}$ | Resistance between the input and output ports with the switch in the ON-state |
| $I_{OZ}$ | Output leakage current measured at the D and S ports with the switch in the OFF-state |
| $I_{OS}$ | Short circuit current measured at the I/O pins. |
| $V_{IN}$ | Voltage at the IN pin |
| $V_{EN}$ | Voltage at the $\overline{EN}$ pin |
| $C_{IN}$ | Capacitance at the control inputs ($\overline{EN}$, IN) |
| $C_{OFF}$ | Capacitance at the analog I/O port when the switch is OFF |
| $C_{ON}$ | Capacitance at the analog I/O port when the switch is ON |
| $V_{IH}$ | Minimum input voltage for logic high for the control inputs ($\overline{EN}$, IN) |
| $V_{IL}$ | Minimum input voltage for logic low for the control inputs ($\overline{EN}$, IN) |
| $V_H$ | Hysteresis voltage at the control inputs ($\overline{EN}$, IN) |
| $V_{IK}$ | I/O and control inputs diode clamp voltage ($\overline{EN}$, IN) |
| $V_I$ | Voltage applied to the I/O pins when I/O is the switch input. |
| $V_O$ | Voltage applied to the I/O pins when I/O is the switch output. |
| $I_{IH}$ | Input high leakage current of the control inputs ($\overline{EN}$, IN) |
| $I_{IL}$ | Input low leakage current of the control inputs ($\overline{EN}$, IN) |
| $I_I$ | Current into the I/O pins when I/O is the switch input. |
| $I_O$ | Current into the I/O pins when I/O is the switch output. |
| $I_{off}$ | Output leakage current measured at the I/O ports with $V_{CC} = 0$ |
| $t_{ON}$ | Propagation delay measured between 50% of the digital input to 90% of the analog output when switch is turned ON. |
| $t_{OFF}$ | Propagation delay measured between 50% of the digital input to 90% of the analog output when switch is turned OFF. |
| BW | Frequency response of the switch in the ON-state measured at –3 dB |
| $X_{TALK}$ | Unwanted signal coupled from channel to channel. Measured in –dB. $X_{TALK} = 20 \text{ LOG } V_{OUT}/V_{IN}$. This is a non-adjacent crosstalk. |
| $O_{IRR}$ | Off-isolation is the resistance (measured in –dB) between the input and output with the switch OFF. |
| $D_G$ | Magnitude variation between analog input and output pins when the switch is ON and the DC offset of composite video signal varies at the analog input pin. In NTSC standard the frequency of the video signal is 3.58 MHz and DC offset is from 0 to 0.714 V. |
| $D_P$ | Phase variation between analog input and output pins when the switch is ON and the DC offset of composite video signal varies at the analog input pin. In NTSC standard the frequency of the video signal is 3.58 MHz and DC offset is from 0 to 0.714 V. |
| $I_{CC}$ | Static power supply current |
| $I_{CCD}$ | Variation of $I_{CC}$ for a change in frequency in the control inputs ($\overline{EN}$, IN) |
| $\Delta I_{CC}$ | This is the increase in supply current for each control input that is at the specified voltage level, rather than $V_{CC}$ or GND. |

## LOGIC DIAGRAM (XX GATE)



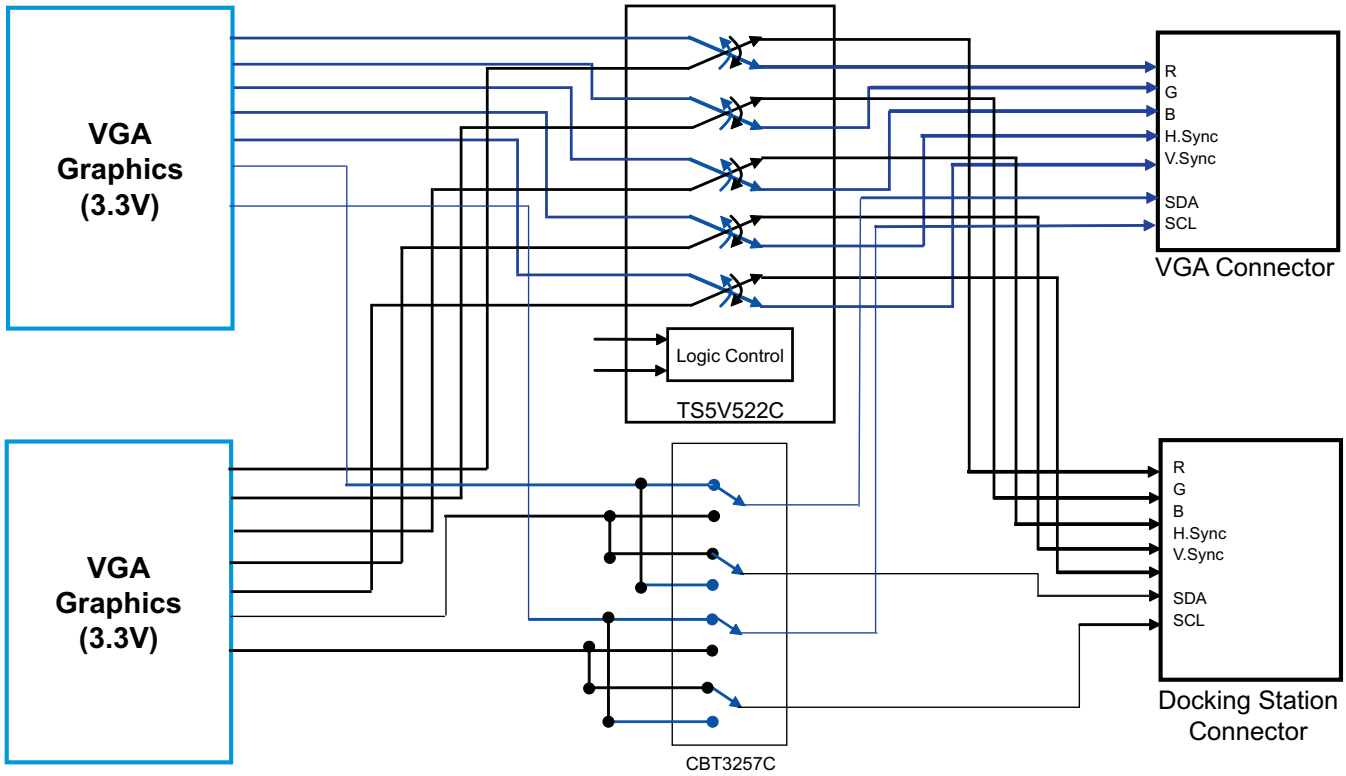
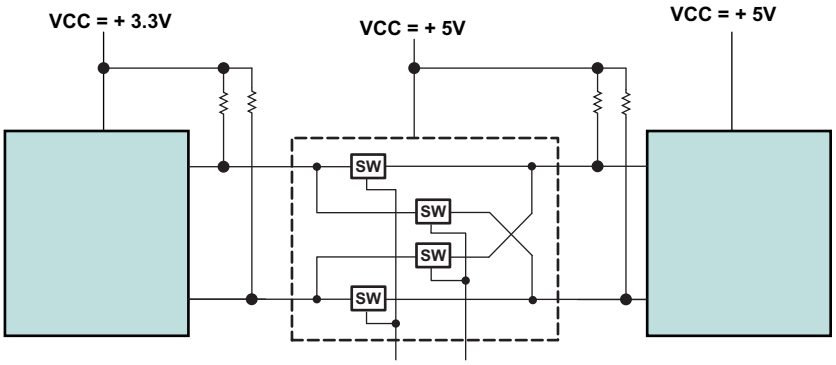



**Figure 1. Typical Design Examples for Dual VGA Source Signal Exchange**




Design Notes:

1. DDC (SCL,SDA) is open drain I²C Bus type and need pull up resistors. N-Channel FET Switch allow to pull up desired Vcc Level not exceeding the Vcc of FET Switch

2. VGA (H.Sync, V.Sync) are TTL/CMOS Type from the source of V ideo and it may required pull up to achieve as high as 5V Signal level to meet VGA Specifications too.

**Figure 2. Typical Design Example for Level Shifting with N-Channel FET Switch**

## ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | –0.5 | 7 | V |
| $V_{IN}$ | Control input voltage range[2][3] | | –0.5 | 7 | V |
| $V_{I/O}$ | Output voltage range[2][3][4] | | –0.5 | 7 | V |
| $I_{IK}$ | Control input clamp current | $V_{IN} < 0$ | | –50 | mA |
| $I_{I/OK}$ | I/O port clamp current | $V_{I/O} < 0$ | | –50 | mA |
| $I_{I/O}$ | ON-state switch current[5] | | | ±128 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±100 | mA |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |

(1) Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All input and output negative voltages are with respect to ground unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) $V_I$ and $V_O$ are used to denote specific conditions for $V_{I/O}$.
(5) $I_I$ and $I_O$ are used to denote specific conditions of $I_{I/O}$.

## THERMAL IMPEDANCE RATINGS

over operating free-air temperature range (unless otherwise noted)

| | | | | UNIT |
|---|---|---|---|---|
| $\theta_{JA}$ | Package thermal impedance | DBQ package[1] | 90 | °C/W |
| | | PW package[1] | 108 | |

(1) The package thermal impedance is calculated in accordance with JESD 51-7.

## RECOMMENDED OPERATING CONDITIONS[1]

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4 | 5.5 | V |
| $V_{IH}$ | High-level control input voltage ($\overline{EN}$, IN) | 2 | 5.5 | V |
| $V_{IL}$ | Low-level control input voltage ($\overline{EN}$, IN) | 0 | 0.8 | V |
| $V_{ANALOG}$ | Analog input/output voltage | 0 | $V_{CC}$ | V |
| $T_A$ | Operating free-air temperature | –40 | 85 | V |

(1) All unused control inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implication of slow or Floating CMOS Inputs*, literature number SCBA004.

## ELECTRICAL CHARACTERISTICS[1]

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP[2] | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IK}$ | $\overline{EN}$, IN | $V_{CC}$ = 4.5 V, | $I_{IN}$ = –18 mA | | | | –1.8 | V |
| $V_H$ | $\overline{EN}$, IN | | | | | | 400 | mV |
| $I_{IH}$ | $\overline{EN}$, IN | $V_{CC}$ = 5.5 V, | $V_{IN}$ and $V_{EN}$ = $V_{CC}$ | | | | ±1 | µA |
| $I_{IL}$ | $\overline{EN}$, IN | $V_{CC}$ = 5.5 V, | $V_{IN}$ and $V_{EN}$ = GND | | | | ±1 | µA |
| $I_{OZ}$[3] | | $V_{CC}$ = 5.5 V, | $V_O$ = 0 to 5.5 V, $V_I$ = 0, | Switch OFF | | | ±10 | µA |
| $I_{OS}$ | | $V_{CC}$ = 5.5 V, | $V_O$ = 0 to 5.5 V, $V_I$ = 0, | Switch ON | | | ±110 | mA |
| $I_{off}$ | | $V_{CC}$ = 0 V, | $V_O$ = 0 to 5.5 V, | $V_I$ = 0 | | | ±1 | µA |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V, | $I_{I/O}$ = 0, | Switch ON or OFF | | | 3 | µA |
| $\Delta I_{CC}$ | $\overline{EN}$, IN | $V_{CC}$ = 5.5 V, | One input at 3.4 V, | Other Inputs at $V_{CC}$ or GND | | | 2.5 | mA |
| $I_{CCD}$ | | $V_{CC}$ = 5.5 V, $V_{EN}$ = GND, | I/O ports are open, | $V_{IN}$ switching 50% duty cycle | | | 0.25 | mA/MHz |
| $C_{in}$ | $\overline{EN}$, IN | $V_{IN}$ or $V_{EN}$ = 0 V, | f = 1 MHz | | | 3..5 | | pF |
| $C_{OFF}$ | D port | $V_{I/O}$ = 3 V or 0 V, | Switch OFF, | $V_{IN}$ = $V_{CC}$ or GND | | 8.5 | | pF |
| | S port | | Switch ON, | | | 5.5 | | |
| $C_{ON}$ | | $V_I$ = 0 V, | f = 1MHz, output open, | Switch ON | | 16.5 | | pF |
| $r_{ON}$[4] | | $V_{CC}$ = 4.5 V, | $V_I$ = 1 V, | $I_O$ = 13 mA, $R_L$ = 75Ω | | 3 | 7 | Ω |
| | | | $V_I$ = 2 V, | $I_O$ = 26 mA, $R_L$ = 75Ω | | 3 | 10 | |

(1) $V_I$, $V_O$, $I_I$, and $I_O$ refer to the I.O pins.
(2) All typical values are at $V_{CC}$ = 5 V (unless otherwise noted). $T_A$ = 25°C
(3) For I/O ports, the parameter $I_{OZ}$ includes the input leakage current.
(4) Measured by the voltage drop between the D and S terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (S or D) terminals.

## SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted), see Figure 9

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{ON}$ | S | D | 1 | | 6.6 | ns |
| $t_{OFF}$ | S | D | 1 | | 6.0 | ns |

## DYNAMIC CHARACTERISTICS

over recommended operating free-air temperature range, VCC = 5 V ±10%(unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP[1] | MAX | UNIT |
|---|---|---|---|---|---|
| $D_G$ | $R_L$ = 150 Ω, f = 3.58 MHz, see Figure 10 | | 0.37 | | % |
| $D_P$ | $R_L$ = 150 Ω, f = 3.58 MHz, see Figure 10 | | 0.0330 | | Deg |
| $B_W$ | $R_L$ = 150 Ω, see Figure 11 | | 380 | | MHz |
| $X_{TALK}$ | $R_{IN}$ = 10 Ω, $R_L$ = 150 Ω, f = 10 MHz, see Figure 11 | | –83 | | dB |
| $O_{IRR}$ | $R_L$ = 150 Ω, f = 10 MHz, see Figure 11 | | –44 | | dB |

(1) All typical values are at $V_{CC}$ = 5V (unless otherwise noted). TA = 25°C.

over recommended operating free-air temperature range, VCC = 5 V ±10%(unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|
| $D_G$ | $R_L$ = 75 Ω, f = 3.58 MHz, see Figure 10 | | 0.37 | | % |
| $D_P$ | $R_L$ = 75 Ω, f = 3.58 MHz, see Figure 10 | | 0.0330 | | Deg |
| $B_W$ | $R_L$ = 75 Ω, see Figure 11 | | 330 | | MHz |
| $X_{TALK}$ | $R_{IN}$ = 10 Ω, $R_L$ = 150Ω, f = 10 MHz, see Figure 11 | | –83 | | dB |
| $O_{IRR}$ | $R_L$ = 75 Ω, f = 10 MHz, see Figure 11 | | –44 | | dB |

(1) All typical values are at $V_{CC}$ = 5V (unless otherwise noted). TA = 25°C.

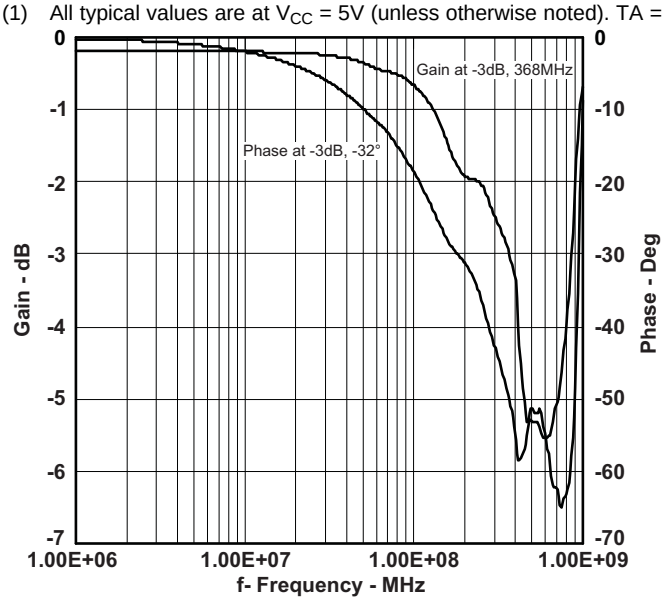



**Figure 3. Frequency Response**

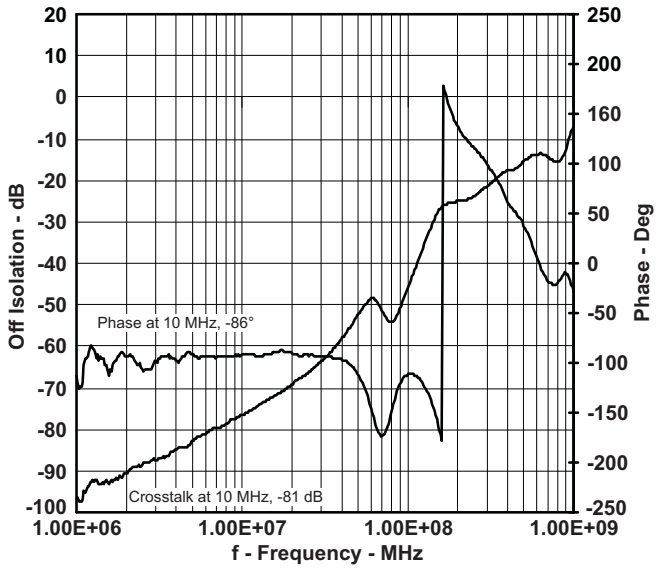



**Figure 4. Non-adjacent Crosstalk vs Frequency**

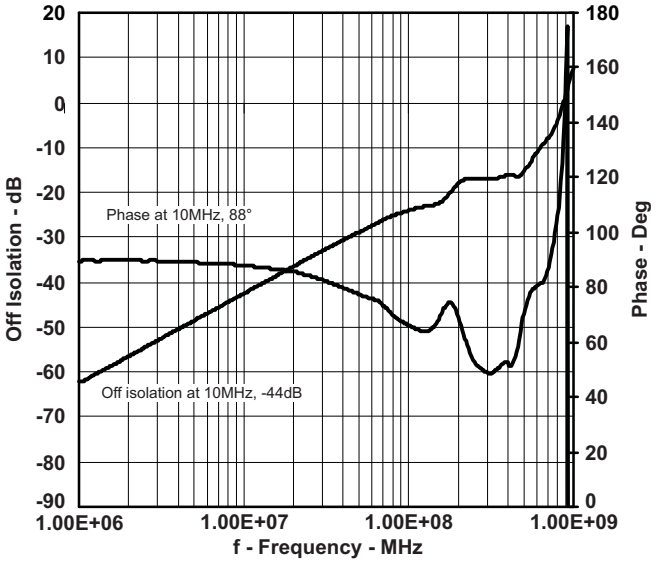



**Figure 5. Off Isolation vs Frequency**

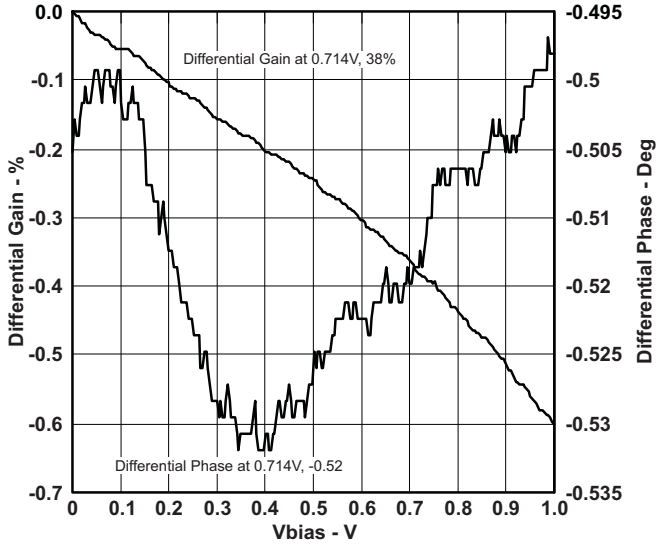



**Figure 6. Differential Phase/Gain vs Vbias**

**Table 3. UNDERSHOOT CHARACTERISTICS (see Figure 7 and Figure 8)**

| PARAMETER | TEST CONDITIONS | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| VOUTU | $V_{CC}$ = 5.5 V, | Switch OFF, | $V_{IN}$ = $V_{CC}$ or GND | 2 | $V_{OH}$ – 0.3 | | V |

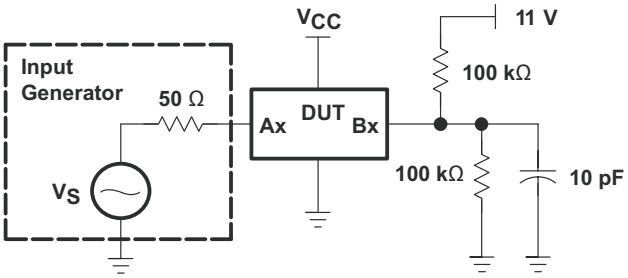



**Figure 7. Device Test Setup**

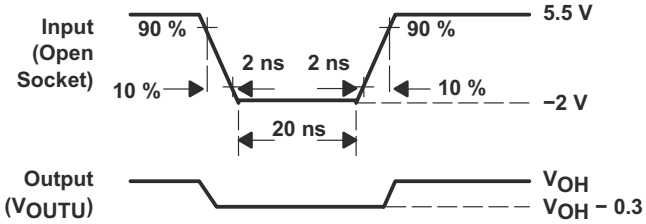
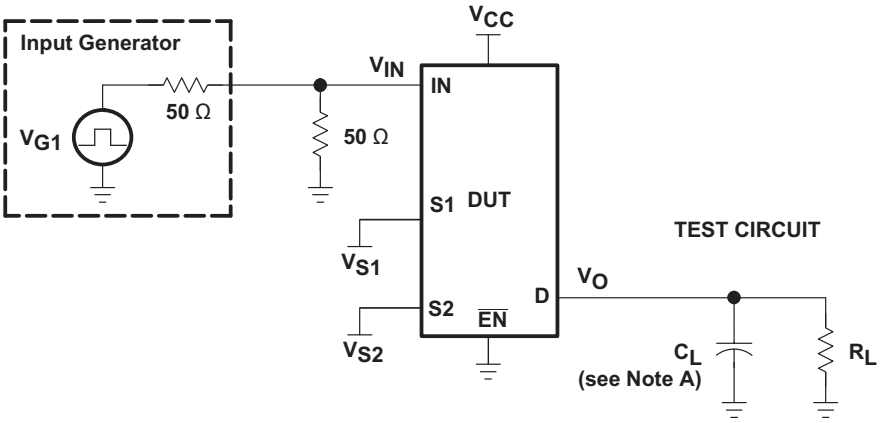



**Figure 8. Transient Input Voltage ($V^I$) and Output Voltage ($V_{OUTU}$) Waveforms (Switch OFF)**

## PARAMETER MEASUREMENT INFORMATION




| TEST | $V_{CC}$ | $R_L$ | $C_L$ | $V_{S1}$ | $V_{S2}$ |
|---|---|---|---|---|---|
| $t_{ON}$ | 5 V ± 0.5 V<br>5 V ± 0.5 V | 75 Ω<br>75 Ω | 20 pF<br>20 pF | GND<br>3 V | 3 V<br>GND |
| $t_{OFF}$ | 5 V ± 0.5 V<br>5 V ± 0.5 V | 75 Ω<br>75 Ω | 20 pF<br>20 pF | GND<br>3 V | 3 V<br>GND |

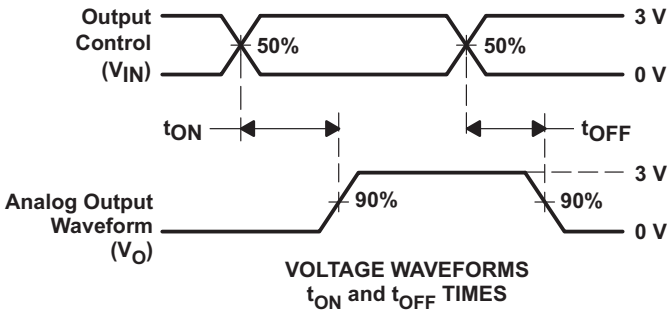
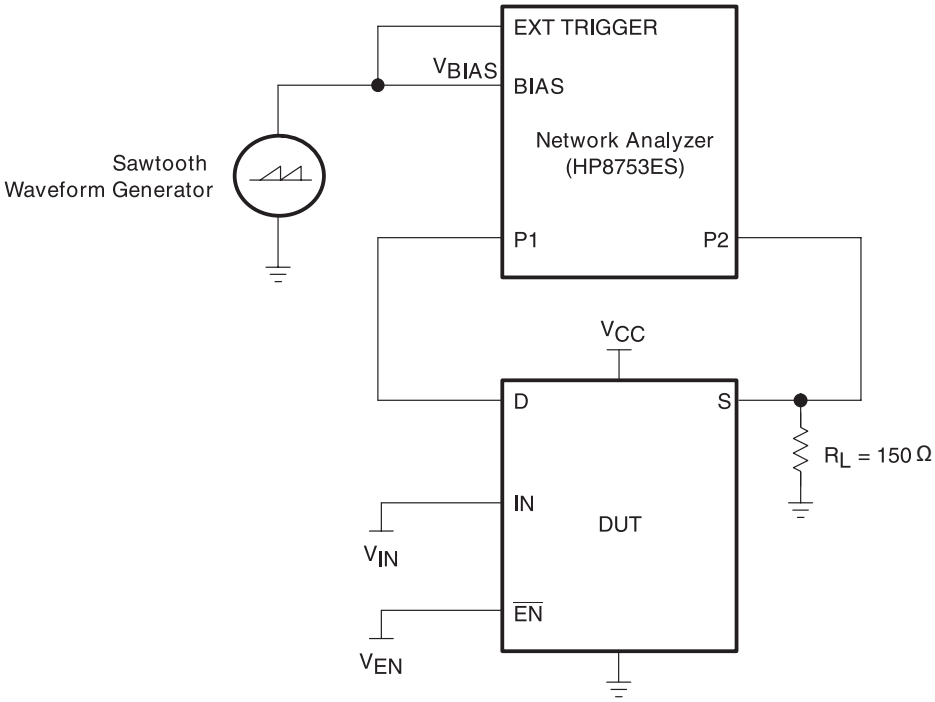



**Figure 9. Test Circuit and Voltage Waveforms**




For additional information, refer to the TI application report, *Measuring Differential Gain and Phase*, literature number SLOA040.

**Figure 10. Test Circuit for Differential Gain/Phase Measurement**

The differential gain and phase is measured at the output of the ON channel. For example, when $V_{IN}$ = 0, $V_{EN}$ = 0, and $D_A$ is the input, the output is measured at $S_{1A}$.

**HP8753ES Setup**

Average = 20

RBW = 300 Hz

Smoothing = 2%

$V_{BIAS}$ = 0 to 1 V

ST = 1.381 s.

P1 = –7 dBM

CW frequency = 3.58 MHz

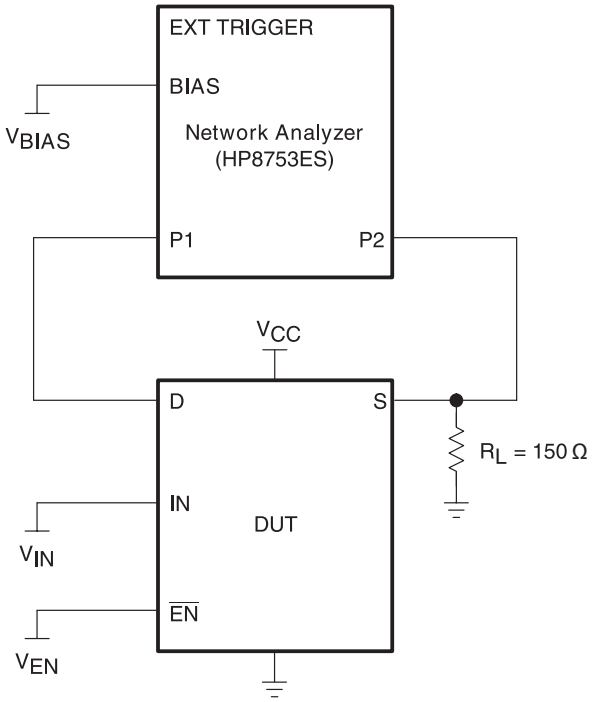



**Figure 11. Test Circuit for Frequency Response, Crosstalk, and OFF-Isolation**

The frequency response is measured at the output of the ON channel. For example, when $V_{IN}$ = 0, $V_{EN}$ = 0, and $D_A$ is the input, the output is measured at $S_{1A}$. All unused analog I/O ports are held at $V_{CC}$ or GND.

The crosstalk is measured at the output of the non-adjacent ON channel. For example, when $V_{IN}$ = 0, $V_{EN}$ = 0, and $D_A$ is the input, the output is measured at $S_{1B}$. All unused analog I/O ports are held at $V_{CC}$ or GND.

The off-isolation is measured at the output of the OFF channel. For example, when $V_{IN}$ = 0, $V_{EN}$ = $V_{CC}$, and $D_A$ is the input, the output is measured at $S_{1A}$. All unused analog I/O ports are held at $V_{CC}$ or GND.

**HP8753ES Setup**

Average = 4

RBW = 3 kHz

Smoothing = 0%

$V_{BIAS}$ = 0.35 V

ST = 2 s

P1 = 0 dBM

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TS5V522CDBQR | Active | Production | SSOP (DBQ) \| 24 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TS5V522C |
| TS5V522CDBQR.B | Active | Production | SSOP (DBQ) \| 24 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TS5V522C |
| TS5V522CPWR | Active | Production | TSSOP (PW) \| 24 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TE522C |
| TS5V522CPWR.B | Active | Production | TSSOP (PW) \| 24 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TE522C |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

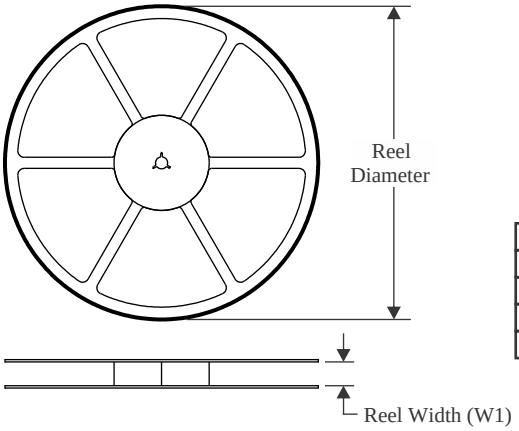
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

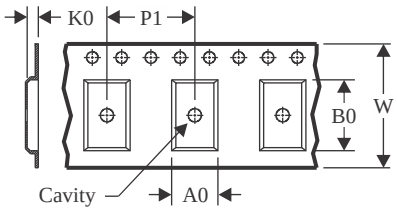
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

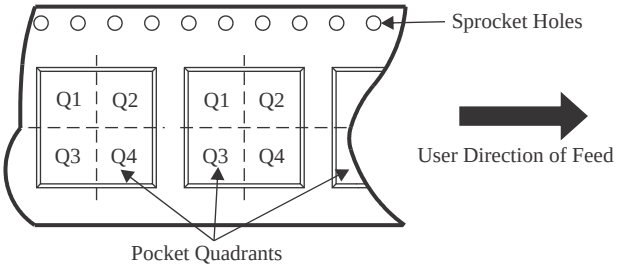



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

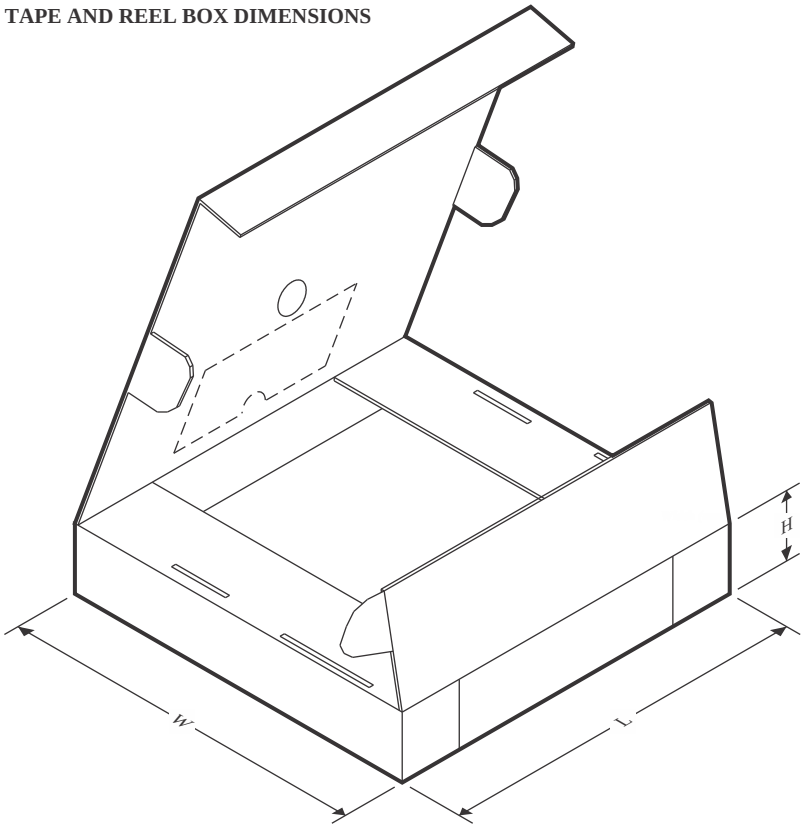
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TS5V522CDBQR | SSOP | DBQ | 24 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TS5V522CPWR | TSSOP | PW | 24 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |

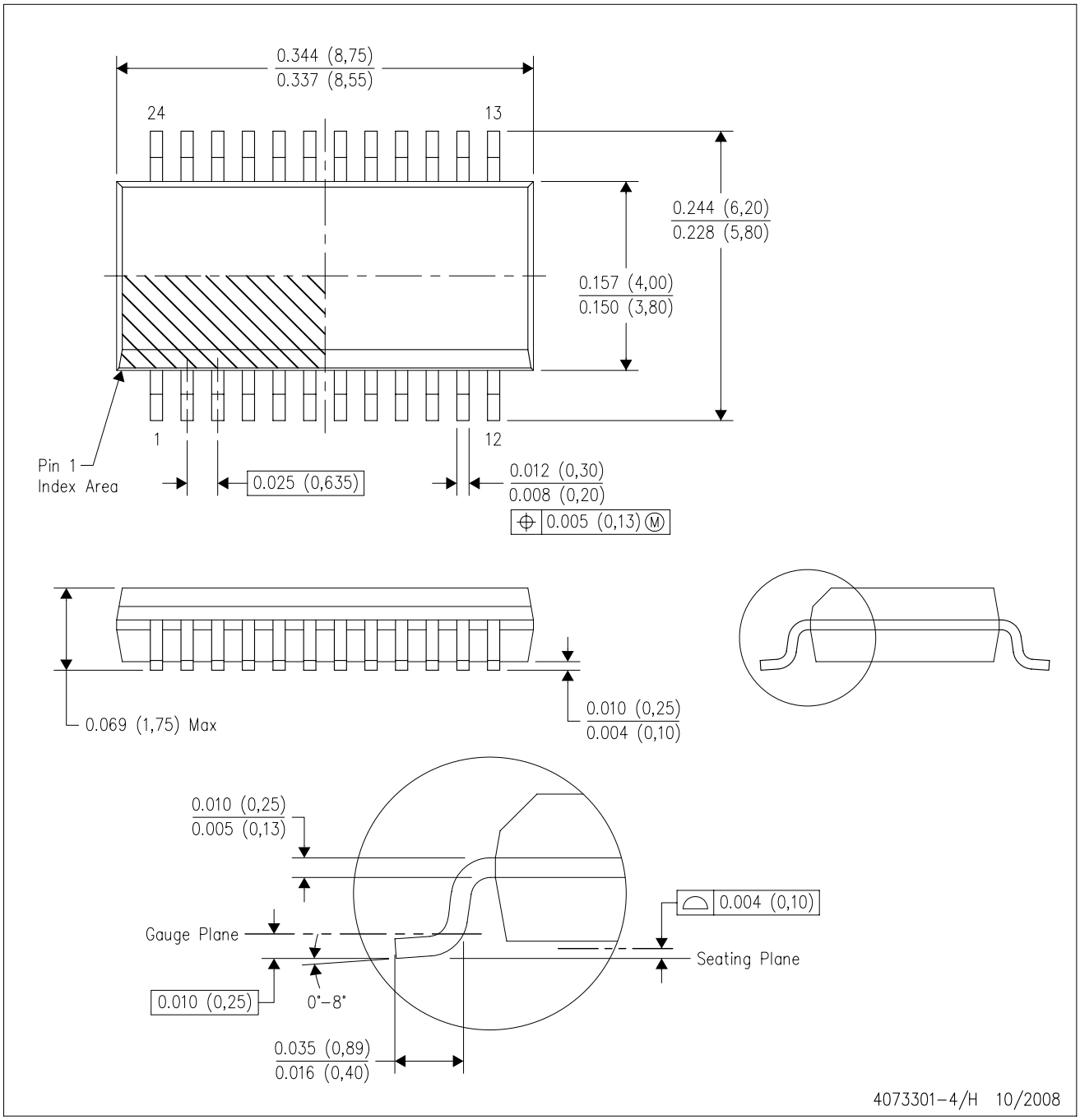
TAPE AND REEL BOX DIMENSIONS



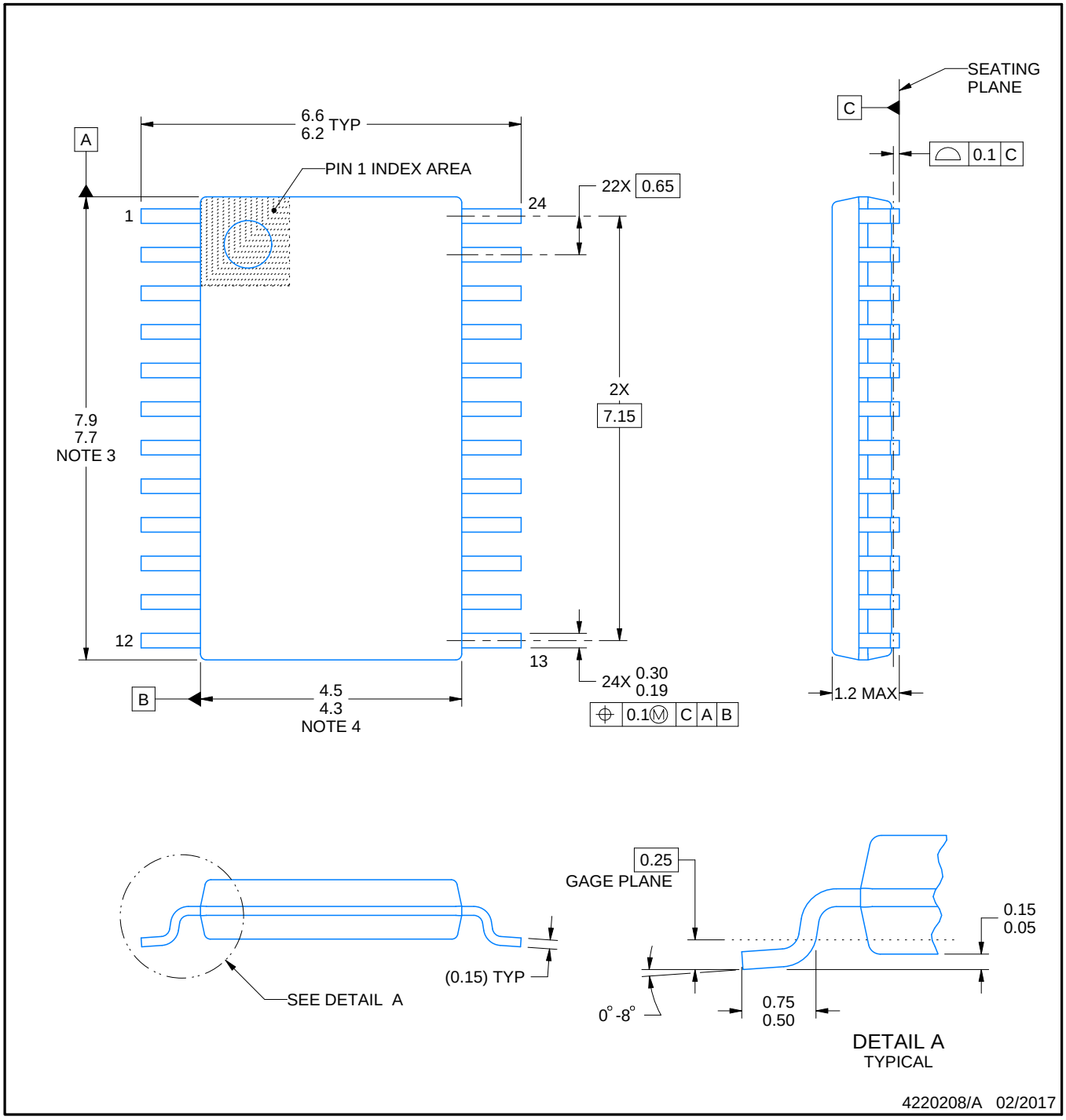

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TS5V522CDBQR | SSOP | DBQ | 24 | 2500 | 353.0 | 353.0 | 32.0 |
| TS5V522CPWR | TSSOP | PW | 24 | 2000 | 353.0 | 353.0 | 32.0 |

DBQ (R–PDSO–G24) PLASTIC SMALL–OUTLINE PACKAGE

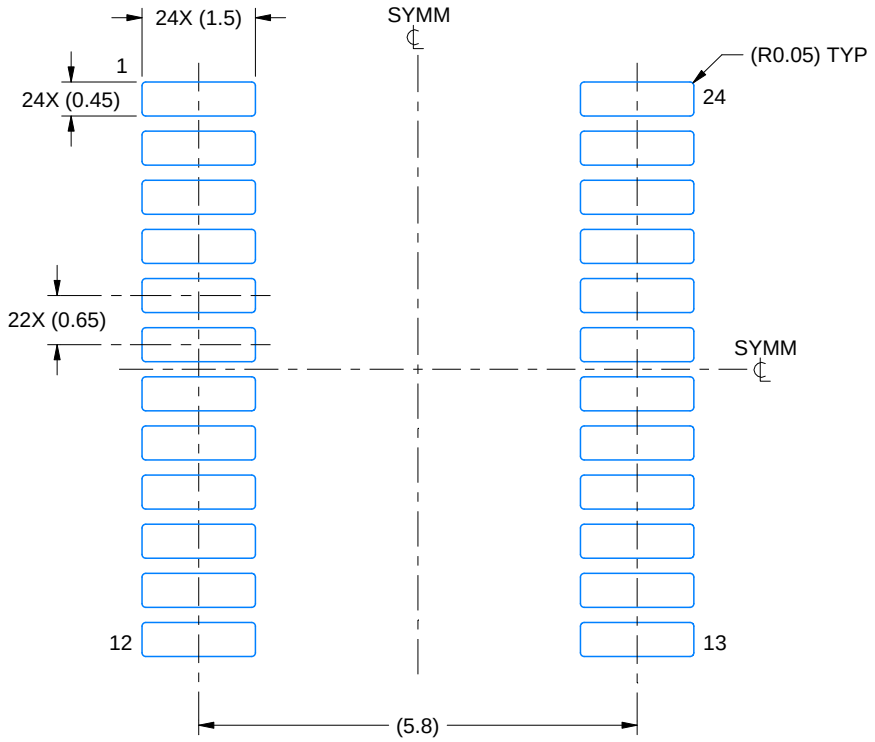



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AE.

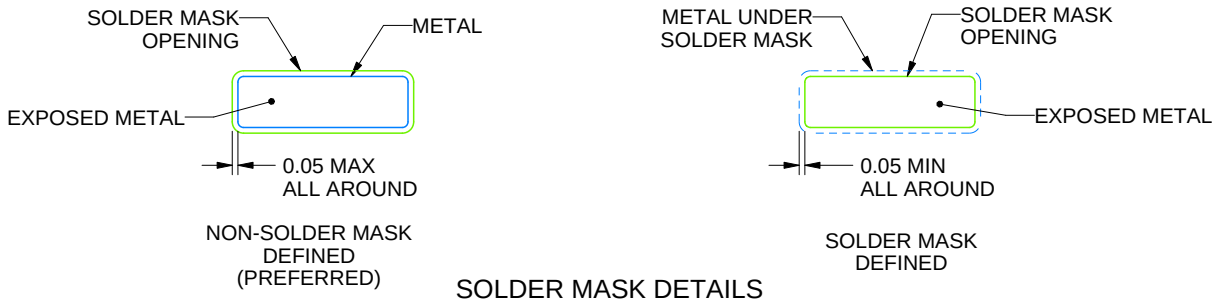



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X




SOLDER MASK DETAILS

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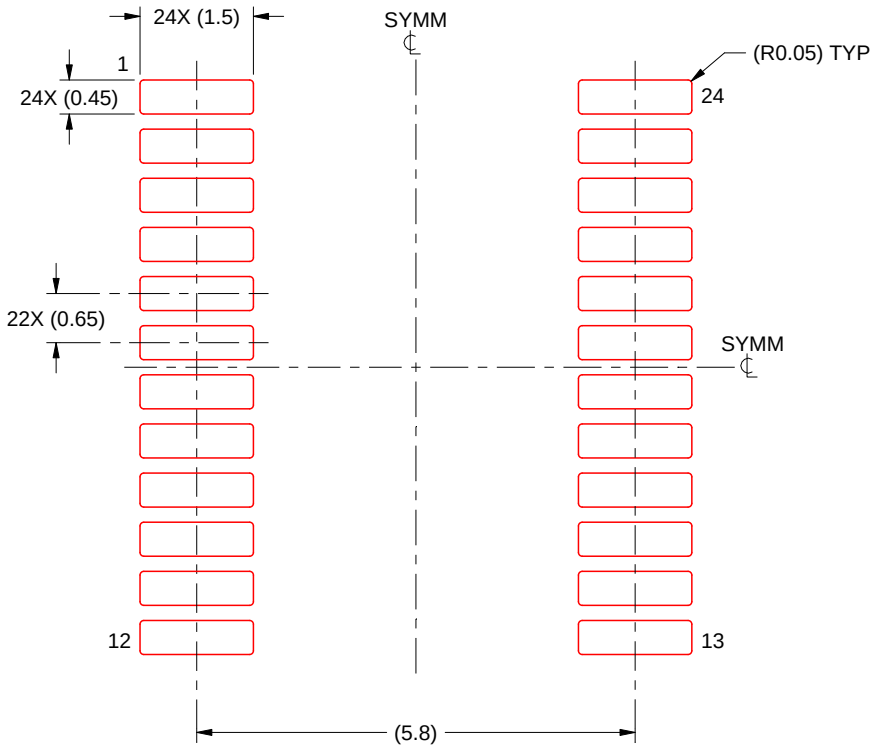
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.