TUSB1042I USB Type-C™ 10 Gbps 2:1 Linear Redriver Switch

1 Features

- USB Type-C™ 2:1 redriver switch
- USB 3.1 Gen 1/Gen 2 up to 10 Gbps
- Ultra-low-power architecture
- Linear redriver with up to 14 dB equalization
- Automatic LFPS de-emphasis control to meet USB 3.1 certification requirements
- Configuration through GPIO or I^2C
- Intel proprietary DCI capability on USB Type-C for closed chassis debugging
- Hot-plug capable
- Industrial temperature range: -40ºC to 85ºC
- 4 mm x 6 mm, 0.4 mm pitch WQFN package

2 Applications

- Tablets
- Notebooks
- Desktops
- Docking stations

3 Description

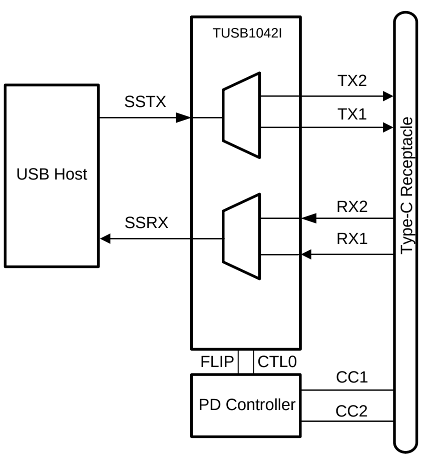
The TUSB1042I is a redriving switch supporting USB 3.1 data rates up to 10 Gbps. The TUSB1042I provides several levels of receive linear equalization to compensate for inter-symbol interference (ISI) due to cable and board trace loss. The device operates on a single 3.3 V supply and comes in the industrial temperature range.

Device Information(1)

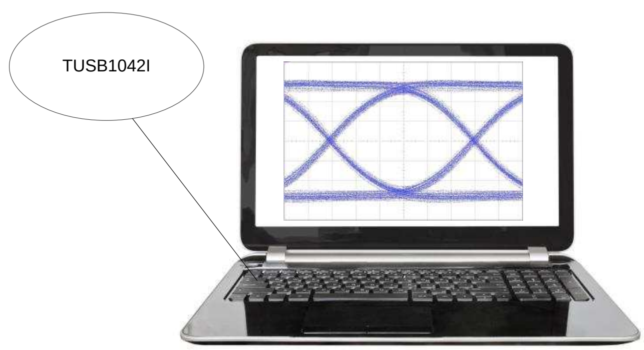
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TUSB1042I	WQFN (40)	4.00 mm x 6.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematics



TUSB1042I Eye Diagram



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4 Revision History

Changes from Revision C (August 2018) to Revision D	Page
• Added following to pin 11 description: If I2C_EN = “F”, then this pin must be set to “F” or “0”.	4

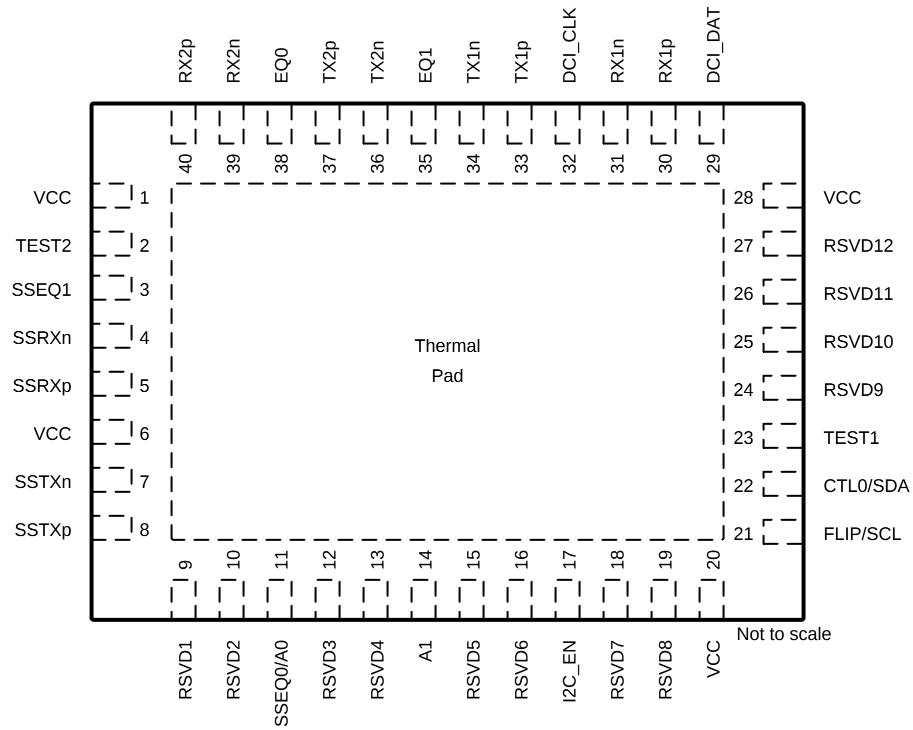
Changes from Revision B (April 2018) to Revision C	Page
• Added Note 1 To pins 29 and 32 in the *Pin Functions* table	3

Changes from Revision A (October 2017) to Revision B	Page
• Changed the appearance of the pinout image in the *Pin Configuration and Function* section	3
• Changed the USB3.1 Control/Status Registers reset value From: 00000000 To: 00000100	23
• Changed the Reset value of bit 3:2 From: 00 To: 01 in Table 12	23

Changes from Original (August 2017) to Revision A	Page
• Changed the Human-body model (HBM) value From: ±6000 To: ±5000 in the *ESD Ratings*	5

5 Pin Configuration and Functions

RNQ Package
40-Pin (WQFN)
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
RX1n	31	Diff I/O	Differential negative input for USB3.1 Downstream Facing port.
RX1p	30	Diff I/O	Differential positive input for USB3.1 Downstream Facing port.
TX1n	34	Diff O	Differential negative output for USB3.1 downstream facing port.
TX1p	33	Diff O	Differential positive output for USB 3.1 downstream facing port.
TX2p	37	Diff O	Differential positive output for USB 3.1 downstream facing port.
TX2n	36	Diff O	Differential negative output for USB 3.1 downstream facing port.
RX2p	40	Diff I/O	Differential positive input for USB3.1 Downstream Facing port.
RX2n	39	Diff I/O	Differential negative input for USB3.1 Downstream Facing port.
SSTXp	8	Diff I	Differential positive input for USB3.1 upstream facing port.
SSTXn	7	Diff I	Differential negative input for USB3.1 upstream facing port.
SSRXp	5	Diff O	Differential positive output for USB3.1 upstream facing port.
SSRXn	4	Diff O	Differential negative output for USB3.1 upstream facing port.
EQ1	35	4 Level I	This pin along with EQ0 sets the USB receiver equalizer gain for downstream facing RX1 and RX2 when USB used.
EQ0	38	4 Level I	This pin along with EQ1 sets the USB receiver equalizer gain for downstream facing RX1 and RX2 when USB used.
DCI_DAT	29 (1)	I/O (PD)	When I2C_EN ! = 0, this pin functions as DCI data output Leave open if not used.
DCI_CLK	32 (1)	I/O (PD)	When I2C_EN ! = 0, this pin functions as DCI clock output Leave open if not used.

(1) Not a fail-safe I/O. Actively driving pin high while VCC is removed results in leakage voltage on VCC pins.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
I2C_EN	17	4 Level I	I^2C Programming Mode or GPIO Programming Select. I2C is only disabled when this pin is ‘0". 0 = GPIO mode (I^2C disabled) R = TI Test Mode (I^2C enabled at 3.3 V) F = I^2C enabled at 1.8 V 1 = I^2C enabled at 3.3 V.
A1	14	4 Level I	When I2C_EN is not ‘0’, this pin will set the TUSB1042I I^2C address.
SSEQ1	3	4 Level I	Along with SSEQ0, sets the USB receiver equalizer gain for upstream facing SSTXP/N.
SSEQ0/A0	11	4 Level I	Along with SSEQ1, sets the USB receiver equalizer gain for upstream facing SSTXP/N. When I2C_EN is not ‘0’, this pin will also set the TUSB1042I I^2C address. If I2C_EN = “F”, then this pin must be set to “F” or “0”.
FLIP/SCL	21	2 Level I	When I2C_EN=’0’ this is Flip control pin, otherwise this pin is I^2C clock. . When used for I^2C clock pullup to I^2C master's VCC I2C supply.
CTL0/SDA	22	2 Level I	When I2C_EN=’0’ this is a USB3.1 Switch control pin, otherwise this pin is I^2C data. When used for I^2C data pullup to I^2C master's VCC I2C supply.
RSVD1 - 12	9, 10, 12, 13, 15, 16, 18, 19, 24, 25, 26, 27	RSVD	Reserved. Leave open.
TEST1	23	2 Level I (Failsafe) (PD)	Test pin. Pull down to GND.
TEST2	2	4 Level I	Test pin. Leave open.
VCC	1, 6, 20, 28	P	3.3-V Power Supply
Thermal Pad		G	Ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
Supply Voltage Range[(2)], V_{CC}		–0.3	4	V
Voltage Range at any input or output pin	Differential voltage between positive and negative inputs		±2.5	V
	Voltage at differential inputs	–0.5	V_{CC} + 0.5	V
	CMOS Inputs	–0.5	V_{CC} + 0.5	V
Maximum junction temperature, T_J			125	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the GND terminals.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±5000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Main power supply		3	3.3	3.6	V
	Supply Ramp Requirement				100	ms
$V_{(12C)}$	Supply that external resistors are pulled up to on SDA and SCL		1.7		3.6	V
$V_{(PSN)}$	Supply Noise on V_{CC} pins				100	mV
T_A	Operating free-air temperature	TUSB1042I	-40		85	°C

6.4 Thermal Information

THERMAL METRIC[(1)]		TUSB1042I RNQ (WQFN) 40 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	37.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	20.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	9.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Power Supply Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$P_{CC(ACTIVE-USB)}$	Average active power USB Only	Link in U0 with GEN2 data transmission. EN, EQ cntrl pins = NC, k28.5 pattern at 10 Gbps, V_{ID} = 1000 mV_{PP} ; CTL1 = L; CTL0 = H		335		mW
$P_{CC(ACTIVE-USB-DP1)}$	Average active power USB + 2 Lane DP	Link in U0 with GEN2 data transmission. EN, EQ cntrl pins = NC, k28.5 pattern at 10 Gbps, V_{ID} = 1000 mV_{PP}; CTL1 = H; CTL0 = H		634		mW
$P_{CC(ACTIVE--DP)}$	Average active power 4 Lane DP Only	Four active DP lanes operating at 8.1Gbps; CTL1 = H; CTL0 = L;		660		mW
$P_{CC(NC-USB)}$	Average power with no connection	No GEN1 device is connected to TXP/TXN; CTL1 = L; CTL0 = H;		2.4		mW
$P_{CC(U2U3)}$	Average power in U2/U3	Link in U2 or U3 USB Mode Only; CTL1 = L; CTL0 = H;		3		mW
$P_{CC(SHUTDOWN)}$	Device Shutdown	CTL1 = L; CTL0 = L; I2C_EN = 0;		0.85		mW

6.6 DC Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
4-State CMOS Inputs(EQ[1:0], SSEQ[1:0], I2C_EN)						
I_{IH}	High level input current	V_{CC} = 3.6 V; V_{IN} = 3.6 V	20		80	µA
I_{IL}	Low level input current	V_{CC} = 3.6 V; V_{IN} = 0 V	–160		-40	µA
4-Level V_{TH}	Threshold 0 / R	V_{CC} = 3.3 V		0.55		V
	Threshold R/ Float	V_{CC} = 3.3 V		1.65		V
	Threshold Float / 1	V_{CC} = 3.3 V		2.7		V
R_{PU}	Internal pull-up resistance			35		kΩ
R_{PD}	Internal pull-down resistance			95		kΩ
2-State CMOS Input (CTL0, TEST1, FLIP) TEST1, CTL0 and FLIP are Failsafe.						
V_{IH}	High-level input voltage		2		3.6	V
V_{IL}	Low-level input voltage		0		0.8	V
R_{PD}	Internal pull-down resistance for CTL1			500		kΩ
$R_{(ENPD)}$	Internal pull-down resistance for pin 29 and pin 32			150		kΩ
I_{IH}	High-level input current	V_{IN} = 3.6 V	–25		25	µA
I_{IL}	Low-level input current	V_{IN} = GND, V_{CC} = 3.6 V	–25		25	µA
I^2C Control Pins SCL, SDA						
V_{IH}	High-level input voltage	I2C_EN = 0	0.7 x $V_{(I2C)}$		3.6	V
V_{IL}	Low-level input voltage	I2C_EN = 0	0		0.3 x $V_{(I2C)}$	V
V_{OL}	Low-level output voltage	I2C_EN = 0; I_{OL} = 3 mA	0		0.4	V
I_{OL}	Low-level output current	I2C_EN = 0; V_{OL} = 0.4 V	20			mA
$I_{I(I2C)}$	Input current on SDA pin	0.1 x $V_{(I2C)}$ < Input voltage < 3.3 V	–10		10	µA
$C_{I(I2C)}$	Input capacitance				10	pF
$C_{(I2C\_FM+\_BUS)}$	I2C bus capacitance for FM+ (1MHz)				150	pF
$C_{(I2C\_FM\_BUS)}$	I2C bus capacitance for FM (400kHz)				150	pF
$R_{(EXT\_I2C\_FM+)}$	External resistors on both SDA and SCL when operating at FM+ (1MHz)	$C_{(I2C\_FM+\_BUS)}$ = 150 pF	620	820	910	Ω
$R_{(EXT\_I2C\_FM)}$	External resistors on both SDA and SCL when operating at FM (400kHz)	$C_{(I2C\_FM\_BUS)}$ = 150 pF	620	1500	2200	Ω

6.7 AC Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
USB Gen 2 Differential Receiver (RX1P/N, RX2P/N, SSTXP/N)						
$V_{(RX\text{-}DIFF\text{-}PP)}$	Input differential peak-peak voltage swing linear dynamic range	AC-coupled differential peak-to-peak signal measured post CTLE through a reference channel		2000		mVpp
$V_{(RX\text{-}DC\text{-}CM)}$	Common-mode voltage bias in the receiver (DC)			0		V
$R_{(RX\text{-}DIFF\text{-}DC)}$	Differential input impedance (DC)	Present after a GEN2 device is detected on TXP/TXN	72		120	Ω
$R_{(RX\text{-}CM\text{-}DC)}$	Receiver DC common mode impedance	Present after a GEN2 device is detected on TXP/TXN	18		30	Ω
$Z_{(RX\text{-}HIGH\text{-}IMP\text{-}DC\text{-}POS)}$	Common-mode input impedance with termination disabled (DC)	Present when no GEN2 device is detected on TXP/TXN. Measured over the range of 0-500mV with respect to GND.	25			kΩ
$V_{(SIGNAL\text{-}DET\text{-}DIFF\text{-}PP)}$	Input differential peak-to-peak signal detect assert level	At 10 Gbps, no input loss, PRBS7 pattern		80		mV
$V_{(RX\text{-}IDLE\text{-}DET\text{-}DIFF\text{-}PP)}$	Input differential peak-to-peak signal detect de-assert Level	At 10 Gbps, no input loss, PRBS7 pattern		60		mV
$V_{(RX\text{-}LFPS\text{-}DET\text{-}DIFF\text{-}PP)}$	Low frequency periodic signaling (LFPS) detect threshold	Below the minimum is squelched	100		300	mV
$V_{(RX\text{-}CM\text{-}AC\text{-}P)}$	Peak RX AC common-mode voltage	Measured at package pin			150	mV
$C_{(RX)}$	RX input capacitance to GND	At 5 GHz		0.5	1	pF
$R_{L(RX\text{-}DIFF)}$	Differential return Loss	50 MHz – 1.25 GHz at 90 Ω		–19		dB
		5 GHz at 90 Ω		–10		dB
$R_{L(RX\text{-}CM)}$	Common-mode return loss	50 MHz – 5 GHz at 90 Ω		–10		dB
$E_{Q(SS\_TX)}$	Receiver equalization for upstream facing port	SSEQ[1:0] at 5 GHz		11		dB
$E_{Q(SS\_RX)}$	Receiver equalization for downstream facing ports	EQ[1:0] at 5 GHz		9		dB
USB Gen 2 Differential Transmitter (TX1P/N, TX2P/N, SSRXP/N)						
$V_{TX(DIFF\text{-}PP)}$	Transmitter dynamic differential voltage swing range.			1600		mV_{PP}
$V_{TX(RCV\text{-}DETECT)}$	Amount of voltage change allowed during receiver detection				600	mV
$V_{TX(CM\text{-}IDLE\text{-}DELTA)}$	Transmitter idle common-mode voltage change while in U2/U3 and not actively transmitting LFPS		–600		600	mV
$V_{TX(DC\text{-}CM)}$	Common-mode voltage bias in the transmitter (DC)			1.75		V
$V_{TX(CM\text{-}AC\text{-}PP\text{-}ACTIVE)}$	Tx AC common-mode voltage active	Max mismatch from Txp + Txn for both time and amplitude			100	mV_{PP}
$V_{TX(IDLE\text{-}DIFF\text{-}AC\text{-}PP)}$	AC electrical idle differential peak-to-peak output voltage	At package pins	0		10	mV
$V_{TX(IDLE\text{-}DIFF\text{-}DC)}$	DC electrical idle differential output voltage	At package pins after low pass filter to remove AC component	0		14	mV
$V_{TX(CM\text{-}DC\text{-}ACTIVE\text{-}IDLE\text{-}DELTA)}$	Absolute DC common-mode voltage between U1 and U0	At package pin			200	mV
$R_{TX(DIFF)}$	Differential impedance of the driver		75		120	Ω
$C_{AC(COUPLING)}$	AC coupling capacitor		75		265	nF
$R_{TX(CM)}$	Common-mode impedance of the driver	Measured with respect to AC ground over 0–500 mV	18		30	Ω
$I_{TX(SHORT)}$	TX short circuit current	TX± shorted to GND			67	mA
$C_{TX(PARASITIC)}$	TX input capacitance for return loss	At package pins, at 5 GHz			1.25	pF
$R_{LTX(DIFF)}$	Differential return loss	50 MHz – 1.25 GHz at 90 Ω		-15		dB
		5 GHz at 90 Ω		-13		dB
$R_{LTX(CM)}$	Common-mode return loss	50 MHz – 5 GHz at 90 Ω		-13		dB
AC Characteristics						
Crosstalk	Differential crosstalk between TX and RX signal pairs	at 5 GHz		–30		dB
$C_{(P1dB\text{-}LF)}$	Low frequency 1-dB compression point	at 100 MHz, 200 mV_{PP} < V_{ID} < 2000 mV_{PP}		1300		mV_{PP}

AC Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$C_{(P1dB-HF)}$	High frequency 1-dB compression point	at 5 GHz, 200 mV_{PP} < V_{ID} < 2000 mV_{PP}		1000		mV_{PP}
f_{LF}	Low frequency cutoff	200 mV_{PP}< V_{ID} < 2000 mV_{PP}		20	50	kHz
	TX output deterministic jitter	200 mV_{PP} < V_{ID} < 2000 mV_{PP}, PRBS7, 10 Gbps		0.11		UIpp
		200 mV_{PP} < V_{ID} < 2000 mV_{PP}, PRBS7, 5 Gbps		0.05		UIpp
	TX output total jitter	200 mV_{PP} < V_{ID} < 2000 mV_{PP}, PRBS7, 10 Gbps		0.15		UIpp
		200 mV_{PP} < V_{ID} < 2000 mV_{PP}, PRBS7, 5 Gbps		0.08		UIpp

6.8 DCI Specific Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DCI_CLK and DCI_DAT LVCMOS Outputs						
V_{OL}	Low-Level output voltage	V_{CC} = 3 V; I_{OL} = 2 mA; C_L = 10 pF			0.45	V
V_{OH}	High-Level output voltage	V_{CC} = 3 V; I_{OL} = –2 mA;	2.4			V
R_{DCI}	Output characteristic impedance		21	25	33	Ω
t_{PERIOD}	DCI Clock period	Measured at 50%	6.67			ns
t_{VALID}	Rising edge of DCI clock to DCI data valid				1	ns
t_{DCI_RISE}	DCI output rise time	Measured at 20% to 80%.	350			ps
t_{DCI_FALL}	DCI output fall time	Measured at 80% to 20%	350			ps

6.9 Timing Requirements

			MIN	NOM	MAX	UNIT
USB Gen 1						
$t_{IDLEEntry}$	Delay from U0 to electrical idle	See Figure 11		10		ns
$t_{IDELExit\_U1}$	U1 exist time: break in electrical idle to the transmission of LFPS	See Figure 11		6		ns
$t_{IDLEExit\_U2U3}$	U2/U3 exit time: break in electrical idle to transmission of LFPS			10		µs
t_{RXDET_INTVL}	RX detect interval while in Disconnect				12	ms
$t_{IDLEExit\_DISC}$	Disconnect Exit Time			10		µs
t_{Exit_SHTDN}	Shutdown Exit Time			1		ms
t_{DIFF_DLY}	Differential Propagation Delay	See Figure 10			300	ps
t_R, t_F	Output Rise/Fall time (see Figure 12)	20%-80% of differential voltage measured 1.7 inch from the output pin		35		ps
t_{RF_MM}	Output Rise/Fall time mismatch	20%-80% of differential voltage measured 1.7 inch from the output pin			2.6	ps

6.10 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I^2C (Refer to Figure 9)						
f_{SCL}	I^2C clock frequency				1	MHz
t_{BUF}	Bus free time between START and STOP conditions		0.5			µs

Switching Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{HDSTA}	Hold time after repeated START condition. After this period, the first clock pulse is generated		0.26			µs
t_{LOW}	Low period of the I^2C clock		0.5			µs
t_{HIGH}	High period of the I^2C clock		0.26			µs
t_{SUSTA}	Setup time for a repeated START condition		0.26			µs
t_{HDDAT}	Data hold time		0			µs
t_{SUDAT}	Data setup time		50			ns
t_R	Rise time of both SDA and SCL signals				120	ns
t_F	Fall time of both SDA and SCL signals		20 × ($V_{(I2C)}$/5.5 V)		120	ns
t_{SUSTO}	Setup time for STOP condition		0.26			µs
C_b	Capacitive load for each bus line				150	pF

6.11 Typical Characteristics

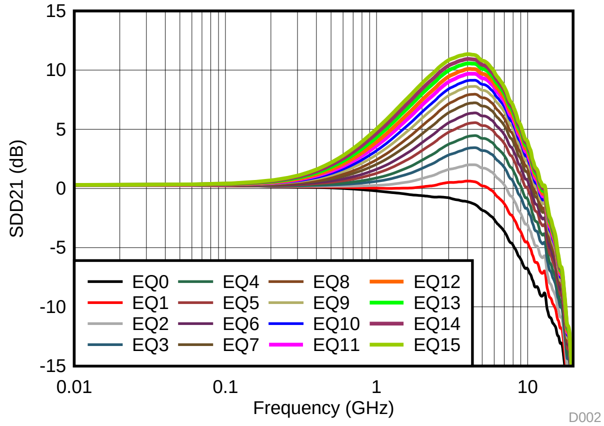


Figure 1. USB RX EQ Settings Curves

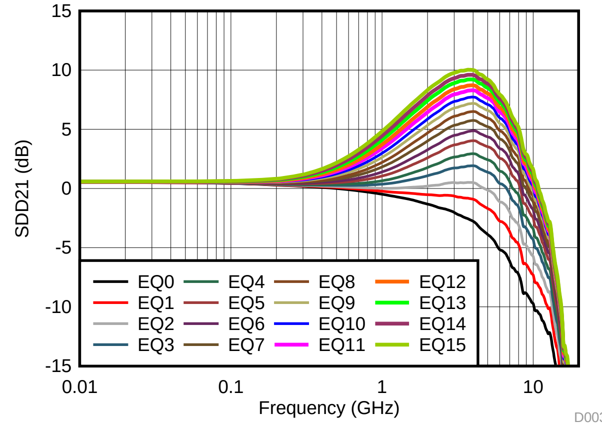


Figure 2. USB TX EQ Settings Curves

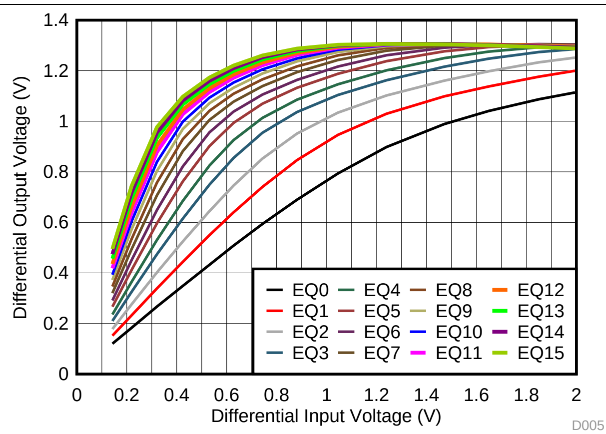


Figure 3. USB TX Linearity Curves at 5 GHz

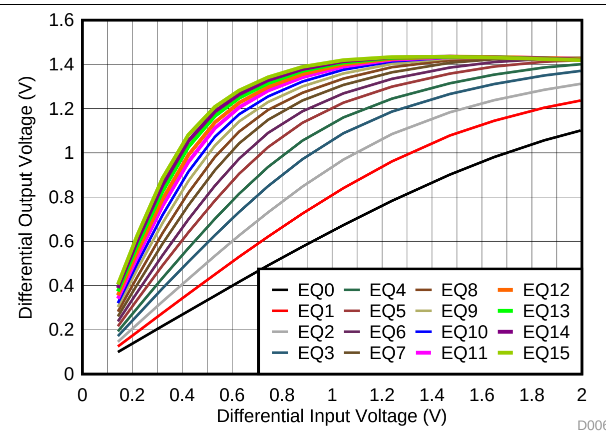


Figure 4. USB RX Linearity Curves at 5 GHz

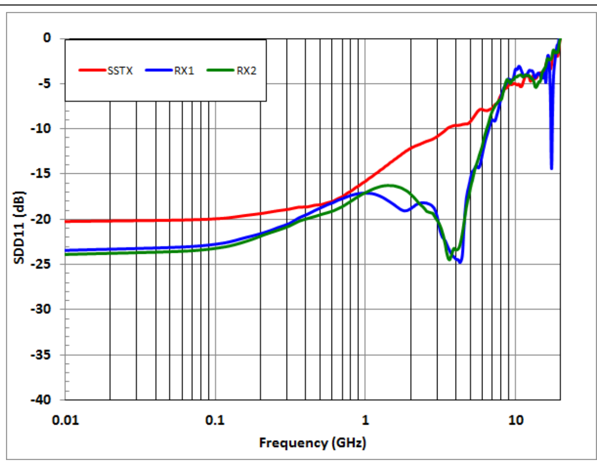


Figure 5. Input Return Loss Performance

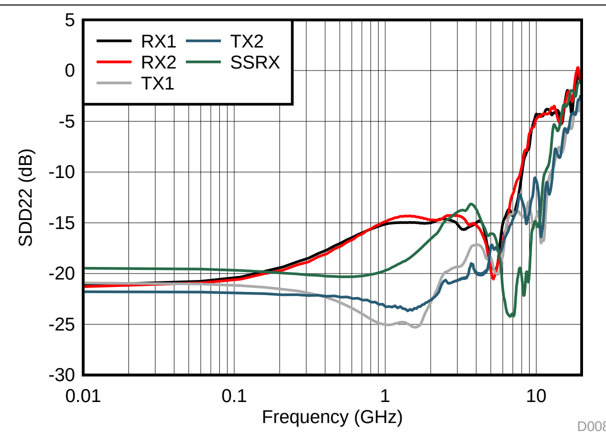


Figure 6. Output Return Loss Performance

Typical Characteristics (continued)

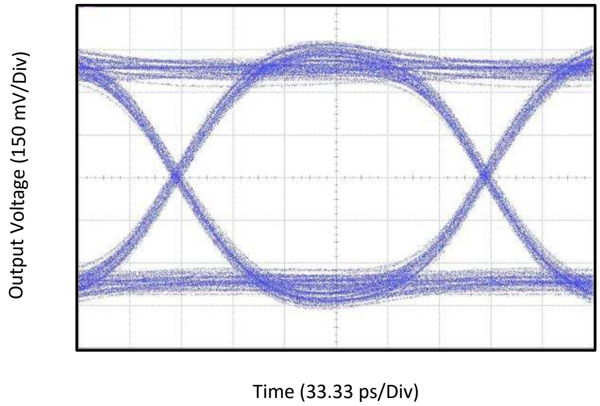


Figure 7. USB 3.1 Gen1 Eye-Pattern Performance with 12-inch Input PCB Trace at 5 Gbps

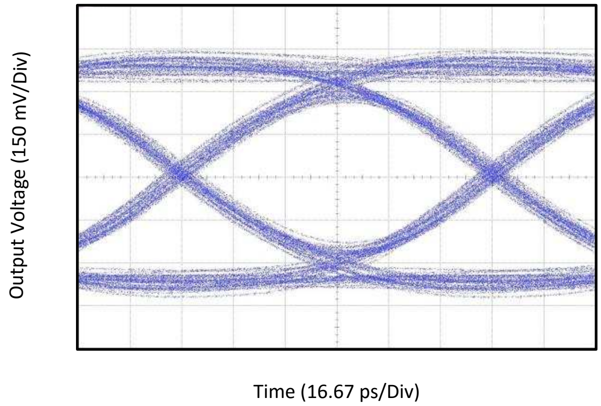


Figure 8. USB 3.1 Gen2 Eye-Pattern Performance with 12-inch Input PCB Trace at 10 Gbps

7 Parameter Measurement Information

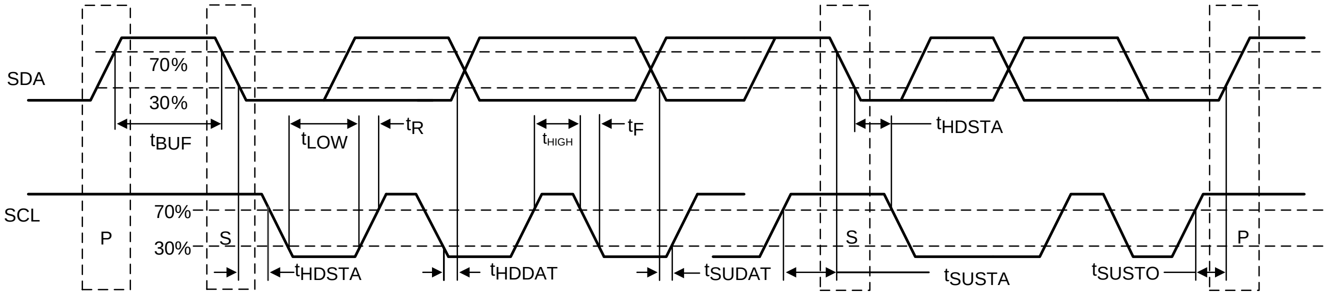


Figure 9. I²C Timing Diagram Definitions

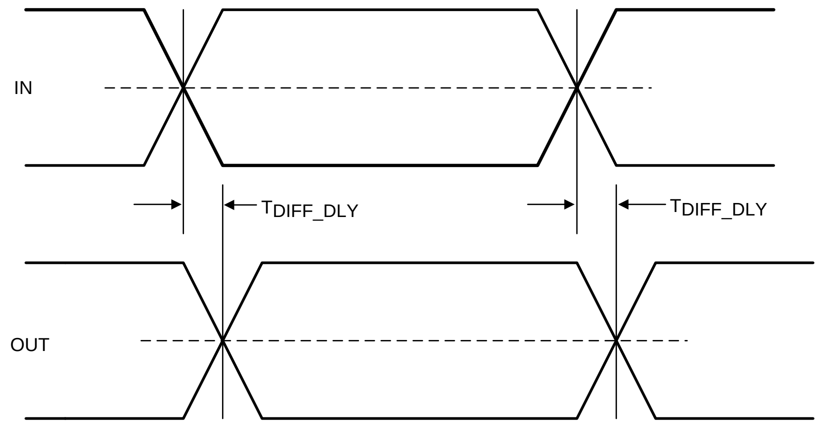


Figure 10. Propagation Delay

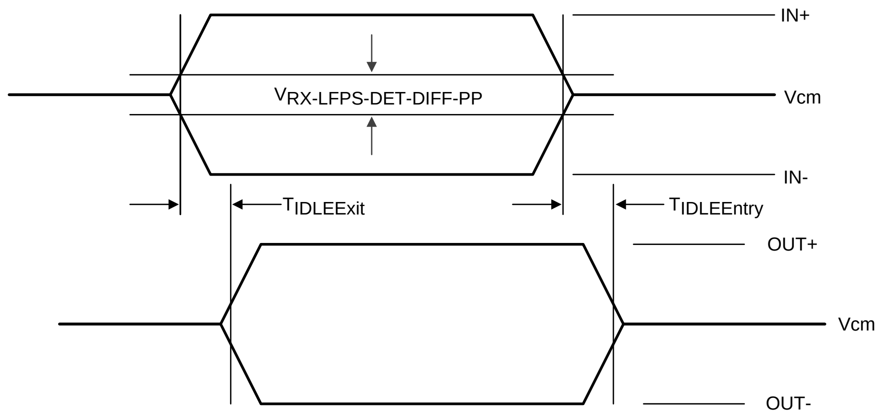


Figure 11. Electrical Idle Mode Exit and Entry Delay

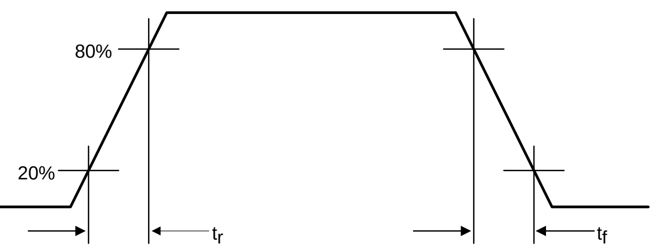


Figure 12. Output Rise and Fall Times

Parameter Measurement Information (continued)

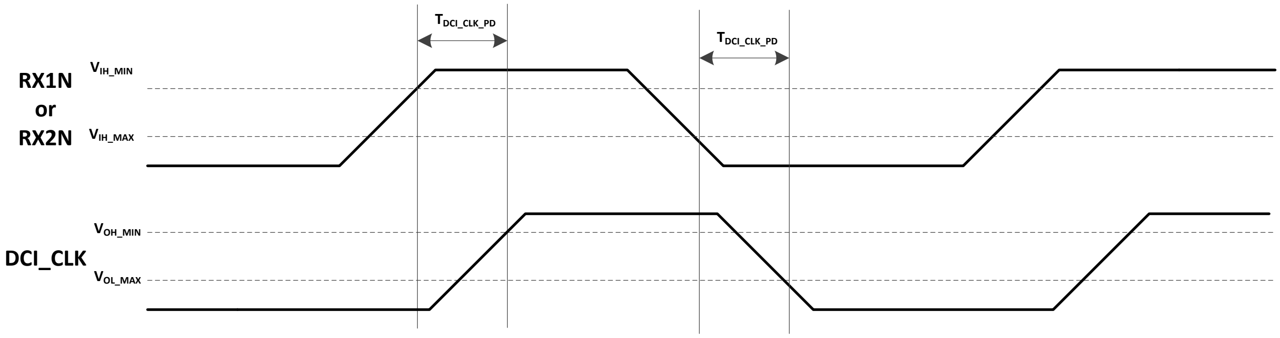


Figure 13. DCI Clock Propagation Delay

8 Detailed Description

8.1 Overview

The TUSB1042I is a USB Type-C redriving switch supporting data rates up to 10 Gbps. This device utilizes 5th generation USB redriver technology.

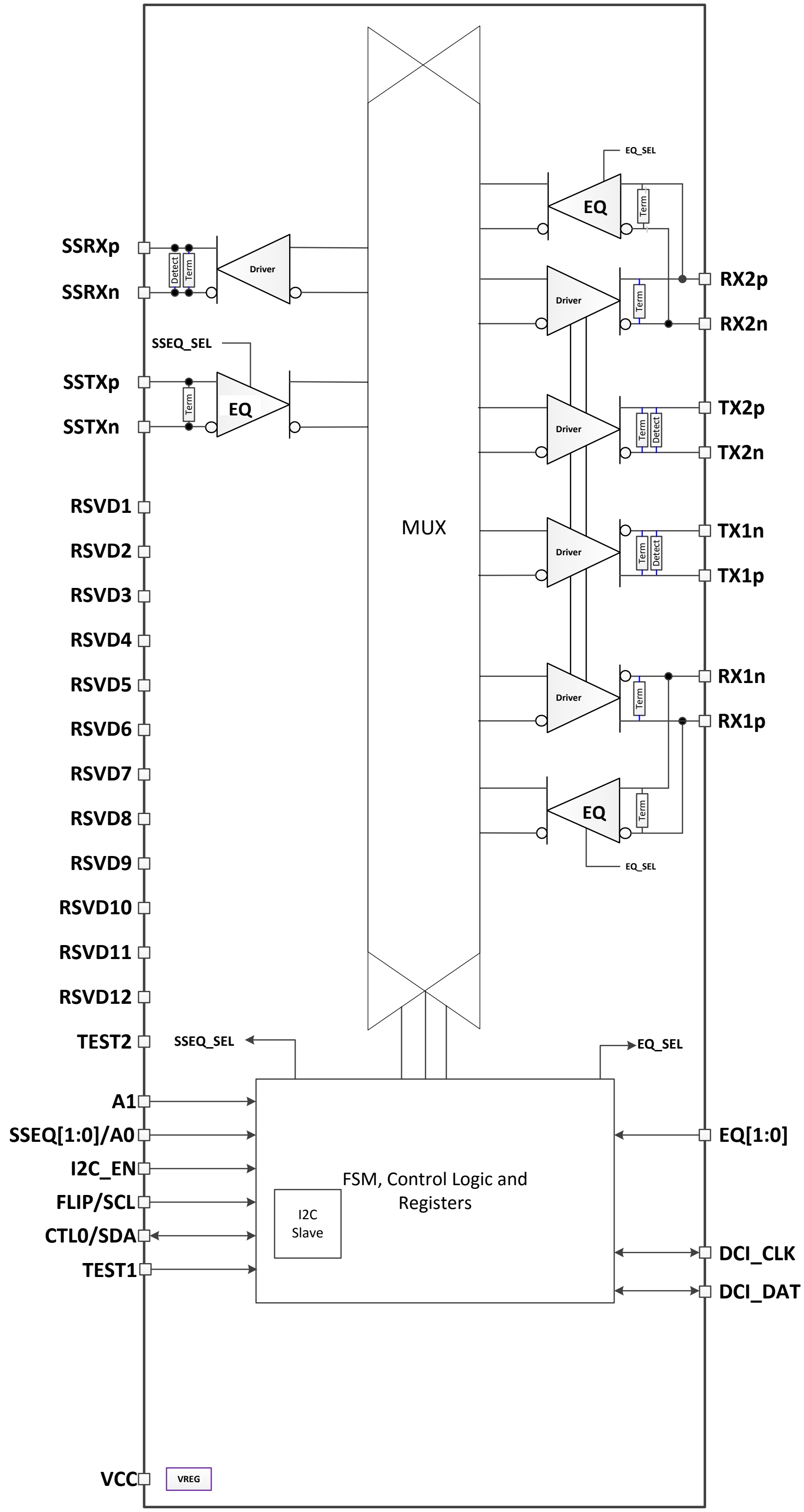
The TUSB1042I provides several levels of receive equalization to compensate for inter-symbol interference (ISI) due to cable and board trace loss when USB 3.1 Gen1/Gen2 signals travel across a PCB or cable. This device requires a 3.3-V power supply. It comes in the industrial temperature range.

For a host or device application the TUSB1042I enables the system to pass both transmitter compliance and receiver jitter tolerance tests for USB 3.1 Gen1/Gen2. The re-driver recovers incoming data by applying equalization that compensates for channel loss, and drives out signals with a high differential voltage. Each channel has a receiver equalizer with selectable gain settings. The equalization should be set based on the amount of insertion loss before or after the TUSB1042I receivers. Independent equalization control for each channel can be set using EQ[1:0] and SSEQ[1:0] pins.

The TUSB1042I advanced state machine makes it transparent to hosts and devices. After power up, the TUSB1042I. periodically performs receiver detection on the TX pairs. If it detects a USB 3.1 Gen1/Gen2 receiver, the RX termination is enabled, and the TUSB1042I is ready to re-drive.

The device ultra-low-power architecture operates at a 3.3-V power supply and achieves enhanced performance. The automatic LFPS de-emphasis control further enables the system to be USB3.1 compliant.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 USB 3.1

The TUSB1042I supports USB 3.1 Gen1/Gen2 data rates up to 10 Gbps. The TUSB1042I supports all the USB defined power states (U0, U1, U2, and U3). Because the TUSB1042I is a linear redriver, it can't decode USB3.1 physical layer traffic. The TUSB1042I monitors the actual physical layer conditions like receiver termination, electrical idle, LFPS, and SuperSpeed signaling rate to determine the USB power state of the USB 3.1 interface.

The TUSB1042I features an intelligent low frequency periodic signaling (LFPS) detector. The LFPS detector automatically senses the low frequency signals and disables receiver equalization functionality. When not receiving LFPS, the TUSB1042I will enable receiver equalization based on the EQ[1:0] and SSEQ[1:0] pins or values programmed into EQ1_SEL, EQ2_SEL, and SSEQ_SEL registers.

8.3.2 4-level Inputs

The TUSB1042I has (I2C_EN, EQ[1:0], and SSEQ[1:0]) 4-level inputs pins that are used to control the equalization gain and place TUSB1042I into different modes of operation. These 4-level inputs utilize a resistor divider to help set the 4 valid levels and provide a wider range of control settings. There is an internal 30 kΩ pull-up and a 94 kΩ pull-down. These resistors, together with the external resistor connection combine to achieve the desired voltage level.

Table 1. 4-Level Control Pin Settings

LEVEL	SETTINGS
0	Option 1: Tie 1 KΩ 5% to GND. Option 2: Tie directly to GND.
R	Tie 20 KΩ 5% to GND.
F	Float (leave pin open)
1	Option 1: Tie 1 KΩ 5%to V_{CC}. Option 2: Tie directly to V_{CC}.

NOTE

All four-level inputs are latched on rising edge of internal reset. After t_{cfg_hd}, the internal pull-up and pull-down resistors will be isolated in order to save power.

8.3.3 Receiver Linear Equalization

The purpose of receiver equalization is to compensate for channel insertion loss and inter-symbol interference in the system before the input or after the output of the TUSB1042I. The receiver overcomes these losses by attenuating the low frequency components of the signals with respect to the high frequency components. The proper gain setting should be selected to match the channel insertion loss. Two 4-level input pins enable up to 16 possible equalization settings. USB3.1 upstream path and USB3.1 downstream path each have their own two 4-level inputs. The TUSB1042I also provides the flexibility of adjusting settings through I^2C registers.

8.4 Device Functional Modes

8.4.1 Device Configuration in GPIO Mode

The TUSB1042I is in GPIO configuration when I2C_EN = “0”. The TUSB1042I supports USB 3.1 operation. The TEST1 pin needs to be pulled down to GND. CTL0 pins enables or disables USB 3.1 operation as detailed in Table 2.

After power-up (V_{CC} from 0 V to 3.3 V), the TUSB1042I defaults to USB3.1 mode. The USB PD controller upon detecting no device attached to Type-C port or USB3.1 operation not required by attached device must take TUSB1042I out of USB3.1 mode by transitioning the CTL0 pin from L to H and back to L.

Table 2. GPIO Configuration Control

CTL0 PIN	FLIP PIN	TUSB1042I CONFIGURATION
L	L	Power Down
L	H	Power Down
H	L	One Port USB 3.1 - No Flip
H	H	One Port USB 3.1 – With Flip

Table 3 Details the TUSB1042I’s mux routing. This table is valid for both I^2C and GPIO configuration modes.

Table 3. INPUT to OUTPUT Mapping

CTL0 PIN	FLIP PIN	FROM INPUT PIN	TO OUTPUT PIN
L	L	NA	NA
L	H	NA	NA
H	L	RX1P	SSRXP
		RX1N	SSRXN
		SSTXP	TX1P
		SSTXN	TX1N
H	H	RX2P	SSRXP
		RX2N	SSRXN
		SSTXP	TX2P
		SSTXN	TX2P

8.4.2 Device Configuration In I^2C Mode

The TUSB1042I is in I^2C mode when I2C_EN is not equal to “0”. The same configurations defined in GPIO mode are also available in I^2C mode. The TUSB1042I USB3.1 configuration is controlled based on Table 4.

Table 4. I^2C Configuration Control

REGISTERS			TUSB1042I CONFIGURATION
CTLSEL1	CTLSEL0	FLIPSEL	
0	0	0	Power Down
0	0	1	Power Down
0	1	0	USB 3.1 - No Flip
0	1	1	USB 3.1 – With Flip
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

8.4.3 Linear EQ Configuration

Each of the TUSB1042I receiver lanes has individual controls for receiver equalization. The receiver equalization gain value can be controlled either through I²C registers or through GPIOs. Table 5 details the gain value for each available combination when TUSB1042I is in GPIO mode. These same options are also available in I²C mode by updating registers EQ1_SEL, EQ2_SEL, and SSEQ_SEL.

Table 5. TUSB1042I Receiver Equalization GPIO Control

Equalization Setting #	USB3.1 DOWNSTREAM FACING PORTS			USB 3.1 UPSTREAM FACING PORT		
	EQ1 PIN LEVEL	EQ0 PIN LEVEL	EQ GAIN at 5 GHz (dB)	SSEQ1 PIN LEVEL	SSEQ0 PIN LEVEL	EQ GAIN at 5 GHz (dB)
0	0	0	-3.9	0	0	-1.8
1	0	R	-1.7	0	R	0.2
2	0	F	-0.1	0	F	1.7
3	0	1	1.4	0	1	3.2
4	R	0	2.4	R	0	4.2
5	R	R	3.5	R	R	5.3
6	R	F	4.4	R	F	6.1
7	R	1	5.2	R	1	7.0
8	F	0	5.9	F	0	7.7
9	F	R	6.6	F	R	8.3
10	F	F	7.1	F	F	8.8
11	F	1	7.6	F	1	9.3
12	1	0	8.0	1	0	9.7
13	1	R	8.5	1	R	10.1
14	1	F	8.8	1	F	10.4
15	1	1	9.2	1	1	10.8

8.4.4 USB3.1 Modes

The TUSB1042I monitors the physical layer conditions like receiver termination, electrical idle, LFPS, and SuperSpeed signaling rate to determine the state of the USB3.1 interface. Depending on the state of the USB 3.1 interface, the TUSB1042I can be in one of four primary modes of operation when USB 3.1 is enabled (CTL0 = H or CTLSEL0 = 1b1): Disconnect, U2/U3, U1, and U0.

The Disconnect mode is the state in which TUSB1042I has not detected far-end termination on both upstream facing port (UFP) or downstream facing port (DFP). The disconnect mode is the lowest power mode of each of the four modes. The TUSB1042I remains in this mode until far-end receiver termination has been detected on both UFP and DFP. The TUSB1042I immediately exits this mode and enter U0 once far-end termination is detected.

Once in U0 mode, the TUSB1042I will redrive all traffic received on UFP and DFP. U0 is the highest power mode of all USB3.1 modes. The TUSB1042I remains in U0 mode until electrical idle occurs on both UFP and DFP. Upon detecting electrical idle, the TUSB1042I immediately transitions to U1.

The U1 mode is the intermediate mode between U0 mode and U2/U3 mode. In U1 mode, the TUSB1042I UFP and DFP receiver termination remains enabled. The UFP and DFP transmitter DC common mode is maintained. The power consumption in U1 is similar to power consumption of U0.

Next to the disconnect mode, the U2/U3 mode is next lowest power state. While in this mode, the TUSB1042I periodically performs far-end receiver detection. Anytime the far-end receiver termination is not detected on either UFP or DFP, the TUSB1042I leaves the U2/U3 mode and transitions to the Disconnect mode. It also monitors for a valid LFPS. Upon detection of a valid LFPS, the TUSB1042I immediately transitions to the U0 mode. In U2/U3 mode, the TUSB1042I receiver terminations remain enabled but the TX DC common mode voltage is not maintained.

8.4.5 Operation Timing – Power Up

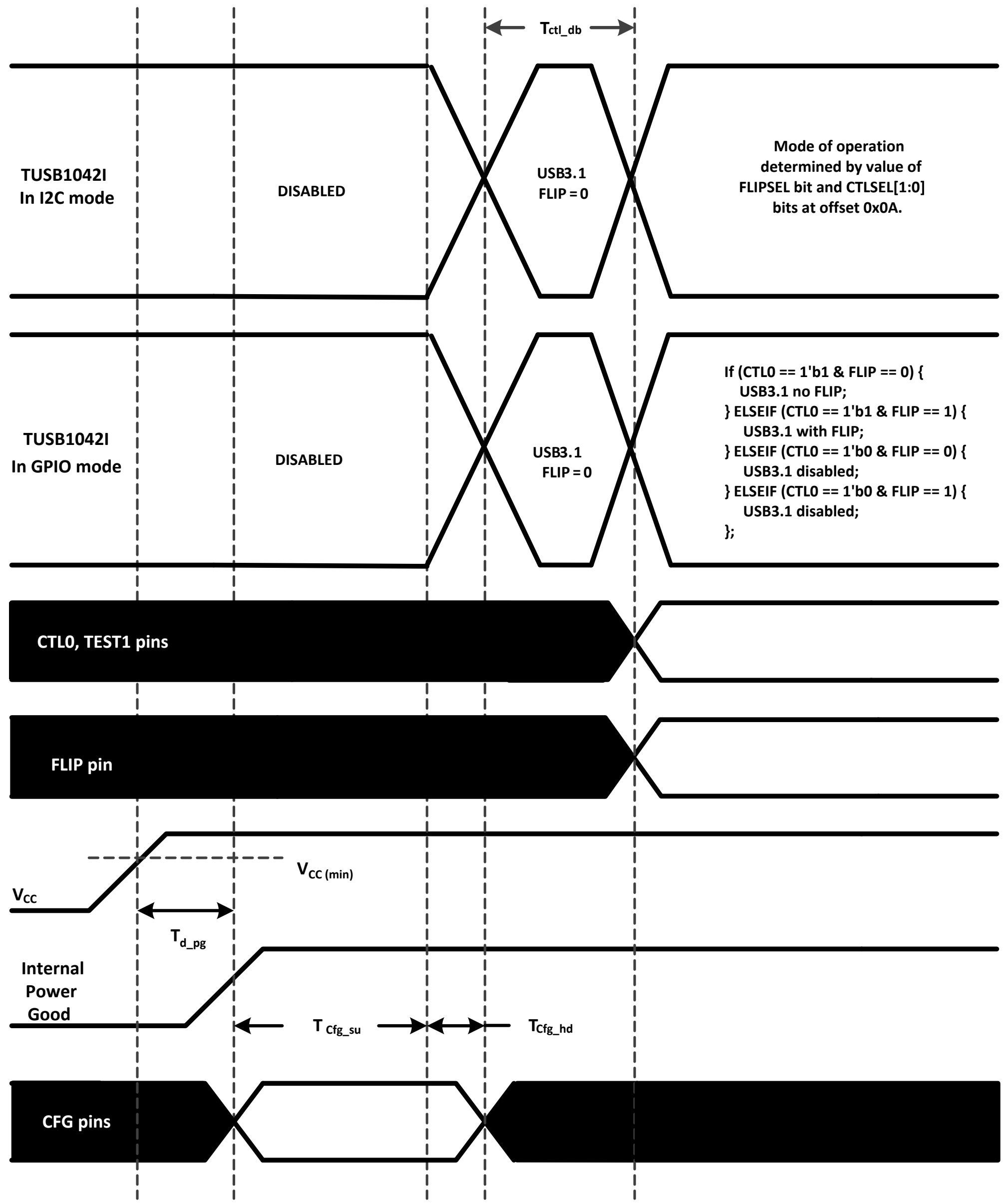


Figure 14. Power-Up Timing

Table 6. Power-Up Timing(1)(2)

PARAMETER		MIN	MAX	UNIT
t_{d_pg}	V_{CC} (minimum) to Internal Power Good asserted high		500	µs
t_{cfg_su}	CFG(1) pins setup(2)	250		µs
t_{cfg_hd}	CFG(1) pins hold	10		µs
t_{CTL_DB}	TEST1, CTL0 and FLIP pin debounce		16	ms
t_{VCC_RAMP}	VCC supply ramp requirement		100	ms

(1) Following pins comprise CFG pins: I2C_EN, EQ[1:0], and SSEQ[1:0].
(2) Recommend CFG pins are stable when V_{CC} is at min.

8.5 Programming

For further programmability, the TUSB1042I can be controlled using I²C. The SCL and SDA pins are used for I²C clock and I²C data respectively.

Table 7. TUSB1042I I²C Target Address

A1 PIN LEVEL	SSEQ0/A0 PIN LEVEL	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (W/R)
0	0	1	0	0	0	1	0	0	0/1
0	R	1	0	0	0	1	0	1	0/1
0	F	1	0	0	0	1	1	0	0/1
0	1	1	0	0	0	1	1	1	0/1
R	0	0	1	0	0	0	0	0	0/1
R	R	0	1	0	0	0	0	1	0/1
R	F	0	1	0	0	0	1	0	0/1
R	1	0	1	0	0	0	1	1	0/1
F	0	0	0	1	0	0	0	0	0/1
F	R	0	0	1	0	0	0	1	0/1
F	F	0	0	1	0	0	1	0	0/1
F	1	0	0	1	0	0	1	1	0/1
1	0	0	0	0	1	1	0	0	0/1
1	R	0	0	0	1	1	0	1	0/1
1	F	0	0	0	1	1	1	0	0/1
1	1	0	0	0	1	1	1	1	0/1

The following procedure should be followed to write to TUSB1042I I²C registers:

1. The master initiates a write operation by generating a start condition (S), followed by the TUSB1042I 7-bit address and a zero-value “W/R” bit to indicate a write cycle.
2. The TUSB1042I acknowledges the address cycle.
3. The master presents the sub-address (I²C register within TUSB1042I) to be written, consisting of one byte of data, MSB-first.
4. The TUSB1042I acknowledges the sub-address cycle.
5. The master presents the first byte of data to be written to the I²C register.
6. The TUSB1042I acknowledges the byte transfer.
7. The master may continue presenting additional bytes of data to be written, with each byte transfer completing with an acknowledge from the TUSB1042I.
8. The master terminates the write operation by generating a stop condition (P).

The following procedure should be followed to read the TUSB1042I I²C registers:

1. The master initiates a read operation by generating a start condition (S), followed by the TUSB1042I 7-bit address and a one-value “W/R” bit to indicate a read cycle.
2. The TUSB1042I acknowledges the address cycle.
3. The TUSB1042I transmit the contents of the memory registers MSB-first starting at register 00h or last read sub-address+1. If a write to the T I²C register occurred prior to the read, then the TUSB1042I shall start at the sub-address specified in the write.
4. The TUSB1042I shall wait for either an acknowledge (ACK) or a not-acknowledge (NACK) from the master after each byte transfer; the I²C master acknowledges reception of each data byte transfer.
5. If an ACK is received, the TUSB1042I transmits the next byte of data.
6. The master terminates the read operation by generating a stop condition (P).

The following procedure should be followed for setting a starting sub-address for I²C reads:

1. The master initiates a write operation by generating a start condition (S), followed by the TUSB1042I 7-bit address and a zero-value “W/R” bit to indicate a write cycle.
2. The TUSB1042I acknowledges the address cycle.
3. The master presents the sub-address (I²C register within TUSB1042I) to be written, consisting of one byte of data, MSB-first.

4. The TUSB1042I acknowledges the sub-address cycle.
5. The master terminates the write operation by generating a stop condition (P).

NOTE

If no sub-addressing is included for the read procedure, and reads start at register offset 00h and continue byte by byte through the registers until the I^2C master terminates the read operation. If a I^2C address write occurred prior to the read, then the reads start at the sub-address specified by the address write.

Table 8. Register Legend

ACCESS TAG	NAME	MEANING
R	Read	The field may be read by software
W	Write	The field may be written by software
S	Set	The field may be set by a write of one. Writes of zeros to the field have no effect.
C	Clear	The field may be cleared by a write of one. Write of zero to the field have no effect.
U	Update	Hardware may autonomously update this field.
NA	No Access	Not accessible or not applicable

8.6 Register Maps

8.6.1 General Register (address = 0x0A) [reset = 00000001]

Figure 15. General Registers

7	6	5	4	3	2	1	0
Reserved		Reserved	EQ_OVERRIDE	Reserved	FLIPSEL	CTLSEL[1:0].	
R		R/W	R/W	R/W	R/W	R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9. General Registers

Bit	Field	Type	Reset	Description
7:6	Reserved	R	00	Reserved.
5	Reserved	R	0	Reserved.
4	EQ_OVERRIDE	R/W	0	Setting of this field will allow software to use EQ settings from registers instead of value sample from pins. 0 – EQ settings based on sampled state of the EQ pins (SSEQ[1:0], EQ[1:0], and DPEQ[1:0]). 1 – EQ settings based on programmed value of each of the EQ registers
3	Reserved	R	0	Reserved.
2	FLIPSEL	R/W	0	FLIPSEL. Refer to Table 4 for this field functionality.
1:0	CTLSEL[1:0].	R/W	01	00 – Disabled. All RX and TX for USB3 are disabled. 01 – USB3.1 enabled. (Default) 10 – Reserved. 11 – Reserved.

8.6.2 USB3.1 Control/Status Registers (address = 0x20) [reset = 00000000]

Figure 16. USB3.1 Control/Status Registers (0x20)

7	6	5	4	3	2	1	0
EQ2_SEL				EQ1_SEL			
R/W/U				R/W/U			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 10. USB3.1 Control/Status Registers (0x20)

Bit	Field	Type	Reset	Description
7:4	EQ2_SEL	R/W/U	0000	Field selects between 0 to 9 dB of EQ for USB3.1 RX2 receiver. When EQ_OVERRIDE = 1'b0, this field reflects the sampled state of EQ[1:0] pins. When EQ_OVERRIDE = 1'b1, software can change the EQ setting for USB3.1 RX2 receiver based on value written to this field.
3:0	EQ1_SEL	R/W/U	0000	Field selects between 0 to 9 dB of EQ for USB3.1 RX1 receiver. When EQ_OVERRIDE = 1'b0, this field reflects the sampled state of EQ[1:0] pins. When EQ_OVERRIDE = 1'b1, software can change the EQ setting for USB3.1 RX1 receiver based on value written to this field.

8.6.3 USB3.1 Control/Status Registers (address = 0x21) [reset = 00000000]

Figure 17. USB3.1 Control/Status Registers (0x21)

7	6	5	4	3	2	1	0
Reserved				SSEQ_SEL			
R				R/W/U			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 11. USB3.1 Control/Status Registers (0x21)

Bit	Field	Type	Reset	Description
7:4	Reserved	R	0000	Reserved
3:0	SSEQ_SEL	R/W/U	0000	Field selects between 0 to 11 dB of EQ for USB3.1 SSTXP/N receiver. When EQ_OVERRIDE = 1'b0, this field reflects the sampled state of SSEQ[1:0] pins. When EQ_OVERRIDE = 1'b1, software can change the EQ setting for USB3.1 SSTXP/N receiver based on value written to this field.

8.6.4 USB3.1 Control/Status Registers (address = 0x22) [reset = 00000100]

Figure 18. USB3.1 Control/Status Registers (0x22)

7	6	5	4	3	2	1	0
CM_ACTIVE	LFPS_EQ	U2U3_LFPS_DEBOUNCE	DISABLE_U2U3_RXDET	DFP_RXDET_INTERVAL		USB3_COMPLIANCE_CTRL	
R/U	R/W	R/W	R/W	R/W		R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 12. USB3.1 Control/Status Registers (0x22)

Bit	Field	Type	Reset	Description
7	CM_ACTIVE	R/U	0	0 –device not in USB 3.1 compliance mode. (Default) 1 –device in USB 3.1 compliance mode
6	LFPS_EQ	R/W	0	Controls whether settings of EQ based on EQ1_SEL, EQ2_SEL and SSEQ_SEL applies to received LFPS signal. 0 – EQ set to zero when receiving LFPS (default) 1 – EQ set to EQ1_SEL, EQ2_SEL, and SSEQ_SEL when receiving LFPS.
5	U2U3_LFPS_DEBOUNCE	R/W	0	0 – No debounce of LFPS before U2/U3 exit. (Default) 1 – 200 µs debounce of LFPS before U2/U3 exit.
4	DISABLE_U2U3_RXDET	R/W	0	0 – Rx.Detect in U2/U3 enabled. (Default) 1 – Rx.Detect in U2/U3 disabled.
3:2	DFP_RXDET_INTERVAL	R/W	01	This field controls the Rx.Detect interval for the Downstream facing port (TX1P/N and TX2P/N). 00 – 8 ms 01 – 12 ms (default) 10 – 48 ms 11 – 96 ms
1:0	USB3_COMPLIANCE_CTRL	R/W	00	00 – FSM determined compliance mode. (Default) 01 – Compliance Mode enabled in DFP direction (SSTX -> TX1/TX2) 10 – Compliance Mode enabled in UFP direction (RX1/RX2 -> SSRX) 11 – Compliance Mode Disabled.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TUSB1042I is a linear redriver switch designed specifically to compensate for intersymbol interference (ISI) jitter caused by signal attenuation through a passive medium like PCB traces and cables. Because the TUSB1042I has one upstream facing USB 3.1 Gen1/Gen2 input, and two downstream facing USB 3.1 Gen1/Gen2 inputs, it can be optimized to correct ISI on all those three inputs through 16 different equalization choices. Placing the TUSB1042I between a USB3.1 Host and a USB3.1 Type-C receptacle can correct signal integrity issues resulting in a more robust system.

9.2 Typical Application

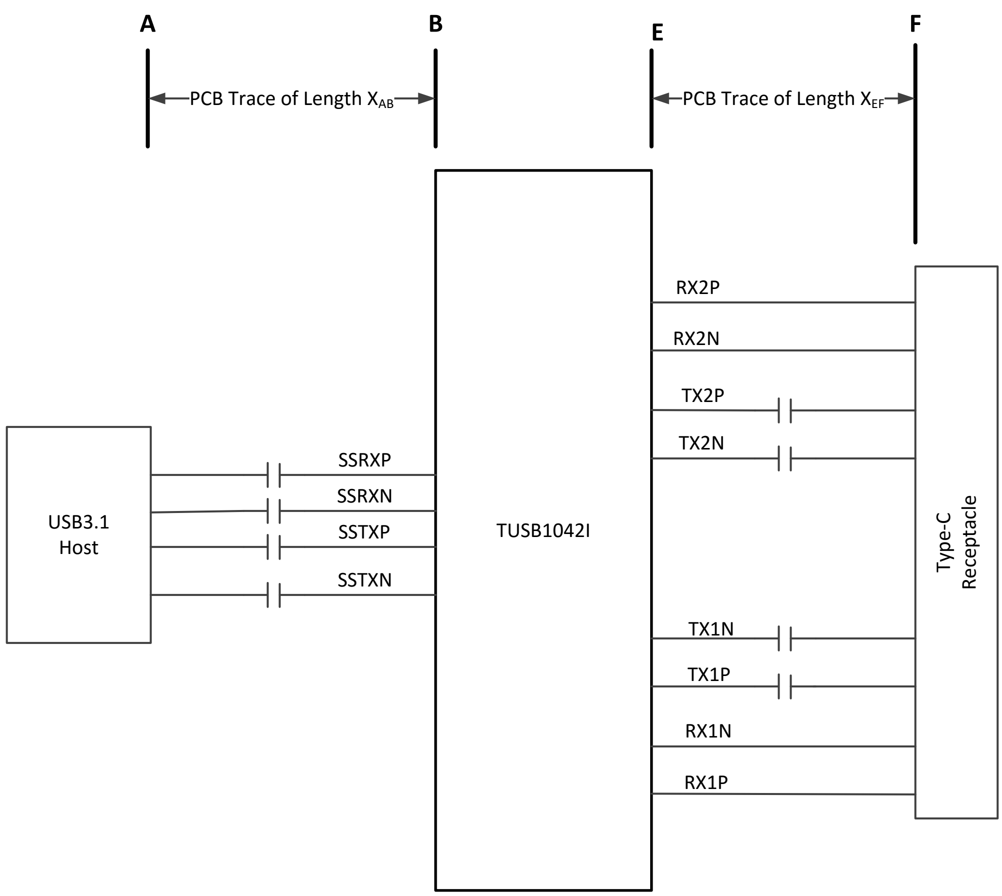


Figure 19. TUSB1042I in a Host Application

Typical Application (continued)

9.2.1 Design Requirements

For this design example, use the parameters shown in Table 13.

Table 13. Design Parameters

PARAMETER	VALUE
A to B PCB trace length, X_{AB}	12 inches
E to F PCB trace length, X_{EF}	2 inches
PCB trace width	4 mils
AC-coupling capacitor (75 nF to 265 nF)	100 nF
VCC supply (3 V to 3.6 V)	3.3 V
I2C Mode or GPIO Mode	I2C Mode. (I2C_EN pin != "0")
1.8V or 3.3V I2C Interface	3.3V I2C. Pull-up the I2C_EN pin to 3.3V with a 1K ohm resistor.

9.2.2 Detailed Design Procedure

A typical usage of the TUSB1042I device is shown in Figure 20. The device can be controlled either through its GPIO pins or through its I^2C interface. In the example shown below, a Type-C PD controller is used to configure the device through the I^2C interface. When configured for I2C mode, pins 29 (DCI_DAT) and 32 (DCI_CLK) can be used for the DCI interface. In I2C mode, the equalization settings for each receiver can be independently controlled through I2C registers. For this reason, all of the equalization pins (EQ[1:0] and SSEQ[1:0]) can be left unconnected. If these pins are left unconnected, the TUSB1042I 7-bit I2C slave address will be 0x12 because both A1 and SSEQ0/A0 will be at pin level "F". If a different I2C slave address is desired, A1 and SSEQ0/A0 pins should be set to a level which produces the desired I2C slave address.

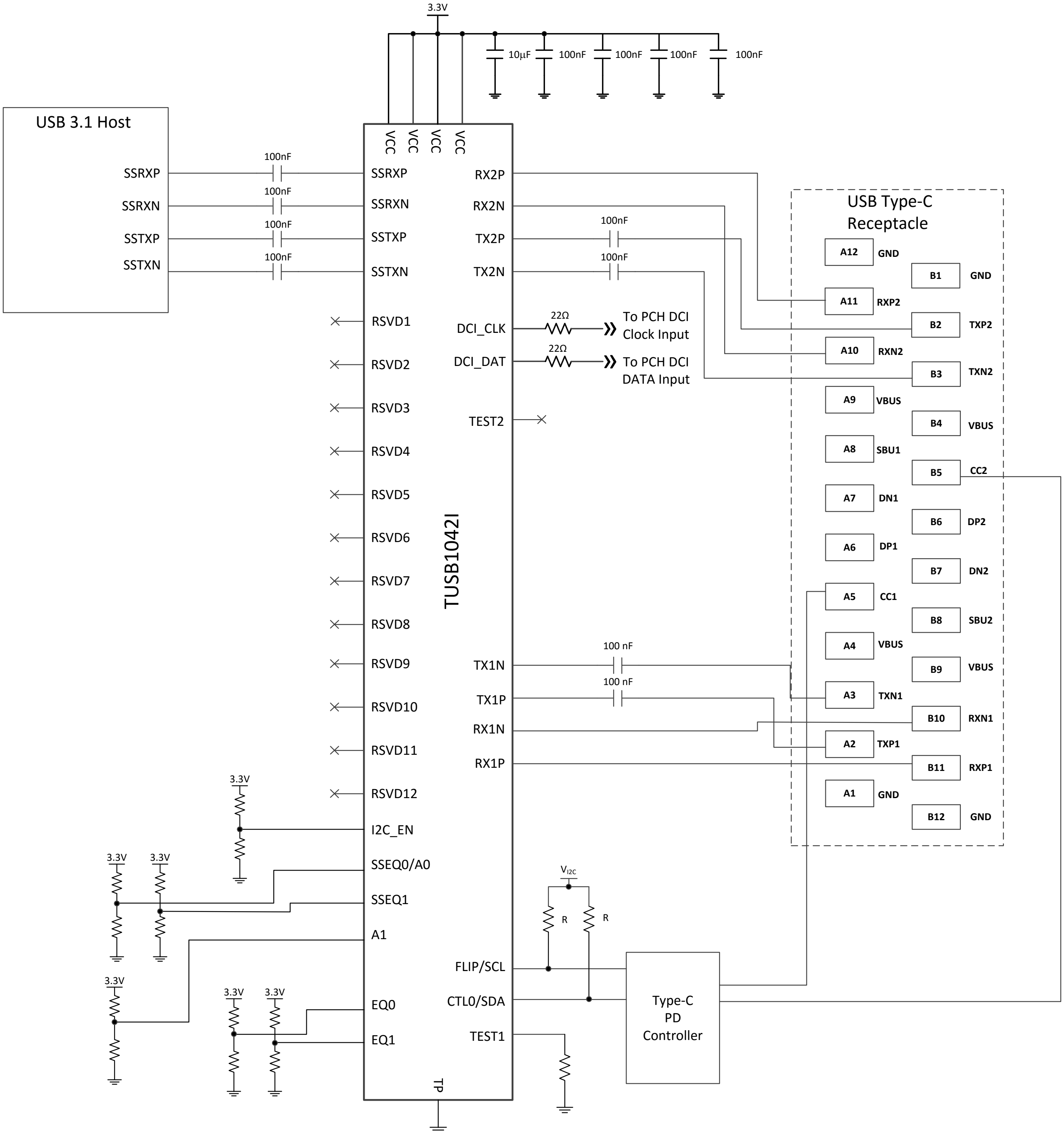


Figure 20. Application Circuit

9.2.3 Application Curve

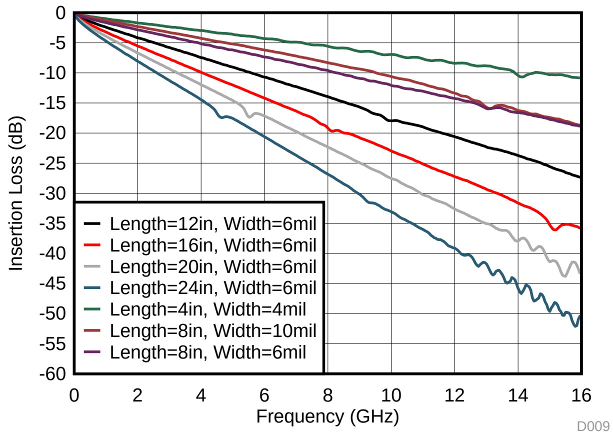


Figure 21. Insertion Loss of FR4 PCB Traces

9.3 System Examples

9.3.1 USB 3.1

The TUSB1042I is in USB3.1 mode when the CTL0 pin is high.

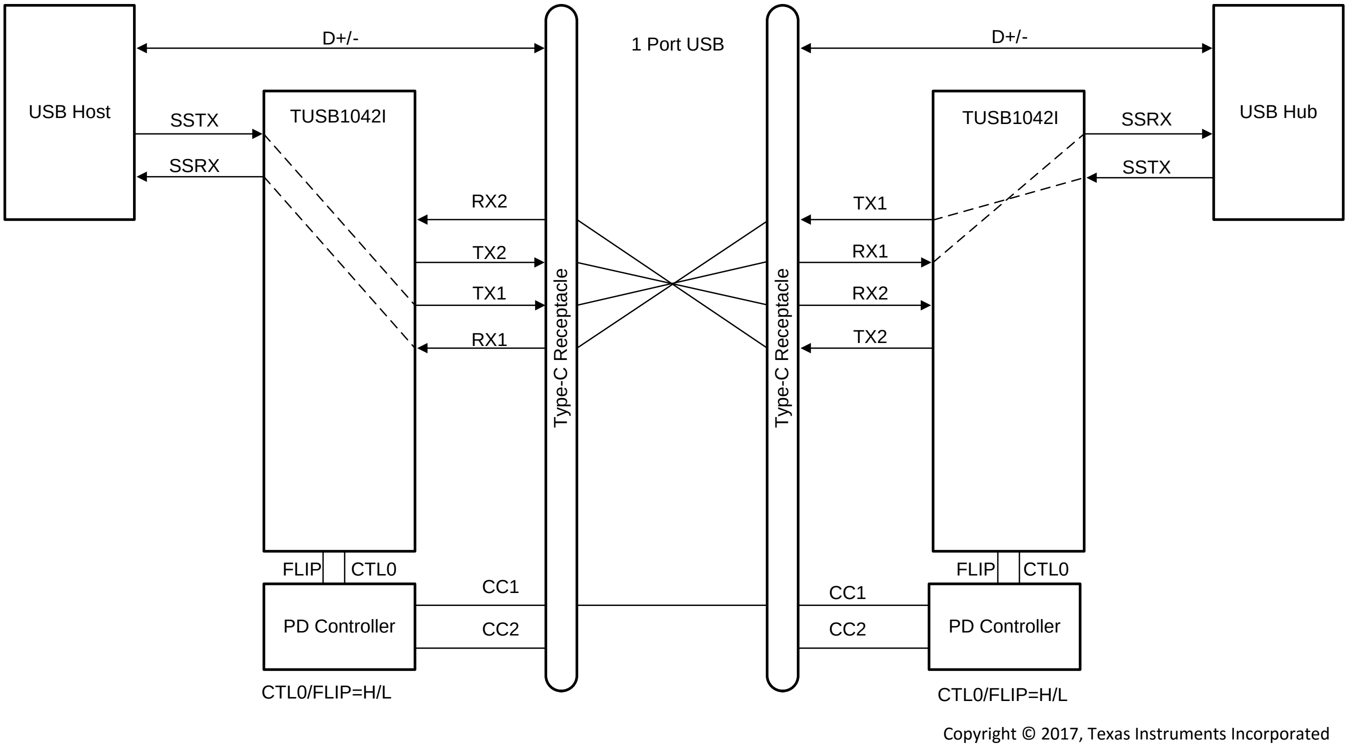


Figure 22. USB3.1 – No Flip (CTL0 = H, FLIP = L)

System Examples (continued)

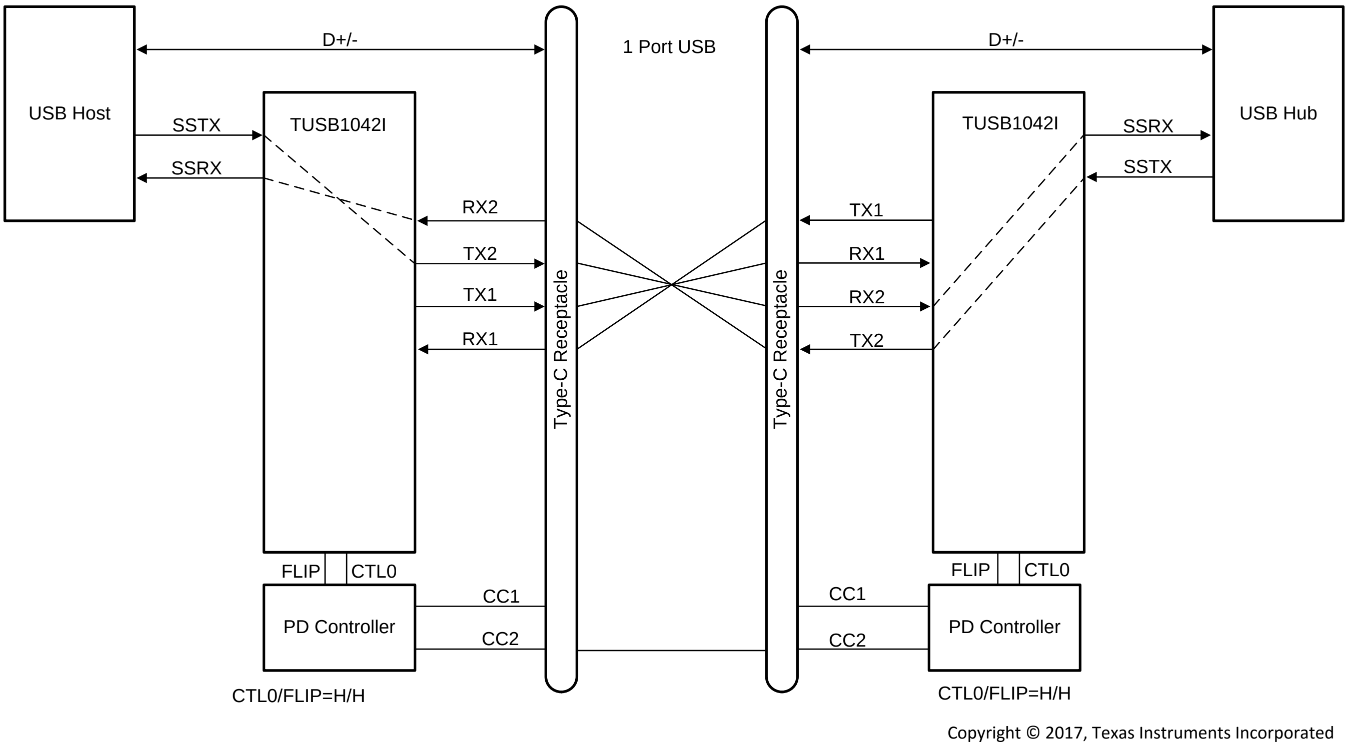


Figure 23. USB3.1 – With Flip (CTL0 = H, FLIP = H)

10 Power Supply Recommendations

The TUSB1042I is designed to operate with a 3.3-V power supply. Levels above those listed in the *Absolute Maximum Ratings* table should not be used. If using a higher voltage system power supply, a voltage regulator can be used to step down to 3.3 V. Decoupling capacitors should be used to reduce noise and improve power supply integrity. A 0.1-µF capacitor should be used on each power pin.

11 Layout

11.1 Layout Guidelines

1. RXP/N and TXP/N pairs should be routed with controlled 90-Ω differential impedance (±15%).
2. Keep away from other high speed signals.
3. Intra-pair routing should be kept to within 2 mils.
4. Length matching should be near the location of mismatch.
5. Each pair should be separated at least by 3 times the signal trace width.
6. The use of bends in differential traces should be kept to a minimum. When bends are used, the number of left and right bends should be as equal as possible and the angle of the bend should be ≥ 135 degrees. This will minimize any length mismatch causes by the bends and therefore minimize the impact bends have on EMI.
7. Route all differential pairs on the same of layer.
8. The number of vias should be kept to a minimum. It is recommended to keep the vias count to 2 or less.
9. Keep traces on layers adjacent to ground plane.
10. Do not route differential pairs over any plane split.
11. Adding Test points will cause impedance discontinuity, and therefore, negatively impact signal performance. If test points are used, they should be placed in series and symmetrically. They must not be placed in a manner that causes a stub on the differential pair.

11.2 Layout Example

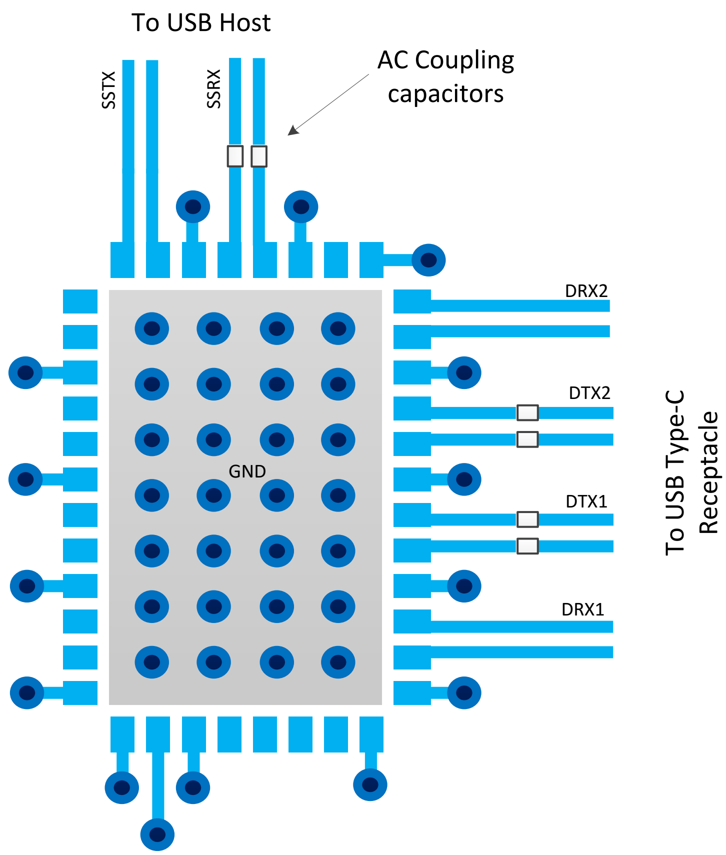


Figure 24. Layout Example

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 14. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TUSB1042I	Click here	Click here	Click here	Click here	Click here

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
USB Type-C is a trademark of USB Implementers Forum.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TUSB1042IRNQR	Active	Production	WQFN (RNQ) | 40	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	T1042
TUSB1042IRNQR.B	Active	Production	WQFN (RNQ) | 40	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	T1042
TUSB1042IRNQRG4	Active	Production	WQFN (RNQ) | 40	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	T1042
TUSB1042IRNQRG4.B	Active	Production	WQFN (RNQ) | 40	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	T1042
TUSB1042IRNQT	Active	Production	WQFN (RNQ) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	T1042
TUSB1042IRNQT.B	Active	Production	WQFN (RNQ) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	T1042

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

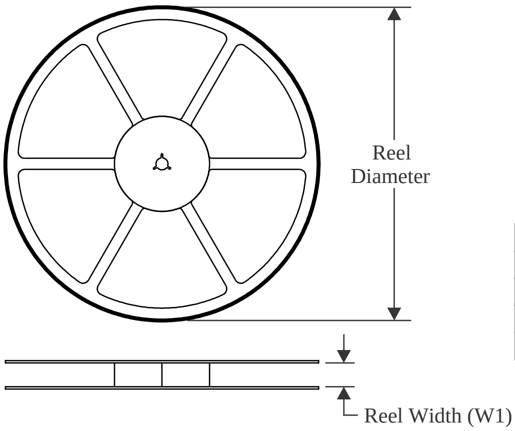
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

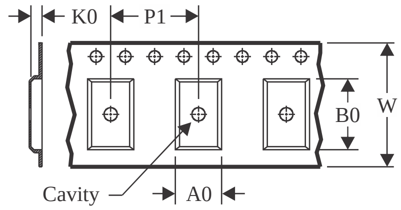
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

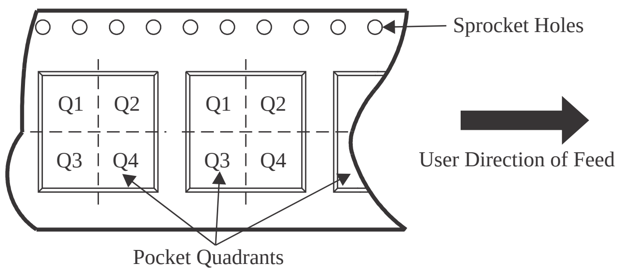


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

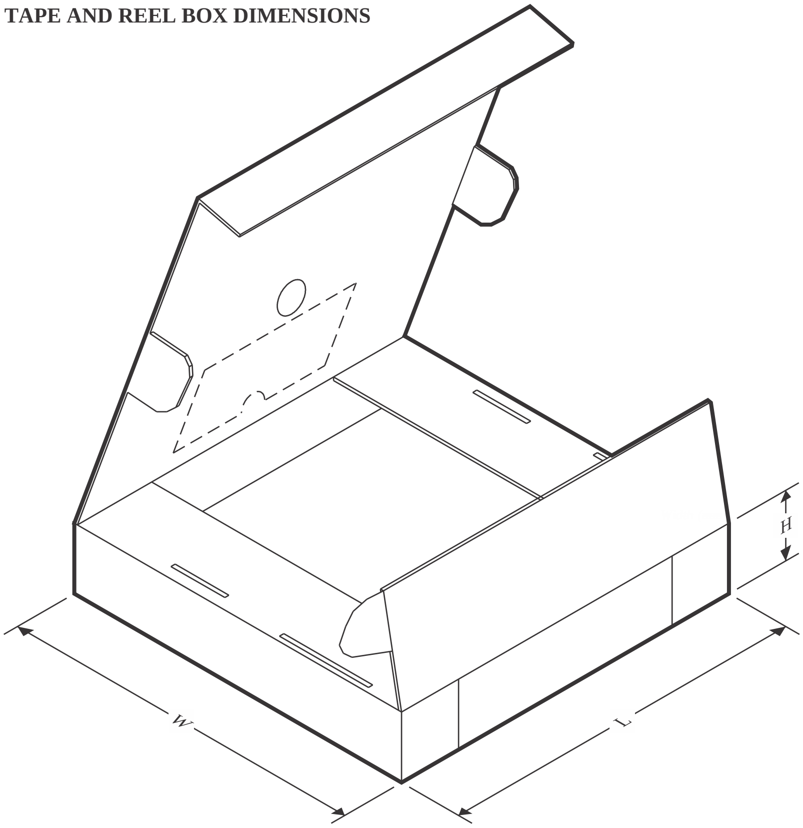
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

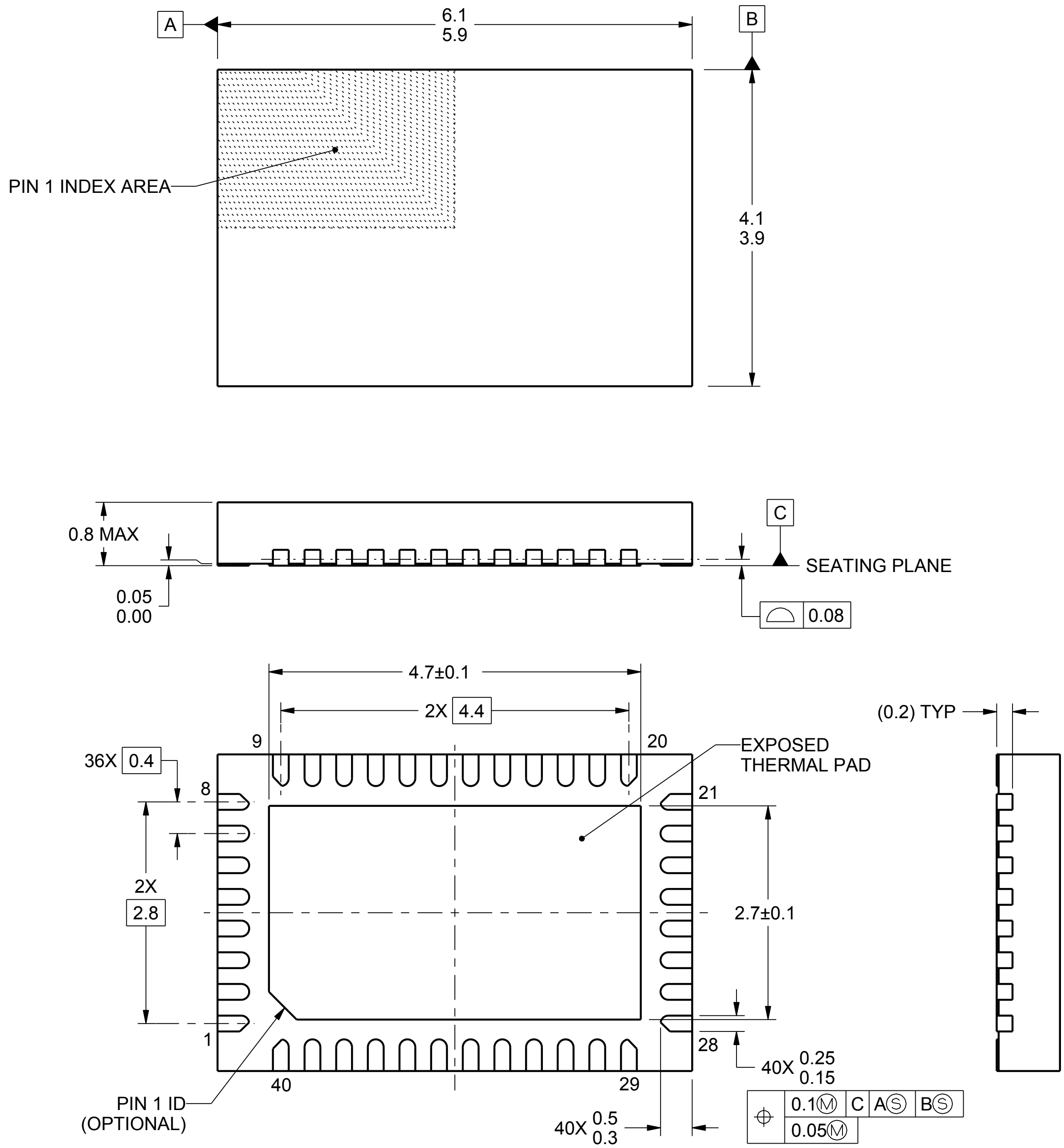
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TUSB1042IRNQR	WQFN	RNQ	40	3000	330.0	12.4	4.3	6.3	1.1	8.0	12.0	Q2
TUSB1042IRNQRG4	WQFN	RNQ	40	3000	330.0	12.4	4.3	6.3	1.1	8.0	12.0	Q2
TUSB1042IRNQT	WQFN	RNQ	40	250	180.0	12.4	4.3	6.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

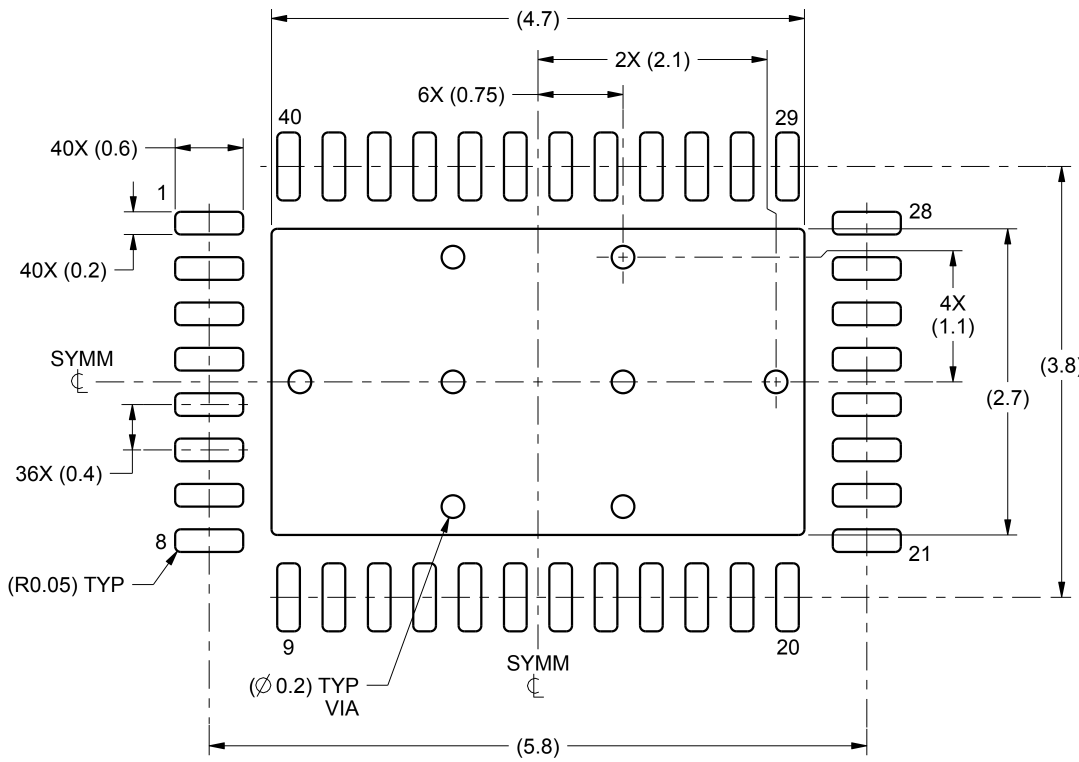
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TUSB1042IRNQR	WQFN	RNQ	40	3000	360.0	360.0	36.0
TUSB1042IRNQRG4	WQFN	RNQ	40	3000	367.0	367.0	35.0
TUSB1042IRNQT	WQFN	RNQ	40	250	210.0	185.0	35.0



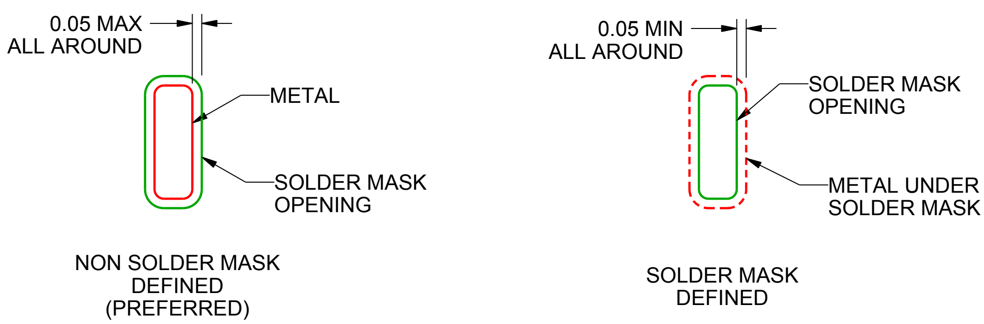
4222125/B 01/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

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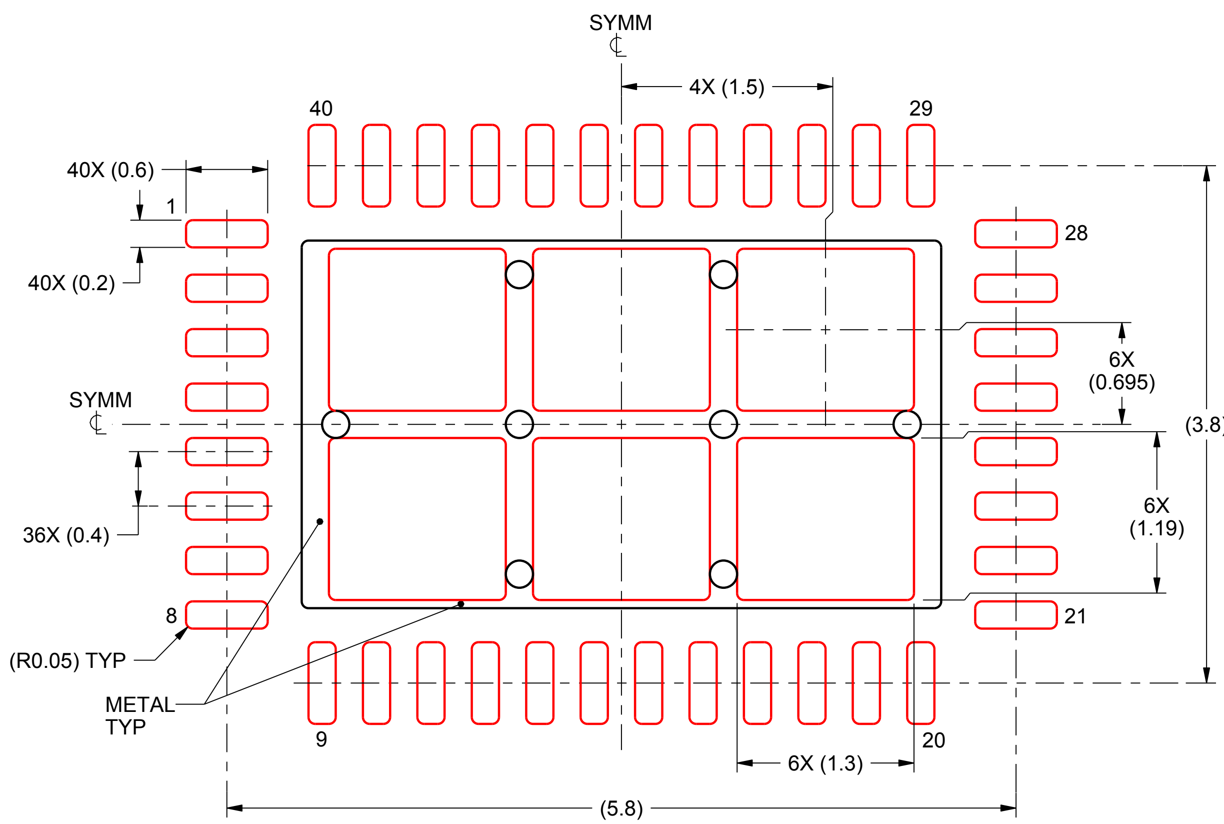
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD
73% PRINTED SOLDER COVERAGE BY AREA
SCALE:18X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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