TUSB215-Q1 USB 2.0 High Speed Signal Conditioner with USB BC1.2 CDP

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results
  - Device Temperature Grade 2: –40°C to 105°C Ambient Operating Temperature
  - Device HBM Classification Level H1C
  - Device CDM Classification Level C3
- Compatible with USB 2.0, OTG 2.0 and BC 1.2
- Pin strap or I^2C Configurable
- USB BC1.2 Charging Downstream Port (CDP) controller
- Support for LS, FS, HS signaling
- Ultra-low USB Disconnect and Shutdown Power Consumption
- Scalable solution - Daisy Chain Device for High Loss Applications
- D1P/M and D2P/M Interchangeable and Host/Device Agnostic
- Supports up to 5m pre-channel or 2m post-channel Cable Length
  - Four Selectable AC Boost Setting Via External Pulldown Resistor
  - DC Boost Along With AC Boost for Best Signal Integrity

2 Applications

- Automotive Infotainment
- Notebooks
- Desktops
- Docking Stations
- Tablets
- Cell Phones
- Active Cable, Cable Extenders
- Backplane
- Televisions

3 Description

The TUSB215-Q1 is a USB High-Speed (HS) signal conditioner, designed to compensate for ISI signal loss in a transmission channel which helps passing USB electrical compliance tests.

TUSB215-Q1 has a patent-pending design which is agnostic to USB Low Speed (LS) and Full Speed (FS) signals. LS and FS signal characteristics are unaffected by the TUSB215-Q1 while HS signals are compensated.

Programmable signal AC boost and DC boost permits fine tuning device performance to optimize High Speed signals at the connector, this allows use in many different applications.

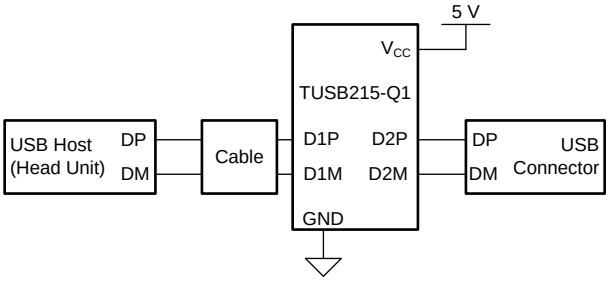
In addition, TUSB215-Q1 is compatible with the USB On-The-Go (OTG) and Battery Charging (BC) protocols. TUSB215-Q1 further acts as Charging Downstream Port (CDP) controller and handles the necessary handshakes with the downstream device.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TUSB215-Q1	VQFN (14)	3.50 mm x 3.50 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



Display

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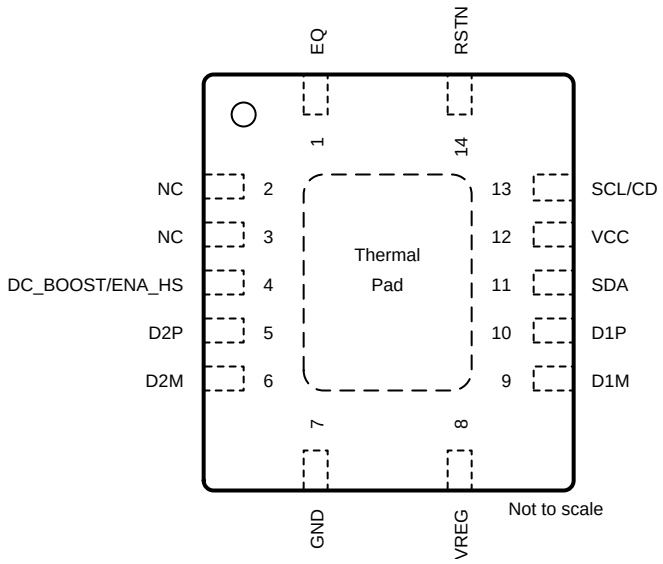
4 Revision History

DATE	REVISION	NOTES
September 2017	*	Initial release.

5 Pin Configuration and Functions

RGY Package
14 Pin (VQFN)
Top View



Pin Functions

PIN		I/O	INTERNAL PULLUP/PULLDOWN	DESCRIPTION
NAME	NO.			
EQ	1	I	N/A	USB High Speed AC boost select via external pull down resistor. Sampled upon de-assertion of RSTN. Does not recognize real time adjustments. See application section for details. Auto selects maximum AC boost level when left floating.
NC	2, 3	N/A	N/A	Leave unconnected.
DC_BOOST(1)/ENA_HS	4	I/O		In I2C mode: Reserved for TI test purpose. In non-I2C mode: At reset: 3-level input signal DC_BOOST. USB High Speed DC signal boost selection. H (pin is pulled high) – 80 mV M (pin is left floating) – 60 mV L (pin is pulled low) – 40 mV After reset: Output signal ENA_HS. Flag indicating that channel is in High Speed mode. Asserted upon: 1. Detection of USB-IF High Speed test fixture from an unconnected state followed by transmission of USB TEST_PACKET pattern. 2. Squelch detection following USB reset with a successful HS handshake [HS handshake is declared to be successful after single chirp J chirp K pair where each chirp is within 18 μs – 128 μs].
D2P	5	I/O	N/A	USB High Speed positive port.
D2M	6	I/O	N/A	USB High Speed negative port.
GND	7	PWR	N/A	Ground
VREG	8	O	N/A	1.8-V LDO output. Only enabled when operating in High Speed mode. Requires 0.1-μF external capacitor to GND to stabilize the core.
D1M	9	I/O	N/A	USB High Speed negative port..
D1P	10	I/O	N/A	USB High Speed positive port.
SDA(2)	11	I/O	RSTN asserted: 500 kΩ PD	I2C Mode: Bidirectional I2C data pin [I2C address = 0x2C]. In non I2C mode: Reserved for TI test purpose.

(1) Pull-down and pull-up (to 3.3 V) resistors for DC_BOOST pins must be between 22 kΩ to 47 kΩ in non I^2C mode.
(2) Pull-up resistors for SDA and SCL pins in I^2C mode should be 4.7 kΩ (5%). If both SDA and SCL are pulled up at reset the device enters into I^2C mode.

Pin Functions (continued)

PIN		I/O	INTERNAL PULLUP/PULLDOWN	DESCRIPTION
NAME	NO.			
VCC	12	PWR	N/A	Supply power
SCL[2]/CD	13	I/O	RSTN asserted: 500 kΩ PD	In I2C mode: I2C clock pin [I2C address = 0x2C]. Non I2C mode: After reset: Output CD. Flag indicating that a USB device is attached (connection detected). Asserted from an unconnected state upon detection of DP or DM pull-up resistor. De-asserted upon detection of disconnect.
RSTN	14	I	500 kΩ PU	Device disable/enable. Low – Device is at reset and in shutdown, and High – Normal operation. Recommend 0.1-µF external capacitor to GND to ensure clean power on reset if not driven. If the pin is driven, it must be held low until the supply voltage for the device reaches within specifications.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature and voltage range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Supply Voltage Range	VCC	-0.3	6	V
Voltage Range on I/O pins	DxP, DxM, RSTN, EQ, SCL, SDA, DC_BOOST, VREG	-0.3	3.8	V
T_{stg}	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature and voltage range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.4	5	5.5	V
T_A	Ambient temperature	TUSB215Q1	-40		105	°C
T_J	Junction temperature	TUSB215Q1	-40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		RGY (VQFN) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	24.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	24.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER						
I_{ACTIVE_HS}	High-speed active curent	USB channel = HS mode; 480 Mbps traffic; V_{CC} = 5V; V_{CC} supply stable; DC Boost = 60 mV		18	30	mA
I_{IDLE_HS}	High-speed idle current	USB channel = HS mode; no traffic; V_{CC} = 5V; V_{CC} supply stable; DC Boost = 60 mV		13	22	mA
$I_{SUSPEND\_HS}$	High-speed suspend current	USB channel = HS suspend mode; V_{CC} = 5V; V_{CC} supply stable		0.76	1.5	mA
I_{FS_LS}	Full/Low speed current	USB channel = FS mode or LS mode; V_{CC} = 5V		0.77	1.5	mA
$I_{DISCONNECT}$	Disconnect current	Host side application; No device attachment; V_{CC} = 5V		0.86	1.5	mA
I_{RSTN}	Disable current	RSTN driven low; V_{CC} supply stable; V_{CC} = 5V		22	80	µA
I_{LKG_FS}	Pin fail-safe leakage current for SDA, SCL, DC_BOOST, DxP/N, RSTN	V_{CC} = 0 V; Pin at 3.6 V			40	µA
RSTN						
V_{IH}	High-level input voltage	V_{CC} = 4.4V	2		3.6	V
V_{IL}	Low-level input voltage	V_{CC} = 5.5V	0		0.8	V
I_{IH}	High-level input current	V_{IH} = 3.6 V	-4		4	µA
I_{IL}	Low-level input current	V_{IL} = 0 V	-11		11	µA
EQ						
R_{EQ}	External pull-down resistor on EQ pin.	AC Boost Level 0			160	Ω
		AC Boost Level 1	1.4		2	kΩ
		AC Boost Level 2	3.7		3.9	kΩ
		AC Boost Level 3	6			kΩ
CD, ENA_HS						
V_{OH}	High-level output voltage	I_O = -50µA	2.4			V
V_{OL}	Low-level output voltage	I_O = 50µA			0.4	V
SCL, SDA						
C_{I2CBUS}	I2C Bus capacitance		4		150	pF
V_{IH}	SDA and SCL input high level voltage	V_{CC} = 4.4V	2		3.6	V
V_{IL}	SDA and SCL input Low level voltage	V_{CC} = 5.5V			0.8	V
V_{SDA_OL}	SDA low-level output voltage	4.7kΩ pullup to 3.6V; V_{CC} = 4.4V			0.4	V
I_{SDA_OL}	SDA Low level output current	V_{CC} = 5.5V; I^2C pulled up to 3.6V	1.1			mA
DC_BOOST						

Electrical Characteristics (continued)

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	V_{CC} = 5V	2.4		3.6	V
V_{IM}	Mid-level input voltage	V_{CC} = 5V		1.6		V
V_{IL}	Low-level input voltage	V_{CC} = 5V	0		0.4	V
DxP, DxM						
C_{IO_DXX}	Capacitance to GND	Measured with LCR meter and device powered down. 1 MHz sinusoid, 30 mVpp ripple		2.7		pF

6.6 Switching Characteristics

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
F_{BR_DXX}	DxP/M Bit Rate	USB channel = HS mode; 480 Mbps traffic; VCC supply stable			480.24	Mbps
t_{RISE_DXX}	DxP/M rise time	10% - 90%; V_{CC} = 5.5V; Max AC Gain;	100			ps
t_{FALL_DXX}	DxP/M fall time	90% - 10%; V_{CC} = 5.5V; Max AC Gain;	100			ps
$t_{RSTN\_PULSE\_WIDTH}$	Minimum width to detect a valid RSTN signal assert when the pin is actively driven	V_{CC} = 4.4 V; Refer to Figure 1	20			µs
t_{STABLE}	VCC stable before RSTN de-assertion	Refer to Figure 1	100			µs
t_{VCC_RAMP}	VCC ramp time		0.2		100	ms

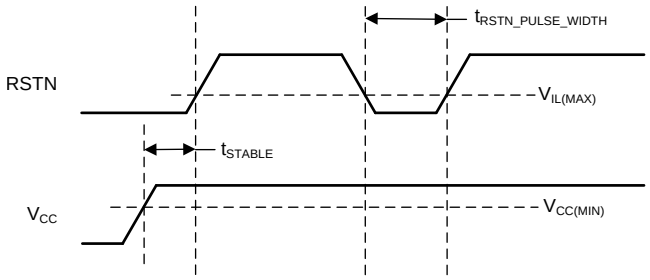


Figure 1. Power On and Reset Timing

6.7 Typical Characteristics

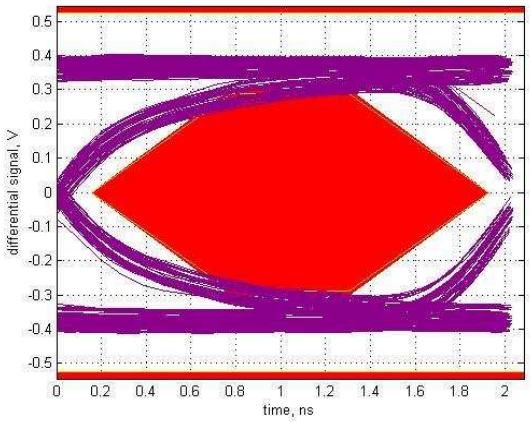


Figure 2. USB2.0 HS Eye diagram, Host far-end with 2m cable post-channel loss without TUSB215-Q1

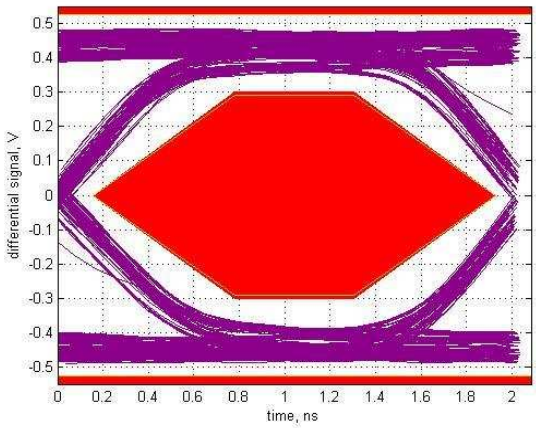


Figure 3. USB2.0 HS Eye diagram, Host far-end with 2m cable post-channel loss with TUSB215-Q1

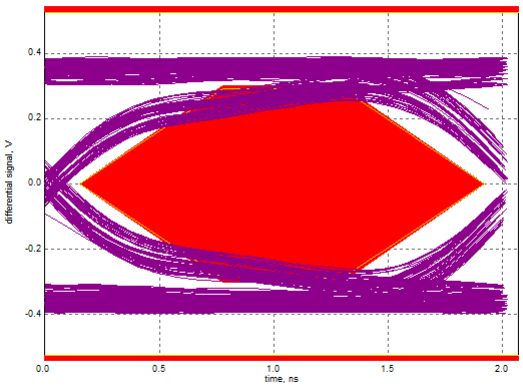


Figure 4. USB2.0 HS Eye diagram, Host far-end with 5m cable pre-channel loss without TUSB215-Q1

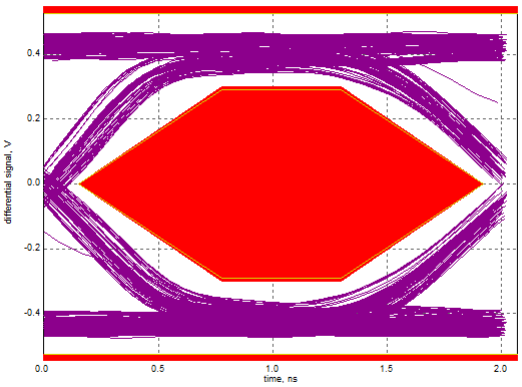


Figure 5. USB2.0 HS Eye diagram, Host far-end with 5m cable pre-channel loss with TUSB215-Q1

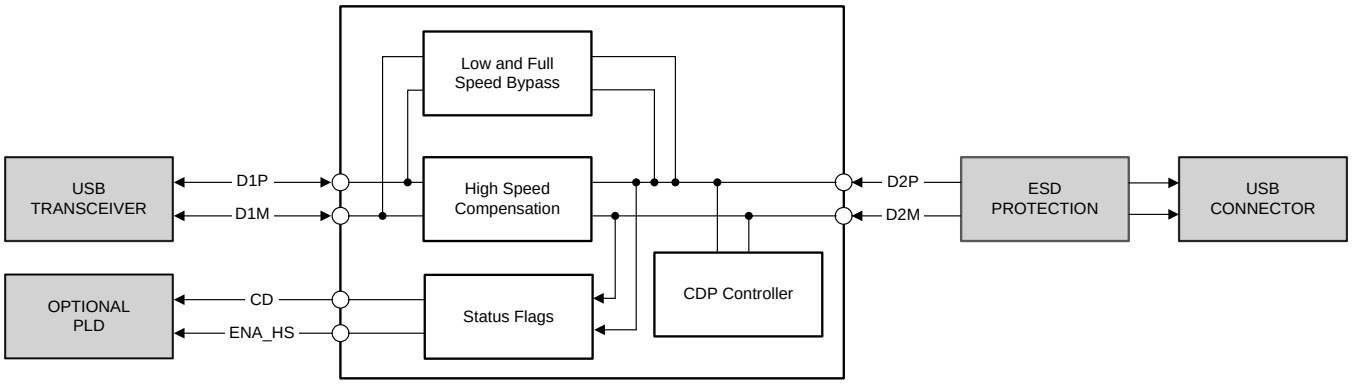
7 Detailed Description

7.1 Overview

The TUSB215-Q1 is a USB High-Speed (HS) signal conditioner, designed to compensate for ISI signal loss in a transmission channel. TUSB215-Q1 has a patent-pending design which is agnostic to USB Low Speed (LS) and Full Speed (FS) signals and does not alter their signal characteristics, while HS signals are compensated. In addition, the design is compatible with USB On-The-Go (OTG) and Battery Charging (BC) specifications. The TUSB215-Q1 provides USB Charging Downstream Port (CDP) controller for applications in which USB host or hub do not have this function.

Programmable signal AC boost through an external resistor on EQ pin permits fine tuning device performance to optimize signals helping to pass USB HS electrical compliance tests at the connector. Additional DC Boost configurable by three level input DC_BOOST pin helps overcoming the cable losses.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 EQ

The EQ pin of the TUSB215-Q1 is used to configure the AC boost of the device. The four levels of AC boost are set through different values of an external pulldown resistor at this pin.

7.3.2 DC BOOST

The DC_BOOST pin of the TUSB215-Q1 is a tri-level pin, used to set the DC gain of the device according to Table 1.

Table 1. DC Boost Settings

DC BOOST SETTING VIA PIN STRAP	
DC_BOOST	**DC Boost Setting (mV)**
V_{IL}	40
V_{IM}	60
V_{IH}	80

7.3.3 BC1.2 CDP Support

The TUSB215-Q1 main function is a signal conditioner offering the EQ/Boost features to the incoming DP/DM signals. For applications in which USB host or hub do not provide USB BC charging downstream port (CDP) functionality, the TUSB215-Q1 can perform this task.

7.4 Device Functional Modes

7.4.1 Low Speed (LS) Mode

TUSB215-Q1 automatically detects a LS connection and does not enable signal compensation. CD pin is asserted high.

7.4.2 Full Speed (FS) Mode

TUSB215-Q1 automatically detects a FS connection and does not enable signal compensation. CD pin is asserted high.

7.4.3 High Speed (HS) Mode

TUSB215-Q1 automatically detects a HS connection and will enable signal compensation as determined by the configuration of the DC_BOOST pin and the external pulldown resistance on its EQ pin. CD pin asserted high.

7.4.4 Shutdown Mode

TUSB215-Q1 is disabled when its RSTN pin is asserted low. In shutdown mode, the USB channel is still fully operational but there is neither signal compensation nor any indication from the CD pin as to the status of the channel.

7.4.5 I^2C Mode

TUSB215-Q1 support 100 kHz I^2C for device configuration, status readback and test purposes. This controller is enabled after SCL and SDA pins are sampled high shortly after de-assertion of RSTN. In this mode, the register as described in Table 2 can be accessed by I^2C read/write transaction to 7-bit slave address 0x2C. It is necessary to set CFG_ACTIVE bit and reset it to zero after making changes to the EQ and DC Boost level registers to restart the state machine.

NOTE

All registers or fields in Table 2 which are not specifically mentioned are considered reserved. The default value of these reserved registers or fields must not be changed. It is suggested to perform a read-modify-write operation to maintain the default value of the reserved fields.

Table 2. Register definition

Offset	Bit(s)	Name	Type	Default	Description
0x01	6:4	ACB_LVL	RW	XXX (Sampled from EQ pin at reset)	Sets the level of AC boost 000 :Level 0 AC boost programmed [MIN] 001 : Level 1 AC boost programmed 011 : Level 2 AC boost programmed 111 : Level 3 AC boost programmed [MAX]
0x03	0	CFG_ACTIVE	RW	1b	Configuration mode 0 : Normal mode. State machine enabled. 1 : Configuration mode: State machine disabled. After reset, if I2C mode is true (SCL and SDA are both pulled high) it is maintained until it is cleared by an I2C write, but, if I2C mode is not true, it is cleared automatically.

Device Functional Modes (continued)

Table 2. Register definition (continued)

Offset	Bit(s)	Name	Type	Default	Description
0x0E	2:0	DCB_LVL	RW	XXX (Sampled from DC_BOOST pin at reset)	Sets the level of DC Boost 011 : 40mV (DC_Boost = L) 101 : 60mV (DC_Boost = M, default) 111 : 80mV (DC_Boost = H)

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The primary purpose of the TUSB215-Q1 is to re-store the signal integrity of a USB High Speed channel up to the USB connector. The loss in signal quality stems from reduced channel bandwidth due to high loss PCB trace and other components that contribute a capacitive load. This can cause the channel to fail the USB near end eye mask. Proper use of the TUSB215-Q1 can help to pass this eye mask. Additionally the DC Boost helps overcoming DC losses from cables and traces.

A secondary purpose is to use the CD pin of the TUSB215-Q1 to control other blocks on the customer platform if so desired. The TUSB215-Q1 also provides CDP controller function.

8.2 Typical Application

A typical application is shown in Figure 6. In this setup, D2P and D2M face the USB connector while D1P and D1M face the USB host or hub. If desired, the orientation may be reversed [that is, D2 faces transceiver and D1 faces connector].

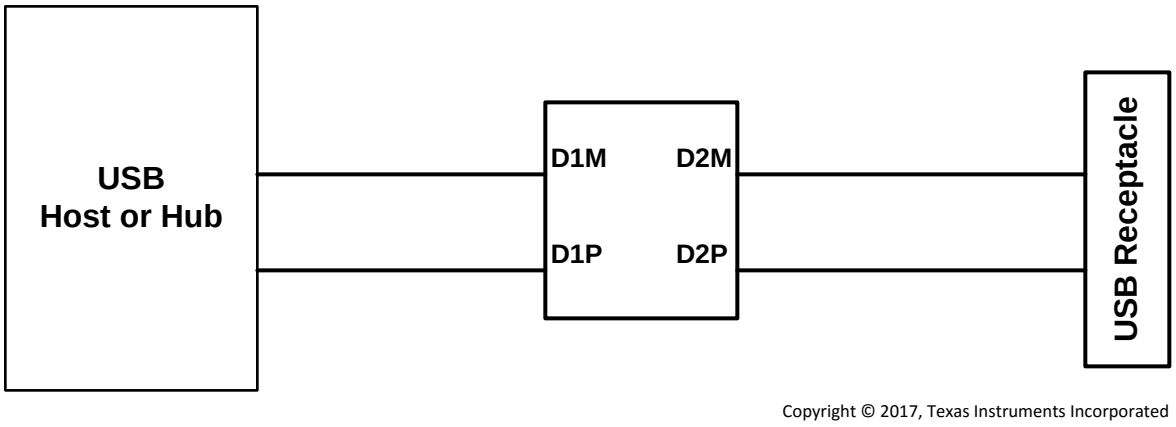


Figure 6. Typical Application

Typical Application (continued)

8.2.1 Design Requirements

For this design example, use the parameters shown in the table below.

Table 3. Design Parameters

PARAMETER				VALUE
V_{CC} (4.4 V to 5.5 V)				5 V
I^2C support required in system (Yes/No)				No
AC Boost		R_{EQ}	Level	AC Boost Level 2: R_{EQ} = 3.83 k
		0-Ω	0	
		1.69 k ±1%	1	
		3.83 k ± 1%	2	
		DNI	3	
DC Boost	R_{DC1}	R_{DC2}	Level	Mid DC Level: R_{DC1} = DNI R_{DC2} = DNI
	22 kΩ - 47 kΩ	Do Not Install (DNI)	40 mV Low DC boost	
	DNI	DNI	60 mV Mid DC boost	
	47 kΩ	24 kΩ	80 mV High DC boost	

8.2.2 Detailed Design Procedure

TUSB215-Q1 requires a valid reset signal as described in the power supply recommendations section. The capacitor at RSTN pin is not required if a microcontroller drives the RSTN pin according to recommendations.

VREG pin is the internal LDO output that requires a 0.1-μF external capacitor to GND to stabilize the core.

The ideal AC boost setting is dependent upon the signal chain loss characteristics of the target platform. The general recommendation is to start with AC boost level 0, and then increment to AC boost level 1, etc. if permissible. Same applies to the DC Boost setting where it is recommended to plan for the required pads or connections to change boost settings, but to start with DC boost level 1.

In order for the TUSB215-Q1 to recognize any change to the AC and DC Boost settings, the RSTN pin must be toggled. This is because the configuration is latched on power up and the inputs are ignored thereafter.

NOTE

The TUSB215-Q1 compensates for DC attenuation in the signal path according to the configuration of the DC_BOOST pin. This pin is not 5V tolerant and therefore when selecting the highest DC boost level, the voltage level at DC_BOOST pin must be less than 3.6V.

Placement of the device is also dependent on the application goal. Table 4 summarizes our recommendations.

Table 4. Platform Placement Guideline

PLATFORM GOAL	SUGGESTED DEVICE PLACEMENT
Pass USB Near End Mask	Close to measurement point
Pass USB Far End Eye Mask	Close to USB PHY
Cascade multiple devices to improve device enumeration	Midway between each USB interconnect

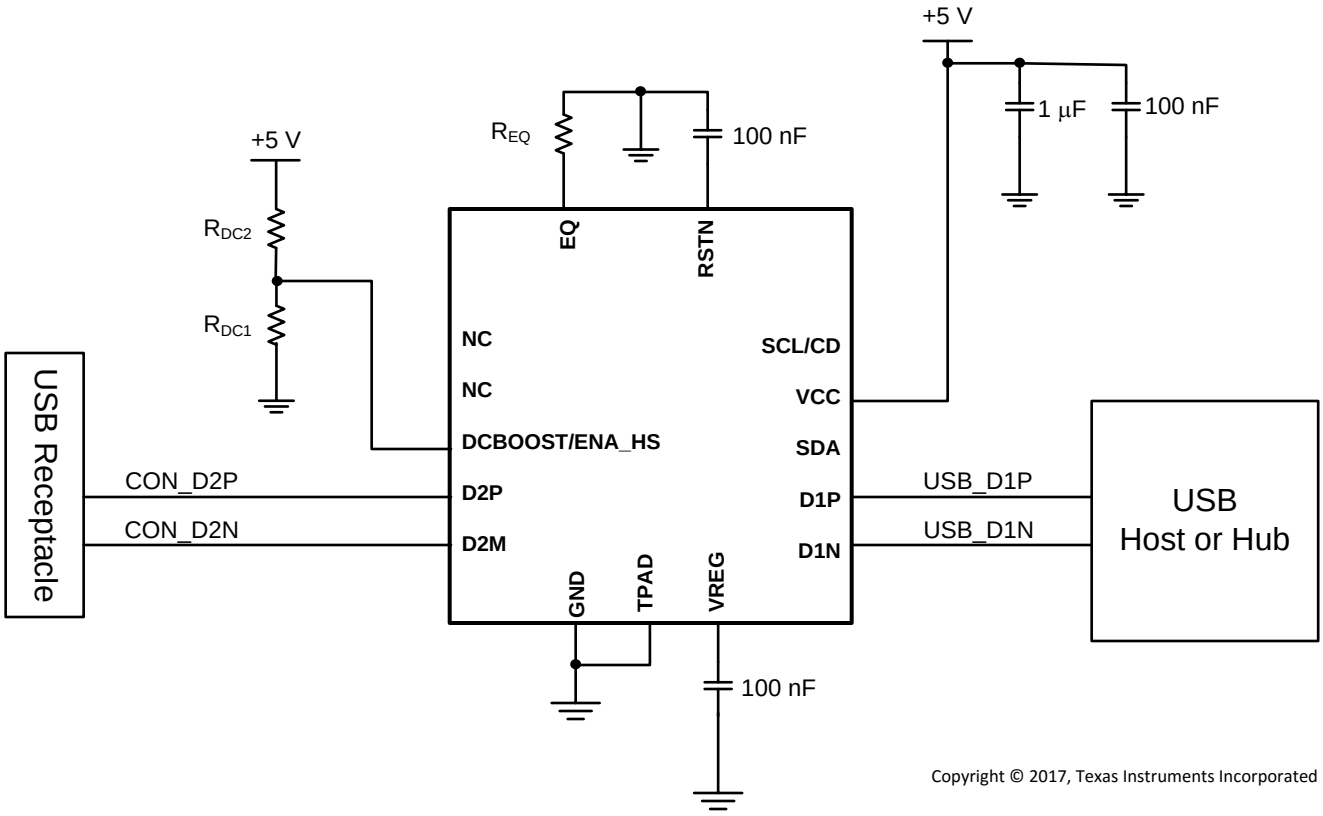


Figure 7. Reference Schematic

8.2.2.1 Test Procedure to Construct USB High Speed Eye Diagram

NOTE

USB-IF certification tests for High Speed eye masks require the *mandated use* of the USB-IF developed test fixtures. These test fixtures do not require the use of oscilloscope probes. Instead they use SMA cables. More information can be found at the USB-IF Compliance Updates Page. It is located under the 'Electricals' section, ID 86 dated March 2013.

The following procedure must be followed before using any oscilloscope compliance software to construct a USB High Speed Eye Mask:

8.2.2.1.1 For a Host Side Application

1. Configure the TUSB215-Q1 to the desired AC and DC Boost settings
2. Power on (or toggle the RSTN pin if already powered on) the TUSB215-Q1
3. Using SMA cables, connect the oscilloscope and the USB-IF host-side test fixture to the TUSB215-Q1
4. Enable the host to transmit USB TEST_PACKET
5. Execute the oscilloscope USB compliance software.
6. Repeat the above steps in order to re-test TUSB215-Q1 with a different settings

8.2.2.1.2 For a Device Side Application

1. Configure the TUSB215-Q1 to the desired AC and DC Boost settings
2. Power on (or toggle the RSTN pin if already powered on) the TUSB215-Q1
3. Connect a USB host, the USB-IF device-side test fixture, and USB device to the TUSB215-Q1. Ensure that the USB-IF device test fixture is configured to the 'INIT' position
4. Allow the host to enumerate the device
5. Enable the device to transmit USB TEST_PACKET
6. Using SMA cables, connect the oscilloscope to the USB-IF device-side test fixture and ensure that the device-side test fixture is configured to the 'TEST' position.
7. Execute the oscilloscope USB compliance software.
8. Repeat the above steps in order to re-test TUSB215-Q1 with a different settings

8.2.3 Application Curves

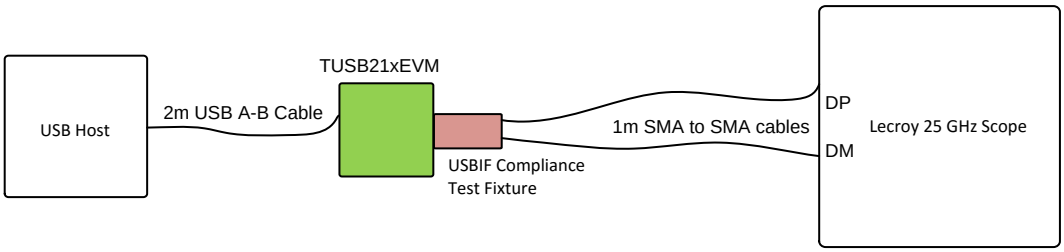


Figure 8. Eye Diagram Bench Setup

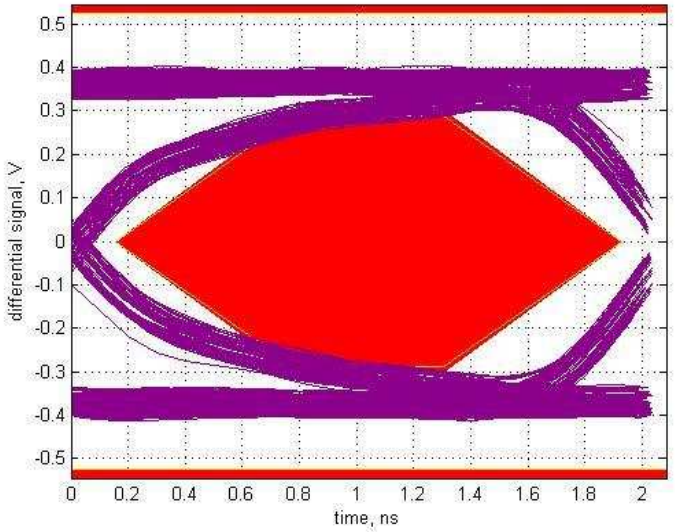


Figure 9. No TUSB215-Q1

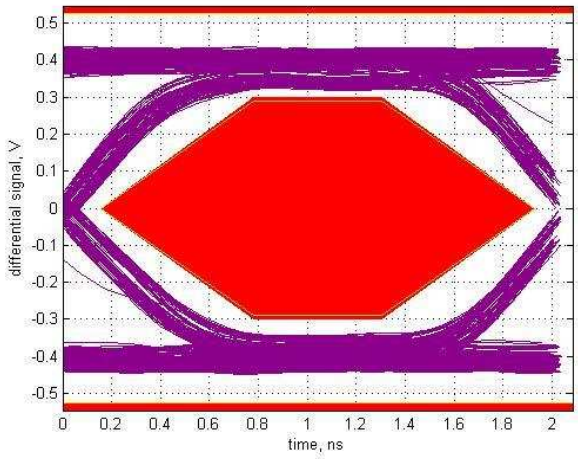


Figure 10. Low DC Boost, AC Boost Level 0

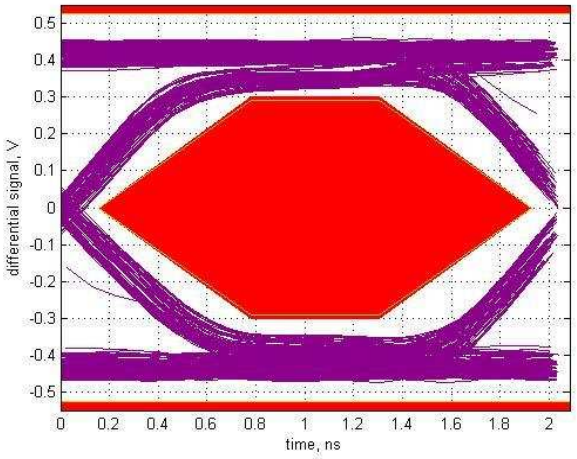


Figure 11. Mid DC Boost, AC Boost Level 0

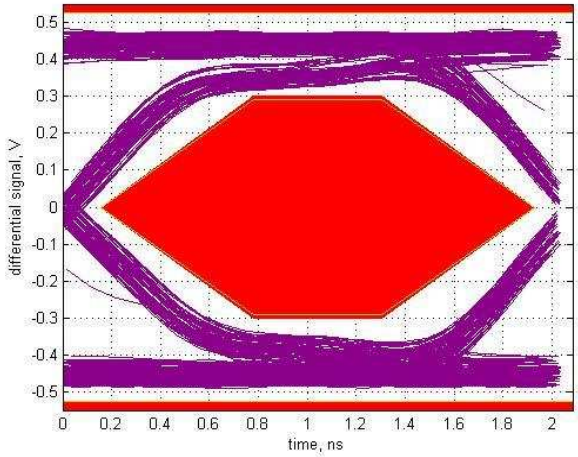


Figure 12. High DC Boost, AC Boost Level 0

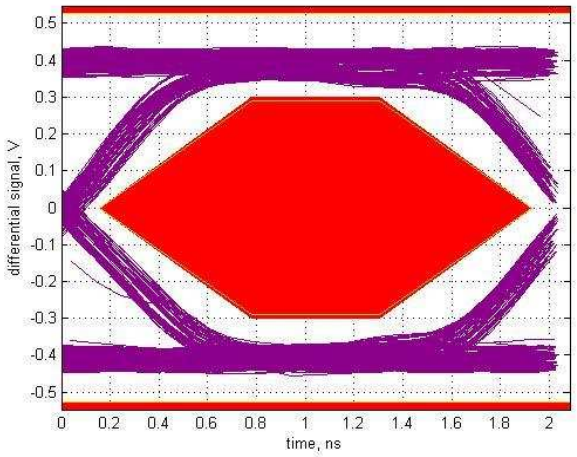


Figure 13. Low DC Boost, AC Boost Level 1

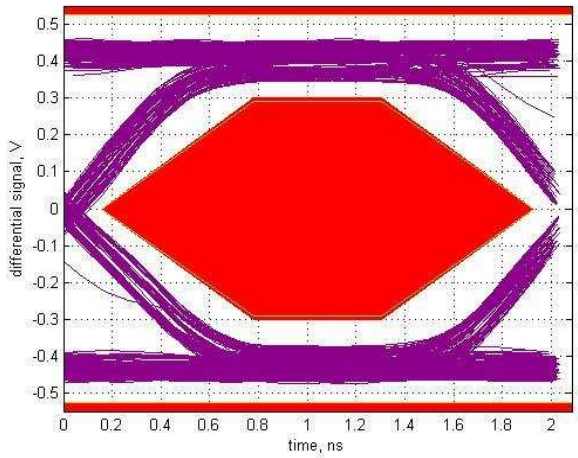


Figure 14. Mid DC Boost, AC Boost Level 1

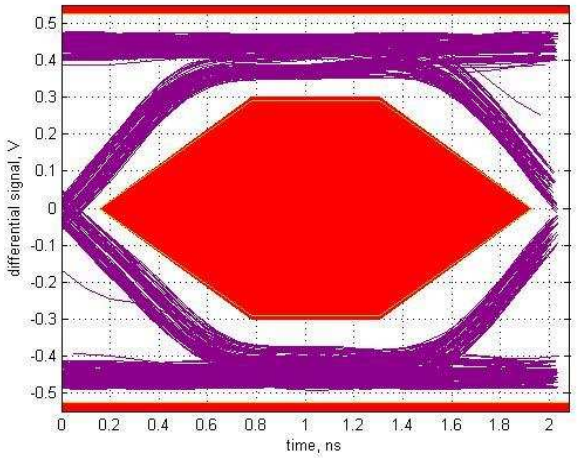


Figure 15. High DC Boost, AC Boost Level 1

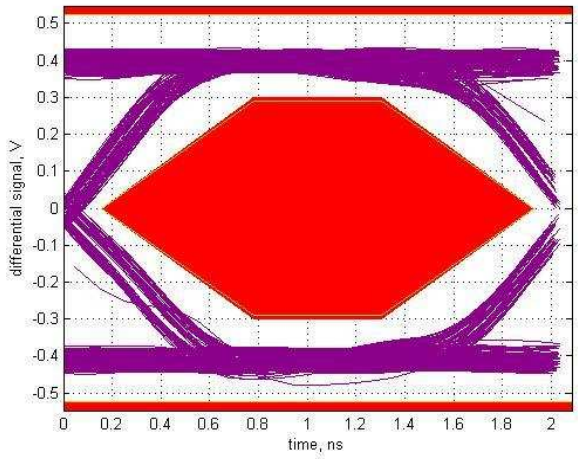


Figure 16. Low DC Boost, AC Boost Level 2

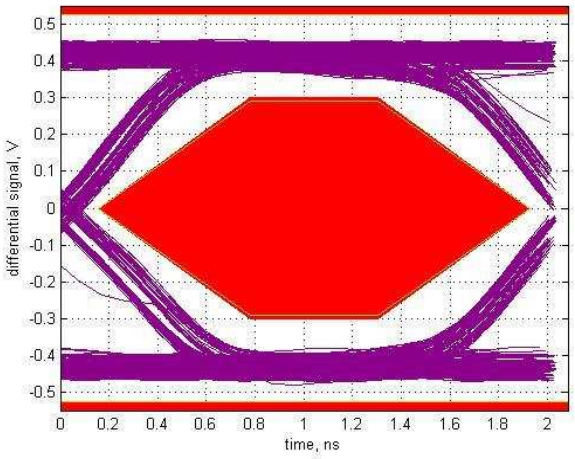


Figure 17. Mid DC Boost, AC Boost Level 2

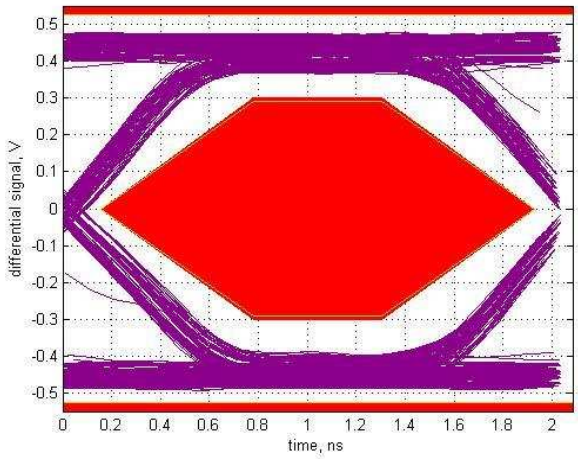


Figure 18. High DC Boost, AC Boost Level 2

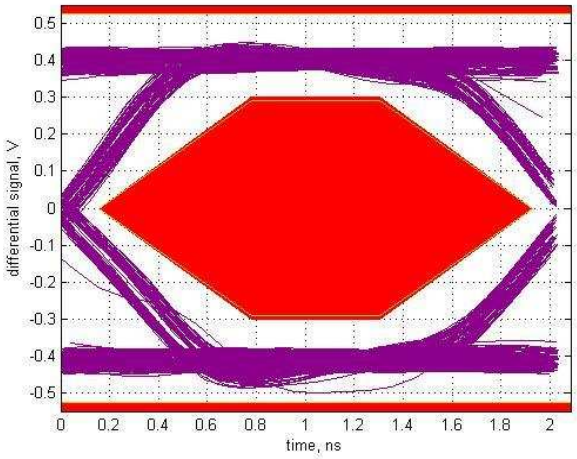


Figure 19. Low DC Boost, AC Boost Level 3

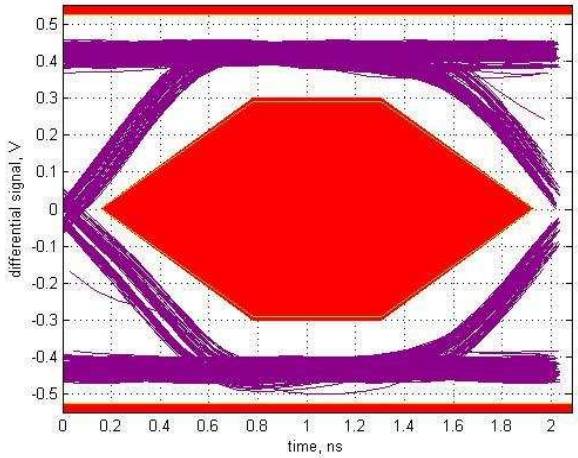


Figure 20. Mid DC Boost, AC Boost Level 3

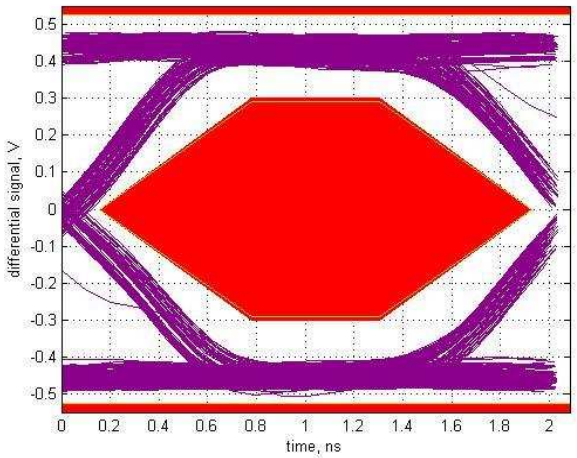


Figure 21. High DC Boost, AC Boost Level 3

9 Power Supply Recommendations

On power up, the interaction of the RSTN pin and power on ramp could result in digital circuits not being set correctly. The device should not be enabled until the power on ramp has settled to 4.4 V or higher to ensure a correct power on reset of the digital circuitry. If RSTN cannot be held low by microcontroller or other circuitry until the power on ramp has settled, then an external capacitor from the RSTN pin to GND is required to hold the device in the low power reset state.

The RC time constant should be larger than five times of the power on ramp time (0 to V_{CC}). With a typical internal pullup resistance of 500 kΩ, the recommended minimum external capacitance is calculated as:

$$C_{RSTN} = [\text{Ramp Time} \times 5] \div [500\ k\Omega] \quad (1)$$

10 Layout

10.1 Layout Guidelines

To avoid the need for signal vias, it is highly recommend to route the High Speed traces on the same surface layer than the TUSB215-Q1 is placed. shows an example how one could layout the PCB for TUSB215-Q1.

The layout should use impedance controlled traces to maintain 90 Ω differential impedance for the whole signal path as required per USB 2.0 specification. General guidelines for highspeed signal routing apply.

10.2 Layout Example

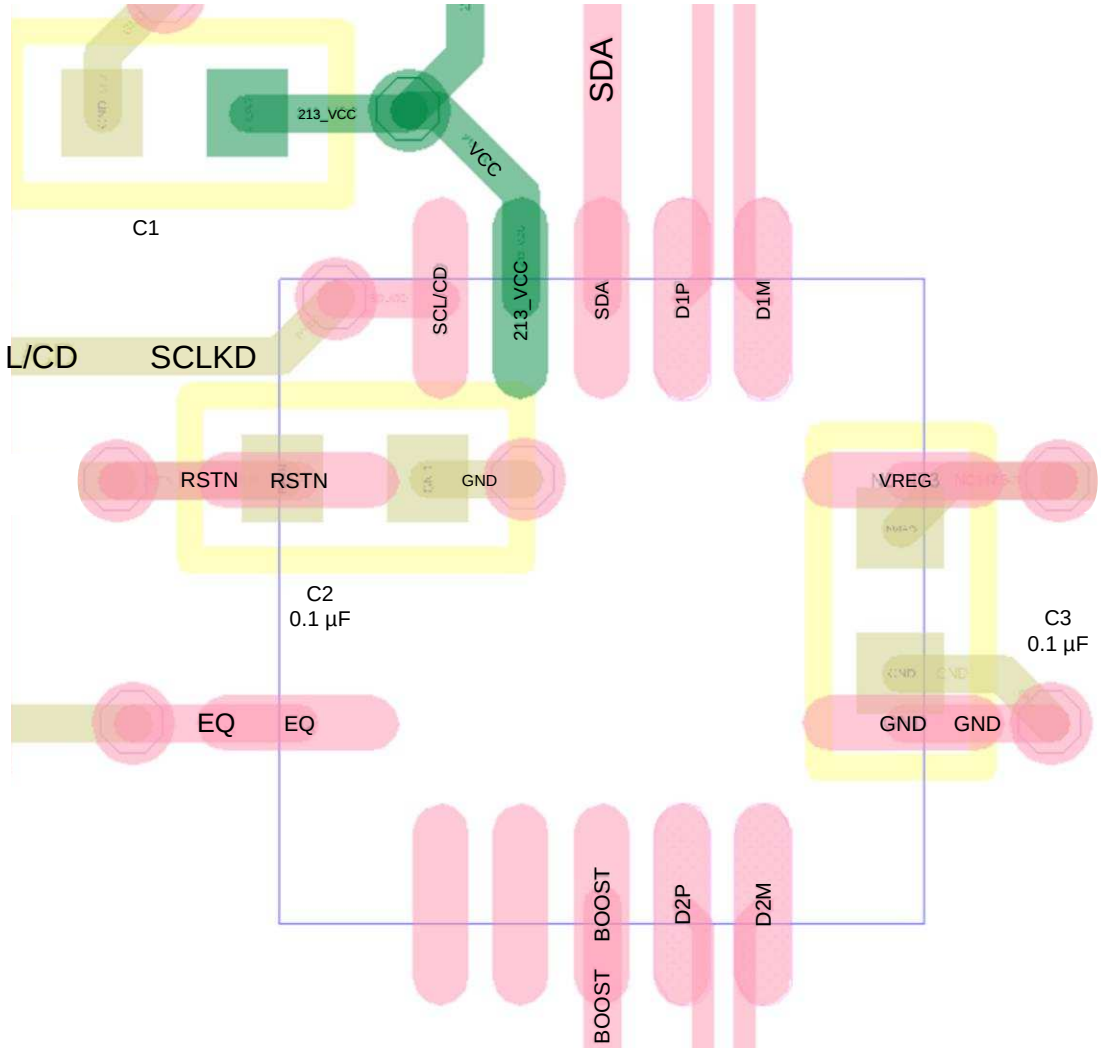


Figure 22. Layout Example

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

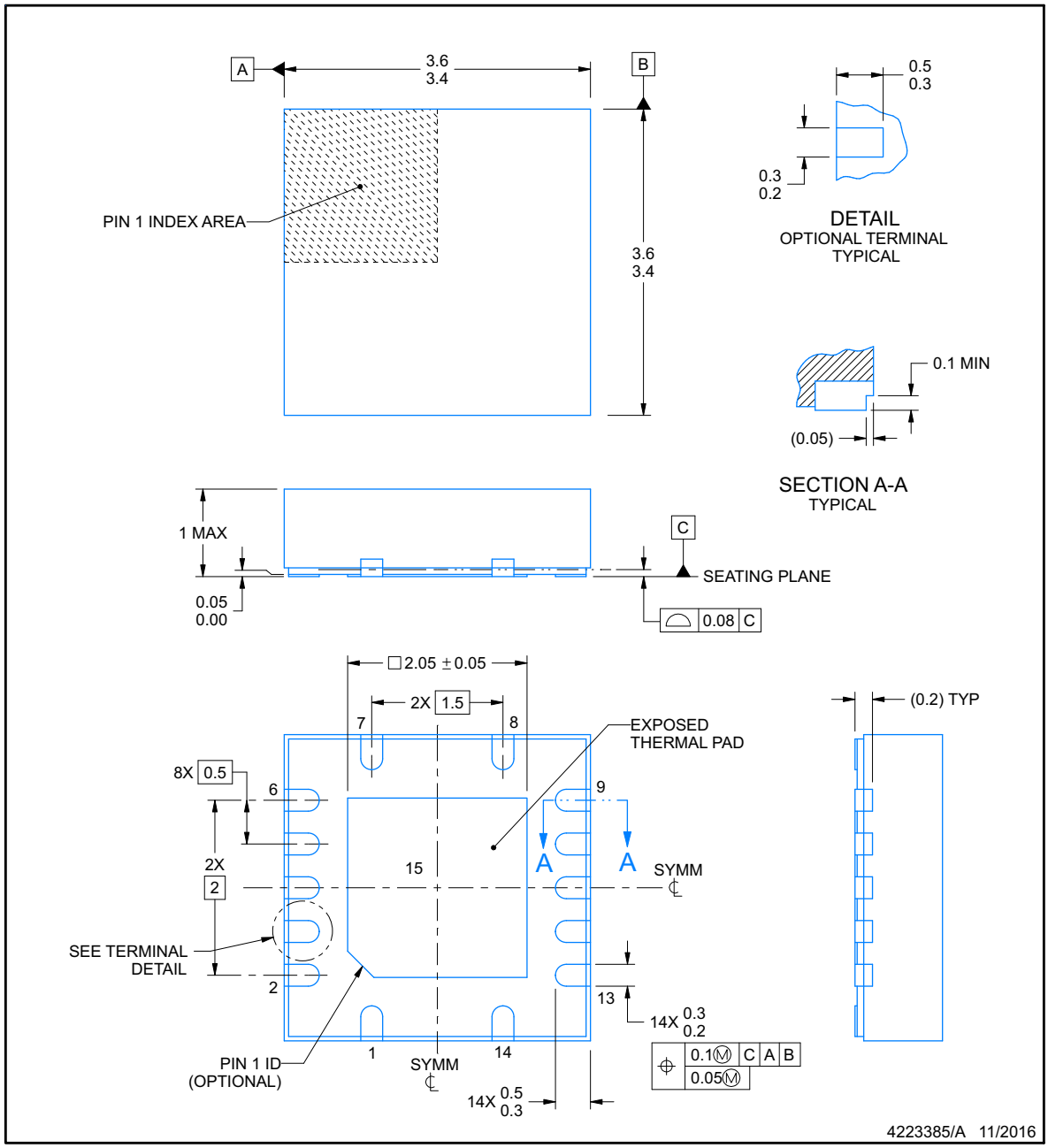
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

RGY0014B

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



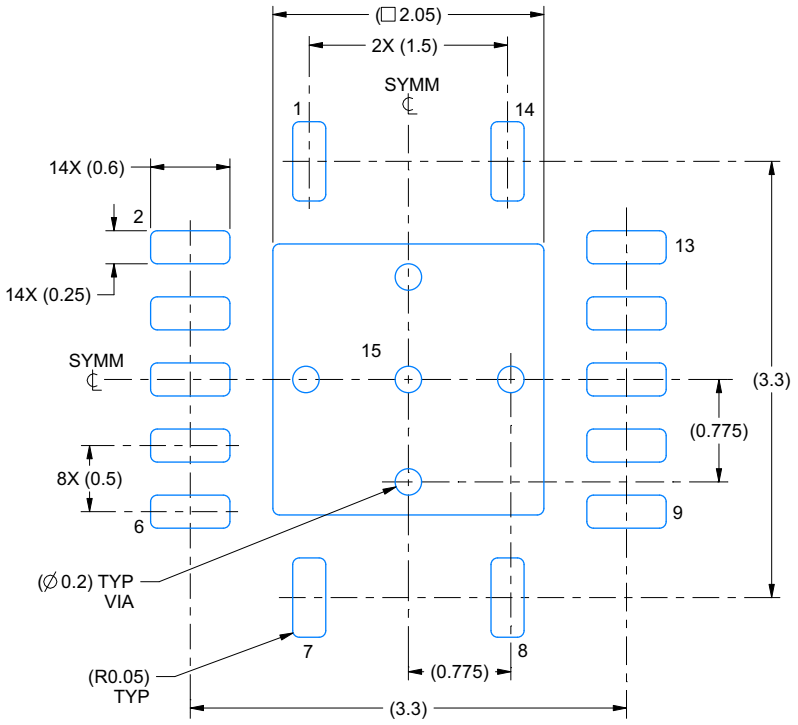
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

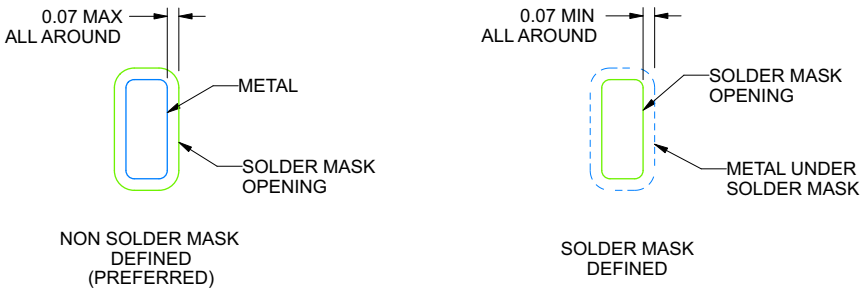
EXAMPLE BOARD LAYOUT

RGY0014B — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

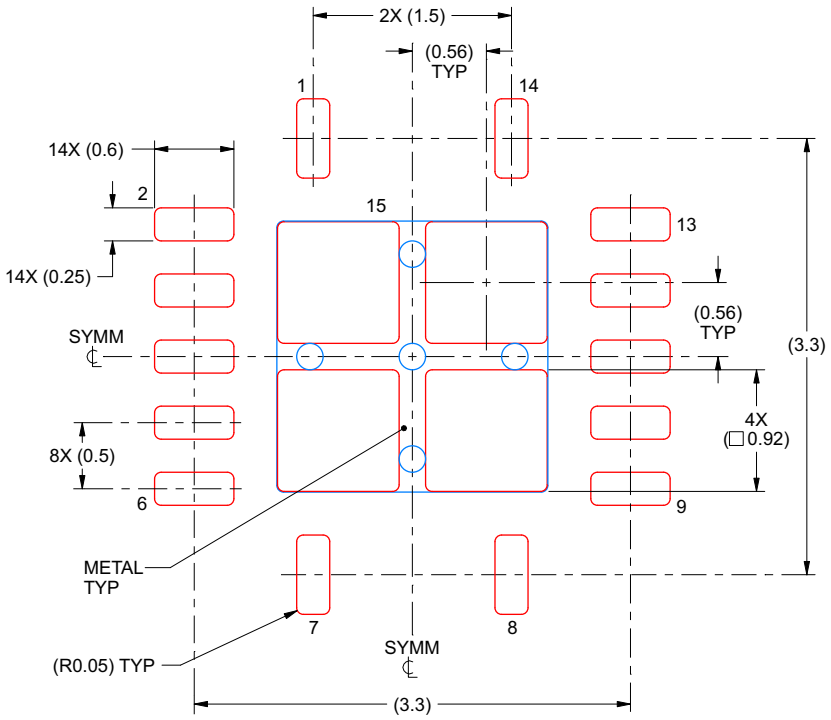
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGY0014B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 15
80% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TUSB215QRGYRQ1	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 105	USB215
TUSB215QRGYRQ1.A	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 105	USB215
TUSB215QRGYTQ1	Active	Production	VQFN (RGY) | 14	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 105	USB215
TUSB215QRGYTQ1.A	Active	Production	VQFN (RGY) | 14	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 105	USB215

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TUSB215-Q1 :

- Catalog : TUSB215

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

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Last updated 10/2025