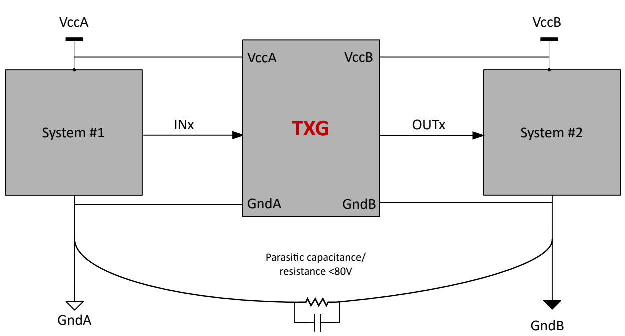
# TXG804x 4-bit, ±80V Ground-Level Translator

## 1 Features

- Supports DC shifts up to ±80V
- AC Noise Rejection of $140V_{PP}$ up to 1MHz
- CMTI of 250V/µs
- Low Prop Delay (<5ns) and Ch-Ch Skew (0.35ns)
- Greater than 250Mbps
- Low power consumption (0.65mA per channel at 1Mbps, 1.8V)
- Fully configurable dual-rail design allows each port to operate from 1.71V to 5.5V
- 4, 2, 1 channel devices with multiple configurations will be available
- Two device variants:
  - TXG8041: 3 forward, 1 reverse
  - TXG8042: 2 forward, 2 reverse
- Supports $V_{CC}$ disconnect feature (I/Os are forced into high-Z)
- Schmitt-trigger inputs allows for slow and noisy signals
- Inputs with integrated static pull-down resistors prevent channels from floating
- Operating temperature from –40°C to +125°C
- Latch-up performance exceeds 100mA per JESD 78, class II
  - ESD protection exceeds JESD 22
  - 4000V human-body model
  - 500V charged-device model
- Package options provided:
  - DYY (SOT-14)
  - DBQ (QSOP-16)




**Simplified Diagram**

## 2 Applications

- Test and Measurement
- Factory Automation
- Appliances

## 3 Description

The TXG804x is a 4-bit, fixed direction, non-galvanic based voltage and ground-level translator that supports both logic-level shifting between 1.71V to 5.5V and ground-level shifting up to ±80V. Compared to traditional level shifters, the TXG804x family solves the challenges of voltage translation across different ground levels. The Simplified Diagram shows a common use case where DC shift occurs between GNDA to GNDB due to parasitic resistance or capacitance.

$V_{CCA}$ is referenced to GNDA and $V_{CCB}$ is referenced to GNDB. Ax pins are referenced to $V_{CCA}$ logic level while Bx pins are referenced to $V_{CCB}$ logic levels. Both A port and B port accept voltages from 1.71V to 5.5V. This device includes two enable pins that place the respective outputs in a high-impedance state when the OE pin is connected to GND or left floating. In the event of input power or signal loss, the output is default low when OE is High (refer to Table 7-1). The leakage between GNDA and GNDB is 70nA when $V_{CC}$ to GND is shorted.

The TXG804x device helps improve noise immunity and power sequencing across different ground domains while providing low power consumption, latency, and channel-to-channel skew. TXG804x supresses noise levels of $140_{PP}$ up to 1MHz (Figure 7-3). This device supports multiple interfaces such as SPI, UART, GPIO, and I2S.

**Package Information**

| PART NUMBER | PACKAGE [(1)] | BODY SIZE (NOM) |
|---|---|---|
| TXG8041<br>TXG8042 | DYY (SOT-14) | 4.20mm × 2.00mm |
| | DBQ (QSOP-16) | 4.90mm x 3.90mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

ADVANCE INFORMATION

ADVANCE INFORMATION

## Table of Contents

## 4 Pin Configuration and Functions

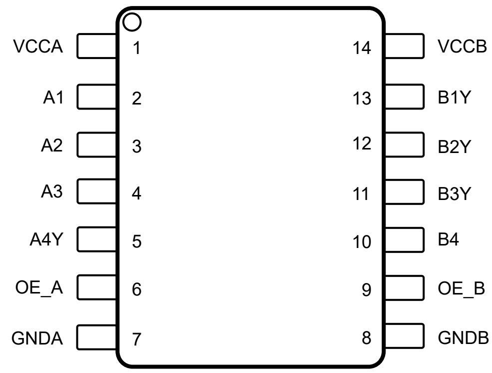



**Figure 4-1. TXGx041DYY 14-Pin SOT Top View**

**Table 4-1. TXGx041 DYY Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| Name | TXGx041 | | |
| A1 | 2 | I | Input A1. Referenced to $V_{CCA}$ |
| A2 | 3 | I | Input A2. Referenced to $V_{CCA}$ |
| A3 | 4 | I | Input A3. Referenced to $V_{CCA}$ |
| A4Y | 5 | O | Output A4. Referenced to $V_{CCA}$ |
| B1Y | 13 | O | Output B1. Referenced to $V_{CCB}$ |
| B2Y | 12 | O | Output B2. Referenced to $V_{CCB}$ |
| B3Y | 11 | O | Output B3. Referenced to $V_{CCB}$ |
| B4 | 10 | I | Input B4. Referenced to $V_{CCB}$ |
| OE_A | 6 | I | Active-High Output Enable (A side). Pull to GND to place all outputs in high-impedance mode. |
| OE_B | 9 | I | Active-High Output Enable (B side). Pull to GND to place all outputs in high-impedance mode. |
| $V_{CCA}$ | 1 | — | A side supply voltage. $1.71V \leq V_{CCA} \leq 5.5V$ |
| $V_{CCB}$ | 14 | — | B side supply voltage. $1.71V \leq V_{CCB} \leq 5.5V$ |
| GNDA | 7 | — | Ground reference for $V_{CCA}$ |
| GNDB | 8 | — | Ground reference for $V_{CCB}$ |

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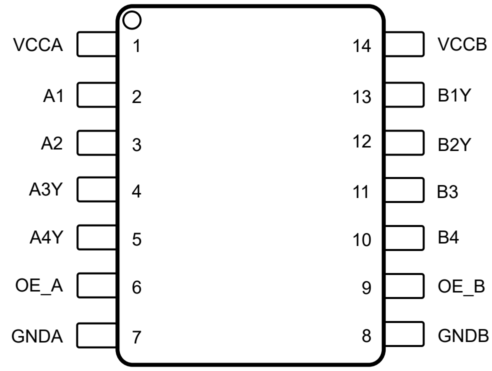


**Figure 4-2. TXGx042DYY 14-Pin SOT Top View**

**Table 4-2. TXGx042 DYY Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| Name | TXGx042 | | |
| A1 | 2 | I | Input A1. Referenced to $V_{CCA}$ |
| A2 | 3 | I | Input A2. Referenced to $V_{CCA}$ |
| A3Y | 4 | O | Output A3. Referenced to $V_{CCA}$ |
| A4Y | 5 | O | Output A4. Referenced to $V_{CCA}$ |
| B1Y | 13 | O | Output B1. Referenced to $V_{CCB}$ |
| B2Y | 12 | O | Output B2. Referenced to $V_{CCB}$ |
| B3 | 11 | I | Input B3. Referenced to $V_{CCB}$ |
| B4 | 10 | I | Input B4. Referenced to $V_{CCA}$ |
| OE_A | 6 | I | Active-High Output Enable (A side). Pull to GND to place all outputs in high-impedance mode. |
| OE_B | 9 | I | Active-High Output Enable (B side). Pull to GND to place all outputs in high-impedance mode. |
| $V_{CCA}$ | 1 | — | A side supply voltage. $1.71V \leq V_{CCA} \leq 5.5V$ |
| $V_{CCB}$ | 14 | — | B side supply voltage. $1.71V \leq V_{CCB} \leq 5.5V$ |
| GNDA | 7 | — | Ground reference for $V_{CCA}$ |
| GNDB | 8 | — | Ground reference for $V_{CCB}$ |

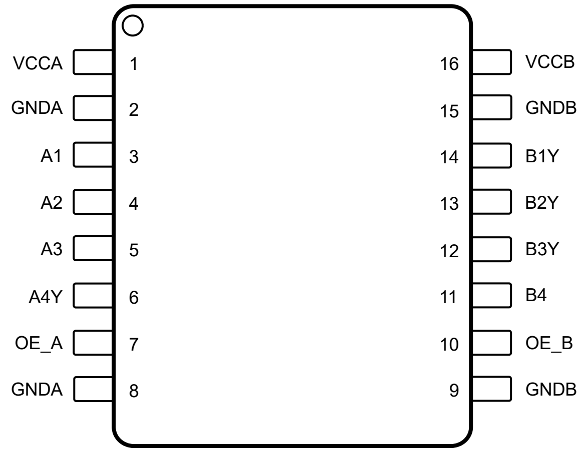


**Figure 4-3. TXGx041DBQ 16-Pin QSOP Top View**

**Table 4-3. TXGx041 DBQ Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| Name | TXGx041 | | |
| A1 | 3 | I | Input A1. Referenced to $V_{CCA}$ |
| A2 | 4 | I | Input A2. Referenced to $V_{CCA}$ |
| A3 | 5 | I | Input A3. Referenced to $V_{CCA}$ |
| A4Y | 6 | O | Output A4. Referenced to $V_{CCA}$ |
| B1Y | 14 | O | Output B1. Referenced to $V_{CCB}$ |
| B2Y | 13 | O | Output B2. Referenced to $V_{CCB}$ |
| B3Y | 12 | O | Output B3. Referenced to $V_{CCB}$ |
| B4 | 11 | I | Input B4. Referenced to $V_{CCB}$ |
| OE_A | 7 | I | Active-High Output Enable (A side). Pull to GND to place all outputs in high-impedance mode. |
| OE_B | 10 | I | Active-High Output Enable (B side). Pull to GND to place all outputs in high-impedance mode. |
| $V_{CCA}$ | 1 | — | A side supply voltage. 1.71V ≤ $V_{CCA}$ ≤ 5.5V |
| $V_{CCB}$ | 16 | — | B side supply voltage. 1.71V ≤ $V_{CCB}$ ≤ 5.5V |
| GNDA | 2, 8 | — | Ground reference for $V_{CCA}$ |
| GNDB | 9, 15 | — | Ground reference for $V_{CCB}$ |

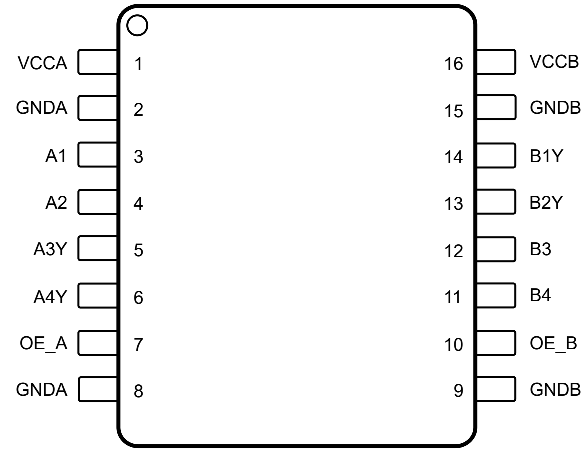


**Figure 4-4. TXGx042DBQ 16-Pin QSOP Top View**

**Table 4-4. TXGx042 DBQ Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| Name | TXGx042 | | |
| A1 | 3 | I | Input A1. Referenced to $V_{CCA}$ |
| A2 | 4 | I | Input A2. Referenced to $V_{CCA}$ |
| A3Y | 5 | O | Output A3. Referenced to $V_{CCA}$ |
| A4Y | 6 | O | Output A4. Referenced to $V_{CCA}$ |
| B1Y | 14 | O | Output B1. Referenced to $V_{CCB}$ |
| B2Y | 13 | O | Output B2. Referenced to $V_{CCB}$ |
| B3 | 12 | I | Input B3. Referenced to $V_{CCB}$ |
| B4 | 11 | I | Input B4. Referenced to $V_{CCB}$ |
| OE_A | 7 | I | Active-High Output Enable (A side). Pull to GND to place all outputs in high-impedance mode. |
| OE_B | 10 | I | Active-High Output Enable (B side). Pull to GND to place all outputs in high-impedance mode. |
| $V_{CCA}$ | 1 | — | A side supply voltage. 1.71V ≤ $V_{CCA}$ ≤ 5.5V |
| $V_{CCB}$ | 16 | — | B side supply voltage. 1.71V ≤ $V_{CCB}$ ≤ 5.5V |
| GNDA | 2, 8 | — | Ground reference for $V_{CCA}$ |
| GNDB | 9, 15 | — | Ground reference for $V_{CCB}$ |

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CCA}$ to $V_{GNDA}$ | Supply voltage A to Ground voltage A | | –0.5 | 6.5 | V |
| $V_{CCB}$ to $V_{GNDB}$ | Supply voltage B to Ground voltage B | | –0.5 | 6.5 | V |
| $V_{GNDA}$ to $V_{GNDB}$ | Voltage between GNDA and GNDB | | -82 | 82 | V |
| $V_I$ | Input Voltage[2] | I/O Ports (A Port) to $V_{GNDA}$ | –0.5 | 6.5 | V |
| | | I/O Ports (B Port) to $V_{GNDB}$ | –0.5 | 6.5 | |
| | | OE | –0.5 | 6.5 | V |
| $V_O$ | Voltage applied to any output in the high-impedance or power-off state[2] | A Port to $V_{GNDA}$ | –0.5 | 6.5 | V |
| | | B Port to $V_{GNDB}$ | –0.5 | 6.5 | |
| $V_O$ | Voltage applied to any output in the high or low state[2] [3] | A Port to $V_{GNDA}$ | –0.5 | 6.5 | V |
| | | B Port to $V_{GNDB}$ | –0.5 | 6.5 | |
| $I_{IK}$ | Input clamp current | $V_I < 0$ | –20 | | mA |
| $I_{OK}$ | Output clamp current | $V_O < 0$ | –20 | | mA |
| $I_O$ | Continuous output current | | –16 | 16 | mA |
| | Continuous current through $V_{CCx}$ or GNDx | | –64 | 64 | mA |
| $T_j$ | Junction Temperature | | | 150 | °C |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Section 5.1* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Section 5.3* Exposure beyond the limits listed in *Section 5.3* may affect device reliability.
(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 6.5V maximum if the output current rating is observed.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1] | ±4000 | V |
| | | Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002[2] | ±500 | |

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

ADVANCE INFORMATION

## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1) (2) (3)

| | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CCA}$ | Supply voltage A - Relative to GNDA | | 1.71 | | 5.5 | V |
| $V_{CCB}$ | Supply voltage B - Relative to GNDB | | 1.71 | | 5.5 | V |
| $V_{GNDA}$ to $V_{GNDB}$ | Voltage between GNDA and GNDB | | -80 | | 80 | V |
| $I_{OH}$ | High-level output current | $V_{CCO}$ = 1.71V | –4.5 | | | mA |
| | | $V_{CCO}$ = 2.3V | –8 | | | |
| | | $V_{CCO}$ = 3V | –10 | | | |
| | | $V_{CCO}$ = 4.5V | –12 | | | |
| $I_{OL}$ | Low-level output current | $V_{CCO}$ = 1.71V | | | 4.5 | mA |
| | | $V_{CCO}$ = 2.3V | | | 8 | |
| | | $V_{CCO}$ = 3V | | | 10 | |
| | | $V_{CCO}$ = 4.5V | | | 12 | |
| $V_I$ | Input voltage - Relative to GNDx | | 0 | | 5.5 | V |
| $V_O$ | Output voltage - Relative to GNDx | | 0 | | $V_{CCO}$ | V |
| $T_A$ | Operating free-air temperature | | –40 | | 125 | °C |

(1) $V_{CCI}$ is the $V_{CC}$ associated with the input port.
(2) $V_{CCO}$ is the $V_{CC}$ associated with the output port.
(3) All control inputs and data I/Os of this device have weak pulldowns to ensure the line is not floating when undefined external to the device. The input leakage from these weak pulldowns is defined by the $I_I$ specification indicated under Section 5.5

## 5.4 Thermal Information

| THERMAL METRIC (1) | | TXGx041 and TXGx042 | | UNIT |
|---|---|---|---|---|
| | | DYY (SOT) | DBQ (QSOP) | |
| | | 14 PINS | 16 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 128.4 | 143.1 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 52.4 | 82.3 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 58.5 | 46.9 | °C/W |
| $Y_{JT}$ | Junction-to-top characterization parameter | 2.7 | 1.2 | °C/W |
| $Y_{JB}$ | Junction-to-board characterization parameter | 51.9 | 81.9 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)[(1)] [(2)]

| PARAMETER | | TEST CONDITIONS | $V_{CCA}$ | $V_{CCB}$ | Operating free-air temperature ($T_A$) –40°C to 125°C MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage [(3)] | $I_{OH}$ = –4.5mA | 1.71V | 1.71V | 1.5 | | | V |
| | | $I_{OH}$ = –8mA | 2.3V | 2.3V | 2.0 | | | |
| | | $I_{OH}$ = –10mA | 3V | 3V | 2.6 | | | |
| | | $I_{OH}$ = –12mA | 4.5V | 4.5V | 4.0 | | | |
| $V_{OL}$ | Low-level output voltage [(4)] | $I_{OL}$ = 4.5mA | 1.71V | 1.71V | | | 0.18 | V |
| | | $I_{OL}$ = 8mA | 2.3V | 2.3V | | | 0.33 | |
| | | $I_{OL}$ = 10mA | 3V | 3V | | | 0.41 | |
| | | $I_{OL}$ = 12mA | 4.5V | 4.5V | | | 0.49 | |
| $V_{T+}$ | Positive-going input-threshold voltage | Data Inputs (Ax, Bx) (Referenced to $V_{CCI}$) | 1.71V | 1.71V | | | 1.14 | V |
| | | | 2.3V | 2.3V | | | 1.42 | |
| | | | 3V | 3V | | | 1.74 | |
| | | | 4.5V | 4.5V | | | 2.47 | |
| | | | 5.5V | 5.5V | | | 2.97 | |
| $V_{T+}$ | Positive-going input-threshold voltage | OE (Referenced to $V_{CCA}$ or $V_{CCB}$) | 1.71V | 1.71V | | | 1.12 | V |
| | | | 2.3V | 2.3V | | | 1.42 | |
| | | | 3V | 3V | | | 1.73 | |
| | | | 4.5V | 4.5V | | | 2.47 | |
| | | | 5.5V | 5.5V | | | 2.94 | |
| $V_{T-}$ | Negative-going input-threshold voltage | Data Inputs (Ax, Bx) (Referenced to $V_{CCI}$) | 1.71V | 1.71V | 0.52 | | | V |
| | | | 2.3V | 2.3V | 0.76 | | | |
| | | | 3V | 3V | 1.09 | | | |
| | | | 4.5V | 4.5V | 1.77 | | | |
| | | | 5.5V | 5.5V | 2.28 | | | |
| $V_{T-}$ | Negative-going input-threshold voltage | OE (Referenced to $V_{CCA}$ or $V_{CCB}$) | 1.71V | 1.71V | 0.46 | | | V |
| | | | 2.3V | 2.3V | 0.76 | | | |
| | | | 3V | 3V | 1.04 | | | |
| | | | 4.5V | 4.5V | 1.86 | | | |
| | | | 5.5V | 5.5V | 2.5 | | | |
| $\Delta V_T$ | Input-threshold hysteresis ($V_{T+} – V_{T-}$) | Data Inputs (Ax, Bx) (Referenced to $V_{CCI}$) | 1.71V | 1.71V | 0.24 | | 0.54 | V |
| | | | 2.3V | 2.3V | 0.29 | | 0.60 | |
| | | | 3V | 3V | 0.33 | | 0.54 | |
| | | | 4.5V | 4.5V | 0.38 | | 0.82 | |
| | | | 5.5V | 5.5V | 0.37 | | 0.96 | |
| $\Delta V_T$ | Input-threshold hysteresis ($V_{T+} – V_{T-}$) | OE (Referenced to $V_{CCA}$ or $V_{CCB}$) | 1.71V | 1.71V | 0.24 | | 0.45 | V |
| | | | 2.3V | 2.3V | 0.28 | | 0.58 | |
| | | | 3V | 3V | 0.32 | | 0.54 | |
| | | | 4.5V | 4.5V | 0.35 | | 0.58 | |
| | | | 5.5V | 5.5V | 0.39 | | 0.62 | |
| $I_I$ | Input leakage current | Data Inputs (Ax, Bx) $V_I$ = $V_{CCI}$ or GND | 1.71V – 5.5V | 1.71V – 5.5V | | | 1.6 | µA |

ADVANCE INFORMATION

over operating free-air temperature range (unless otherwise noted)[(1)] [(2)]

| PARAMETER | | TEST CONDITIONS | $V_{CCA}$ | $V_{CCB}$ | Operating free-air temperature ($T_A$) –40°C to 125°C MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $I_{off\text{-}float}$ | Floating supply Partial power down current | A Port or B Port<br>$V_I$ = GND | Floating[(5)] | 0V - 5.5V | –2.5 | | 2.5 | µA |
| | | | 0V - 5.5V | Floating[(5)] | –2.5 | | 2.5 | |
| $I_O$ | Tri-state output Output current | A or B Port:<br>$V_I = V_{CCA}$ or $V_{GNDA}$<br>OE = GND | 1.71V – 5.5V | 1.1V – 5.5V | –5 | | 5 | µA |
| $C_i$ | Control Input Capacitance | $V_I$ = 3.3V or $V_{GNDA}$ | 3.3V | 3.3V | | 2 | | pF |
| $C_{io}$ | Data I/O Capacitance | OE = GND, $V_O$ = 1.71V DC +1MHz -16dBm sine wave | 3.3V | 3.3V | | 5 | | pF |
| $C_{GND}$ | Cap between grounds | All channels combined ($V_{CC}$ both sides are powered on) | | | | | 49 | pF |
| | | All channels combined ($V_{CC}$ to GND shorted) | | | | | 54 | pF |
| Leakage | Current Leakage between GndA to GndB | All channels combined ($V_{CC}$ to GND shorted) | 1.71V – 5.5V | 1.71V – 5.5V | | 70 | | nA |
| | | All channels combined ($V_{CC}$ both sides are powered on and inputs are all low) | 1.71V – 5.5V | 1.71V – 5.5V | | 70 | | nA |
| | | All channels combined ($V_{CC}$ both sides are powered on and inputs are all high) | 1.71V – 5.5V | 1.71V – 5.5V | | 33 | | µA |
| CMTI | Common Mode Transient Immunity | Input toggling at 100Mbps<br>Ground shift up to 80V | 1.71V – 5.5V | 1.71V – 5.5V | | | 250 | V/µs |
| $V_{UVLO+}$ | Positive-Going Undervoltage Lockout Voltage | A Supply | 1.71V – 5.5V | | | | 1.55 | V |
| | | B Supply | | 1.71V – 5.5V | | | 1.55 | |
| $V_{UVLO-}$ | Negative-Going Undervoltage Lockout Voltage | A Supply | 1.71V – 5.5V | | 1.36 | | | V |
| | | B Supply | | 1.71V – 5.5V | 1.36 | | | |
| $V_{UVLO\_Hys}$ | Undervoltage Lockout Hysteresis | A Supply | 1.71V – 5.5V | | 36 | | 147 | mV |
| | | B Supply | | 1.71V – 5.5V | 36 | | 147 | |

(1) $V_{CCI}$ is the $V_{CC}$ associated with the input port and referenced to $GND_A$
(2) $V_{CCO}$ is the $V_{CC}$ associated with the output port and referenced to $GND_B$
(3) Tested at $V_I = V_{T+(MAX)}$
(4) Tested at $V_I = V_{T-(MIN)}$
(5) Floating is defined as a node that is both not actively driven by an external device and has leakage not exeeding 10nA

## 5.6 Supply Current

over operating free-air temperature range (unless otherwise noted)[(1)] [(2)]

| PARAMETER | | TEST CONDITIONS | $V_{CCA}$ | $V_{CCB}$ | Operating free-air temperature ($T_A$) –40°C to 125°C MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| **TXGx041** | | | | | | | | |
| $I_{CCA}$ | $V_{CCA}$ supply current | $V_I = V_{CCI}$ or GND, $I_O = 0$ | 1.71V – 5.5V | 1.71V – 5.5V | | 546 | 1220 | µA |
| | | | 0V | 5.5V | | -3 | 13 | |
| | | | 5.5V | 0V | | 509 | 1050 | |
| | | $V_I$ = GND, $I_O = 0$ | 5.5V | Floating[(3)] | | 509 | 1050 | |
| $I_{CCB}$ | $V_{CCB}$ supply current | $V_I = V_{CCI}$ or GND, $I_O = 0$ | 1.71V – 5.5V | 1.71V – 5.5V | | 750 | 1836 | µA |
| | | | 0V | 5.5V | | 654 | 1350 | |
| | | | 5.5V | 0V | | -3 | 36 | |
| | | $V_I$ = GND, $I_O = 0$ | Floating[(3)] | 5.5V | | 656 | 1350 | |
| $I_{CCA} + I_{CCB}$ | Supply Current - Disable | EN = 0 | 1.8V | 1.8V | | 1.9 | 3.1 | mA |
| | | | 2.5V | 2.5V | | 1.9 | 3.1 | |
| | | | 3.3V | 3.3V | | 2.0 | 3.1 | |
| | | | 5V | 5V | | 2.1 | 3.3 | |
| $I_{CCA} + I_{CCB}$ | Supply Current - DC Signal | $V_I = V_{CCI}$ | 1.8V | 1.8V | | 1 | 2.65 | mA |
| | | | 2.5V | 2.5V | | 1.3 | 2.7 | |
| | | | 3.3V | 3.3V | | 1.3 | 2.8 | |
| | | | 5V | 5V | | 1.4 | 3.1 | |
| | | $V_I$ = GND | 1.8V | 1.8V | | 1.2 | 2.7 | |
| | | | 2.5V | 2.5V | | 1.3 | 2.7 | |
| | | | 3.3V | 3.3V | | 1.3 | 2.8 | |
| | | | 5V | 5V | | 1.4 | 3.1 | |

ADVANCE INFORMATION

over operating free-air temperature range (unless otherwise noted)[(1) (2)]

| PARAMETER | | TEST CONDITIONS | $V_{CCA}$ | $V_{CCB}$ | Operating free-air temperature ($T_A$) –40°C to 125°C MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $I_{CCA} + I_{CCB}$ | Supply Current - AC Signal | All channels switching with square wave clock input; $C_L$ = 15pF, 1Mbps | 1.8V | 1.8V | 1.5 | | 2.6 | mA |
| | | | 2.5V | 2.5V | 1.6 | | 2.7 | |
| | | | 3.3V | 3.3V | 1.6 | | 2.8 | |
| | | | 5V | 5V | 1.9 | | 3.3 | |
| | | All channels switching with square wave clock input; $C_L$ = 15pF, 50Mbps | 1.8V | 1.8V | 9.2 | | 12.1 | |
| | | | 2.5V | 2.5V | 10.8 | | 14 | |
| | | | 3.3V | 3.3V | 12.4 | | 16.2 | |
| | | | 5V | 5V | 17.6 | | 20.6 | |
| | | All channels switching with square wave clock input; $C_L$ = 15pF, 100Mbps | 1.8V | 1.8V | 16.5 | | 20.1 | |
| | | | 2.5V | 2.5V | 20.2 | | 24.7 | |
| | | | 3.3V | 3.3V | 24.1 | | 29 | |
| | | | 5V | 5V | 35 | | 38 | |
| **TXGx042** | | | | | | | | |
| $I_{CCA}$ | $V_{CCA}$ supply current | $V_I = V_{CCI}$ or GND, $I_O = 0$ | 1.71V – 5.5V | 1.71V – 5.5V | 547 | | 1365 | µA |
| | | | 0V | 5.5V | -2.6 | | 25 | |
| | | | 5.5V | 0V | 625 | | 1052 | |
| | | $V_I$ = GND, $I_O = 0$ | 5.5V | Floating[(3)] | 625 | | 1052 | |
| $I_{CCB}$ | $V_{CCB}$ supply current | $V_I = V_{CCI}$ or GND, $I_O = 0$ | 1.71V – 5.5V | 1.71V – 5.5V | 753 | | 1692 | µA |
| | | | 0V | 5.5V | 819 | | 1380 | |
| | | | 5.5V | 0V | -2.4 | | 25 | |
| | | $V_I$ = GND, $I_O = 0$ | Floating[(3)] | 5.5V | 823 | | 1380 | |
| $I_{CCA} + I_{CCB}$ | Supply Current - Disable | EN = 0 | 1.8V | 1.8V | 1.9 | | 3.1 | mA |
| | | | 2.5V | 2.5V | 1.9 | | 3.1 | |
| | | | 3.3V | 3.3V | 2 | | 3.1 | |
| | | | 5V | 5V | 2.1 | | 3.3 | |

over operating free-air temperature range (unless otherwise noted)(1) (2)

| PARAMETER | | TEST CONDITIONS | $V_{CCA}$ | $V_{CCB}$ | Operating free-air temperature ($T_A$) –40°C to 125°C MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $I_{CCA} + I_{CCB}$ | Supply Current - DC Signal | $V_I = V_{CCI}$ | 1.8V | 1.8V | 1.2 | | 2.7 | mA |
| | | | 2.5V | 2.5V | 1.3 | | 2.6 | |
| | | | 3.3V | 3.3V | 1.3 | | 2.7 | |
| | | | 5V | 5V | 1.4 | | 3.1 | |
| | | $V_I$ = GND | 1.8V | 1.8V | 1.2 | | 2.7 | |
| | | | 2.5V | 2.5V | 1.3 | | 2.6 | |
| | | | 3.3V | 3.3V | 1.3 | | 2.7 | |
| | | | 5V | 5V | 1.4 | | 3.1 | |
| $I_{CCA} + I_{CCB}$ | Supply Current - AC Signal | All channels switching with square wave clock input; $C_L$ = 15pF, 1Mbps | 1.8V | 1.8V | 1.5 | | 2.6 | mA |
| | | | 2.5V | 2.5V | 1.6 | | 2.7 | |
| | | | 3.3V | 3.3V | 1.6 | | 2.8 | |
| | | | 5V | 5V | 1.9 | | 3.3 | |
| | | All channels switching with square wave clock input; $C_L$ = 15pF, 50Mbps | 1.8V | 1.8V | 9.5 | | 12.9 | |
| | | | 2.5V | 2.5V | 10.6 | | 13.9 | |
| | | | 3.3V | 3.3V | 12.9 | | 15.9 | |
| | | | 5V | 5V | 17.7 | | 20.8 | |
| | | All channels switching with square wave clock input; $C_L$ = 15pF, 100Mbps | 1.8V | 1.8V | 16.5 | | 20 | |
| | | | 2.5V | 2.5V | 20.5 | | 25.2 | |
| | | | 3.3V | 3.3V | 24.4 | | 28.7 | |
| | | | 5V | 5V | 34.9 | | 38.4 | |

(1) $V_{CCI}$ is the $V_{CC}$ associated with the input port
(2) $V_{CCO}$ is the $V_{CC}$ associated with the output port
(3) Floating is defined as a node that is both not actively driven by an external device and has leakage not exeeding 10nA

ADVANCE INFORMATION

ADVANCE INFORMATION

## 5.7 Switching Characteristics, $V_{CCA}$ = 1.8 ± 0.15V

| PARAMETER | | TEST CONDITIONS | FROM | TO | TEMPERATURE | B-Port Supply Voltage ($V_{CCB}$) | | | | | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | 1.8 ± 0.15V | | | 2.5 ± 0.2V | | | 3.3 ± 0.3V | | | 5.0 ± 0.5V | | | |
| | | | | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| $t_{pd}$ | Propagation delay | 1Mbps all 4 channels toggling | A | B | -40°C to 85°C | 3 | | 7.4 | 3 | | 7.5 | 3.1 | | 7.5 | 3.1 | | 7.9 | ns |
| | | | A | B | -40°C to 125°C | 3 | | 7.8 | 3 | | 7.8 | 3.1 | | 7.9 | 3.1 | | 8.4 | |
| | | | B | A | -40°C to 85°C | 3 | | 7.4 | 2.8 | | 5.8 | 2.8 | | 5.2 | 2.8 | | 4.9 | |
| | | | B | A | -40°C to 125°C | 3 | | 7.8 | 2.8 | | 6.1 | 2.8 | | 5.5 | 2.8 | | 5.2 | |
| $t_{dis}$ | Disable time | | OE | A | -40°C to 85°C | 16.1 | | 35 | 16.1 | | 35 | 16.1 | | 35 | 16.1 | | 35 | ns |
| | | | OE | A | -40°C to 125°C | 16.1 | | 35.6 | 16.1 | | 35.5 | 16.1 | | 35.6 | 16.1 | | 35.6 | |
| | | | OE | B | -40°C to 85°C | 17.6 | | 40.9 | 12.6 | | 28.2 | 14.7 | | 27.4 | 10 | | 18.8 | |
| | | | OE | B | -40°C to 125°C | 17.6 | | 42 | 12.6 | | 29.1 | 14.7 | | 28 | 10 | | 19.3 | |
| $t_{en}$ | Enable time | | OE | A | -40°C to 85°C | 5.4 | | 18.1 | 5.4 | | 18.1 | 5.4 | | 18.1 | 5.4 | | 18.1 | ns |
| | | | OE | A | -40°C to 125°C | 5.4 | | 18.9 | 5.4 | | 18.8 | 5.4 | | 18.9 | 5.4 | | 18.8 | |
| | | | OE | B | -40°C to 85°C | 7.5 | | 26.5 | 5.5 | | 15.3 | 4.5 | | 11 | 3.8 | | 7.9 | |
| | | | OE | B | -40°C to 125°C | 7.9 | | 27.5 | 5.5 | | 16.3 | 4.5 | | 11.8 | 3.8 | | 8.4 | |
| PWD | Pulse width distortion | $\lvert t_{phl} - t_{plh} \rvert$ | A | B | -40°C to 85°C | 0.7 | | 1.5 | 0.6 | | 1.4 | 0.6 | | 1.3 | 0.5 | | 1.2 | ns |
| | | | A | B | -40°C to 125°C | 0.7 | | 1.5 | 0.6 | | 1.4 | 0.6 | | 1.3 | 0.5 | | 1.2 | |
| | | | B | A | -40°C to 85°C | 0.7 | | 1.5 | 0.6 | | 1.4 | 0.6 | | 1.3 | 0.5 | | 1.2 | |
| | | | B | A | -40°C to 125°C | 0.7 | | 1.5 | 0.6 | | 1.4 | 0.6 | | 1.3 | 0.5 | | 1.2 | |
| $t_r$ | Output signal rise time | | A | B | -40°C to 85°C | 0.6 | | 1.1 | 0.5 | | 1.2 | 0.5 | | 1.5 | 0.6 | | 1.8 | ns |
| | | | A | B | -40°C to 125°C | 0.6 | | 1.3 | 0.5 | | 1.5 | 0.5 | | 1.6 | 0.6 | | 1.9 | |
| | | | B | A | -40°C to 85°C | 0.5 | | 0.9 | 0.5 | | 1 | 0.5 | | 0.9 | 0.5 | | 0.9 | |
| | | | B | A | -40°C to 125°C | 0.5 | | 1 | 0.5 | | 1.1 | 0.5 | | 1 | 0.5 | | 1.1 | |
| tf | Output signal fall time | | A | B | -40°C to 85°C | 0.5 | | 1.3 | 0.5 | | 1.6 | 0.5 | | 1.6 | 0.6 | | 1.9 | ns |
| | | | A | B | -40°C to 125°C | 0.5 | | 1.6 | 0.5 | | 1.8 | 0.5 | | 1.9 | 0.6 | | 2.2 | |
| | | | B | A | -40°C to 85°C | 0.5 | | 1.1 | 0.5 | | 1.1 | 0.5 | | 1.1 | 0.5 | | 1.1 | |
| | | | B | A | -40°C to 125°C | 0.5 | | 1.4 | 0.5 | | 1.5 | 0.5 | | 1.4 | 0.5 | | 1.4 | |
| $t_{DO}$ | Default output delay time from input power loss | Measured from the time $V_{CC}$ goes below 1.36V | | | -40°C to 85°C | | | 8.4 | | | 8.3 | | | 8.2 | | | 8 | µs |
| | | | | | -40°C to 125°C | | | 8.4 | | | 8.3 | | | 8.2 | | | 8 | |
| $t_{PU}$ | Time from ULVO to valid output data | | | | -40°C to 85°C | | | 66.8 | | | 66.8 | | | 66.8 | | | 66.9 | µs |
| | | | | | -40°C to 125°C | | | 66.8 | | | 66.8 | | | 66.8 | | | 66.9 | |

## 5.8 Switching Characteristics, $V_{CCA}$ = 2.5 ± 0.2V

| PARAMETER | | TEST CONDITIONS | FROM | TO | TEMPERATURE | B-Port Supply Voltage ($V_{CCB}$) | | | | | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | 1.8 ± 0.15V | | | 2.5 ± 0.2V | | | 3.3 ± 0.3V | | | 5.0 ± 0.5V | | | |
| | | | | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| $t_{pd}$ | Propagation delay | 1Mbps all 4 channels toggling | A | B | -40°C to 85°C | 2.9 | | 5.9 | 2.9 | | 5.9 | 2.9 | | 6 | 3 | | 6.2 | ns |
| | | | A | B | -40°C to 125°C | 2.9 | | 6.1 | 2.9 | | 6.2 | 2.9 | | 6.3 | 3 | | 6.6 | |
| | | | B | A | -40°C to 85°C | 3 | | 7.4 | 2.9 | | 5.9 | 2.8 | | 5.2 | 2.8 | | 5 | |
| | | | B | A | -40°C to 125°C | 3 | | 7.8 | 2.9 | | 6.2 | 2.8 | | 5.6 | 2.8 | | 5.4 | |
| $t_{dis}$ | Disable time | | OE | A | -40°C to 85°C | 11.6 | | 24.7 | 11.6 | | 24.7 | 11.6 | | 24.7 | 11.6 | | 24.7 | ns |
| | | | OE | A | -40°C to 125°C | 11.6 | | 25.2 | 11.6 | | 25.2 | 11.6 | | 25.2 | 11.6 | | 25.2 | |
| | | | OE | B | -40°C to 85°C | 17.6 | | 40.9 | 12.6 | | 28.3 | 14.7 | | 27.4 | 10.1 | | 18.8 | |
| | | | OE | B | -40°C to 125°C | 17.6 | | 41.9 | 12.6 | | 29.1 | 14.7 | | 28 | 10.1 | | 19.3 | |
| $t_{en}$ | Enable time | | OE | A | -40°C to 85°C | 3.8 | | 10.9 | 3.8 | | 10.9 | 3.8 | | 10.9 | 3.8 | | 10.9 | ns |
| | | | OE | A | -40°C to 125°C | 3.8 | | 11.6 | 3.8 | | 11.6 | 3.8 | | 11.6 | 3.8 | | 11.6 | |
| | | | OE | B | -40°C to 85°C | 7.5 | | 26.5 | 5.5 | | 15.3 | 4.5 | | 11 | 3.8 | | 7.8 | |
| | | | OE | B | -40°C to 125°C | 7.9 | | 27.5 | 5.5 | | 16.3 | 4.5 | | 11.8 | 3.8 | | 8.4 | |
| PWD | Pulse width distortion | $\|t_{phl} - t_{plh}\|$ | A | B | -40°C to 85°C | 0.1 | | 0.6 | 0.1 | | 0.57 | 0.002 | | 0.56 | 0.002 | | 0.48 | ns |
| | | | A | B | -40°C to 125°C | 0.1 | | 0.6 | 0.1 | | 0.57 | 0.002 | | 0.56 | 0.002 | | 0.48 | |
| | | | B | A | -40°C to 85°C | 0.1 | | 0.6 | 0.1 | | 0.57 | 0.002 | | 0.56 | 0.002 | | 0.48 | |
| | | | B | A | -40°C to 125°C | 0.1 | | 0.6 | 0.1 | | 0.57 | 0.002 | | 0.56 | 0.002 | | 0.48 | |
| $t_r$ | Output signal rise time | | A | B | -40°C to 85°C | 0.6 | | 1.1 | 0.5 | | 1.2 | 0.5 | | 1.5 | 0.6 | | 1.8 | ns |
| | | | A | B | -40°C to 125°C | 0.6 | | 1.3 | 0.5 | | 1.4 | 0.5 | | 1.7 | 0.6 | | 1.9 | |
| | | | B | A | -40°C to 85°C | 0.5 | | 1 | 0.5 | | 1 | 0.5 | | 1 | 0.5 | | 1 | |
| | | | B | A | -40°C to 125°C | 0.5 | | 1.1 | 0.5 | | 1.2 | 0.5 | | 1.2 | 0.5 | | 1.1 | |
| tf | Output signal fall time | | A | B | -40°C to 85°C | 0.5 | | 1.2 | 0.5 | | 1.5 | 0.5 | | 1.7 | 0.5 | | 1.9 | ns |
| | | | A | B | -40°C to 125°C | 0.5 | | 1.6 | 0.5 | | 1.7 | 0.5 | | 1.8 | 0.5 | | 2.1 | |
| | | | B | A | -40°C to 85°C | 0.5 | | 1.3 | 0.5 | | 1.3 | 0.5 | | 1.4 | 0.5 | | 1.3 | |
| | | | B | A | -40°C to 125°C | 0.5 | | 1.5 | 0.5 | | 1.5 | 0.5 | | 1.5 | 0.5 | | 1.6 | |
| $t_{DO}$ | Default output delay time from input power loss | Measured from the time $V_{CC}$ goes below 1.36V | | | -40°C to 85°C | | | 8.1 | | | 8.1 | | | 8 | | | 7.8 | µs |
| | | | | | -40°C to 125°C | | | 8.1 | | | 8.1 | | | 8 | | | 7.8 | |
| $t_{PU}$ | Time from ULVO to valid output data | | | | -40°C to 85°C | | | 71.3 | | | 71.3 | | | 71.3 | | | 71.3 | µs |
| | | | | | -40°C to 125°C | | | 71.3 | | | 71.3 | | | 71.3 | | | 71.3 | |

## 5.9 Switching Characteristics, $V_{CCA}$ = 3.3 ± 0.3V

| PARAMETER | | TEST CONDITIONS | FROM | TO | TEMPERATURE | B-Port Supply Voltage ($V_{CCB}$) | | | | | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | 1.8 ± 0.15V | | | 2.5 ± 0.2V | | | 3.3 ± 0.3V | | | 5.0 ± 0.5V | | | |
| | | | | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| $t_{pd}$ | Propagation delay | 1Mbps all 4 channels toggling | A | B | -40°C to 85°C | 2.9 | | 5.2 | 2.9 | | 5.3 | 2.8 | | 5.4 | 3 | | 5.7 | ns |
| | | | A | B | -40°C to 125°C | 2.9 | | 5.5 | 2.9 | | 5.6 | 2.8 | | 5.8 | 3 | | 6.1 | |
| | | | B | A | -40°C to 85°C | 3 | | 7.5 | 2.9 | | 5.9 | 2.8 | | 5.3 | 2.8 | | 5.1 | |
| | | | B | A | -40°C to 125°C | 3 | | 7.9 | 2.9 | | 6.3 | 2.8 | | 5.7 | 2.8 | | 5.5 | |
| $t_{dis}$ | Disable time | | OE | A | -40°C to 85°C | 13.9 | | 25.3 | 13.8 | | 25.3 | 13.8 | | 25.3 | 13.8 | | 25.3 | ns |
| | | | OE | A | -40°C to 125°C | 13.9 | | 25.7 | 13.8 | | 25.7 | 13.8 | | 25.7 | 13.8 | | 25.7 | |
| | | | OE | B | -40°C to 85°C | 17.6 | | 40.9 | 12.6 | | 28.2 | 14.7 | | 27.4 | 10.1 | | 18.8 | |
| | | | OE | B | -40°C to 125°C | 17.6 | | 41.9 | 12.6 | | 29 | 14.7 | | 28 | 10.1 | | 19.3 | |
| $t_{en}$ | Enable time | | OE | A | -40°C to 85°C | 3 | | 8 | 3.1 | | 8 | 3.1 | | 8 | 3 | | 8 | ns |
| | | | OE | A | -40°C to 125°C | 3 | | 8.5 | 3.1 | | 8.5 | 3.1 | | 8.6 | 3 | | 8.5 | |
| | | | OE | B | -40°C to 85°C | 7.5 | | 26.5 | 5.5 | | 15.3 | 4.5 | | 11 | 3.8 | | 7.8 | |
| | | | OE | B | -40°C to 125°C | 8 | | 27.5 | 5.5 | | 16.3 | 4.5 | | 11.8 | 3.8 | | 8.4 | |
| PWD | Pulse width distortion | $\|t_{phl} - t_{plh}\|$ | A | B | -40°C to 85°C | 0.006 | | 0.37 | 0.002 | | 0.37 | 0.001 | | 0.34 | 0 | | 0.36 | ns |
| | | | A | B | -40°C to 125°C | 0.006 | | 0.37 | 0.002 | | 0.37 | 0.001 | | 0.34 | 0 | | 0.36 | |
| | | | B | A | -40°C to 85°C | 0.006 | | 0.37 | 0.002 | | 0.37 | 0.001 | | 0.34 | 0 | | 0.36 | |
| | | | B | A | -40°C to 125°C | 0.006 | | 0.37 | 0.002 | | 0.37 | 0.001 | | 0.34 | 0 | | 0.36 | |
| $t_r$ | Output signal rise time | | A | B | -40°C to 85°C | 0.6 | | 1.1 | 0.6 | | 1.2 | 0.5 | | 1.5 | 0.6 | | 1.8 | ns |
| | | | A | B | -40°C to 125°C | 0.6 | | 1.3 | 0.6 | | 1.5 | 0.5 | | 1.7 | 0.6 | | 1.9 | |
| | | | B | A | -40°C to 85°C | 0.6 | | 1.1 | 0.6 | | 1.2 | 0.5 | | 1.5 | 0.6 | | 1.8 | |
| | | | B | A | -40°C to 125°C | 0.6 | | 1.3 | 0.6 | | 1.5 | 0.5 | | 1.7 | 0.6 | | 1.9 | |
| tf | Output signal fall time | | A | B | -40°C to 85°C | 0.5 | | 1.2 | 0.5 | | 1.6 | 0.5 | | 1.6 | 0.6 | | 1.9 | ns |
| | | | A | B | -40°C to 125°C | 0.5 | | 1.7 | 0.5 | | 1.7 | 0.5 | | 1.8 | 0.6 | | 2.1 | |
| | | | B | A | -40°C to 85°C | 0.5 | | 1.4 | 0.5 | | 1.5 | 0.5 | | 1.4 | 0.5 | | 1.5 | |
| | | | B | A | -40°C to 125°C | 0.5 | | 1.7 | 0.5 | | 1.7 | 0.5 | | 1.7 | 0.5 | | 1.6 | |
| $t_{DO}$ | Default output delay time from input power loss | Measured from the time $V_{CC}$ goes below 1.36V | | | -40°C to 85°C | | | 8 | | | 7.9 | | | 7.9 | | | 7.7 | μs |
| | | | | | -40°C to 125°C | | | 8 | | | 7.9 | | | 7.9 | | | 7.7 | μs |
| $t_{PU}$ | Time from ULVO to valid output data | | | | -40°C to 85°C | | | 79.1 | | | 79.1 | | | 79.1 | | | 79.1 | μs |
| | | | | | -40°C to 125°C | | | 79.1 | | | 79.1 | | | 79.1 | | | 79.1 | μs |

## 5.10 Switching Characteristics, $V_{CCA}$ = 5.0 ± 0.5V

| PARAMETER | | TEST CONDITIONS | FROM | TO | TEMPERATURE | B-Port Supply Voltage ($V_{CCB}$) 1.8 ± 0.15V | | | 2.5 ± 0.2V | | | 3.3 ± 0.3V | | | 5.0 ± 0.5V | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| $t_{pd}$ | Propagation delay | 1Mbps all 4 channels toggling | A | B | -40°C to 85°C | 2.8 | | 5 | 2.8 | | 5 | 2.9 | | 5.2 | 2.9 | | 5.5 | ns |
| | | | A | B | -40°C to 125°C | 2.8 | | 5.3 | 2.8 | | 5.3 | 2.9 | | 5.6 | 2.9 | | 5.9 | |
| | | | B | A | -40°C to 85°C | 3.1 | | 7.8 | 3 | | 6.3 | 2.9 | | 5.7 | 2.8 | | 5.6 | |
| | | | B | A | -40°C to 125°C | 3.1 | | 8.3 | 3 | | 6.6 | 2.9 | | 6.1 | 2.8 | | 5.8 | |
| $t_{dis}$ | Disable time | | OE | A | -40°C to 85°C | 9.4 | | 17.4 | 9.4 | | 17.4 | 9.4 | | 17.4 | 9.4 | | 17.4 | ns |
| | | | OE | A | -40°C to 125°C | 9.4 | | 17.7 | 9.4 | | 17.7 | 9.4 | | 17.7 | 9.4 | | 17.7 | |
| | | | OE | B | -40°C to 85°C | 17.7 | | 40.9 | 12.6 | | 28.3 | 14.7 | | 27.4 | 10.1 | | 18.8 | |
| | | | OE | B | -40°C to 125°C | 17.7 | | 41.9 | 12.6 | | 29.1 | 14.7 | | 28 | 10.1 | | 19.4 | |
| $t_{en}$ | Enable time | | OE | A | -40°C to 85°C | 2.5 | | 5.9 | 2.5 | | 5.9 | 2.5 | | 5.9 | 2.5 | | 5.9 | ns |
| | | | OE | A | -40°C to 125°C | 2.5 | | 6.3 | 2.5 | | 6.3 | 2.5 | | 6.3 | 2.5 | | 6.3 | |
| | | | OE | B | -40°C to 85°C | 7.5 | | 26.5 | 5.5 | | 15.3 | 4.5 | | 11 | 3.8 | | 7.8 | |
| | | | OE | B | -40°C to 125°C | 8 | | 27.5 | 5.5 | | 16.3 | 4.5 | | 11.8 | 3.8 | | 8.4 | |
| PWD | Pulse width distortion | $\|t_{phl} - t_{plh}\|$ | A | B | -40°C to 85°C | 0 | | 0.2 | 0 | | 0.3 | 0.003 | | 0.4 | 0.011 | | 0.7 | ns |
| | | | A | B | -40°C to 125°C | 0 | | 0.2 | 0 | | 0.3 | 0.003 | | 0.4 | 0.011 | | 0.7 | |
| | | | B | A | -40°C to 85°C | 0 | | 0.2 | 0 | | 0.3 | 0.003 | | 0.4 | 0.011 | | 0.7 | |
| | | | B | A | -40°C to 125°C | 0 | | 0.2 | 0 | | 0.3 | 0.003 | | 0.4 | 0.011 | | 0.7 | |
| $t_r$ | Output signal rise time | | A | B | -40°C to 85°C | 0.6 | | 1.1 | 0.5 | | 1.1 | 0.5 | | 1.6 | 0.6 | | 1.8 | ns |
| | | | A | B | -40°C to 125°C | 0.6 | | 1.3 | 0.5 | | 1.5 | 0.5 | | 1.7 | 0.6 | | 1.9 | |
| | | | B | A | -40°C to 85°C | 0.5 | | 1.6 | 0.5 | | 1.6 | 0.5 | | 1.7 | 0.5 | | 1.7 | |
| | | | B | A | -40°C to 125°C | 0.5 | | 1.7 | 0.5 | | 1.7 | 0.5 | | 1.8 | 0.5 | | 1.7 | |
| tf | Output signal fall time | | A | B | -40°C to 85°C | 0.5 | | 1.4 | 0.4 | | 1.6 | 0.5 | | 1.8 | 0.6 | | 1.9 | ns |
| | | | A | B | -40°C to 125°C | 0.5 | | 1.7 | 0.5 | | 1.7 | 0.5 | | 1.8 | 0.6 | | 2.2 | |
| | | | B | A | -40°C to 85°C | 0.5 | | 1.4 | 0.5 | | 1.6 | 0.5 | | 1.8 | 0.6 | | 1.9 | |
| | | | B | A | -40°C to 125°C | 0.5 | | 1.7 | 0.5 | | 1.7 | 0.5 | | 1.8 | 0.6 | | 2.2 | |
| $t_{DO}$ | Default output delay time from input power loss | Measured from the time $V_{CC}$ goes below 1.36V | | | -40°C to 85°C | | | 7.9 | | | 7.8 | | | 7.7 | | | 7.6 | µs |
| | | | | | -40°C to 125°C | | | 7.9 | | | 7.8 | | | 7.7 | | | 7.6 | |
| $t_{PU}$ | Time from ULVO to valid output data | | | | -40°C to 85°C | | | 98.3 | | | 98.3 | | | 98.3 | | | 98.3 | µs |
| | | | | | -40°C to 125°C | | | 98.3 | | | 98.3 | | | 98.3 | | | 98.3 | |

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## 5.11 Switching Characteristics: $T_{sk}$, $T_{MAX}$

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | $V_{CCI}$ | $V_{CCO}$ | Operating free-air temperature ($T_A$) -40°C to 125°C MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $T_{MAX}$ - Maximum Data Rate | 50% Duty Cycle Input<br>One channel switching<br>20% of pulse > 0.7*$V_{CCO}$<br>20% of pulse < 0.3*$V_{CCO}$ | No Translation | 1.65V - 1.95V | 1.65V - 1.95V | 264 | | | Mbps |
| | | | 2.3V - 2.7V | 2.3V - 2.7V | 264 | | | Mbps |
| | | | 3.0V - 3.6V | 3.0V - 3.6V | 176 | | | Mbps |
| | | | 4.5V - 5.5V | 4.5V - 5.5V | 176 | | | Mbps |
| $T_{MAX}$ - Maximum Data Rate | 50% Duty Cycle Input<br>One channel switching<br>20% of pulse > 0.7*$V_{CCO}$<br>20% of pulse < 0.3*$V_{CCO}$ | Up Translation | 1.65V - 1.95V | 2.3V - 2.7V | 264 | | | Mbps |
| | | | 1.65V - 1.95V | 3.0V - 3.6V | 264 | | | Mbps |
| | | | 1.65V - 1.95V | 4.5V - 5.5V | 264 | | | Mbps |
| | | | 2.3V - 2.7V | 3.0V - 3.6V | 264 | | | Mbps |
| | | | 2.3V - 2.7V | 4.5V - 5.5V | 220 | | | Mbps |
| | | | 3.0V - 3.6V | 4.5V - 5.5V | 176 | | | Mbps |
| $T_{MAX}$ - Maximum Data Rate | 50% Duty Cycle Input<br>One channel switching<br>20% of pulse > 0.7*$V_{CCO}$<br>20% of pulse < 0.3*$V_{CCO}$ | Down Translation | 2.3V - 2.7V | 1.65V - 1.95V | 285 | | | Mbps |
| | | | 3.0V - 3.6V | 2.3V - 2.7V | 220 | | | Mbps |
| | | | 3.0V - 3.6V | 1.65V - 1.95V | 220 | | | Mbps |
| | | | 4.5V - 5.5V | 3.0V - 3.6V | 176 | | | Mbps |
| | | | 4.5V - 5.5V | 2.3V - 2.7V | 220 | | | Mbps |
| | | | 4.5V - 5.5V | 1.65V - 1.95V | 220 | | | Mbps |
| $t_{sk}$ - Output skew | Timing skew between any switching outputs on the rising or falling edge (same direction channels) | No Translation | 1.65V - 1.95V | 1.65V - 1.95V | | | 0.35 | ns |
| | | | 2.3V - 2.7V | 2.3V - 2.7V | | | 0.35 | ns |
| | | | 3.0V - 3.6V | 3.0V - 3.6V | | | 0.35 | ns |
| | | | 4.5V - 5.5V | 4.5V - 5.5V | | | 0.35 | ns |
| $t_{sk}$ - Output skew | Timing skew between any switching outputs on the rising or falling edge (same direction channels) | Up Translation | 1.65V - 1.95V | 2.3V - 2.7V | | | 0.35 | ns |
| | | | 1.65V - 1.95V | 3.0V - 3.6V | | | 0.35 | ns |
| | | | 1.65V - 1.95V | 4.5V - 5.5V | | | 0.35 | ns |
| | | | 2.3V - 2.7V | 3.0V - 3.6V | | | 0.35 | ns |
| | | | 2.3V - 2.7V | 4.5V - 5.5V | | | 0.35 | ns |
| | | | 3.0V - 3.6V | 4.5V - 5.5V | | | 0.35 | ns |

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | $V_{CCI}$ | $V_{CCO}$ | Operating free-air temperature ($T_A$) -40°C to 125°C MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $t_{sk}$ - Output skew | Timing skew between any switching outputs on the rising or falling edge (same direction channels) | Down Translation | 2.3V - 2.7V | 1.65V - 1.95V | | | 0.35 | ns |
| | | | 3.0V - 3.6V | 2.3V - 2.7V | | | 0.35 | ns |
| | | | 3.0V - 3.6V | 1.65V - 1.95V | | | 0.35 | ns |
| | | | 4.5V - 5.5V | 3.0V - 3.6V | | | 0.35 | ns |
| | | | 4.5V - 5.5V | 2.3V - 2.7V | | | 0.35 | ns |
| | | | 4.5V - 5.5V | 1.65V - 1.95V | | | 0.35 | ns |

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### 5.12 Typical Characteristics

$T_A$ = 25°C (unless otherwise noted)

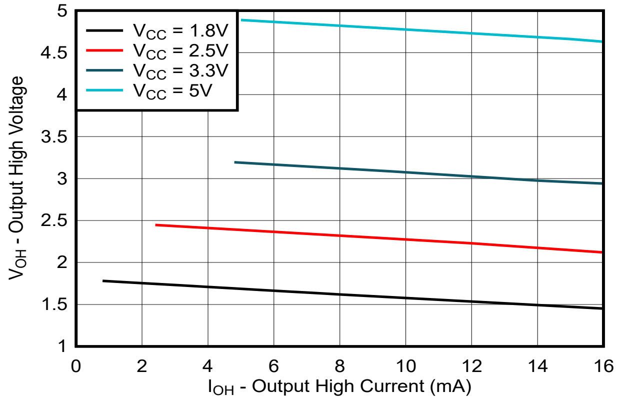


**Figure 5-1. Output High Voltage ($V_{OH}$) vs Source Current ($I_{OH}$)**

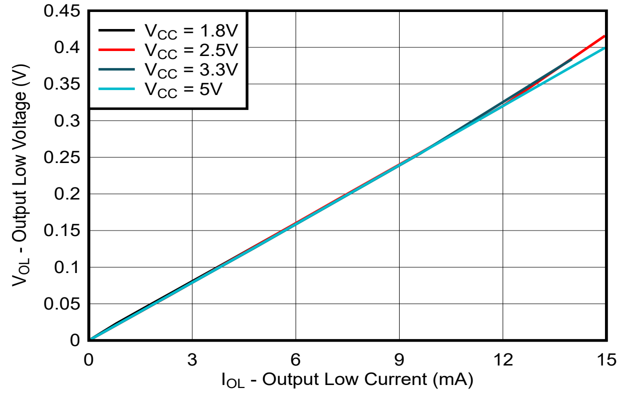


**Figure 5-2. Output Low Voltage ($V_{OL}$) vs Sink Current ($I_{OL}$)**

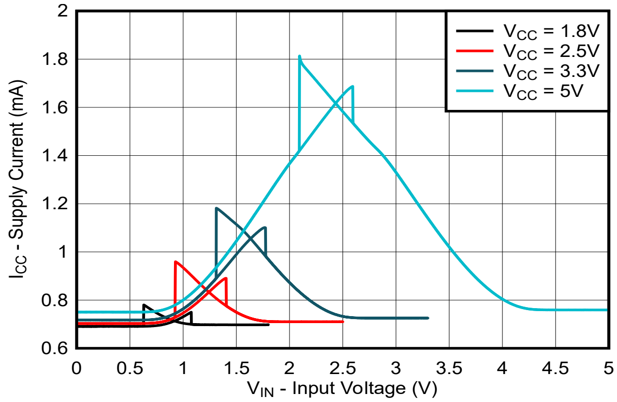


**Figure 5-3. Supply Current ($I_{CC}$) vs Input Voltage ($V_{IN}$) [TXG0x041]**

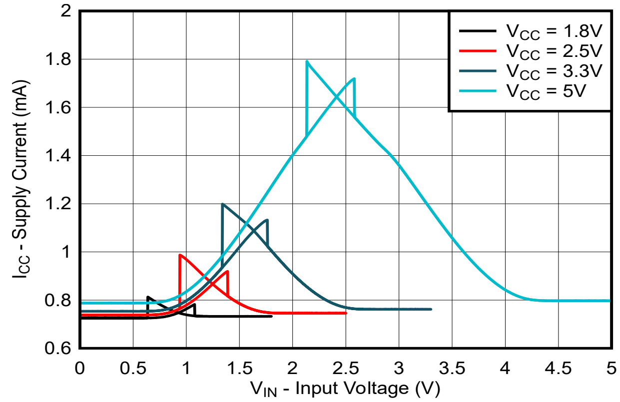


**Figure 5-4. Supply Current ($I_{CC}$) vs Input Voltage ($V_{IN}$) [TXGx042]**

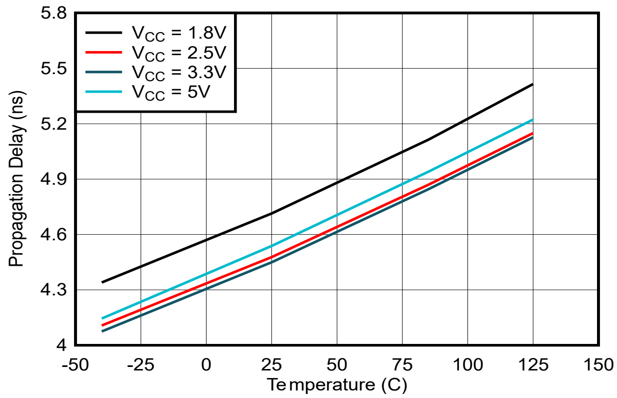


**Figure 5-5. Propagation Delay, $T_{PLH}$, vs Temperature**

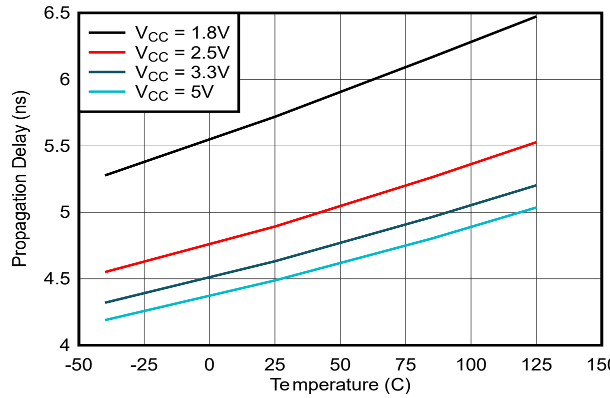


**Figure 5-6. Propagation Delay, $T_{PHL}$, vs Temperature**

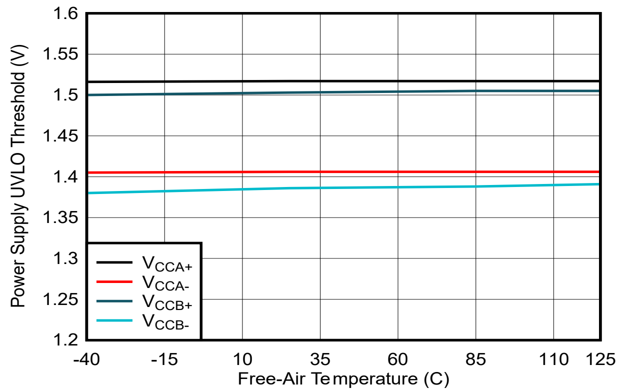


**Figure 5-7. Power Supply Undervoltage Threshold vs Free-Air Temperature**

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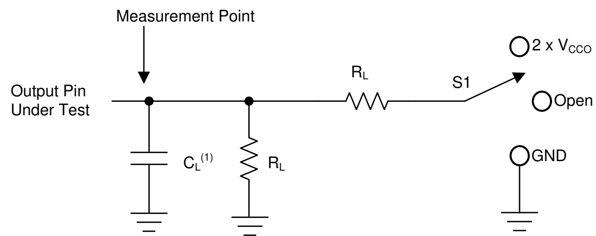
# 6 Parameter Measurement Information

## 6.1 Load Circuit and Voltage Waveforms

Unless otherwise noted, generators supply all input pulses that have the following characteristics:

- f = 1MHz
- $Z_O$ = 50Ω
- Δt/ΔV ≤ 1ns/V

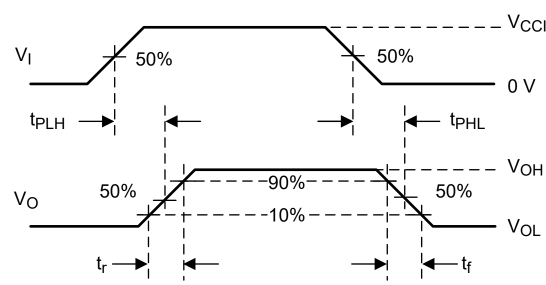



A. $C_L$ includes probe and jig capacitance.

**Figure 6-1. Load Circuit**

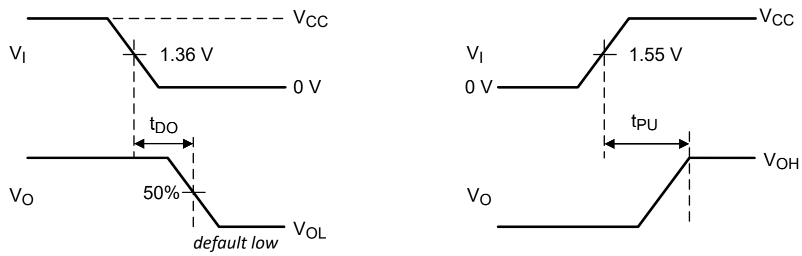
**Table 6-1. Load Circuit Conditions**

| Parameter | | $V_{CCO}$ | $R_L$ | $C_L$ | $S_1$ | $V_{TP}$ |
|---|---|---|---|---|---|---|
| $t_{pd}$ | Propagation (delay) time | 1.71V – 5.5V | 10kΩ | 15pF | Open | N/A |
| $t_{en}$, $t_{dis}$ | Enable time, disable time | 1.71V – 2.7V | 10kΩ | 15pF | 2 × $V_{CCO}$ | 0.15V |
| | | 3.0V – 5.5V | 10kΩ | 15pF | 2 × $V_{CCO}$ | 0.3V |
| $t_{en}$, $t_{dis}$ | Enable time, disable time | 1.71V – 2.7V | 10kΩ | 15pF | GND | 0.15V |
| | | 3.0V – 5.5V | 10kΩ | 15pF | GND | 0.3V |



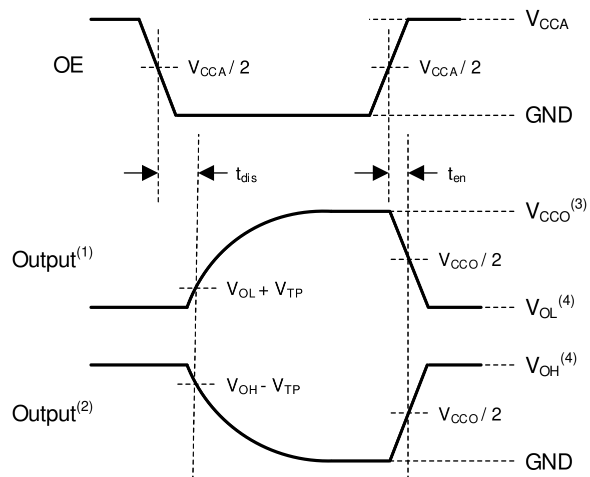

1. $V_{CCI}$ is the supply pin associated with the input port.
2. $V_{OH}$ and $V_{OL}$ are typical output voltage levels that occur with specified $R_L$, $C_L$, and $S_1$

**Figure 6-2. Switching Characteristics Voltage Waveforms**




1. $V_{CCI}$ is the supply pin associated with the input port.
2. $V_{OH}$ and $V_{OL}$ are typical output voltage levels that occur with specified $R_L$, $C_L$, and $S_1$

**Figure 6-3. Default Output Delay Time & Time from UVLO to Valid Output Voltage Waveform**




1. Output waveform on the condition that input is driven to a valid Logic Low.
2. Output waveform on the condition that input is driven to a valid Logic High.
3. $V_{CCO}$ is the supply pin associated with the output port.
4. $V_{OH}$ and $V_{OL}$ are typical output voltage levels with specified $R_L$, $C_L$, and $S_1$.

**Figure 6-4. Enable Time And Disable Time**

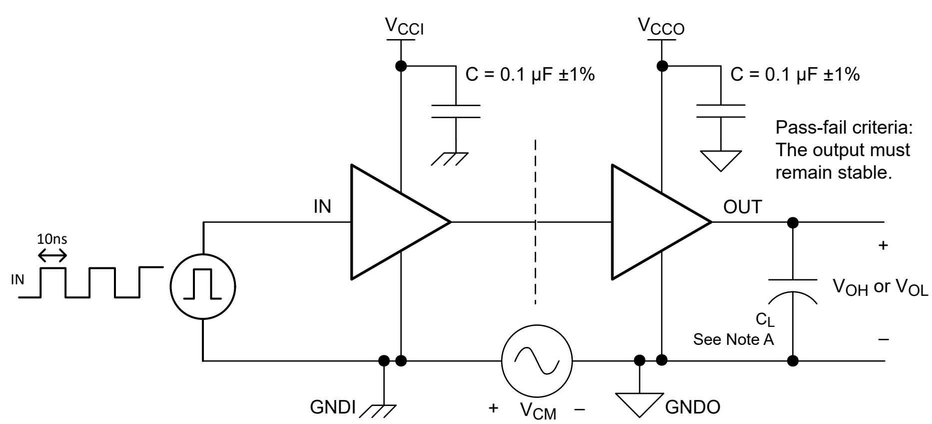



**Figure 6-5. Common-Mode Transient Immunity Test Circuit**

1. $C_L$ = 15pF and includes instrumentation and fixture capacitance within ±20%.

ADVANCE INFORMATION

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# 7 Detailed Description

## 7.1 Overview

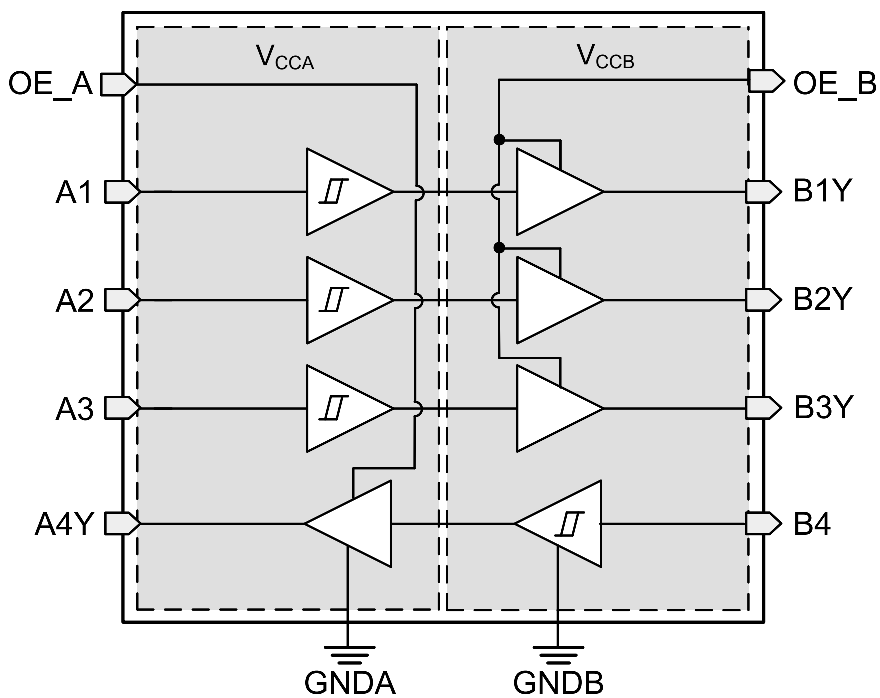
The TXG804x is a 4-bit ground-level translator that uses two individually configurable power-supply rails which allows it to translate across two different power domains. The device is operational with $V_{CCA}$ and $V_{CCB}$ supplies as low as 1.71V and as high as 5.5V. The A port is designed to track $V_{CCA}$ and the B port is designed to track $V_{CCB}$. In addition to I/O level shifting, this translator can support a difference of -80V to +80V between GNDA and GNDB. $V_{CCA}$ is referenced to GNDA and $V_{CCB}$ is referenced to GNDB.

The TXG804x device is designed for asynchronous communication between data buses, and transmits data with fixed direction from the A bus to the B bus on some channels and from the B bus to the A bus on the remaining channels. The output-enable input (OE) is used to disable the outputs so the buses are effectively isolated. The OE_A pin is referenced to $V_{CCA}$ and OE_B pin is referenced to $V_{CCB}$. The OE pin can be left floating or externally pulled down to ground to keep the translator outputs in a high-impedance state during power-up or power-down.

The $V_{CC}$ disconnect feature ensures that if $V_{CC}$ is disconnected with the complementary supply within recommended operating conditions, outputs are disabled and set to the high-impedance state while the supply current is maintained. The $I_{off\text{-}float}$ circuitry ensures that no excessive current is drawn from or sourced into an input or output while the supply is floating.

Glitch-free power supply sequencing allows either supply rail to be powered on or off in any order while providing robust power sequencing performance.

## 7.2 Functional Block Diagram




**TXG804x Functional Block Diagram**

## 7.3 Feature Description

### *7.3.1 CMOS Schmitt-Trigger Inputs with Integrated Pulldowns*

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Section 5.5*. The worst case resistance is calculated with the maximum input voltage, given in the *Section 5.1*, and the maximum input leakage current, given in the *Section 5.5*, using ohm's law (R = V ÷ I).

The Schmitt-trigger input architecture provides hysteresis as defined by $\Delta V_T$ in the *Section 5.5*, which makes this device extremely tolerant to slow or noisy inputs. Driving the inputs slowly will increase dynamic current consumption of the device. See *Understanding Schmitt Triggers* for additional information regarding Schmitt-trigger inputs.

#### 7.3.1.1 Inputs with Integrated Static Pull-Down Resistors

This device has 5MΩ typical integrated weak pull-downs for each input. This feature allows all inputs to be left floating without the concern for unstable outputs or increased current consumption. This also helps to reduce external component count for applications where not all channels are used or need to be fixed low. If an external pull-up is required, it should be no larger than 1MΩ to avoid contention with the 5MΩ internal pull-down.

### *7.3.2 Balanced High-Drive CMOS Push-Pull Outputs*

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. *Section 5.1* defines the electrical and thermal limits that must be followed at all times.

### *7.3.3 $V_{CC}$ Disconnect*

The outputs for this device are disabled and enter a high-impedance state when either supply is left floating (disconnected), and with the complementary supply within recommended operating conditions. It is recommended that the inputs are kept low before floating (disconnecting) either supply.

The $I_{CCx(floating)}$ in the *Section 5.5* specifies the maximum supply current. The $I_{off(float)}$ in the *Section 5.5* specifies the maximum leakage into or out of any input or output pin on the device.

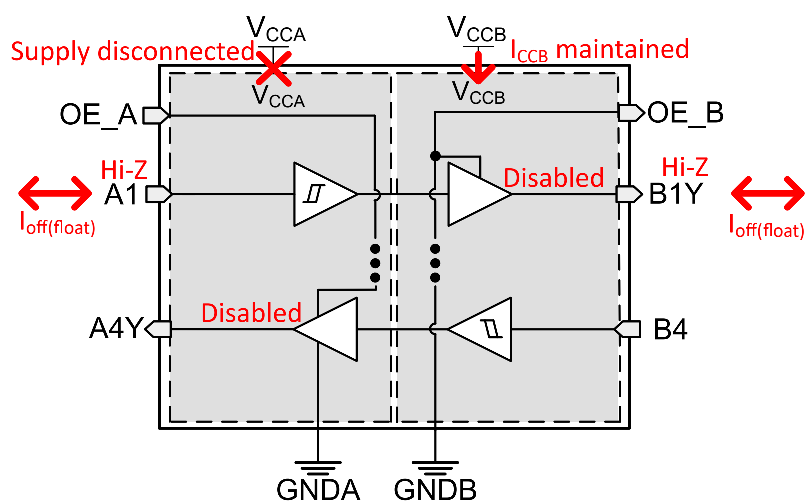



**Figure 7-1. $V_{CC}$ Disconnect Feature**

### *7.3.4 Over-Voltage Tolerant Inputs*

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the *Section 5.3*.

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### 7.3.5 Glitch-Free Power Supply Sequencing

Either supply rail may be powered on or off in any order without producing a glitch on the inputs or outputs (that is, where the output erroneously transitions to $V_{CC}$ when it should be held low or vice versa). Glitches of this nature can be misinterpreted by a peripheral as a valid data bit, which could trigger a false device reset of the peripheral, a false device configuration of the peripheral, or even a false data initialization by the peripheral.

### 7.3.6 Negative Clamping Diodes

Figure 7-2 depicts the inputs and outputs to this device that have negative clamping diodes.

> **CAUTION**
>
> Voltages beyond the values specified in the Section 5.1 table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

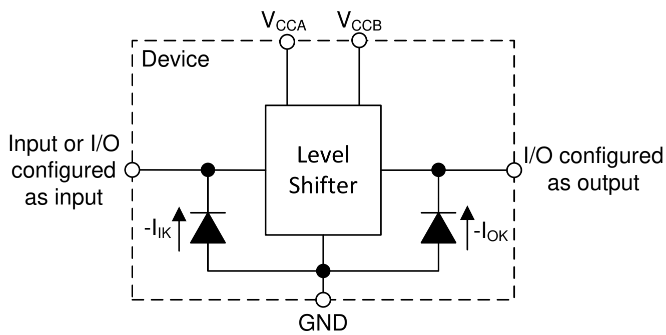


**Figure 7-2. Electrical Placement of Clamping Diodes for Each Input and Output**

### 7.3.7 Fully Configurable Dual-Rail Design

The $V_{CCA}$ and $V_{CCB}$ pins can be supplied at any voltage from 1.71V to 5.5V, making the device suitable for translating between any of the voltage nodes (1.8V, 2.5V, 3.3V, and 5.0V).

### 7.3.8 Supports High-Speed Translation

The TXG804x device can support high data-rate applications. The translated signal data rate can be greater than 250Mbps when the signal is translated from 1.71V to 5.5V.

### 7.3.9 AC Noise Rejection

TXG804x supports I/O voltage translation in environments with noisy grounds. The plot below illustrates the amount of noise that GNDA and GNDB can reject in terms peak-to-peak voltage over frequency without disrupting communication between two systems. As an example, Figure 7-4 below shows GNDA with a ground bounce of $2V_{PP}$ at 10kHz but still effectively translating 5V to 2.5V without any degradation.

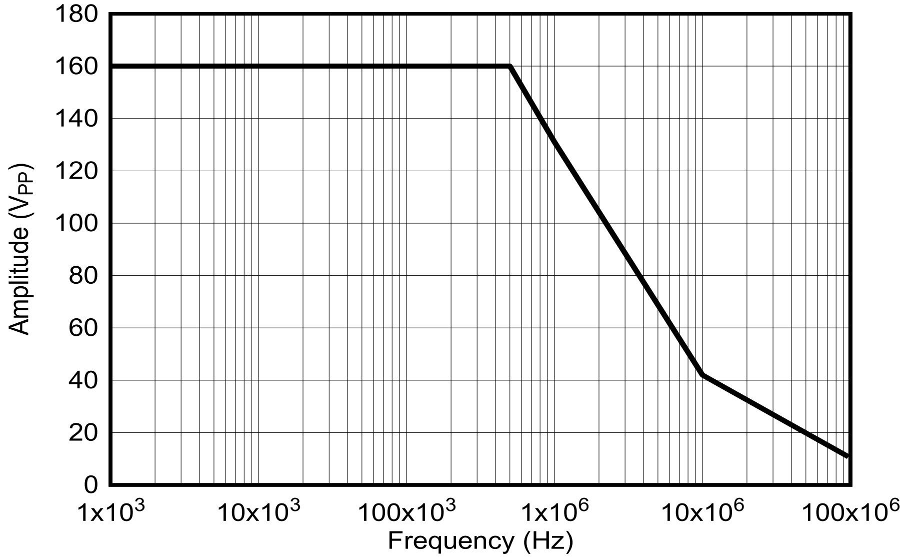


**Figure 7-3. AC Noise Rejection Plot**

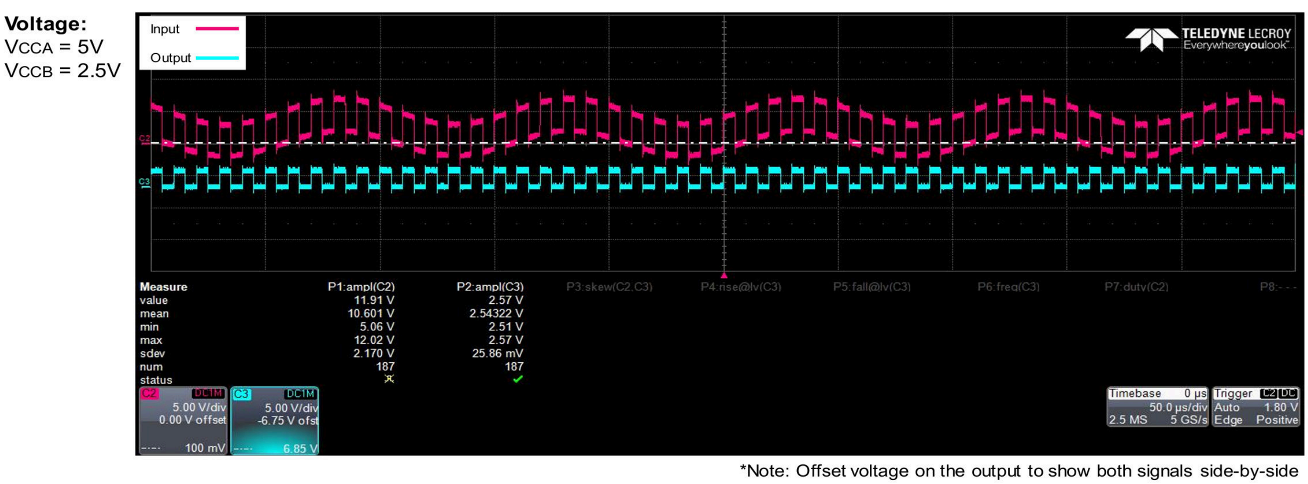


**Figure 7-4. Waveform showing 5V to 2.5V I/O translation with AC Ground Noise of $2V_{PP}$ at 10kHz**

ADVANCE INFORMATION

## 7.4 Device Functional Modes

**Table 7-1. Function Table**

| Power Supply | | Control Inputs | Port Status | |
|---|---|---|---|---|
| **VCCI** | **VCCO** | **OE** | **Input** | **Output** |
| PU | PU | H | H | H |
| PU | PU | H | L | L |
| PU | PU | L or Open | X | Hi-Z |
| PU | PU | H | Open | L |
| PD | PU | H | X | L |
| X | PU | L or Open | X | High-Z |
| X | PU | H | X | L |
| X | PD | X | X | Undetermined |

1. In the table above: PU = Powered Up; PD = Powered Down; X = Irrelevant; H = High Level; L = Low Level; Open = Floating

ADVANCE INFORMATION

# 8 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 8.1 Application Information

The TXG804x is used for level translation, enabling communication between devices or systems operating at different interface and ground voltages. The TXG804x device is ideal for use in applications where a push-pull driver is connected to the data inputs. Figure 8-1 is an example of two systems that translate from 1.8V to 3.3V across a SPI interface while also seeing a ground shift of -3V on GNDB while GNDA is at 0V. The ground shift of 3V is from the noisy power ground of the Digital-to-Analog Converter (DAC).

## 8.2 Typical Application

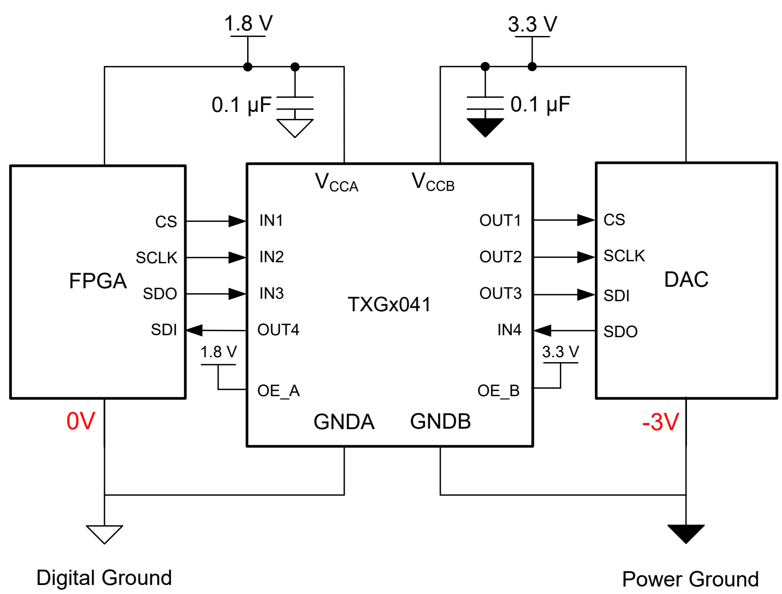


**Figure 8-1. TXG804x in Test and Measurement**

### *8.2.1 Design Requirements*

Use the parameters listed in Table 8-1 for this design example.

**Table 8-1. Design Parameters**

| DESIGN PARAMETERS | EXAMPLE VALUES |
|---|---|
| Input voltage range | 1.71V to 5.5V |
| Output voltage range | 1.71V to 5.5V |

### 8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the TXG804x device to determine the input voltage range. For a valid logic-high, the value must exceed the positive-going input-threshold voltage ($V_{T+}$) of the input port. For a valid logic low the value must be less than the negative-going input-threshold voltage ($V_{T-}$) of the input port.
- Output voltage range
  - Use the supply voltage of the device that the TXG804x device is driving to determine the output voltage range.

### 8.2.3 Application Curves

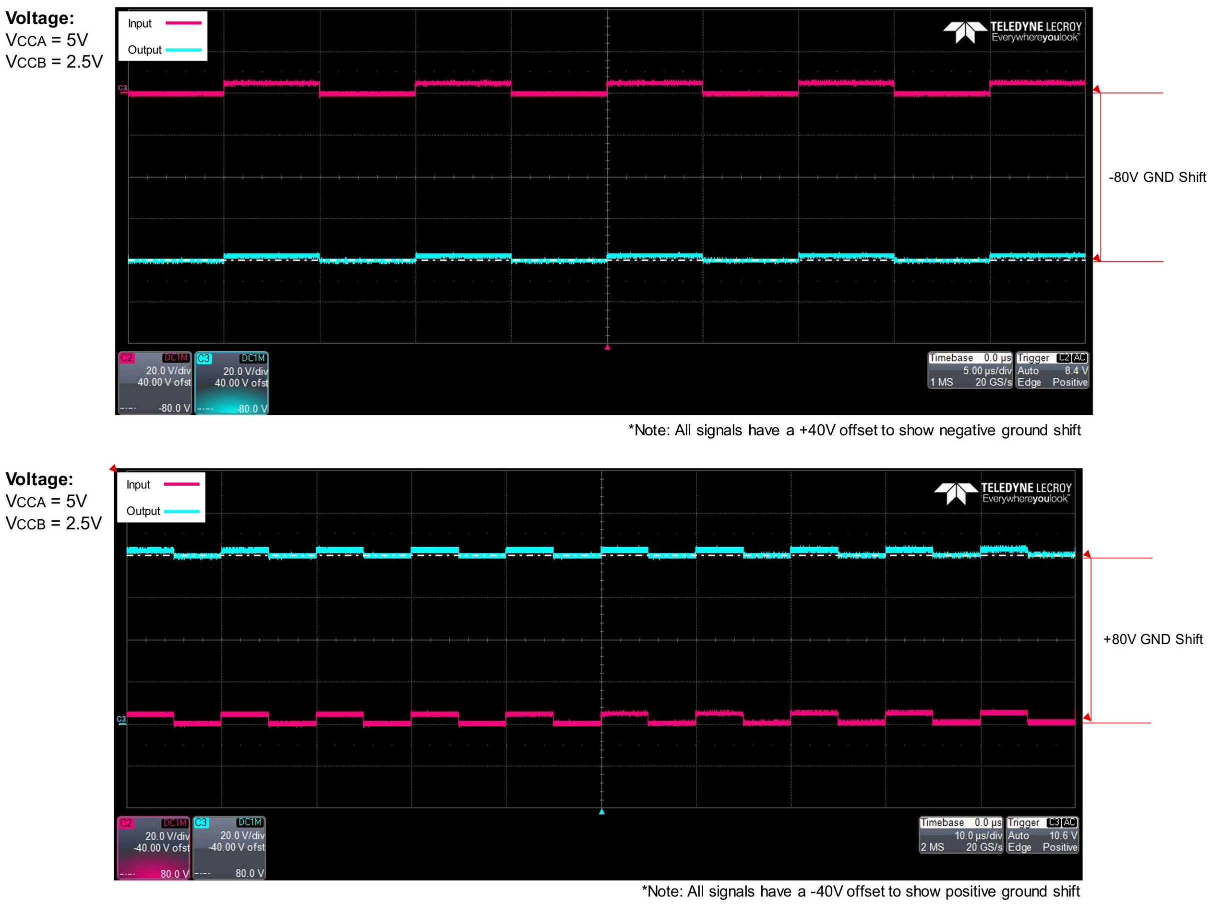


**Figure 8-2. Waveform showing -80V (top) and +80V (bottom) Ground Shift with 5V to 2.5V I/O Translation**

## 8.3 Power Supply Recommendations

Always apply a ground reference to the GND pins first. This device is designed for glitch free power sequencing without any supply sequencing requirements such as ramp order or ramp rate. Please make sure the difference between $V_{CC}$ and GND remains at 6.5V max at all times.

## 8.4 Layout

### *8.4.1 Layout Guidelines*

To ensure reliability of the device, following common printed-circuit board layout guidelines are recommended:

- Use bypass capacitors on the power supply pins and place them as close to the device as possible. A 0.1μF capacitor is recommended, but transient performance can be improved by having 1μF and 0.1μF capacitors in parallel as bypass capacitors.
- The high drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing.
- A 0.1μF capacitor can be added between GNDA and GNDB to improve performances of CMTI.

### *8.4.2 Layout Example*

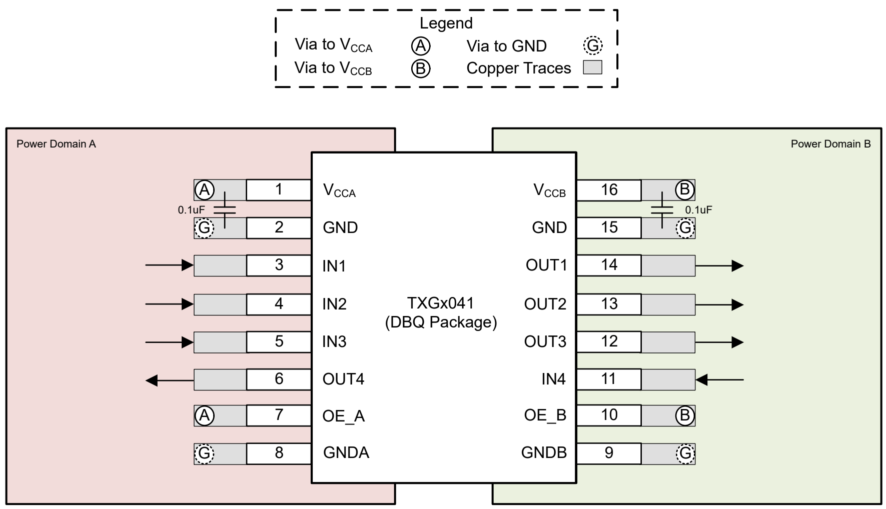


**Figure 8-3. DBQ Layout Example**

# 9 Device and Documentation Support

## 9.1 Device Support

### *9.1.1 Regulatory Requirements*

No statutory or regulatory requirements apply to this device.

There are no special characteristics for this product.

## 9.2 Documentation Support

### *9.2.1 Related Documentation*

For related documentation, see the following:

- Texas Instruments, *Understanding Schmitt Triggers* application report
- Texas Instruments, *CMOS Power Consumption and $C_{pd}$ Calculation* application report

## 9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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## 9.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

# 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE | REVISION | NOTES |
| --- | --- | --- |
| May 2025 | * | Initial APL Release |

# 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| PTXG8041DYYR | Active | Preproduction | SOT-23-THIN (DYY) \| 14 | 3000 \| LARGE T&R | - | Call TI | Call TI | -40 to 125 | |
| PTXG8042DYYR | Active | Preproduction | SOT-23-THIN (DYY) \| 14 | 3000 \| LARGE T&R | - | Call TI | Call TI | -40 to 125 | |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

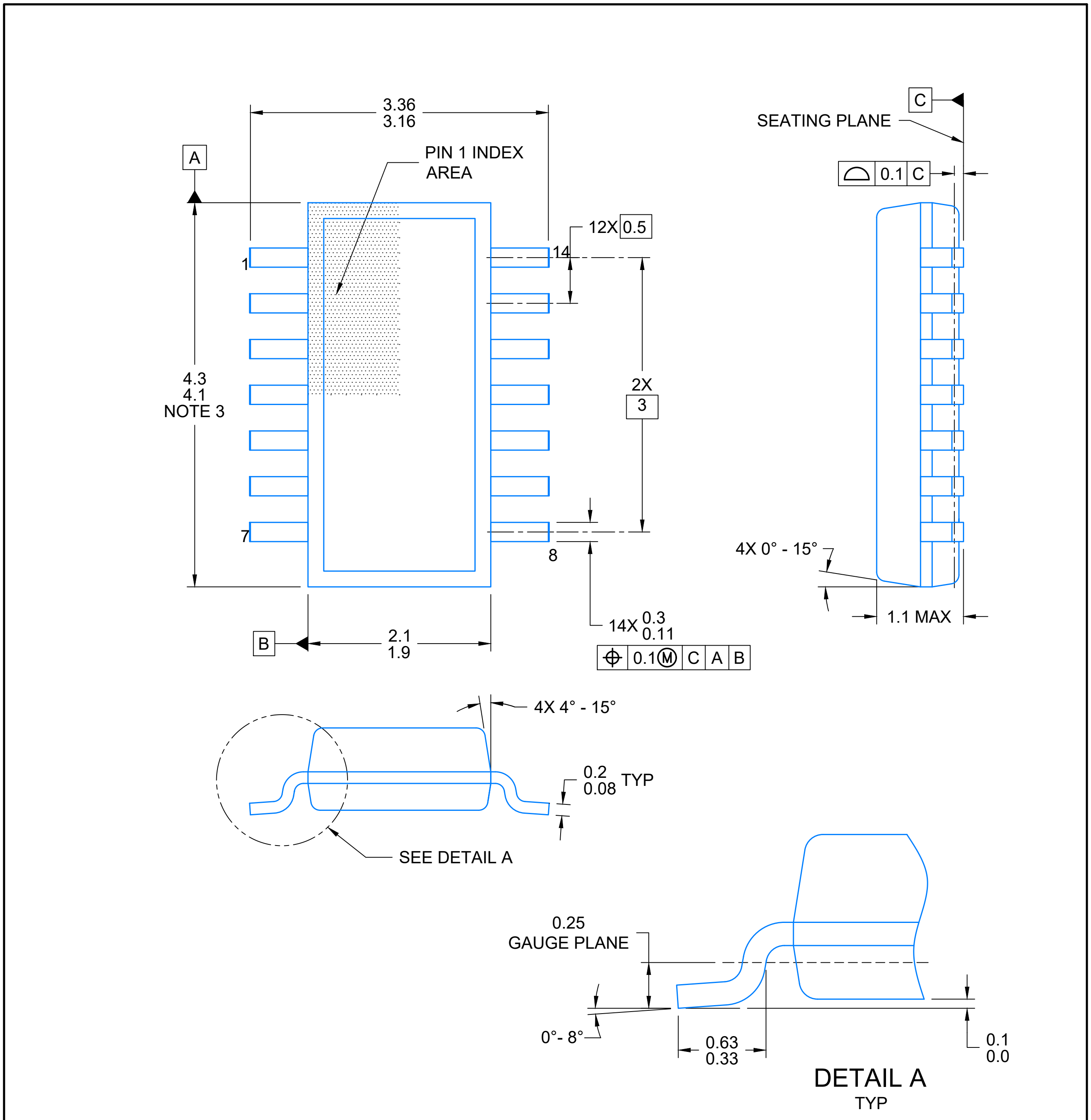
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TXG8041, TXG8042 :**

- Automotive : TXG8041-Q1, TXG8042-Q1
- Enhanced Product : TXG8041-EP

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

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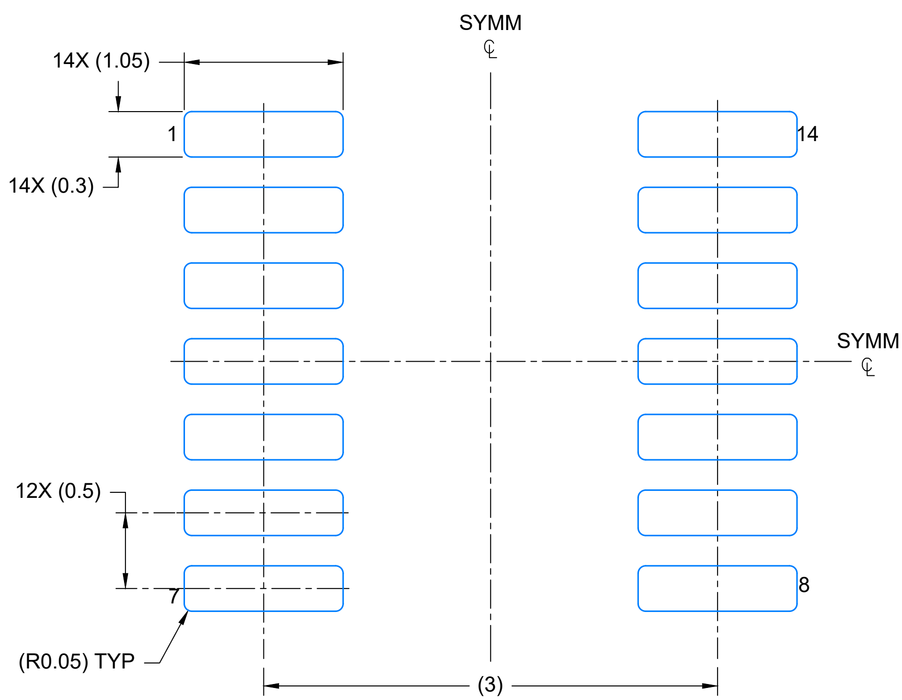
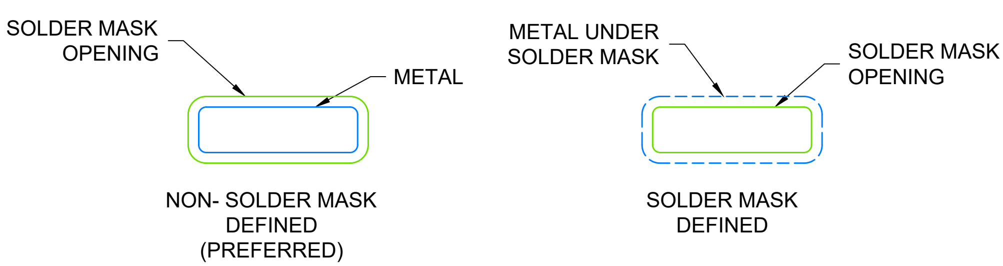
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

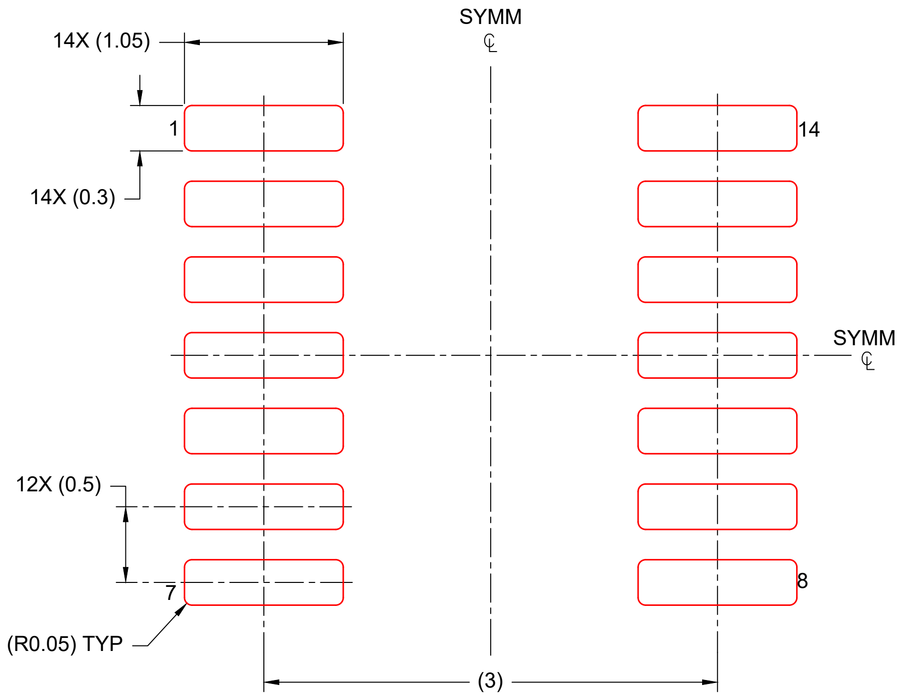



SOLDER MASK DETAILS

4224643/D 07/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224643/D 07/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.