µA741 General-Purpose Operational Amplifiers

1 Features

- Short-Circuit Protection
- Large Common-Mode and Differential Voltage Ranges
- No Frequency Compensation Required
- No Latch-Up

2 Applications

- DVD Recorders and Players
- Pro Audio Mixers

3 Description

The µA741 device is a general-purpose operational amplifier.

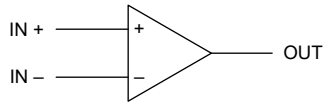
The high common-mode input voltage range and the absence of latch-up make the amplifier an excellent choice for voltage-follower applications. The device is short-circuit protected and the internal frequency compensation provides stability without external components.

The µA741C device is characterized for operation from 0°C to 70°C.

Package Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
µA741CD	SOIC (8)	4.90mm × 3.91mm
µA741CP	PDIP (8)	9.81mm × 6.35mm
µA741CPS	SO (8)	6.20mm × 5.30mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Functional Block Diagram

Table of Contents

4 Pin Configurations and Functions

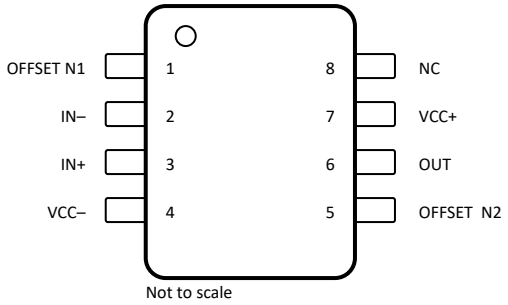


Figure 4-1. uA741C PS Package 8-Pin SO Top View

Table 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
IN+	3	I	Noninverting input
IN–	2	I	Inverting input
NC	8	—	No internal connection
OFFSET N1	1	I	External input offset voltage adjustment
OFFSET N2	5	I	External input offset voltage adjustment
OUT	6	O	Output
VCC+	7	—	Positive supply
VCC–	4	—	Negative supply

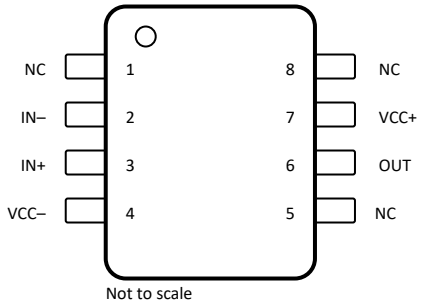


Figure 4-2. uA741C D or P Package 8-Pin SOIC, PDIP Top View

Table 4-2. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
IN+	3	I	Noninverting input
IN–	2	I	Inverting input
NC	8	—	No internal connection
NC	1	—	No internal connection
NC	5	—	No internal connection
OUT	6	O	Output
VCC+	7	—	Positive supply
VCC–	4	—	Negative supply

5 Specifications

5.1 Absolute Maximum Ratings

over virtual junction temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Supply voltage, V_{CC} (2)	μA741C		–18	18	V
Differential input voltage, V_{ID} (3)	μA741C		–15	15	V
Input voltage, V_I (any input) (2) (4)	μA741C		–15	15	V
Duration of output short circuit(5)			Unlimited		
Continuous total power dissipation			See *Section 5.3*		
Case temperature for 60 seconds		μA741C	N/A	N/A	°C
Lead temperature 1.6mm (1/16inch) from case for 60 seconds		μA741C	N/A	N/A	°C
Lead temperature 1.6mm (1/16inch) from case for 10 seconds	D, P, or PS package	μA741C		260	°C
Operating junction temperature, T_J				150	°C
Storage temperature range, T_{stg}		μA741C	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and $V_{CC–}$.
(3) Differential voltages are at IN+ with respect to IN –.
(4) The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15V, whichever is less.
(5) The output may be shorted to ground or either power supply.

5.2 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC+}	Supply Voltage		5	15	V
$V_{CC–}$			–5	–15	
T_A	Operating free-air temperature	μA741C	0	70	°C

5.3 Thermal Information

THERMAL METRIC(1)		μA741			UNIT
		D (SOIC)	P (PDIP)	PS (SO)	
		8 PINS	8 PINS	8 PINS	
$R_{θJA}$	Junction-to-ambient thermal resistance	138.7	87.4	119.7	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	78.7	89.3	66	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	82.2	64.4	70	°C/W
$ψ_{JT}$	Junction-to-top characterization parameter	27.8	49.8	27.2	°C/W
$ψ_{JB}$	Junction-to-board characterization parameter	81.4	64.1	69	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.4 Electrical Characteristics: µA741C

at specified virtual junction temperature, $V_{CC\pm}$ = ±15V (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 0	25°C		0.3	6	mV
			Full range			7.5	
I_{IO}	Input offset current	V_O = 0	25°C		0.005	200	nA
			Full range			300	
I_{IB}	Input bias current	V_O = 0	25°C		0.01	500	nA
			Full range			800	
V_{ICR}	Common-mode input voltage range	25°C		±12	±13		V
		Full range		±12			
V_{OM}	Maximum peak output voltage swing	R_L = 10kΩ	25°C	±12	±14.95		V
		R_L ≥ 10kΩ	Full range	±12			
		R_L = 2kΩ	25°C	±10			
		R_L ≥ 2kΩ	Full range	±10			
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 2kΩ	25°C	20	200		V/mV
		V_O = ±10V	Full range	15			
r_i	Input resistance	25°C			540		GΩ
r_o	Output resistance	f = 1MHz, I_O = 0A	25°C		575		Ω
C_i	Input capacitance	25°C			3		pF
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICRmin}	25°C	70	90		dB
			Full range	70			
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	V_{CC} = ±9 V to ±15V	25°C		30	150	µV/V
			Full range			150	
I_{OS}	Short-circuit output current	25°C			±80		mA
I_{CC}	Supply current	V_O = 0; no load	25°C		0.13	2.8	mA
			Full range			3.3	

(1) All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for the µA741C is 0°C to 70°C.

5.5 Electrical Characteristics: µA741Y

at specified virtual junction temperature, $V_{CC±}$ = ±15V, T_A = 25°C (unless otherwise noted

PARAMETER		TEST CONDITIONS (1)	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 0		0.3	5	mV
I_{IO}	Input offset current	V_O = 0		0.005	200	nA
I_{IB}	Input bias current	V_O = 0		0.01	500	nA
V_{ICR}	Common-mode input voltage range		±12	±13		V
V_{OM}	Maximum peak output voltage swing	R_L = 10kΩ	±12	±14.95		V
		R_L = 2kΩ	±10	±14.8		
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 2kΩ	20	200		V/mV
r_i	Input resistance			540		GΩ
r_o	Output resistance	f = 1MHz, I_O = 0A		575		Ω
C_i	Input capacitance			3		pF
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICRmin}	70	90		dB
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	V_{CC} = ±9 V to ±15 V		30	150	µV/V
I_{OS}	Short-circuit output current			±80		mA
I_{CC}	Supply current	V_O = 0; no load		0.13	2.8	mA

(1) All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified.

5.6 Switching Characteristics: µA741C

over operating free-air temperature range, $V_{CC±}$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time	V_I = 20 mV, R_L = 2 kΩ C_L = 100 pF		0.3		µs
	Overshoot factor			5%		
SR	Slew rate at unity gain	V_I = 10 V, R_L = 2 kΩ C_L = 100 pF		0.5		V/µs

5.7 Switching Characteristics: µA741Y

over operating free-air temperature range, $V_{CC±}$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time	V_I = 20 mV, R_L = 2 kΩ C_L = 100 pF		0.3		µs
	Overshoot factor			5%		
SR	Slew rate at unity gain	V_I = 10 V, R_L = 2 kΩ C_L = 100 pF		0.5		V/µs

5.8 Typical Characteristics

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

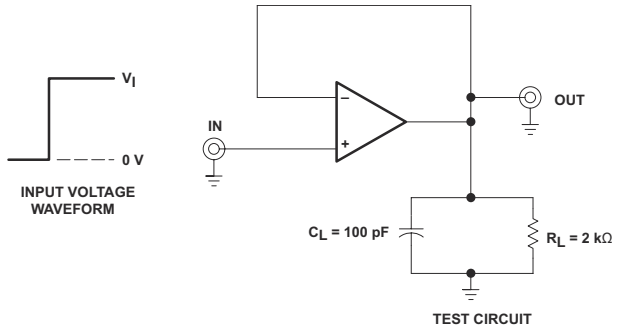


Figure 5-1. Rise Time, Overshoot, and Slew Rate

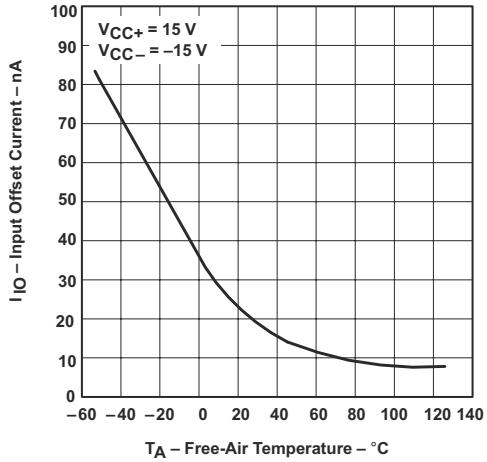


Figure 5-2. Input Offset Current vs Free-Air Temperature

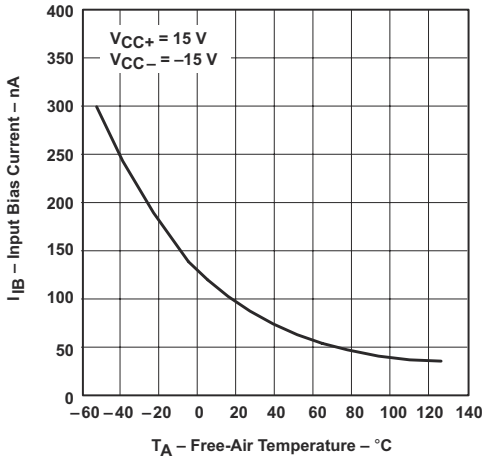


Figure 5-3. Input Bias Current vs Free-Air Temperature

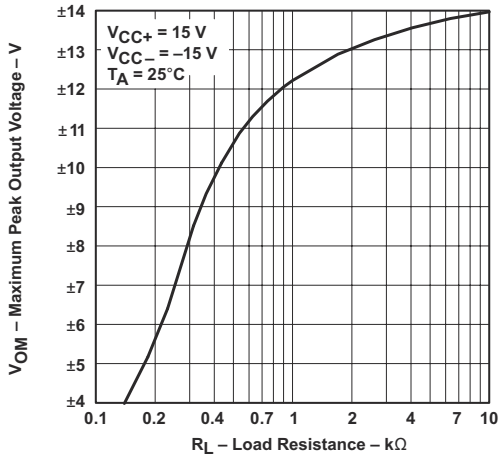


Figure 5-4. Maximum Output Voltage vs Load Resistance

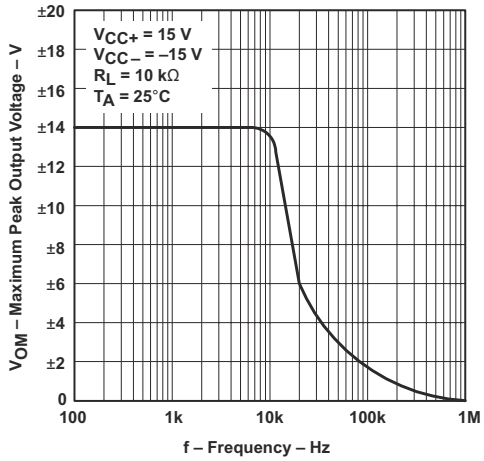


Figure 5-5. Maximum Peak Output Voltage vs Frequency

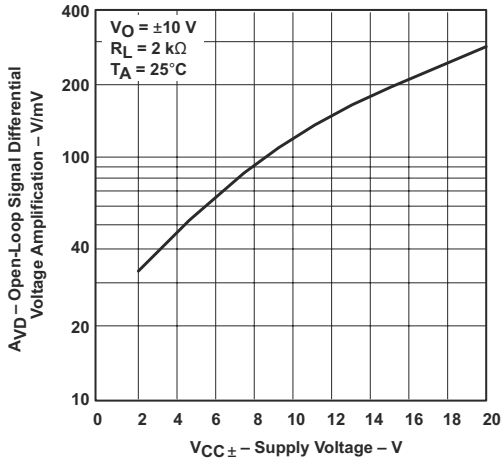


Figure 5-6. Open-Loop Signal Differential Voltage Amplification vs Supply Voltage

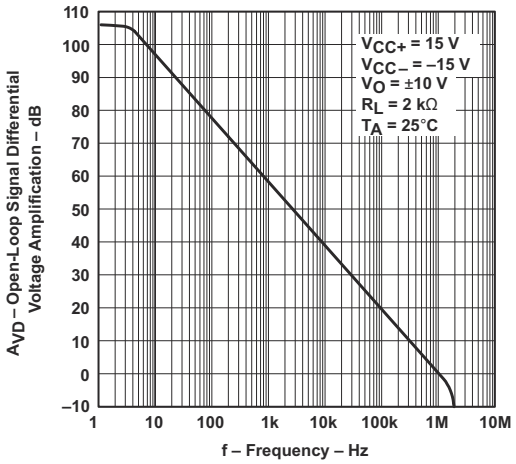


Figure 5-7. Open-Loop Large-Signal Differential Voltage Amplification vs Frequency

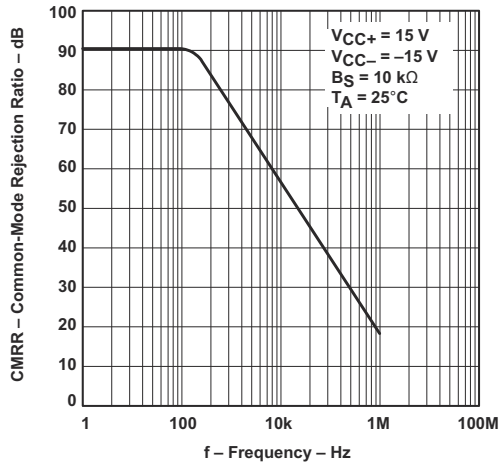


Figure 5-8. Common-Mode Rejection Ratio vs Frequency

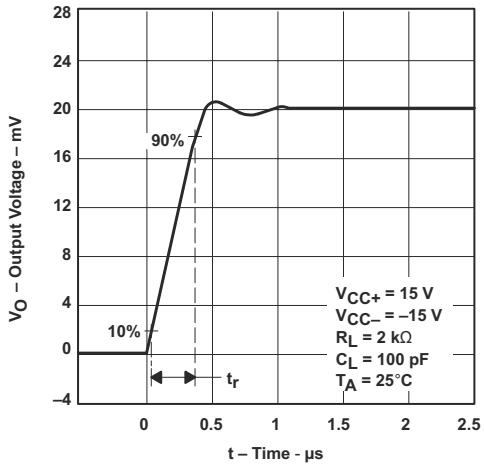


Figure 5-9. Output Voltage vs Elapsed Time

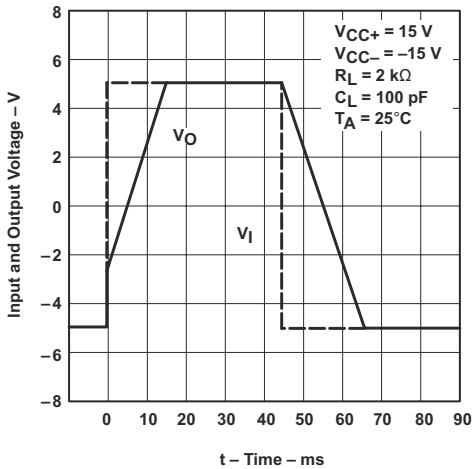


Figure 5-10. Voltage-Follower Large-Signal Pulse Response

6 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7 Power Supply Recommendations

The µA741 device is specified for operation from ±5 to ±15 V; many specifications apply from 0°C to 70°C. *Section 5.8* presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, see *Section 8.1* .

CAUTION

Supply voltages larger than ±18 V can permanently damage the device (see *Section 5.1*).

8 Layout

8.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier. Bypass capacitors reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close as possible to the device. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see *Circuit Board Layout Techniques*.
- To reduce parasitic coupling, run the input traces as far away as possible from the supply or output traces. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close as possible to the device. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in *Section 8.2* .
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

8.2 Layout Example

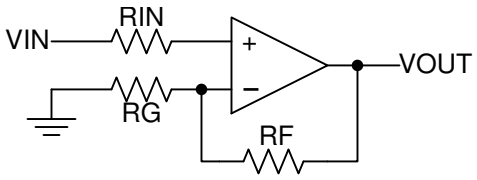


Figure 8-1. Operational Amplifier Schematic for Noninverting Configuration

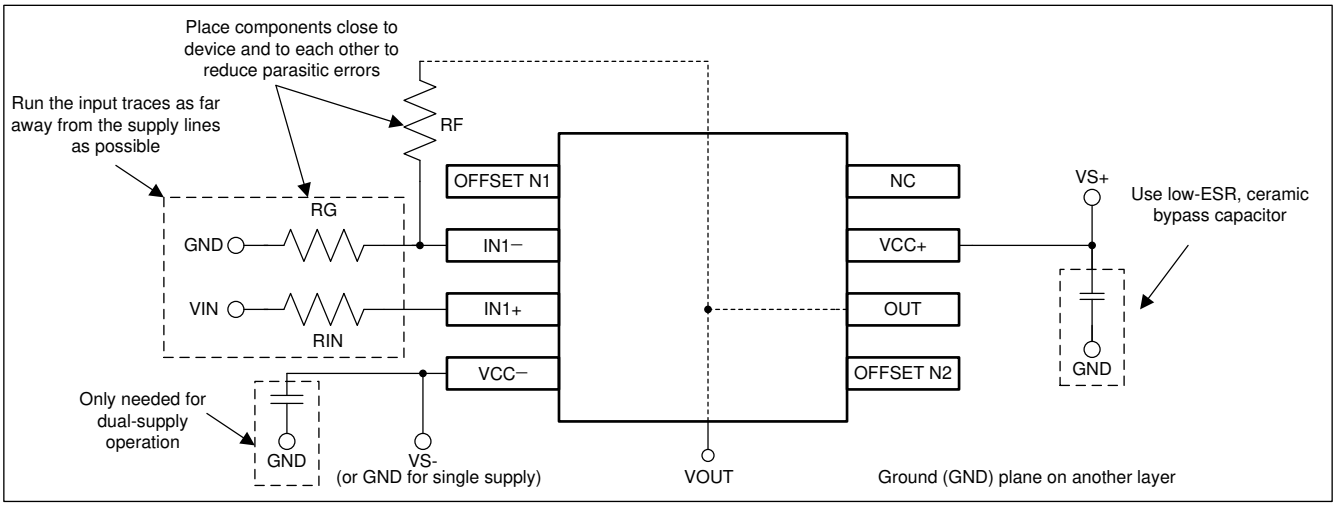


Figure 8-2. Operational Amplifier Board Layout for Noninverting Configuration

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Trademarks

All trademarks are the property of their respective owners.

9.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.4 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (January 2018) to Revision H (January 2026) **Page**

- Deleted Offset-Voltage Null Capability....1
- Deleted offset-voltage null capability 1
- Deleted Simplified schematic....1
- Updated Functional Block Diagram....1
- Changed Pin 1 and 5 of "uA741C D, P package" from "Offset N1 and Offset N2" to "No internal connection (NC)"....3
- Deleted Voltage between offset null (either OFFSET N1 or OFFSET N2) and V_{CC-} 4
- Changed Junction-to-ambient thermal resistance of D from 129.2°C/W to 138.7°C/W....4
- Changed Junction-to-case (top) thermal resistance of D from 73.6°C/W to 78.7°C/W....4
- Changed Junction-to-board thermal resistance of D from 72.4°C/W to 82.2°C/W....4
- Changed Junction-to-top characterization parameter of D from 25.9°C/W to 27.8°C/W....4
- Changed Junction-to-board characterization parameter of D from 71.7°C/W to 81.4°C/W....4
- Changed Input offset voltage in µA741C at 15V typ value from 1mV to 0.3mV....5
- Changed Input offset current in µA741C at 15V typ value from 20nA to 0.005nA....5
- Changed Input bias current in µA741C at 15V typ value from 80nA to 0.01nA....5
- Changed Maximum peak output voltage swing in µA741C at 15V typ value at R_L = 10kΩ from ±14V to ±14.95V....5
- Changed Input resistance in µA741C at 15V typ value from 2MΩ to 540GΩ....5
- Changed Output resistance in µA741C at 15V typ value from 75Ω to 575Ω....5
- Changed Input capacitance in µA741C at 15V typ value from 1.4pF to 3pF....5
- Changed Short-circuit output current in µA741C at 15V typ value from ±25mA to ±80mA....5
- Changed Supply current at 25°C in µA741C at 15V typ value from 1.7mA to 0.13mA....5
- Deleted Total power dissipation section in µA741C electrical characteristics....5
- Changed Input offset voltage in µA741Y at 15V typ value from 1mV to 0.3mV....6
- Deleted offset voltage adjust range....6
- Changed Input offset current in µA741Y at 15V typ value from 20nA to 0.005nA....6
- Changed Input bias current in µA741Y at 15V typ value from 80nA to 0.01nA....6
- Changed Maximum peak output voltage swing in µA741Y at 15V typ value at R_L = 10kΩ from ±14V to ±14.95V....6
- Changed Maximum peak output voltage swing in µA741Y at 15V typ value at R_L = 2kΩ from ±13V to ±14.8V....6
- Changed Input resistance in µA741Y at 15V typ value from 2MΩ to 540GΩ....6
- Changed Output resistance in µA741Y at 15V typ value from 75Ω to 575Ω....6
- Changed Input capacitance in µA741Y at 15V typ value from 1.4pF to 3pF....6
- Changed Short-circuit output current in µA741Y at 15V typ value from ±25mA to ±80mA....6
- Changed Supply current at 25°C in µA741Y at 15V typ value from 1.7mA to 0.13mA....6
- Deleted Total power dissipation section in µA741Y electrical characteristics....6

Changes from Revision F (May 2017) to Revision G (January 2018) **Page**

- Changed supply voltage unit from "°C" to "V" in *Absolute Maximum Ratings* table 4

Changes from Revision D (February 2014) to Revision E (January 2015) **Page**

- Added *Applications*, *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section....1

- Moved *Typical Characteristics* into *Specifications* section. 7

Changes from Revision E (January 2015) to Revision F (May 2017) **Page**

- Updated data sheet text to the latest documentation and translation standards 1
- Deleted text regarding µA741M device (obsolete package) from *Description* section..... 1
- Added µA741CD, µA741CP, and µA741CPS devices to *Device Information* table 1
- Deleted µA741x device from *Device Information* table 1
- Updated pinout diagrams and *Pin Functions* tables in the *Pin Configurations and Functions* section..... 3
- Deleted µA741M pinout drawings information from *Pin Configurations and Functions* section 3
- Added operating junction temperature (T_J) and values to *Absolute Maximum Ratings* table 4
- Deleted text regarding µA741M from *Absolute Maximum Ratings* table 4
- Deleted text regarding µA741M device from *Recommended Operating Conditions* table 4
- Deleted *Dissipation Ratings* table 4
- Added *Thermal Information* table and values 4
- Deleted µA741M in *Switching Characteristics* table 6
- Correct typo in Figure 5-1 7
- Changed pins 1 and 5 from "NC" to "Offset N1" and "Offset N2" in Figure 8-2 10

Changes from Revision C (January 2014) to Revision D (February 2014) **Page**

- Fixed *Typical Characteristics* graphs to remove extra lines. 7

Changes from Revision B (September 2000) to Revision C (January 2014) **Page**

- Updated document to new TI data sheet format - no specification changes..... 1
- Deleted *Ordering Information* table..... 1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UA741CD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	UA741C
UA741CDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UA741C
UA741CDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UA741C
UA741CP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UA741CP
UA741CP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UA741CP
UA741CPE4	Active	Production	PDIP (P) | 8	50 | TUBE	-	Call TI	Call TI	0 to 70	
UA741CPSR	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	U741
UA741CPSR.A	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	U741
UA741CPSRE4	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	U741

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

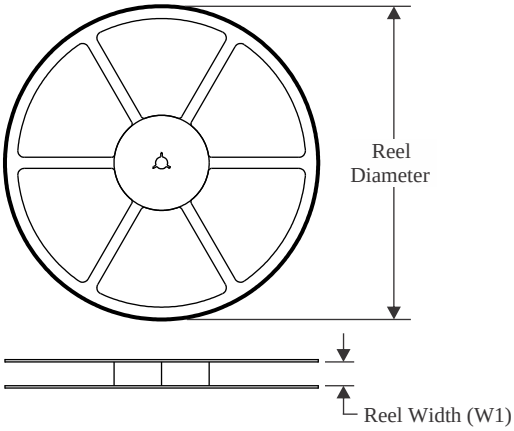
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

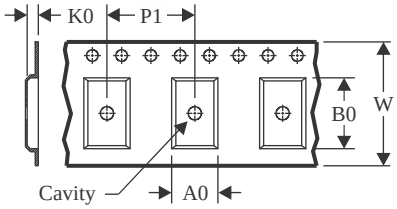
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

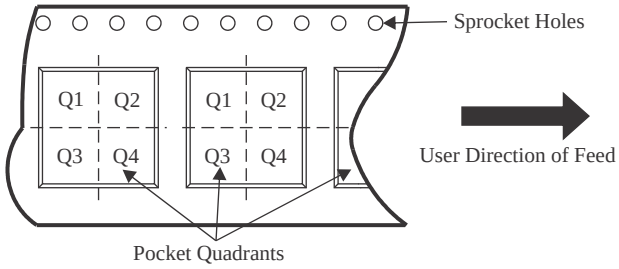


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

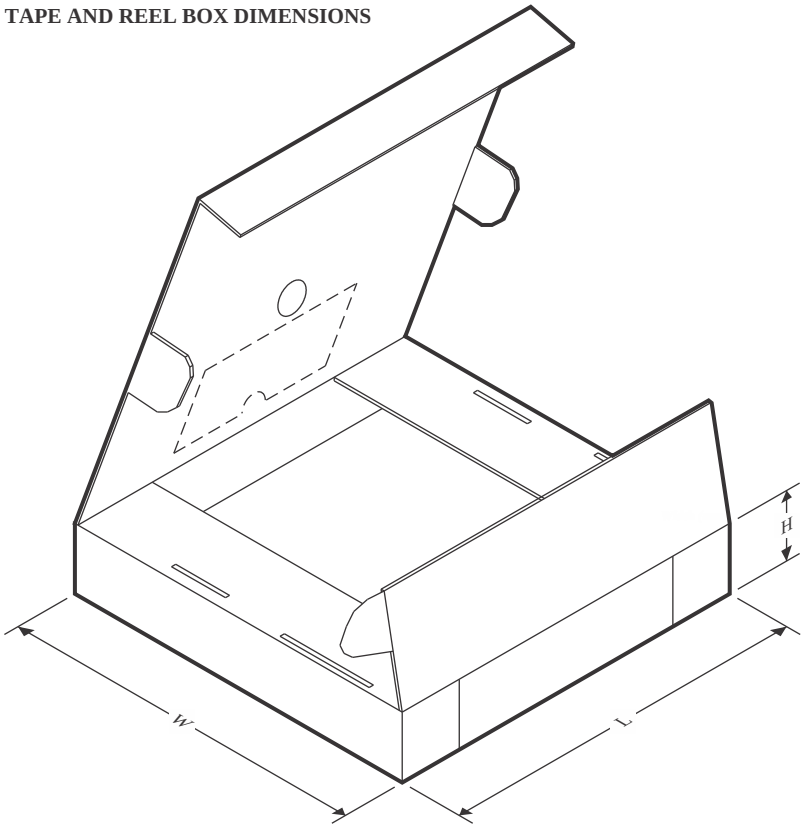
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UA741CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UA741CPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1

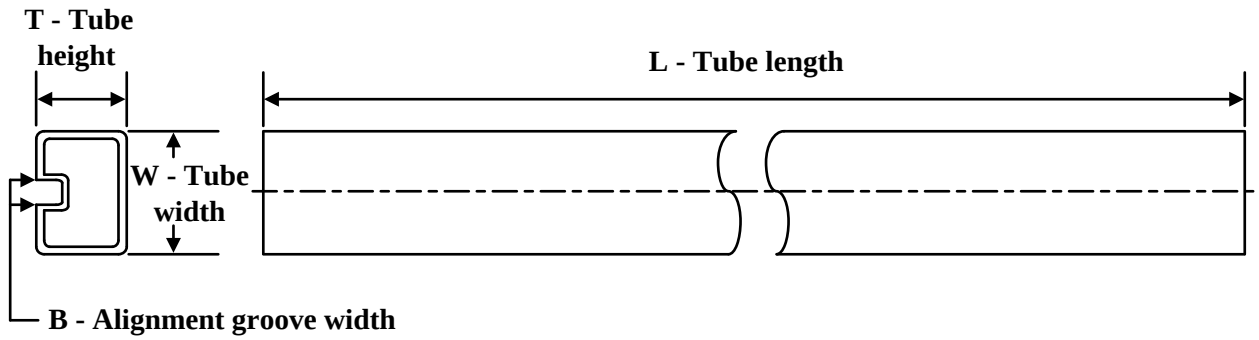
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UA741CDR	SOIC	D	8	2500	353.0	353.0	32.0
UA741CPSR	SO	PS	8	2000	353.0	353.0	32.0

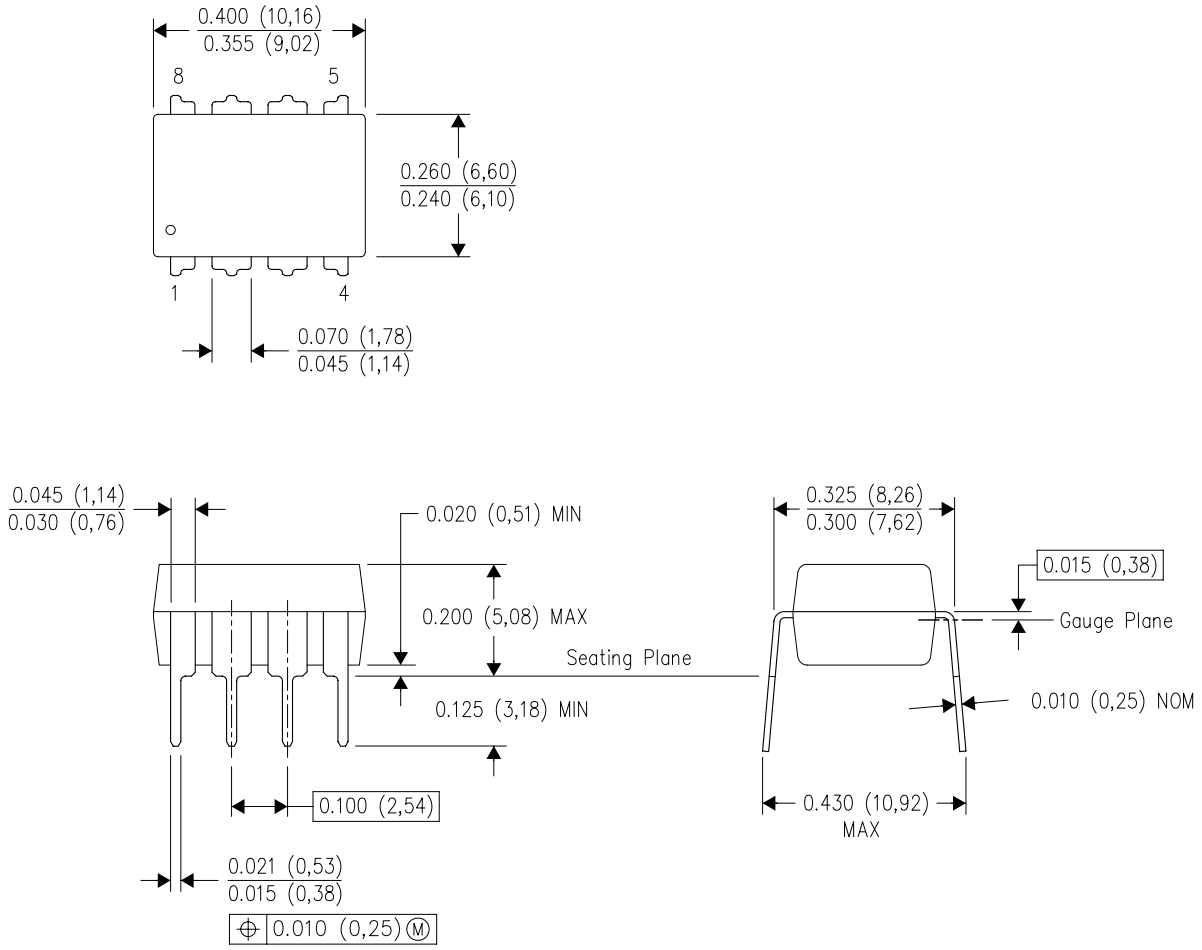
TUBE



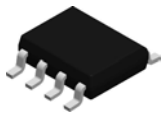
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UA741CP	P	PDIP	8	50	506	13.97	11230	4.32
UA741CP.A	P	PDIP	8	50	506	13.97	11230	4.32

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

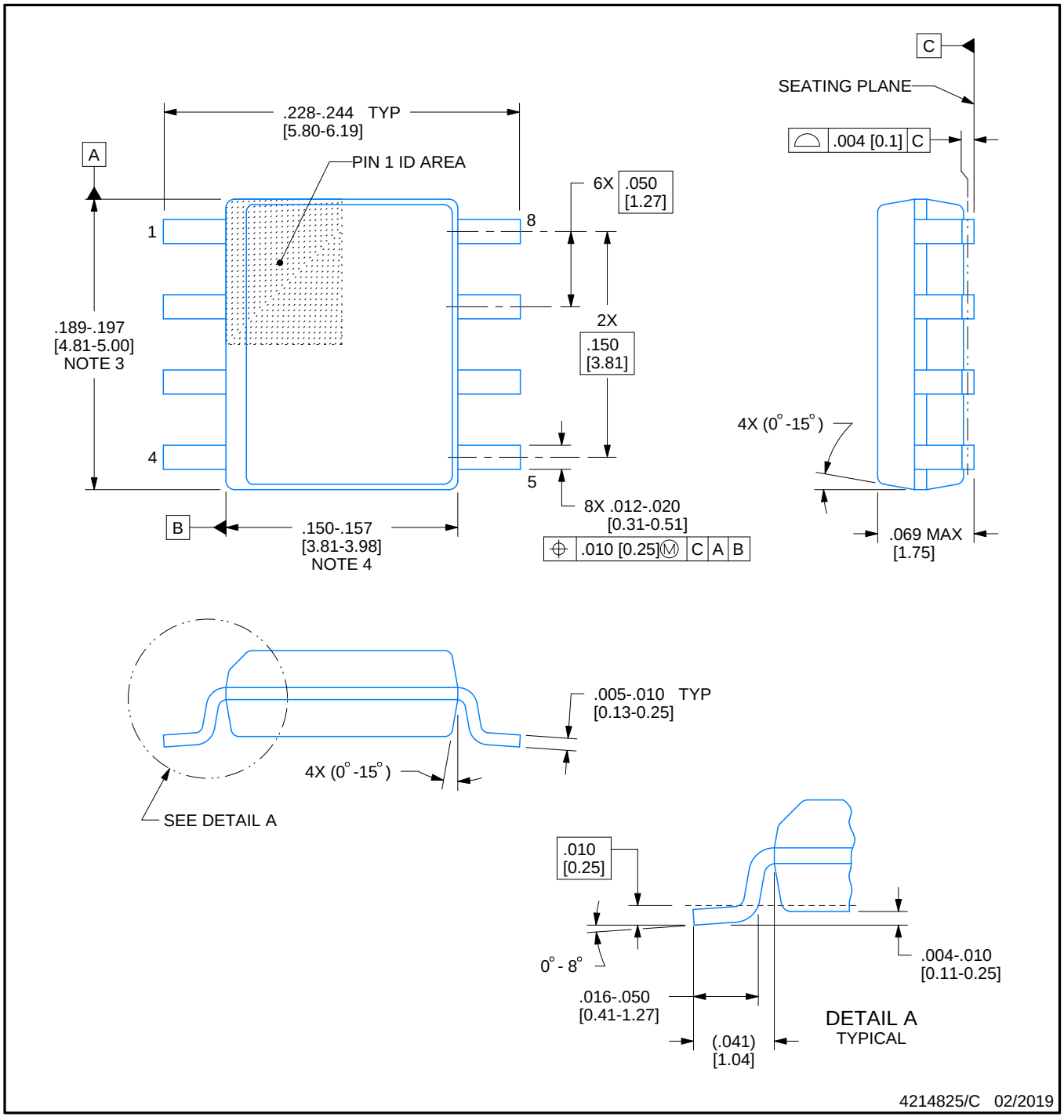


PACKAGE OUTLINE

D0008A

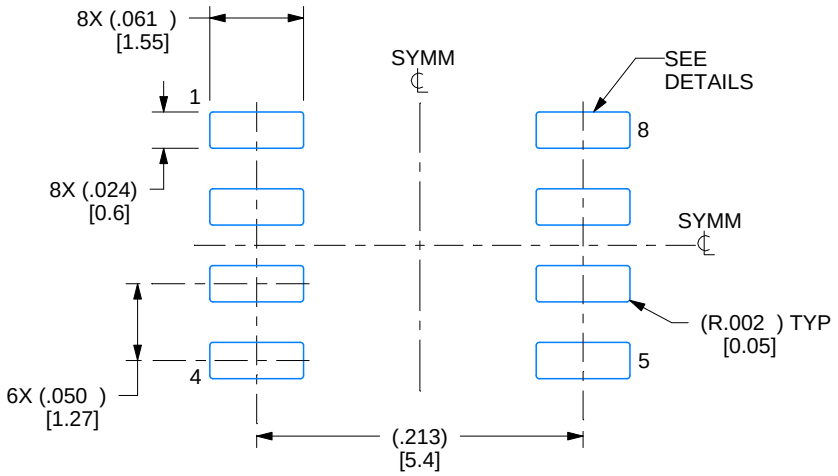
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

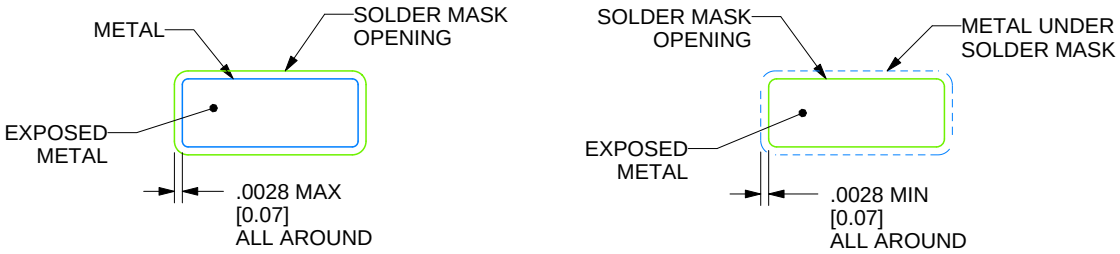


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

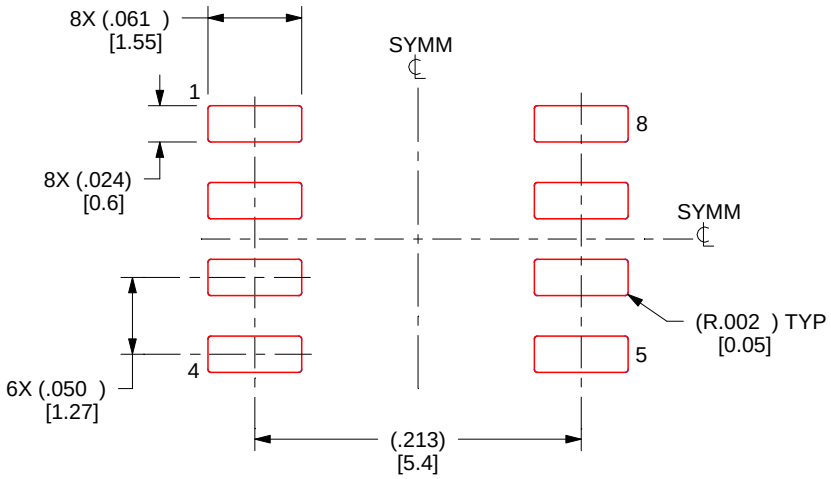
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

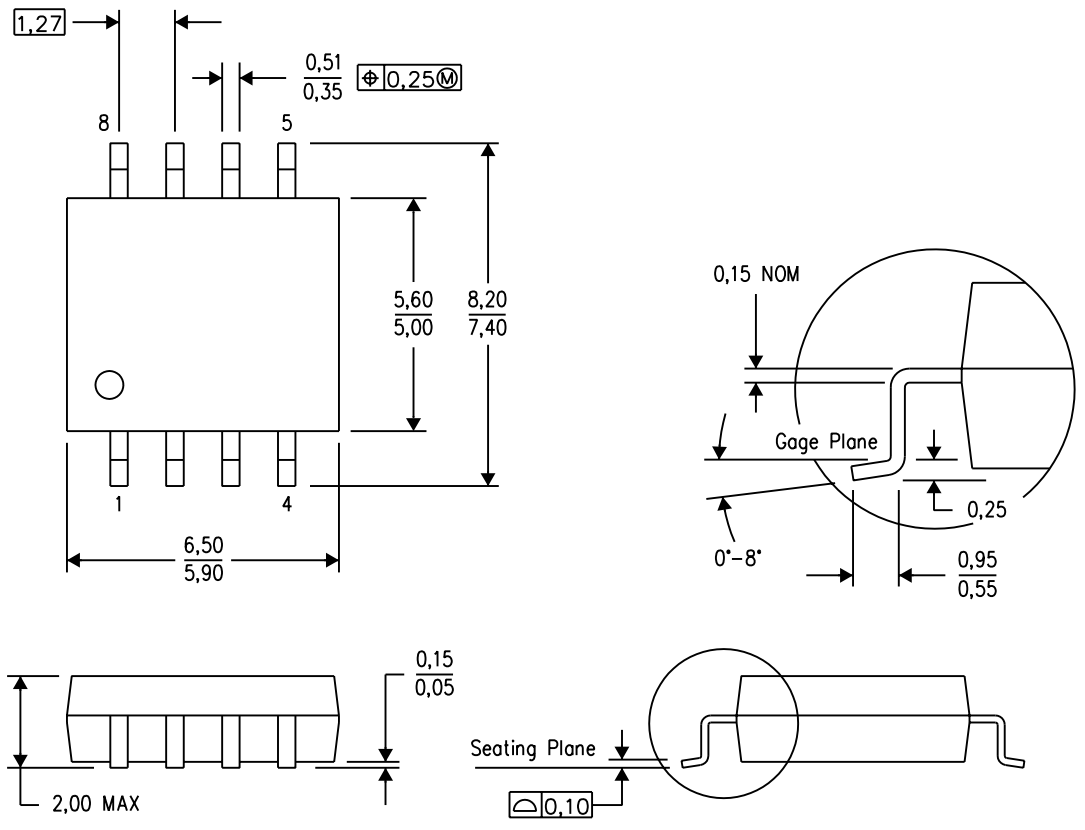
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

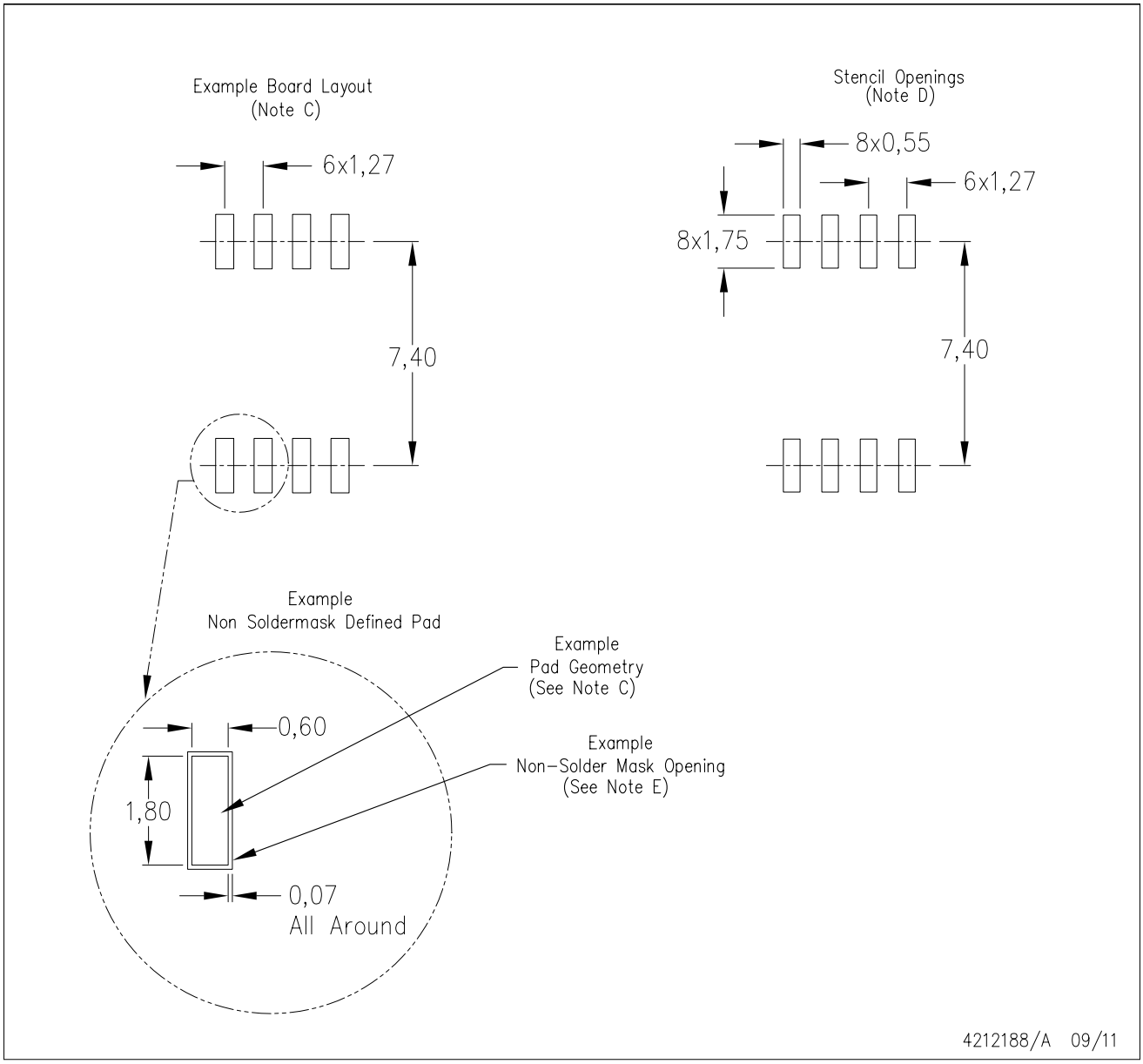
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025