UC1825A-SP Class-V, Radiation Hardened High-Speed PWM Controller

1 Features

- QML-V Qualified, SMD 5962-87681
- 5962**P**8768105Vxx:
  - Radiation Hardness Assurance (RHA) up to 30-krad(Si) Total Ionizing Dose (TID)
  - Passes Functional and Specified Post-Radiation Parametric Limits at 45 krad at LDR (10 mrad(Si)/s) per 1.5× Over Test as Defined in MIL-STD-883 Test Method 1019.9 Paragraph 3.13.3.b
  - Exhibits Low Dose Rate Sensitivity but Remains Within the Pre-Radiation Electrical Limits at 30-krad Total Dose Level, as Allowed by MIL-STD-883, TM1019
- Compatible With Voltage-Mode or Current-Mode Control Methods
- Practical Operation at Switching Frequencies to 1 MHz
- 50-ns Propagation Delay to Output
- High-Current Dual Totem Pole Outputs (2-A Peak)
- Trimmed Oscillator Discharge Current
- Low 100-μA Start-Up Current
- Pulse-by-Pulse Current Limiting Comparator
- Latched Overcurrent Comparator With Full Cycle Restart
- Qualified Over the Military Temperature Range (–55°C to 125°C)

2 Applications

- Radiation-Hardened DC-DC Converters
- Satellite Buses and Payloads
- Space Launch Vehicles
- Undersea Cabling
- Supports Various Topologies:
  - Flyback, Forward, Buck, Boost
  - Push-Pull, Half-Bridge, Full Bridge With External Interface Circuit

3 Description

The UC1825A-SP PWM controller is a radiation hardened version of the standard UC1825 family. Performance enhancements have been made to several of the circuit blocks. Error amplifier gain bandwidth product is 12 MHz, while input offset voltage is 2 mV. Current limit threshold is assured to a tolerance of 5%. Oscillator discharge current is specified at 10 mA for accurate dead time control. Frequency accuracy is improved to 6%. Start-up supply current, typically

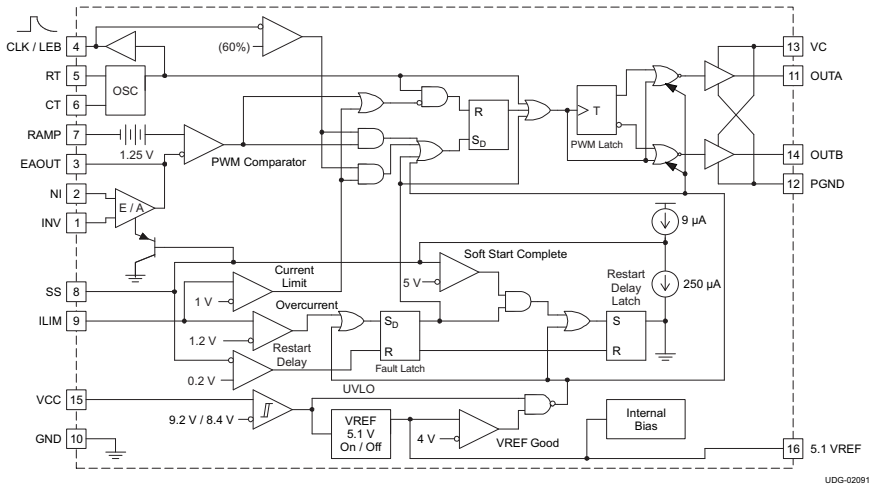
100 μA, is ideal for offline applications. The output drivers are redesigned to actively sink current during UVLO at no expense to the start-up current specification. In addition each output is capable of 2-A peak currents during transitions.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UC1825A-SP	CDIP (16)	19.56 mm × 6.92 mm
UC1825A-SP RHA	CDIP (16)	19.56 mm × 6.92 mm
	CFP (16)	10.16 mm × 7.10 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (October 2015) to Revision C — **Page**

- Added new RHA features ... 1
- Added new RHA packages to *Device Information* table ... 1
- Added new HKT pin diagram to *Pin Configuration and Functions* section ... 4
- Changed T_J MIN from –40°C : to –55°C ... 5
- Added *Receiving Notification of Documentation Updates* section to *Device and Documentation Support* section ... 34

Changes from Revision A (January 2009) to Revision B — **Page**

- Added *ESD Ratings* table, *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

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5 Description (continued)

Functional improvements have also been implemented in this device family. The UC1825 shutdown comparator is now a high-speed overcurrent comparator with a threshold of 1.2 V. The overcurrent comparator sets a latch that ensures full discharge of the soft-start capacitor before allowing a restart. While the fault latch is set, the outputs are in the low state. In the event of continuous faults, the soft-start capacitor is fully charged before discharge to insure that the fault frequency does not exceed the designed soft start period. The UC1825 CLOCK pin has become CLK/LEB. This pin combines the functions of clock output and leading edge blanking adjustment and has been buffered for easier interfacing.

The UC1825A-SP has dual alternating outputs and the same pin configuration of the UC1825. The UC1825A-SP version parts have UVLO thresholds identical to the original UC1825.

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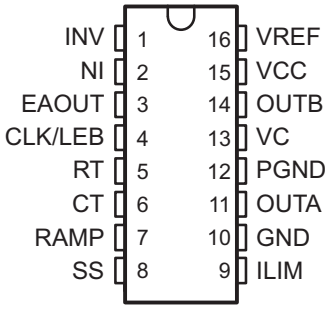
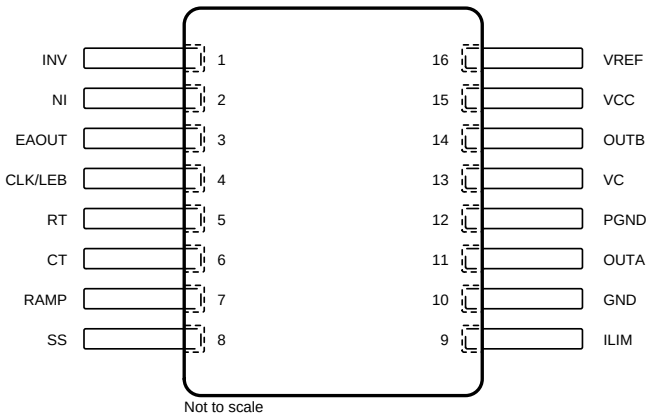
6 Pin Configuration and Functions

J Package
16-Pin CDIP
Top View



HKT Package
16-Pin CFP
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CLK/LEB	4	O	Output of the internal oscillator.
CT	6	I	Timing capacitor connection pin for oscillator frequency programming. The timing capacitor must be connected to the device ground using minimal trace length.
EAOUT	3	O	Output of the error amplifier for compensation.
GND	10	—	Analog ground return pin.
ILIM	9	I	Input to the current limit comparator.
INV	1	I	Inverting input to the error amplifier.
NI	2	I	Noninverting input to the error amplifier.
OUTA	11	O	High current totem pole output A of the on-chip drive stage.
OUTB	14	O	High current totem pole output B of the on-chip drive stage.
PGND	12	—	Ground return pin for the output driver stage.
RAMP	7	I	Noninverting input to the PWM comparator with 1.25-V internal input offset. In voltage mode operation, this serves as the input voltage feed-forward function by using the CT ramp. In peak current mode operation, this serves as the slope compensation input.
RT	5	I	Timing resistor connection pin for oscillator frequency programming.
SS	8	I	Soft-start input pin that also doubles as the maximum duty cycle clamp.
VC	13	—	Power supply pin for the output stage. This pin must be bypassed with a 0.1-μF monolithic ceramic low ESL capacitor with minimal trace lengths.
VCC	15	—	Power supply pin for the device. This pin must be bypassed with a 0.1-μF monolithic ceramic low ESL capacitor with minimal trace lengths.
VREF	16	O	5.1-V reference. For stability, the reference must be bypassed with a 0.1-μF monolithic ceramic low ESL capacitor and minimal trace length to the ground plane.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{IN}	Supply voltage	VC, VCC		22	V
I_O	Source or sink current, DC	OUTA, OUTB		0.5	A
I_O	Source or sink current, pulse (0.5 μs)	OUTA, OUTB		2.2	A
	Analog inputs	INV, NI, RAMP	–0.3	to 7	V
		ILIM, SS	–0.3	to 6	V
	Power ground	PGND		±0.2	V
	Outputs	OUTA, OUTB	P_{GND} – 0.3	to V_C + 0.3	V
I_{CLK}	Clock output current	CLK/LEB	–5		mA
$I_{O(EA)}$	Error amplifier output current	EAOUT		5	mA
I_{SS}	Soft-start sink current	SS		20	mA
I_{OSC}	Oscillator charging current	RT	–5		mA
T_J	Operating virtual junction temperature		–55	150	°C
	Lead temperature 1.6 mm (1/16 inch) from cases for 10 seconds			300	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (T_A = T_J = –55°C to 125°C), unless otherwise noted

		MIN	MAX	UNIT
V_{CC}	Supply voltage	12	20	V
	Sink/source output current (continuous or time average)	0	100	mA
	Reference load current	0	10	mA

7.4 Thermal Information

THERMAL METRIC(1)		UC1825A-SP J (CDIP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	55.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	N/A	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	33.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	35.89	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	8.024	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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7.5 Electrical Characteristics

T_A = –55°C to 125°C, R_T = 3.65 kΩ, C_T = 1 nF, V_{CC} = 12 V, T_A = T_J (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE, V_{REF}						
V_O	Ouput voltage	T_J = 25°C, I_O = 1 mA	5.05	5.1	5.15	V
	Line regulation	12 V ≤ VCC ≤ 20 V		2	15	mV
	Load regulation	1 mA ≤ I_O ≤ 10 mA		5	20	mV
	Total output variation	Line, load, temperature	5.03		5.17	V
	Temperature stability(1)	$T_{(min)}$ < T_A < $T_{(max)}$		0.2	0.4	mV/°C
	Output noise voltage	10 Hz < f < 10 kHz		50		μV_{RMS}
	Short circuit current	VREF = 0 V	30	60	90	mA
OSCILLATOR						
f_{OSC}	Initial accuracy(1)	T_J = 25°C	375	400	425	kHz
		R_T = 6.6 kΩ, C_T = 220 pF, T_A = 25°C	0.9	1	1.1	MHz
	Total variation(1)	Line, temperature	350		450	kHz
		R_T = 6.6 kΩ, C_T = 220 pF	0.82		1.18	MHz
	Voltage stability	12 V < VCC < 20 V			1%	
	Temperature stability	$T_{(min)}$ < T_A < $T_{(max)}$		±5%		
	High-level output voltage, clock		3.7	4		V
	Low-level output voltage, clock			0	0.2	V
	Ramp peak		2.6	2.8	3	V
	Ramp valley		0.7	1	1.25	V
	Ramp valley-to-peak		1.55	1.8	2	V
I_{OSC}	Oscillator discharge current	R_T = OPEN, V_{CT} = 2 V	8.5	10	11	mA
ERROR AMPLIFIER						
	Input offset voltage			2	10	mV
	Input bias current			0.6	3	µA
	Input offset current			0.1	1	µA
	Open loop gain	1 V < V_O < 4 V	60	95		dB
CMRR	Common mode rejection ratio	1.5 V < V_{CM} < 5.5 V	75	95		dB
PSRR	Power supply rejection ratio	12 V < V_{CC} < 20 V	85	110		dB
$I_{O(sink)}$	Output sink current	V_{EAOUT} = 1 V	1	2.5		mA
$I_{O(src)}$	Output source current	V_{EAOUT} = 4 V	–0.5	–1.3		mA
	High-level output voltage	I_{EAOUT} = –0.5 mA	4.5	4.7	5	V
	Low-level output voltage	I_{EAOUT} = –1 mA	0	0.5	1	V
	Gain bandwidth product(1)	f = 200 kHz	6	12		MHz
	Slew rate(1)		5	7		V/µs
PWM COMPARATOR						
I_{BIAS}	Bias current, RAMP	V_{RAMP} = 0 V		–1	–8	µA
	Minimum duty cycle				0%	
	Maximum duty cycle		85%			
t_{LEB}	Leading edge blanking time	R_{LEB} = 2 kΩ, C_{LEB} = 470 pF	300	375	450	ns
R_{LEB}	Leading edge blanking resistance	$V_{CLK/LEB}$ = 3 V	8.5	10	11.5	kΩ
V_{ZDC}	Zero DC threshold voltage, EAOUT	V_{RAMP} = 0 V	1.10	1.25	1.4	V
t_{DELAY}	Delay-to-output time(1)	V_{EAOUT} = 5-V to 0-V step		50	120	ns

(1) Parameters ensured by design and/or characterization, if not production tested.

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Electrical Characteristics (continued)

T_A = –55°C to 125°C, R_T = 3.65 kΩ, C_T = 1 nF, V_{CC} = 12 V, T_A = T_J (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT LIMIT, START SEQUENCE, FAULT						
I_{SS}	Soft-start charge current	V_{SS} = 2.5 V	8	14	20	µA
V_{SS}	Full soft-start threshold voltage		4.3	5		V
I_{DSCH}	Restart discharge current	V_{SS} = 2.5 V	100	250	350	µA
I_{SS}	Restart threshold voltage	0 V ≤ V_{ILIM} ≤ 1.5 V		0.3	0.5	V
I_{BIAS}	ILIM bias current				15	µA
I_{CL}	Current limit threshold voltage		0.95	1	1.05	V
	Overcurrent threshold voltage		1.14	1.2	1.26	V
t_d	Delay-to-output time, ILIM(1)	V_{ILIM} = 0-V to 2-V step		50	80	ns
OUTPUT						
	Low-level output saturation voltage	I_{OUT} = 20 mA		0.25	0.45	V
		I_{OUT} = 200 mA		1.2	2.2	
	High-level output saturation voltage	I_{OUT} = –20 mA		1.9	2.9	V
		I_{OUT} = –200 mA		2	3	
t_r, t_f	Rise/fall time(1)	C_L = 1 nF		20	45	ns
UNDERVOLTAGE LOCKOUT (UVLO)						
	Start threshold voltage		8.3	9.2	9.6	V
	UVLO hysteresis		0.4	0.8	1.25	V
SUPPLY CURRENT						
I_{su}	Start-up current	VC = VCC = 8 V		100	300	µA
I_{CC}	Input current			28	36	mA

7.6 Typical Characteristics

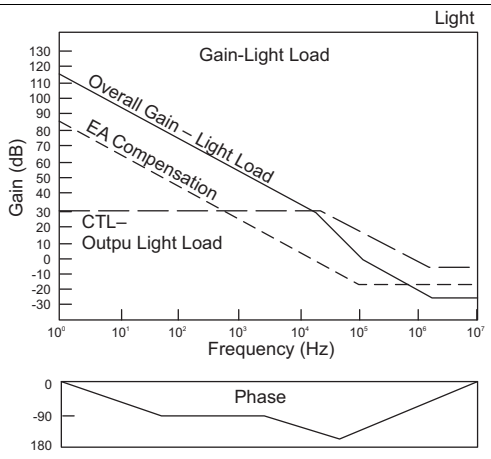


Figure 1. Gain: Light Load

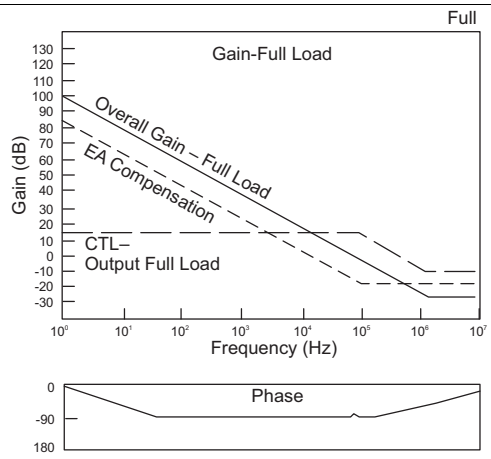


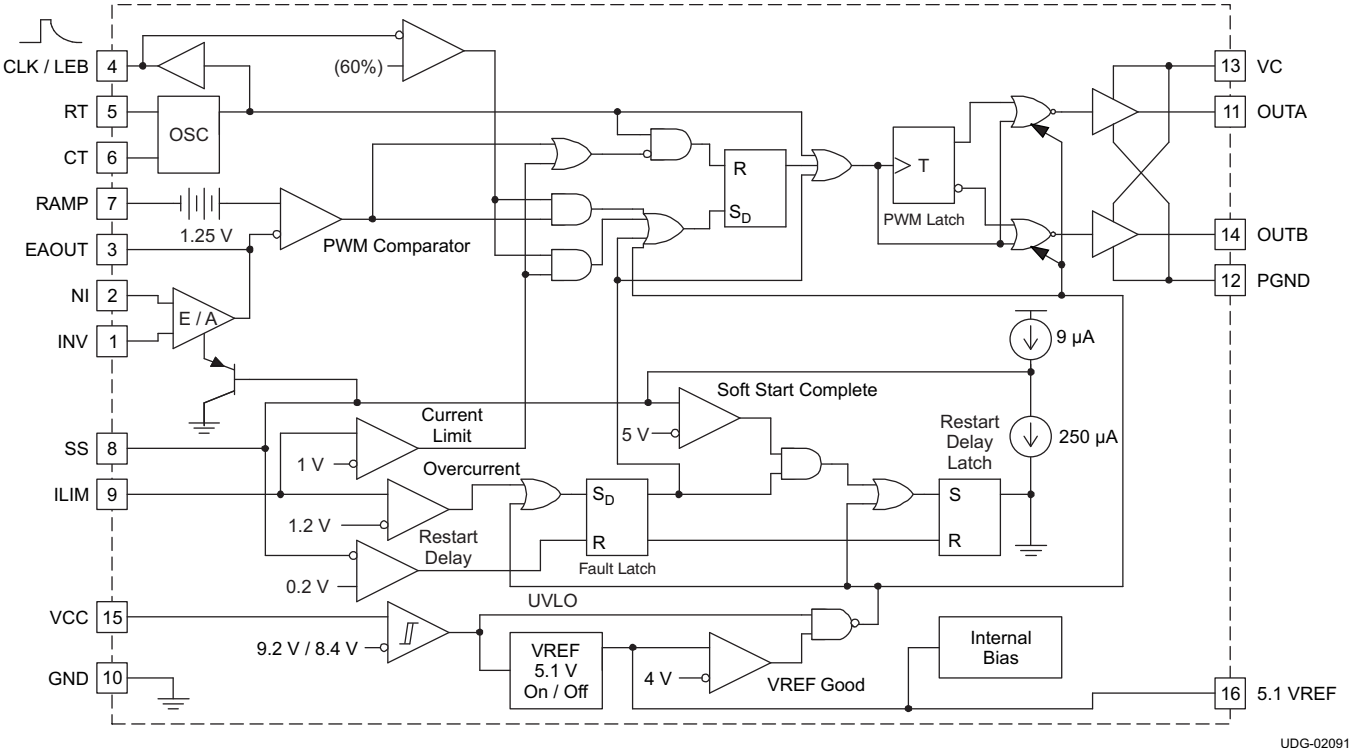
Figure 2. Gain: Full Load

8 Detailed Description

8.1 Overview

UC1825A-SP PWM controller is an improved version of the standard UC1825 family. Performance enhancements have been made to several of the circuit blocks. Error amplifier gain bandwidth product is 12 MHz, while input offset is 2 mV. Current limit threshold is assured to a tolerance of 5%. Oscillator discharge current is specified to 10 mA for accurate dead time control. Frequency accuracy is improved to 6%. Start-up supply current, typically 100 µA, is ideal for offline applications. The output drivers are redesigned to actively sink current during UVLO at no expense to the start-up current specifications. In addition, each output is capable of 2-A peak currents during transitions.

8.2 Functional Block Diagram



8.3 Feature Description

UC1825A-SP can be configured as current mode controller, used to support various topologies such as forward, flyback, Buck, Boost and using an external interface circuit will also support half-bridge, full bridge, and push-pull configurations.

8.3.1 Leading Edge Blanking

The UC1825A-SP performs fixed frequency pulse width modulation control. The UC1825A-SP outputs are alternately controlled. During every other cycle, one output is off. Each output then switches at one-half the oscillator frequency, varying in duty cycle from 0 to less than 50%.

To limit maximum duty cycle, the internal clock pulse blanks both outputs low during the discharge time of the oscillator. On the falling edge of the clock, the appropriate output is driven high. The end of the pulse is controlled by the PWM comparator, current limit comparator, or the overcurrent comparator.

Normally the PWM comparator senses a ramp crossing a control voltage (error amplifier output) and terminates the pulse. Leading edge blanking (LEB) causes the PWM comparator to be ignored for a fixed amount of time after the start of the pulse. This allows noise inherent with switched mode power conversion to be rejected. The PWM ramp input may not require any filtering as result of leading edge blanking.

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Feature Description (continued)

To program a leading edge blanking (LEB) period, connect a capacitor, C, to CLK/LEB. The discharge time set by C and the internal 10-kΩ resistor determines the blanked interval. The 10-kΩ resistor has a 10% tolerance. For more accuracy, an external 2-kΩ 1% resistor (R) can be added, resulting in an equivalent resistance of 1.66 kΩ with a tolerance of 2.4%. The design equation is shown in Equation 1:

$$t_{LEB} = 0.5 \times (R \parallel 10\ k\Omega) \times C \quad (1)$$

Values of R less than 2 kΩ must not be used.

Leading edge blanking is also applied to the current limit comparator (see Figure 3). After LEB, if the ILIM pin exceeds the 1-V threshold, the pulse is terminated. The overcurrent comparator, however, is not blanked. It catches catastrophic overcurrent faults without a blanking delay. Any time the ILIM pin exceeds 1.2 V, the fault latch is set and the outputs driven low. For this reason, some noise filtering may be required on the ILIM pin.

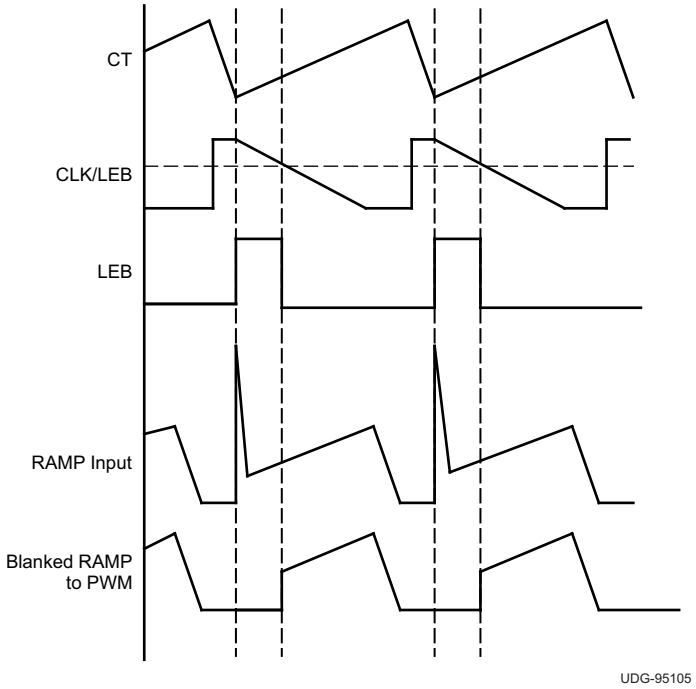

Figure 3. Leading Edge Blanking Operational Waveforms

8.3.2 UVLO, Soft-Start, and Fault Management

Soft-start is programmed by a capacitor on the SS pin. At power up, SS is discharged. When SS is low, the error amplifier output is also forced low. While the internal 9-μA source charges the SS pin, the error amplifier output follows until closed loop regulation takes over.

Anytime ILIM exceeds 1.2 V, the fault latch is set and the output pins are driven low, as shown in Figure 4. The soft-start cap is then discharged by a 250-μA current sink. No more output pulses are allowed until soft-start is fully discharged and ILIM is less than 1.2 V. At this point the fault latch resets and the chip executes a soft-start.

Should the fault latch get set during soft-start, the outputs are immediately terminated, but the soft-start capacitor does not discharge until it has been fully charged first. This results in a controlled hiccup interval for continuous fault conditions.

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Feature Description (continued)

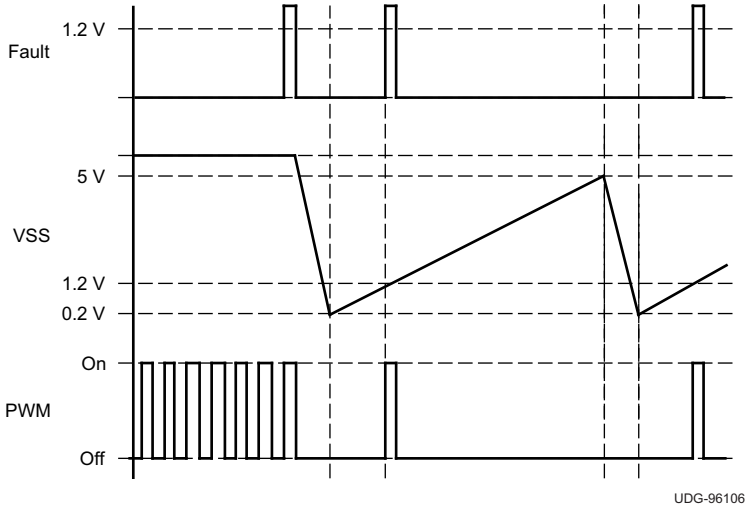

Figure 4. Soft-Start and Fault Waveforms

8.3.3 Active Low Outputs During UVLO

The UVLO function forces the outputs to be low and considers both VCC and VREF before allowing the chip to operate (see Figure 5 and Figure 6).

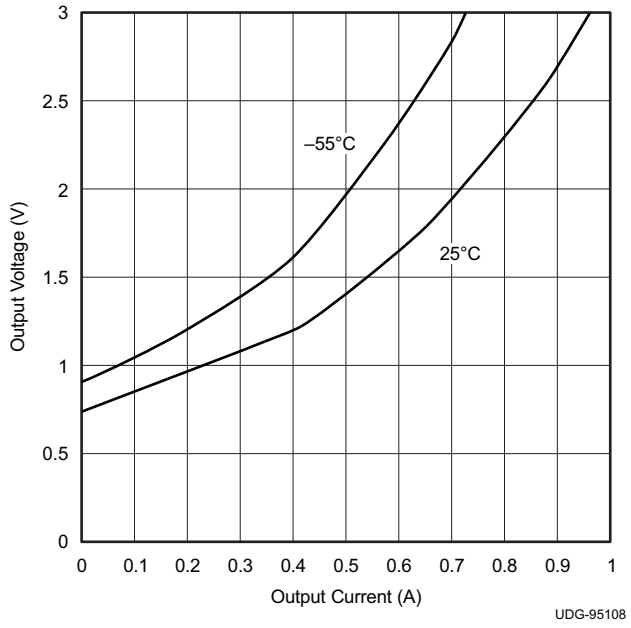

Figure 5. Output Voltage vs Output Current

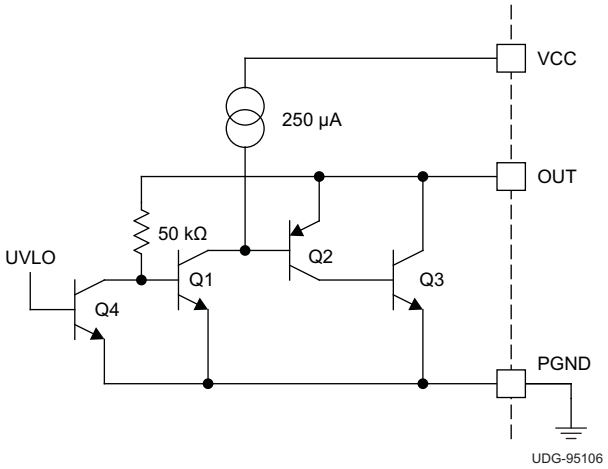

Figure 6. Output V And I During UVLO

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Feature Description (continued)

8.3.4 Control Methods

Figure 7 shows the control methods.

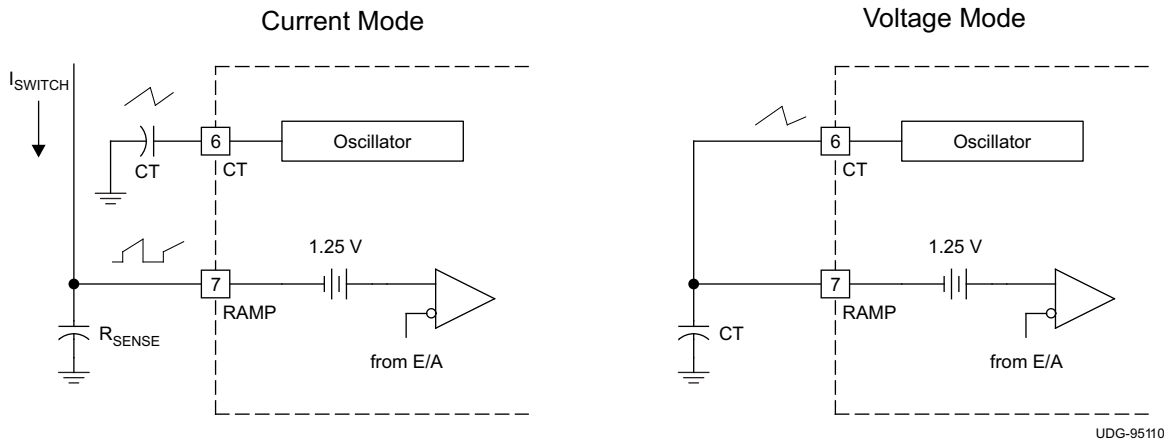

Figure 7. Control Methods

8.3.5 Synchronization

The oscillator can be synchronized by an external pulse inserted in series with the timing capacitor (see Figure 8). Program the free running frequency of the oscillator to be 10% to 15% slower than the desired synchronous frequency. The pulse width must be greater than 10 ns and less than half the discharge time of the oscillator. Figure 9 shows how to synchronize two ICs, with one as master and one as slave. Figure 10 shows the waveforms in a master and slave configuration.

NOTE

The CLK/LEB pin no longer accepts an incoming synchronizing signal.

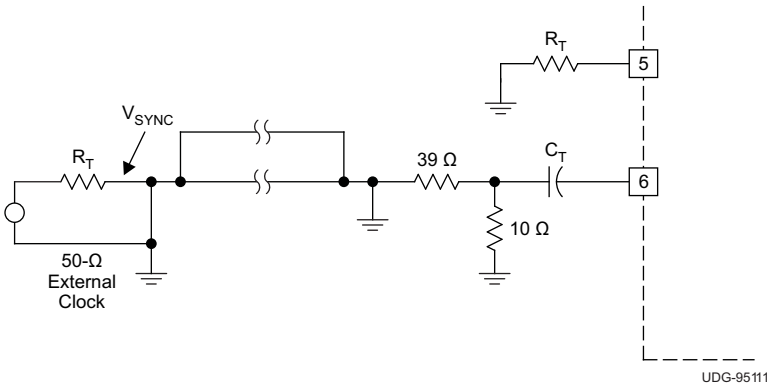

Figure 8. General Oscillator Synchronization

Feature Description (continued)

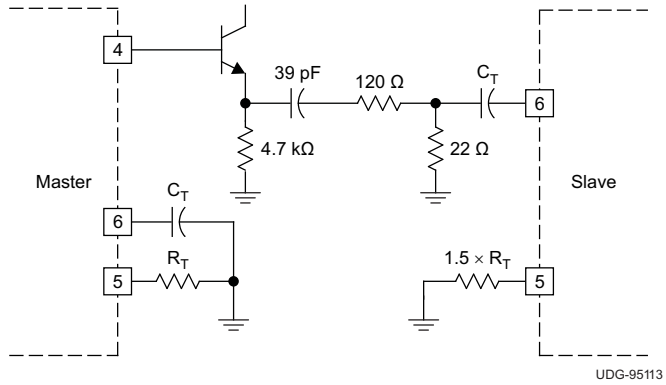

Figure 9. Two Unit Interface

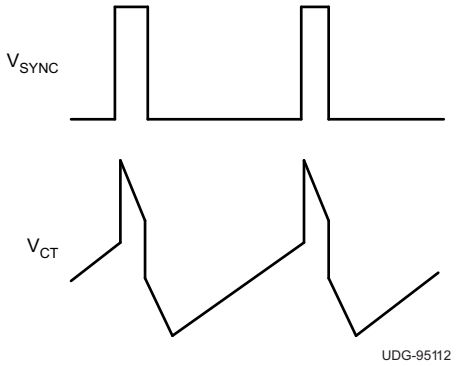

Figure 10. Operational Waveforms

8.3.6 High Current Outputs

Each totem pole output of the UC1825A-SP can deliver a 2-A peak current into a capacitive load. The output can slew a 1000-pF capacitor by 15 V in approximately 20 ns. Separate collector supply (VC) and power ground (PGND) pins help decouple the analog circuitry of the device from the high-power gate drive noise. The use of 3-A Schottky diodes (1N5120, USD245, or equivalent) as shown in the Figure 25 from each output to both VC and PGND are recommended. The diodes clamp the output swing to the supply rails, necessary with any type of inductive or capacitive load, typical of a MOSFET gate, as shown in Figure 11. Schottky diodes must be used because a low forward voltage drop is required.

NOTE

Do **not** use standard silicon diodes.

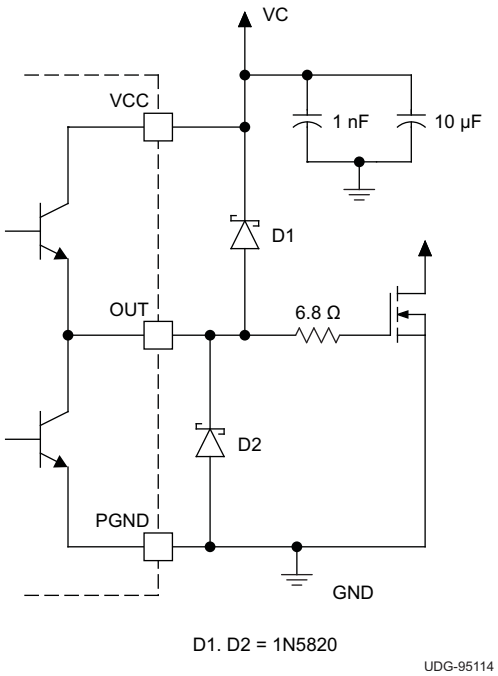

Figure 11. Power MOSFET Drive Circuit

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Feature Description (continued)

8.3.7 Open Loop Test Circuit

This test fixture is useful for exercising many functions of this device family and measuring their specifications (see Figure 12). As with any wideband circuit, careful grounding and bypass procedures must be followed. TI highly recommends using a ground plane.

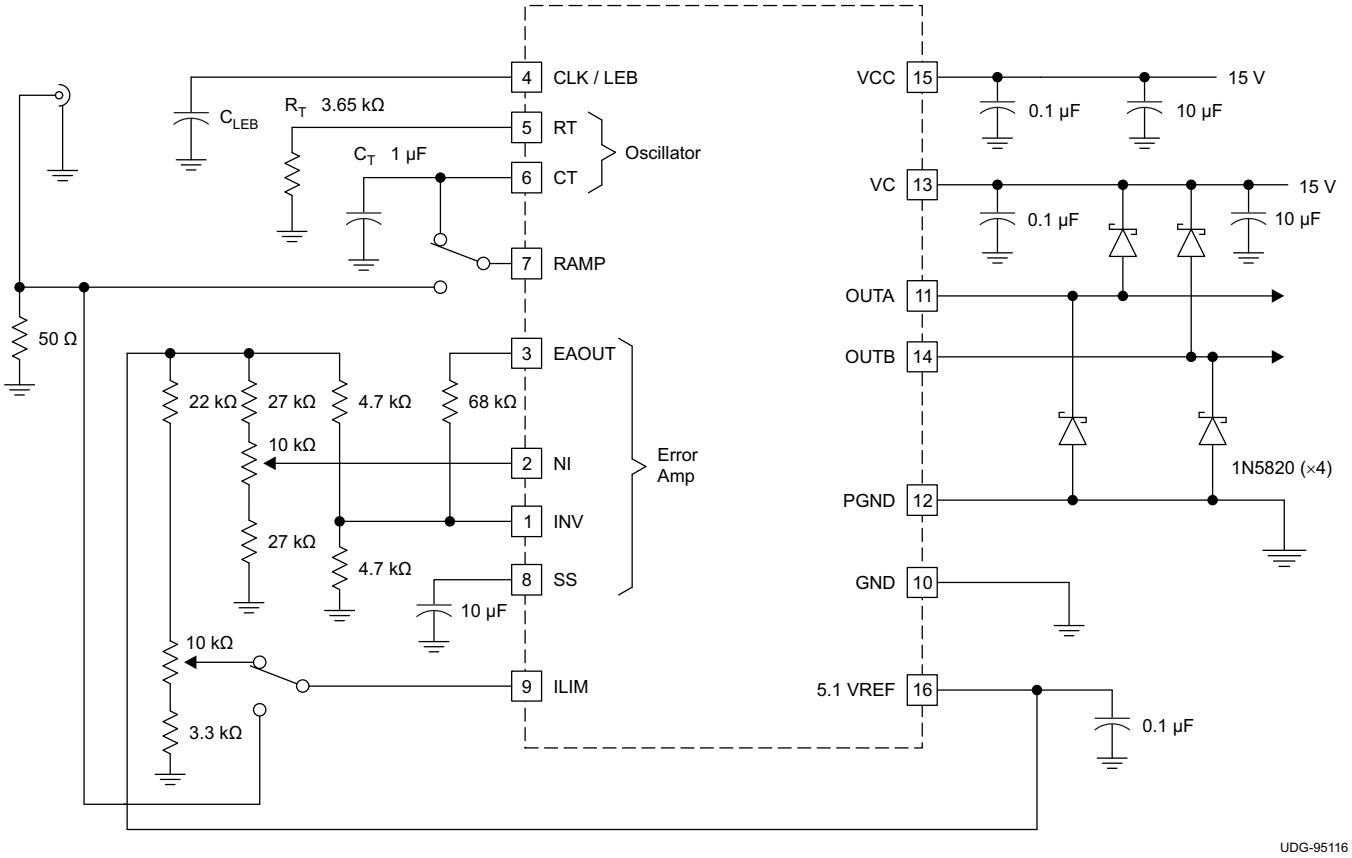

Figure 12. Open Loop Test Circuit Schematic

8.4 Device Functional Modes

The UC1825A-SP is compatible with voltage-mode or current-mode topologies. The UC1825A-SP uses fixed frequency, peak current mode control. An internal oscillator initiates the turnon of the driver to high-side power switch. The external power switch current is sensed through an external resistor and is compared through internal comparator. The voltage generated at the COMP pin is stepped down through internal resistors (as shown in *Functional Block Diagram*). When the sensed current reaches the stepped down COMP voltage, the high-side power switch is turned off.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The oscillator of the UC1825A-SP is a saw tooth (see Figure 13). The rising edge is governed by a current controlled by the RT pin and value of capacitance at the CT pin (C_{CT}). The falling edge of the sawtooth sets dead time for the outputs. Selection of RT must be done first, based on desired maximum duty cycle (see Figure 15). CT can then be chosen based on the desired frequency (RT) and D_{MAX} (see Figure 14). Equation 2 shows the design equations.

$$R_T = \frac{3\ V}{(10\ mA) \times \left(1 - D_{MAX}\right)} \qquad C_T = \frac{\left(1.6 \times D_{MAX}\right)}{\left(R_T \times f\right)} \tag{2}$$

Recommended values for R_T range from 1 kΩ to 100 kΩ. Control of D_{MAX} less than 70% is not recommended.

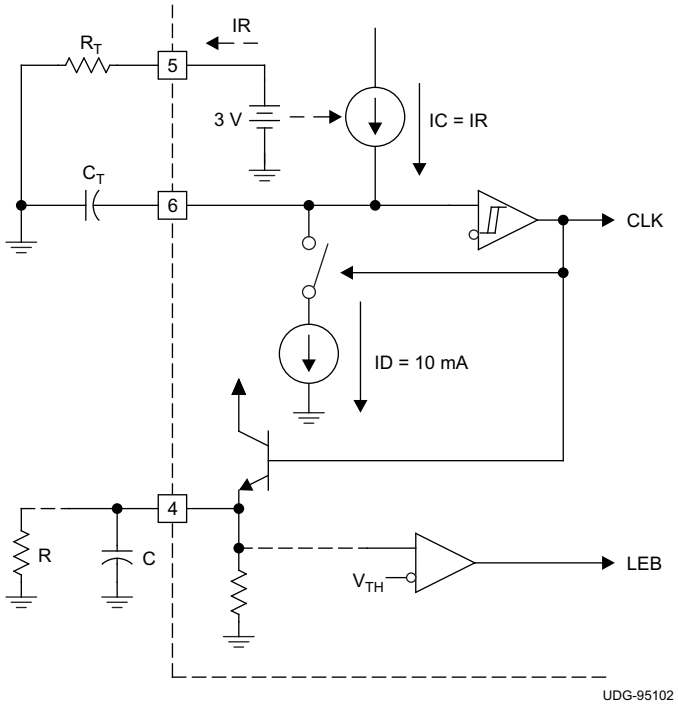

Figure 13. Oscillator

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Application Information (continued)

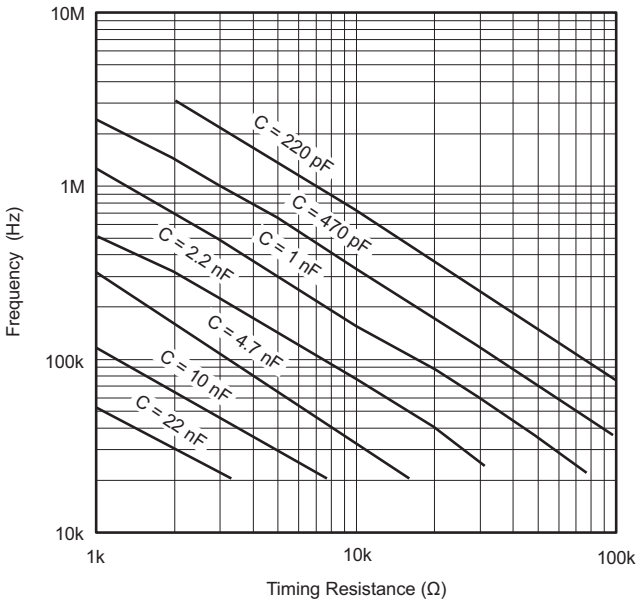

Figure 14. Oscillator Frequency vs Timing Resistance

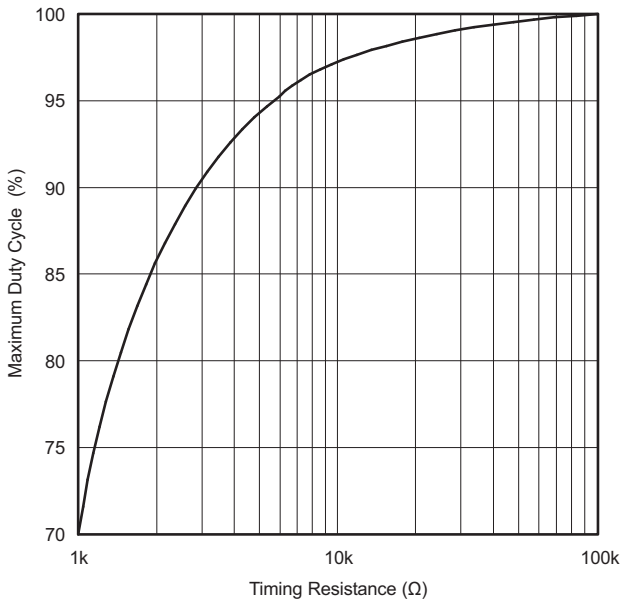

Figure 15. Maximum Duty Cycle vs Timing Resistance

9.2 Typical Application

Power can efficiently be converted using any of several standard topologies. Design tradeoffs of cost, size and performance will generally narrow the field to one that is most appropriate.

For this application, the center-tapped push-pull configuration has been selected. Current mode control provides numerous advantages over conventional duty cycle control, and has been implemented as the regulation method.

In review, the error amplifier output (outer control loop) defines the level at which the primary current (inner loop) will regulate the pulse width, and output voltage. Pulse-by-pulse symmetry correction (flux balancing) is inherent to current mode controllers, and essential for the push-pull topology to prevent core saturation. A basic current-mode-controlled, MOSFET-switched, push-pull converter is shown in Figure 16. Transistor Q1 is turned on by a drive pulse from the PWM, causing primary current Ip to flow through the transformer primary, mosfet Q1 and sense resistor Rs. Simultaneously, diode D1 conducts current Ip × Np / Ns in the secondary, storing energy in inductor L1 and delivering power to the output load. When Q1 receives a turnoff pulse from the PWM, it halts the current flow in the primary. Secondary current continues due to the filter inductor L1. Diodes D1 and D2 each conduct one-half the DC output current during these converter off times. This entire process is repeated on alternate cycles, as Q2 next is toggled on and off. The basic waveforms are shown in Figure 16 for reference.

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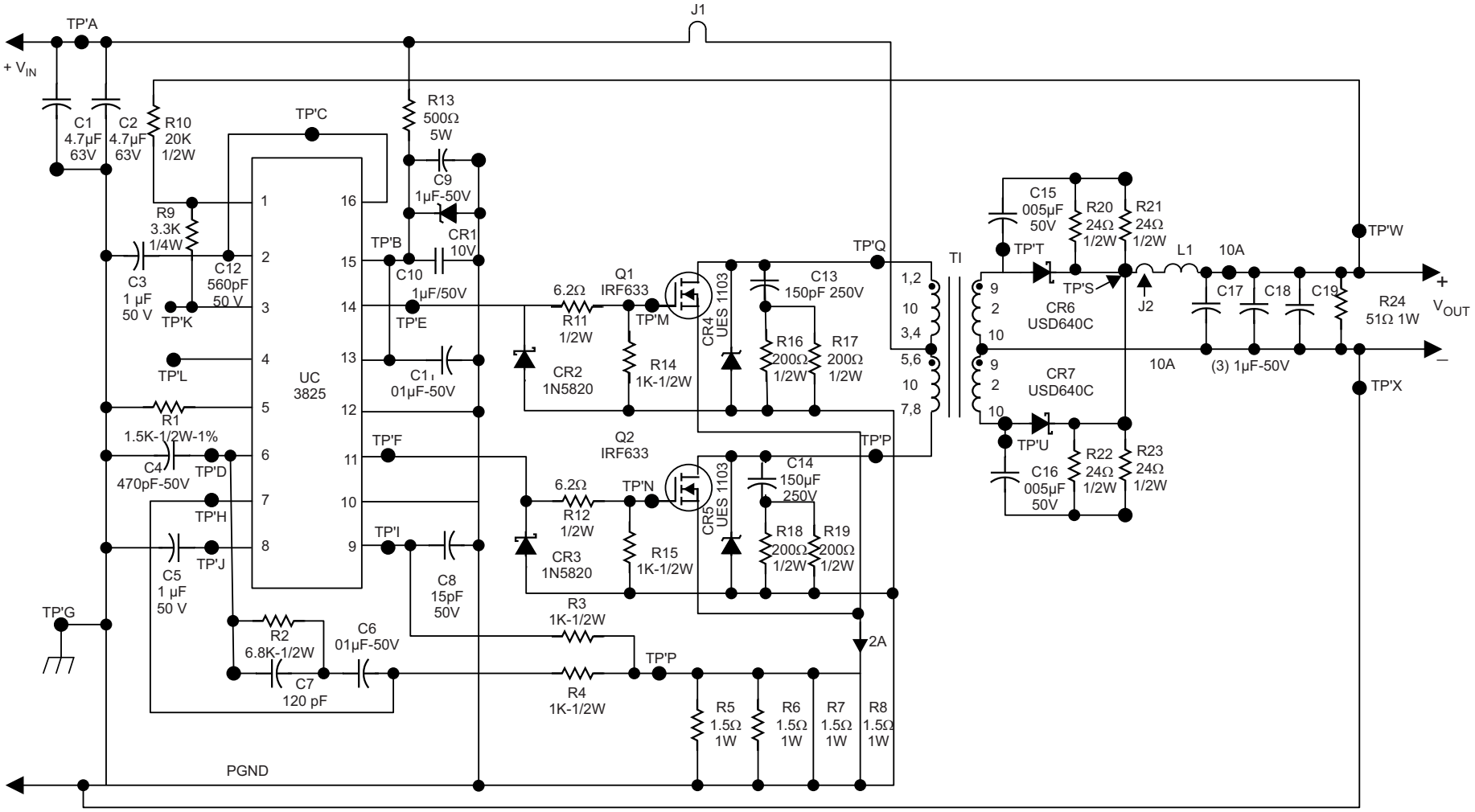

Figure 16. Typical Application Schematic

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9.2.1 Design Requirements

Table 1 lists the design parameters for this example.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	42 to 56 VDC
Switching Frequency	1.5 MHz
Output Power	51 W Maximum
Output Voltage	5.1 VDC (nom)
Output Current	2-10
ADC Line Regulation	5 mV
Load Regulation	15 mV
Output Ripple	100 mV (typical)
Efficiency	75% (typical)

9.2.2 Detailed Design Procedure

9.2.2.1 Auxiliary Supply Voltage

The 9.2-V minimum requirement of the UC1825 and 20-V gate-source maximum of the mosfets imply an approximate range from 10 V to 18 V of inputs. The 10-V value was selected to supply both VCC and VC (totem pole outputs) while keeping power dissipation in the IC low. The circuit used is a simple resistor-Zener dissipative network with ample bypassing capacitors located near the IC to reduce noise. The oscillator frequency selected is 1.5 MHz, thus resulting in a 670-ns period.

Oscillator frequency versus Rt, Ct, and deadtime curves:

- F0 = 1.5 MHz
- T period = 670 ns
- Cl = 470 pF
- Rt = 1.5 K

Therefore;

- T (on) = 570 ns (maximum)
- T (off) = 100 ns (minimum) DUTY CYCLE
- d max = T (on) max = 570 ns = 85% T (period) 670 ns

NOTE

These times will determine the mosfet device selection and transformer turns ratio. Preliminary

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9.2.2.2 Oscillator Frequency

The oscillator frequency selected is 1.5 MHz, resulting in a 670-ns period. For these equations, oscillator frequency versus Rt, Ct, and deadtime curves:

- F_0 = 1.5 MHz; T period = 670 ns
- C_l = 470 pF
- R_t = 1.5 K

Therefore;

- T (on) = 570 ns (maximum)
- T (on) = 570 ns (maximum)

$$\text{DUTY CYCLE, d max} = \frac{\text{T(on)max}}{\text{T(period)}} = 570\text{ ns}, 670\text{ ns} = 85\% \quad (3)$$

NOTE

These times will determine the mosfet device selection and transformer turns ratio.

9.2.2.3 Preliminary Considerations

Before designing the main transformer, several parameters must be defined and determined. Standard design procedures are used for this first-cut approximation.

9.2.2.4 Input Power

$$\text{Input power, P(in)} = \frac{\text{Output power, P(out)}}{\text{Efficiency, n}} \quad (4)$$

Let n = 75% for a 5 V, single output power supply.

$$\text{P(in)} = \frac{5.1\text{ V} \times 10\text{ a}}{0.75} = \frac{51\text{ watts}}{0.75} = 68\text{ watts} \quad (5)$$

9.2.2.5 Primary Current

The primary current can be approximated using the low-line constraints of 42-V DC as shown in Equation 6:

$$\text{Primary Current (dc)} = \frac{\text{Input power P(in)}}{\text{Input power V(in)}} = 68\text{ watts}, 42\text{ volts} \quad (6)$$

The primary current during the transistor on time is calculated by Equation 7:

$$\text{I(p)} = \frac{\text{I(dc)}}{\text{d(max)}} = \frac{1.62\text{A}}{0.85} = 1.9\text{ amps, or approx. 2 A} \quad (7)$$

The RMS primary current is calculated by Equation 8:

$$\text{Ip(rms)} = \text{Ip}\sqrt{\text{duty}} = 1.24\text{ A (rms)} \quad (8)$$

9.2.2.6 Sense Resistor R(s)

Primary current is sensed and controlled in a current mode controller by first developing a voltage proportional to the primary current, used as an input to UC1825A-SP. This is accomplished by sense resistor R(s) with a calculated value of the I limit threshold value divided by the primary current at the desired current limit point, typically 120% I (maximum) shown in Equation 9.

$$\text{R(s)} \le \frac{\text{V th (pin 9)}}{120\%_1 \times \text{I(pri)}} = \frac{1\text{ volt}}{1.2 \times 2\text{ amps}} = 0.42\ \Omega \quad (9)$$

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9.2.2.7 MOSFET DC Losses

A high-quality mosfet is used to keep both DC and switching losses low, with an R(ds) on max of 0.8 Ω (see Equation 10 to Equation 13). Calculation of the voltage drops across the device are required for the transformer design.

$$Vds(on) = Rds(max) = 0.8 \times 2 = 1.6\ V \quad (10)$$

During an overload:

$$Vds(max) = 0.8 \times 2 \times 1.2 = 1.92\ V\ (2\ V) \quad (11)$$

$$P\ dc = Idc^2\ Rds(max) \times duty \quad (12)$$

$$= 2^2 \times 0.8 \times 0.85 / 2 = 1.35\ W \quad (13)$$

9.2.2.8 Selection of Core Material

Few manufacturers provide core loss curves for frequencies above 500 khz. To minimize power dissipation in the core, the flux density must be drastically reduced in comparison to the 20 kHz to 150 kHz versions. Typical operation is at a total flux density swing, delta B, of 0.030 Tesla (300 Gauss) while approaching the 1 MHz region. TDK's H7C4 material was selected for it's low loss, high frequency characteristics.

9.2.2.9 Main Transformer Design

The first step in transformer design is to determine the preliminary turns ratio. Once obtained, the minimum cross-sectional area core (Ae) can be calculated, and core selection made possible.

9.2.2.10 Calculation of Transformer

Voltages and Turns Ratio is calculated by Equation 14 through Equation 19.

$$V\ pri\ (min) = Vin(min) - V\ xtor(max) - V(Rs)\ max \quad (14)$$

$$Vp(min) = 42\ V - 2\ V - 1\ V \quad (15)$$

$$= 39\ V \quad (16)$$

$$V\ sec\ (min) = Vout(max) + V\ diode\ (maximum) + V\ choke\ (DC) + V\ (losses) \quad (17)$$

$$V\ sec(min) = 5.1 + 0.65 + 0.1\ _\ 0.05\ (est) = 5.9\ V \quad (18)$$

$$\text{Turns ratio } N = \frac{V\ pri\ (min)\ Duty\ (max)}{V\ sec\ (min)} = \frac{39.0 \times 0.85}{5.9} = 5.6:1 \quad (19)$$

The secondary is designed for excellent coupling using copper foil, and the primary has been rounded to the nearest lower turns (see Equation 20).

$$\text{Turns ratio: } N = N\ pri / N\ sec = 5{:}1 \quad (20)$$

The actual number of both primary and secondary turns will be determined by the ferrite core characteristics as a function of operating frequency and Gauss level.

9.2.2.11 Minimum Core Size

The minimum cross-sectional area core that can be used is calculated with Equation 21 for core loss limited applications.

$$Ac\ (min) = \frac{V\ (pri)\ min \times Duty\ (max) \times 10^4}{2 \times Freq \times N(p) \times \Delta B\ (Tesla)} (cm^2) \quad (21)$$

At first it would seem that the core area required for this 1.5-MHz switcher would be ten times smaller than that of a 150-kHz version. This would be true if the flux density, number of turns and core losses remained constant. However, losses are a function of frequency, and as frequency increases, the flux density swing (Delta B) must be drastically reduced to provide a similar core loss, hence temperature rise. In this example, an acceptable figure was selected of one percent of the total output power, or one-half watt. Empirically, this translates to a temperature rise of 25°C, at 325 Gauss (0.0325 Tesla) for cores with a cross-sectional area of 0.70 cm^2, a ballpark estimate of the true core size. This formula can be rewritten as Equation 22:

$$Ac \times Np = \frac{V\ (pri) \times D\ max \times 10^4}{2 \times F \times \Delta B} \quad (22)$$

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Equation 22 is a more convenient formula because the right hand side of the equation contains all constants. Input voltage, frequency of operation and flux density have already been determined. The selection of core size (cross-sectional area) is inversely proportional to the number of primary turns, and conversely. Based on the five-to-one turns ratio, an original assumption of five turns for the primary would result in a large core size for this 50-W application. Alternatively, a ten turn primary is used to minimize core size.

Substituting previous values for high line operation at 0.0325 Tesla (325 Gauss) and a magnetic operating frequency of 750 kHz is calculated by Equation 23:

$$\text{Ac (min)} = \frac{39 \times 0.85 \times 10^4}{2 \times 750{,}000 \times 10 \times 0.0325} \tag{23}$$

9.2.2.12 Core Loss Limited Conditions

As the switching frequencies are increased, generally a reduction of core size or minimum number of turns is realized. This is true, however, but only to the point at which the increasing core losses prevent a further reduction of either size or minimum turns. This crossover point occurs at different frequencies for each individual ferrite material based upon their losses and acceptable circuit losses, or temperature rise.

9.2.2.13 Core Geometry Selection

A variety of standard core shapes are available in the cross-sectional area range of 0.62 cm^2 to 0.84 cm^2 (see Table 2). Considerations of safety agency spacing requirements, physical dimensions, window area and relative cost of assembly must be evaluated.

Table 2. Core-Style Descriptions

CORE STYLE	DESCRIPTION	AC (cm^2)	WEIGHT (g)
PQ	PQ 20/20	0.62	15
POT CORE	P 22/13	0.63	13
LP	LP 22/13	0.68	21
TOROID	T 28/13	0.76	26
EE	EE 35/28	0.78	28

The LP 22/13 style was selected to easily terminate (breakout) the high current output windings. For a given cross-sectional area, it occupies less PC board space, and has good shielding characteristics.

9.2.2.14 Wire Size Selection

The single, most difficult task in high frequency magnetic design is to minimize the eddy current losses, or skin effects while optimizing wire sizes. Penetration depth refers to the thickness (or depth) into a copper conductor in which a wave will penetrate for a specific frequency. For copper at 100°C, use Equation 24:

d pen = 7.5 / (frequencyo5) (cm) (24)

At 750 kHz, this corresponds to 8.66 × 103 cm, or about the thickness of an AWG #39 wire. Larger size wire can be used, however the AC current flows only in the depth penetrated at the switching frequency.

For low current windings, several strands of thin wire can be paralleled, or twisted together forming a bundle. Seven wires twisted around each other closely approximate a round conductor with a net diameter of three times the individual wire diameter. This twisting is commonly done at 10-12 turns per foot, and significantly reduces parasitics between wires at high frequencies.

Medium to high current windings require the use of Litz wire, a similar bundle of numerous conductors. Copper foil is also an excellent choice.

Industry practice is to operate at 450-A (RMS) per centimeter squared, or 2.22 × 10^{-3} cm^2/A, which applies to windings operating at an acceptable temperature rise (see Equation 25 through Equation 31).

Area required = Irms 450 A / cm* (25)

Primary area (Axp) = 1.24 A / 450 A / cm^2 = 2.75 × 10^{-3} cm^2 (26)

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9.2.2.15 Calculate Secondary RMS Current

$$I_{rms}(sec) = \sqrt{I_{sec}{}^2 \times (duty_on) + \left(\frac{I_{sec}}{2}\right)^2 (2 \times duty_off)} \quad (27)$$

$$I_{rms}(sec) = \sqrt{(10)^2 \times (duty_on) + \left(\frac{10}{2}\right)^2 (2 \times duty_off)} \quad (28)$$

Irms(sec) = 4.81 A (29)

Secondary Area (Axs) = 4.81 A / 450 A I cm* (30)

= 1.07×10^{-2} cm^2 (31)

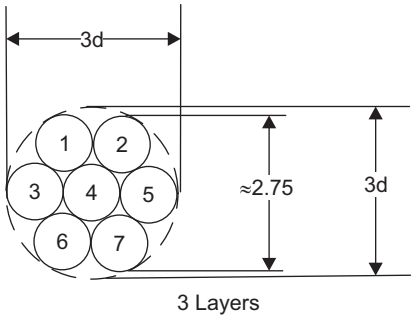

Figure 17. 7 Conductors

For a given bundle of 7 conductors as shown in Figure 17, the cross-sectional area of each conductor can be calculated by Equation 32:

$$\frac{\text{Required area}}{\#\text{ conductors}} = \frac{Axp}{7} = \frac{2.75\,10^{-3}}{7} = 3.93 \times 10^{-4}\,cm^2 \quad (32)$$

The cross-sectional area of an AWG 36 wire is 1.32×10^{-4}; therefore, three bundles of seven conductors each must be used. Two bundles were used as a compromise between practical winding considerations and acceptable eddy current losses.

Copper foil is used for the secondary, with a required width slightly less than the bobbin width, and thickness determined by Equation 33:

$$\frac{\text{Secondary area (Axs)}}{\text{Bobbin width}} = \frac{1.07\,10^{-2}\ cm}{1.40\ cm} = 7.64 \times 10^{-3}\ cm \quad (33)$$

This corresponds to 0.003” thick foil, a standard value. In practice, slightly thicker foil (0.004” to 0.005”) may be required to minimize power losses in the transformer.

9.2.2.16 Transformer Assembly

Standard practice to increase coupling between primary and secondary is position both as closely as possible to each other inside the transformer. In this design, the first layer wound is one primary, and the next layer is the corresponding secondary. This is again followed by the other secondary and primary. It is important to keep the secondaries in close proximity because both will be conducting simultaneously twice per period. The primaries do not conduct in this manner, so coupling from primary A to primary B is not critical, only primary A to secondary C, and primary B to secondary D.

Referring to Figure 18, primary A is wound closest to the bobbin. After insulation, secondaries C and D are wound bifilar and insulated (see Figure 19). Primary B is wound last, then terminated so that primaries A and B are wired in series, likewise for secondaries C and D.

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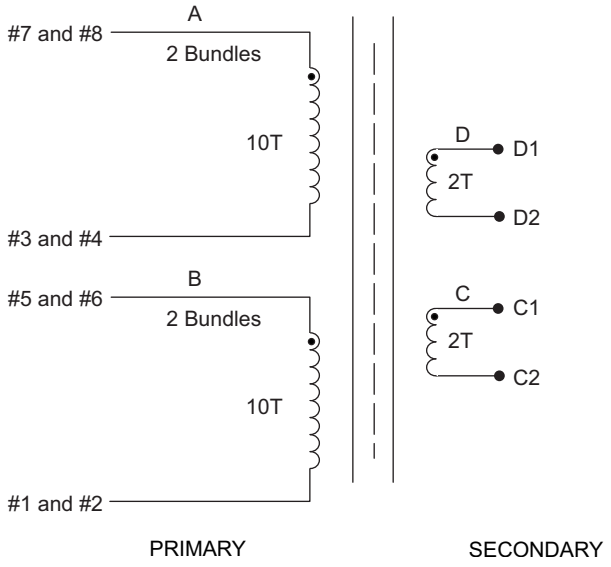

Figure 18. Transformer Schematic

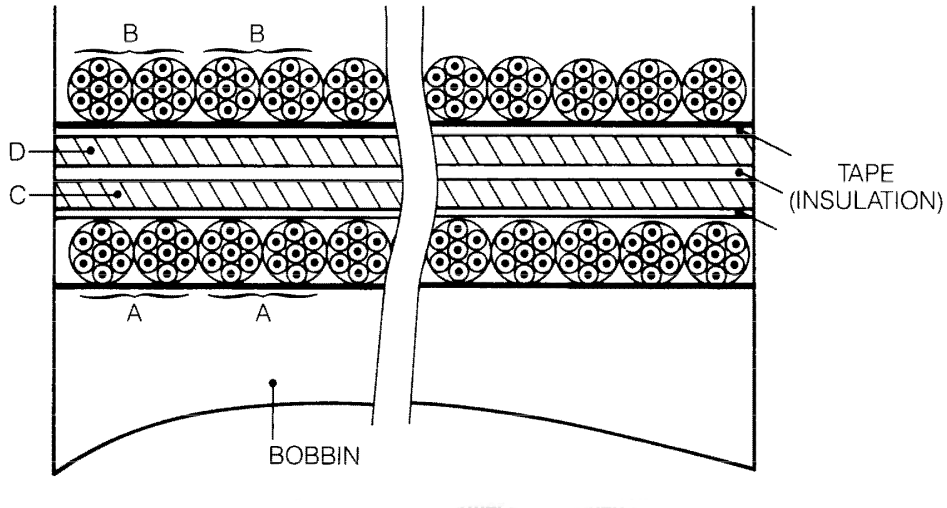

Figure 19. Transformer – Exploded View

9.2.2.17 Calculation of Winding Resistances and Losses

The mean length of turn for the bobbin can be determined from the specifications of O.D. and I.D., and for the BLP 22/13 a figure of 4.51 cm or 1.77 inches was obtained. AWG #36 wire has a resistance of 1.82×10^{-2} Ω/cm at 100°C for the following:

Primary resistance can be calculated by Equation 34:

$$\frac{\text{R wire} \times \text{M.L.T.} \times \#\text{turns}}{\#\text{wires}} = \frac{0.0182.4.51 \times 10}{14} = 0.0586\ \Omega \quad (34)$$

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Voltage drop and power loss in each half winding can also be calculated by Equation 35 through Equation 37:

$$V(Rpri) = Ipri \times Rpri = 2 \times 0.58 = 0.116\ V \text{ (negligible)} \quad (35)$$

$$P(Rpri) = R\ pri \times I\ pri^2 \times duty = 0.0586 \times (2^2) \times 0.425 \quad (36)$$

$$= 0.0996\ W \quad (37)$$

The resistance of the secondary can be approximated by using the wire tables, and substituting the foil for wire of similar cross-sectional area. In this example, AWG #16 wire is used to obtain Rsec = 1.58×10^{-4} Ω/cm.

$$Rsec = R\ foil \times M.L.T \times I\ number\ turns = 1.58 \times 10^{-3} \times 4.5 \times 2 = 0.00143\ \Omega \quad (38)$$

$$V(Rsec) = 1.43 \times 10^{-3} \times 10 = 0.0143\ V \text{ (negligible)} \quad (39)$$

$$\sqrt{I_{dc}^2(D_on) + \left(\frac{I_{dc}}{2}\right)^2 \times 2 \times D_off} \quad (40)$$

$$P(Rsec) = 0.00143\ (10^2 \times 0.425) + (5^2 \times 0.15)] = 0.066\ W \quad (41)$$

9.2.2.18 Transformer Power Losses

The total copper losses for two windings are then calculated by Equation 42:

$$Pcu = P(Rpri) + P(Rsec) = 2 \times (0.066 + 0.0996) = 0.332\ W \quad (42)$$

Estimated eddy current losses are approximately 50% of the copper losses. Pcu ≈ 0.50 W.

Given the core material type, geometry, frequency and operating Gauss level, the ferrite losses can be calculated. From the manufacturers information, the typical loss coefficient for H7C4 material operating at a flux density swing of 0.035 Tesla (350 Gauss) at 750 kHz is 0.15 W per cubic centimeter of core volume, which is 3.327 cm^3 per LP 22/13 core set; therefore Equation 43:

$$Pcore = 3.327 \times 0.15 = 0.50\ W \quad (43)$$

The total power lost is a summation of the copper and ferrite losses calculated by Equation 44:

$$Pxfmr = Pcu + Pcore = 0.50 + 0.50 = 1.00\ W \quad (44)$$

9.2.2.19 Output Section

9.2.2.19.1 Output Choke Calculations

Typically, the RMS output ripple current is less than 15% Idc, or 1.5 A in this case. Delta I, the peak-to-peak ripple therefore is twice the RMS, or 3 A as calculated by Equation 45.

$$V = \frac{L\ di}{dt} \quad L = \frac{V\ dt}{di} = \frac{5.9\ v\ (350)\ 10^{-9}\ s}{3.0\ A} = 690\ \text{nanohenries} \quad (45)$$

Due to the small value of inductance required, the conventional approach will not be used. Instead, a simple RF type wound coil will be designed using the solenoid equation found in most reference texts. A thick pencil will be used as the coil form with a diameter of 0.425 inches; however, any similar item will suffice.

The form factor, F, is a function of the form diameter divided by the length of the wound coil, or D/L (see Equation 46). A few gyrations will take place before the exact values are obtained; however, this goes quickly. The form factor is listed in Table 3 for various practical values of D/L.

Table 3. Form Factor

COIL DIAMETER, LENGTH	FORM FACTOR F
0.1	0.0025
0.25	0.0054
0.5	0.01
1	0.0173
2	0.026
5	0.04

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$L(\mu H) = F \times N^2 \times D(\text{inches}),\ N = (L/F \times D)^1 \text{ (turns)}$

where

- D = 0.425
- D/L = 1 (approximately)
- F = 0.0173
- $N = (0.690 / 0.0173 \times 0.425)^{12} = 9.76$ turns (46)

Rounding off to the nearest next number of turns the actual inductance for 10 turns can be calculated by Equation 47:

$L(\mu H) = 0.0173 \times 10^2 \times 0.425 = 744$ nH (47)

In an air core inductor, the permeability *u* equals unity; therefore, the flux density B equals the driving function H.

9.2.2.19.2 Output Capacitor

$$Q = \frac{\text{Ip-p}}{2} \times \frac{\text{T period}}{2} \times \frac{1}{2}, \text{Delta } Q = \text{Ip-p} / 8 \times F \quad (48)$$

C = Q / dV

where

- dV (output ripple) equals 0.1 V. (49)

$C = \text{Ip-p} / 8 \times F \times dV = 3/8 \times 1.5 \times 10^6 \times 0.1 = 2.5\ \mu F$ (50)

Three 1-µF capacitors are used in parallel. With a typical ripple voltage of approximately 50 mV due to ESR, the ESR each (at 1.5 mHz) must be approximately 150 mΩ. The Unitrode ceramic monolithic capacitor series was selected for their excellent high frequency characteristics.

Resonance, and its effect at these frequencies must be taken into account. In this case, the capacitor reaches resonance at 1.5 mHz, and the effective impedance is resistive.

9.2.2.19.3 Output Diodes

Schottky diodes were selected for their short reverse recovery times to minimize switching losses, and low forward drop for high DC efficiency.

9.2.2.20 UC1825A-SP PWM Control Section

9.2.2.20.1 Current Limit and Shutdown

Pulse-by-pulse current limiting is performed by the UC1825A-SP by an input of the primary current waveform to the IC at pin 9. The small RC network of R3 and C8 are used to suppress the leading edge glitch caused by turnon of the MOSFET and transformer parasitics. The input must be less than the 1-V threshold or current limiting will occur. Once reached, an input above the threshold will narrow the pulse width accordingly. When this reaches a 1.4-V amplitude, shutdown of the outputs will occur, and the UC1825A-SP will initiate a soft start routine.

9.2.2.20.2 Ramp

The UC1825A-SP offers the flexibility of both Current Mode Control or conventional duty cycle control through the RAMP input pin. When connected to the timing capacitor, the UC1825A-SP operates as a duty cycle control IC. Connecting the RAMP input to the current waveform changes the control method to Current Mode. In this application, the ramp waveform is tied through a small RC filter network to the primary current waveform. This network is defined in the next section, *Slope Compensation*. The dynamic range of this input is 1 V to 3 V, and is generally used for introducing slope compensation to the PWM.

9.2.2.20.3 Slope Compensation

Slope compensation is required to compensate for the peak to average differences in primary current as a function of pulse width. Adding a minimum of 50% of the reflected downslope of the output current waveform to the primary current is required. See the Unitrode application note *A New Integrated Circuit for Current Mode Control* (SLUA075) and the Unitrode application note *Modelling, Analysis and Compensation of the Current-Mode Converter* (SLUA101) for further information. Empirically, 60-75% must be used to accommodate circuit

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tolerances and increase stability5 Resistors R2 and R4 in this circuit form a voltage divider from the oscillator output to the RAMP input, superimposing the slope compensation on the primary current waveform. Capacitor C6 is an AC coupling capacitor, and allows the 1.8-V swing of the oscillator to be used without adding offset circuitry. Capacitor C7 has a two-fold purpose. During turnon it filters the leading edge noise of the current waveform, and provides a negative going pulse across R4 to the ramp input at the end of each cycle. This overrides any parasitic capacitance at the ramp input, (pin 7) that would tend to hold it above 0 V. This insures the proper voltage input at the beginning of the next cycle.

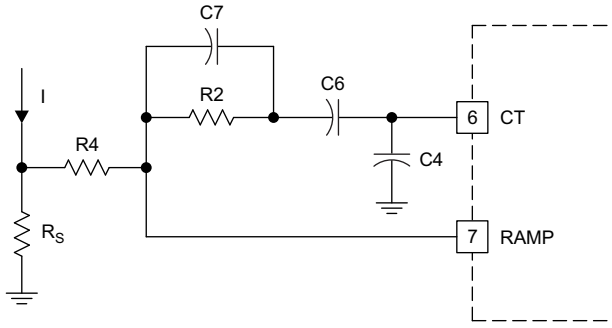

Figure 20. Slope Compensation Steps

For the purposes of determining the resistor values, capacitors C4 (timing), C6 (ac coupling) and C7 (filtering) can be removed from the circuit schematic. The simplified model represented in Figure 21 is used for the calculations in Equation 51 through Equation 61. These calculations can be applied to all current-mode circuits using a similar scheme.

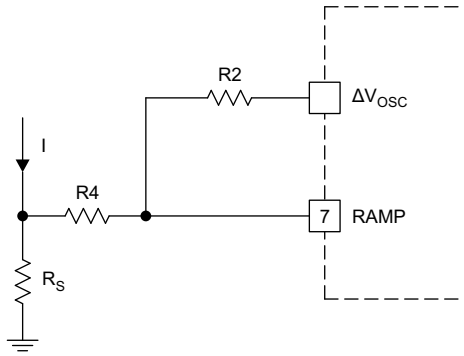

Figure 21. Slope Compensation Steps

- STEP 1. Calculate Inductor Downslope:
  $S_L' = di/dt = Vsec / L = 5.9\ V / 0.740\ pH = 8\ A/\mu S$ (51)
- STEP 2: Calculate Inductor Downslope:
  $S_L' = S_L' / N\ (turns\ ratio) = 8/5 = 1.6\ A/\mu S$ (52)
- STEP 3: Calculate Equivalent Ramp Downslope Voltage:
  $V\ S_L' = S_L' \times Rsense = 1.6 \times 0.375 = 0.600\ V/\mu S$ (53)
- STEP 4: Calculate Oscillator Slope:
  $VS(osc) = d(V_{osc}) / T\ on = 1.8\ V / 570\ ns = 3.15\ V/\mu S$ (54)
- STEP 5: Generate the Ramp Equations: Using superpostion, the circuit can be configured as shown in Figure 22.

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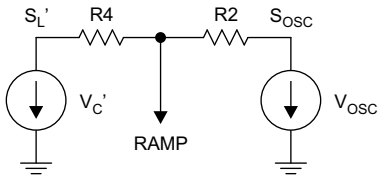

Figure 22. Slope Compensation Steps

$$V(ramp) = \frac{VS(L) \times R2}{R2 + R4} = \frac{VS(osc) \times R4}{R2 + R4} \quad (55)$$

Substituting

$$V(ramp) = VS(L) + VS(comp) \quad (56)$$

Where

$$VS(comp) = \frac{VS(osc) \times R4}{R2 + R4}; VS(L)'' \frac{VS(L)' \times R2}{R2 + R4} \quad (57)$$

- STEP 6: Calculate Slope Compensation:

  $$VS(comp) = m \times S(L)$$

  where

  - m equals the amount of inductor to be introduced.

  In this example, let m = 75%, or 0.75. (58)

  $$\frac{VS(osc) \times R4}{R2 + R4} = \frac{m \times VS(L)' \times R2}{R2 + R4} \quad (59)$$

  Solving for R2:

  $$R2 = R4 \times \frac{VS(osc)}{VS(L)' \times m} = R4 \times \frac{3.15}{0.600 \times 0.75} \quad (60)$$

  Using Circuit Values:

  $$R2 = 7.05 \times R4 \quad (61)$$

  For simplicity, let R4 equal 1 kΩ and R2 therefore equals 7.05 K. Using the nearest standard value resistor of 6.8 K, the exact amount of downslope is minimally affected. It is important that the series combination of R2 and R4 is high enough in resistance not to load down the oscillator and cause frequency shifting.

9.2.2.21 Closing the Feedback Loop

9.2.2.21.1 Error Amplifier

Compensation of the high gain error amplifier in the UC1825A-SP is straight forward. There is a single- pole at approximately 5 Hz. A zero will be introduced in the compensation network to provide gain once the zero db threshold is crossed. Using Current Mode control greatly simplifies the compensation task as the output choke is controlled by the inner current loop, thus making the output section appear as a single pole response with a zero at the ESR frequency.

9.2.2.21.2 Control to Output Gain

The control to output gain will vary with output loading, and as the load is increased the gain decreases. Output capacitor ESR will determine the frequency at which the zero occurs, thus changing the gain as a function of ESR. To ensure stability through all combinations of load and ESR, the amplifier will be compensated to cross zero db at approximately one-fifth of the switching frequency with ample phase margin.

The output filter pole and zero occur at:

$$F_p = 1/2\ \pi\ R(load)\ C(output) \quad (62)$$

$$F_p = 1/2\ \pi\ R\ (esr)\ C\ (output) \quad (63)$$

Circuit Parameters:

C (output) = 3 pF; ESR (each) = 0.050 min – 0.300 max (64)

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For three capacitors in parallel:

ESR = 0.016 – 0.100 Ω (65)

R(output) = 2.5 Ω at 2 A, 0.5 Ω at 10 A (66)

Using the previous Equations:

F_p (2 A) = 1 / (2 × 3.14 × 2.5 × 3 × 10^{-6}) = 21.2 kHz (67)

F_p (10 A) = 1 / (2 × 3.14 × 0.5 × 3 × 10^{-6}) = 106.1 kHz (68)

F_p (high) = 1 / (2 × 3.14 × 0.016 × 3 × 10^{-6}) = 3.315 mHz (69)

F_Z(low) = 1 / (2 × 3.14 × 0.100 × 3 × 10^{-6}) = 530.5 kHz (70)

Gain:

$$\frac{V(output)}{V(control)} = K \times R_O, \text{ where } K = \frac{Ipri \times N_p / N_s}{V(control)} = \frac{2 \times 5}{0.85} = 11.76 \quad (71)$$

Therefore, at 2 A and 10 A:

V_o / V_c = K × ro = 11.76 × 2.5 = 29.4 db (2A) (72)

V_o / V_c = K × ro = 11.76 × 0.5 = 15.4 db (73)

9.2.2.21.3 Error Amplifier Compensation

The control to output gain can be plotted along with the desired zero db crossing point and an estimate of the error amplifier required compensation network can be made. The amp compensation must have a zero at approximately 100 kHz, and a gain of –16 db at this frequency. Resistor R9 has been selected to be 3.3 kΩ based on the output drive capability of the UC1825A-SP amplifier (see *Specifications*).

F zero (amp) = 1 / (2 × 7r × R9 × C12) (74)

Therefore,

Cl2 = 1 / (2 × π × R9 × F zero) (75)

C12 = 1 / (2 × 3.14 × 3300 × 100.000) = 480 pF (use 560 pF) (76)

R10 / R9 = approximately –16 db (0.16) (77)

R10 = R9 / gain = 3.3 K / 0.16 = 20.4 K (use 20 K) (78)

This compensated response can now be plotted, along with the control to output gain and the overall power supply response is a summation of the two curves, as seen in Figure 1 and Figure 2. Low-frequency gains of 100 db at full load, and 115 db at light load are obtained, with a zero db crossing at approximately 100 kHz for both. Phase margin is generous with approximately 90 degrees for both light and 45 degrees at full load. See Figure 1 and Figure 2 for more details.

Table 4. List of Materials: Capacitors

CAPACITOR	DESCRIPTION
C1, 2	4.7 µF, 63 VDC Electrolytic
C3, 5	0.1 µF, 50 VDC Monolithic
C4	470 pF, VDC Monolithic
C6	0.01 µF, 50 VDC Monolithic
C7	120 pF, 50 VDC Monolithic
C8	15 pF, 50 VDC Monolithic
C9-11, 17-19	1 µF, 50 VDC Monolithic
C12	560 pF, 50 VDC Monolithic
C13,14	150 pF, 150 VDC Ceramic
C15, 16	5000 pF, 50 VDC Ceramic

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Table 5. List of Materials: Diodes

DIODE	DESCRIPTION
CR1	1N4465 10 V, 1.5 W Zener
CR2,3	USD1140 40 V, 1 A Schottky
CR4,5	UES1105 150 V, 2.5 A Ultrafast
CR6,7	USD640C 40 V, 12 ASchottky

Table 6. List of Materials: Integrated Circuits

INTEGRATED CIRCUIT	DESCRIPTION
U1	UC1825A-SP TI High Speed PWM

Table 7. List of Materials: Transistors

TRANSISTORS	DESCRIPTION
Q1,2	UFN633 150 V, 8A Mosfet

Table 8. List of Materials: Resistors

RESISTORS	DESCRIPTION
R1	1.5 K, 1/2 W, 1%
R2	6.8 K, 1/2 W, 5%
R3, 4, 14, 15	1 K, 1/2 W, 5%
R5-8	1.5 R, 1 W, 5%
R9	3.3 K, 1/2 W, 5%
R10	20 K, 1/2 W, 5%
R11, 12	6.2 R, 1/2 W, 5%
R13	500 R, 5W, 10%
R16-19	200 R, 1/2 W, 5%
R20-23	24 R, 1/2 W, 5%
R24	51 R, 1 W, 5%

Table 9. List of Materials: Magnetics

MAGNETIC	DESCRIPTION
L1	740 nH Wound Coil
T1	AIE Magnetics Custom Transformer, 5:1 Turns Ratio

Table 10. List of Materials: Miscellaneous

MISCELLANEOUS	DESCRIPTION
H1	Heatsink-Mosfets (AAALL #5786B)
H2	Heatsink-Diodes (AAALL #5299B)

Table 11. List of Materials: Efficiency Measurements

V(IN)	I(IN)	P(IN)	P(LOSS)	EFFICIENCY
42	1.707	71.1	20.2	71.8%
48	1.483	71.2	19.7	72.4%
56	1.331	73.2	21.7	70.4%

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Table 12. List of Materials: Efficiency Measurements

V(IN) V	VOUT (2 A)	VOUT (5 A)	VOUT (10 A)	LOAD REGULATION (mV)
42	5.110	5.102	5.093	17
48	5.108	5.101	5.092	16
56	5.108	5.102	5.089	19
Line	2 mV	1 mV	4 mV	—

9.2.2.21.4 Dynamic Performance

The power supply was pulse loaded from 5 A to 10 A at a frequency of 100 kHz. Recovery to within 50 mV was less than 2 ms with a total excursion of less than 200 mV. High speed FETS were used to switch the load current with typical rise and fall times of 50 ns.

9.2.2.21.5 Short Circuit

The short circuit input current is approximately 0.75 A, or an input power of 36 W.

9.2.2.21.6 Circuit Power Losses

Table 13 lists the total circuit losses are approximated using both the calculated and measured losses throughout the power supply.

Table 13. Circuit Power-Loss Descriptions

POWER LOSSES	VALUE
Current sense circuit	1.2 W
Output Diodes	98 W
Switching transistors	3.2 W
Dropping resistor	3 W
Snubber networks	1 W
Transformer losses	1 W
Auxillary supply	0.8 W
Miscellaneous	0.2 W
TOTAL LOSSES	**20.2 W**

If a bootstrapped technique is used in the auxiliary supply to the IC and drive circuitry, the dropping resistor losses of three watts can be reduced to 0.1 W in the bootstrap circuitry. In addition, the lossy resistive current sensing network can be replaced by a small current transformer, lowering the losses by a half-watt. Overall efficiency would then increase to 75%, fairly high for a five volt output application. Switching losses at this high of frequency can be minimized, and have little overall effect on circuit efficiency.

9.2.2.22 Summary

The demands of higher power densities will undoubtedly throttle many switch-mode power supply designs into and beyond the megahertz region in the near future. Designers will be facing the challenges of selecting switching devices, magnetic materials and IC controllers built exclusively for high efficiency at these frequencies. The thrust from contemporary hundreds of kHz designs to MHz versions is rapidly making progress. This 1.5-MHz current mode push-pull is an example of what can successfully be accomplished with existing high speed components and technology.

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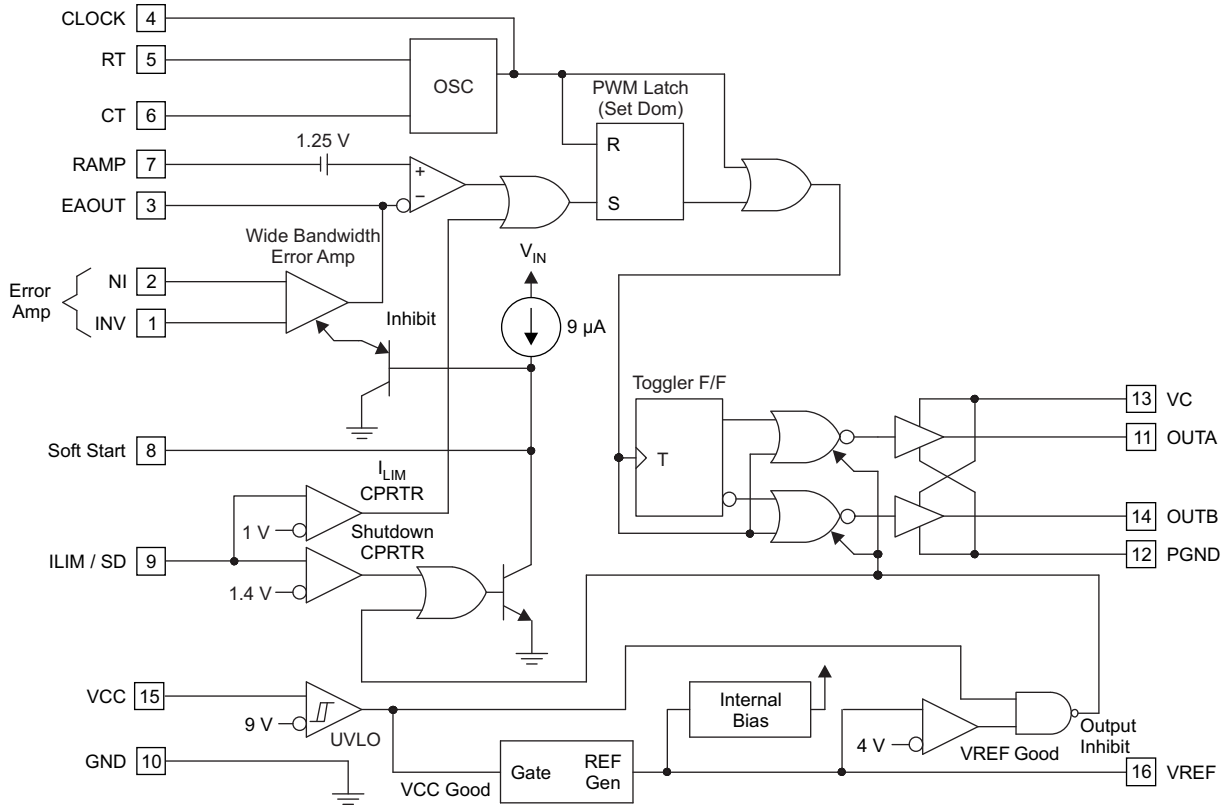

Figure 23. UC1825A-SP Block Diagram

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9.2.3 Application Curves

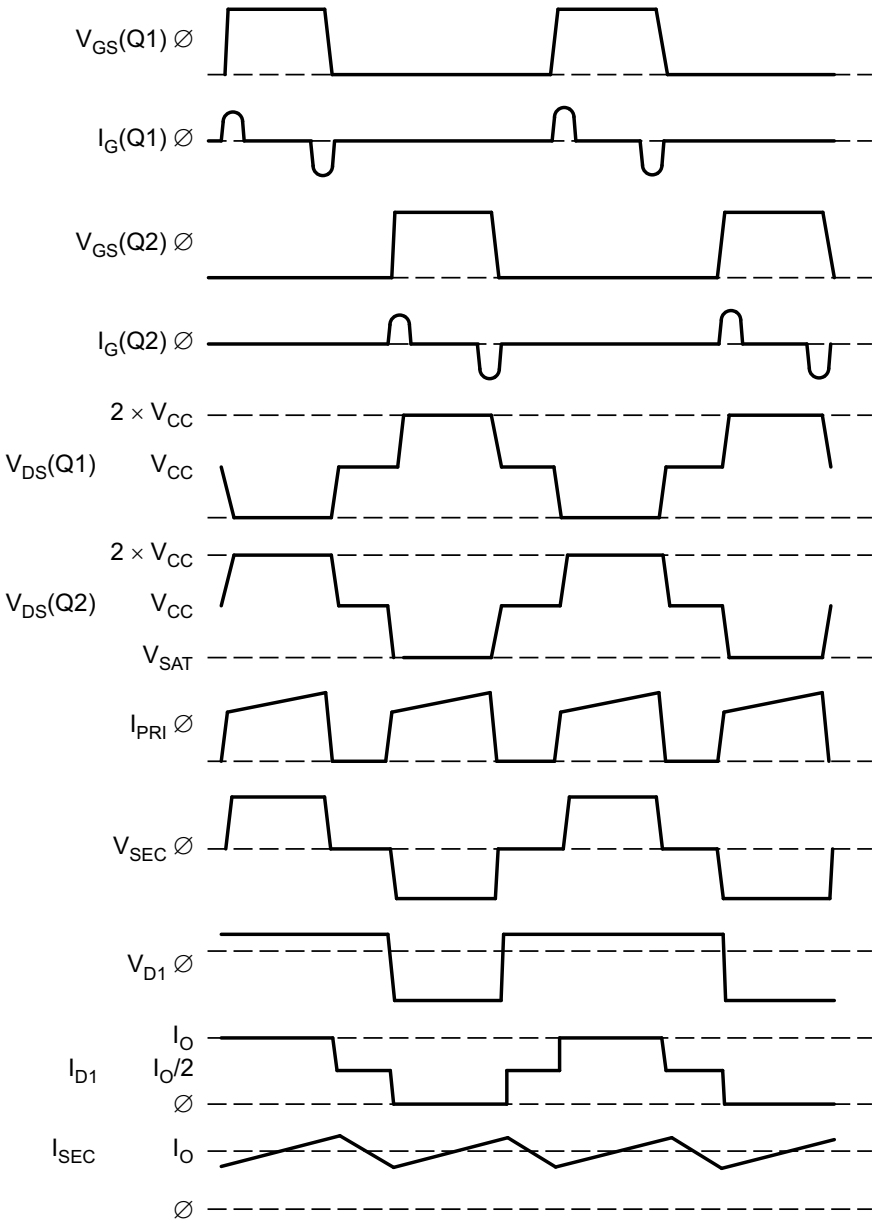

Figure 24. Basic Push-Pull Waveforms

10 Power Supply Recommendations

The UC1825A-SP is designed to operate from an input voltage supply range between 12 V and 20 V. This input supply should be well regulated. If the input supply is located more than few inches from the UC1825-SP converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. A tantalum capacitor with a value of 47 uf is a typical choice; however, this may vary depending upon the output power being delivered.

The UC1825A-SP controller can be used to convert power efficiently using any of several standard topologies such as push-pull, forward, half-bridge, or full bridge. Design tradeoffs of cost, size, and performance narrow the field to the one that is most appropriate. For a typical application, such as in Figure 16, push-pull converter topology is highlighted.

11 Layout

11.1 Layout Guidelines

Always use a low EMI inductor with a ferrite-type closed core. Some examples would be toroid and encased E core inductors. Open core can be used if they have low EMI characteristics and are located a bit more away from the low power traces and components. Make the poles perpendicular to the PCB as well if using an open core. Stick cores usually emit the most unwanted noise.

11.1.1 Feedback Traces

Run the feedback trace as far from the inductor and noisy power traces as possible. The feedback trace should be as direct as possible and somewhat thick, which sometimes involves a trade-off, but keeping the feedback trace away from inductor EMI and other noise sources is more critical. Run the feedback trace on the side of the PCB opposite of the inductor with a ground plane separating the two.

11.1.2 Input/Output Capacitors

When using a low-value ceramic input filter capacitor, it must be located as close as possible to the VIN pin of the IC. This will eliminate as much trace inductance effects as possible and give the internal IC rail a cleaner voltage supply. Some designs require the use of a feed-forward capacitor connected from the output to the feedback pin as well, usually for stability reasons. In this case, it must also be positioned as close as possible to the IC. Using surface-mount capacitors also reduces lead length and lessens the chance of noise coupling into the effective antenna created by through-hole components.

11.1.3 Compensation Components

External compensation components for stability must also be placed close to the IC. Surface mount components are recommended here as well for the same reasons discussed for the filter capacitors. Locate the surface-mount components away from the inductor.

11.1.4 Traces and Ground Planes

Make all of the power (high current) traces as short, direct, and thick as possible. It is good practice on a standard PCB board to make the traces an absolute minimum of 15 mils (0.381 mm) per Ampere. The inductor, output capacitors, and output diode must be as close as possible to each other. This helps reduce the EMI radiated by the power traces due to the high switching currents through them. This will also reduce lead inductance and resistance as well, which in turn reduces noise spikes, ringing, and resistive losses that produce voltage errors. The grounds of the IC, input capacitors, output capacitors, and output diode (if applicable) must be connected close together directly to a ground plane. It would also be a good idea to have a ground plane on both sides of the PCB. This will reduce noise as well by reducing ground loop errors as well as by absorbing more of the EMI radiated by the inductor. For multilayer boards with more than two layers, a ground plane can be used to separate the power plane (where the power traces and components are) and the signal plane (where the feedback and compensation and components are) for improved performance. On multilayer boards, the use of vias will be required to connect traces and different planes. It is good practice to use one standard via per 200 mA of current if the trace must conduct a significant amount of current from one plane to the other. Arrange the components so that the switching current loops curl in the same direction. Due to the way switching

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Layout Guidelines (continued)

regulators operate, there are two power states. One state when the switch is on and one when the switch is off. During each state there will be a current loop made by the power components that are currently conducting. Place the power components so that during each of the two states the current loop is conducting in the same direction. This prevents magnetic field reversal caused by the traces between the two half-cycles and reduces radiated EMI.

11.1.5 Ground Planes

Each output driver of these devices is capable of 2-A peak currents. Careful layout is essential for correct operation of the chip. A ground plane must be employed. A unique section of the ground plane must be designated for high di/dt currents associated with the output stages. This point is the power ground to which the PGND pin is connected. Power ground can be separated from the rest of the ground plane and connected at a single point, although this is not necessary if the high di/dt paths are well understood and accounted for. VCC must be bypassed directly to power ground with a good high frequency capacitor. The sources of the power MOSFET must connect to power ground as must the return connection for input power to the system and the bulk input capacitor. The output must be clamped with a high current Schottky diode to both VCC and PGND. Nothing else should be connected to power ground.

VREF must be bypassed directly to the signal portion of the ground plane with a good high frequency capacitor. TI recommends low ESR/ESL ceramic 1-mF capacitors for both VCC and VREF. All analog circuitry must likewise be bypassed to the signal ground plane. See Figure 25.

11.2 Layout Example

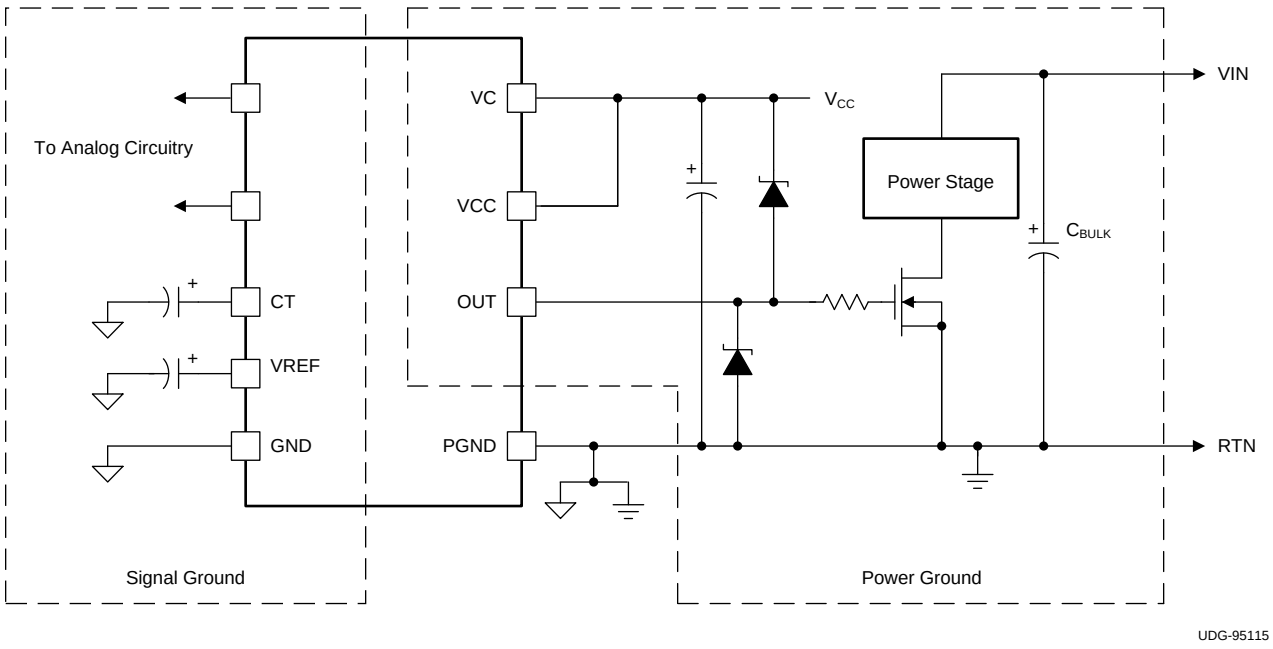

Figure 25. Ground Planes Diagram

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- *Unitrode Application Note U-93*, SLUA075.
- *Unitrode Application Note U-97*, SLUA101.
- *Unitrode Application Note U-110*, SLUA053.

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-8768102V2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8768102V2A UC1825AL QMLV
5962-8768102V2A.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8768102V2A UC1825AL QMLV
5962-8768102VEA	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8768102VEA UC1825AJQMLV
5962-8768102VEA.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8768102VEA UC1825AJQMLV
5962-8768105VEA	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8768105VEA UC1825AJ-SP
5962-8768105VEA.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8768105VEA UC1825AJ-SP
5962P8768105VEA	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962P8768105VEA UC1825AJ-SP
5962P8768105VEA.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962P8768105VEA UC1825AJ-SP
5962P8768105VYC	Active	Production	CFP (HKT) | 16	25 | TUBE	No	NIAU	N/A for Pkg Type	-55 to 125	5962P8768105VYC UC1825AHKT-SP
5962P8768105VYC.A	Active	Production	CFP (HKT) | 16	25 | TUBE	No	NIAU	N/A for Pkg Type	-55 to 125	5962P8768105VYC UC1825AHKT-SP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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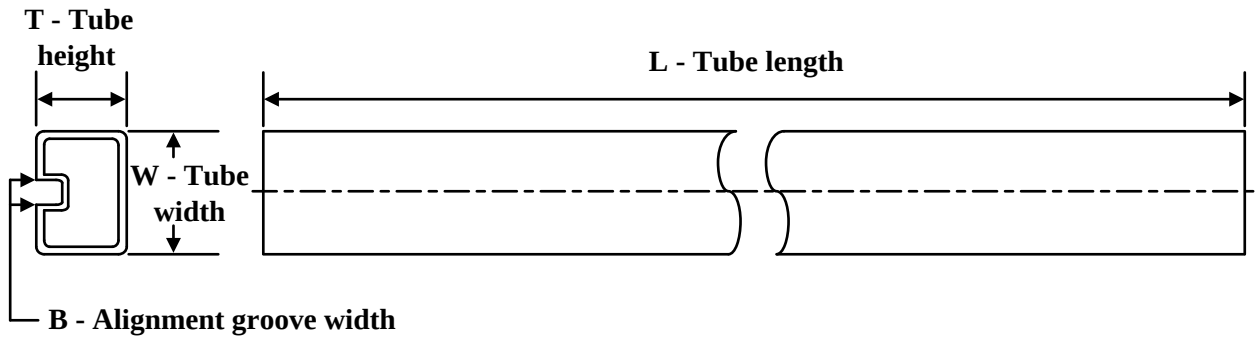
OTHER QUALIFIED VERSIONS OF UC1825A-SP :

- Catalog : UC1825A

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-8768102V2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-8768102V2A.A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962P8768105VYC	HKT	CFP (HSL)	16	25	506.98	26.16	6220	NA
5962P8768105VYC.A	HKT	CFP (HSL)	16	25	506.98	26.16	6220	NA

GENERIC PACKAGE VIEW

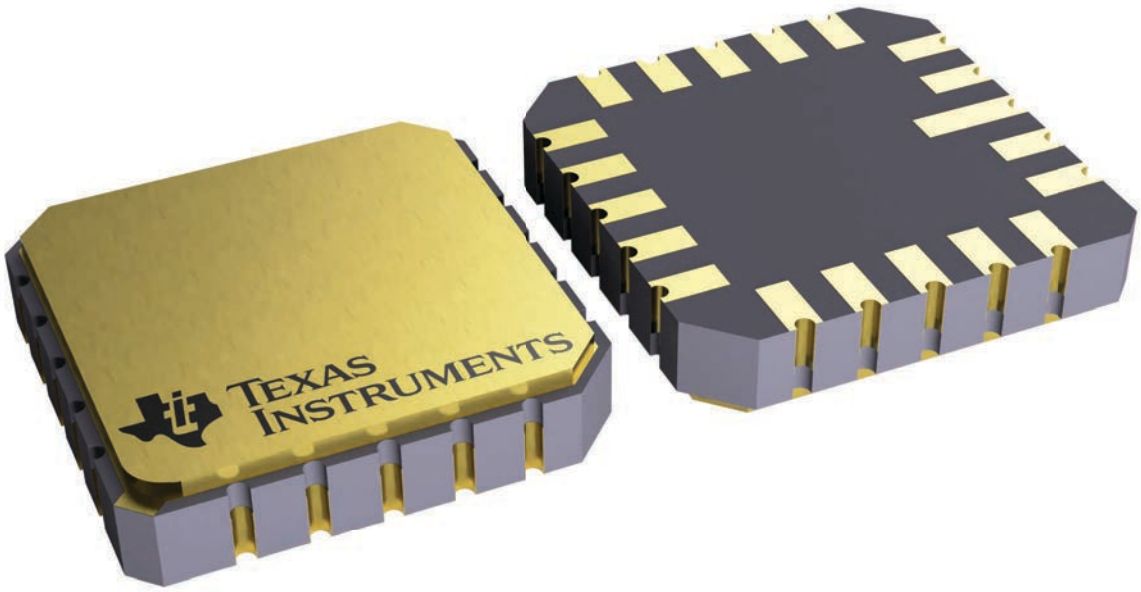
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

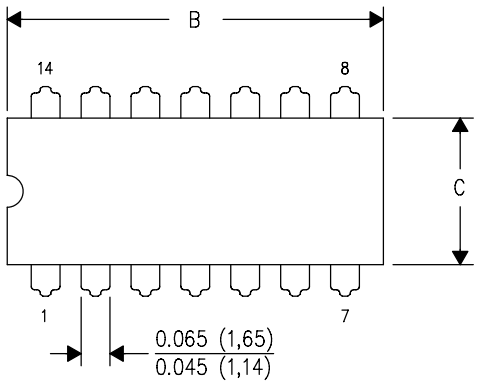


4229370VA\

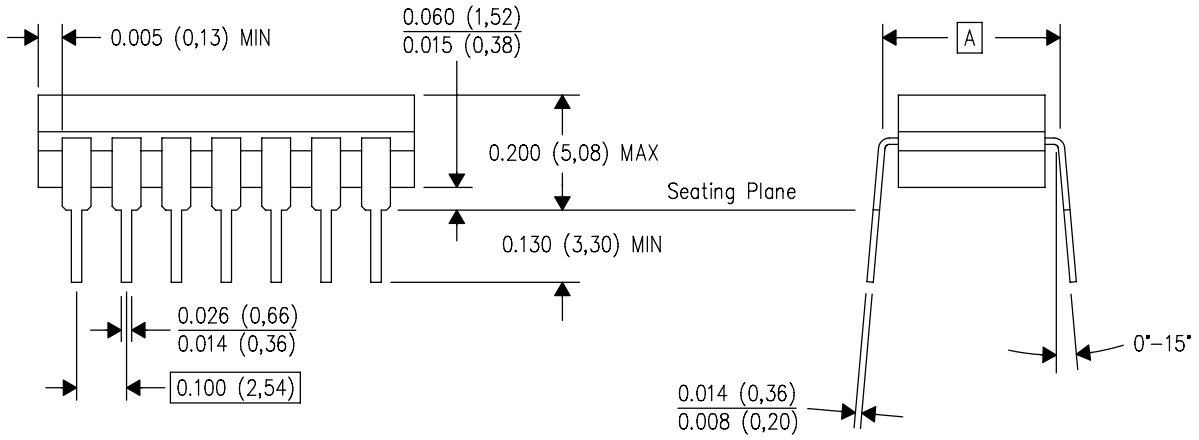
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

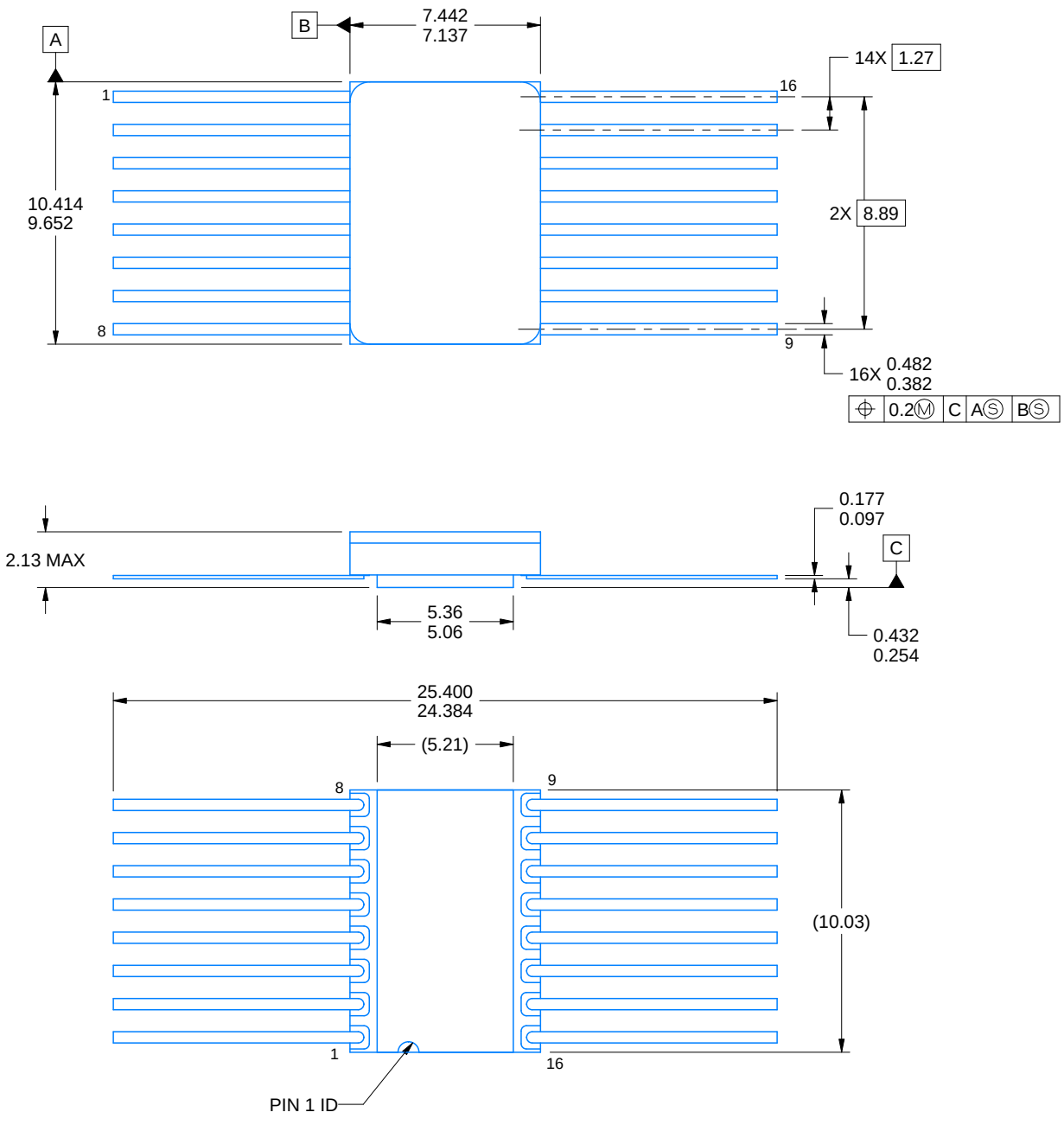
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

PACKAGE OUTLINE

HKT0016A

CFP - 2.13 mm max height

CERAMIC DUAL FLATPACK



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a metal lid. Lid and cavity are electrically isolated
4. The terminals are gold plated.
5. Falls within MIL-STD-1835 CDFP-F11A.

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