# UC1856-SP Improved Current-Mode PWM Controller

## 1 Features

- Pin-for-Pin Compatible With the UC1846
- 65-ns Typical Delay From Shutdown to Outputs, and 50-ns Typical Delay From SYNC to Outputs
- Improved Current-Sense Amplifier With Reduced Noise Sensitivity
- Differential Current Sense with 3-V Common-Mode Range
- Trimmed-Oscillator Discharge Current for Accurate Deadband Control
- Accurate 1-V Shutdown Threshold
- High-Current Dual Totem-Pole Outputs (1.5-A peak)
- TTL Compatible Oscillator SYNC Pin Thresholds
- 4-kV ESD Protection

## 2 Applications

- DC-DC Converters
- Supports Various Topologies:
  - Push-Pull, Forward, Half-Bridge, Full Bridge
- Available in Military Temperature range (-55°C to 125°C)

## 3 Description

The UC1856 is a high-performance version of the popular UC1846 series of current-mode controllers, and is intended for both design upgrades and new applications where speed and accuracy are important. All input-to-output delays have been minimized, and the current sense output is slew-rate limited to reduce noise sensitivity. Fast 1.5-A peak output stages have been added to allow rapid switching of power FETs.

A low-impedance TTL-compatible sync output has been implemented with a TRI-STATE function when used as a sync input.

Internal-chip grounding has been improved to minimize internal noise caused when driving large capacitive loads. This improvement, in conjunction with the improved differential current-sense amplifier, results in enhanced noise immunity.

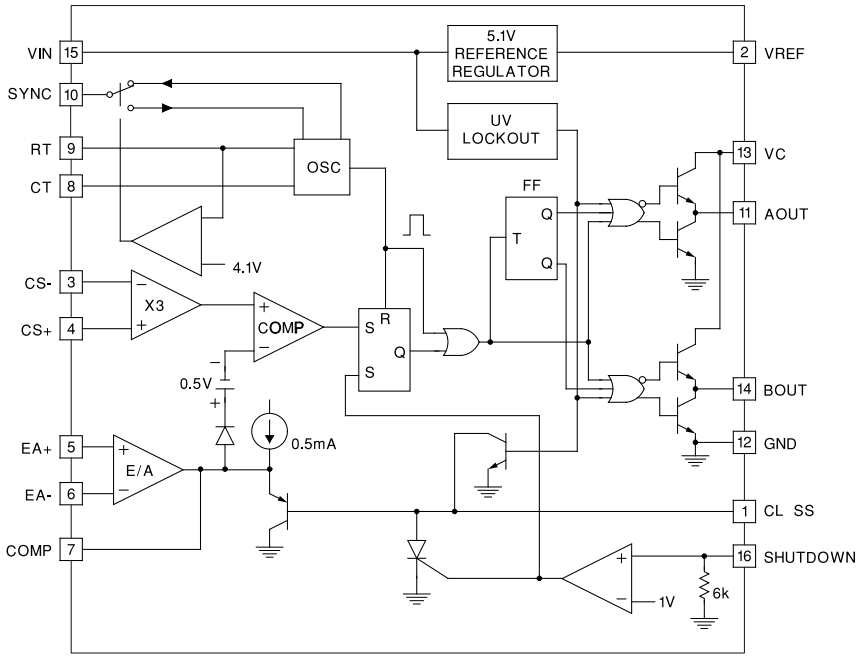
Other features include a trimmed oscillator current (8%) for accurate frequency and dead-time control; a 1-V 5% shutdown threshold; and 4-kV minimum electrostatic discharge (ESD) protection on all pins.

**Device Information**[1]

| DEVICE NAME | PACKAGE | BODY SIZE |
|---|---|---|
| UC1856-SP | CDIP (16) | 20.57 mm x 7.37 mm |
| | CFP (16) | 10.16 mm x 7.1 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

**Block Diagram**




An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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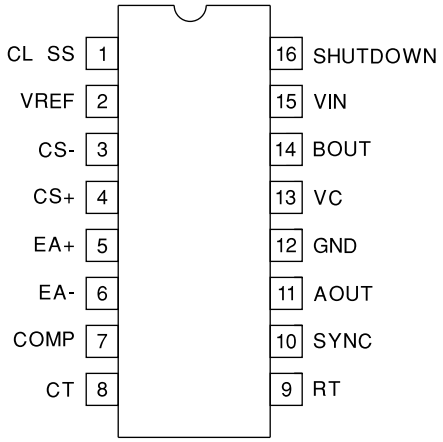
## 4 Revision History

| DATE | REVISION | NOTES |
|---|---|---|
| April 2014 | * | Initial release |


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# 5 Pin Configuration and Functions

**16-Pin**
**J and HKT Packages**
**(Top View)**




**Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| CL SS | 1 | I | Current limit/Soft start |
| VREF | 2 | O | 5.1V internally generated reference |
| CS- | 3 | I | Inverting input of current sense operational amplifier |
| CS+ | 4 | I | Non-Inverting input of current sense operational amplifier |
| EA+ | 5 | I | Non-Inverting input of error amplifier |
| EA- | 6 | I | Inverting input of error amplifier |
| COMP | 7 | O | Output of error amplifier |
| CT | 8 | I | Timing capacitance. Capacitor connected from CT to ground is charged via current established by RT pin via current mirror. Output Pulse dead time is determined by the size of the capacitor during capacitor discharge time. |
| RT | 9 | I | Determines oscillator frequency. VREF sources thru RT to create a current which is mirrored to CT pin. |
| SYNC | 10 | I/O | Sync pin is an output under normal operation when RT is above 4.1V Sync output high. Sync pin is an input when RT pin is high and CT pin tied low. |
| AOUT | 11 | O | Output driver (source/sink) |
| GND | 12 | - | Ground connection |
| VC | 13 | I | Gate drive collector supply voltage. Decouple with capacitor. |
| BOUT | 14 | O | Output driver (source/sink) |
| VIN | 15 | I | Input voltage decouple with capacitor |
| SHUTDOWN | 16 | I | Shutdown threshold 1V. Voltage above threshold latches off oscillator. |

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# 6 Specifications

## 6.1 Absolute Maximum Ratings(1)(2)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage | | | 40 | V |
| Collector supply voltage | | | 40 | V |
| Current sense inputs | | –0.3 | 3 | V |
| Error amplifier inputs | | –0.3 | $V_{IN}$ | V |
| Shutdown input | | –0.3 | 10 | V |
| Error-amplifier output current | | | –5 | mA |
| Output current, source or sink | DC | | 0.5 | A |
| | Pulse (0.5 µs) | | 2 | |
| Oscillator Charging current | | | 5 | mA |
| Soft-start sink current | | | 50 | mA |
| SYNC output current | | | ±10 | mA |
| Junction temperature | | –55 | 150 | °C |
| Lead temperature (Soldering, 10 sec.) | | | 300 | °C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to Ground. Currents are positive into, negative out of the specified pin. Consult packaging section of databook for thermal/imitations and considerations of package.

## 6.2 Handling Ratings

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $T_{stg}$ | Storage temperature range | -65 | 150 | °C |

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $T_J$ | Operating junction temperature | -55 | | 125 | °C |

## 6.4 Thermal Information(1)

| THERMAL METRIC(2) | | UC1856-SP | UNIT |
|---|---|---|---|
| | | 16 PIN | |
| $R_{\theta JC(bottom)}$ | J package | 7.3 | °C/W |
| | HKT package | 2.9 | |

(1) HKT: Computational fluid dynamics (CFD) model of 16 pin HKT package to Mil Std 883 Method 1012.1 standard. 16/J: Curve based on CFD models correlated to available physical measurement data points. Reference: http://www.sh.sc.ti.com/process-packaging/pkgchar/Tjc_by_die_size.htm
(2) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.


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## 6.5 Electrical Characteristics

Unless otherwise stated, these specifications apply for $T_A$ –55°C to +125°C, $V_{IN}$ = 15 V, $R_T$ = 10 kΩ, $C_T$ = 1 nF, $T_A$ = $T_J$.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **REFERENCE SECTION** | | | | | |
| Output voltage | $T_J$ = 25°C, $I_O$ = 1 mA | 5.05 | 5.1 | 5.15 | V |
| Line regulation | $V_{IN}$ = 8 to 40 V | | | 20 | mV |
| Load regulation | $I_O$ = –1 mA to –10 mA | | | 15 | mV |
| Total output variation | Line, load, and temperature | 5 | | 5.2 | V |
| Output noise voltage | 10 Hz < f < 10 kHz, $T_J$ = 25°C | | 50 | | µV |
| Long-term stability | $T_J$ = 125°C, 1000 Hrs (1) | | 5 | 25 | mV |
| Short-circuit current | $V_{REF}$ = 0 V | –25 | –45 | –65 | mA |
| **OSCILLATOR SECTION** | | | | | |
| Initial accuracy | $T_J$ = 25°C | 180 | 200 | 220 | kHz |
| | Over operating range | 170 | | 230 | |
| Voltage stability | $V_{IN}$ = 8 to 40 V | | | 2% | |
| Discharge current | $T_J$ = 25°C, $V_{CT}$ = 2 V | 7.5 | 8 | 8.8 | mA |
| | Over operating range, $V_{CT}$ = 2 V | 6.7 | 8 | 8.8 | |
| Sync output high level | $I_O$ = –1 mA | 2.4 | 3.6 | | V |
| Sync output low level | $I_O$ = 1 mA | | 0.2 | 0.4 | V |
| Sync input high level | $C_T$ = 0 V, $R_T$ = $V_{REF}$ | 2 | 1.5 | | V |
| Sync input low level | $C_T$ = 0 V, $R_T$ = $V_{REF}$ | | 1.5 | 0.8 | V |
| Sync input current | $C_T$ = 0 V, $R_T$ = $V_{REF}$, $V_{SYNC}$ = 5 V | | 1 | 10 | µA |
| Sync delay to outputs | $C_T$ = 0 V, $R_T$ = $V_{REF}$, $V_{SYNC}$ = 0.8 to 2 V | | 50 | 100 | ns |
| **ERROR AMPLIFIER SECTION** | | | | | |
| Input offset voltage | $V_{CM}$ = 2 V | | | 5 | mV |
| Input bias current | | | | –1 | µA |
| Input offset current | | | | 500 | nA |
| Common mode range | $V_{IN}$ = 8 V to 40 V | 0 | | $V_{IN}$-2 | V |
| Open loop gain | $V_O$ = 1.2 V to 3 V | 80 | 100 | | dB |
| Unity gain bandwidth | $T_J$ = 25°C | 1 | 1.5 | | MHz |
| CMRR | $V_{CM}$ = 0 V to 38 V, $V_{IN}$ = 40 V | 75 | 100 | | dB |
| PSRR | $V_{IN}$ = 8 V to 40 V | 80 | 100 | | dB |
| Output sink current | $V_{ID}$ = –15 mV, $V_{COMP}$ = 1.2 V | 5 | 10 | | mA |
| Output source current | $V_{ID}$ = 15 mV, $V_{COMP}$ = 2.5 V | –0.4 | –0.5 | | mA |
| Output high level | $V_{ID}$ = 50 mV, $R_L$ (COMP) = 15 kΩ | 4.3 | 4.6 | 4.9 | V |
| Output low level | $V_{ID}$ = –50 mV, $R_L$ (COMP) = 15 kΩ | | 0.7 | 1 | V |
| **CURRENT SENSE AMPLIFIER SECTION** | | | | | |
| Amplifier gain | $V_{CS}$– = 0 V, CL SS Open (2)(3) | 2.5 | 2.75 | 3 | V/V |
| Maximum differential-input signal ($V_{CS}$+ – $V_{CS}$–) | CL SS Open (2), $R_L$ (COMP) = 15 kΩ | 1.1 | 1.2 | | V |
| Input offset voltage | $V_{CL\ SS}$ = 0.5 V, COMP Open (3) | | 5 | 35 | mV |
| CMRR | $V_{CM}$ = 0 V to 3 V | 60 | | | dB |
| PSRR | $V_{IN}$ = 8 V to 40 V | 60 | | | dB |
| Input bias current | $V_{CL\ SS}$ = 0.5 V, COMP Open (2) | –1 | | 1 | µA |
| Input offset current | $V_{CL\ SS}$ = 0.5 V, COMP Open (2) | –1 | | 1 | µA |
| Input common-mode range | | 0 | | 3 | V |
| Delay to outputs | $V_{EA}$+ = VREF, EA– = 0 V<br>CS+ – CS– = 0 V to 1.5 V | | 120 | 250 | ns |

(1) This parameter, although ensured over the recommended operating conditions, is not 100% tested in production.
(2) Parameter measured at trip point of latch with $V_{EA}$+ = VREF, $V_{EA}$– = 0 V.
(3) Amplifier gain defined as:

$$G = \frac{\Delta V_{COMP}}{\Delta V_{CS+}}; \qquad \Delta V_{CS-} = 0 \text{ to } 1\ V$$

## Electrical Characteristics (continued)

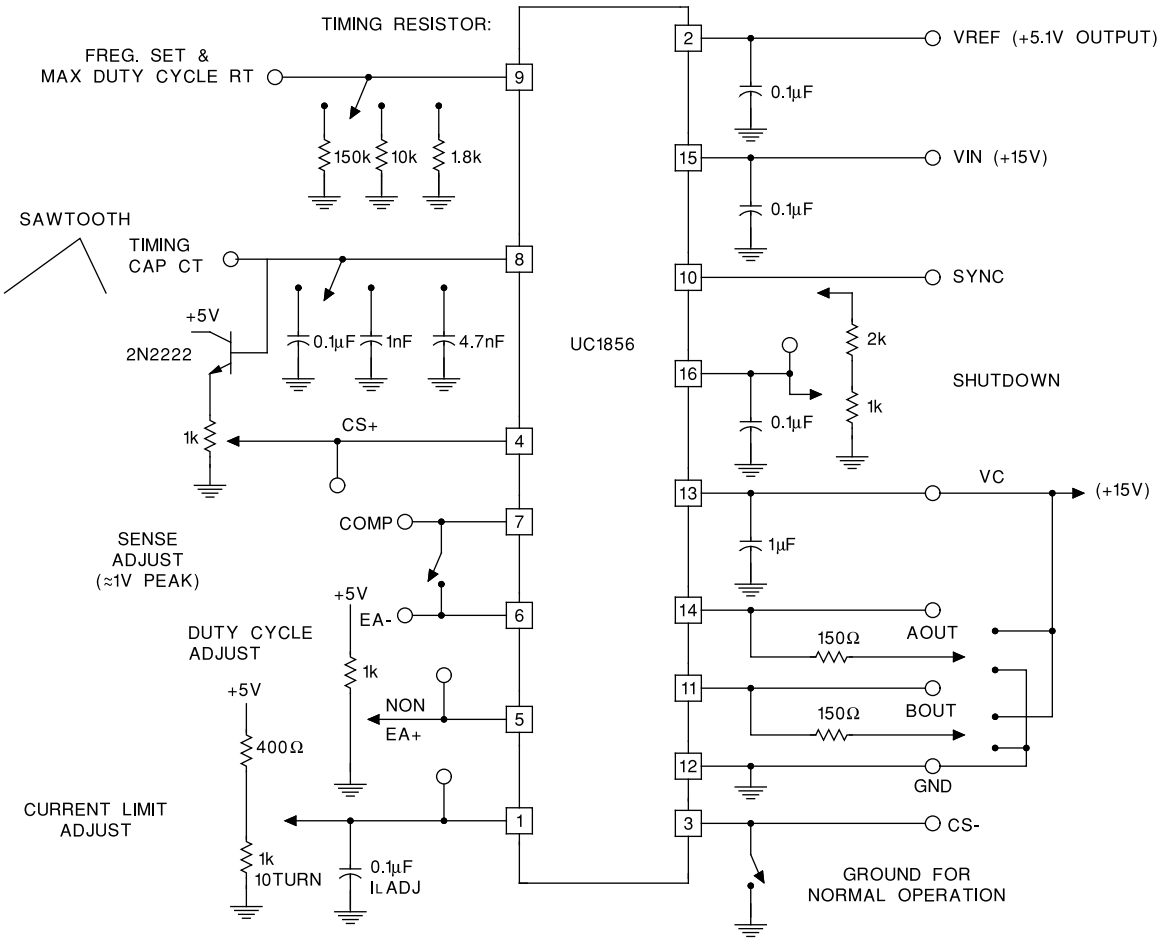
Unless otherwise stated, these specifications apply for $T_A$ –55°C to +125°C, $V_{IN}$ = 15 V, $R_T$ = 10 kΩ, $C_T$ = 1 nF, $T_A$ = $T_J$.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **CURRENT LIMIT ADJUST SECTION** | | | | | |
| Current limit offset | $V_{CS}$– = 0 V , $V_{CS}$+ = 0V, COMP = Open(4) | 0.43 | 0.5 | 0.57 | V |
| Input bias current | | | –10 | –30 | µA |
| **SHUTDOWN PIN SECTION** | | | | | |
| Threshold voltage | | 0.95 | 1 | 1.05 | V |
| Input voltage range | | 0 | | 5 | V |
| Minimum latching current ($I_{CL\ SS}$) | See (5) | 3 | 1.5 | | mA |
| Maximum non-latching current ($I_{CL\ SS}$) | See (6) | | 1.5 | 0.8 | mA |
| Delay to outputs | $V_{SHUTDOWN}$ = 0 V to 1 .3 V | | 65 | 110 | ns |
| **OUTPUT SECTION** | | | | | |
| Collector-emitter voltage | | 40 | | | V |
| Off-state bias current | VC = 40 V | | | 250 | µA |
| Output low level | $I_{OUT}$ = 20 mA | | 0.1 | 0.5 | V |
| | $I_{OUT}$ = 200 mA | | 0.5 | 2.6 | |
| Output high level | $I_{OUT}$ = –20 mA | 12.5 | 13.2 | | V |
| | $I_{OUT}$ = –200 mA | 12 | 13.1 | | |
| Rise time | C1 = 1 nF | | 40 | 80 | ns |
| Fall time | C1 = 1 nF | | 40 | 80 | ns |
| UVLO low saturation | $V_{IN}$ = 0 V, $I_{OUT}$ = 20 mA | | 0.8 | 1.5 | V |
| **PWM SECTION** | | | | | |
| Maximum duty cycle | | 45% | 47% | 50% | |
| Minimum duty cycle | | | | 0% | |
| **UNDERVOLTAGE LOCKOUT SECTION** | | | | | |
| Startup threshold | | | 7.7 | 8 | V |
| Threshold hysterisis | | | 0.7 | | V |
| **TOTAL STANDBY CURRENT** | | | | | |
| Supply current | | | 18 | 23 | mA |

(4) Parameter measured at trip point of latch with $V_{EA}$+ = VREF, $V_{EA}$– = 0 V.
(5) Current into CL SS ensued to latch circuit into shutdown state.
(6) Current into CL SS ensured not to latch circuit into shutdown state.


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# 7 Parameter Measurement Information




Bypass caps should be low ESR and ESL type.
Short E/A– and comp for unity gain testing.
**The use of a ground plane is highly recommended.**

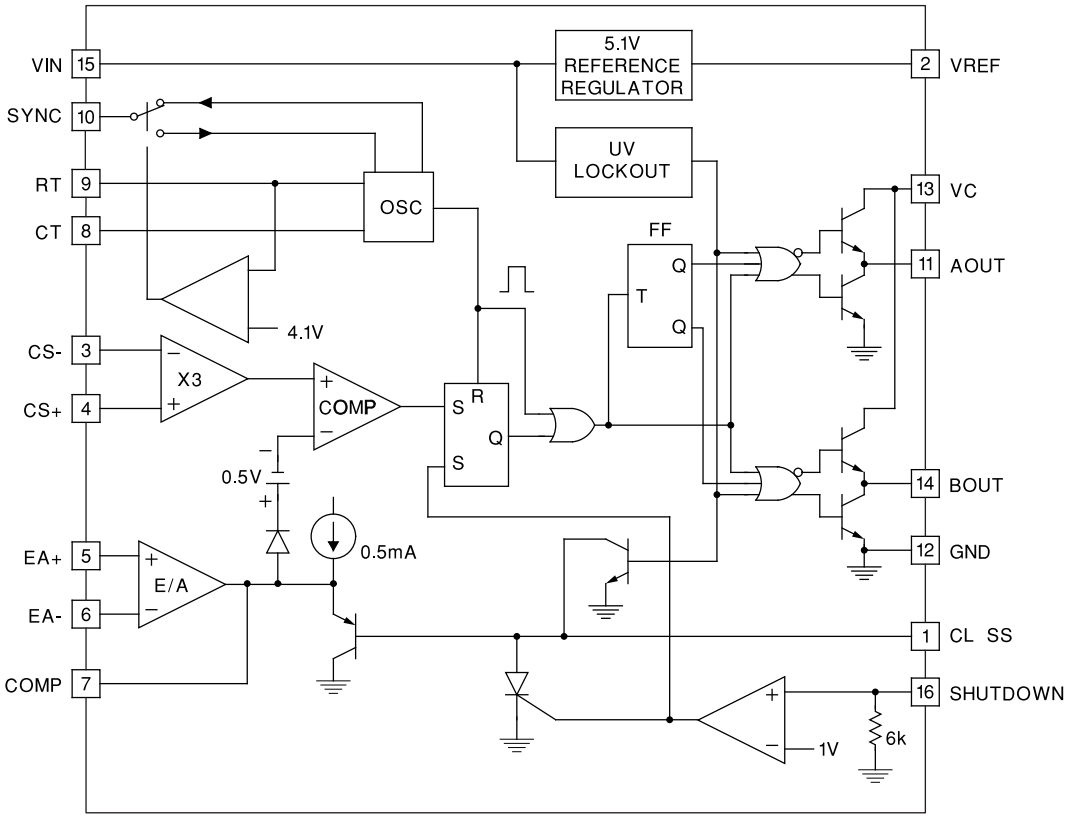
**Figure 1. UC1856 Open-Loop Test Circuit**

# 8 Detailed Description

## 8.1 Overview

The UC1856 is a high-performance version of the popular UC1846 series of current-mode controllers, and is intended for both design upgrades and new applications where speed and accuracy are important. All input-to-output delays have been minimized, and the current sense output is slew-rate limited to reduce noise sensitivity. Fast 1.5-A peak output stages have been added to allow rapid switching of power FETs.

## 8.2 Functional Block Diagram




## 8.3 Feature Description

UC1856 is a current mode controller, used to support various topologies such as forward, flyback, half-bridge, full bridge, push-pull configurations.

Current mode control is a two-loop system. The switching power supply inductor is hidden within the inner current control loop. This simplifies the design of the outer voltage control loop and improves power supply performance in many ways, including better dynamics. The objective of this inner loop is to control the state-space averaged inductor current, but in practice the instantaneous peak inductor current is the basis for control (switch current - equal to inductor current during the on time - is often sensed). If the inductor ripple current is small, peak inductor current control is nearly equivalent to average inductor current control.

The peak method of inductor current control functions by comparing the upslope of inductor current (or switch current) to a current program level set by the outer loop. The comparator turns the power switch off when the instantaneous current reaches the desired level. The current ramp is usually quite small compared to the programming level, especially when $V_{IN}$ is low. As a result, this method is extremely susceptible to noise. A noise spike is generated each time the switch turns on. A fraction of a volt coupled into the control circuit can cause it to turn off immediately, resulting in a sub-harmonic operating mode with much greater ripple. Circuit layout and bypassing are critically important to successful operation.


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## Feature Description (continued)

The peak current mode control method is inherently unstable at duty ratios exceeding 0.5, resulting in sub-harmonic oscillation. A compensating ramp (with slope equal to the inductor current downslope) is usually applied to the comparator input to eliminate this instability. A slope compensation must be added to the sensed current waveform or subtracted from the control voltage to ensure stability above a 50% duty cycle. A compensating ramp (with slope equal to the inductor current downslope) is usually applied to the comparator input to eliminate this instability.

The pulse width modulator (PWM) of UC1856-SP is limited to a maximum duty cycle of 50%, thus it can be used in topologies such as push-pull, half bridge, full bridge, forward, flyback configurations. Limiting PWM to 50% duty cycle ensures that for isolated or transformer based topologies. The transformer is allowed to reset and prevent saturation of the transformer core.

Pulse-by-pulse symmetry correction (flux balancing) is inherent to current mode controllers and essential for the push-pull topology to prevent core saturation.

Current limit control design has numerous advantages:

1. Current mode control provided peak switch current limiting – pulse by pulse current limit.
2. Control loop is simplified as one pole due to output inductor is pushed to higher frequency , thus a two pole system turns into two real poles. Thus system reduces to a first order system thus simplifies the control.
3. Multiple converter can be paralleled and allows equal current sharing amount the various converters.
4. Inherently provides for input voltage feed-forward as any perturbation in the input voltage will be reflected in the switch or inductor current. Since switch or inductor current is a direct control input, thus this perturbation is very rapidly corrected.
5. The error amplifier output (outer control loop) defines the level at which the primary current (inner loop) will regulate the pulse width, and output voltage.

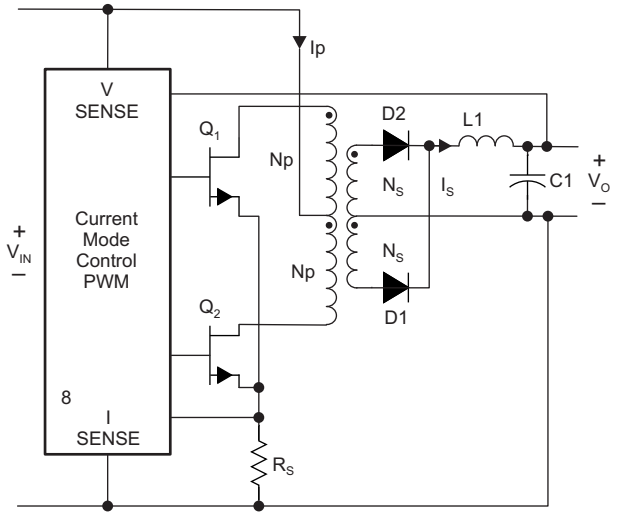



**Figure 2. Push-Pull Converter Using Current Mode Control**

### 8.3.1 Reference

As highlighted in the Functional Block Diagram, UC1856-SP incorporates a 5.1-V internal reference regulator with ±10% set point variation over temperature.

### 8.3.2 Oscillator

Figure 7 highlights the oscillator circuit. Connecting a resistor RT from pin 9 to ground establishes a current, which is mirrored to pin 8 and charges the capacitor connected from pin 8 to ground. Maximum on-time corresponds to the maximum charging time of the timing capacitor. Oscillator frequency can be determined by Equation 5.

Off-time corresponds to capacitor discharge time establishes the converter dead time between the pulses according to Equation 4. Internal 8-mA current sink discharges the CT pin capacitor.

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## Feature Description (continued)

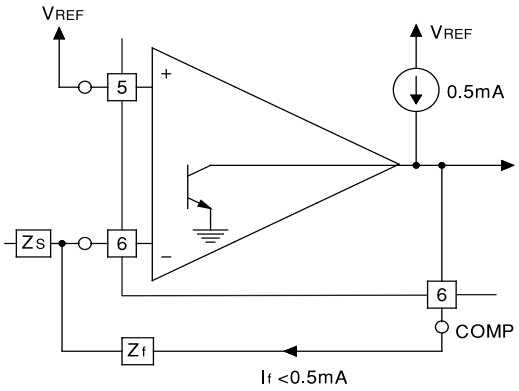
### 8.3.3 Slope Compensation

For duty cycle above 50% slope compensating can be implemented by using a buffer (i.e. 2N2222) and connecting base to timing capacitor pin 8 , collector to VREF (5 V), a resistor in series with emitter connected to (pin 4) CS+ of differential current sense amplifier. Injecting a downslope proportional to the sawtooth into current sense amplifier.

As with any bipolar PWM IC, outputs should be protected from negatively biasing the substrate. This is typically done by using Schottky diodes from ground to each output. Failure to do this could cause spurious interruption and restart of the oscillator, dropping of output pulses and a significant increase in propagation delays.

### 8.3.4 Error Amplifier

UC1856-SP incorporates an error amplifier with typical open loop gain of 100 db and gain bandwidth of 1.5 MHz. With Source and sink capability of 10 mA and 0.5 mA respectively.




Error amplifier sources up to 0.5 mA.

**Figure 3. Error Amplifier Output Configuration**

### 8.3.5 Current Sense Amplifier

UC1856-SP incorporates a differential current sense amplifier which can eliminate ground loop problems and increase noise immunity. An R-C snubber can also be implemented thus helping in blanking the peak current spike when the switch is turned on. The input of the current sense amplifier is slew rate limited allowing lower values of filter capacitors to be used to eliminate leading edge noise.

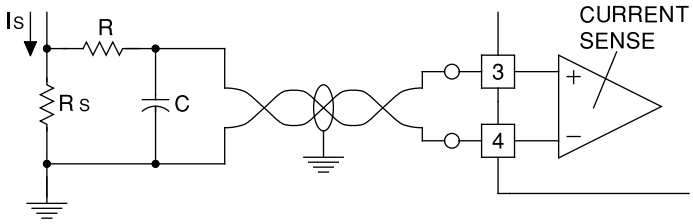



**Figure 4. Current-Sense Amplifier Connections**

In some applications, a small RC filter is required to reduce switch transients. Differential input allows remote noise sensing.

### 8.3.6 Current Limit

Over current trip point is determined by Equation 1. Differential current sense amplifier has a gain of three, as shown in Figure 5.


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## Feature Description (continued)

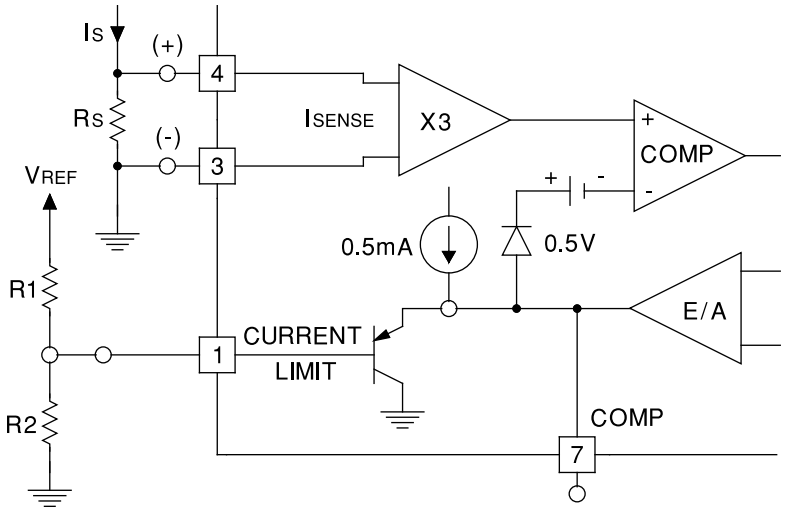



**Figure 5. Pulse-By-Pulse Current Limiting**

Referring to Figure 5, Equation 1 determines the peak current, Is.

$$Is = \frac{\left(\frac{R2V_{REF}}{R1+R2}\right) - 0.5}{3R_S} \quad (1)$$

### 8.3.7 Shutdown

UC1856-SP incorporates a shutdown pin (pin16). Shutdown threshold voltage is 1 V. Exceeding the shutdown threshold voltage causes the device to shutdown.

- If current into ICL_SS $V_{REF}$/R1 > 3-mA SCR holding current (minimum latch current), then the device latches off. Power recycle is required to un-latch the device.
- If $V_{REF}$/R1 < 0.8 mA, that is ICL_SS < 0.8 A, then this ensures that the circuit does not latch in a shutdown state.

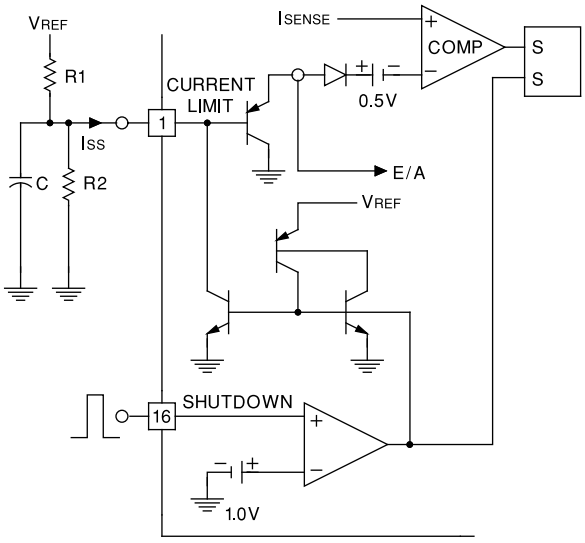



**Figure 6. Shutdown Latch**

## Feature Description (continued)

Referring to Figure 10, if

$$\frac{V_{REF}}{R1} < 0.8\,mA \quad (2)$$

the shutdown latch commutates when ISS = 0.8 mA and a restart cycle initiates.

Referring to Figure 11, if

$$\frac{V_{REF}}{R1} > 3\,mA \quad (3)$$

the device latches off until power is recycled.

### 8.3.8 Output Section

UC1856-SP incorporates high current dual totem pole output stage capable of sourcing/sinking 1.5 A peak current for fast switching of power MOSFETs and limited to 0.5 A dc current.

### 8.3.9 Undervoltage Lockout

Minimum input voltage for converter is 8 V or higher, with typical value being 7.7 V. At input voltages below the actual UVLO voltage, the devices will not operate.

### 8.3.10 Soft-Start

Connecting a capacitor from CL/SS pin 1 to ground which is charged by 0.5-mA internal current source will determine the soft-start time. If over current is also implemented as shown in Figure 5, then SS charge time will be determined by charging SS capacitor by 0.5-mA current as well as current contributed by R1 resistor in charging the SS capacitor.

## 8.4 Device Functional Modes

### 8.4.1 Operation with $V_{IN}$ < 8 V (Minimum $V_{IN}$)

The devices operate with input voltages above 8 V. The maximum UVLO voltage is 8 V and will operate at input voltages above 8 V. The typical UVLO voltage is 7.7 V and the devices may operate at input voltages above that point. The devices also may operate at lower input voltages, the minimum UVLO voltage is not specified. At input voltages below the actual UVLO voltage, the devices will not operate.

### 8.4.2 Synchronization

The synchronization pin (pin10) can be configured as an output for master/slave application. When the converter is configured as a master or standalone converter, SYNC (pin 10) is an output. As highlighted in the functional block diagram, voltage at RT (pin 9) is greater than 4.1-V internal threshold.

When using the part in slave configuration, SYNC pin becomes an input. Typical example of parallel operation with master/slave configuration is shown in Figure 12. Slave unit CT (pin 8) is grounded and RT pin is connected to VREF (pin 2).

When using the part in slave configuration, SYNC pin becomes an input. Typical example of parallel operation with master/slave configuration is shown in Figure 12. Slave unit CT (pin 8) is grounded and RT pin is connected to VREF (pin 2). Under parallel configuration two or more units can be paralleled, with COMP pins tied together each will share current equally.

### 8.4.3 Parallel Operation

Under parallel configuration two or more units can be paralleled, with COMP pins tied together each will share current equally.

Figure 12 highlights typical parallel operation configuration.


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# 9 Applications and Implementation

## 9.1 Application Information

UC1856-SP can be used as a controller to design various topologies such as push-pull, half-bridge, full bridge, and flyback.

The following sections highlight the topologies for oscillators, error amplifiers, and parallel configurations (paralleling two EVMS).

## 9.2 Typical Applications

### 9.2.1 Oscillator Circuit

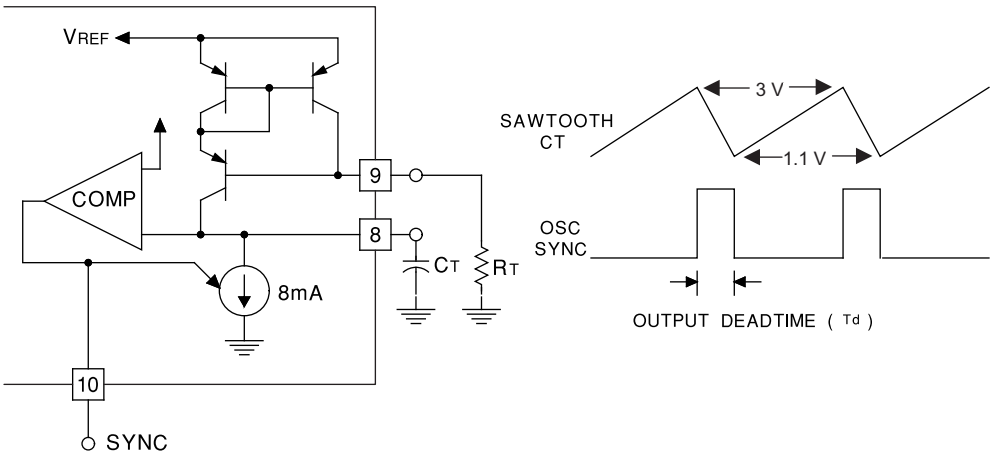



**Figure 7. Oscillator Circuit**

Referring to Figure 7, the size of the external capacitor, $C_T$, determines output dead time, according to Equation 4.

$$Td = \frac{2C_T}{8mA - \frac{3.6}{R_T}} \quad (4)$$

For large values of $R_T$: Td = 250 $C_T$.

Oscillator frequency is approximated by Equation 5.

$$f_T = \frac{2}{R_T C_T} \quad (5)$$

#### *9.2.1.1 Design Requirements*

**Table 1. Design Parameters**

| DESIGN PARAMETER | EXAMPLE VALUE | REFERENCE |
|---|---|---|
| Oscillator frequency = 200 kHz | $R_T$ = 10 kΩ, $C_T$ = 1 nF | Equation 4, Figure 7 |
| Dead time, Td = 75.8 ns | $R_T$ = 10 kΩ $C_T$ = 1 nF | Equation 5, Figure 7 |

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### 9.2.1.2 Detailed Design Procedure

#### 9.2.1.2.1 Input Capacitor Selection

Load current, duty cycle, and switching frequency are several factors which determine the magnitude of the input ripple voltage. Without the input capacitor, the pulsating current of Q1 would need to be completely supplied by the host source, VIN, which commonly does not have sufficiently low output impedance. Thus there would be substantial noise on the host dc voltage source and an increase in the conducted EMI on the board. The input capacitor, CIN, effectively filters the input current so the current from the host dc source is approximately an average current.

The input ripple voltage amplitude is directly proportional to the output load current. The maximum input ripple amplitude occurs at maximum output load. Also, the amplitude of the voltage ripple varies with the duty cycle of the converter.

UC1856-SP requires a high quality ceramic, type X5R or X7R, input decoupling capacitor of at least 47 µF of effective capacitance on the VIN input voltage pins. In some applications additional bulk capacitance may also be required for the VIN input. The effective capacitance includes any DC bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the UC1856-SP. The input ripple current can be calculated using Equation 6.

$$\text{Icirms} = \text{Iout} \times \sqrt{\frac{\text{Vout}}{\text{Vinmin}} \times \frac{(\text{Vinmin} - \text{Vout})}{\text{Vinmin}}} \tag{6}$$

The value of a ceramic capacitor varies significantly over temperature and the amount of DC bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is stable over temperature. X5R and X7R ceramic dielectrics are usually selected for power regulator capacitors because they have a high capacitance to volume ratio and are fairly stable over temperature. The output capacitor must also be selected with the DC bias taken into account. The capacitance value of a capacitor decreases as the DC bias across a capacitor increases.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 7.

$$\Delta\text{Vin} = \frac{\text{Ioutmax} \times 0.25}{\text{Cin} \times \text{fsw}} \tag{7}$$

#### 9.2.1.2.2 Output Capacitor Selection

The output capacitance of a switching regulator is a vital part of the overall feedback system. The energy storage inductor and the output capacitor form a second-order low-pass filter.

In switching power supply power stages, the function of output capacitance is to store energy. The energy is stored in the capacitor's electric field due to the voltage applied. Thus, qualitatively, the function of a capacitor is to attempt to maintain a constant voltage.

The value of output capacitance of a buck power stage is generally selected to limit output voltage ripple to the level required by the specification. Since the ripple current in the output inductor is usually already determined, the series impedance of the capacitor primarily determines the output voltage ripple. The three elements of the capacitor that contribute to its impedance (and output voltage ripple) are equivalent series resistance (ESR), equivalent series inductance (ESL), and capacitance (C). The following gives guidelines for output capacitor selection.

For continuous inductor current mode operation, to determine the amount of capacitance needed as a function of inductor current ripple, $\Delta I_L$, switching frequency, $f_S$, and desired output voltage ripple, $\Delta V_O$, Equation 8 is used assuming all the output voltage ripple is due to the capacitor's capacitance.

$$C \geq \frac{\Delta I_L}{8 \times fs \times \Delta Vo} \tag{8}$$

Where $\Delta I_L$ is the inductor ripple current.


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Each capacitor type is characterized by its impedance and the frequency range over which it is most effective. The frequency at which the impedance reaches its minimum is determined by its ESR and ESL. It is known as the self resonant frequency of the capacitor. The self resonant frequency is considered to be the maximum usable frequency for a capacitor. Above this frequency the impedance of the capacitor begins to rise as the ESL of the capacitor begins to dominate. Note that each capacitor type has a specific frequency band over which it is most effective. Therefore, a capacitor network of multiple capacitor types is more effective in reducing impedance than just one type.

The current slew rate of a regulator is limited by its output filter inductor. When the amount of current required by the load changes, the initial current deficit must be supplied by the output capacitors until the regulator can meet the load demand.

The desired response to a large change in the load current is the first criteria. The output capacitor needs to supply the load with current when the regulator control loop can not supply the current. This happens when Load (ie: memory, processor) has a large and fast increase in current, such as a transition from no load to full load. The regulator typically needs two or more clock cycles for the control loop to see the change in load current, output voltage and adjust the duty cycle to react to the change. The output capacitor must be properly sized to supply the extra current to the Load until the control loop responds to the Load change. The output capacitance must be large enough to supply the difference in current for 2 clock cycles while only allowing a tolerable amount of droop in the output voltage. Equation 9 shows the minimum output capacitance necessary to accomplish this.

$$C_O > \frac{2 \times \Delta I_{out}}{f_{SW} \times \Delta V_{out}} \tag{9}$$

Where ΔIout is the change in output current, $f_{SW}$ is the regulators switching frequency and ΔVout is the allowable change in the output voltage. For this example, the transient load response is specified as a 5% change in Vout for a load step of 1A. For this example, ΔIout = 1.0 A and ΔVout = 0.05 x 3.3 = 0.165 V. Using these numbers gives a minimum capacitance of 25 µF. This value does not take the ESR of the output capacitor into account in the output voltage change. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation.

#### 9.2.1.2.3 Output Inductor Selection

To calculate the value of the output inductor, use Equation 10. Kind is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. The inductor ripple current is filtered by the output capacitor. Therefore, choosing high inductor ripple currents impact the selection of the output capacitor since the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value is at the discretion of the designer; however, Kind is normally from 0.1 to 0.3 for the majority of applications. VinLC refers to the voltage at the input of output LC filter.

$$L1 = \frac{VinLC - Vout}{Io \times Kind} \times \frac{Vout}{VinLC \times f_{SW}} \tag{10}$$

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the peak inductor current.

#### 9.2.1.2.4 Switching Frequency

Initial accuracy of UC1856-SP oscillator frequency is 200 kHz ±15% over the temperature range. Switching frequency selection is a trade-off between the overall design size and efficiency. Operating at lower switching frequency will result in higher efficiency at the expense of larger solution footprint.

Oscillator frequency can be determined as follows:

$$R_T = 10\ k\Omega \tag{11}$$

$$C_T = 1\ nF \tag{12}$$

$$f_T = \frac{2}{R_T \times C_T} \tag{13}$$

$$f_T = 200\ kHz \tag{14}$$

### 9.2.1.3 Application Curves

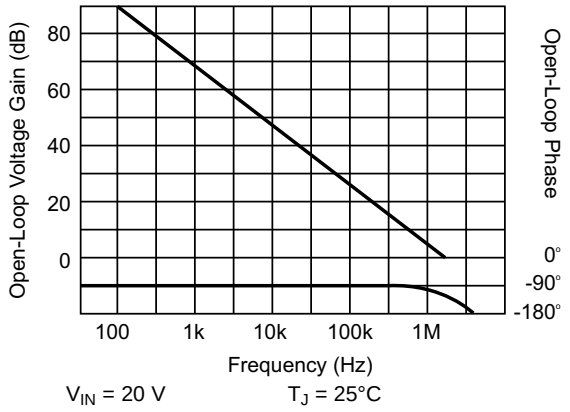



**Figure 8. Error Amplifier Gain and Phase vs Frequency**

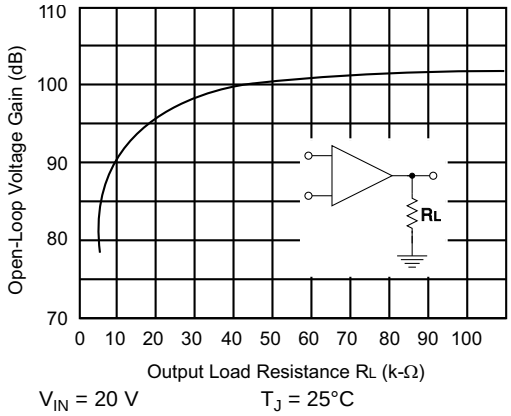



**Figure 9. Error Amplifier Open-Loop D.C. Gain vs Load Resistance**

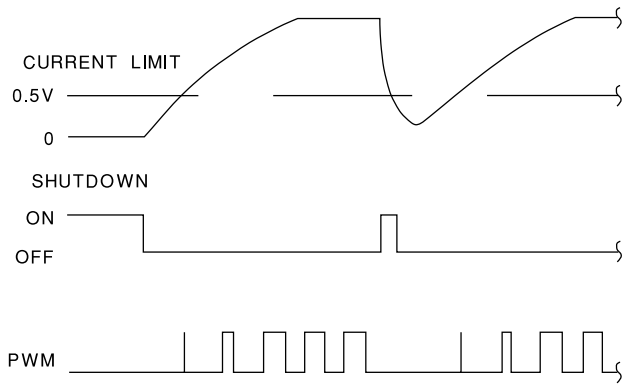



**Figure 10. Shutdown With Auto-Restart**

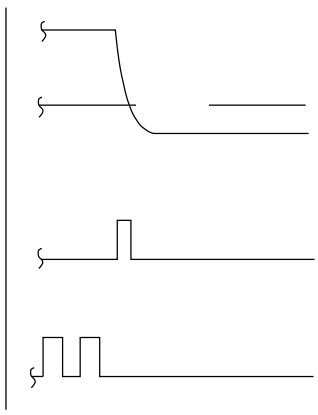
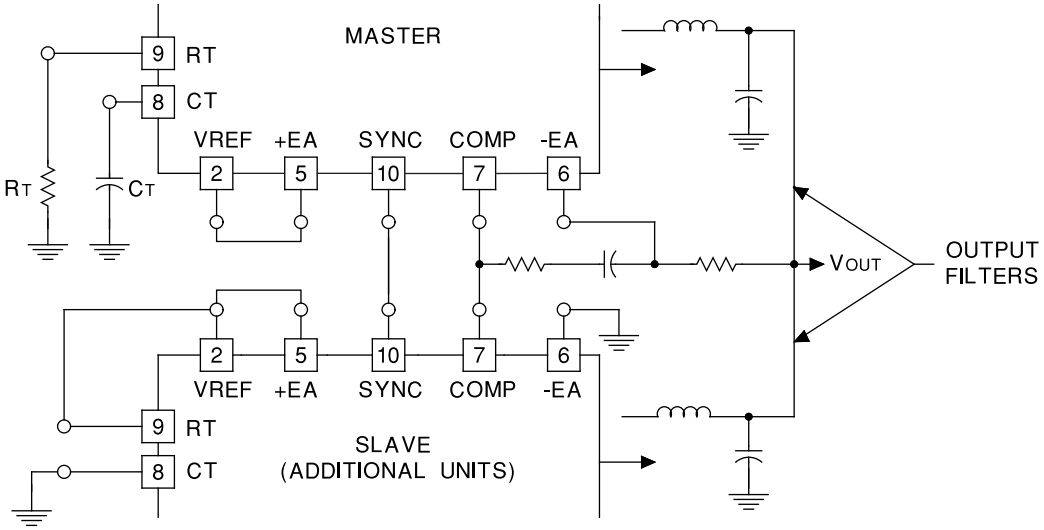


**Figure 11. Shutdown Without Auto-Restart (Latched)**


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### 9.2.2 Parallel Operation




Slaving allows parallel operation of two or more units with equal current sharing.

**Figure 12. Parallel Operation**

#### *9.2.2.1 Design Requirements*

Refer to Design Requirements for the Oscillator Circuit Design Requirements.

#### *9.2.2.2 Detailed Design Procedure*

Refer to Detailed Design Procedure for the Oscillator Circuit Detailed Design Procedure.

## 10 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 8 V and 40 V. This input supply should be well regulated. If the input supply is located more than a few inches from the UC1856-SP converter additional bulk capacitance may be required in addition to the ceramic bypass capacitors. A tantalum capacitor with a value of 47 µF is a typical choice, however this may vary depending upon the output power being delivered.

## 11 Layout

### 11.1 Layout Guidelines

Always try to use a low EMI inductor with a ferrite type closed core. Some examples would be toroid and encased E core inductors. Open core can be used if they have low EMI characteristics and are located a bit more away from the low power traces and components. Make the poles perpendicular to the PCB as well if using an open core. Stick cores usually emit the most unwanted noise.

#### 11.1.1 Feedback Traces

Try to run the feedback trace as far from the inductor and noisy power traces as possible. You would also like the feedback trace to be as direct as possible and somewhat thick. These two sometimes involve a trade-off, but keeping it away from inductor EMI and other noise sources is the more critical of the two. Run the feedback trace on the side of the PCB opposite of the inductor with a ground plane separating the two.

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## Layout Guidelines (continued)

### 11.1.2 Input/Output Capacitors

When using a low value ceramic input filter capacitor, it should be located as close to the VIN pin of the IC as possible. This will eliminate as much trace inductance effects as possible and give the internal IC rail a cleaner voltage supply. Some designs require the use of a feed-forward capacitor connected from the output to the feedback pin as well, usually for stability reasons. In this case it should also be positioned as close to the IC as possible. Using surface mount capacitors also reduces lead length and lessens the chance of noise coupling into the effective antenna created by through-hole components.

### 11.1.3 Compensation Components

External compensation components for stability should also be placed close to the IC. Surface mount components are recommended here as well for the same reasons discussed for the filter capacitors. These should not be located very close to the inductor either.

### 11.1.4 Traces and Ground Planes

Make all of the power (high current) traces as short, direct, and thick as possible. It is good practice on a standard PCB board to make the traces an absolute minimum of 15 mils (0.381 mm) per Ampere. The inductor, output capacitors, and output diode should be as close to each other possible. This helps reduce the EMI radiated by the power traces due to the high switching currents through them. This will also reduce lead inductance and resistance as well, which in turn reduces noise spikes, ringing, and resistive losses that produce voltage errors. The grounds of the IC, input capacitors, output capacitors, and output diode (if applicable) should be connected close together directly to a ground plane. It would also be a good idea to have a ground plane on both sides of the PCB. This will reduce noise as well by reducing ground loop errors as well as by absorbing more of the EMI radiated by the inductor. For multi-layer boards with more than two layers, a ground plane can be used to separate the power plane (where the power traces and components are) and the signal plane (where the feedback and compensation and components are) for improved performance. On multi-layer boards the use of vias will be required to connect traces and different planes. It is good practice to use one standard via per 200 mA of current if the trace will need to conduct a significant amount of current from one plane to the other. Arrange the components so that the switching current loops curl in the same direction. Due to the way switching regulators operate, there are two power states. One state when the switch is on and one when the switch is off. During each state there will be a current loop made by the power components that are currently conducting. Place the power components so that during each of the two states the current loop is conducting in the same direction. This prevents magnetic field reversal caused by the traces between the two half-cycles and reduces radiated EMI.


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# 12 Device and Documentation Support

## 12.1 Trademarks

All trademarks are the property of their respective owners.

## 12.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| 5962-9453001VEA | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9453001VEA UC1856J-SP |
| 5962-9453001VEA.A | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9453001VEA UC1856J-SP |
| 5962-9453001VXC | Active | Production | CFP (HKT) \| 16 | 25 \| TUBE | ROHS Exempt | NIAU | N/A for Pkg Type | -55 to 125 | 5962-9453001VXC UC1856HKT-SP |
| 5962-9453001VXC.A | Active | Production | CFP (HKT) \| 16 | 25 \| TUBE | ROHS Exempt | NIAU | N/A for Pkg Type | -55 to 125 | 5962-9453001VXC UC1856HKT-SP |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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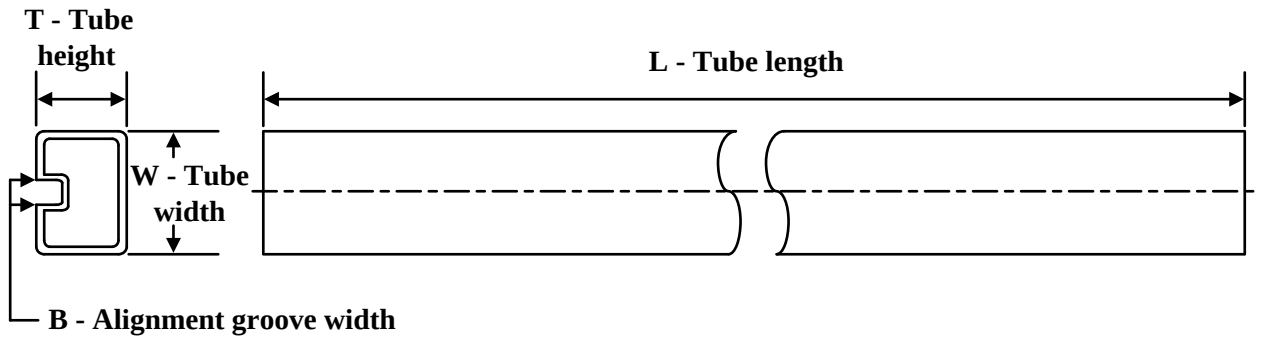
**OTHER QUALIFIED VERSIONS OF UC1856-SP :**

- Catalog : UC1856

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

## TUBE



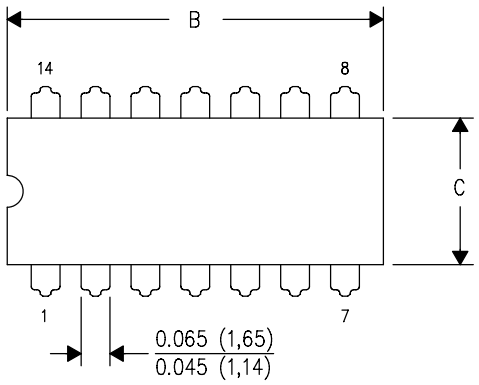

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| 5962-9453001VEA | J | CDIP | 16 | 25 | 506.98 | 15.24 | 13440 | NA |
| 5962-9453001VEA.A | J | CDIP | 16 | 25 | 506.98 | 15.24 | 13440 | NA |
| 5962-9453001VXC | HKT | CFP (HSL) | 16 | 25 | 506.98 | 26.16 | 6220 | NA |
| 5962-9453001VXC.A | HKT | CFP (HSL) | 16 | 25 | 506.98 | 26.16 | 6220 | NA |

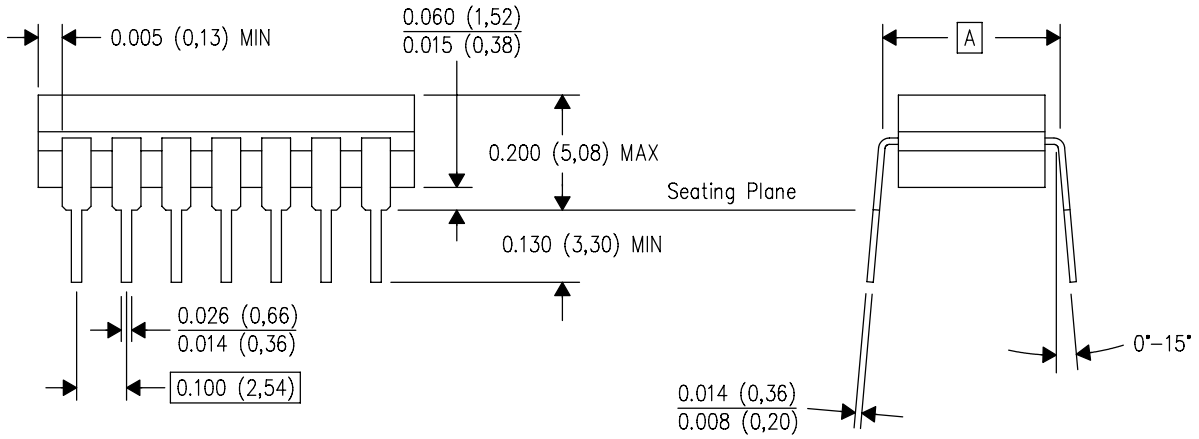
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |




4040083/F 03/03

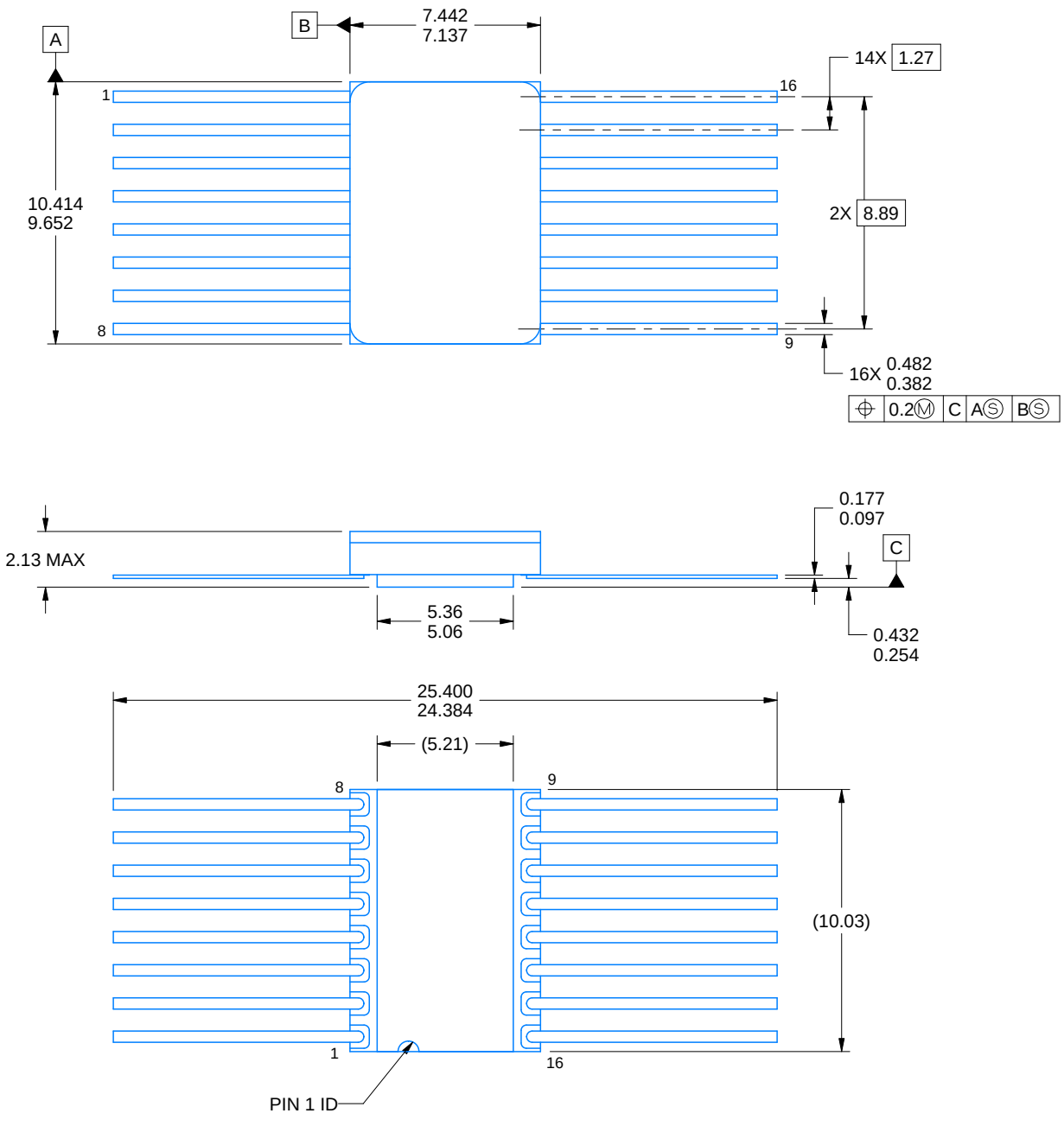
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

# PACKAGE OUTLINE

## HKT0016A

## CFP - 2.13 mm max height

CERAMIC DUAL FLATPACK




NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a metal lid. Lid and cavity are electrically isolated
4. The terminals are gold plated.
5. Falls within MIL-STD-1835 CDFP-F11A.

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