Unitrode Products
from Texas Instruments

application INFO available

UC1875/6/7/8
UC2875/6/7/8
UC3875/6/7/8

Phase Shift Resonant Controller

FEATURES

- Zero to 100% Duty Cycle Control
- Programmable Output Turn-On Delay
- Compatible with Voltage or Current Mode Topologies
- Practical Operation at Switching Frequencies to 1MHz
- Four 2A Totem Pole Outputs
- 10MHz Error Amplifier
- Undervoltage Lockout
- Low Startup Current –150µA
- Outputs Active Low During UVLO
- Soft-Start Control
- Latched Over-Current Comparator With Full Cycle Restart
- Trimmed Reference

DESCRIPTION

The UC1875 family of integrated circuits implements control of a bridge power stage by phase-shifting the switching of one half-bridge with respect to the other, allowing constant frequency pulse-width modulation in combination with resonant, zero-voltage switching for high efficiency performance at high frequencies. This family of circuits may be configured to provide control in either voltage or current mode operation, with a separate over-current shutdown for fast fault protection.

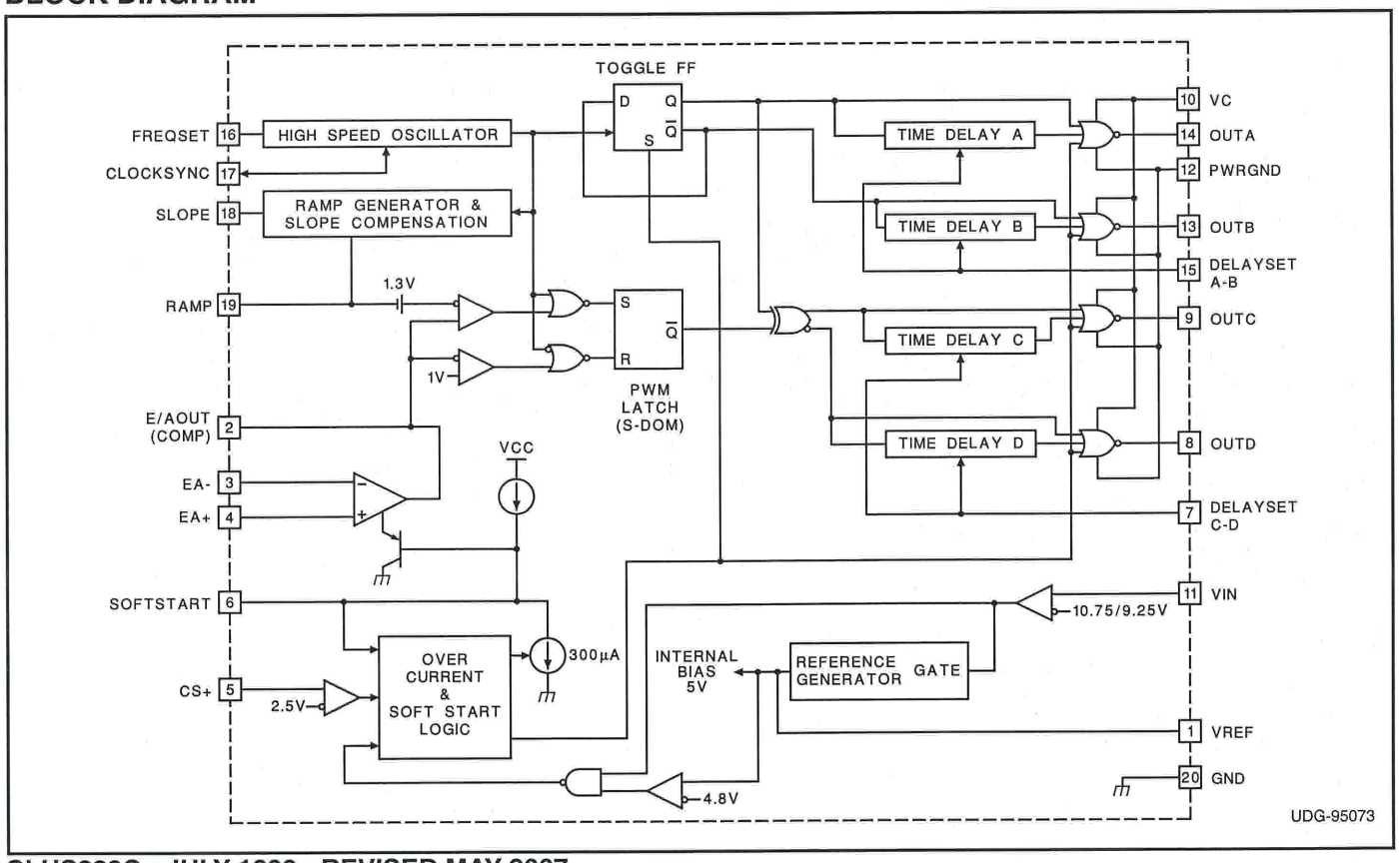
A programmable time delay is provided to insert a dead-time at the turn-on of each output stage. This delay, providing time to allow the resonant switching action, is independently controllable for each output pair (A-B, C-D).

With the oscillator capable of operation at frequencies in excess of 2MHz, overall switching frequencies to 1MHz are practical. In addition to the standard free running mode, with the CLOCKSYNC pin, the user may configure these devices to accept an external clock synchronization signal, or may lock together up to 5 units with the operational frequency determined by the fastest device.

Protective features include an undervoltage lockout which maintains all outputs in an active-low state until the supply reaches a 10.75V threshold. 1.5V hysteresis is built in for reliable, boot-strapped chip supply. Over-current protection is provided, and will latch the outputs in the OFF state within 70nsec of a fault. The current-fault circuitry implements full-cycle restart operation.

(continued)

BLOCK DIAGRAM



DESCRIPTION (cont.)

Additional features include an error amplifier with bandwidth in excess of 7MHz, a 5V reference, provisions for soft-starting, and flexible ramp generation and slope compensation circuitry.

These devices are available in 20-pin DIP, 28-pin "bat-wing" SOIC and 28 lead power PLCC plastic packages for operation over both 0°C to 70°C and –25°C to +85°C temperature ranges; and in hermetically sealed cerdip, surface mount, and ceramic leadless chip carrier packages for –55°C to +125°C operation.

Device	UVLO Turn-On	UVLO Turn-Off	Delay Set
UC1875	10.75	9.25V	Yes
UC1876	15.25V	9.25V	Yes
UC1877	10.75V	9.25V	No
UC1878	15.25V	9.25V	No

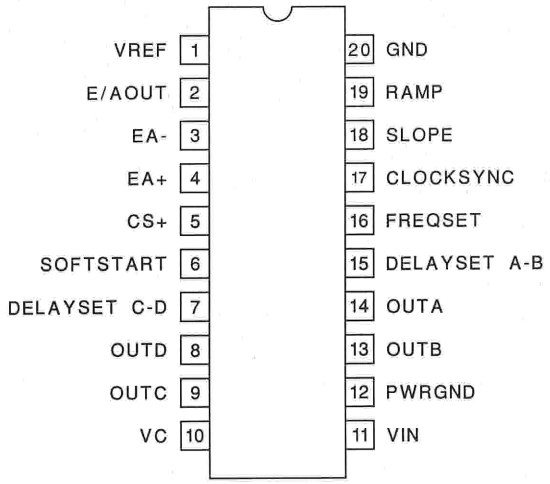
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VC, VIN) 20V
Output Current, Source or Sink
DC 0.5A
Pulse (0.5µs) 3A
Analog I/0s
(Pins 1, 2, 3, 4, 5, 6, 7, 15, 16, 17, 18, 19) . . . . –0.3 to 5.3V
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature. . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

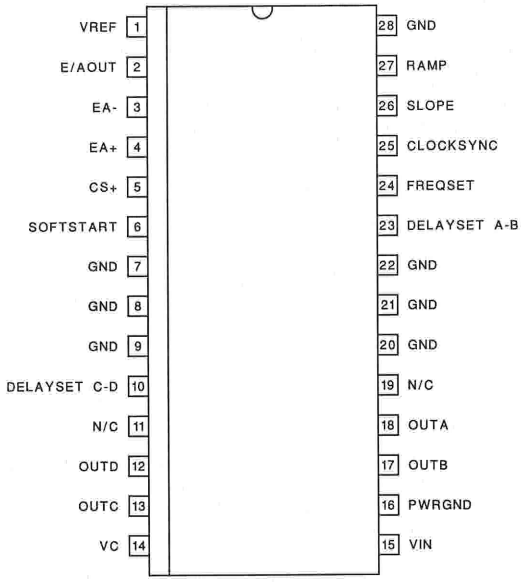
Note: Pin references are to 20 pin packages. All voltages are with respect to ground. Currents are positive into, negative out of, device terminals. Consult Unitrode databook for information regarding thermal specifications and limitations of packages.

CONNECTION DIAGRAMS

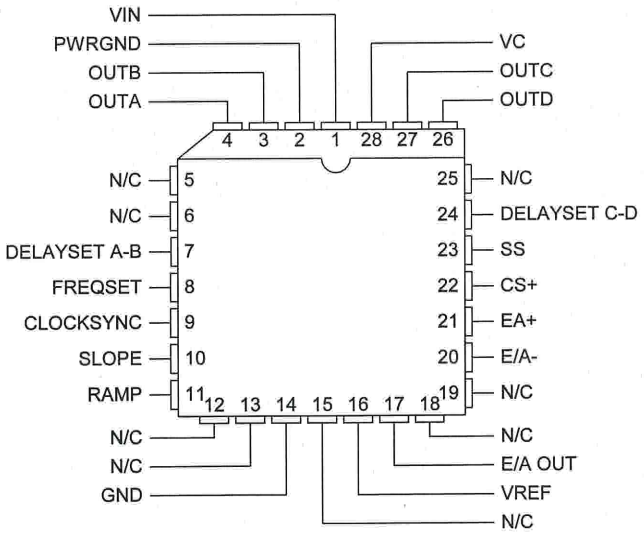
Dil-20 (Top View)
J or N Package



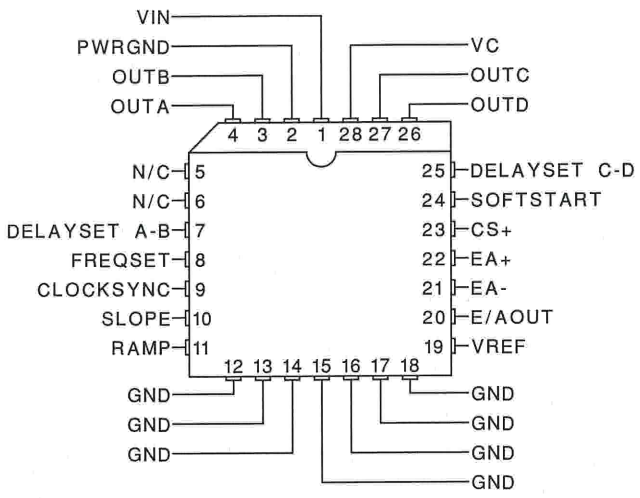
SOIC-28, (Top View)
DWP Package



CLCC-28 (Top View) L Package



PLCC-28 (Top View)
QP Package



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, –55°C < T_A < 125°C for the UC1875/6/7/8, –25°C < T_A < 85°C for the UC2875/6/7/8 and 0°C < T_A < 70°C for the UC3875/6/7/8, VC = VIN = 12V, $R_{FREQSET}$ = 12kΩ, $C_{FREQSET}$ = 330pF, R_{SLOPE} = 12kΩ, C_{RAMP} = 200pF, $C_{DELAYSET\ A\text{-}B}$ = $C_{DELAYSET\ C\text{-}D}$ = 0.01µF, $I_{DELAYSET\ A\text{-}B}$ = $I_{DELAYSET\ C\text{-}D}$ = –500µA, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Undervoltage Lockout					
Start Threshold	UC1875/UC1877		10.75	11.75	V
	UC1876/UC1878		15.25		V
UVLO Hysteresis	UC1875/UC1877	0.5	1.25	2.0	V
	UC1876/UC1878		6.0		V
Supply Current					
I_{IN} Startup	VIN = 8V, VC = 20V, R_{SLOPE} open, I_{DELAY} = 0		150	600	µA
I_C Startup	VIN = 8V, VC = 20V, R_{SLOPE} open, I_{DELAY} = 0		10	100	µA
I_{IN}			30	44	mA
I_C			15	30	mA
Voltage Reference					
Output Voltage	T_J = +25°C	4.92	5	5.08	V
Line Regulation	11 < VIN < 20V		1	10	mV
Load Regulation	I_{VREF} = –10mA		5	20	mV
Total Variation	Line, Load, Temperature	4.9		5.1	V
Noise Voltage	10Hz to 10kHz		50		µVrms
Long Term Stability	T_J = 125°C, 1000 hours		2.5		mV
Short Circuit Current	VREF = 0V, T_J = 25°C		60		mA

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PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Error Amplifier					
Offset Voltage			5	15	mV
Input Bias Current			0.6	3	µA
AVOL	1V < $V_{E/AOUT}$ < 4V	60	90		dB
CMRR	1.5V < V_{CM} < 5.5V	75	95		dB
PSRR	11V < VIN < 20V	85	100		dB
Output Sink Current	$V_{E/AOUT}$ = 1V	1	2.5		mA
Output Source Current	$V_{E/AOUT}$ = 4V		–1.3	–0.5	mA
Output Voltage High	$I_{E/AOUT}$ = –0.5mA	4	4.7	5	V
Output Voltage Low	$I_{E/AOUT}$ = 1mA	0	0.5	1	V
Unity Gain BW	(Note 8)	7	11		MHz
Slew Rate	(Note 8)	6	11		V/µsec
PWM Comparator					
Ramp Offset Voltage	T_J = 25°C (Note 3)		1.3		V
Zero Phase Shift Voltage	(Note 4)	0.55	0.9		V
PWM Phase Shift (Note1) and (Note 7)	$V_{E/AOUT}$ > (Ramp Peak + Ramp Offset)	98	99.5	102	%
	$V_{E/AOUT}$ < Zero Phase Shift Voltage	0	0.5	2	%
Output Skew (Note 1) and (Note 7)	$V_{E/AOUT}$ < 1V		5	±20	nsec
Ramp to Output Delay, (Note 8)	UC3875/6/7/8 (Note 6)		65	100	nsec
	UC1875/6/7/8, UC2875/6/7/8 (Note 6)		65	125	nsec
Oscillator					
Initial Accuracy	T_J = 25°C	0.85	1	1.15	MHz
Voltage Stability	11V < VIN < 20V		0.2	2	%
Total Variation	Line, Temperature	0.80		1.20	MHz
Sync Pin Threshold	T_J = 25°C		3.8		V
Clock Out Peak	T_J = 25°C		4.3		V
Clock Out Low	T_J = 25°C		3.3		V
Clock Out Pulse Width	$R_{CLOCKSYNC}$ = 3.9kΩ		30	100	nsec
Maximum Frequency, (Note 7)	$R_{FREQSET}$ = 5kΩ	2			MHz
Ramp Generator/Slope Compensation					
Ramp Current, Minimum	I_{SLOPE} = 10µA, $V_{FREQSET}$ = VREF		–11	–14	µA
Ramp Current, Maximum	I_{SLOPE} = 1mA, $V_{FREQSET}$ = VREF	–0.8	–0.95		mA
Ramp Valley			0		V
Ramp Peak - Clamping Level	$R_{FREQSET}$ = 100kΩ	3.8	4.1	5.0	V
Current Limit					
Input Bias	V_{CS+} = 3V		2	5	µA
Threshold Voltage		2.4	2.5	2.6	V
Delay to Output, (Note 8)	UC3875/6/7/8		85	125	nsec
	UC1875/6/7/8, UC2875/6/7/8		85	150	nsec

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PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Soft-Start/Reset Delay					
Charge Current	$V_{SOFTSTART}$ = 0.5V	–20	–9	–3	µA
Discharge Current	$V_{SOFTSTART}$ = 1V	120	230		µA
Restart Threshold		4.3	4.7		V
Discharge Level			300		mV
Output Drivers					
Output Low Level	I_{OUT} = 50mA		0.2	0.4	V
	I_{OUT} = 500mA		1.2	2.6	V
Output High Level	I_{OUT} = –50mA		1.5	2.5	V
	I_{OUT} = –500mA		1.7	2.6	V
Delay Set (UC1875 and UC1876 only)					
Delay Set Voltage	I_{DELAY} = –500µA	2.3	2.4	2.6	V
Delay Time, (Note 8)	I_{DELAY} = –250µA (Note 5) (UC3875/6/7/8, UC2875/6/7/8)	150	250	400	nsec
	I_{DELAY} = –250µA (Note 5) (UC1875/6/7/8)	150	250	600	nsec

Note 1: Phase shift percentage (0% = 0°, 100% = 180°) is defined as $\theta = \frac{200}{T}\Phi\%$*, where* θ *is the phase shift, and* Φ *and T are defined in Figure 1. At 0% phase shift,* Φ *is the output skew.*

Note 2: Delay time is defined as delay = T (1/2–(duty cycle)), where T is defined in Fig. 1.

Note 3: Ramp offset voltage has a temperature coefficient of about –4mV/°C.

Note 4: Zero phase shift voltage has a temperature coefficient of about –2mV/°C.

Note 5: Delay time can be programmed via resistors from the delay set pins to ground. Delay time $\cong \frac{62.5 \bullet 10^{-12}}{I_{DELAY}}$ *sec. Where*

$I_{DELAY} = \frac{\text{Delay set voltage}}{R_{DELAY}}$ *The recommended range for* I_{DELAY} *is* $25\mu A \le I_{DELAY} \le 1mA$

Note 6: Ramp delay to output time is defined in Fig. 2.

Note 7: Not production tested at -55°C.

Note 8: Not production tested.

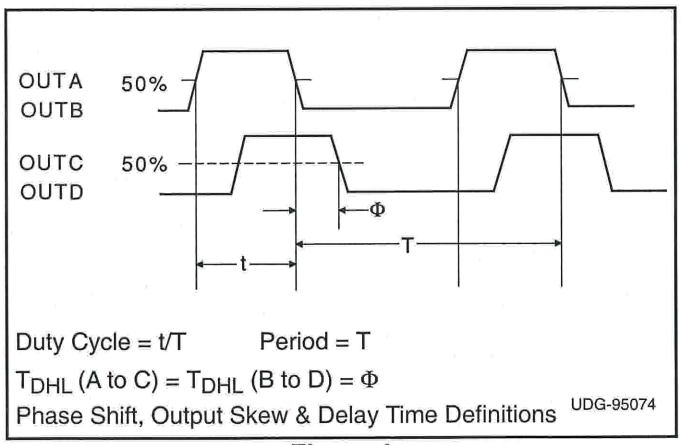


Figure 1

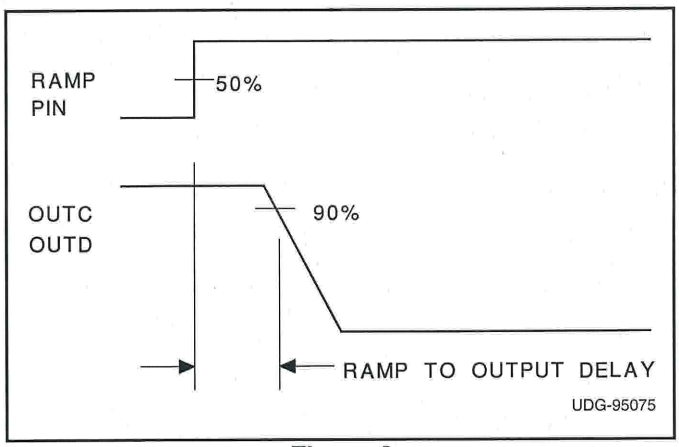


Figure 2

PIN DESCRIPTIONS

CLOCKSYNC (bi-directional clock and synchronization pin): Used as an output, this pin provides a clock signal. As an input, this pin provides a synchronization point. In its simplest usage, multiple devices, each with their own local oscillator frequency, may be connected together by the CLOCKSYNC pin and will synchronize on the fastest oscillator. This pin may also be used to synchronize the device to an external clock, provided the external signal is of higher frequency than the local oscillator. A resistor load may be needed on this pin to minimize the clock pulse width.

E/AOUT (error amplifier output): This is is the gain stage for overall feedback control. Error amplifier output voltage levels below 1 volt will force 0° phase shift. Since the error amplifier has a relatively low current drive capability, the output may be overridden by driving with a sufficiently low impedance source.

CS+ (current sense): The non-inverting input to the current-fault comparator whose reference is set internally to a fixed 2.5V (separate from VREF). When the voltage at this pin exceeds 2.5V the current-fault latch is set, the outputs are forced OFF and a SOFT-START cycle is initiated. If a constant voltage above 2.5V is applied to this pin the outputs are disabled from switching and held in a low state until the CS+ pin is brought below 2.5V. The outputs may begin switching at 0 degrees phase shift before the SOFTSTART pin begins to rise -- this condition will not prematurely deliver power to the load.

FREQSET (oscillator frequency set pin): A resistor and a capacitor from FREQSET to GND will set the oscillator frequency.

DELAYSET A-B, DELAYSET C-D (output delay control): The user programmed current flowing from these pins to GND set the turn-on delay for the corresponding output pair. This delay is introduced between turn-off of one switch and turn-on of another in the same leg of the bridge to provide a dead time in which the resonant switching of the external power switches takes place. Separate delays are provided for the two half-bridges to accommodate differences in the resonant capacitor charging currents.

EA– (error amplifier inverting input): This is normally connected to the voltage divider resistors which sense the power supply output voltage level.

EA+ (error amplifier non-inverting input): This is normally connected to a reference voltage used for comparison with the sensed power supply output voltage level at the EA+ pin.

GND (signal ground): All voltages are measured with respect to GND. The timing capacitor, on the FREQSET pin, any bypass capacitor on the VREF pin, bypass capacitors on VIN and the ramp capacitor, on the RAMP pin, should be connected directly to the ground plane near the signal ground pin.

OUTA-OUTD (outputs A-D): The outputs are 2A totem-pole drivers optimized for both MOSFET gates and level-shifting transformers. The outputs operate as pairs with a nominal 50% duty-cycle. The A-B pair is intended to drive one half-bridge in the external power stage and is syncronized with the clock waveform. The C-D pair will drive the other half-bridge with switching phase shifted with respect to the A-B outputs.

PWRGND (power ground): VC should be bypassed with a ceramic capacitor from the VC pin to the section of the ground plane that is connected to PWRGND. Any required bulk reservoir capacitor should parallel this one. Power ground and signal ground may be joined at a single point to optimize noise rejection and minimize DC drops.

RAMP (voltage ramp): This pin is the input to the PWM comparator. Connect a capacitor from here to GND. A voltage ramp is developed at this pin with a slope:

$$\frac{dV}{dT} = \frac{Sense\,Voltage}{R_{SLOPE} \bullet C_{RAMP}}$$

Current mode control may be achieved with a minimum amount of external circuitry, in which case this pin provides slope compensation.

Because of the 1.3V offset between the ramp input and the PWM comparator, the error amplifier output voltage can not exceed the effective ramp peak voltage and duty cycle clamping is easily achievable with appropriate values of R_{SLOPE} and C_{RAMP}.

SLOPE (set ramp slope/slope compensation): A resistor from this pin to VCC will set the current used to generate the ramp. Connecting this resistor to the DC input line voltage will provide voltage feed-forward.

SOFTSTART (soft start): SOFTSTART will remain at GND as long as VIN is below the UVLO threshold. SOFTSTART will be pulled up to about 4.8V by an internal 9μA current source when VIN becomes valid (assuming a non-fault condition). In the event of a current-fault (CS+ voltage exceeding 2.5V), SOFTSTART will be pulled to GND and them ramp to 4.8V. If a fault occurs during the SOFTSTART cycle, the outputs will be immediately disabled and SOFTSTART must charge fully prior to resetting the fault latch.

For paralleled controllers, the SOFTSTART pins may be paralled to a single capacitor, but the charge currents will be additive.

PIN DESCRIPTIONS (cont.)

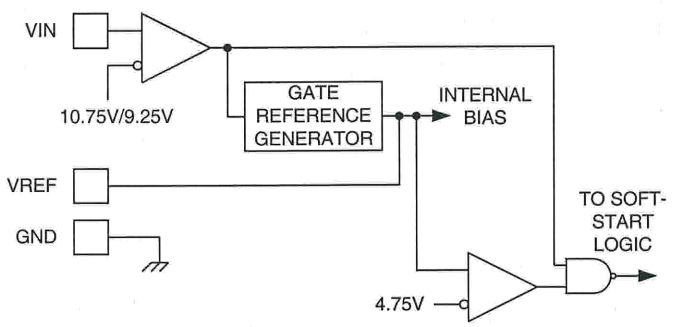
VC (output switch supply voltage): This pin supplies power to the output drivers and their associated bias circuitry. Connect VC to a stable source above 3V for normal operation, above 12V for best performance. This supply should be bypassed directly to the PWRGND pin with low ESR, low ESL capacitors.

VIN (primary chip supply voltage): This pin supplies power to the logic and analog circuitry on the integrated circuit that is not directly associated with driving the output stages. Connect VIN to a stable source above 12V for normal operation. To ensure proper chip functionality, these devices will be inactive until VIN exceeds the upper undervoltage lockout threshold. This pin should by bypassed directly to the GND pin with low ESR, low ESL capacitors.

NOTE: When VIN exceeds the UVLO threshold the supply current (I_{IN}) will jump from about 100μA to a current in excess of 20μA. If the UC1875 is not connected to a well bypassed supply, it may immediately enter UVLO again.

VREF: This pin is an accurate 5V voltage reference. This output is capable of delivering about 60mA to peripheral circuitry and is internally short circuit current limited. VREF is disabled while VIN is low enough to force the chip into UVLO. The circuit is also in UVLO until VREF reaches approximately 4.75V. For best results bypass VREF with a 0.1μF, low ESR, low ESL, capacitor to the GND pin.

APPLICATION INFORMATION
Undervoltage Lockout Section

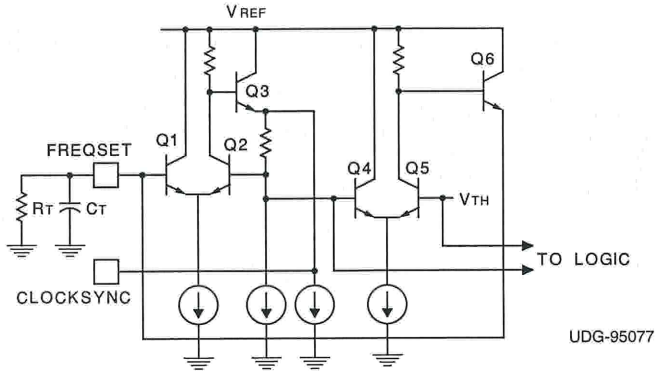


When power is applied to the circuit and VIN is below the upper UVLO threshold, I_{IN} will be below 600μA, the reference generator will be off, the fault latch is reset, the soft-start pin is discharged, and the outputs are actively held low. When VIN exceeds the upper UVLO threshold, the reference generator turns on. All else remains in the shut-down mode until the output of the reference, VREF, exceeds 4.75V.

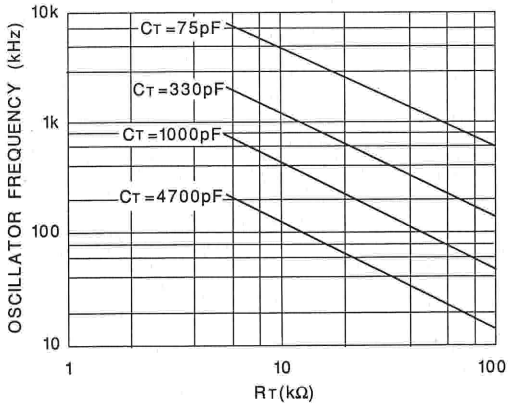
UDG-99136

The high frequency oscillator may be either free-running or externally synchronized. For free-running operation, the frequency is set via an external resistor and capacitor to ground from the FREQSET pin.

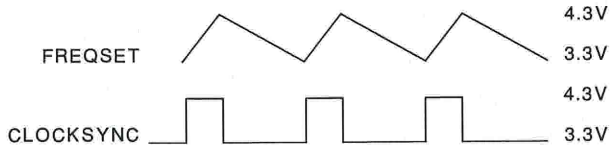
Simplified Oscillator Schematic



UDG-95077



UDG-95079



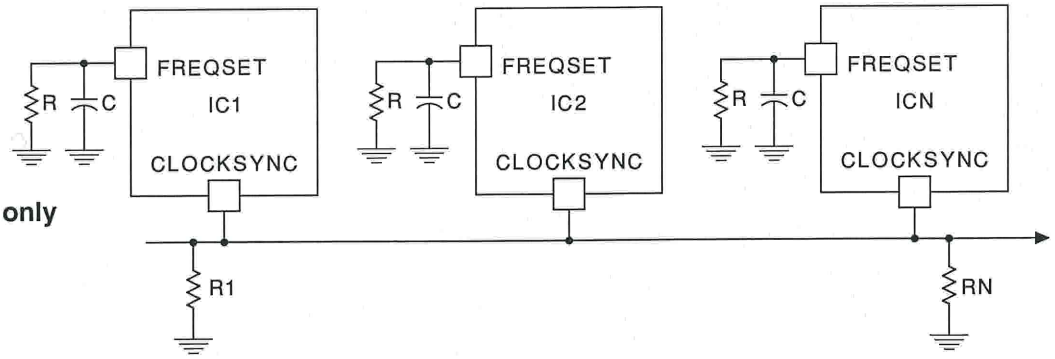
UDG-95078

APPLICATION INFORMATION (cont.)

Synchronizing The Oscillator

The CLOCKSYNC pin of the oscillator may be used to synchronize multiple UC1875 devices simply by connecting the CLOCKSYNC of each UC1875 to the others:

1875/6/7/8s only



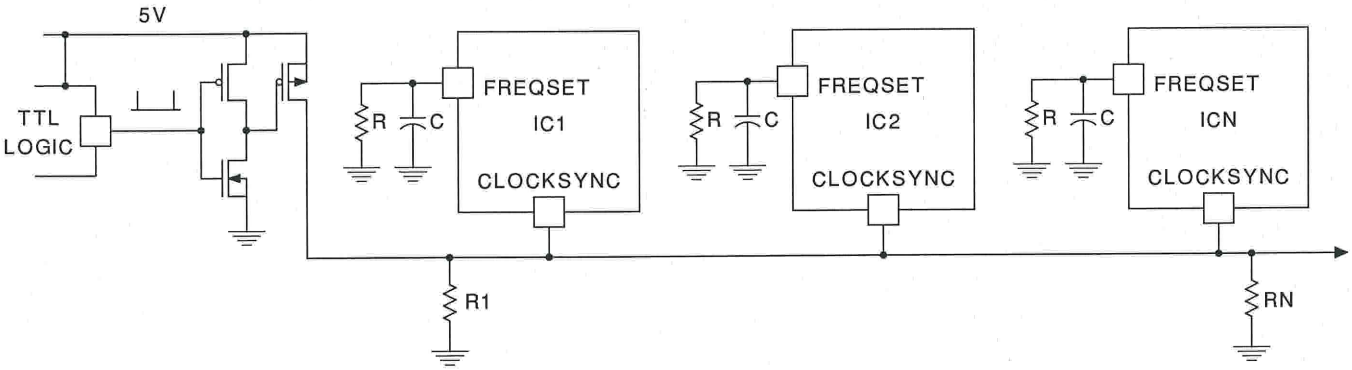
UDG-95080

All ICs will sync to chip with the fastest local oscillator.

R1 & RN *may* be needed to keep sync pulse narrow due to capacitance on line.

R1 & RN *may* also be needed to properly terminate R_{SYNC} line.

Syncing to external TTL/CMOS



UDG-95081

ICs will sync to fastest chip or TTL clock if it is higher frequency.

R & RN *may* be needed for same reasons as above

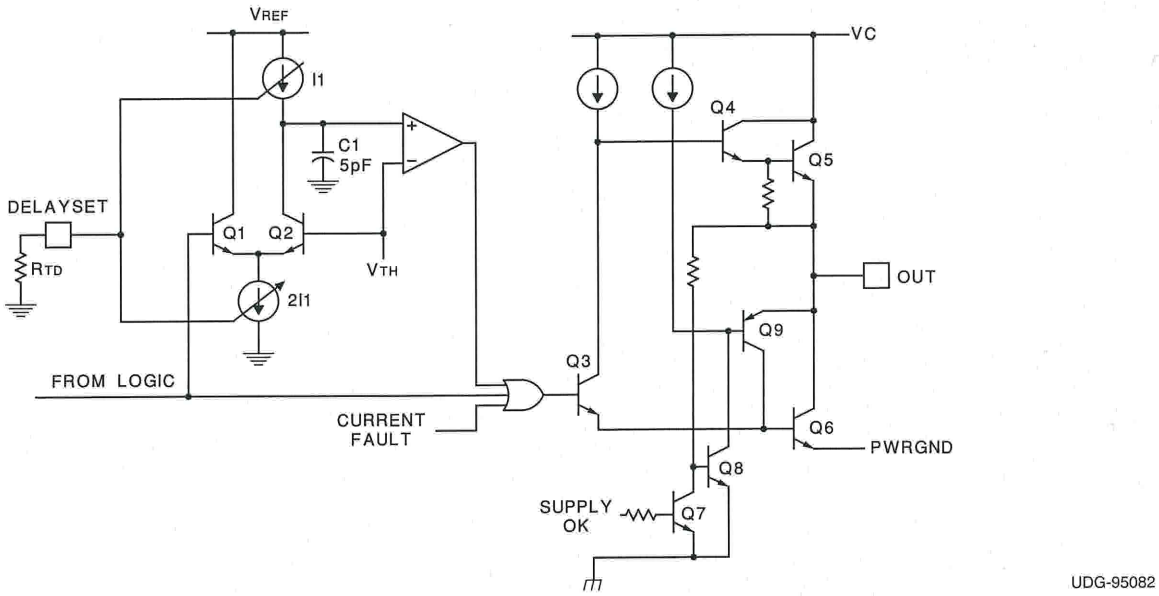
Although each UC1875/6/7/8 has a local oscillator frequency, the group of devices will synchronize to the fastest oscillator driving the CLOCKSYNC pin. This arrangement allows the synchronizing connection between ICs to be broken without any local loss of functionality.

Synchronizing the device to an external clock signal may be accomplished with a minimum of external circuitry, as shown in the previous figure.

Capacitive loading on the CLOCKSYNC pin will increase the clock pulse width, and may adversely effect system performance. Therefore, a resistor to ground from the CLOCKSYNC pin is optional, but may be required to offset capacitive loading on this pin. These resistors are shown in the oscillator schematics as R1, RN.

APPLICATION INFORMATION (cont.)
Delay Blocks And Output Stages

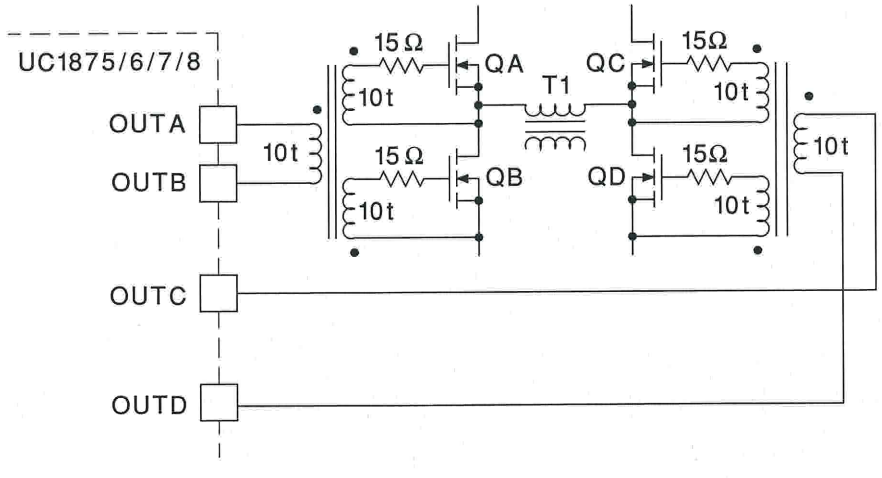
In each of the output stages, transistors Q3 through Q6 form a high-speed totem-pole driver which will source or sink more than one amp peak with a total delay of approximately 30 nanoseconds. To ensure a low output level prior to turn-on, transistors Q7 through Q9 form a self-biased driver to hold Q6 on prior to the supply reaching its turn-on threshold. This circuit is operable when the chip supply is zero. Q6 is also turned on and held low with a signal from the fault logic portion of the chip.



The delay providing the dead-time is accomplished with C1 which must discharge to V_{TH} before the output can go high. The time is defined by the current sources, I1, which is programmed by an external resistor, R_{TD}. The voltage on the Delay Set pins is internally regulated to 2.5V and the range of dead time control is from 50 to 200 nanoseconds. NOTE: There is no way to disable the delay circuitry, and the delay time must be programmed.

Output Switch Orientation

The four outputs of the UC1875/6/7/8 interface to the full bridge converter switches as shown below:



3 Winding Bifilar, AWG 30 Kynar Insulation

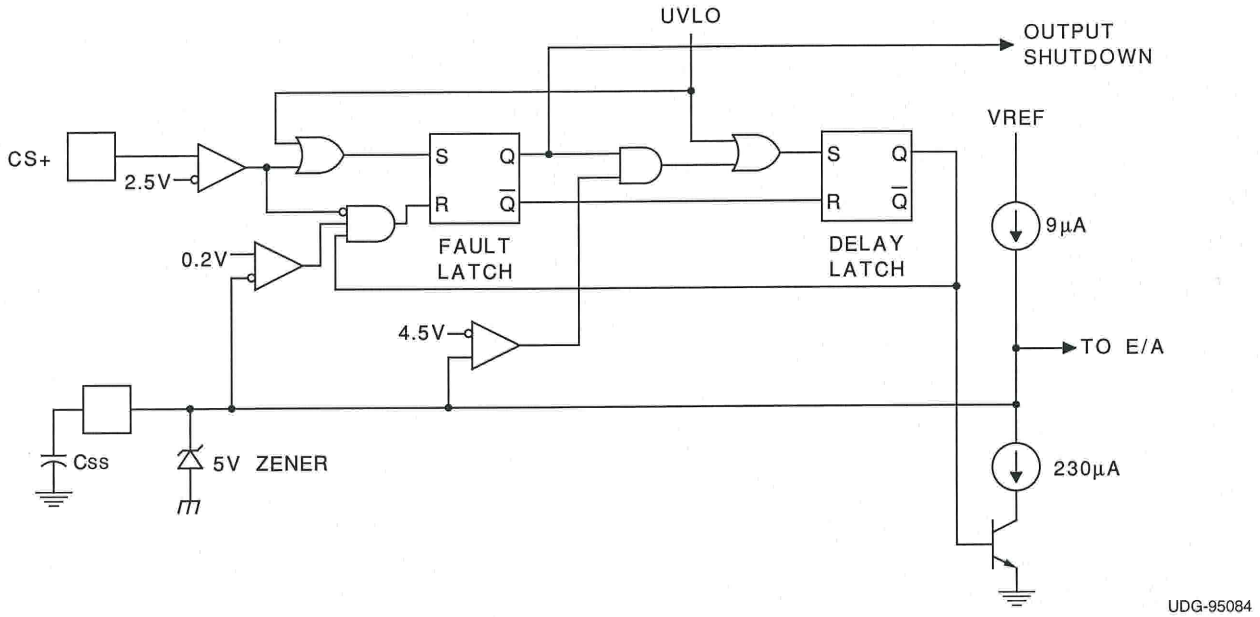
APPLICATION INFORMATION (cont.)
Fault/Soft-Start

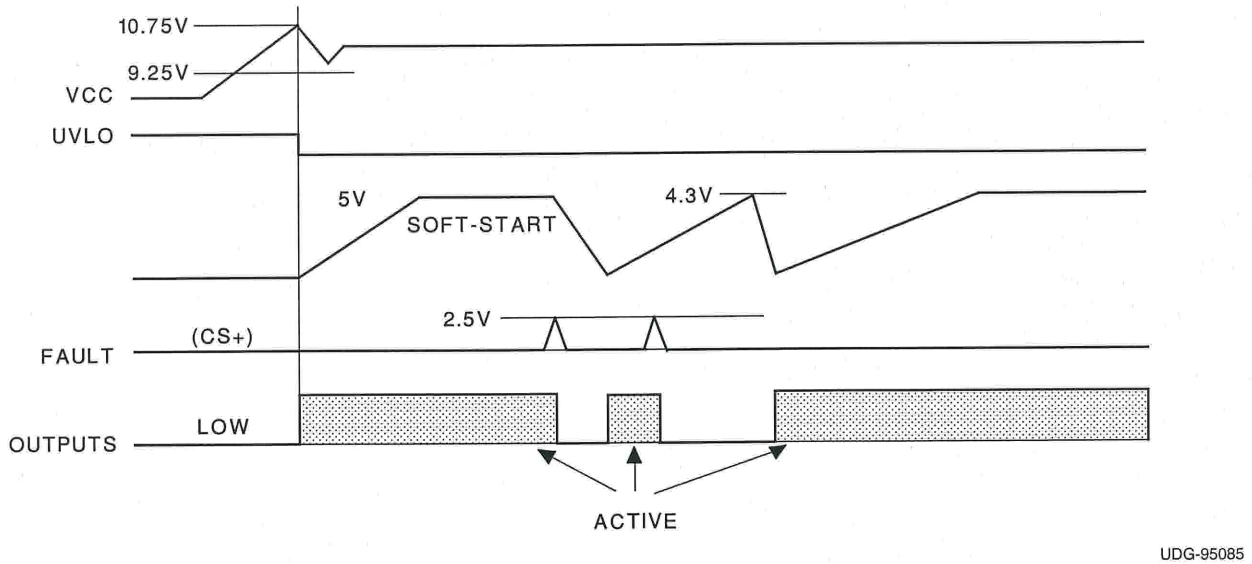
The fault control circuitry provides two forms of power shutdown:

- Complete turn-off of all four output power stages.
- Clamping the phase shift command to zero.

Complete turn-off is ordered for an over-current fault or a low supply voltage. When the SOFTSTART pin reaches its low threshold, switching is allowed to proceed while the phase-shift is advanced from zero to its nominal value with the time constant of the SOFT-START capacitor.

The fault logic insures that a continuous fault will institute a low frequency "hiccup" retry cycle by forcing the SOFT-START capacitor to charge through its full cycle between each restart attempt.





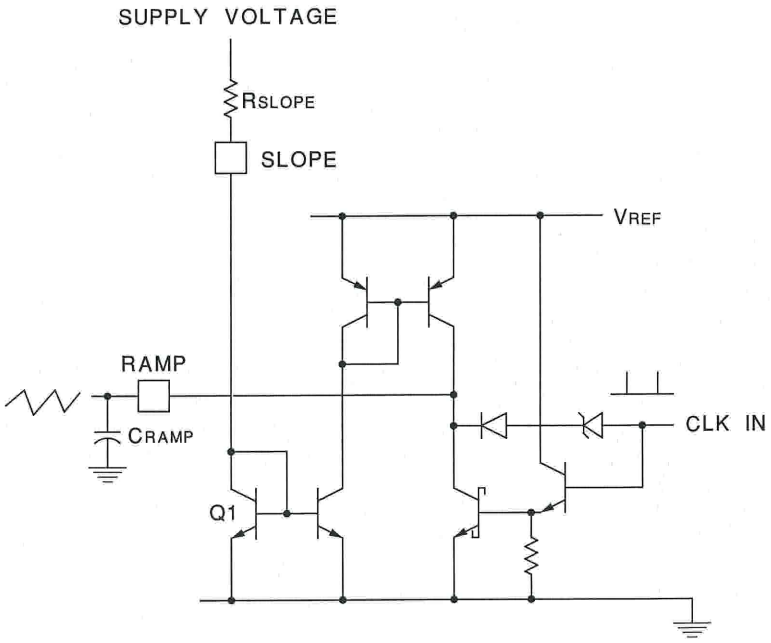
APPLICATIONS INFORMATION (cont.)
Slope/Ramp Pins

The ramp generator may be configured for the following control methods:

- Voltage Mode
- Voltage Feedforward
- Current Mode
- Current Mode with Slope Compensation

The figure below shows a voltage-mode configuration. With R_{SLOPE} tied to a stable voltage source, the waveform on C_{RAMP} will be a constant-slope ramp, providing conventional voltage-mode control. If R_{SLOPE} is connected to the power supply input voltage, a variable-slope ramp will provide voltage feedforward.

Voltage Mode Operation



UDG-95086

1. Simple voltage mode operation achieved by placing R_{SLOPE} between VIN and SLOPE.

2. Voltage Feedforward achieved by placing R_{SLOPE} between supply voltage and SLOPE pin of UC1875.

RAMP

$$\frac{dV}{dT} \approx \frac{V_{Rslope}}{R_{SLOPE} \bullet C_{RAMP}}$$

For current-mode control the ramp generator may be disabled by grounding the slope pin and using the ramp pin as a direct current sense input to the PWM comparator.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9455501M3A	NRND	Production	LCCC (FK) | 28	42 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9455501M3A UC1875L/883B
5962-9455501MRA	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9455501MRA UC1875J/883B
UC1875J	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	UC1875J
UC1875J.A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	UC1875J
UC1875J883B	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9455501MRA UC1875J/883B
UC1875J883B.A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9455501MRA UC1875J/883B
UC1875L	NRND	Production	LCCC (FK) | 28	42 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	UC1875L
UC1875L.A	NRND	Production	LCCC (FK) | 28	42 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	UC1875L
UC1875L883B	NRND	Production	LCCC (FK) | 28	42 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9455501M3A UC1875L/883B
UC1875L883B.A	NRND	Production	LCCC (FK) | 28	42 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9455501M3A UC1875L/883B
UC2875DWP	Obsolete	Production	SOIC (DW) | 28	-	-	Call TI	Call TI	-25 to 85	UC2875DWP
UC2875DWPTR	NRND	Production	SOIC (DW) | 28	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	UC2875DWP
UC2875DWPTR.A	NRND	Production	SOIC (DW) | 28	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	UC2875DWP
UC2875N	NRND	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU | SN	N/A for Pkg Type	-25 to 85	UC2875N
UC2875N.A	NRND	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-25 to 85	UC2875N
UC2875NG4	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-25 to 85	UC2875N
UC2875NG4.A	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-25 to 85	UC2875N
UC3875DWPTR	Obsolete	Production	SOIC (DW) | 28	-	-	Call TI	Call TI	0 to 70	UC3875DWP

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UC3875N	NRND	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU | SN	N/A for Pkg Type	0 to 70	UC3875N
UC3875N.A	NRND	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UC3875N
UC3875NG4	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UC3875N
UC3875NG4.A	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UC3875N
UC3876N	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU | SN	N/A for Pkg Type	0 to 70	UC3876N
UC3876N.A	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UC3876N

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF UC1875, UC2875, UC3875 :

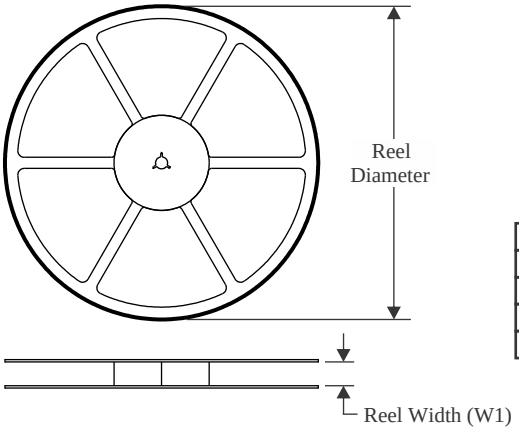
- Catalog : UC3875
- Enhanced Product : UC2875-EP
- Military : UC1875
- Space : UC1875-SP

NOTE: Qualified Version Definitions:

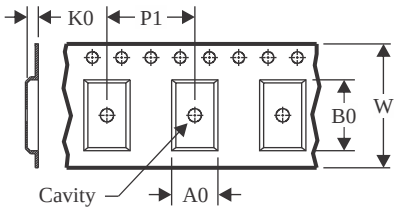
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

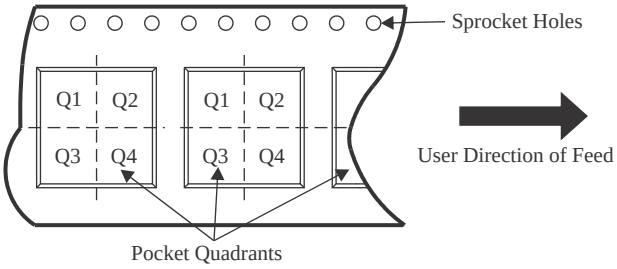


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

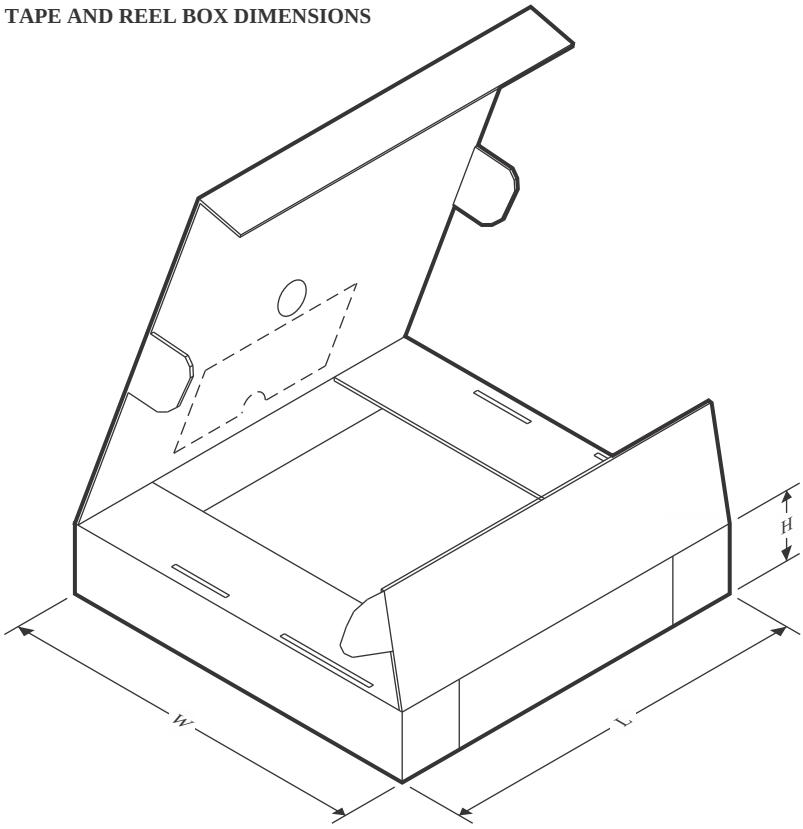
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2875DWPTR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

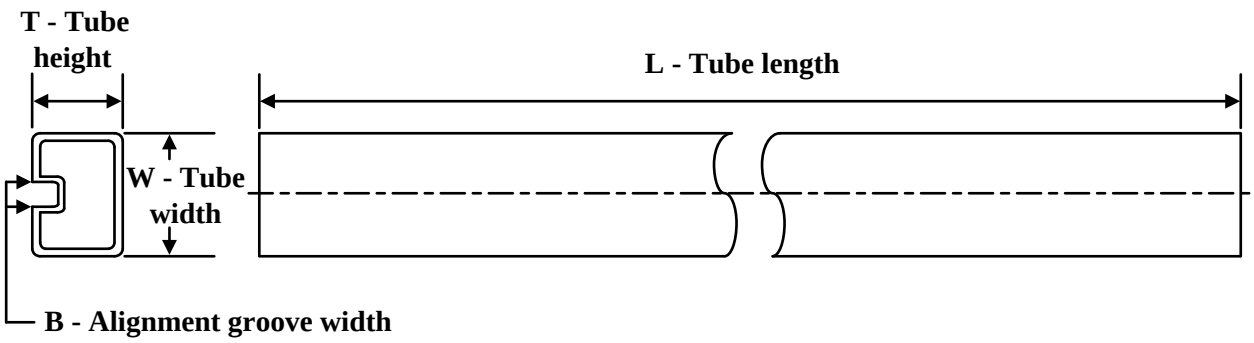
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2875DWPTR	SOIC	DW	28	1000	356.0	356.0	53.0

TUBE

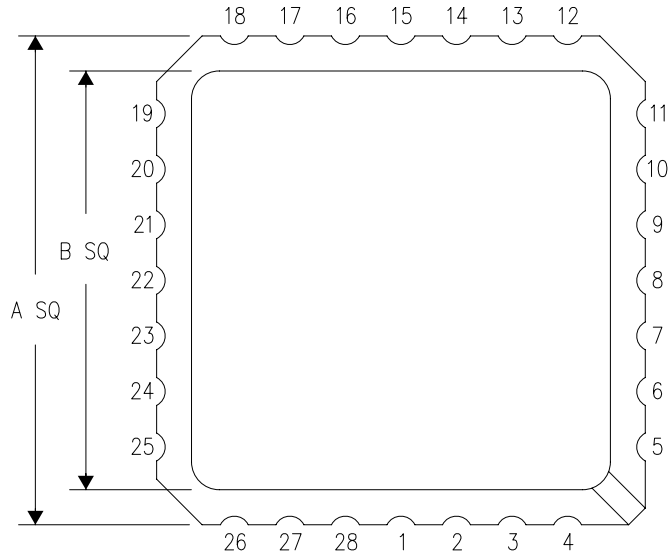


*All dimensions are nominal

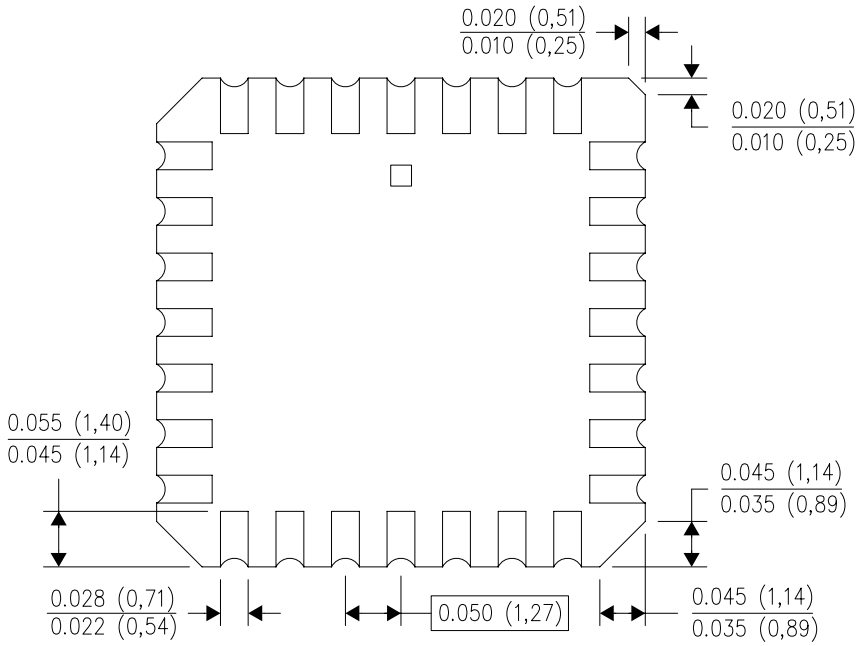
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UC2875N	N	PDIP	20	20	506	13.97	11230	4.32
UC2875N.A	N	PDIP	20	20	506	13.97	11230	4.32
UC2875NG4	N	PDIP	20	20	506	13.97	11230	4.32
UC2875NG4.A	N	PDIP	20	20	506	13.97	11230	4.32
UC3875N	N	PDIP	20	20	506	13.97	11230	4.32
UC3875N.A	N	PDIP	20	20	506	13.97	11230	4.32
UC3875NG4	N	PDIP	20	20	506	13.97	11230	4.32
UC3875NG4.A	N	PDIP	20	20	506	13.97	11230	4.32
UC3876N	N	PDIP	20	20	506	13.97	11230	4.32
UC3876N.A	N	PDIP	20	20	506	13.97	11230	4.32

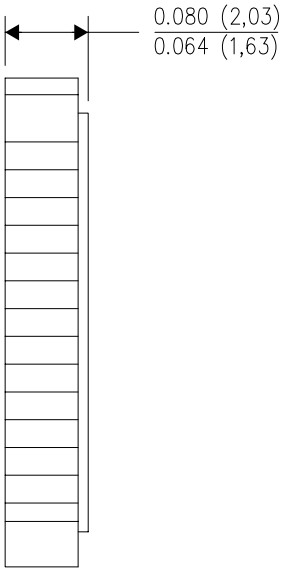
FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



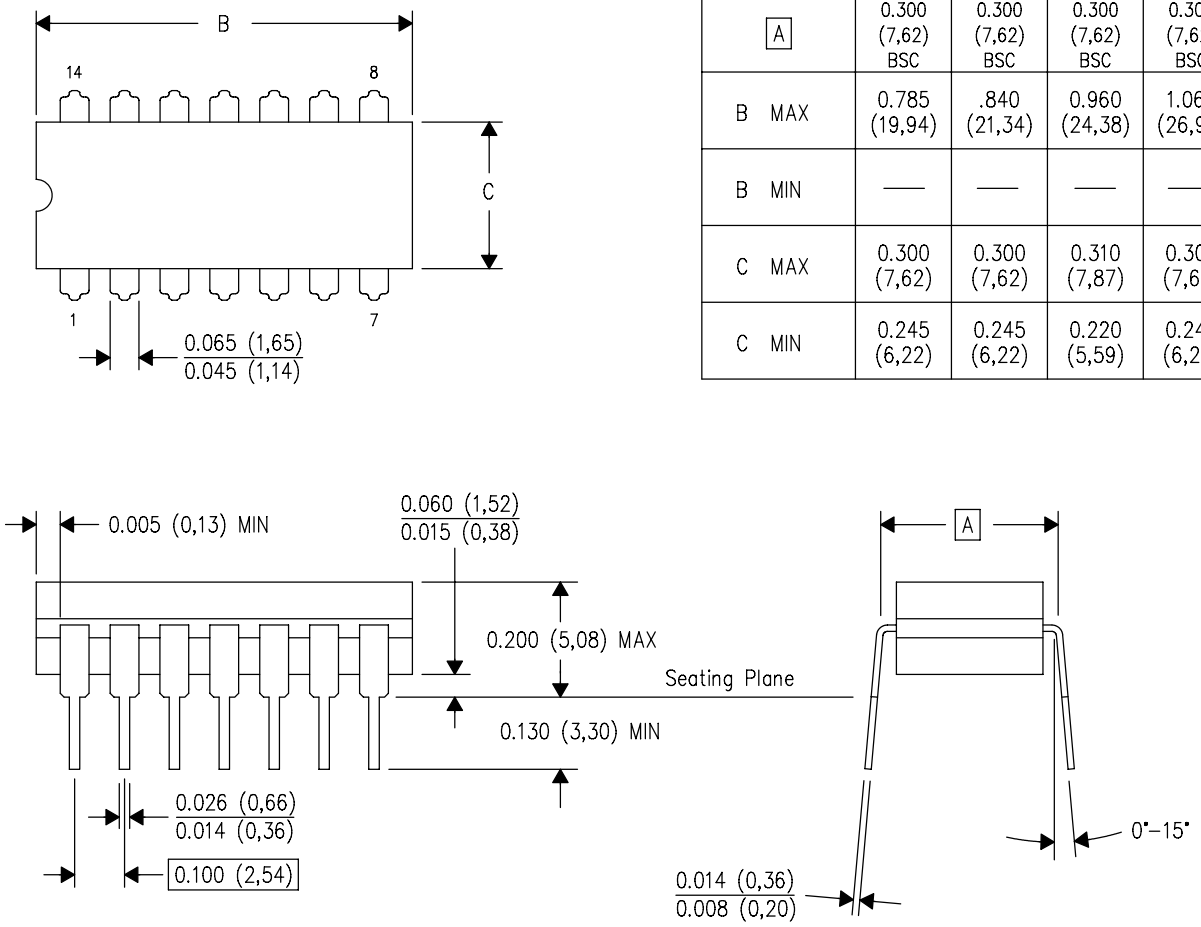


4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

J (R–GDIP–T**) CERAMIC DUAL IN–LINE PACKAGE

14 LEADS SHOWN



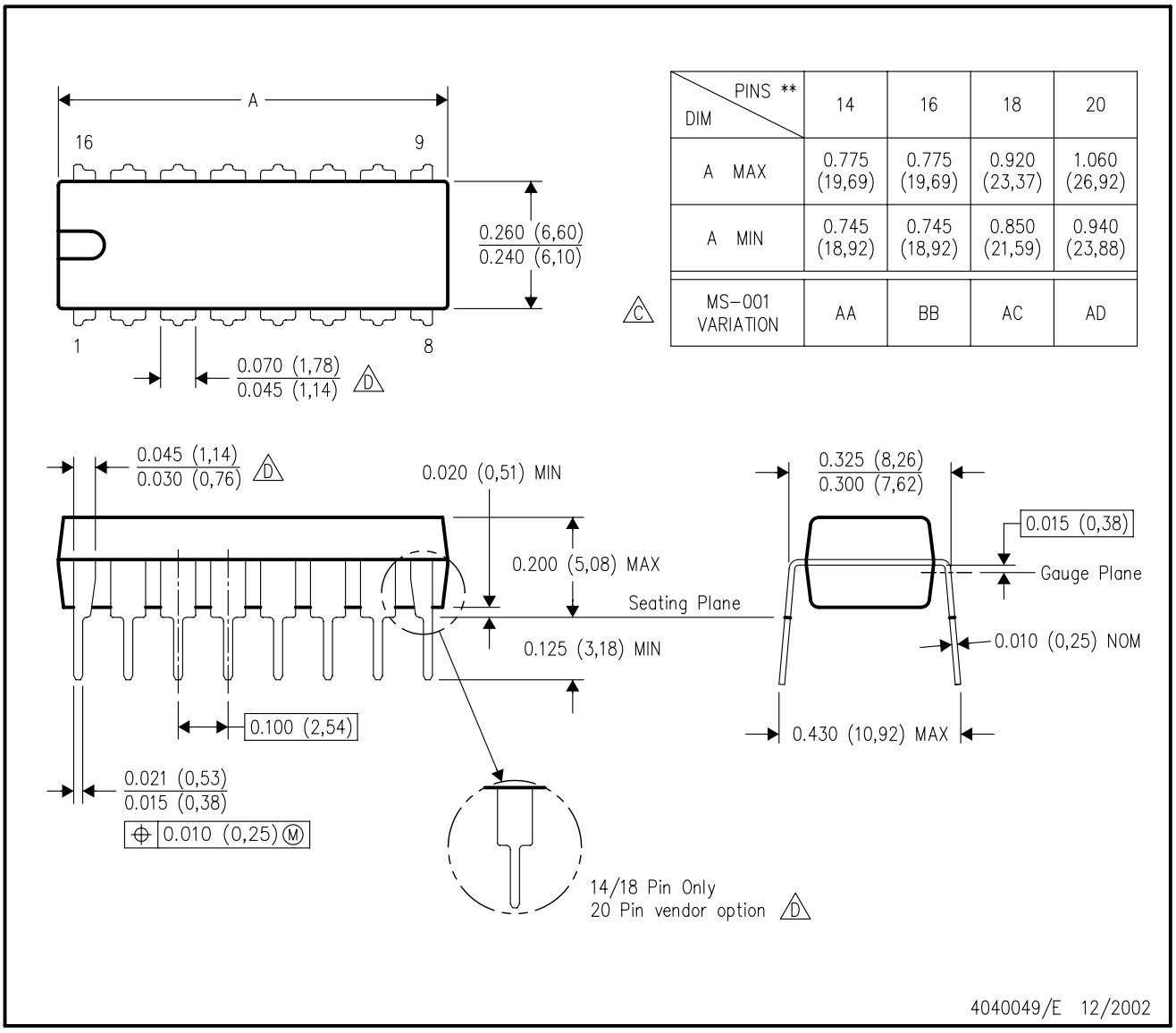
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

4040083/F 03/03

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

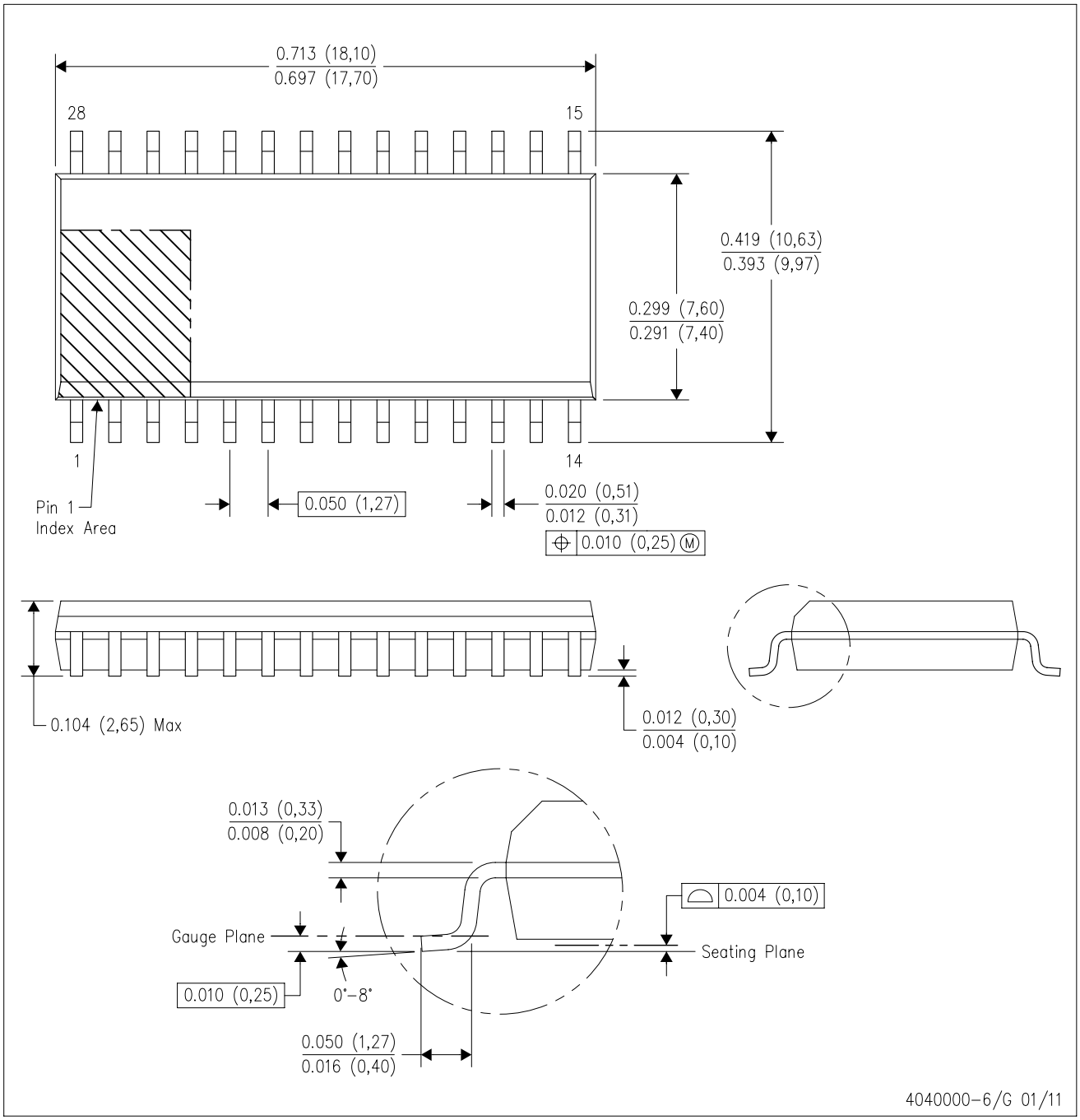
16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD

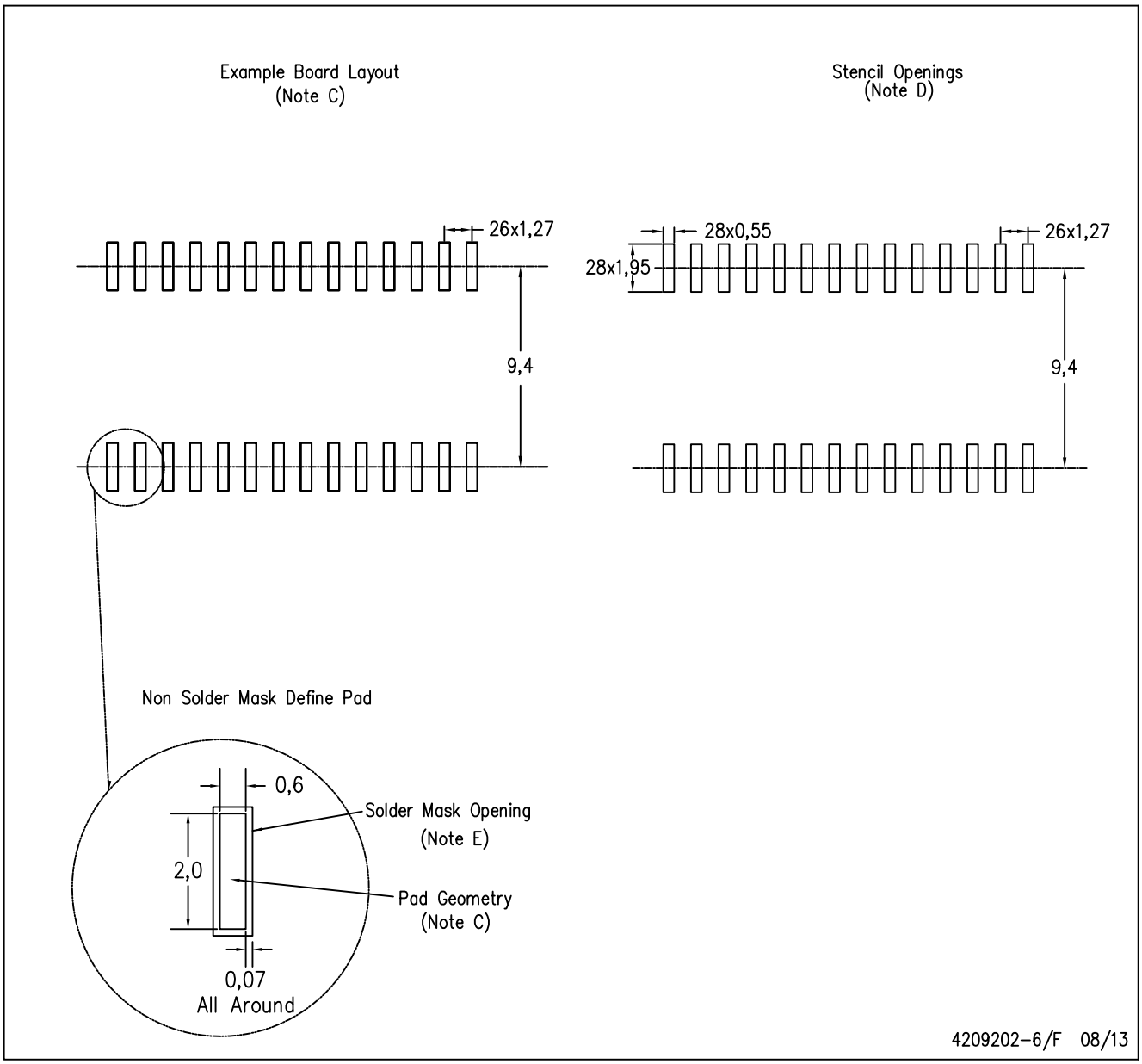
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AE.

DW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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