UCx52xA Regulating Pulse Width Modulators

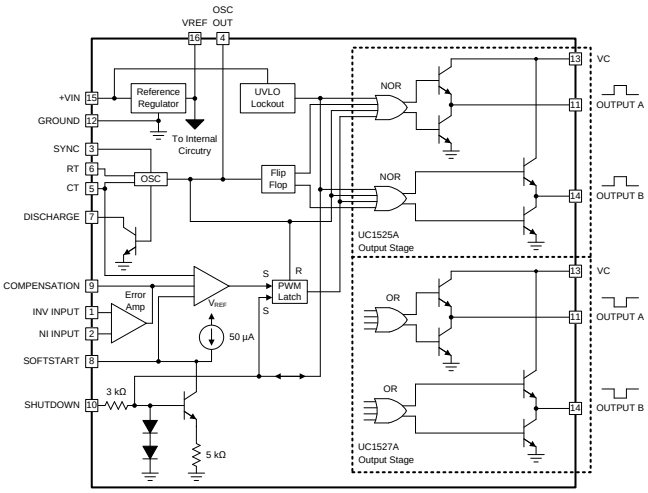
1 Features

- 8-V to 35-V Operation
- 5.1-V Reference Trimmed to 1%
- 100-Hz to 500-kHz Oscillator Range
- Separate Oscillator Sync Terminal
- Adjustable Dead-Time Control
- Internal Soft Start
- Pulse-by-Pulse Shutdown
- Input Undervoltage Lockout With Hysteresis
- Latching PWM to Prevent Multiple Pulses
- Dual Source and Sink Output Drivers

2 Applications

- Off-Line and DC/DC Power Supplies
- Converters Using Voltage Mode
- Single-Ended or Two-Switch Topology Designs
- Solar Inverters
- Welding Inverters
- Motor Control
- Battery Chargers

Block Diagram



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3 Description

The UC1525A/1527A series of pulse width modulator integrated circuits are designed to offer improved performance and lowered external parts count when used in designing all types of switching power supplies. The on-chip 5.1-V reference is trimmed to 1% and the input common-mode range of the error amplifier includes the reference voltage, eliminating external resistors. A sync input to the oscillator allows multiple units to be slaved or a single unit to be synchronized to an external system clock. A single resistor between C_T and the discharge terminals provides a wide range of dead-time adjustment. These devices also feature built-in soft-start circuitry with only an external timing capacitor required. A shutdown terminal controls both the soft-start circuitry and the output stages, providing instantaneous turn off through the PWM latch with pulsed shutdown, as well as soft-start recycle with longer shutdown commands.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCx52xA	LCCC (20)	8.89 mm × 8.89 mm
	CDIP (16)	19.56 mm × 6.67 mm
	SOIC (16)	10.30 mm × 7.50 mm
	PDIP (16)	19.30 mm × 6.35 mm
	PLCC (20)	8.96 mm × 8.96 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Revision C (January 2008) to Revision D — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Added *Thermal Information* table ... 5
- Changed $R_{\theta JA}$ values in the *Thermal Information table: from 80-120 to N/A for J; from 90 to 47.6 for N; from 45-90 to 72.6 for DW; from 43-75 to 55.8 for FN; and from 70-80 to N/A for FK* ... 5
- Changed $R_{\theta JC}$ values in the *Thermal Information* table: from 28 to 37.4 (top) and 10.1 (bottom) for J; from 45 to 37.3 (top) for N; from 25 to 34 (top) for DW; from 34 to 33.7 (top) for FN; and from 20 to 32.9 (top) to 3.5 (bottom) for FK ... 5

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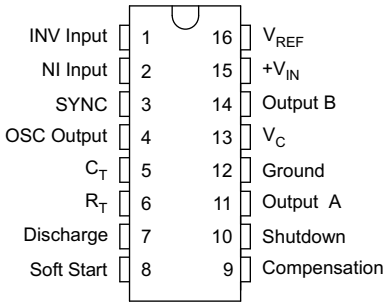
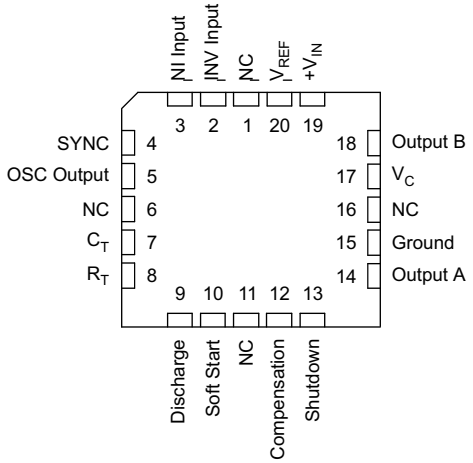
5 Pin Configuration and Functions

J and N Package
16-Pin CDIP and PDIP
Top View



FN and FK Packages
20-Pin PLCC or LCCC
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	CDIP, PDIP	PLCC, LCCC		
INV Input	1	2	I	Inverting input to the error amplifier
NI Input	2	3	I	Noninverting input to the error amplifier
SYNC	3	4	I	Oscillator sync terminal
OSC Output	4	5	O	Oscillator frequency output
C_T	5	7	I	Timing capacitor connection pin for oscillator frequency programming. The timing capacitor should be connected to the device ground using minimal trace length.
R_T	6	8	I	Timing resistor connection pin for oscillator frequency programming
Discharge	7	9	I	A single resistor between C_T and the discharge terminals provides dead-time adjustment
Soft Start	8	10	I	Soft-start input pin.
Compensation	9	12	O	Output of the error amplifier for compensation
Shutdown	10	13	I	Pull this pin high to shut down PWM output
Output A	11	14	O	output A of the on-chip drive stage
Ground	12	15	—	Ground return pin
V_C	13	17	—	Power supply pin for the output stage. This pin should be bypassed with a 0.1-µF monolithic ceramic low ESL capacitor with minimal trace lengths.
Output B	14	18	O	Output B of the on-chip drive stage.
$+V_{IN}$	15	19	—	Input voltage
V_{REF}	16	20	O	5.1-V reference. For stability, the reference should be bypassed with a 0.1-µF monolithic ceramic low ESL capacitor and minimal trace length to the ground plane.
NC	—	1, 6, 11, 16	—	No internal connection

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
$+V_{IN}$	Supply voltage		40	V
V_C	Collector supply voltage		40	V
	Logic inputs	–0.3	5.5	V
	Analog inputs	–0.3	$+V_{IN}$	V
	Output current, source or sink		500	mA
	Reference output current		50	mA
	Oscillator charging current		5	mA
	Power dissipation at T_A = +25°C(2)		1000	mW
	Power dissipation at T_C = +25°C(2)		2000	mW
	Operating junction temperature	–55	150	°C
	Lead temperature (soldering, 10 seconds)		300	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]	1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
$+V_{IN}$	Input voltage		8	35	V
V_C	Collector supply voltage		4.5	35	V
	Sink/source load current (steady state)		0	100	mA
	Sink/source load current (peak)		0	400	mA
	Reference load current		0	20	mA
	Oscillator frequency range		100	400	Hz
	Oscillator timing resistor		2	150	kΩ
	Oscillator timing capacitor		0.001	0.01	µF
	Dead time resistor range		0	500	Ω
	Operating ambient temperature	UC1525A, UC1527A	–55	125	°C
		UC2525A, UC2527A	–25	85	
		UC3525A, UC3527A	0	70	

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6.4 Thermal Information

THERMAL METRIC[1]		UCx52xA					UNIT
		FK (LCCC)	J (CDIP)	DW (SOIC)	N (PDIP)	FN (PLCC)	
		20 PINS	16 PINS	16 PINS	16 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	N/A	N/A	72.6	47.6	55.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	32.9	37.4	34	37.3	33.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	32.1	54.2	37.3	27.7	21.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	N/A	N/A	8.9	17.3	9.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	N/A	N/A	36.8	27.5	20.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.5	10.1	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
REFERENCE						
Output voltage	T_J = 25°C	UC152xA, UC252xA	5.05	5.1	5.15	V
		UC352xA	5	5.1	5.2	
Line regulation	V_{IN} = 8 V to 35 V			10	20	mV
Load regulation	I_L = 0 mA to 20 mA			20	50	mV
Temperature stability[1]	Over operating			20	50	mV
Total output variation[1]	Line, load, and temperature	UC152xA, UC252xA	5		5.2	V
		UC352xA	4.95		5.25	
Shorter circuit current	V_{REF} = 0, T_J = 25°C			80	100	mA
Output noise Voltage[1]	10 Hz ≤ 10 kHz, T_J = 25°C			40	200	µVrms
Long-term stability[1]	T_J = 125°C			20	50	mV
OSCILLATOR SECTION[2]						
Initial accuracy[1][2]	T_J = 25°C			2%	6%	
Voltage stability[1][2]	V_{IN} = 8 V to 35 V	UC152xA, UC252xA		0.3%	1%	
		UC352xA		1%	2%	
Temperature stability[1]	Over operating			3%	6%	
Minimum frequency	R_T = 200 kΩ, C_T = 0.1 mF				120	Hz
Maximum frequency	R_T = 2 kΩ, C_T = 470 pF		400			kHz
Current mirror	I_{RT} = 2 mA		1.7	2	2.2	mA
Clock amplitude[1][2]			3	3.5		V
Clock width[1][2]	T_J = 25°C		0.3	0.5	1	µs
Syncronization threshold[1][2]			1.2	2	2.8	V
Sync input current	Sync voltage = 3.5 V			1	2.5	mA
ERROR AMPLIFIER SECTION (V_{CM} = 5.1 V)						
Input offset voltage	UC152xA, UC252xA			0.5	5	mV
	UC352xA			2	10	

(1) These parameters, although ensured over the recommended operating conditions, are not 100% tested in production.
(2) Tested at f_{OSC} = 40 kHz (R_T = 3.6 kΩ, C_T = 0.01 mF, R_D = 0. Approximate oscillator frequency is defined by

$$f = \frac{1}{C_T\left(0.7R_T + 3R_D\right)}.$$

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input bias current			1	10	µA
Input offset current				1	
DC open loop gain	$R_L \geq 10$ MΩ	60	75		dB
Gain-bandwidth product(1)	A_V = 0 dB, T_J = 25°C	1	2		MHz
DC transconductance(1)(3)	T_J = 25°C, 30 kΩ ≤ R_L ≤ 1 MΩ	1.1	1.5		mS
Low-level output voltage			0.2	0.5	V
High-level output voltage		3.8	5.6		
Common mode rejection	V_{CM} = 1.5 V to 5.2 V	60	75		dB
Supply voltage rejection	V_{IN} = 8 V to 35 V	50	60		
PWM COMPARATOR					
Minimum duty-cycle				0%	
Maximum duty-cycle		45%	49%		
Input threshold(4)	Zero duty-cycle	0.7	0.9		V
	Maximum duty-cycle		3.3	3.6	
Input bias current(4)			0.05	1	µA
SHUTDOWN					
Soft-start current	V_{SD} = 0 V, V_{SS} = 0 V	25	50	80	µA
Soft-start low level	V_{SD} = 2.5 V		0.4	0.7	V
Shutdown threshold	To outputs, V_{SS} = 5.1 V, T_J = 25°C	0.6	0.8	1	
Shutdown input current	V_{SD} = 2.5 V		0.4	1	mA
Shutdown Delay(5)	V_{SD} = 2.5 V, T_J = 25°C		0.2	0.5	µS
OUTPUT DRIVERS (EACH OUTPUT) (V_C = 20 V)					
Low-level output voltage	I_{SINK} = 20 mA		0.2	0.4	V
	I_{SINK} = 100 mA		1	2	
High-level output voltage	I_{SOURCE} = 20 mA	18	19		V
	I_{SOURCE} = 100 mA	17	18		
Undervoltage lockout	V_{COMP} and V_{SS} = High	6	7	8	V
V_C OFF current(6)	V_C = 35 V			200	µA
Rise time(5)	C_L = 1 nF, T_J = 25°C		100	600	ns
Fall time(5)	C_L = 1 nF, T_J = 25°C		50	300	
TOTAL STANDBY CURRENT					
Supply current	V_{IN} = 35 V		14	20	mA

(3) DC transconductance (g_M) relates to DC open-loop voltage gain (A_V) according to the following equation: A_V = gMRL where R_L is the resistance from pin 9 to ground. The minimum g_M specification is used to calculate minimum A_V when the error amplifier output is loaded.
(4) Tested at f_{OSC} = 40 kHz (R_T = 3.6 kΩ, C_T = 0.01 mF, R_D = 0 Ω.
(5) These parameters, although ensured over the recommended operating conditions, are not 100% tested in production.
(6) Collector off-state quiescent current measured at pin 13 with outputs low for UC1525A and high for UC1527A.

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6.6 Typical Characteristics

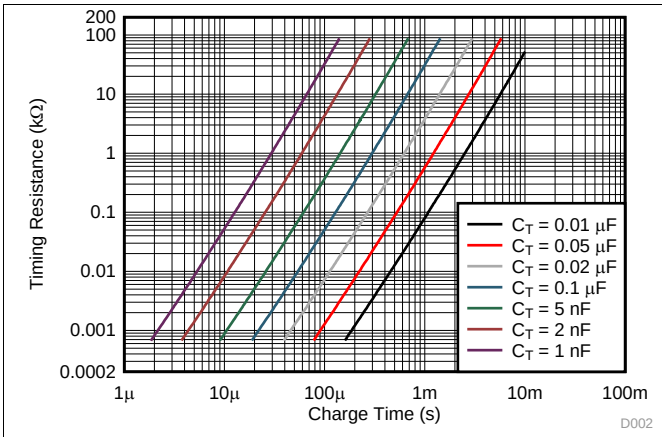


Figure 1. Oscillator Charge Time vs R_T and C_T

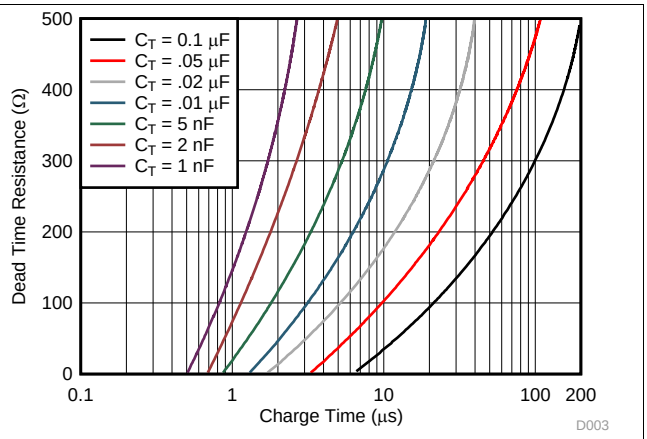


Figure 2. Oscillator Discharge Time vs R_T C_T

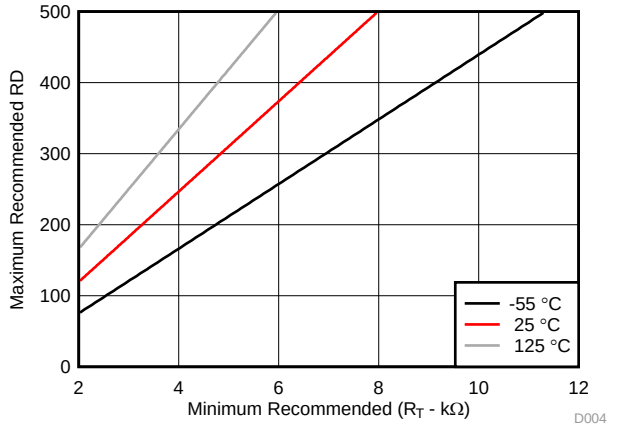


Figure 3. Maximum Value R_D vs Minimum Value R_T

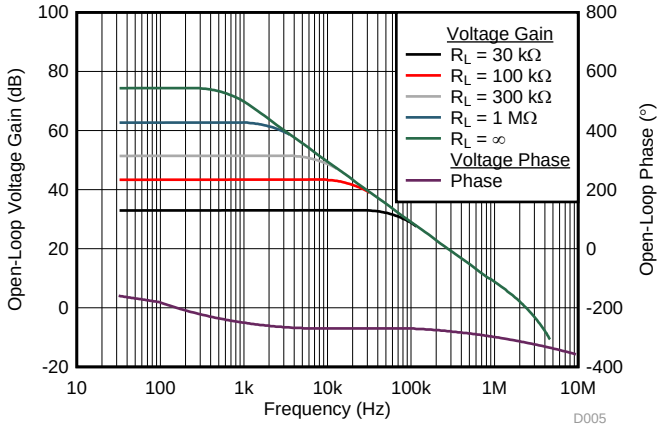


Figure 4. Error Amplifier Voltage Gain and Phase vs Frequency

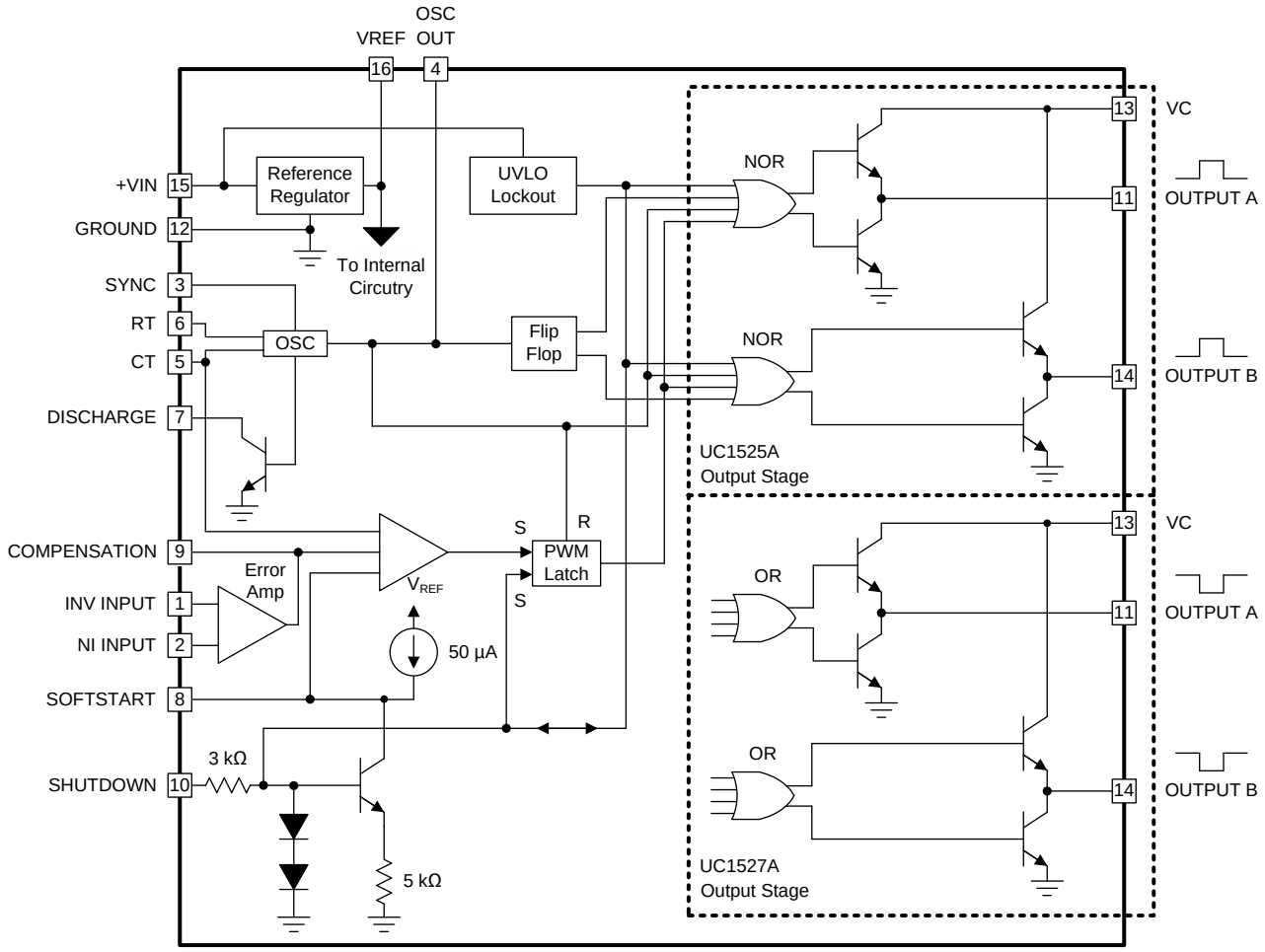
7 Detailed Description

7.1 Overview

The UCx52xA series of pulse width modulator integrated circuits are designed to offer improved performance and lowered external parts count when used in designing all types of switching power supplies. The on-chip 5.1-V reference is trimmed to 1% and the input common-mode range of the error amplifier includes the reference voltage, eliminating external resistors. A sync input to the oscillator allows multiple units to be slaved or a single unit to be synchronized to an external system clock. A single resistor between CT and the discharge terminals provides a wide range of dead-time adjustment. These devices also feature built-in soft-start circuitry with only an external timing capacitor required. A shutdown terminal controls both the soft-start circuitry and the output stages, providing instantaneous turn off through the PWM latch with pulsed shutdown, as well as soft-start recycle with longer shutdown commands.

These functions are also controlled by an undervoltage lockout which keeps the outputs off and the soft-start capacitor discharged for subnormal input voltages. This lockout circuitry includes approximately 500 mV of hysteresis for jitter-free operation. Another feature of these PWM circuits is a latch following the comparator. Once a PWM pulse has been terminated for any reason, the outputs will remain off for the duration of the period. The latch is reset with each clock pulse. The output stages are totem-pole designs capable of sourcing or sinking in excess of 200 mA. The UC1525A output stage features NOR logic, giving a LOW output for an OFF state. The UC1527A uses OR logic, which results in a HIGH output level when OFF.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Adjustable Dead-Time Control

A single resistor between CT and the discharge terminals provides a wide range of dead-time adjustment.

7.3.2 Soft Start

Soft start is achieved by connecting the soft-start pin to ground through a capacitor, charged by the 50-µA current source. See Functional Block Diagram.

7.3.3 Input Undervoltage Lockout With Hysteresis

The undervoltage lockout keeps the outputs off and the soft-start capacitor discharged for subnormal input voltages. This lockout circuitry includes approximately 500 mV of hysteresis for jitter-free operation.

7.3.4 Shutdown and Pulse-by-Pulse Current Limiting

See *Shutdown Options (See Functional Block Diagram)*.

7.4 Device Functional Modes

This device has no functional modes.

7.4.1 Shutdown Options (See *Functional Block Diagram*)

Since both the compensation and soft-start terminals have current source pullups, either can readily accept a pull-down signal which only has to sink a maximum of 100 A to turn off the outputs. This is subject to the added requirement of discharging whatever external capacitance may be attached to these pins.

An alternate approach is the use of the shutdown circuitry of the shutdown pin which has been improved to enhance the available shutdown options. Activating this circuit by applying a positive signal on the shutdown pin performs two functions; the PWM latch is immediately set providing the fastest turn-off signal to the outputs; and a 150-A current sink begins to discharge the external soft-start capacitor. If the shutdown command is short, the PWM signal is terminated without significant discharge of the soft-start capacitor, thus, allowing, for example, a convenient implementation of pulse-by-pulse current limiting. Holding the shutdown pin high for a longer duration, however, will ultimately discharge this external capacitor, recycling slow turnon upon release.

The shutdown pin should not be left floating as noise pickup could conceivably interrupt normal operation. All transitions of the voltage on the shutdown pin should be within the time frame of one clock cycle and not repeated at a frequency higher than 10 clock cycles.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The UC1525A/1527A series of pulse width modulator integrated circuits are designed to offer improved performance and lowered external parts count when used in designing all types of switching power supplies. The UC1525A output stage features NOR logic, giving a LOW output for an OFF state. The UC1527A utilizes OR logic which results in a HIGH output level when OFF.

8.2 Typical Application

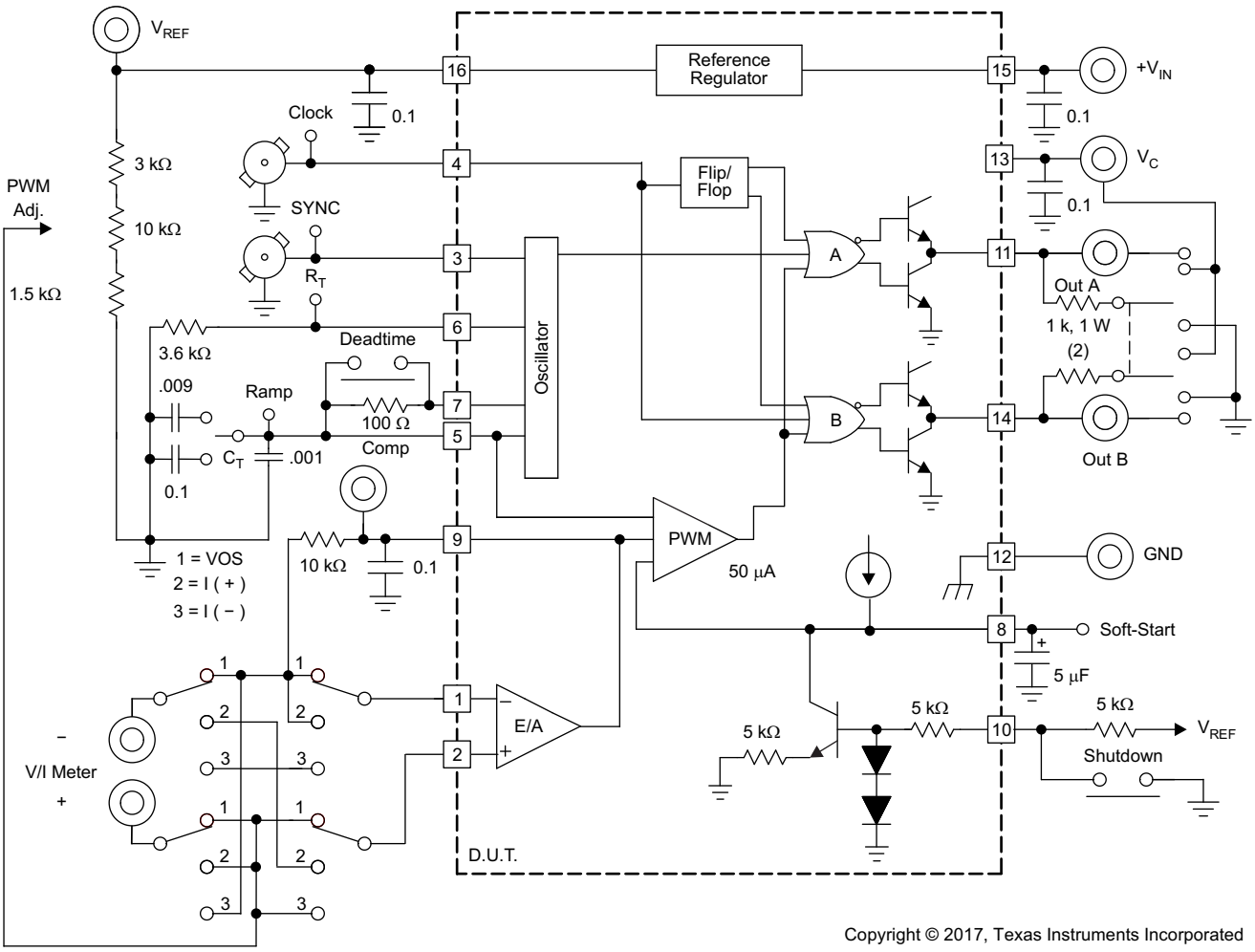

Figure 5. Lab Test Fixture

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Typical Application (continued)

8.2.1 Theory of Operation

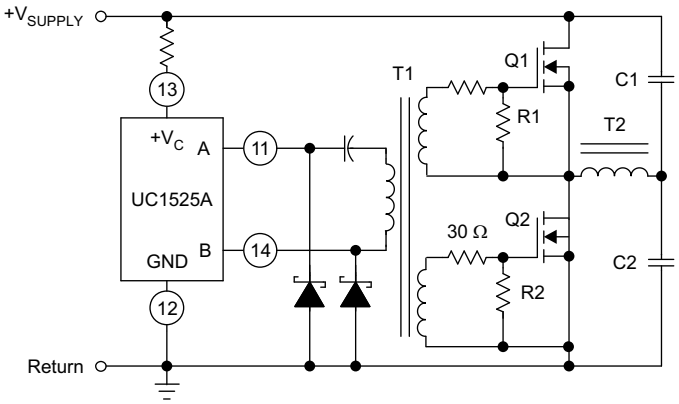

Figure 6. Low Power Transformers

Low power transformers can be driven by the UC1525A. Automatic reset occurs during dead time, when both ends of the primary winding are switched to ground.

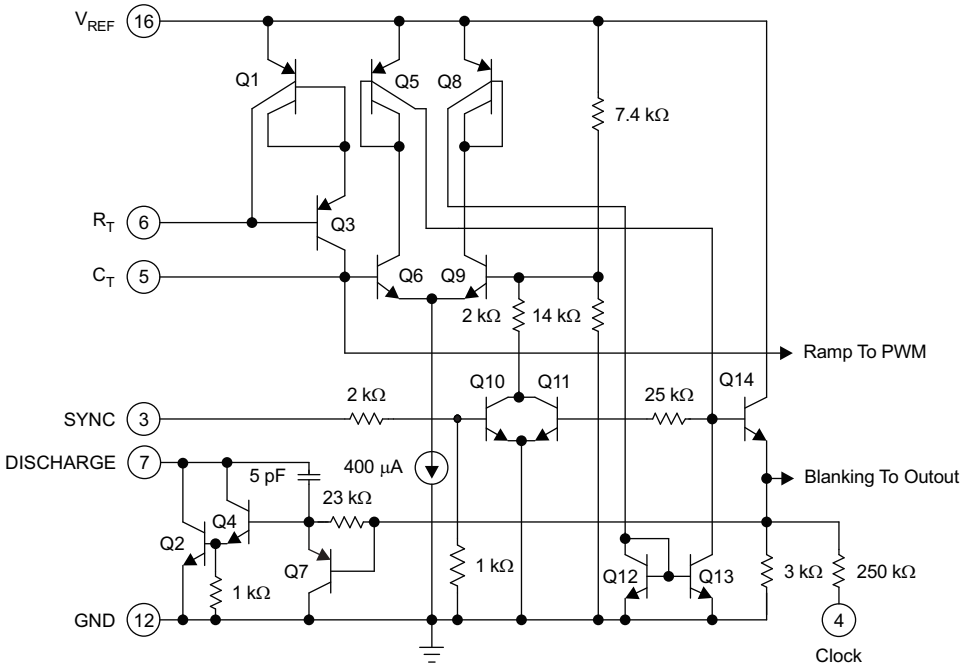

Figure 7. UC1525A Oscillator Schematic

Typical Application (continued)

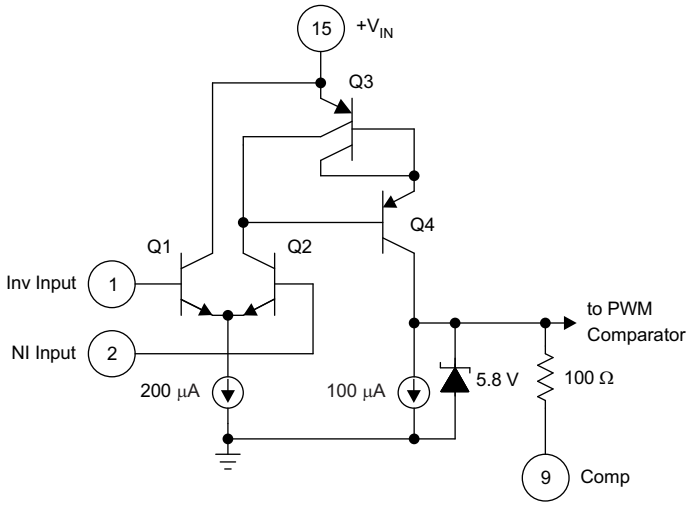

Figure 8. UC1525A Error Amplifier

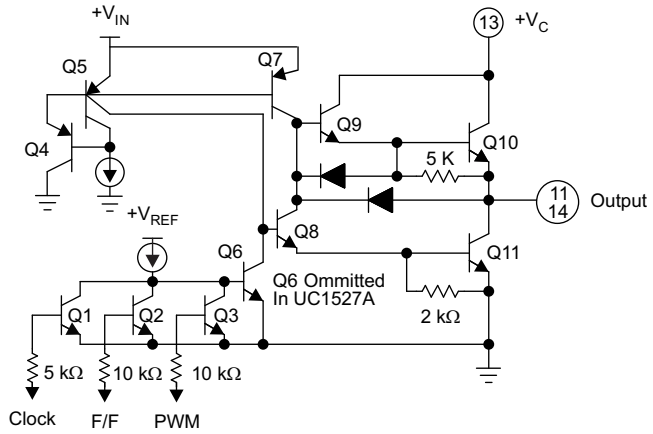

Figure 9. UC1525A Output Circuit (1/2 circuit shown)

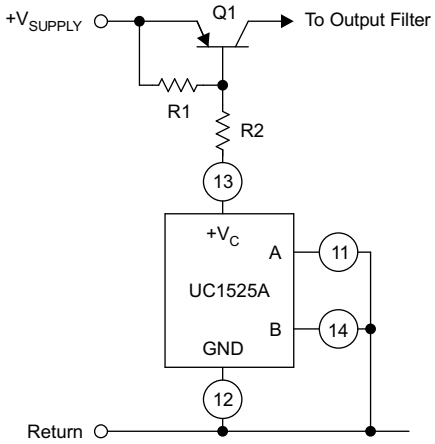

Figure 10. Grounded Driver Outputs For Single-Ended Supplies

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Typical Application (continued)

For single-ended supplies, the driver outputs are grounded. The V_C terminal is switched to ground by the totem-pole source transistors on alternate oscillator cycles.

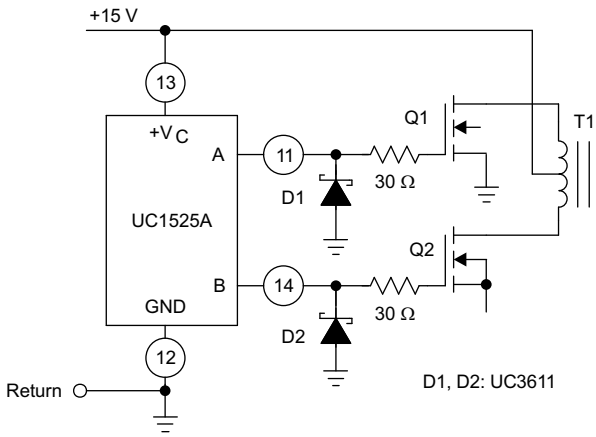

Figure 11. Output Drivers With Low Source Impedance

The low source impedance of the output drivers provides rapid charging of power FET input capacitance while minimizing external components.

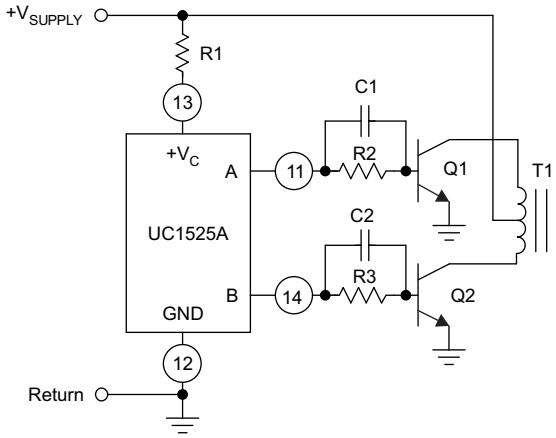

Figure 12. Conventional Push-Pull Bipolar Design

In conventional push-pull bipolar designs, forward base drive is controlled by R1–R3. Rapid turn-off times for the power devices are achieved with speed-up capacitors C1 and C2.

8.2.2 Design Requirements

This example illustrates the design process and component selection for a push-pull DC-DC converter utilizing the UC1525A. The converter regulates a 30-V input to a 5-V output with 10-A maximum load.

Table 1. Design Parameters

PARAMETER		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range	25	30	35	V
V_{OUT}	Output voltage		5		V
i_{OUT}	Output current	1		10	A
f_O	Oscillator frequency		100		kHz
f_S	Switching frequency		50		kHz

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8.2.3 Detailed Design Procedure

8.2.3.1 Timing Resistor and Capacitor Selection

Generally, higher switching frequency gives smaller size but have higher switching loss. Operation at 100 kHz was selected in this example as a reasonable compromise between size and efficiency. The value of R_T = 10 kΩ, C_T = 1.37 nF and R_D = 100 Ω were chosen for 100-kHz oscillator frequency based on equation:

$$f = \frac{1}{C_T(0.7\,R_T + 3\,R_D)} \tag{1}$$

8.2.3.2 Turns Ratio Selection

The maximum primary-to-secondary turns ratio N_{MAX} can be determined by the target output voltage, minimum input voltage, and the estimated maximum duty cycle. D_{LIM} = 0.35 was selected for this example. N_{MAX} can be calculated using Equation 1.

$$N_{MAX} = \frac{2 \times D_{LIM} \times V_{IN(min)}}{V_{OUT} + V_F} = \frac{2 \times 0.35 \times 25\,V}{5\,V + 0.3\,V} = 3.3 \tag{2}$$

Rounding N_{MAX} down to the next lowest integer results in a turns ratio of N = 3.

8.2.3.3 Inductor Selection

The maximum inductor ripple current occurs at the maximum input voltage. Typically, 20% to 40% of the full load current ripple is a good compromise between core loss and copper loss of the inductor. Higher ripple current allows for a smaller inductor size, but places more burden on the output capacitor to smooth the ripple voltage on the output. In this example, a ripple current of 25% of 10 A was chosen. The inductor value can be calculated as:

$$L_O = \frac{V_{OUT} + V_F}{\Delta I_L \times f_{SW}} \times \left(\frac{1}{2} - \frac{N \times (V_{OUT} + V_F)}{2 \times V_{IN(max)}}\right) = 11.57\,\mu H \tag{3}$$

8.2.3.4 Rectification Diode Selection

A rectification diode should always possess low-forward voltage drop. When used in high-frequency switching applications, the diode must also possess a short recovery time. Schottky diodes meet both requirements and are therefore strongly recommended in push-pull converter designs.

8.2.3.5 VC Capacitor Selection

The primary purpose of the VC capacitor is to supply the peak transient currents of the drivers as well as provide stability for the VC regulator. These peak currents can be several amperes. The recommended value of VC capacitor should be no smaller than 0.1 μF, and should be a good quality, low ESR, ceramic capacitor. VC capacitor should be placed as close as possible to the VC pin to minimize potentially damaging voltage transients caused by trace inductance.

8.2.3.6 Output Capacitor Selection

The output capacitors smooth the output voltage ripple caused by inductor ripple current and provide a source of charge during load transient conditions.

8.2.3.7 Input Capacitor Selection

The input supply voltage typically has high source impedance at the switching frequency. Good quality input capacitors are necessary to limit the ripple voltage at the VIN pin while supplying most of the switch current during the on-time. The input capacitor should be selected for RMS current rating and minimum ripple voltage.

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8.2.4 Application Curves

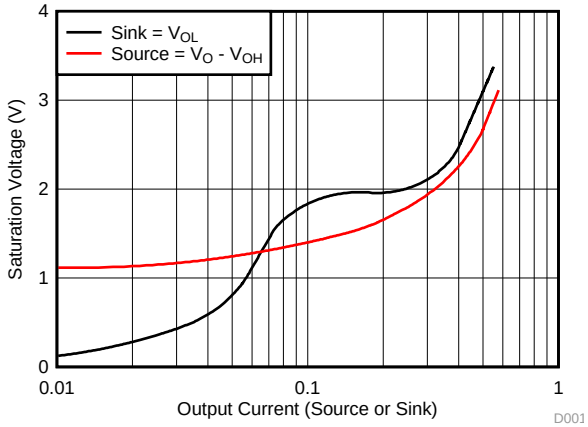

Figure 13. UC1525A Output Saturation Characteristics

9 Power Supply Recommendations

The voltage range for V_{IN} is 8 V to 35 V.

The voltage range for V_C is 4.5 V to 35 V. Choose a voltage level which is suitable for the power switch, for example, 12 V for MOSFET.

10 Layout

10.1 Layout Guidelines

High-speed circuits demand careful attention to layout and component placement. To assure proper performance of the UC1525A follow these rules:

- Use a ground plane
- Damp or clamp parasitic inductive kick energy from the gate of driven MOSFETs. Do not allow the output pins to ring below ground. A series gate resistor or a shunt 1-A Schottky diode at the output pin will serve this purpose.
- Bypass V_{IN}, V_C, and V_{REF}. Use 0.1-µF monolithic ceramic capacitors with low equivalent series inductance. Allow less than 1 cm of total lead length for each capacitor between the bypassed pin and the ground plane.
- Treat the timing capacitor, C_T, like a bypass capacitor.

10.2 Layout Example

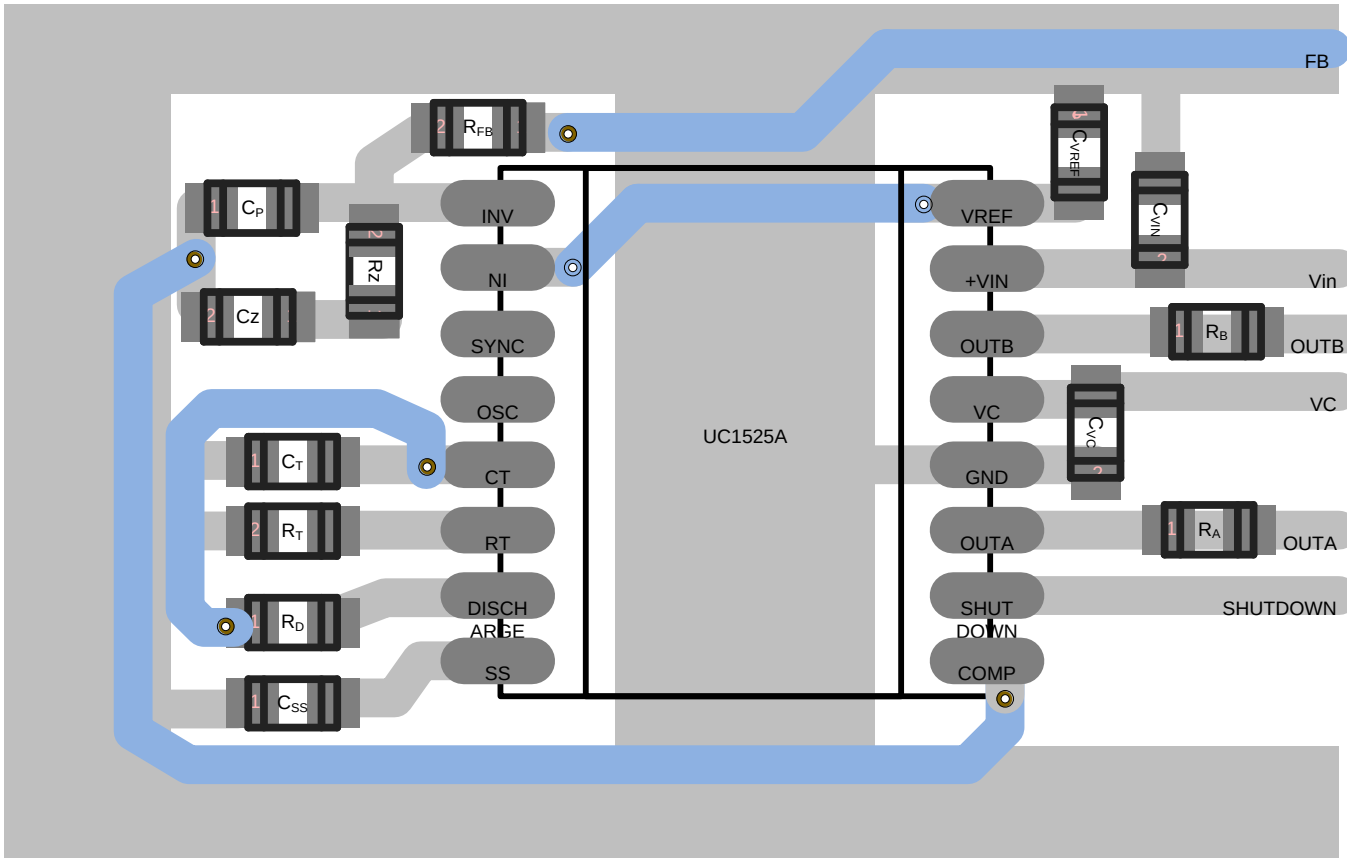

Figure 14. UC1525A Layout Example

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11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

Switching Power Supply Topology Voltage Mode vs Current Mode (SLUA119)

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
UC1525A	Click here	Click here	Click here	Click here	Click here
UC1527A	Click here	Click here	Click here	Click here	Click here
UC2525A	Click here	Click here	Click here	Click here	Click here
UC2527A	Click here	Click here	Click here	Click here	Click here
UC3525A	Click here	Click here	Click here	Click here	Click here
UC3527A	Click here	Click here	Click here	Click here	Click here

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-89511032A	NRND	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-89511032A UC1525AL/883B
5962-8951103EA	NRND	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8951103EA UC1525AJ/883B
5962-8951104EA	NRND	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8951104EA UC1527AJ/883B
UC1525AJ	NRND	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	UC1525AJ
UC1525AJ.A	NRND	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	UC1525AJ
UC1525AJ883B	NRND	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8951103EA UC1525AJ/883B
UC1525AJ883B.A	NRND	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8951103EA UC1525AJ/883B
UC1525AL	NRND	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	UC1525AL
UC1525AL.A	NRND	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	UC1525AL
UC1525AL883B	NRND	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-89511032A UC1525AL/883B
UC1525AL883B.A	NRND	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-89511032A UC1525AL/883B
UC1527AJ	NRND	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	UC1527AJ
UC1527AJ.A	NRND	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	UC1527AJ
UC1527AJ883B	NRND	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8951104EA UC1527AJ/883B
UC1527AJ883B.A	NRND	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8951104EA UC1527AJ/883B
UC2525ADW	Obsolete	Production	SOIC (DW) | 16	-	-	Call TI	Call TI	-25 to 85	UC2525ADW
UC2525ADWTR	NRND	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	UC2525ADW
UC2525ADWTR.A	NRND	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	UC2525ADW

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UC2525AJ	NRND	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-25 to 85	UC2525AJ
UC2525AJ.A	NRND	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-25 to 85	UC2525AJ
UC2525AN	NRND	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-25 to 85	UC2525AN
UC2525AN.A	NRND	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-25 to 85	UC2525AN
UC2525ANG4	NRND	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-25 to 85	UC2525AN
UC2525BDW	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	UC2525BDW
UC2525BDW.A	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	UC2525BDW
UC2525BN	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-25 to 85	UC2525BN
UC2525BN.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-25 to 85	UC2525BN
UC2527AN	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	UC2527AN
UC2527AN.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	UC2527AN
UC3525ADW	NRND	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3525ADW
UC3525ADW.A	NRND	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3525ADW
UC3525ADWG4	NRND	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3525ADW
UC3525ADWTR	NRND	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3525ADW
UC3525ADWTR.A	NRND	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3525ADW
UC3525ADWTRG4	NRND	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3525ADW
UC3525AJ	NRND	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	0 to 70	UC3525AJ
UC3525AJ.A	NRND	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	0 to 70	UC3525AJ
UC3525AN	NRND	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UC3525AN
UC3525AN.A	NRND	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UC3525AN
UC3525ANG4	NRND	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UC3525AN
UC3527AN	NRND	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UC3527AN
UC3527AN.A	NRND	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UC3527AN
UC3527ANG4	NRND	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UC3527AN

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF UC1525A, UC1527A, UC2525A, UC2525AM, UC3525A, UC3525AM, UC3527A :

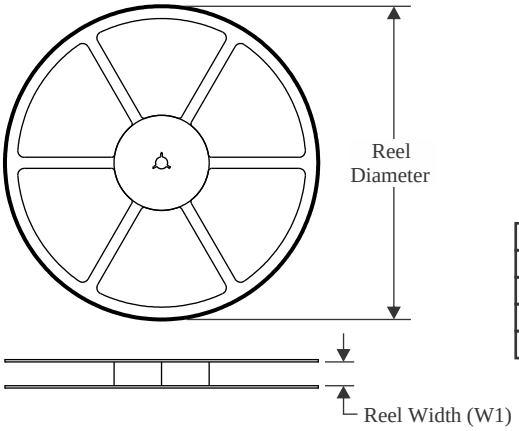
- Catalog : UC3525A, UC3527A, UC2525A, UC3525AM, UC3525A
- Military : UC2525AM, UC1525A, UC1525A, UC1527A

NOTE: Qualified Version Definitions:

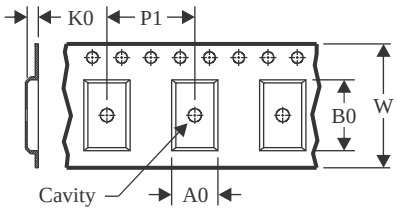
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

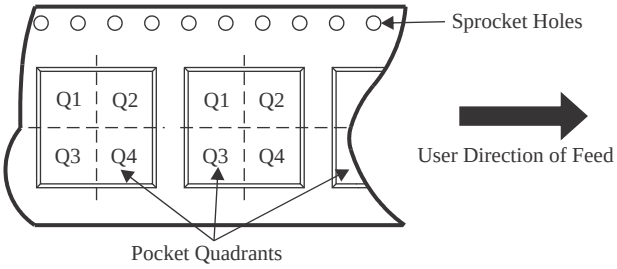


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

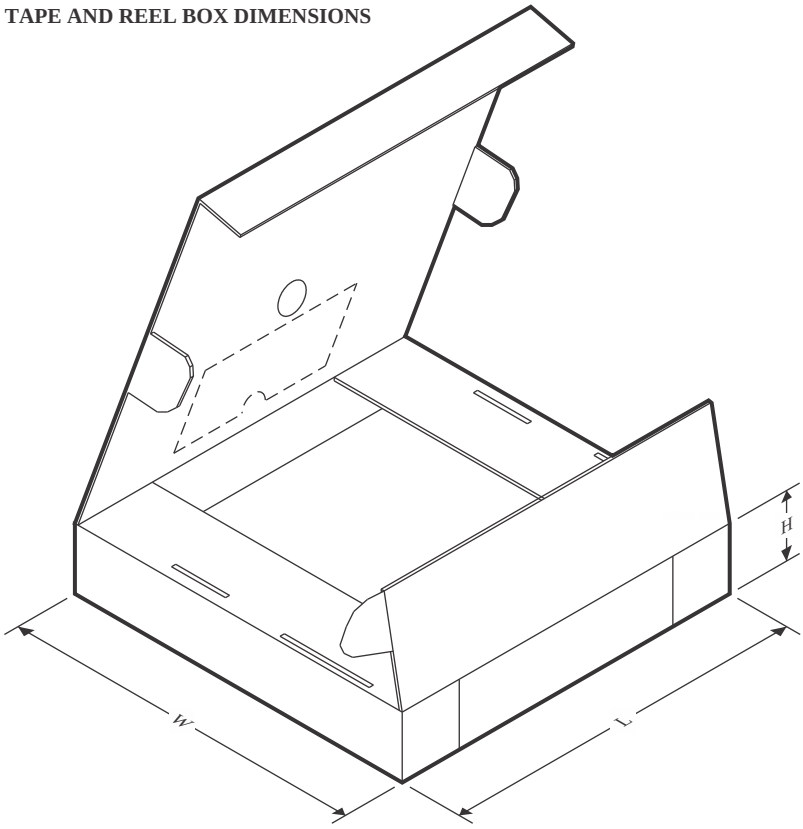
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2525ADWTR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
UC3525ADWTR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

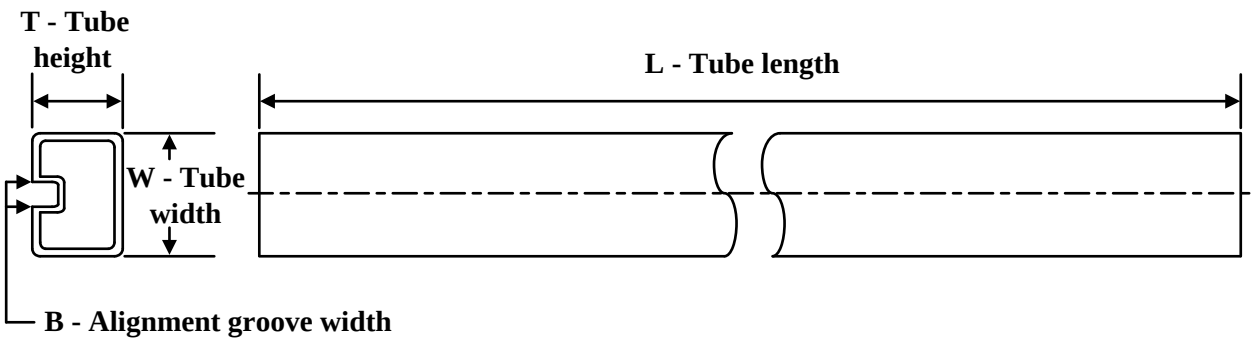
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2525ADWTR	SOIC	DW	16	2000	353.0	353.0	32.0
UC3525ADWTR	SOIC	DW	16	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-89511032A	FK	LCCC	20	55	506.98	12.06	2030	NA
UC1525AL	FK	LCCC	20	55	506.98	12.06	2030	NA
UC1525AL.A	FK	LCCC	20	55	506.98	12.06	2030	NA
UC1525AL883B	FK	LCCC	20	55	506.98	12.06	2030	NA
UC1525AL883B.A	FK	LCCC	20	55	506.98	12.06	2030	NA
UC2525AN	N	PDIP	16	25	506	13.97	11230	4.32
UC2525AN.A	N	PDIP	16	25	506	13.97	11230	4.32
UC2525ANG4	N	PDIP	16	25	506	13.97	11230	4.32
UC2525BDW	DW	SOIC	16	40	507	12.83	5080	6.6
UC2525BDW.A	DW	SOIC	16	40	507	12.83	5080	6.6
UC2525BN	N	PDIP	16	25	506	13.97	11230	4.32
UC2525BN.A	N	PDIP	16	25	506	13.97	11230	4.32
UC2527AN	N	PDIP	16	25	506	13.97	11230	4.32
UC2527AN.A	N	PDIP	16	25	506	13.97	11230	4.32
UC3525ADW	DW	SOIC	16	40	507	12.83	5080	6.6
UC3525ADW.A	DW	SOIC	16	40	507	12.83	5080	6.6
UC3525ADWG4	DW	SOIC	16	40	507	12.83	5080	6.6
UC3525AN	N	PDIP	16	25	506	13.97	11230	4.32
UC3525AN.A	N	PDIP	16	25	506	13.97	11230	4.32
UC3525ANG4	N	PDIP	16	25	506	13.97	11230	4.32
UC3527AN	N	PDIP	16	25	506	13.97	11230	4.32
UC3527AN.A	N	PDIP	16	25	506	13.97	11230	4.32
UC3527ANG4	N	PDIP	16	25	506	13.97	11230	4.32

GENERIC PACKAGE VIEW

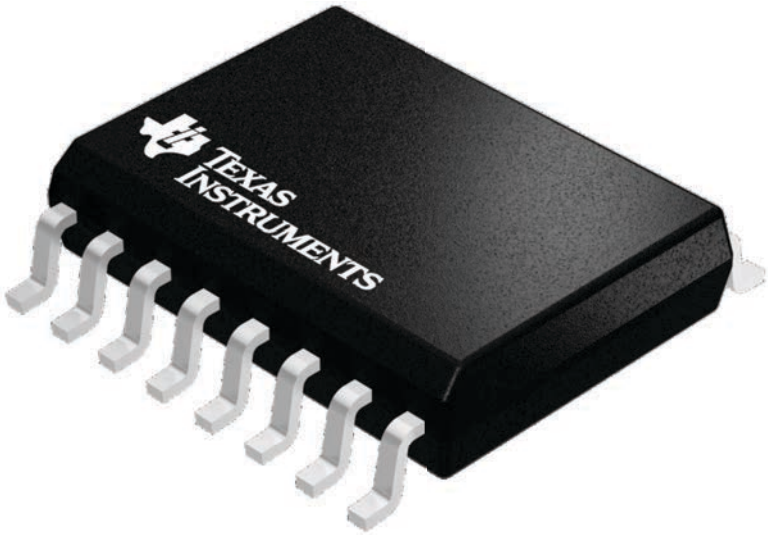
DW 16

SOIC - 2.65 mm max height

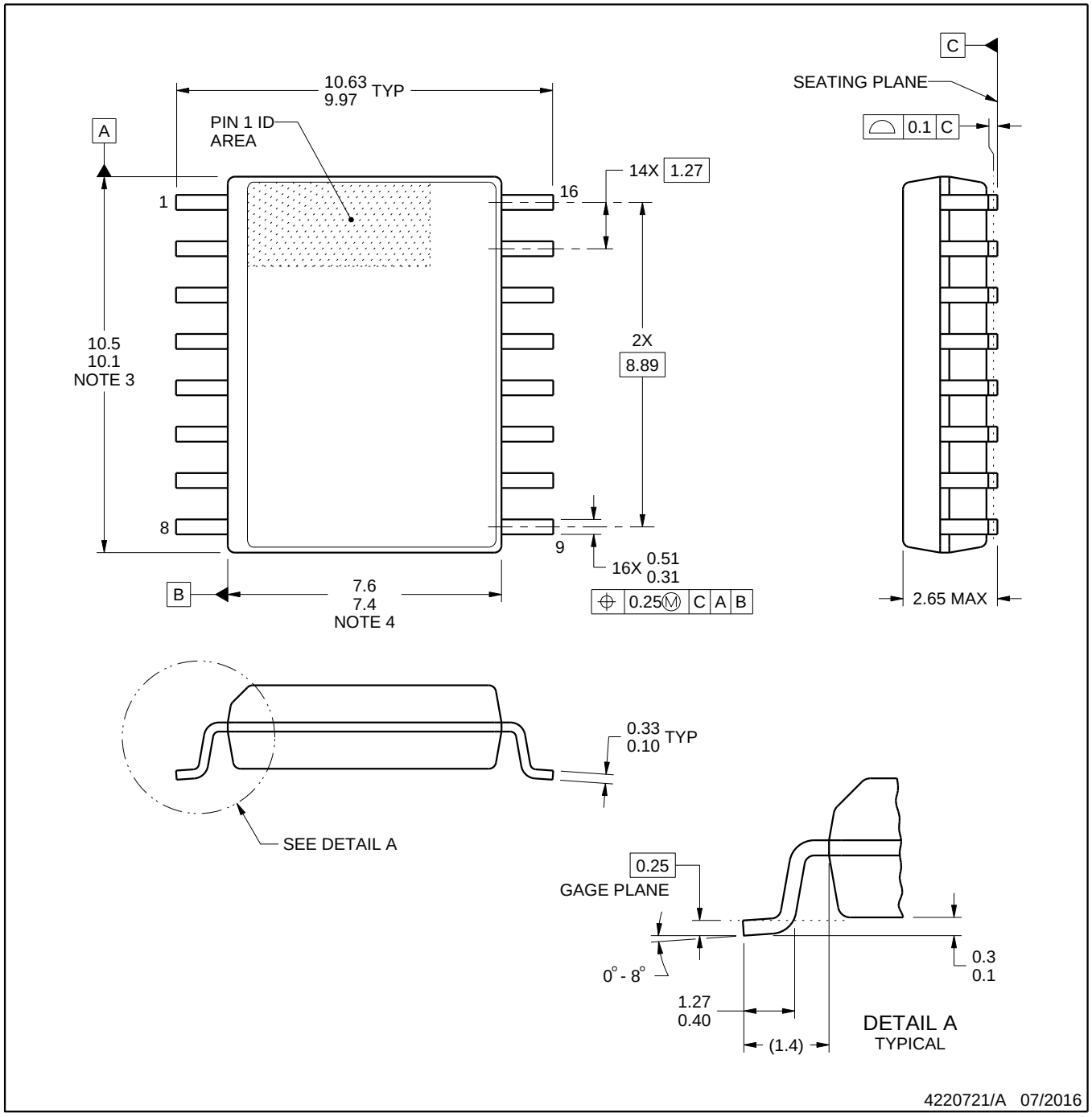
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

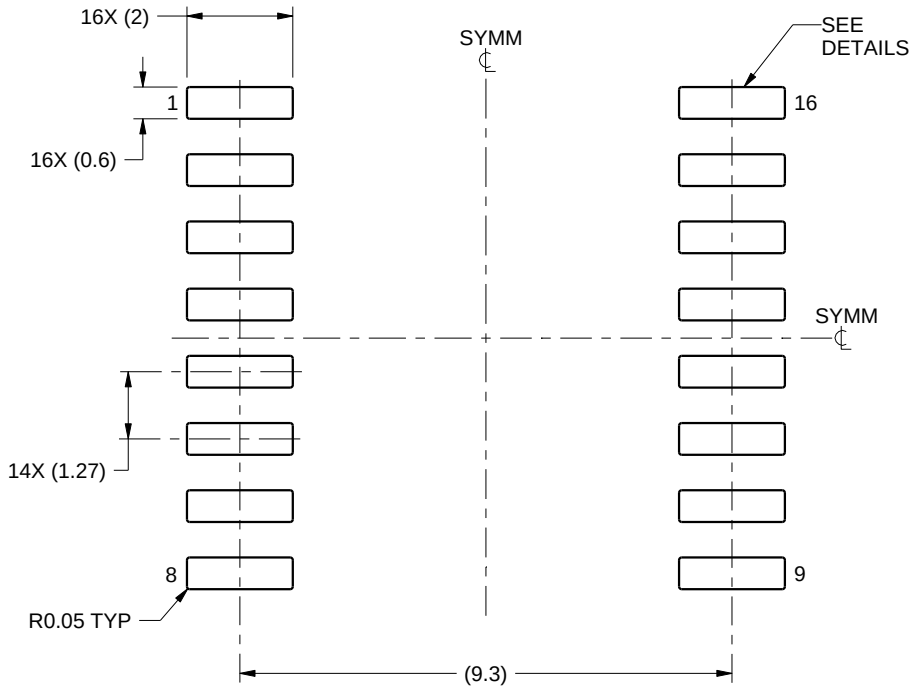


4224780/A

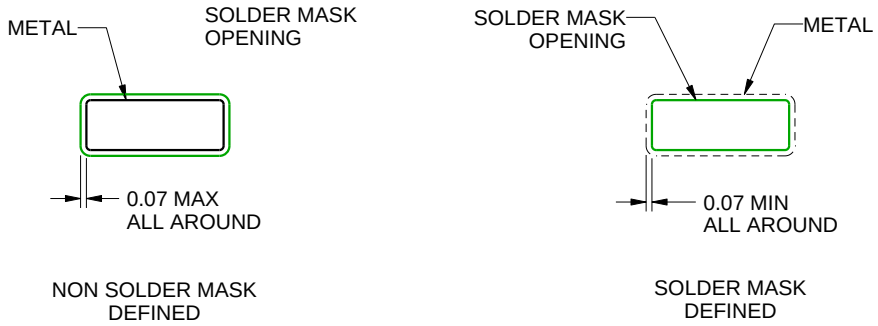


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

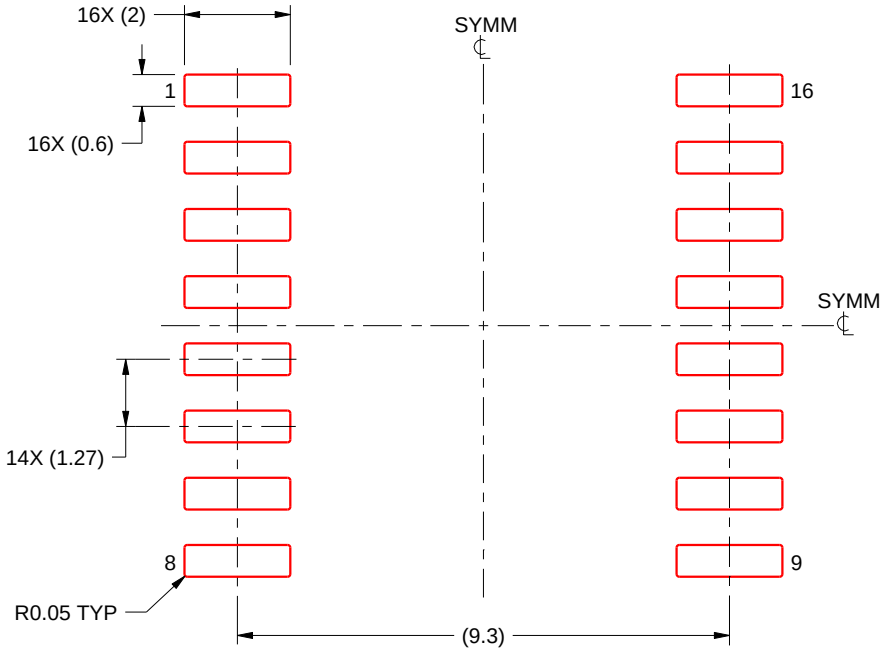


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

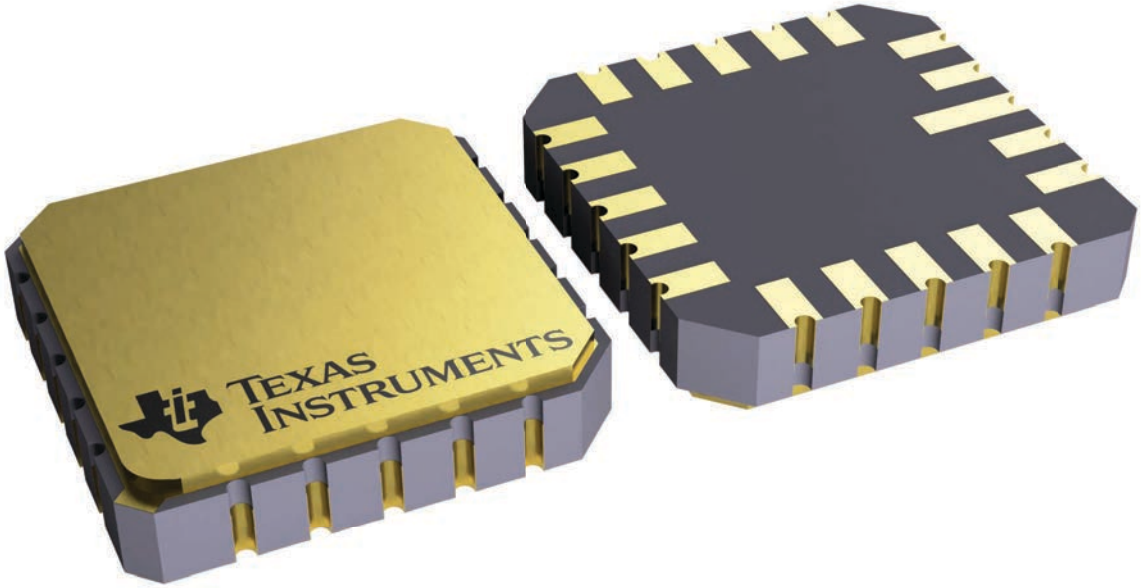
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

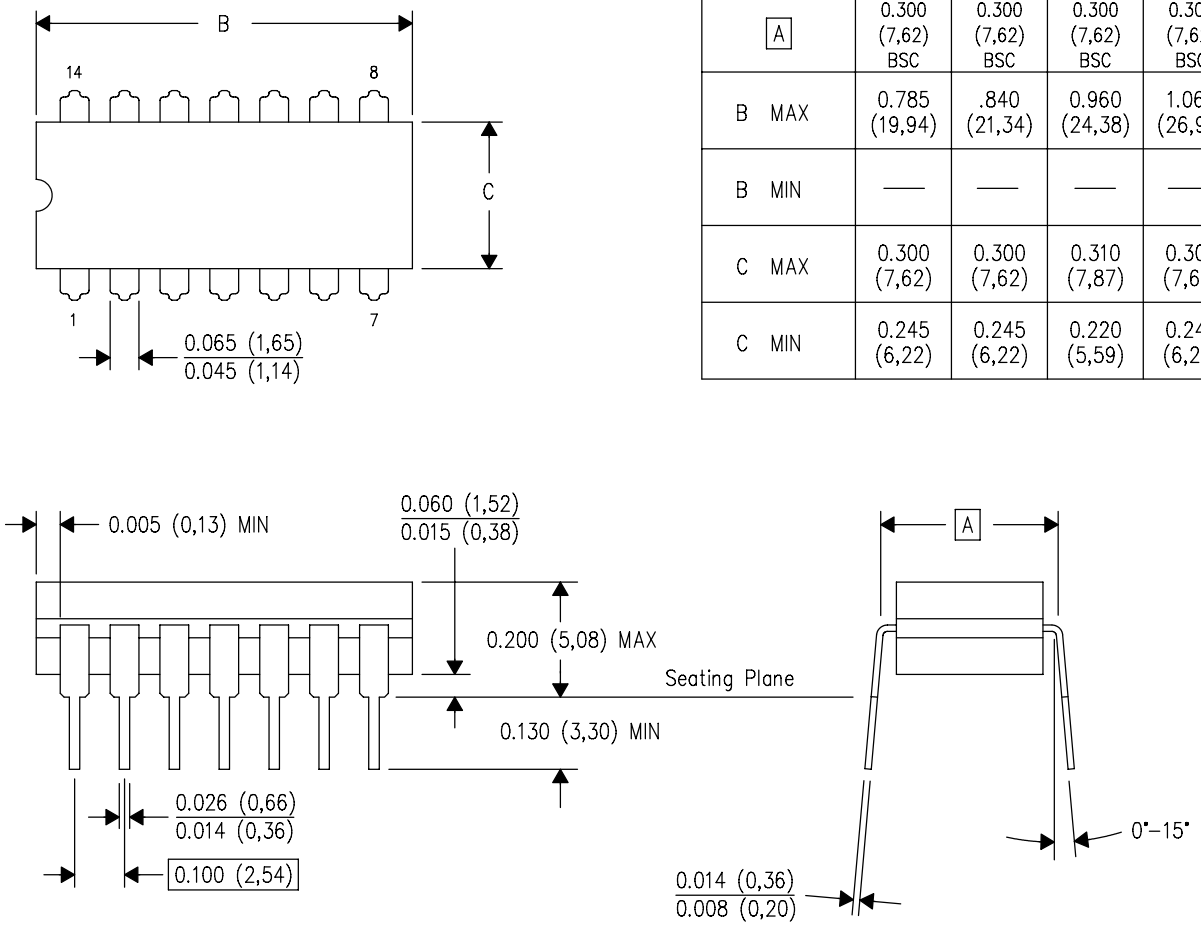
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

J (R–GDIP–T**) CERAMIC DUAL IN–LINE PACKAGE

14 LEADS SHOWN



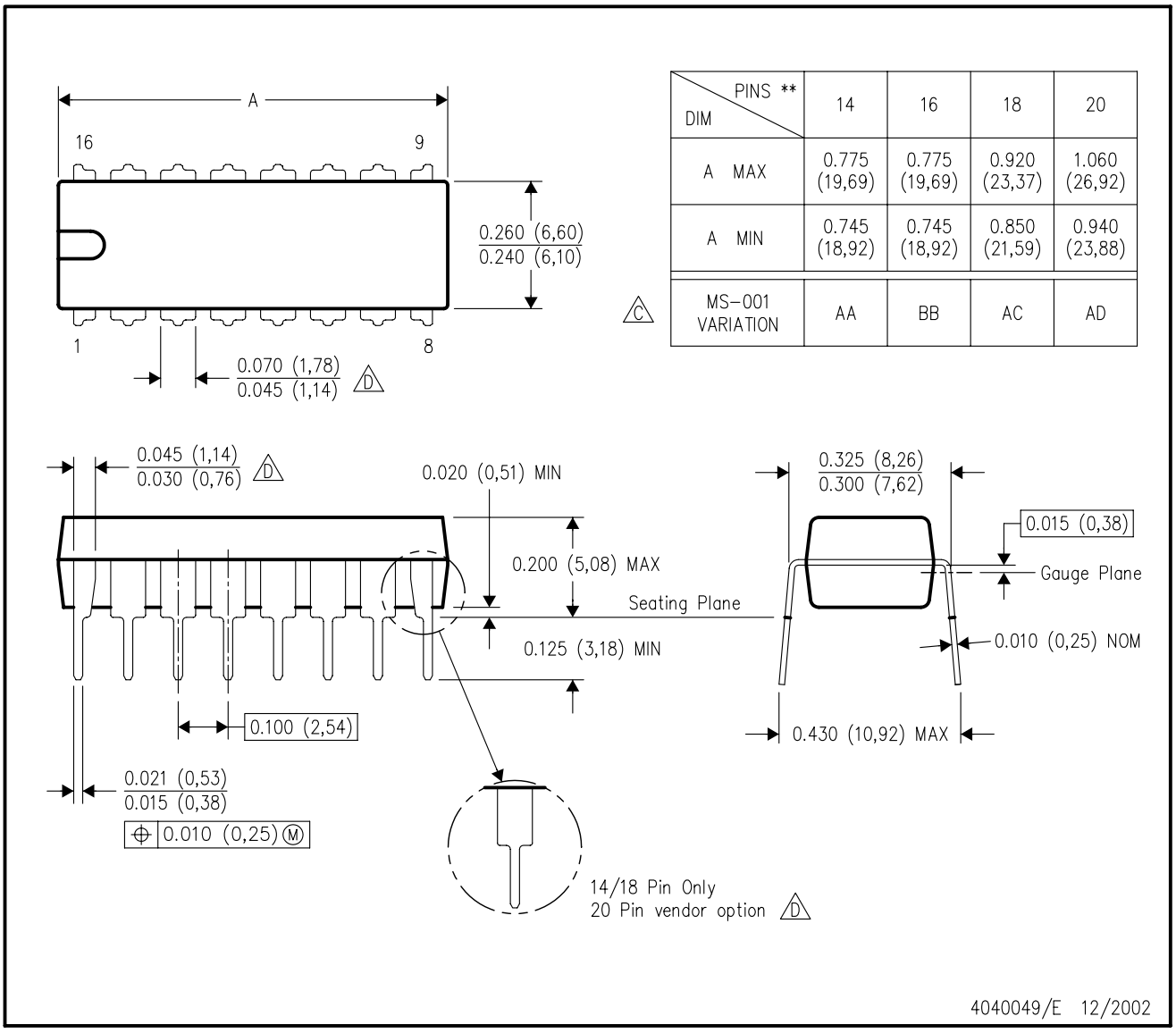
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

4040083/F 03/03

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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