UCx84xA Current-Mode PWM Controller

1 Features

- Optimized for Off-Line and DC-DC Converters
- Low Start-Up Current (< 0.5mA)
- Trimmed Oscillator Discharge Current
- Automatic Feedforward Compensation
- Pulse-by-Pulse Current Limiting
- Enhanced Load Response Characteristics
- Undervoltage Lockout With Hysteresis
- Double Pulse Suppression
- High-Current Totem Pole Output
- Internally-Trimmed Bandgap Reference
- Up to 500kHz Operation
- Create a Custom Design Using the UCx84xA With the WEBENCH® Power Designer

2 Applications

- Switch Mode Power Supplies (SMPS)
- DC-DC Converters
- Power Modules
- Industrial PSU
- Battery Operated PSU

3 Description

The UCx84xA family of control devices is a pin-for-pin compatible improved version of the UCx84x family. Providing the necessary features to control current-mode or switched-mode power supplies, this family of devices has many improved features: startup current is less than 0.5mA, oscillator discharge is trimmed to 8.3mA, and during UVLO, the output stage can sink at least 10mA at less than 1.2V for V_{CC} over 5V.

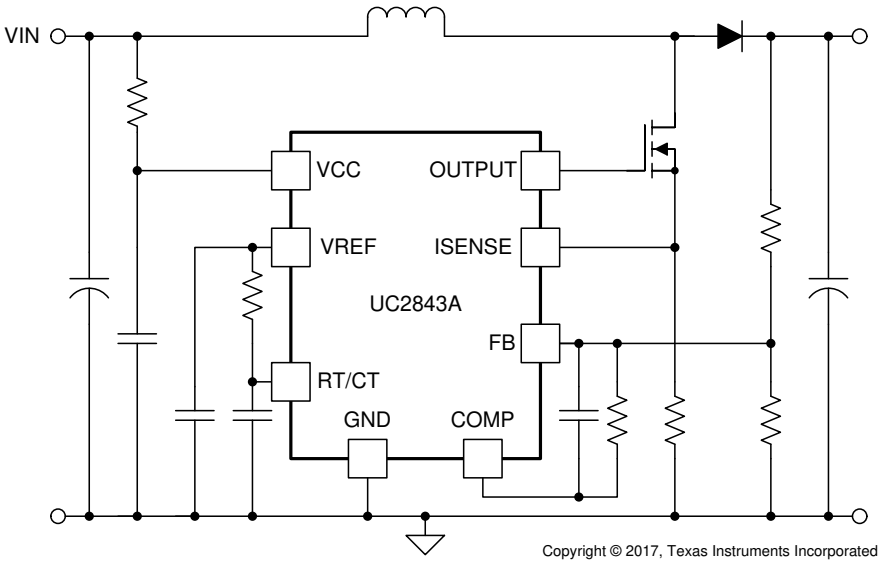
Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
UC1842A, UC1843A, UC1844A, UC1845A	JG (CDIP, 8)	6.67mm × 9.60mm
	FK (LCCC, 20)	8.89mm × 8.89mm
UC2843A	FN (PLCC, 20)	9.90mm × 9.90mm
UC2842A, UC2843A, UC2844A, UC2845A, UC3842A, UC3843A, UC3844A, UC3845A	P (PDIP, 8)	9.81mm × 9.43mm
	D (SOIC, 8)	4.90mm × 6.00mm
	D (SOIC, 14)	8.65mm × 6.00mm
	DW (SOIC, 16)	10.30mm × 10.30mm

(1) For more information, see Section 12.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

Device Comparison Table

DEVICE	UVLO ON	UVLO OFF	MAX DUTY CYCLE
UC1842A	16V	10V	<100%
UC1843A	8.4V	7.6V	<100%
UC1844A	16V	10V	<50%
UC1845A	8.4V	7.6V	<50%



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Simplified Application Diagram

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4 Pin Configuration and Functions

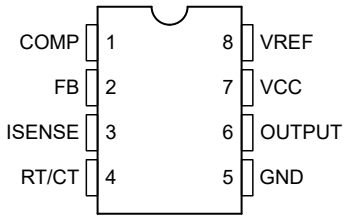


Figure 4-1. CDIP, PDIP, and SOIC Packages, 8-Pin JG, P, and D (Top View)

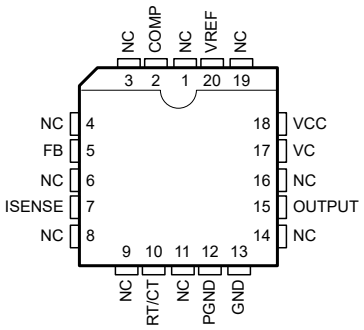


Figure 4-2. LCCC and PLCC Packages, 20-Pin FK and FN (Top View)

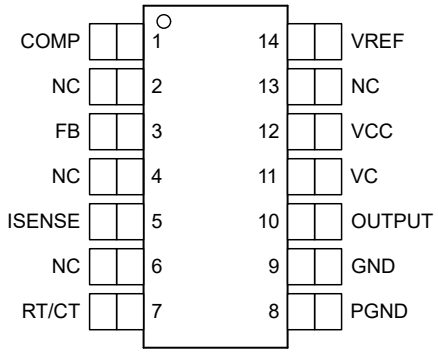


Figure 4-3. SOIC Package, 14-Pin D (Top View)

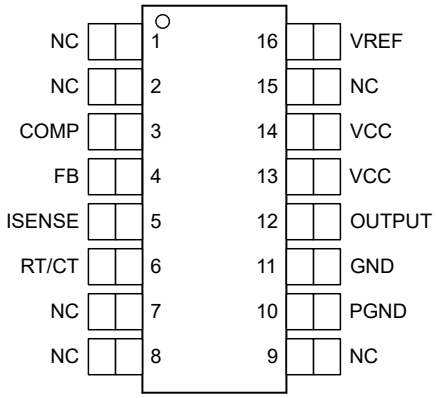


Figure 4-4. SOIC Package, 16-Pin DW (Top View)

Table 4-1. Pin Functions

PIN					Type (1)	DESCRIPTION
NAME	NO.					
	CDIP (8), PDIP (8), SOIC (8)	LCCC (20), PLCC (20)	SOIC (14)	SOIC (16)		
COMP	1	2	1	3	O	Outputs the low impedance 1-MHz internal error amplifier that is also the input to the peak current limit or PWM comparator, with an open-loop gain (AVOL) of 80 dB. This pin is capable of sinking a maximum of 6 mA and is not internally current limited.
FB	2	5	3	4	I	Input to the error amplifier that can be used to control the power converter voltage-feedback loop for stability.
GND	5	13	9	11	—	This is the controller signal ground.
ISENSE	3	7	5	5	I	Input to the peak current limit, PWM comparator of the UCx84xA controllers. When used in conjunction with a current sense resistor, the error amplifier output voltage controls the power systems cycle-by-cycle peak current limit. The maximum peak current sense signal is internally clamped to 1 V. See *Section 6.2*.
OUTPUT	6	15	10	12	O	Output of 1-A totem pole gate driver. This pin can sink and source up to 1 A of gate driver current. A gate driver resistor must be used to limit the gate driver current.
PGND	—	12	8	10	—	Power ground and the gate driver return. For devices that have this pin, star grounding techniques can be used to redirect the gate driver current away from the signal ground pin (GND). This technique can reduce PWM controller instabilities caused by gate driver return current.
RT/CT	4	10	7	6	I	Input to the internal oscillator that is programmed with an external timing resistor (RT) and timing capacitor (CT). See *Section 6.3.5* for information on properly selecting these timing components. TI recommends using capacitance values from 470 pF to 4.7 nF. TI also recommends that the timing resistor values chosen be from 5 kΩ to 100 kΩ.
VC	—	17	11	—	I	Bias input to the gate driver. For PWM controllers that do not have this pin, the gate driver is biased from the VCC pin. This pin must have a biasing capacitor that is at least 10 times greater than the gate capacitance of the main switching FET used in the design.
VCC	7	18	12	13, 14	I	Bias input to the gate driver. This pin must have a biasing capacitor that is at least 10 times greater than the gate capacitance of the main switching FET used in the design.
VREF	8	20	14	15	O	Reference voltage output of the PWM controller. This pin must supply no more than 10 mA under normal operation. This output is short-circuit protected at roughly 100 mA. This reference is also used for internal comparators and needs a high frequency bypass capacitor of 1 µF. The VCC capacitor also must be at least 10 times greater than the capacitor on the VREF pin.
NC	—	1, 3, 4, 6, 8, 9, 11, 14, 16, 19	2, 4, 6, 13	1, 2, 7, 8, 9, 16	—	No connection

(1) I = Input; O = Output

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage (low impedance source)	VCC pin		30	V
Output current, I_{OUT}			±1	A
Output energy (capacitive load)			5	µJ
Analog inputs		–0.3	6.3	V
Maximum negative voltage	All pins	–0.3		V
Differential voltage between VC and VCC	VC pin	–0.3		V
Error amplifier output sink current, I_{COMP}			10	mA
Power dissipation at $T_A \leq 25°C$			1	W
Lead temperature (soldering, 10 s)			300	°C
Junction temperature, T_J		–55	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Bias supply voltage	VCC pin		11		V
V_{FB}, V_{RC}, V_{VFB}	Voltage on analog pins	FB, ISENSE, and RT/CT pins	–0.1		5	V
V_{OUT}	Gate driver output voltage		–0.1		V_{CC}	V
I_{VCC}	Supply bias current				25	mA
I_{VREF}	Output current	VREF pin			10	mA
f_{OSC}	Oscillator frequency				500	kHz
T_A	Operating free-air temperature	UC184xA	–55		125	°C
		UC284xA	–40		85	
		UC384xA	0		70	

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5.4 Thermal Information

THERMAL METRIC[1]		UC184xA		UC2843A	UC284xA, UC384xA				UNIT
		JG (CDIP)	FK (LCCC)	FN (PLCC)	P (PDIP)	D (SOIC)	D (SOIC)	DW (SOIC)	
		8 PINS	20 PINS	20 PINS	8 PINS	8 PINS	14 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	—	—	56.7	74.1	117.4	87.9	73.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	64	36.2	34.6	63.4	51.5	42.2	35	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	92.5	35.4	21.8	50.5	61	44.7	38.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	—	—	10.4	34.6	7.8	8.8	9.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	—	—	21.5	49.2	60.2	44.3	37.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	15.1	4.1	—	—	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

Unless otherwise stated, these specifications apply for T_A = –55°C to 125°C (UC184xA), T_A = –40°C to 125°C (UC284xAQ), T_A = –40°C to 85°C (UC284xA), T_A = 0°C to 70°C (UC384xA); $T_A = T_J$; V_{CC} = 15 V[4]; R_T = 10 kΩ; C_T = 3.3 nF.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
REFERENCE						
Output voltage	T_J = 25°C, I_O = 1 mA	UC184xA, UC284xA	4.95	5	5.05	V
		UC384xA	4.9	5	5.1	
Line regulation	12 ≤ V_{IN} ≤ 25 V			6	20	mV
Load regulation	1 ≤ I_O ≤ 20 mA			6	25	mV
Temperature stability	See (1) (6)			0.2	0.4	mV/°C
Total output variation	Line, Load, Temperature	UC184xA, UC284xA	4.9		5.1	V
		UC384xA	4.82		5.18	
Output noise voltage	10 Hz ≤ f ≤ 10 kHz; T_J = 25°C[1]			50		μV
Long-term stability	T_A = 125°C, 1000 hrs[1]			5	25	mV
Output short circuit			–30	–100	–180	mA
OSCILLATOR						
Initial accuracy	T_J = 25°C[5]		47	52	57	kHz
Voltage stability	12 ≤ V_{CC} ≤ 25 V			0.2%	1%	
Temperature stability	T_{MIN} ≤ T_A ≤ T_{MAX} [1]			5%		
Amplitude	$V_{RT/CT}$ peak to peak[1]			1.7		V
Discharge current	T_J = 25°C, $V_{RT/CT}$ = 2 V[7]		7.8	8.3	8.8	mA
	$V_{RT/CT}$ = 2 V[7]	UC184xA, UC284xA	7.5		8.8	
		UC384xA	7.6		8.8	

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5.5 Electrical Characteristics (continued)

Unless otherwise stated, these specifications apply for T_A = –55°C to 125°C (UC184xA), T_A = –40°C to 125°C (UC284xAQ), T_A = –40°C to 85°C (UC284xA), T_A = 0°C to 70°C (UC384xA); $T_A = T_J$; V_{CC} = 15 V[4]; R_T = 10 kΩ; C_T = 3.3 nF.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ERROR AMPLIFIER							
	Input voltage	V_{COMP} = 2.5 V	UC184xA, UC284xA	2.45	2.5	2.55	V
			UC384xA	2.42	2.5	2.58	
	Input bias current				–0.3	–1	µA
					–0.3	–2	
A_{VOL}	Open-loop gain	2 ≤ V_O ≤ 4 V		65	90		dB
	Unity gain bandwidth	T_J = 25°C[1]		0.7	1		MHz
CMRR	Common mode rejection ratio	12 ≤ V_{CC} ≤ 25 V		60	70		dB
	Output sink current	V_{FB} = 2.7 V, V_{COMP} = 1.1 V		2	6		mA
	Output source current	V_{FB} = 2.3 V, V_{COMP} = 5 V		–0.5	–0.8		mA
	V_{OUT} high	V_{FB} = 2.3 V, R_L = 15 kΩ to ground		5	6		V
	V_{OUT} low	V_{FB} = 2.7 V, R_L = 15 kΩ to VREF			0.7	1.1	V
CURRENT SENSE							
	Gain	See [2] [3]		2.85	3	3.15	V/V
	Maximum input signal	V_{COMP} = 5 V[2]		0.9	1	1.1	V
PSRR	Power supply rejection ratio	12 ≤ V_{CC} ≤ 25 V[2]			70		dB
	Input bias current				–2	–10	µA
	Delay to output	V_{ISENSE} = 0 to 2 V[1]			150	300	ns
OUTPUT							
	Output low level	I_{SINK} = 20 mA			0.1	0.4	V
		I_{SINK} = 200 mA			1.5	2.2	
	Output high level	I_{SOURCE} = 20 mA		13	13.5		V
		I_{SOURCE} = 200 mA		12	13.5		
	Rise time	T_J = 25°C, C_L = 1 nF[1]			25	150	ns
	Fall time	T_J = 25°C, C_L = 1 nF[1]			25	150	ns
	UVLO saturation	V_{CC} = 5 V, I_{SINK} = 10 mA			0.7	1.2	V
UNDERVOLTAGE LOCKOUT							
	Start threshold	UC1842A, UC1844A, UC2842A, and UC2844A		15	16	17	V
		UC3842A and UC3844A		14.5	16	17.5	
		UCx843A and UCx845A		7.8	8.4	9	
	Minimum operation voltage after turnon	UC1842A, UC1844A, UC2842A, and UC2844A		9	10	11	V
		UC3842A and UC3844A		8.5	10	11.5	
		UCx843A and UCx845A		7	7.6	8.2	
PWM							
	Maximum duty cycle	UCx842A, UCx843A		92%	96%	100%	
		UCx844A, UCx845A		46%	48%	50%	
	Minimum duty cycle					0%	
TOTAL STANDBY CURRENT							
	Start-up current				0.3	0.5	mA
	Operating supply current	V_{FB} = V_{ISENSE} = 0 V			11	17	mA
	V_{CC} Zener voltage	I_{CC} = 25 mA		30	39		V

(1) Verified by design, but not 100% production tested.
(2) Parameter measured at trip point of latch with V_{FB} = 0.
(3) Gain defined as: A = ΔV_{COMP} / ΔV_{ISENSE}; 0 ≤ V_{ISENSE} ≤ 0.8 V.

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(4) Adjust V_{CC} above the start threshold before setting at 15 V.
(5) Output frequency equals oscillator frequency for the UCx842A and UCx843A. Output frequency is one half oscillator frequency for the UCx844A and UCx845A.
(6) Temperature stability, sometimes referred to as *average temperature coefficient*, is described by: Temperature stability = ($V_{REF(max)}$ – $V_{REF(min)}$) / ($T_{J(max)}$ – $T_{J(min)}$). $V_{REF(max)}$ and $V_{REF(min)}$ are the maximum and minimum reference voltage measured over the appropriate temperature range. Note that the extremes in voltage do not necessarily occur at the extremes in temperature.
(7) This parameter is measured with R_T = 10 kΩ to V_{REF}. This contributes approximately 300 µA of current to the measurement. The total current flowing into the RT/CT pin is approximately 300 µA higher than the measured value.

5.6 Typical Characteristics

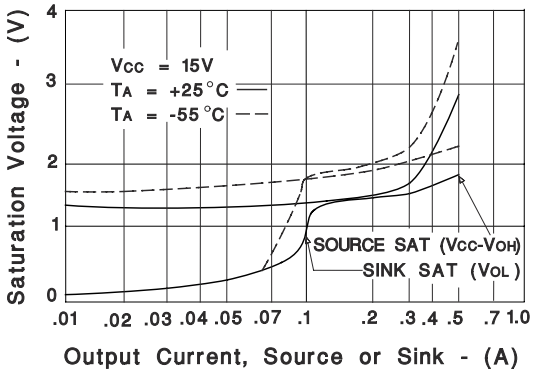


Figure 5-1. Output Saturation Characteristics

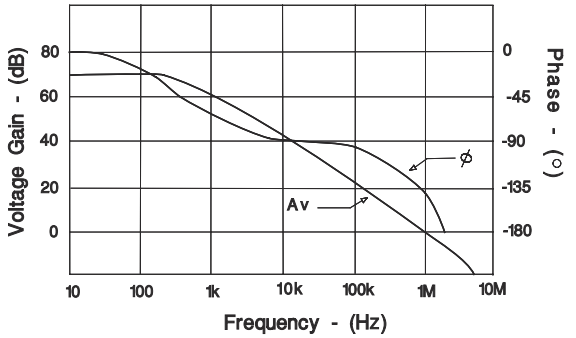


Figure 5-2. Error Amplifier Open-Loop Frequency Response

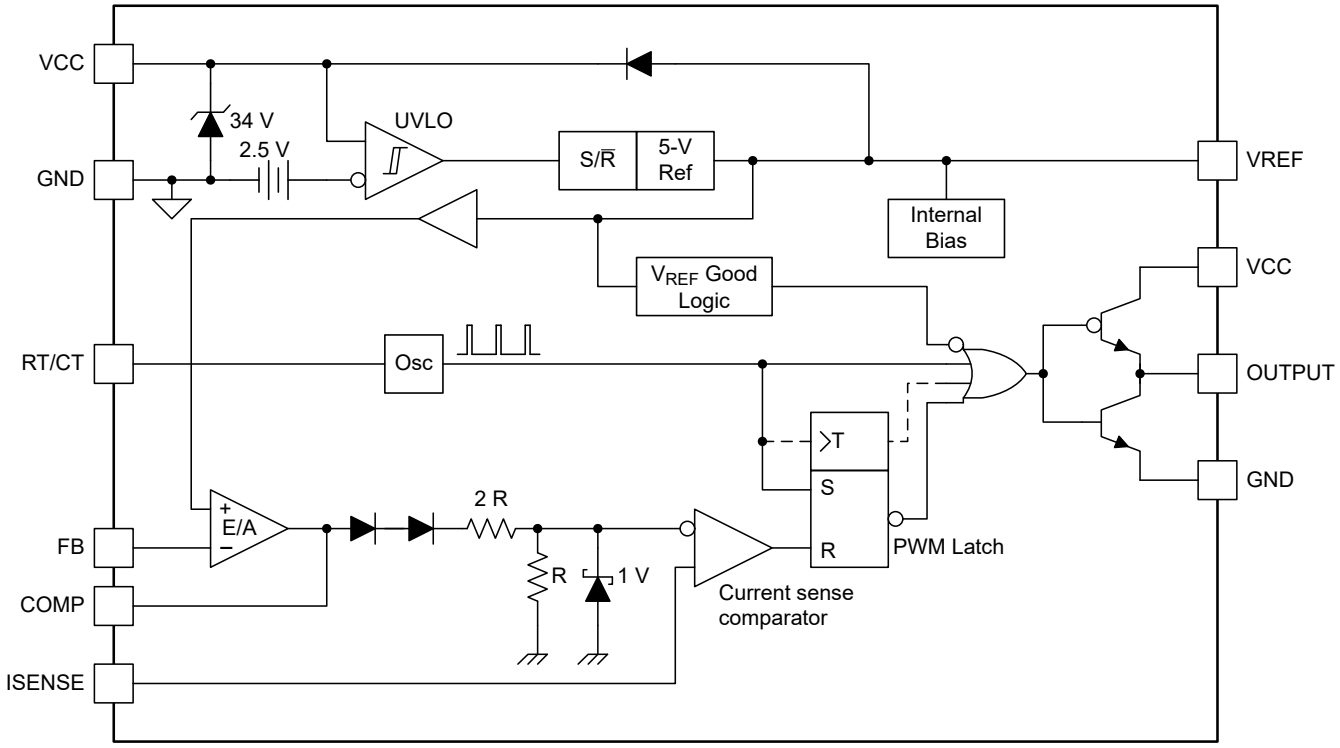
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6 Detailed Description

6.1 Overview

The UCx84xA family of fixed-frequency pulse-width-modulator (PWM) controllers are designed to operate at switching frequencies of 500 kHz. These controllers are designed for peak current mode (PCM) and can be used in isolated and non-isolated power supply designs. These controllers can drive FETs directly from the output, which is capable of sourcing and sinking up to 1 A of gate driver current. These devices also have a built-in low-impedance amplifier that can be used in non-isolated designs to control the power supply output voltage and feedback loop.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Pulse-by-Pulse Current Limiting

Pulse-by-pulse limiting is inherent in the current mode control scheme. An upper limit on the peak current can be established by simply clamping the error voltage. Accurate current limiting allows optimization of magnetic and power semiconductor elements while providing reliable supply operation.

6.3.2 Current Sense Circuit

Peak current (I_S) is determined by Equation 1:

$$I_{S(max)} \times \frac{1\,V}{R_S} \tag{1}$$

A small RC filter can be required to suppress switch transients.

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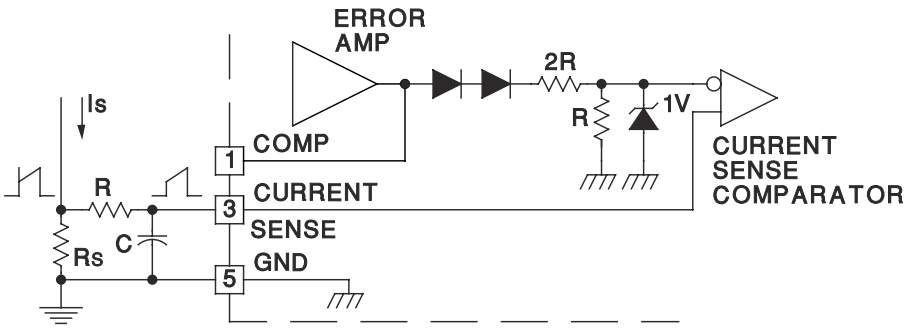


Figure 6-1. Current Sense Circuit Diagram

6.3.3 Error Amplifier Configuration

The error amplifier can source up to 0.8 mA, and sink up to 6 mA.

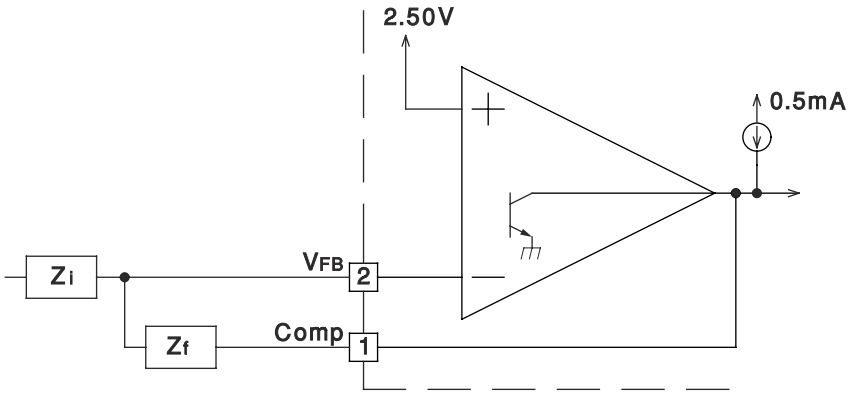


Figure 6-2. Error Amplifier Configuration Diagram

6.3.4 Undervoltage Lockout

The UCx84xA devices feature undervoltage lockout protection circuits for controlled operation during power-up and power-down sequences. Undervoltage lockout thresholds for the UCx842A, UCx843A, UCx844A, and UCx845A devices are optimized for two groups of applications: off-line power supplies and DC-DC converters. With a wider VCC_{ON} to VCC_{OFF} range, the UCx842A and UCx844A devices are ideally suited to off-line AC input applications. The UCx843A and UCx845A controllers have a much narrower VCC_{ON} to VCC_{OFF} hysteresis and can be used in DC to DC applications where the input is considered regulated.

During UVLO the IC draws typically 0.3 mA of supply current. This VCC current is considerable less than the UCx84x family and results in lower power drawn from the line. The reduced start-up current is of particular concern in off-line supplies where the IC is *powered-up* from the high-voltage DC rail, then bootstrapped to an auxiliary winding on the main transformer. Power is then dissipated in the start-up resistor which is sized by the IC start-up current. Lowering this by 50% in the UCx84xA version family, as compared to the UCx84x family, reduces the resistors power loss by the same percentage. Once crossing the turnon threshold the IC supply current increases typically to approximately 11 mA, During undervoltage lockout, the UCx84xA series of devices prevent the power MOSFET from parasitically turning on due to the *Miller* effect at power-up. This improved design to the lower totem-pole transistor operation during undervoltage lockout allows the IC to sink higher currents, up to 10 mA, at saturation voltages as low as 0.7 V, compared to the UCx84x devices which only sinks up to 0.2 mA under the same conditions.

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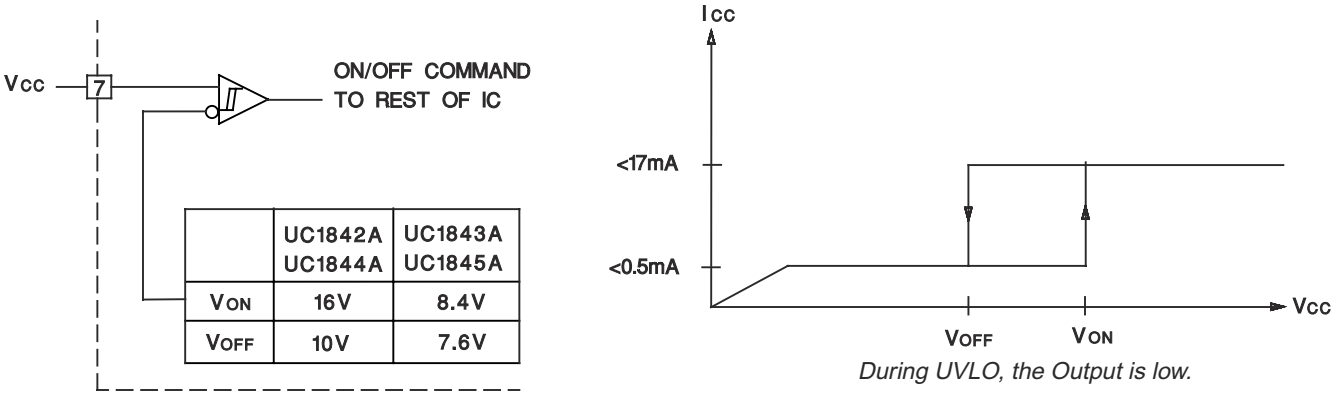


Figure 6-3. Undervoltage Lockout

6.3.5 Oscillator

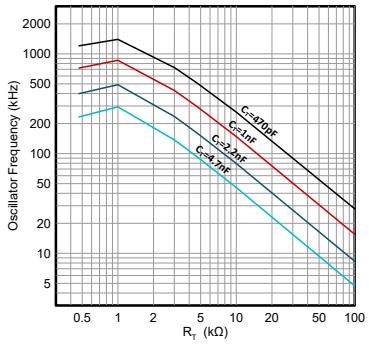


Figure 6-4. Oscillator Frequency vs Timing Resistance

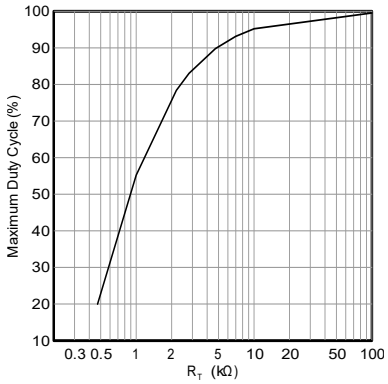
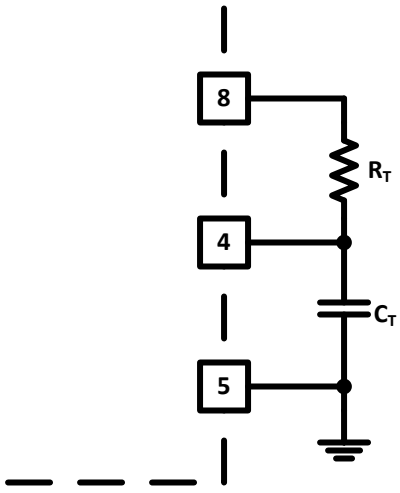


Figure 6-5. Maximum Duty Cycle vs Timing Resistance



$$\text{For } R_T > 5\,k \quad f \approx \frac{1.72}{R_T \times C_T}$$

Figure 6-6. Oscillator Section

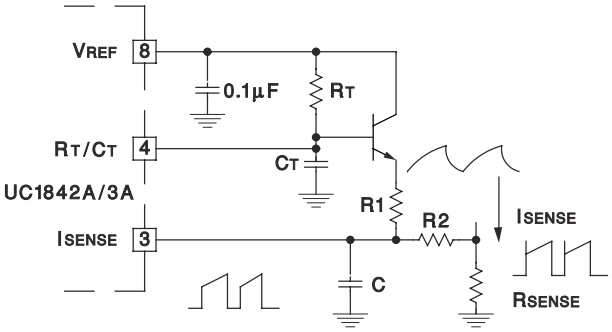


Figure 6-7. Slope Compensation

Precision operation at high frequencies with an accurate maximum duty cycle, see Figure 6-5, can be obtained with the UCx84xA family of devices due to the trimmed oscillator discharge current. This nullifies the effects of production variations in the initial discharge current or dead time. Previous versions of the UCx84x devices had greater than a 2:1 oscillator discharge current range and resulted in less reliable maximum duty cycle programming.

A fraction of the oscillator ramp can be resistively summed with the current sense signal, to provide slope compensation for converters requiring duty cycles over 50%. Capacitor C forms a filter with R2 to suppress the leading-edge switch spikes.

6.4 Device Functional Modes

6.4.1 Normal Operation

The IC can be used in peak current mode (PCM) control or voltage mode (VM) control. When the converter is operating in PCM, the voltage amplifier output regulates the converter peak current and duty cycle. When the IC is used in VM control, the voltage amplifier output regulates the power converter duty cycle. The regulation of the system peak current and duty cycle can be achieved with the use of the integrated error amplifier and external feedback circuitry.

6.4.2 Undervoltage Lockout (UVLO) Start-Up

During system start-up, VCC voltage starts to rise from 0. Before the VCC voltage reaches the corresponding start threshold, the IC is operating in UVLO mode. After the UVLO turn start-up threshold is met the device becomes active and the reference comes up to 5 V.

6.4.3 UVLO Turnoff Mode

If the bias voltage to VCC drops below the UVLO minimum operating voltage, PWM switching stops and the reference becomes inactive, returning to 0 V. The device can be restarted by applying a voltage greater than the UVLO start threshold to the VCC pin.

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The UCx84xA controllers are peak-current mode pulse-width modulators. These controllers have an onboard amplifier and can be used in isolated or nonisolated power supply designs. There is an onboard totem-pole gate driver capable of delivering 1 A of peak current. This is a high-speed PWM capable of operating at switching frequencies up to 500 kHz.

7.2 Typical Application

A typical application for the UC3842A in an off-line flyback converter is shown in Figure 7-1. The UC3842A uses an inner current control loop that contains a small current sense resistor which senses the primary inductor current ramp. This current sense resistor transforms the inductor current waveform to a voltage signal that is input directly into the primary side PWM comparator. This inner loop determines the response to input voltage changes. An outer voltage control loop involves comparing a portion of the output voltage to a reference voltage at the input of an error amplifier. When used in an off-line isolated application, the voltage feedback of the isolated output is accomplished using a secondary-side error amplifier and adjustable voltage reference, such as the TL431. The error signal crosses the primary to secondary isolation boundary using an opto-isolator whose collector is connected to the VREF pin and the emitter is connected to FB. The outer voltage control loop determines the response to load changes.

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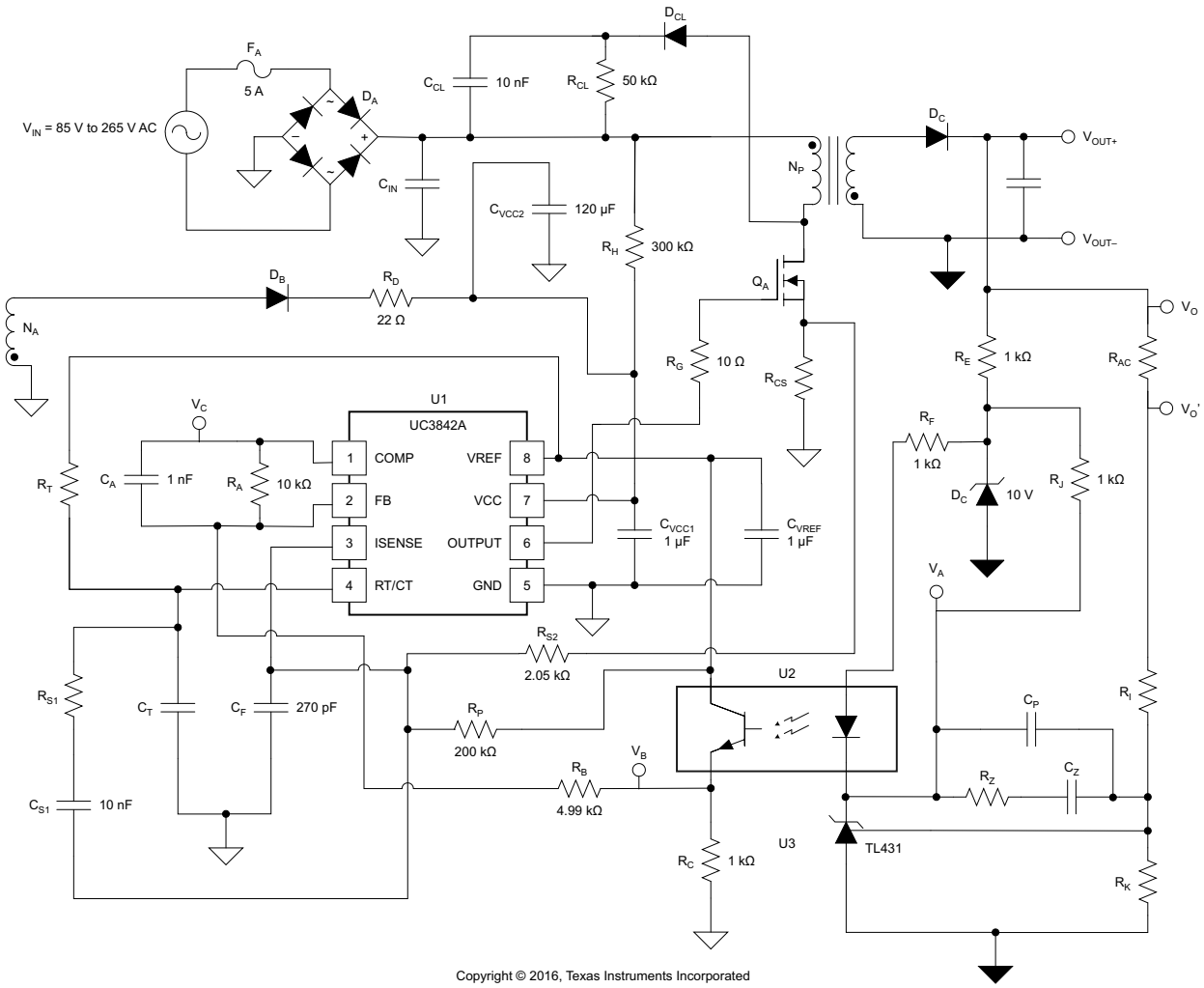


Figure 7-1. Typical Flyback Application Circuit

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7.2.1 Design Requirements

For this design example, use the parameters listed in Table 7-1 as the input parameters.

Table 7-1. Design Parameters

PARAMETER		MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS					
V_{IN}	Input voltage (RMS)	85		265	V
f_{LINE}	Line frequency	47		63	Hz
OUTPUT CHARACTERISTICS					
V_{OUT}	Output voltage	11.75	12	12.25	V
	Output ripple voltage		50		mV_{PP}
I_{OUT}	Output current		4	4.33	A
	Load step	11.75		12.25	V
SYSTEMS CHARACTERISTICS					
η	Maximum load efficiency	86%			

7.2.2 Detailed Design Procedure

7.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the UCx84xA device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

7.2.2.2 UC2842A Design Procedure

This application design procedure shows how to setup and use the UC2842A peak current mode controller in an offline flyback converter, with universal input to a 12-V, 48-W regulated output.

Setting up and designing with the UC2842A peak current mode controller in a continuous mode flyback application requires knowing some things about the power stage. First, calculate the required input bulk capacitance (C_{IN}) based on output power level (P_{OUT}), efficiency (η), minimum input voltage ($V_{IN(min)}$), line frequency (f_{LINE}) and minimum bulk voltage. For this design example let $V_{BULK(min)}$ = 95 V.

$$V_{INripple} = \frac{2 \times \frac{P_{OUT}}{\eta} \times \left[0.25 + \frac{1}{\pi} \times \arcsin \times \left(\frac{V_{BULK(min)}}{\sqrt{2} \times V_{IN(min)}} \right) \right]}{\left(2 \times V_{IN(min)}^2 - V_{BULK(min)}^2 \right) \times f_{LINE}} \quad (2)$$

$$C_{IN} = \frac{2 \times \frac{P_{OUT}}{\eta} \times \left[0.25 + \frac{1}{\pi} \times \arcsin \times \left(\frac{V_{BULK(min)}}{\sqrt{2} \times V_{IN(min)}} \right) \right]}{\left(2 \times V_{IN(min)}^2 - V_{BULK(min)}^2 \right) \times f_{LINE}} \approx 180\ \mu F \quad (3)$$

The output capacitor (C_{OUT}) is sized so the output voltage does not droop more than 10% during a large-signal transient response. The voltage-loop crossover frequency (f_C) is estimated to be 2.5 kHz at this point in the design.

$$C_{OUT} \geq \frac{\frac{I_{OUT}}{f_C}}{V_{OUT} \times 10\%} \approx 1.33\text{mF} \tag{4}$$

The C_{OUT} selected for the design is a 2200-µF capacitor, with an equivalent series resistance (ESR) of 45 mΩ.

Next calculate the maximum primary to secondary turns ratio (N_{PS}) of the transformer, based on the minimum input voltage and output voltage.

$$N_{PS} \leq \frac{V_{IN(min)} \times \sqrt{2}}{V_{OUT}} = \frac{85\text{ V} \times \sqrt{2}}{12\text{ V}} \approx 10 \tag{5}$$

Next calculate the auxiliary to secondary turns ratio (N_{AS}) of the transformer, based on the output voltage and the bias voltage of the UC2842A.

$$N_{AS} \leq \frac{V_{VCC}}{V_{OUT}} = \frac{12\text{ V}}{12\text{ V}} = 1 \tag{6}$$

Once the transformer turns ratios have been determined, the minimum primary magnetizing inductance (L_{PM}) of the transformer can be calculated based on minimum bulk voltage, Duty Cycle (D), reflected output current and efficiency. The transformer used in this design has an L_{PM} of 1.7 mH, N_{PS} = 10, and a N_{AS} = 1, f_{sw} = 100 kHz

$$D = \frac{N_{PS} \times V_{OUT}}{V_{BULK(min)} + N_{PS} \times V_{OUT}} \approx 0.56 \tag{7}$$

$$L_{PM} \geq \frac{V_{BULK\,(min)} \times D}{\frac{70\% \times I_{OUT} \times f_{sw}}{\eta \times N_{PS}}} = 1.632\text{mH} \approx 1.7\text{mH} \tag{8}$$

After the transformer has been selected, the primary peak current (I_{LpPK}) of the transformer can be calculated based on the primary magnetizing inductance ripple (I_{LPM}) and the reflected output current across the transformer.

$$I_{LPM} = \frac{V_{BULK(min)} \times D}{f_{SW} \times L_M} \approx 0.31\text{ A} \tag{9}$$

$$I_{LpPK} = \frac{I_{OUT}}{N_{PS} \times (1 - D)} + \frac{I_{LM}}{2} \approx 1.1\text{ A} \tag{10}$$

Once the primary peak current has been calculated the current sense resistor (R_{CS}) can be selected.

$$R_{CS} = \frac{1\text{ V}}{I_{LpPK} \times 1.3} = 0.725\ \Omega \approx 0.75\ \Omega \tag{11}$$

Resistors R_{S1} and R_{S2} are used to set the slope compensation of the design. Capacitor C_{S1} is a DC blocking capacitor, and pull-up resistor R_P is used to provide some offset to the current sense signal for noise immunity. R_P and R_{S2} were preselected to add a DC offset of 50 mV to the current sense signal.

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R_{S1} is selected to set the slope compensation to one-half of the ripple current down slope of the flyback inductor. This can be accomplished by calculating the secondary magnetizing inductance (L_{SM}) and using the following calculation for R_{S1}. The 1.7 V in the R_{S1} equation is the peak-to-peak ripple voltage amplitude of the oscillator.

$$R_{S1} = \frac{1.7\ V \times R_{S2} \times f_{SW} \times (2 \times L_{SM} \times N_{PS})}{V_{OUT} \times (1-D) \times R_{CS}} - R_{S2} = 27.72\ k\Omega \approx 27.4\ k\Omega \quad (12)$$

where

- $R_{S2} = 2.05\ k\Omega$

Resistors R_I and R_K are selected to the output reference and can be calculated by preselecting a value for R_K and knowing the TL431 reference voltage ($V_{TL431REF}$). After choosing 2.49 kΩ for R_K, R_I is calculated and a standard resistor value of 9.53 kΩ is chosen for this resistor.

$$R_I = \frac{R_K \times (V_{OUT} - V_{TL431REF})}{V_{TL431REF}} = \frac{2.49\ k\Omega \times (12\ V - 2.5\ V)}{2.5\ V} = 9.462\ k\Omega \approx 9.53\ k\Omega \quad (13)$$

This design using the UC2842A controller has an interesting control loop with many components. $G_{OPTO}(f)$ is the approximate transfer function across the opto isolator in the design. The pole frequency of the opto isolator is represented by f_P. The opto isolator used in this design has a current transfer ratio of 1 and pole frequency of roughly 5 kHz. See Figure 7-1 for component placement and node voltages. The voltage loop (f_C) must cross-over less than the opto isolator pole for simplified compensation.

$$s(f) = 2 \times \pi \times 1i \times f \quad (14)$$

$$f_P = 5\ kHz \quad (15)$$

$$G_{OPTO}(f) = \frac{\Delta V_B}{\Delta V_A} = \frac{R_C}{R_F} \times \frac{ctr}{\frac{s(f)}{2 \times \pi \times f_P} + 1} \quad (16)$$

$G_{BC}(f)$ is an estimate of the transfer function from the output of the opto isolator to the PWM's control voltage .

$$G_{BC}(f) = \frac{\Delta V_C}{\Delta V_B} = \frac{R_A}{R_B} \times \frac{1}{s(f) \times R_A \times C_A + 1} \quad (17)$$

The duty cycle varies with the bulk input voltage (V_{BULK}). V_{BULK} varies from 95 V to 375 V during normal operation. This causes the duty cycle to vary from 24% to 56%.

$$D = \frac{N_{PS} \times V_{OUT}}{V_{BULK} + N_{PS} \times V_{OUT}} = 0.24 \text{ to } 0.56 \quad (18)$$

$G_{CO}(f)$ is an estimate of the control (V_C) to output transfer function, where variable Q is the quality factor.

$$G_{CO}(f) = \frac{\Delta V_{OUT}}{\Delta V_C} = N_{PS} \times \frac{1-D}{1+D} \times \left[\frac{s(f) \times ESR \times C_{OUT} + 1}{s(f) \times R_{OUT} \times C_{OUT} + 1}\right] \times \left[1 - \frac{s(f) L_{SM} \times D}{R_{OUT} \times (1-D)^2}\right] \times \frac{\frac{1}{3}}{1 + \frac{s(f)}{2 \times \pi \times \frac{f_{SW} \times}{2} Q} + \left(\frac{s(f)}{2 \times \pi \times \frac{f_{SW}}{2}}\right)^2} \quad (19)$$

The quality factor (Q) is defined by the primary magnetizing inductance change in voltage (S_N) as a function of duty cycle; as well as, the added slope compensation (S_E).

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$$S_N = \frac{V_{BULK} \times R_{CS}}{L_{PM}} \quad (20)$$

$$S_E = 1.7\ V \times \frac{R_{S2} \times f_{SW}}{R_{S1} + R_{S2}} \quad (21)$$

$$Q = \frac{1}{\pi\left[\left(1 + \frac{S_E}{S_N}\right) \times (1 - D) - 0.5\right]} \quad (22)$$

To verify that the voltage loop is stable, the crossover frequency must be less than one half of the right-half-plane zero frequency (f_{RHPZ}) of the flyback converter. The right-half-plane zero frequency at the minimum bulk voltage is approximately 9.8 kHz. For this design example the target crossover of the voltage loop is at 1 kHz. The actual f_C can be higher or lower than the target.

$$f_{RHPz} = \frac{(N_{PS})^2}{\frac{2 \times \pi \times Lpm}{R_{OUT}} \frac{D}{(1-D)^2}} \approx 9.8kHz \quad (23)$$

$$f_C \leq \frac{f_{RHPz}}{2} \approx 5\ kHZ \quad (24)$$

The DC gain of $G_{CO}(f)$ moves with the bulk input voltage. Resistor R_Z is selected to crossover the voltage loop when input to the converter is at $V_{BULK(min)}$ and to crossover at 1/5th the maximum crossover frequency.

$$R_Z = \frac{R_I}{\left|G_{OPTO}(f_C/5) \times G_{BC}(f_C/5) \times G_O \times G_{CO}(f_C/5)\right|} = 23.95\ k\Omega, \text{ a } 23.7\ k\Omega \text{ was used} \quad (25)$$

Capacitor C_Z is selected to add 45° of phase margin at voltage loop crossover. For this design example a 6.8-nF capacitor is used.

$$C_Z = \frac{1}{2\pi \times \frac{f_C}{5} \times R_Z} \approx 6.7\ nF \quad (26)$$

Capacitor C_P is selected to attenuate the high frequency gain of the control loop.

$$C_P = \frac{C_Z}{10} = 680\ pF \quad (27)$$

$G_C(f)$ is the estimated transfer function of the TL431 compensation.

$$G_C(f) = \frac{\Delta V_C}{\Delta V_O'} = \frac{s(f) \times R_Z \times C_Z + 1}{s(f) \times R_I \times (C_Z + C_P) \times \left(\frac{s(f) \times R_Z \times C_Z \times C_P}{C_Z + C_P} + 1\right)} \quad (28)$$

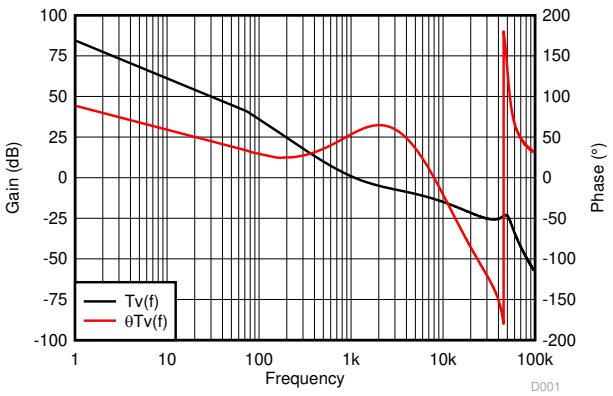
$T_V(f)$ is the estimated theoretical transfer function of the close-loop gain of the system. The feedback loop response can be different in the actual circuit and can have to be adjusted with a network analyzer to meet actual circuit performance and reliability. The feedback loop response must be evaluated over worse case variations in design parameters.

$$T_V(f) = G_C(f) \times G_{OPTO}(f) \times G_{BC}(f) \times G_O \times G_{CO}(f_C) \quad (29)$$

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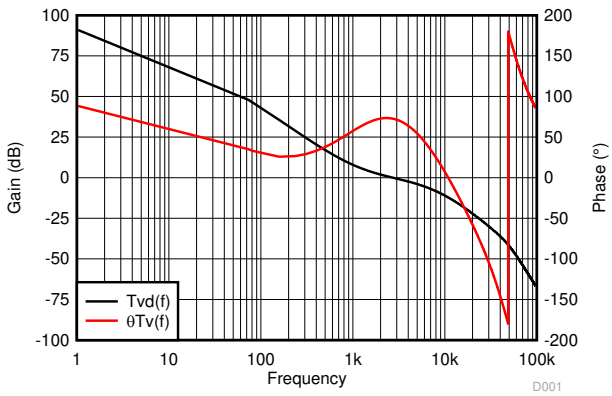
For this application example, this design technique generated a theoretical feedback loop ($T_V(f)$) crossover at 1 kHz with roughly 55° of phase margin at a minimum input bulk voltage of 95 V. The theoretical voltage loop at high-line crossed over at 2.7 kHz with a phase margin of 72°. See Figure 7-2 and Figure 7-3. $T_V(f)$ must be evaluated with a network analyzer and adjust the loop compensation as necessary based on the actual circuitry behavior. Also conduct transient testing to verify that the device remains stable.

7.2.3 Application Curves



V_{BULK} = 95 V

Figure 7-2. Voltage Loop Gain



V_{BULK} = 375 V

Figure 7-3. Voltage Loop Gain

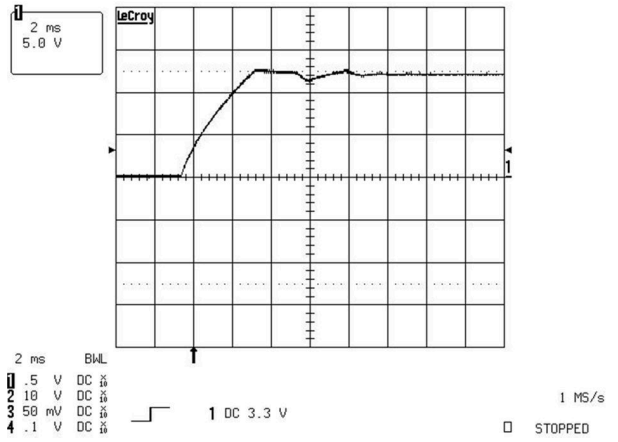


Figure 7-4. V_{OUT} Start-Up Full Load

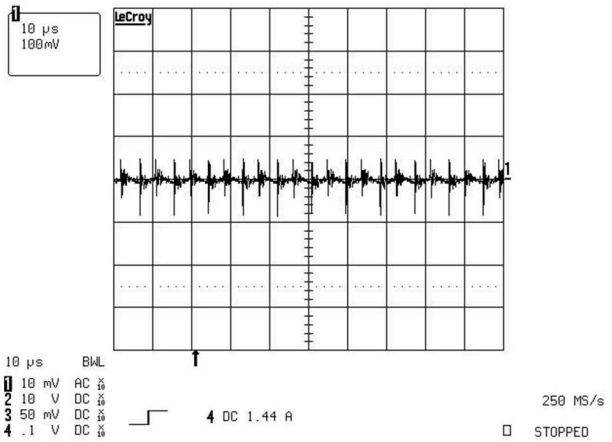


Figure 7-5. V_{OUT} Ripple Voltage

8 Power Supply Recommendations

TI recommends using the UCx84xA in isolated or non-isolated peak current mode control power supplies. The device can be used in buck, boost, flyback, and forwarded converter-based power supply topologies.

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9 Layout

9.1 Layout Guidelines

- Star grounding techniques must be used.
- Current loops must be kept as short and narrow as possible.
- The IC ground and power ground must meet at the return for the input bulk capacitor. Verify that high frequency and high current from the power stage does not go through the signal ground paths.
- A high-frequency bypass capacitor (C_{VCC1}) must be placed across VCC and GND pins as close as possible to the pins.
- Resistor R_{S2} and capacitor C_F form a low-pass filter for the current sense signal. C_F must be as close to CS and GND pins as possible.
- Capacitor C_{VREF} must be as close to VREF and GND pins as possible.
- Figure 9-1 shows the SMD components arranged for wave-solder on a single-layer board. If multiple layers are used, some components can be rearranged for easier interconnection and reduced current-loop areas. If the solder process allows, placing the SMD components in perpendicular orientations can improve interconnections and loop areas.

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9.2 Layout Example

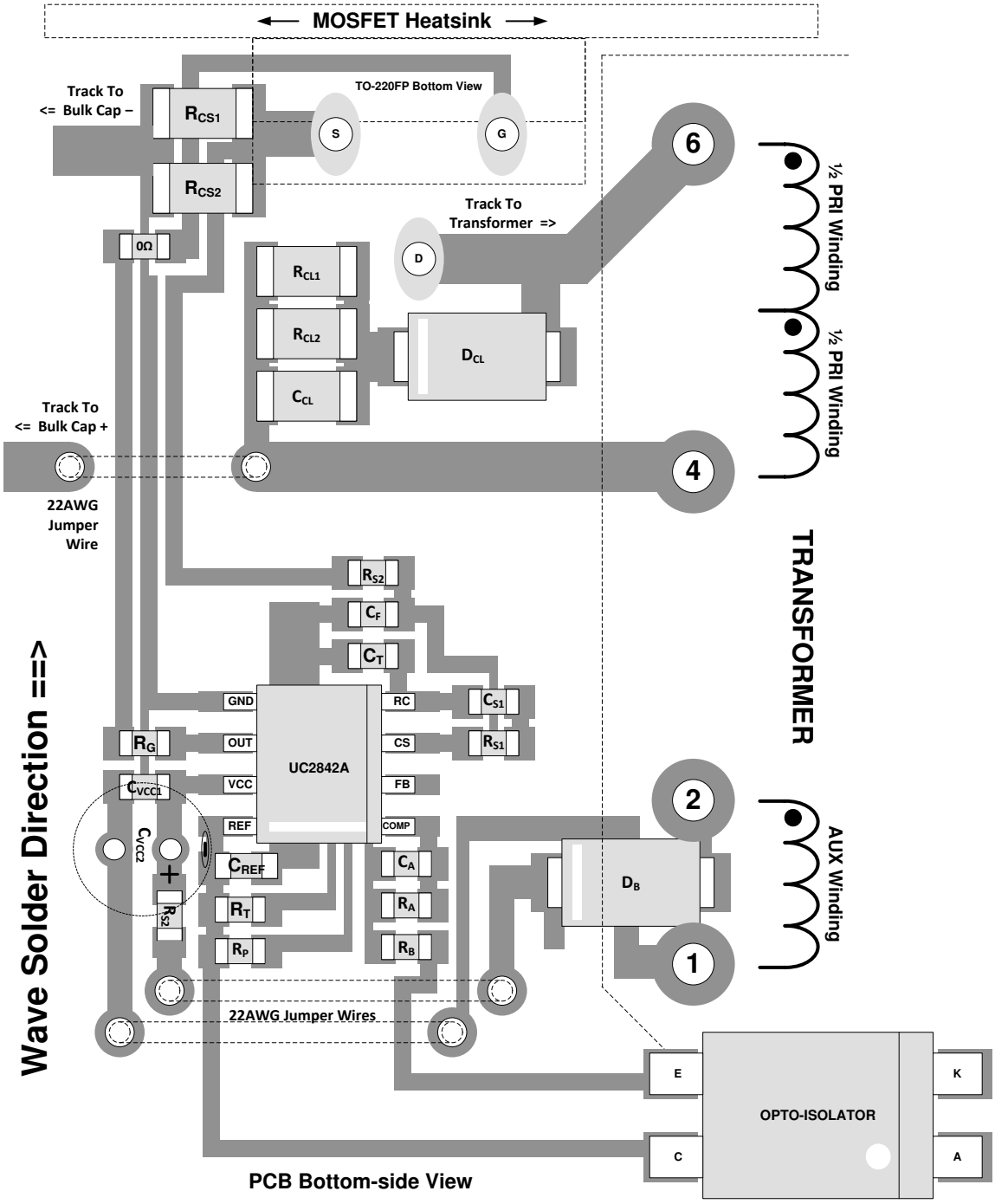


Figure 9-1. Layout Diagram

10 Device and Documentation Support

10.1 Device Support

10.1.1 Development Support

- TI Engineer-to-Engineer Support Forum, https://e2e.ti.com/

10.1.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the UCx84xA device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

10.1.2 Device Nomenclature

C_{IN}	Input bulk capacitance
C_{OUT}	Output capacitance
D	Duty cycle
ESR	Equivalent series resistance
$G_{BC}(f)$	An estimate of the transfer function from the output of the opto-isolator to the PWM control voltage.
G_O	The DC gain of the control to output transfer function.
$G_{OPTO}(f)$	The approximate transfer function across the opto-isolator in the design.
I_{LPM}	Transformer primary average current
I_{LpPK}	Peak transformer primary current
L_{PM}	Transformer primary magnetizing inductance
L_{SM}	Transformer secondary magnetizing inductance
N_{PS}	Primary to secondary transformer turns ratio
N_{AS}	Auxiliary to secondary transformer turns ratio
$T_V(f)$	is the feedback control loop transfer function.
$V_{INripple}$	Input ripple voltage

10.2 Documentation Support

10.2.1 Related Documentation

For related documentation see the following:

Design Review: 150 Watt Current-Mode Flyback (SLUP078)

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10.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 10-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
UC1842A	Click here	Click here	Click here	Click here	Click here
UC1843A	Click here	Click here	Click here	Click here	Click here
UC1844A	Click here	Click here	Click here	Click here	Click here
UC1845A	Click here	Click here	Click here	Click here	Click here
UC2842A	Click here	Click here	Click here	Click here	Click here
UC2843A	Click here	Click here	Click here	Click here	Click here
UC2844A	Click here	Click here	Click here	Click here	Click here
UC2845A	Click here	Click here	Click here	Click here	Click here
UC3842A	Click here	Click here	Click here	Click here	Click here
UC3843A	Click here	Click here	Click here	Click here	Click here
UC3844A	Click here	Click here	Click here	Click here	Click here
UC3845A	Click here	Click here	Click here	Click here	Click here

10.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.5 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.6 Trademarks

TI E2E™ is a trademark of Texas Instruments.
WEBENCH® is a registered trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.7 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.8 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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Changes from Revision G (July 2022) to Revision H (October 2024) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document..... 1
- Changed thermal information for D-8, D-14, and P-8 packages..... 6
- Changed the OUTPUT SECTION: Rise and fall time, typical value from 50ns to 25ns in the Electrical Characteristics section..... 6
- Changed the OUTPUT SECTION: Output low level, typical value from 15V to 1.5V in the Electrical Characteristics section..... 6
- Changed the PWM: maximum duty cycle of UCx842/3A, minimum value from 94% to 92% in the Electrical Characteristics section..... 6
- Changed the PWM SECTION: maximum duty cycle of UCx844/5A, minimum value from 47% to 46% in the Electrical Characteristics section..... 6
- Changed the TOTAL STANDBY CURRENT, VCC Zener voltage, typical value from 34V to 39V in the Electrical Characteristics section..... 6
- Updated the Frequency vs Rt and Maximum Duty Cycle vs Rt figures in the Typical Characteristics..... 8

Changes from Revision F (October 2017) to Revision G (July 2022) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document..... 1

Changes from Revision E (October 2017) to Revision F (October 2017) **Page**

- Added WEBENCH links in three places, Features, Application and Implementation and Device and Documentation Support..... 1
- Added copyright information to the Simplified Application Diagram 1
- Changed operating free-air temperature of the UC284xA changed from 125°C to 85°C. 5
- Changed operating free-air temperature of the UC384xA changed from -40°C to 0°C. 5
- Changed operating free-air temperature of the UC384xA changed from 85°C to 70°C. 5
- Changed the frequency (f) calculation to the correct equation..... 11
- Changed the C_{OUT} equation to the corrected equation. 15
- Changed the L_{PM} equation to the corrected equation..... 15
- Added $G_{CO}(f)$ definition and equation..... 15
- Changed the f_{RHPz} equation to the corrected equation..... 15

Changes from Revision D (July 2011) to Revision E (July 2016) **Page**

- Added *Applications* section, *Device Information* table, *Pin Configuration and Functions* section, *Specifications* section, *Detailed Description* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1
- Deleted *Ordering Information Table*; see POA at the end of the data sheet..... 1

Changes from Revision C (August 2010) to Revision D (July 2011) **Page**

- Changed Absolute Maximum ratings table with maximum negative voltage and GND pin notes..... 5

Changes from Revision B (September 2009) to Revision C (August 2010) **Page**

- Corrected I_{SINK} voltage..... 6

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-8670405PA	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8670405PA UC1842A
5962-8670405XA	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8670405XA UC1842AL/ 883B
5962-8670406PA	NRND	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8670406PA UC1843A
5962-8670406XA	NRND	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8670406XA UC1843AL/ 883B
5962-8670407PA	NRND	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8670407PA UC1844A
5962-8670407XA	NRND	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8670407XA UC1844AL/ 883B
5962-8670408PA	NRND	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8670408PA UC1845A
5962-8670408XA	NRND	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8670408XA UC1845AL/ 883B
UC1842AJ	NRND	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	UC1842AJ
UC1842AJ.A	NRND	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	UC1842AJ
UC1842AJ883B	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8670405PA UC1842A
UC1842AJ883B.A	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8670405PA UC1842A
UC1842AL883B	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8670405XA UC1842AL/ 883B

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UC1842AL883B.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8670405XA UC1842AL/883B
UC1843AJ	NRND	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	UC1843AJ
UC1843AJ.A	NRND	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	UC1843AJ
UC1843AJ883B	NRND	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8670406PA UC1843A
UC1843AJ883B.A	NRND	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8670406PA UC1843A
UC1843AL883B	NRND	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8670406XA UC1843AL/883B
UC1843AL883B.A	NRND	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8670406XA UC1843AL/883B
UC1844AJ	NRND	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	UC1844AJ
UC1844AJ.A	NRND	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	UC1844AJ
UC1844AJ883B	NRND	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8670407PA UC1844A
UC1844AJ883B.A	NRND	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8670407PA UC1844A
UC1844AL883B	NRND	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8670407XA UC1844AL/883B
UC1844AL883B.A	NRND	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8670407XA UC1844AL/883B
UC1845AJ	NRND	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	UC1845AJ
UC1845AJ.A	NRND	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	UC1845AJ
UC1845AJ883B	NRND	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8670408PA UC1845A

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UC1845AJ883B.A	NRND	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8670408PA UC1845A
UC1845AL883B	NRND	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8670408XA UC1845AL/ 883B
UC1845AL883B.A	NRND	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8670408XA UC1845AL/ 883B
UC2842AD	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2842AD
UC2842AD.A	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2842AD
UC2842AD8	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	UC2842A UC2842 AD8
UC2842AD8TR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2842A UC2842 AD8
UC2842AD8TR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2842A UC2842 AD8
UC2842ADG4	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2842AD
UC2842ADTR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2842AD
UC2842ADTR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2842AD
UC2842ADW	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2842ADW
UC2842ADW.A	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2842ADW
UC2842ADWTR	NRND	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2842ADW
UC2842ADWTR.A	NRND	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2842ADW
UC2842AN	NRND	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	UC2842AN
UC2842AN.A	NRND	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	UC2842AN
UC2842ANG4	NRND	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	UC2842AN
UC2843AD	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 85	UC2843AD
UC2843AD8	NRND	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2843A UC2843 AD8

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UC2843AD8.A	NRND	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2843A UC2843 AD8
UC2843AD8G4	NRND	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2843A UC2843 AD8
UC2843AD8TR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2843A UC2843 AD8
UC2843AD8TR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2843A UC2843 AD8
UC2843AD8TRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2843A UC2843 AD8
UC2843ADTR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2843AD
UC2843ADTR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2843AD
UC2843AN	NRND	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	UC2843AN
UC2843AN.A	NRND	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	UC2843AN
UC2843ANG4	NRND	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	UC2843AN
UC2844AD	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 85	UC2844AD
UC2844AD8TR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2844A UC2844 AD8
UC2844AD8TR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2844A UC2844 AD8
UC2844AD8TRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2844A UC2844 AD8
UC2844ADTR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2844AD
UC2844ADTR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2844AD
UC2844AN	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	UC2844AN
UC2844AN.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	UC2844AN
UC2844ANG4	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	UC2844AN

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UC2844AQD8	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	(2844AQ, UC2844AQ)
UC2844AQDR	NRND	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(2844AQ, UC2844AQ)
UC2844AQDR.A	NRND	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(2844AQ, UC2844AQ)
UC2845AD	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2845AD
UC2845AD.A	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2845AD
UC2845AD8	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	UC2845A UC2845 AD8
UC2845AD8TR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2845A UC2845 AD8
UC2845AD8TR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2845A UC2845 AD8
UC2845AD8TRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2845A UC2845 AD8
UC2845ADTR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2845AD
UC2845ADTR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2845AD
UC2845ADW	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2845ADW
UC2845ADW.A	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2845ADW
UC2845AN	NRND	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	UC2845AN
UC2845AN.A	NRND	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	UC2845AN
UC2845ANG4	NRND	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	UC2845AN
UC3842AD	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3842AD
UC3842AD.A	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3842AD
UC3842AD8	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	UC3842A UC3842 AD8
UC3842AD8TR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3842A UC3842 AD8

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UC3842AD8TR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3842A UC3842 AD8
UC3842AD8TRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3842A UC3842 AD8
UC3842ADG4	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3842AD
UC3842ADTR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3842AD
UC3842ADTR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3842AD
UC3842ADW	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3842ADW
UC3842ADW.A	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3842ADW
UC3842AN	NRND	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UC3842AN
UC3842AN.A	NRND	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UC3842AN
UC3842ANG4	NRND	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UC3842AN
UC3842J	NRND	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-40 to 85	UC3842J
UC3842J.A	NRND	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-40 to 85	UC3842J
UC3843AD	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3843AD
UC3843AD.A	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3843AD
UC3843AD8	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	UC3843A UC3843 AD8
UC3843AD8TR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3843A UC3843 AD8
UC3843AD8TR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3843A UC3843 AD8
UC3843AD8TRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3843A UC3843 AD8
UC3843ADG4	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3843AD
UC3843ADTR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3843AD
UC3843ADTR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3843AD
UC3843AN	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UC3843AN

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UC3843AN.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UC3843AN
UC3843ANG4	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UC3843AN
UC3844AD	NRND	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3844AD
UC3844AD.A	NRND	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3844AD
UC3844AD8	NRND	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3844A UC3844 AD8
UC3844AD8.A	NRND	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3844A UC3844 AD8
UC3844AD8G4	NRND	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3844A UC3844 AD8
UC3844AD8TR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3844A UC3844 AD8
UC3844AD8TR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3844A UC3844 AD8
UC3844ADTR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3844AD
UC3844ADTR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3844AD
UC3844AN	NRND	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UC3844AN
UC3844AN.A	NRND	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UC3844AN
UC3844ANG4	NRND	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UC3844AN
UC3845AD	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3845AD
UC3845AD.A	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3845AD
UC3845AD8	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	UC3845A UC3845 AD8
UC3845AD8TR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3845A UC3845 AD8
UC3845AD8TR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3845A UC3845 AD8

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UC3845AD8TRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3845A UC3845 AD8
UC3845ADG4	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3845AD
UC3845ADTR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3845AD
UC3845ADTR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3845AD
UC3845ADTRG4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3845AD
UC3845AN	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UC3845AN
UC3845AN.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UC3845AN
UC3845ANG4	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UC3845AN

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF UC1842A, UC1843A, UC1844A, UC1845A, UC2843A, UC3842A, UC3842M, UC3843A, UC3844A, UC3845A :

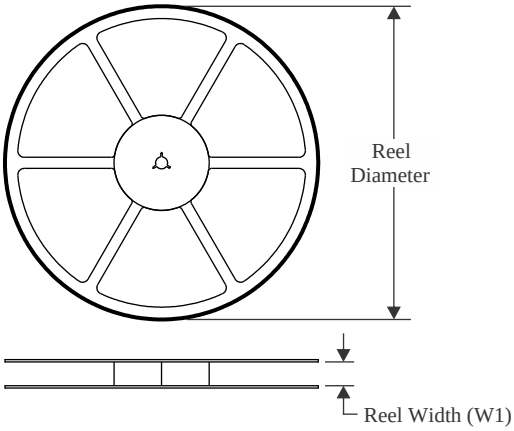
- Catalog : UC3842A, UC3843A, UC3844A, UC3845A, UC3842, UC3845AM
- Automotive : UC2843A-Q1
- Enhanced Product : UC1842A-EP, UC1843A-EP, UC1844A-EP, UC1845A-EP, UC1842A-EP, UC1843A-EP, UC1844A-EP, UC1845A-EP
- Military : UC1842A, UC1842, UC1843A, UC1844A, UC1845A
- Space : UC1842A-SP, UC1843A-SP, UC1844A-SP, UC1845A-SP, UC1842A-SP, UC1843A-SP, UC1844A-SP, UC1845A-SP

NOTE: Qualified Version Definitions:

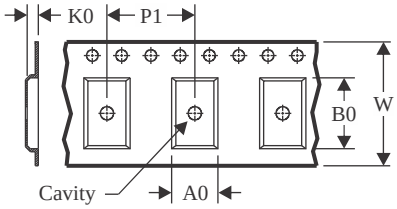
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

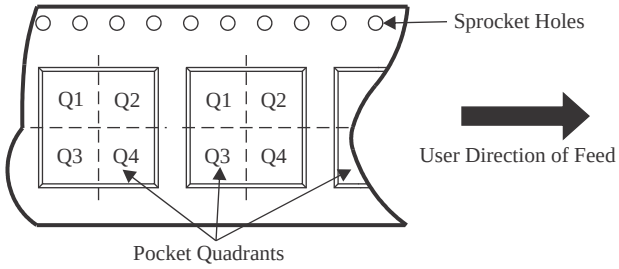


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

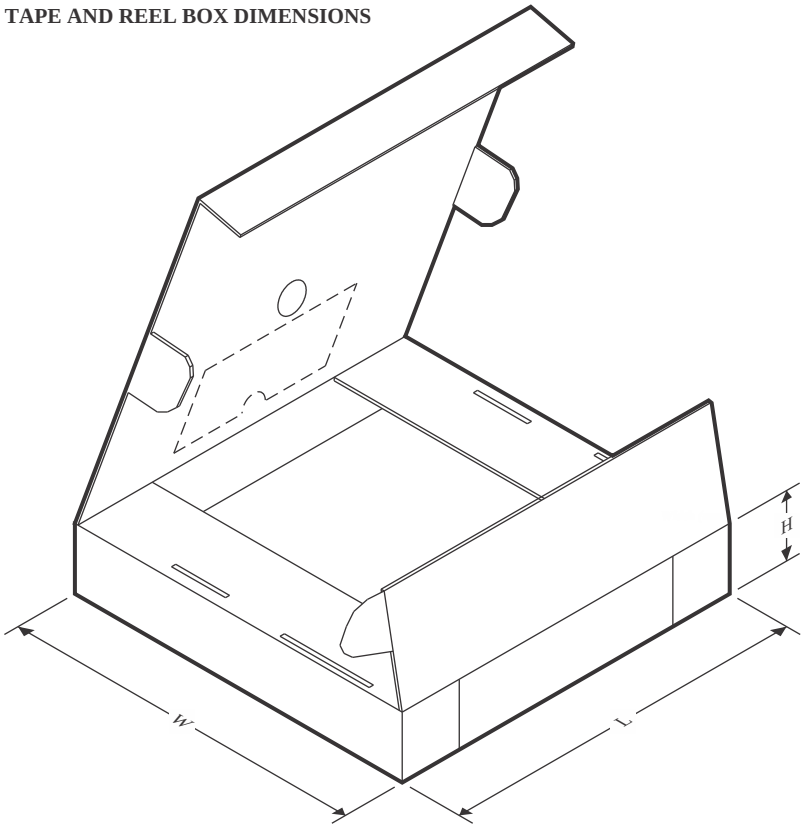


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2842AD8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC2842ADTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC2842ADWTR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
UC2843AD8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC2843ADTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC2844AD8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC2844ADTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC2844AQDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC2845AD8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC2845ADTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC3842AD8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC3842ADTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC3843AD8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC3843ADTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC3844AD8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC3844ADTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC3845AD8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC3845ADTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

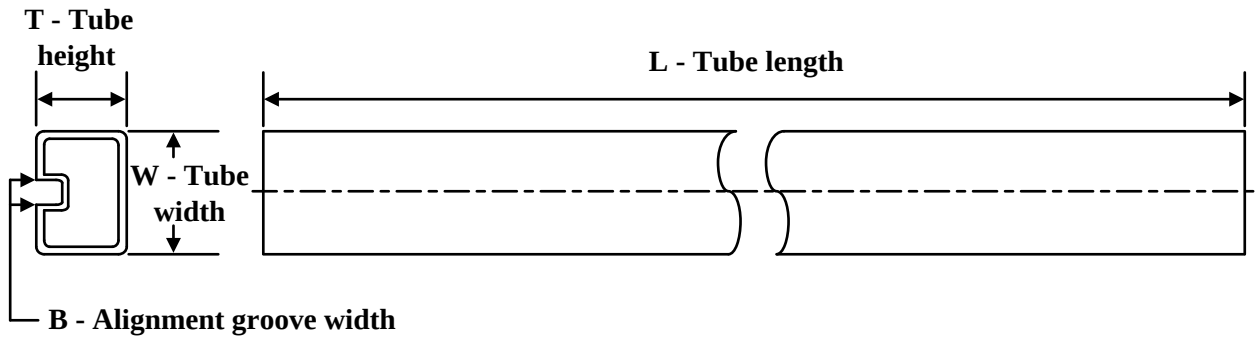
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2842AD8TR	SOIC	D	8	2500	353.0	353.0	32.0
UC2842ADTR	SOIC	D	14	2500	353.0	353.0	32.0
UC2842ADWTR	SOIC	DW	16	2000	353.0	353.0	32.0
UC2843AD8TR	SOIC	D	8	2500	353.0	353.0	32.0
UC2843ADTR	SOIC	D	14	2500	353.0	353.0	32.0
UC2844AD8TR	SOIC	D	8	2500	353.0	353.0	32.0
UC2844ADTR	SOIC	D	14	2500	353.0	353.0	32.0
UC2844AQDR	SOIC	D	14	2500	353.0	353.0	32.0
UC2845AD8TR	SOIC	D	8	2500	353.0	353.0	32.0
UC2845ADTR	SOIC	D	14	2500	353.0	353.0	32.0
UC3842AD8TR	SOIC	D	8	2500	353.0	353.0	32.0
UC3842ADTR	SOIC	D	14	2500	340.5	336.1	32.0
UC3843AD8TR	SOIC	D	8	2500	353.0	353.0	32.0
UC3843ADTR	SOIC	D	14	2500	353.0	353.0	32.0
UC3844AD8TR	SOIC	D	8	2500	353.0	353.0	32.0
UC3844ADTR	SOIC	D	14	2500	333.2	345.9	28.6
UC3845AD8TR	SOIC	D	8	2500	353.0	353.0	32.0
UC3845ADTR	SOIC	D	14	2500	353.0	353.0	32.0

TUBE

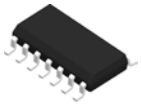


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-8670405XA	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-8670406XA	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-8670407XA	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-8670408XA	FK	LCCC	20	55	506.98	12.06	2030	NA
UC1842AL883B	FK	LCCC	20	55	506.98	12.06	2030	NA
UC1842AL883B.A	FK	LCCC	20	55	506.98	12.06	2030	NA
UC1843AL883B	FK	LCCC	20	55	506.98	12.06	2030	NA
UC1843AL883B.A	FK	LCCC	20	55	506.98	12.06	2030	NA
UC1844AL883B	FK	LCCC	20	55	506.98	12.06	2030	NA
UC1844AL883B.A	FK	LCCC	20	55	506.98	12.06	2030	NA
UC1845AL883B	FK	LCCC	20	55	506.98	12.06	2030	NA
UC1845AL883B.A	FK	LCCC	20	55	506.98	12.06	2030	NA
UC2842AD	D	SOIC	14	50	507	8	3940	4.32
UC2842AD.A	D	SOIC	14	50	507	8	3940	4.32
UC2842ADG4	D	SOIC	14	50	507	8	3940	4.32
UC2842ADW	DW	SOIC	16	40	507	12.83	5080	6.6
UC2842ADW.A	DW	SOIC	16	40	507	12.83	5080	6.6
UC2842AN	P	PDIP	8	50	506	13.97	11230	4.32
UC2842AN	P	PDIP	8	50	506	13.97	11230	4.32
UC2842AN.A	P	PDIP	8	50	506	13.97	11230	4.32
UC2842AN.A	P	PDIP	8	50	506	13.97	11230	4.32
UC2842ANG4	P	PDIP	8	50	506	13.97	11230	4.32
UC2842ANG4	P	PDIP	8	50	506	13.97	11230	4.32
UC2843AD8	D	SOIC	8	75	507	8	3940	4.32
UC2843AD8.A	D	SOIC	8	75	507	8	3940	4.32
UC2843AD8G4	D	SOIC	8	75	507	8	3940	4.32
UC2843AN	P	PDIP	8	50	506	13.97	11230	4.32
UC2843AN	P	PDIP	8	50	506	13.97	11230	4.32
UC2843AN.A	P	PDIP	8	50	506	13.97	11230	4.32

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UC2843AN.A	P	PDIP	8	50	506	13.97	11230	4.32
UC2843ANG4	P	PDIP	8	50	506	13.97	11230	4.32
UC2843ANG4	P	PDIP	8	50	506	13.97	11230	4.32
UC2844AN	P	PDIP	8	50	506	13.97	11230	4.32
UC2844AN	P	PDIP	8	50	506	13.97	11230	4.32
UC2844AN.A	P	PDIP	8	50	506	13.97	11230	4.32
UC2844AN.A	P	PDIP	8	50	506	13.97	11230	4.32
UC2844ANG4	P	PDIP	8	50	506	13.97	11230	4.32
UC2844ANG4	P	PDIP	8	50	506	13.97	11230	4.32
UC2845AD	D	SOIC	14	50	507	8	3940	4.32
UC2845AD.A	D	SOIC	14	50	507	8	3940	4.32
UC2845ADW	DW	SOIC	16	40	507	12.83	5080	6.6
UC2845ADW.A	DW	SOIC	16	40	507	12.83	5080	6.6
UC2845AN	P	PDIP	8	50	506	13.97	11230	4.32
UC2845AN	P	PDIP	8	50	506	13.97	11230	4.32
UC2845AN.A	P	PDIP	8	50	506	13.97	11230	4.32
UC2845AN.A	P	PDIP	8	50	506	13.97	11230	4.32
UC2845ANG4	P	PDIP	8	50	506	13.97	11230	4.32
UC2845ANG4	P	PDIP	8	50	506	13.97	11230	4.32
UC3842AD	D	SOIC	14	50	507	8	3940	4.32
UC3842AD.A	D	SOIC	14	50	507	8	3940	4.32
UC3842ADG4	D	SOIC	14	50	507	8	3940	4.32
UC3842ADW	DW	SOIC	16	40	507	12.83	5080	6.6
UC3842ADW.A	DW	SOIC	16	40	507	12.83	5080	6.6
UC3842AN	P	PDIP	8	50	506	13.97	11230	4.32
UC3842AN	P	PDIP	8	50	506	13.97	11230	4.32
UC3842AN.A	P	PDIP	8	50	506	13.97	11230	4.32
UC3842AN.A	P	PDIP	8	50	506	13.97	11230	4.32
UC3842ANG4	P	PDIP	8	50	506	13.97	11230	4.32
UC3842ANG4	P	PDIP	8	50	506	13.97	11230	4.32
UC3843AD	D	SOIC	14	50	507	8	3940	4.32
UC3843AD.A	D	SOIC	14	50	507	8	3940	4.32
UC3843ADG4	D	SOIC	14	50	507	8	3940	4.32
UC3843AN	P	PDIP	8	50	506	13.97	11230	4.32
UC3843AN	P	PDIP	8	50	506	13.97	11230	4.32
UC3843AN.A	P	PDIP	8	50	506	13.97	11230	4.32
UC3843AN.A	P	PDIP	8	50	506	13.97	11230	4.32
UC3843ANG4	P	PDIP	8	50	506	13.97	11230	4.32
UC3843ANG4	P	PDIP	8	50	506	13.97	11230	4.32
UC3844AD	D	SOIC	14	50	507	8	3940	4.32
UC3844AD.A	D	SOIC	14	50	507	8	3940	4.32
UC3844AD8	D	SOIC	8	75	507	8	3940	4.32
UC3844AD8.A	D	SOIC	8	75	507	8	3940	4.32

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UC3844AD8G4	D	SOIC	8	75	507	8	3940	4.32
UC3844AN	P	PDIP	8	50	506	13.97	11230	4.32
UC3844AN	P	PDIP	8	50	506	13.97	11230	4.32
UC3844AN.A	P	PDIP	8	50	506	13.97	11230	4.32
UC3844AN.A	P	PDIP	8	50	506	13.97	11230	4.32
UC3844ANG4	P	PDIP	8	50	506	13.97	11230	4.32
UC3844ANG4	P	PDIP	8	50	506	13.97	11230	4.32
UC3845AD	D	SOIC	14	50	507	8	3940	4.32
UC3845AD.A	D	SOIC	14	50	507	8	3940	4.32
UC3845ADG4	D	SOIC	14	50	507	8	3940	4.32
UC3845AN	P	PDIP	8	50	506	13.97	11230	4.32
UC3845AN.A	P	PDIP	8	50	506	13.97	11230	4.32
UC3845ANG4	P	PDIP	8	50	506	13.97	11230	4.32

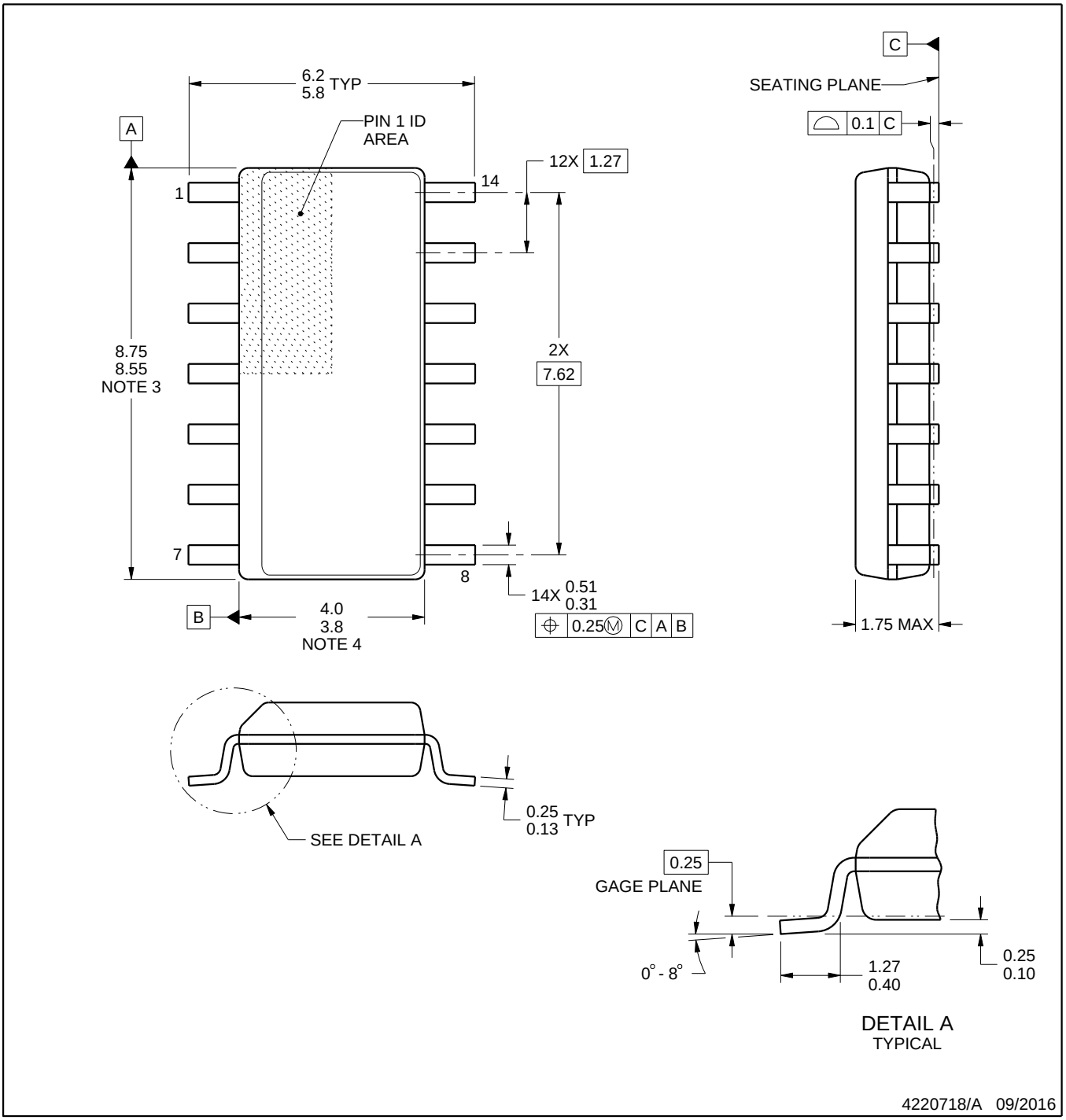


PACKAGE OUTLINE

D0014A

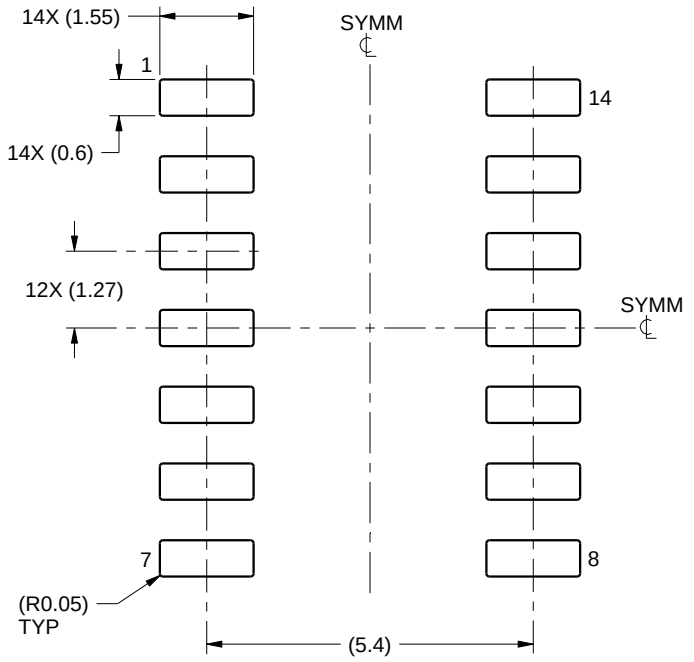
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

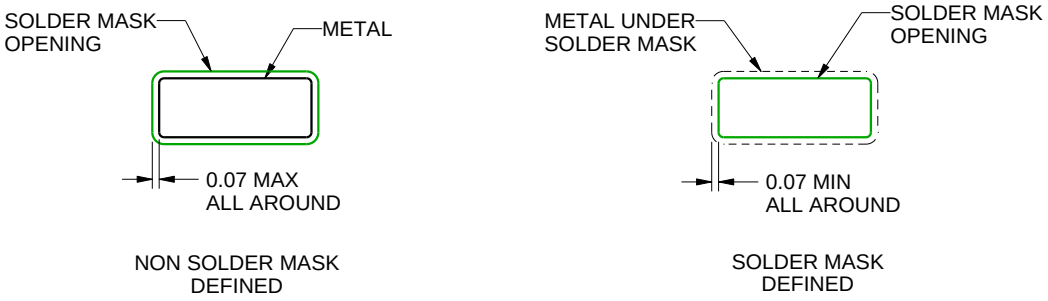


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

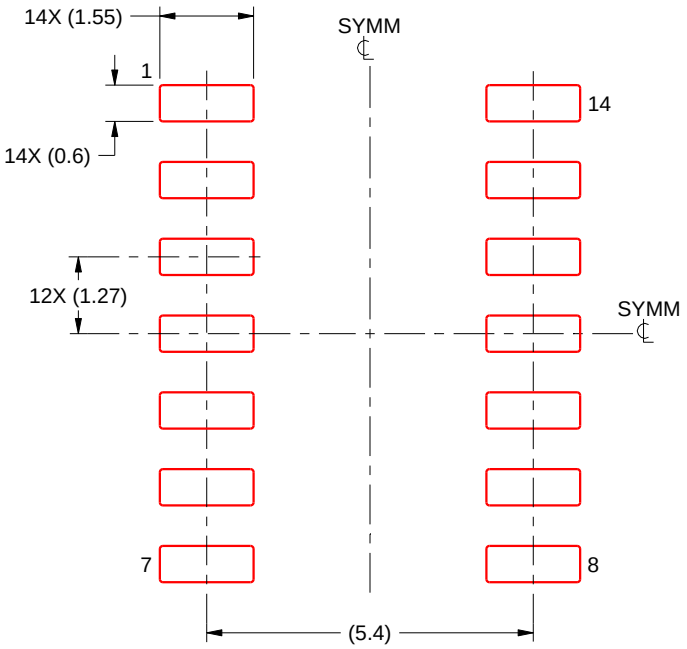
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

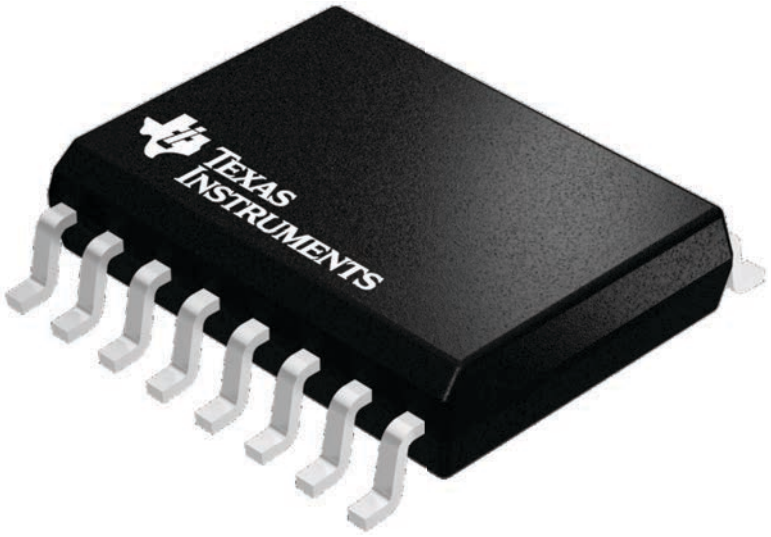
DW 16

SOIC - 2.65 mm max height

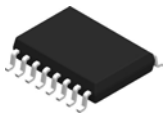
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

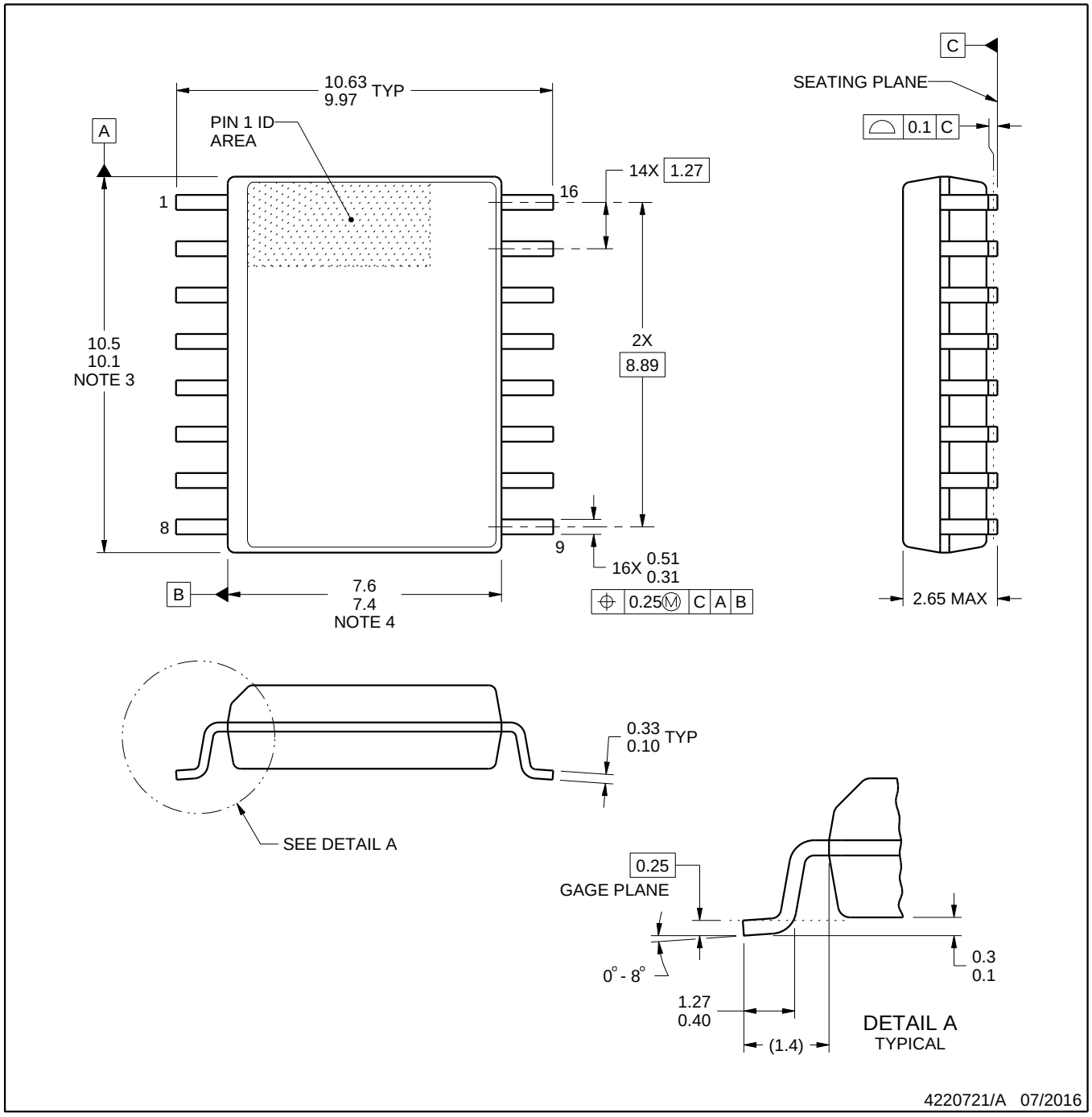


PACKAGE OUTLINE

DW0016A

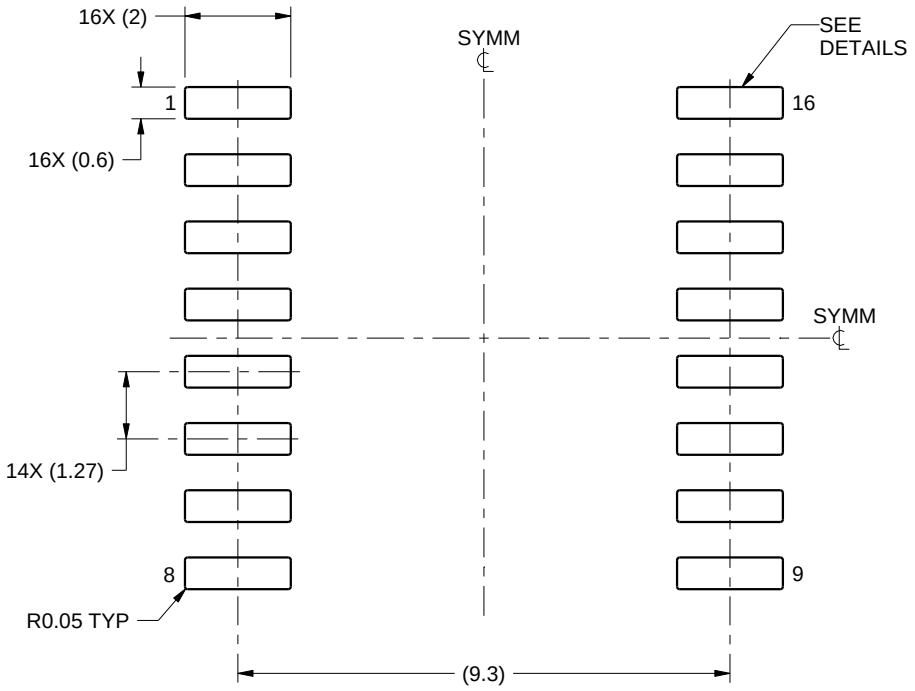
SOIC - 2.65 mm max height

SOIC

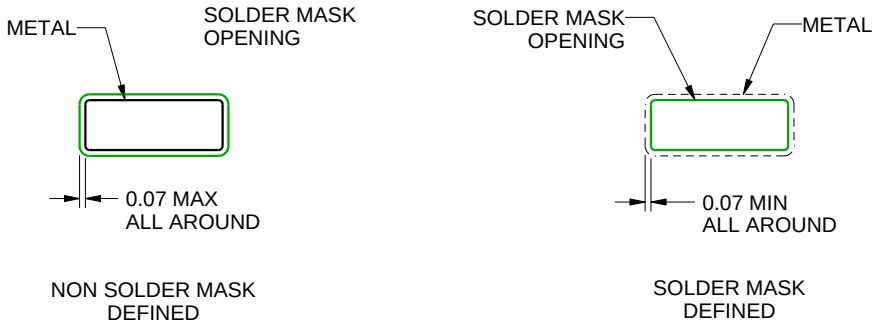


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

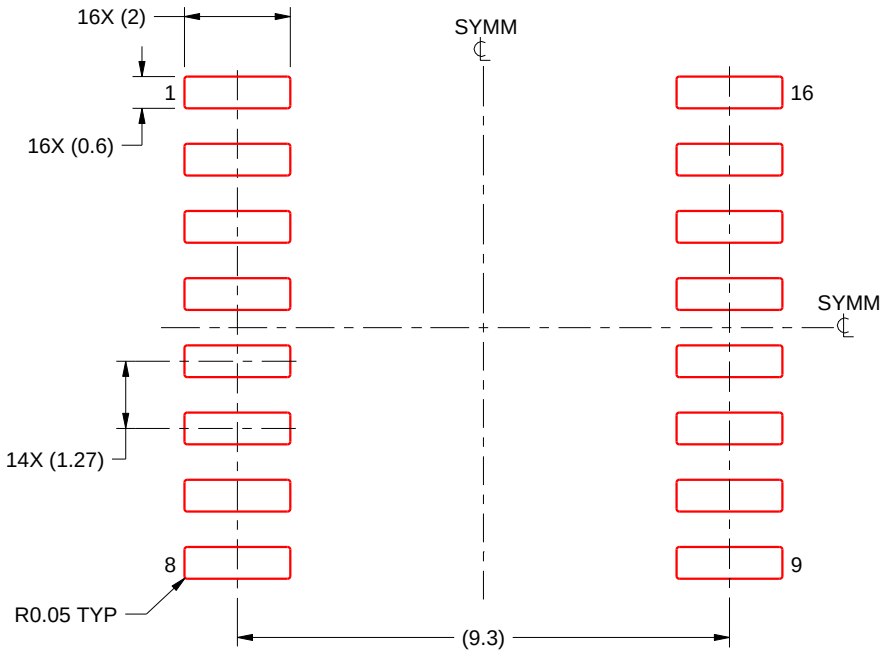


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

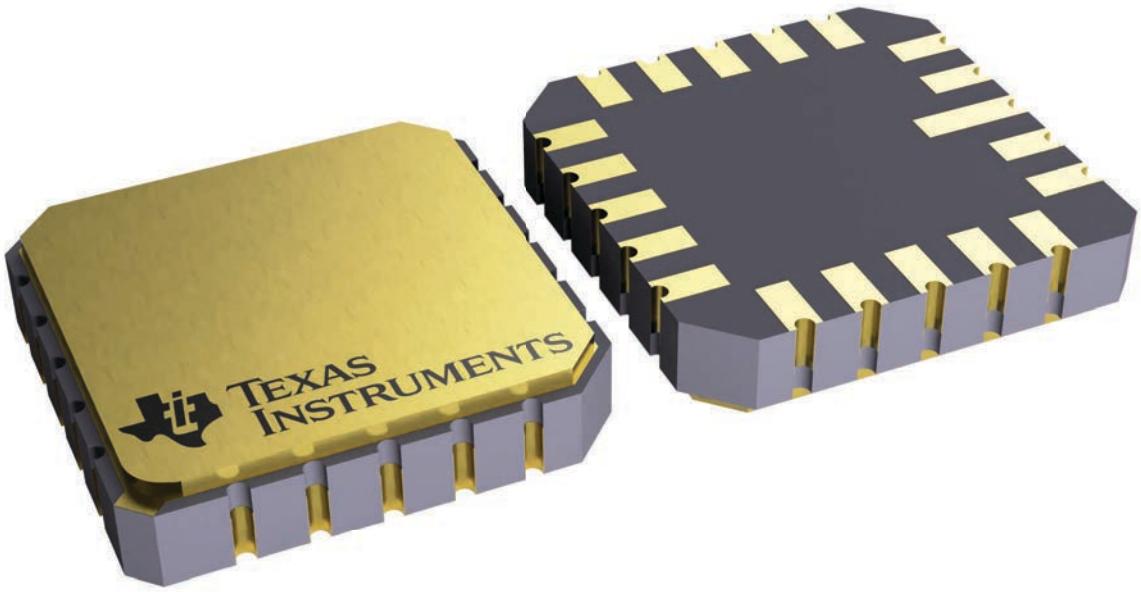
FK 20

LCCC - 2.03 mm max height

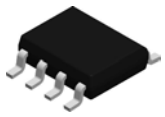
8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

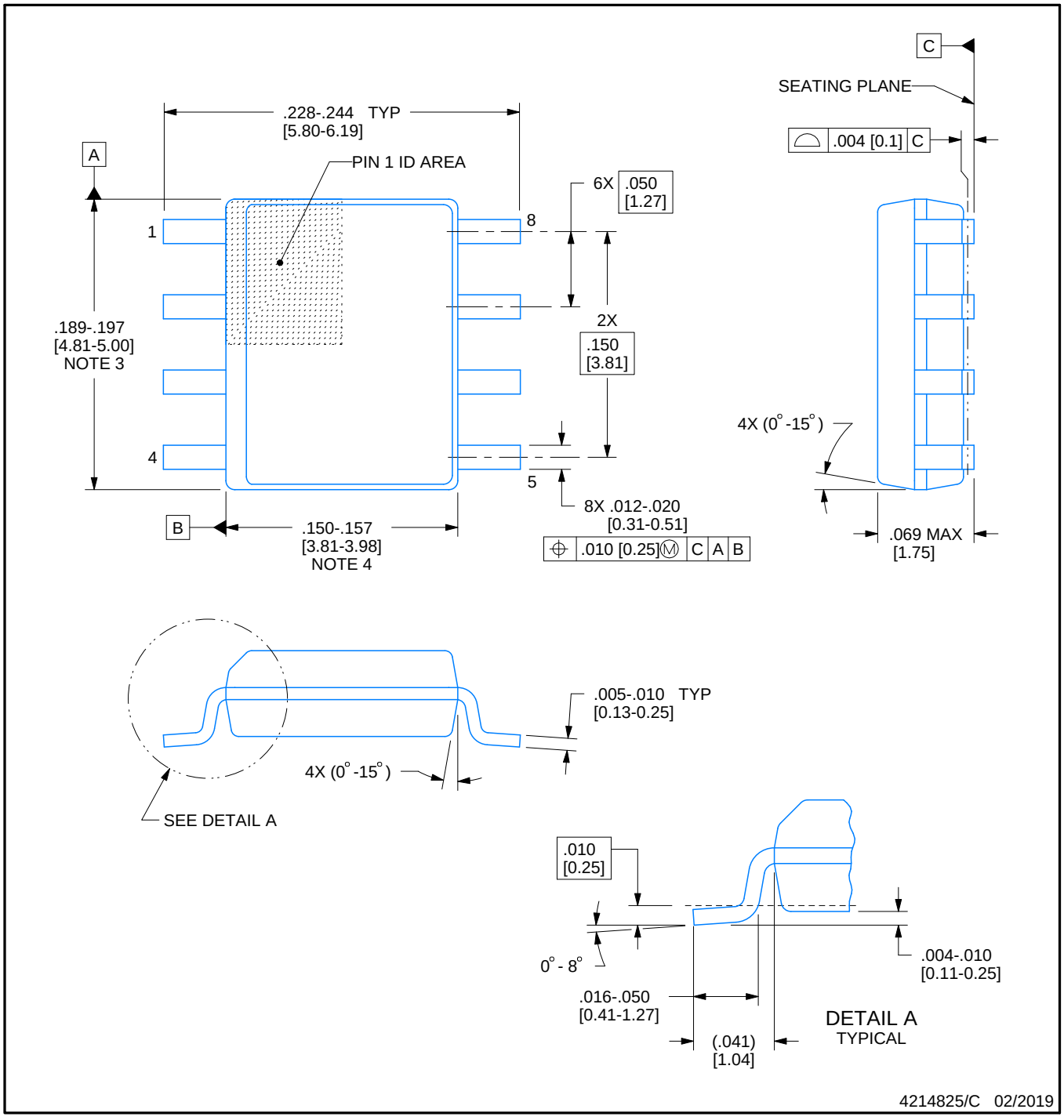


PACKAGE OUTLINE

D0008A

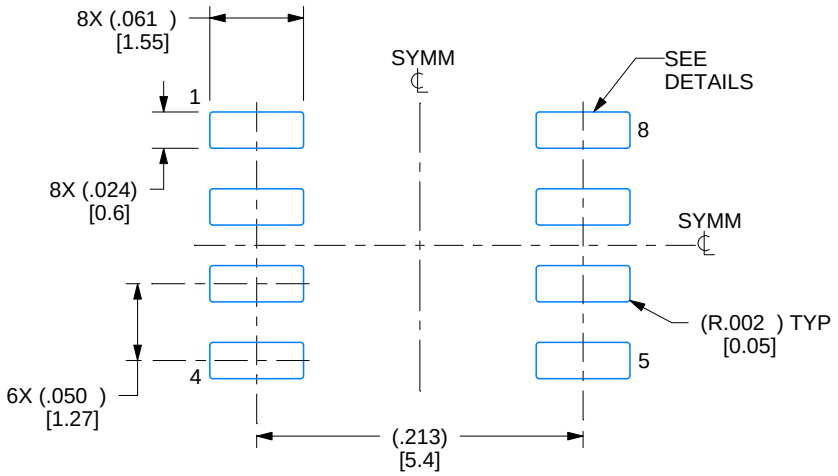
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

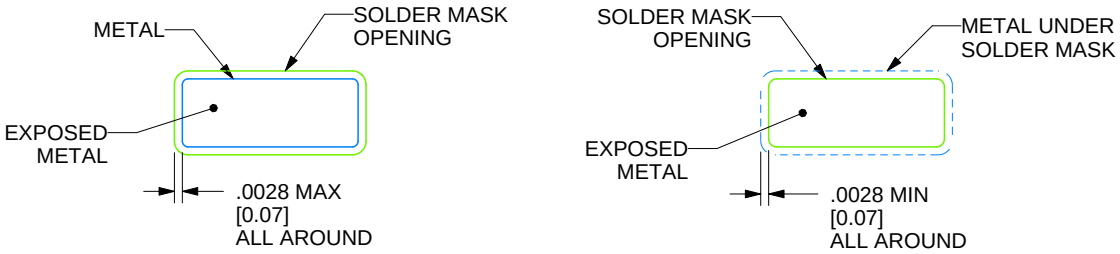


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

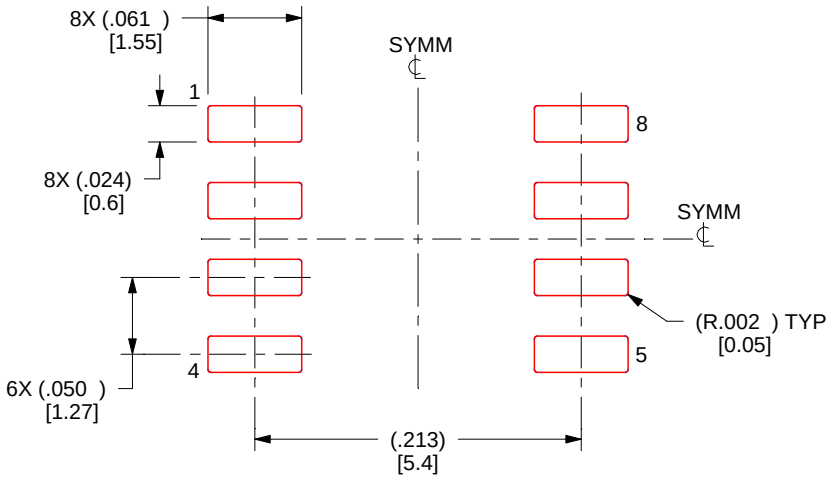
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



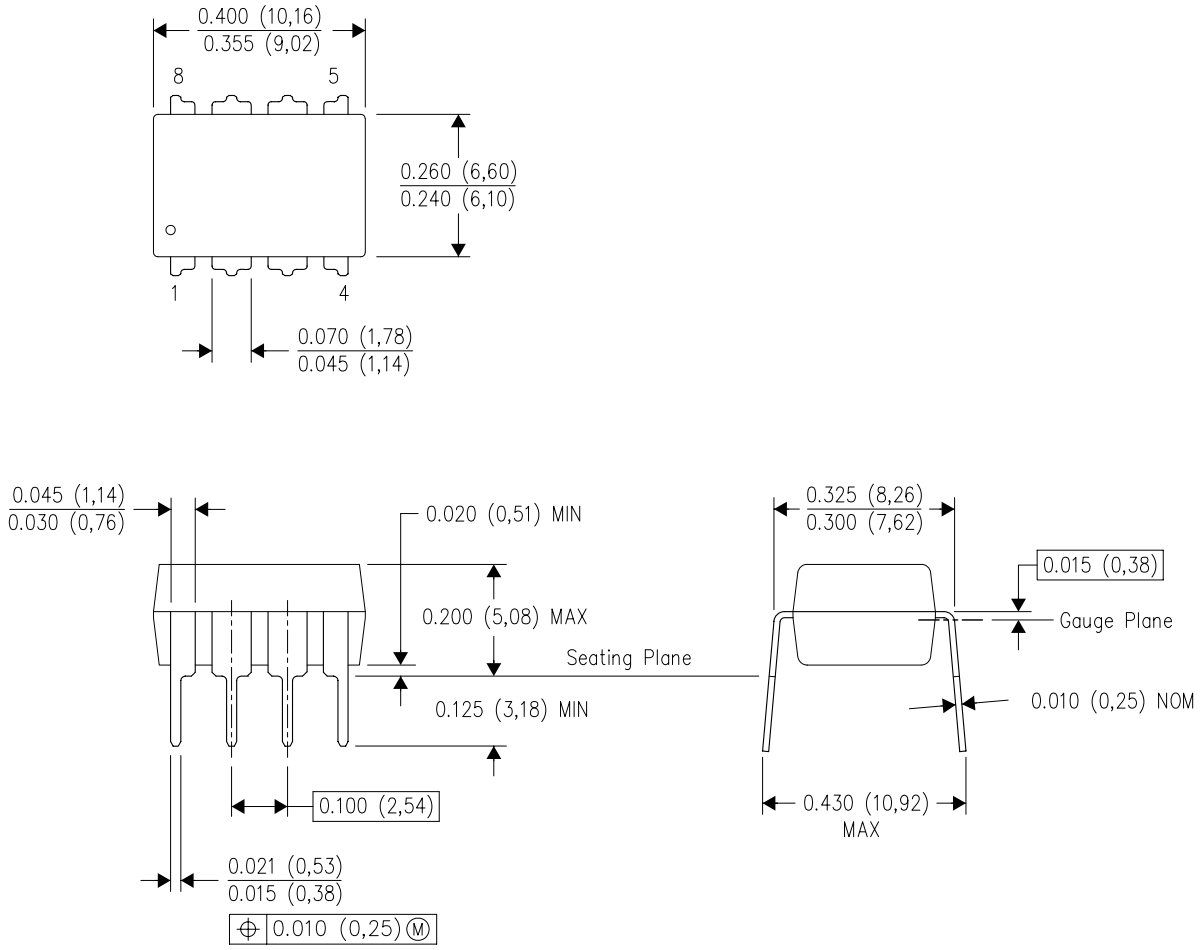
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



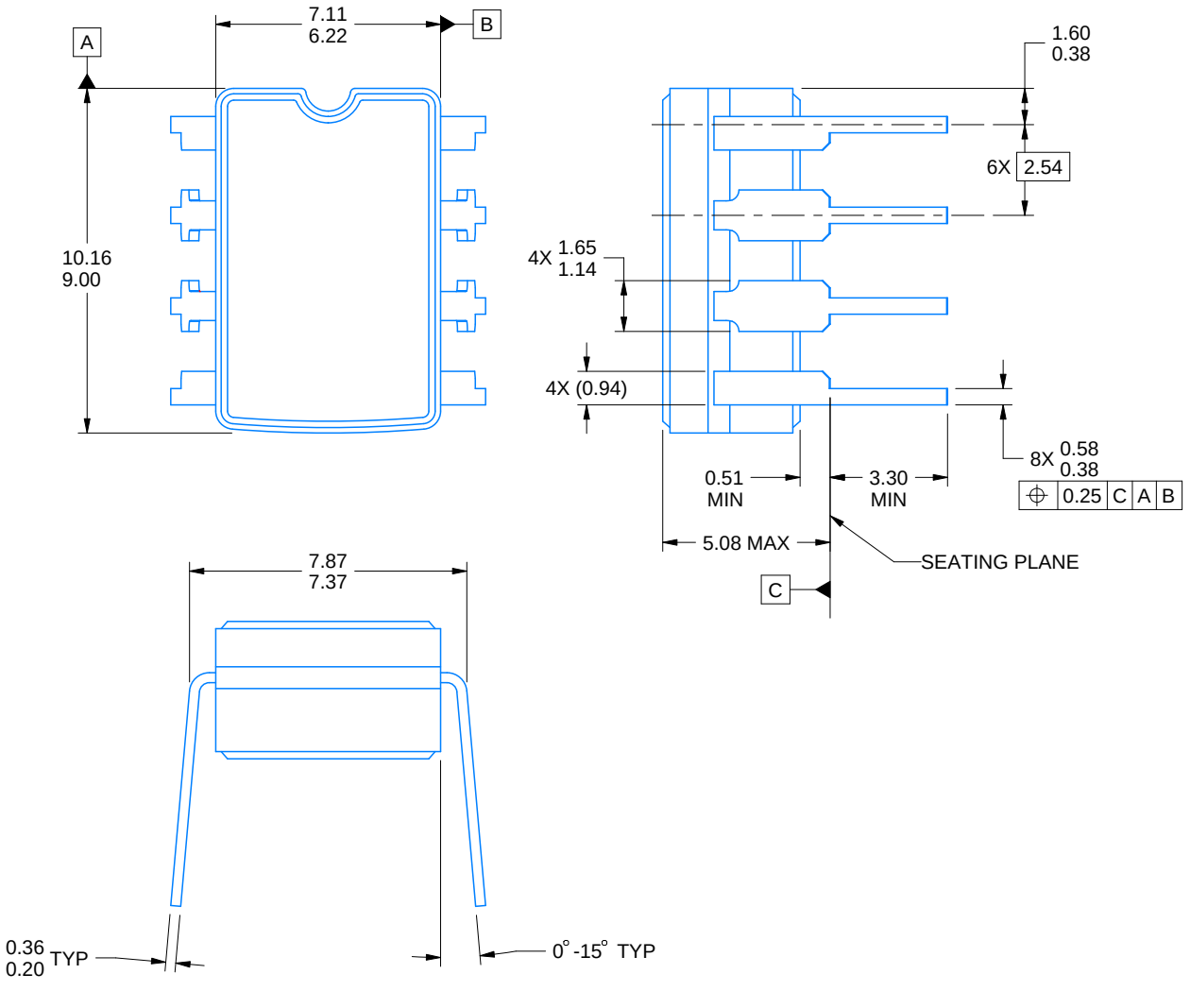
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

PACKAGE OUTLINE

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



4230036/A 09/2023

NOTES:

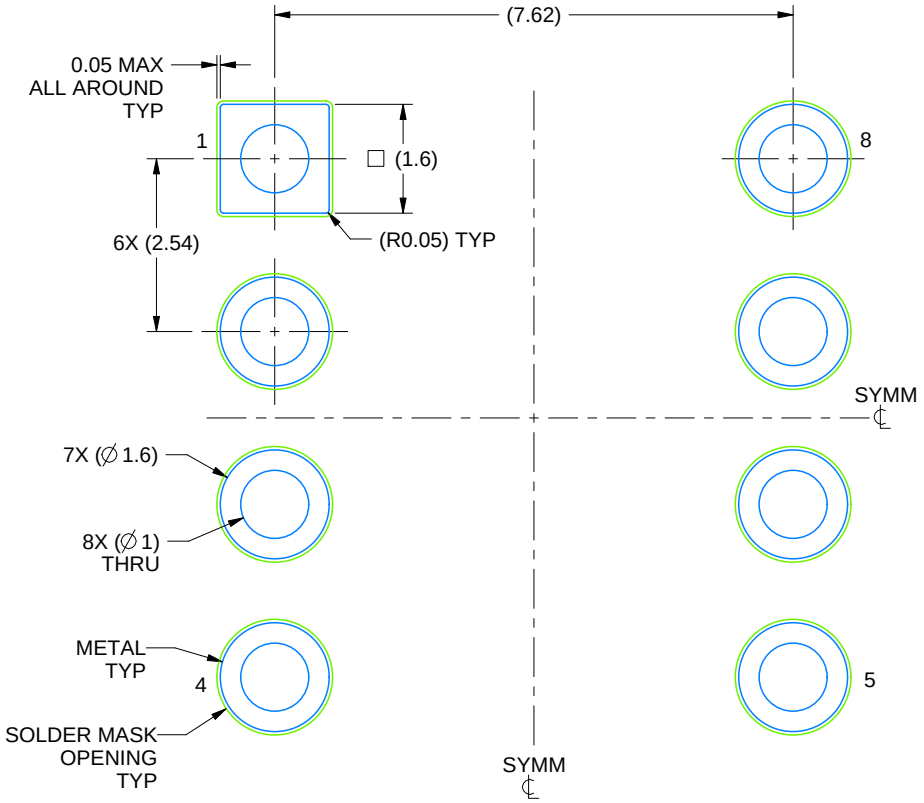
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package can be hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification.
5. Falls within MIL STD 1835 GDIP1-T8

EXAMPLE BOARD LAYOUT

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



LAND PATTERN EXAMPLE
NON SOLDER MASK DEFINED
SCALE: 9X

4230036/A 09/2023

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