

## ADVANCED REGULATING PULSE WIDTH MODULATORS

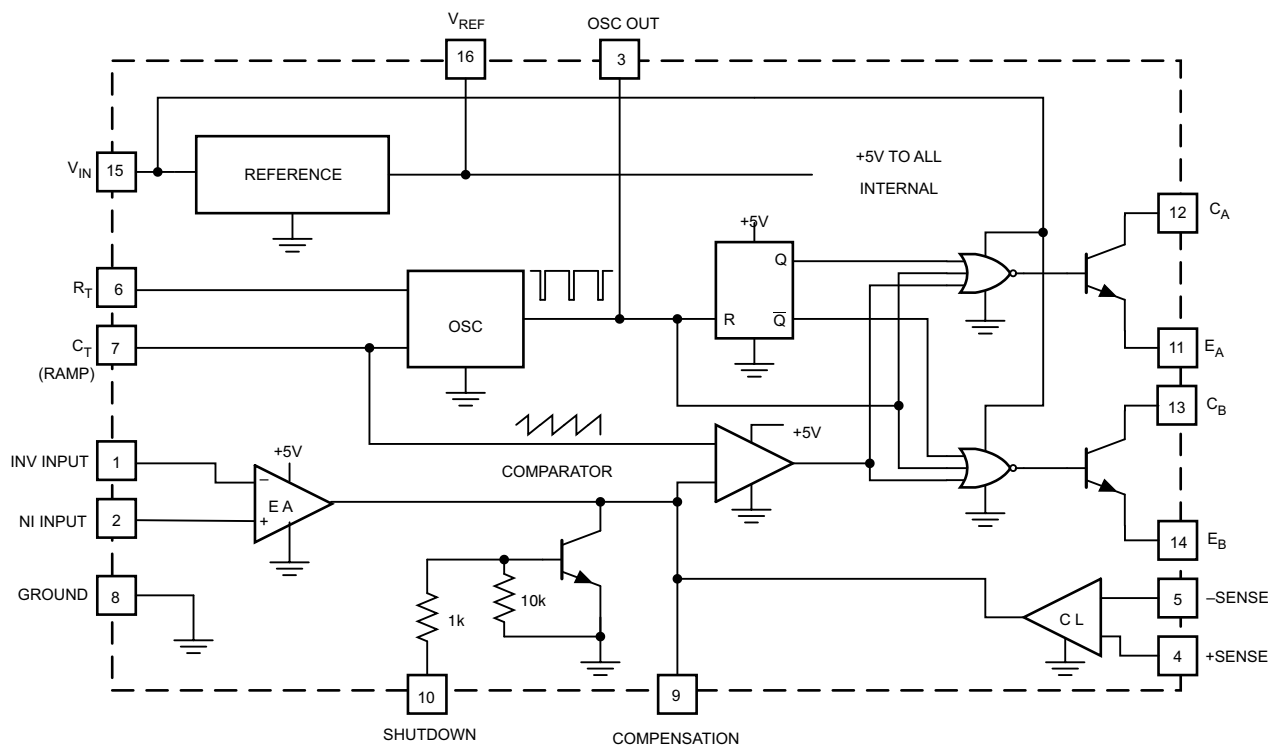
### FEATURES

- Complete PWM Power Control Circuitry
- Uncommitted Outputs for Single-Ended or Push-Pull Applications
- Low Standby Current . . . 8 mA Typical
- Interchangeable With SG1524, SG2524 and SG3524, Respectively

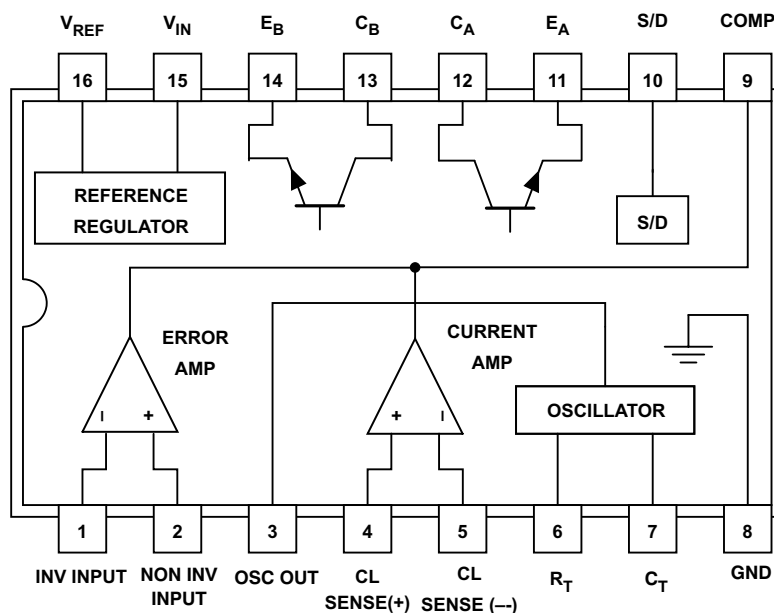
### DESCRIPTION

The UC1524, UC2524 and UC3524 incorporate on a single monolithic chip all the functions required for the construction of regulating power supplies, inverters or switching regulators. They can also be used as the control element for high-power-output applications. The UC1524 family was designed for switching regulators of either polarity, transformer-coupled dc-to-dc converters, transformerless voltage doublers and polarity converter applications employing fixed-frequency, pulse-width modulation techniques. The dual alternating outputs allow either single-ended or push-pull applications. Each device includes an on-chip reference, error amplifier, programmable oscillator, pulse-steering flip-flop, two uncommitted output transistors, a high-gain comparator, and current-limiting and shut-down circuitry. The UC1524 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The UC2524 and UC3524 are designed for operation from  $-25^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  and  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ , respectively.

### BLOCK DIAGRAM



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**CONNECTION DIAGRAM****ABSOLUTE MAXIMUM RATINGS**

over operating free-air temperature range (unless otherwise noted)

|                   |                                      | UNIT            |
|-------------------|--------------------------------------|-----------------|
| $V_{CC}$          | Supply voltage <sup>(1)(2)</sup>     | 40 V            |
|                   | Collector output current             | 100 mA          |
|                   | Reference output current             | 50 mA           |
|                   | Current through $C_T$ terminalg      | –50 mA          |
| Power dissipation | $T_A = 25^\circ\text{C}^{(3)}$       | 1000 mW         |
|                   | $T_C = 25^\circ\text{C}^{(3)}$       | 2000 mW         |
|                   | Operating junction temperature range | –55°C to 150°C  |
|                   | Storage temperature range            | –65°C to +150°C |

(1) All voltage values are with respect to the ground terminal, pin 8.

(2) The reference regulator may be bypassed for operation from a fixed 5 V supply by connecting the  $V_{CC}$  and reference output pins both to the supply voltage. In this configuration the maximum supply voltage is 6 V.

(3) Consult packaging section of data book for thermal limitations and considerations of package.

**RECOMMENDED OPERATING CONDITIONS**

over operating free-air temperature range (unless otherwise noted)

|                                     |                                | MIN   | NOM | MAX | UNIT          |
|-------------------------------------|--------------------------------|-------|-----|-----|---------------|
| $V_{CC}$                            | Supply voltage                 | 8     |     | 40  | V             |
|                                     | Reference output current       | 0     |     | 20  | mA            |
|                                     | Current through $C_T$ terminal | –0.03 |     | –2  | mA            |
| $R_T$                               | Timing resistor                | 1.8   |     | 100 | k $\Omega$    |
| $C_T$                               | Timing capacitor               | 0.001 |     | 0.1 | $\mu\text{F}$ |
| Operating ambient temperature range | UC1524                         | –55   |     | 125 | °C            |
|                                     | UC2524                         | –25   |     | 85  |               |
|                                     | UC3524                         | 0     |     | 70  |               |

## ELECTRICAL CHARACTERISTICS

these specifications apply for  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$  for the UC1524,  $-25^\circ\text{C}$  to  $85^\circ\text{C}$  for the UC2524, and  $0^\circ\text{C}$  to  $70^\circ\text{C}$  for the UC3524,  $V_{IN} = 20\text{ V}$ , and  $f = 20\text{ kHz}$ ,  $T_A = T_J$ , over operating free-air temperature range (unless otherwise noted)

| PARAMETER                    | TEST CONDITIONS                                                             | UC1524/UC2524 |      |     | UC3524 |      |     | UNIT  |
|------------------------------|-----------------------------------------------------------------------------|---------------|------|-----|--------|------|-----|-------|
|                              |                                                                             | MIN           | TYP  | MAX | MIN    | TYP  | MAX |       |
| REFERENCE SECTION            |                                                                             |               |      |     |        |      |     |       |
| Output voltage               |                                                                             | 4.8           | 5.0  | 5.2 | 4.6    | 5.0  | 5.4 | V     |
| Line regulation              | V <sub>IN</sub> = 8 V to 40 V                                               |               | 10   | 20  |        | 10   | 30  | mV    |
| Load regulation              | I <sub>L</sub> = 0 mA to 20 mA                                              |               | 20   | 50  |        | 20   | 50  | mV    |
| Ripple rejection             | f = 120 Hz, T <sub>J</sub> = 25°C                                           |               | 66   |     |        | 66   |     | dB    |
| Short circuit current limit  | V <sub>REF</sub> = 0, T <sub>J</sub> = 25°C                                 |               | 100  |     |        | 100  |     | mA    |
| Temperature stability        | Over operating temperature range                                            |               | 0.3% | 1%  |        | 0.3% | 1%  |       |
| Long term stability          | T <sub>J</sub> = 125°C, t = 1000 Hrs                                        |               | 20   |     |        | 20   |     | mV    |
| OSCILLATOR SECTION           |                                                                             |               |      |     |        |      |     |       |
| Maximum frequency            | C <sub>T</sub> = 1 nF, R <sub>T</sub> = 2 kΩ                                |               | 300  |     |        | 300  |     | kHz   |
| Initial accuracy             | R <sub>T</sub> and C <sub>T</sub> constant                                  |               | 5%   |     |        | 5%   |     |       |
| Voltage stability            | V <sub>IN</sub> = 8 V to 40 V, T <sub>J</sub> = 25°C                        |               |      | 1%  |        |      | 1%  |       |
| Temperature stability        | Over operating temperature range                                            |               |      | 5%  |        |      | 5%  |       |
| Output amplitude             | Pin 3, T <sub>J</sub> = 25°C                                                |               | 3.5  |     |        | 3.5  |     | V     |
| Output pulse width           | C <sub>T</sub> = 0.01 mfd, T <sub>J</sub> = 25°C                            |               | 0.5  |     |        | 0.5  |     | μs    |
| ERROR AMPLIFIER SECTION      |                                                                             |               |      |     |        |      |     |       |
| Input offset voltage         | V <sub>CM</sub> = 2.5 V                                                     |               | 0.5  | 5   |        | 2    | 10  | mV    |
| Input bias current           | V <sub>CM</sub> = 2.5 V                                                     |               | 2    | 10  |        | 2    | 10  | μA    |
| Open loop voltage gain       |                                                                             | 72            | 80   |     | 60     | 80   |     | dB    |
| Common mode voltage          | T <sub>J</sub> = 25°C                                                       | 1.8           |      | 3.4 | 1.8    |      | 3.4 | V     |
| Common mode rejection ratio  | T <sub>J</sub> = 25°C                                                       |               | 70   |     |        | 70   |     | dB    |
| Small signal bandwidth       | A <sub>V</sub> = 0 dB, T <sub>J</sub> = 25°C                                |               | 3    |     |        | 3    |     | MHz   |
| Output voltage               | T <sub>J</sub> = 25°C                                                       | 0.5           |      | 3.8 | 0.5    |      | 3.8 | V     |
| COMPARATOR SECTION           |                                                                             |               |      |     |        |      |     |       |
| Duty-cycle                   | % Each output on                                                            | 0%            |      | 45% | 0%     |      | 45% |       |
| Input threshold              | Zero duty-cycle                                                             |               | 1    |     |        | 1    |     | V     |
|                              | Maximum duty-cycle                                                          |               | 3.5  |     |        | 3.5  |     |       |
| Input bias current           |                                                                             |               | 1    |     |        | 1    |     | μA    |
| CURRENT LIMITING SECTION     |                                                                             |               |      |     |        |      |     |       |
| Sense voltage                | Pin 9 = 2 V with error amplifier set for maximum out, T <sub>J</sub> = 25°C | 190           | 200  | 210 | 180    | 200  | 220 | mV    |
| Sense voltage T.C.           |                                                                             |               | 0.2  |     |        | 0.2  |     | mV/°C |
| Common mode voltage          | T <sub>J</sub> = −55°C to 85°C for the −1 V to 1 V limit                    | −1            |      | 1   | −1     |      | 1   | V     |
|                              | T <sub>J</sub> = 25°C                                                       | −0.3          |      | 1   |        |      |     |       |
| OUTPUT SECTION (EACH OUTPUT) |                                                                             |               |      |     |        |      |     |       |
| Collector-emitter voltage    |                                                                             | 40            |      |     | 40     |      |     | V     |
| Collector leakage current    | V <sub>CE</sub> = 40 V                                                      |               | 0.1  | 50  |        | 0.1  | 50  | μ A   |
| Saturation voltage           | I <sub>C</sub> = 50 mA                                                      |               | 1    | 2   |        | 1    | 2   | V     |
| Emitter output voltage       | V <sub>IN</sub> = 20 V                                                      | 17            | 18   |     | 17     | 18   |     | V     |
| Rise Time                    | R <sub>C</sub> = 2 kΩ, T <sub>J</sub> = 25°C                                |               | 0.2  |     |        | 0.2  |     | μs    |
| Fall Time                    | R <sub>C</sub> = 2 kΩ, T <sub>J</sub> = 25°C                                |               | 0.1  |     |        | 0.1  |     | μs    |
| Total standby current (Note) | V <sub>IN</sub> = 40 V                                                      |               | 8    | 10  |        | 8    | 10  | mA    |

## PRINCIPLES OF OPERATION

The UC1524 is a fixed-frequency pulse-width-modulation voltage regulator control circuit. The regulator operates at a frequency that is programmed by one timing resistor ( $R_T$ ), and one timing capacitor ( $C_T$ ).  $R_T$  establishes a constant charging current for  $C_T$ . This results in a linear voltage ramp at  $C_T$ , which is fed to the comparator providing linear control of the output pulse width by the error amplifier. The UC1524 contains an on-board 5 V regulator that serves as a reference as well as powering the UC1524's internal control circuitry and is also useful in supplying external support functions. This reference voltage is lowered externally by a resistor divider to provide a reference within the common-mode range of the error amplifier or an external reference may be used. The power supply output is sensed by a second resistor divider network to generate a feedback signal to the error amplifier. The amplifier output voltage is then compared to the linear voltage ramp at  $C_T$ . The resulting modulated pulse out of the high-gain comparator is then steered to the appropriate output pass transistor ( $Q_1$  or  $Q_2$ ) by the pulse-steering

flip-flop, which is synchronously toggled by the oscillator output. The oscillator output pulse also serves as a blanking pulse to assure both outputs are never on simultaneously during the transition times. The width of the blanking pulse is controlled by the value of  $C_T$ . The outputs may be applied in a push-pull configuration in which their frequency is half that of the base oscillator. Note that for buck regulator topologies, the two outputs can be wire-ORed for an effective 0-90% duty cycle range. With this connection, the output frequency is the same as the oscillator frequency. The output of the error amplifier shares a common input to the comparator with the current limiting and shutdown circuitry and can be overridden by signals from either of these inputs. This common point is also available externally and may be employed to control the gain of, or to compensate, the error amplifier or to provide additional control to the regulator.

## TYPICAL CHARACTERISTICS

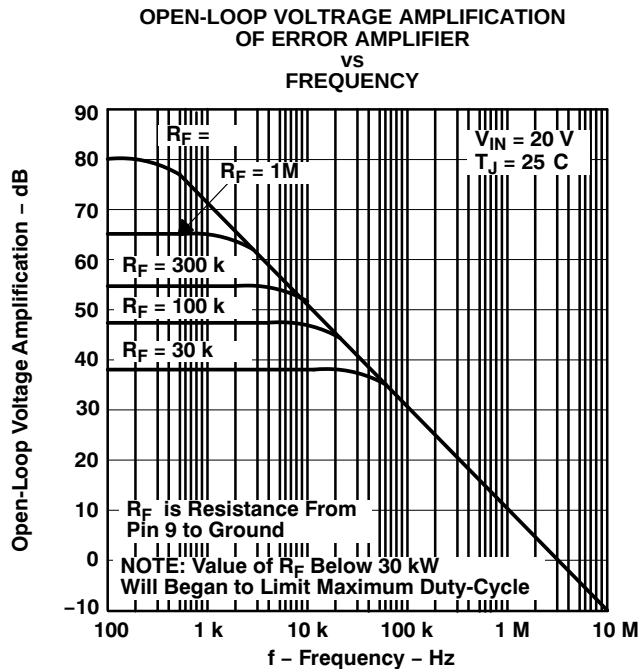


Figure 1.

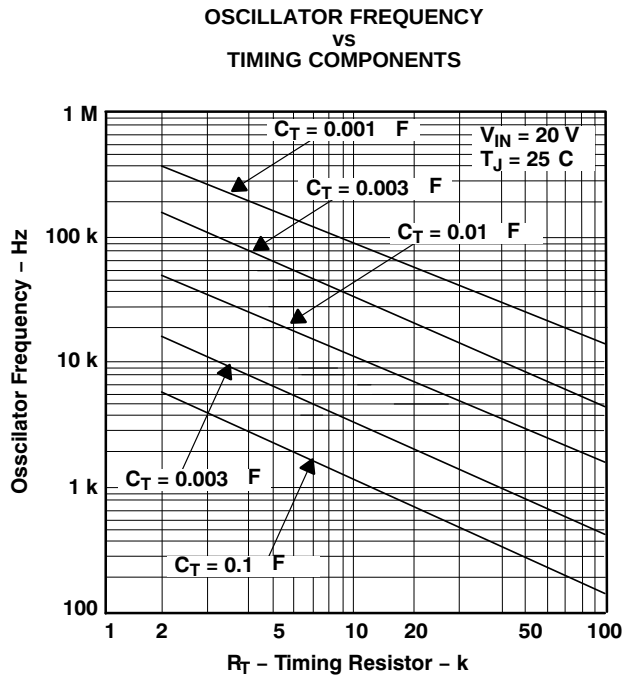


Figure 2.

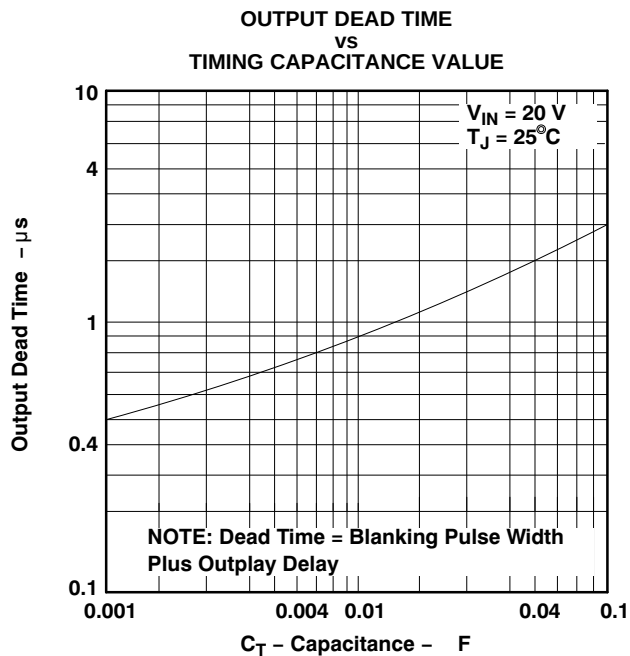


Figure 3.

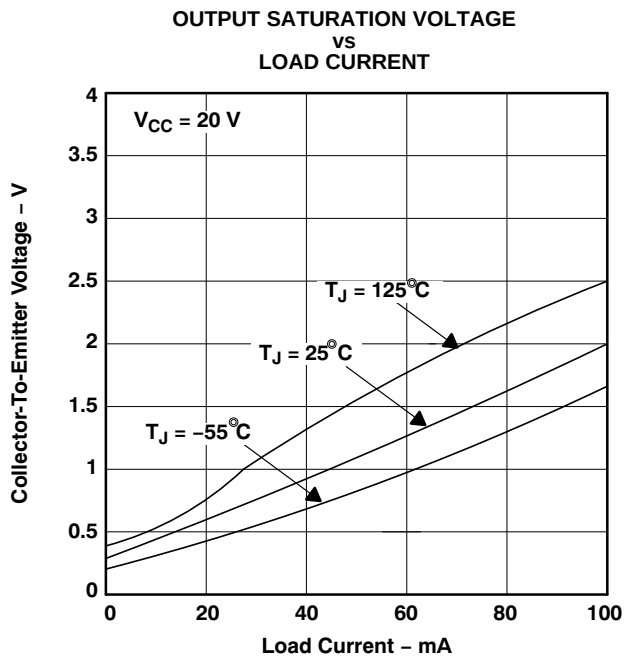


Figure 4.

## APPLICATION INFORMATION

## OSCILLATOR

The oscillator controls the frequency of the UC1524 and is programmed by  $R_T$  and  $C_T$  according to the approximate formula:

$$f = \frac{1.18}{R_T C_T} \quad (1)$$

where

$R_T$  is in  $k\Omega$

$C_T$  is in  $\mu F$

f is in kHz

Practical values of  $C_T$  fall between 1 nF and 100 nF. Practical values of  $R_T$  fall between 1.8 k $\Omega$  and 100 k $\Omega$ . This results in a frequency range typically from 120 Hz to 500 kHz.

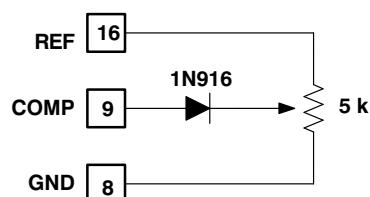
## BLANKING

The output pulse of the oscillator is used as a blanking pulse at the output. This pulse width is controlled by the value of  $C_T$ . If small values of  $C_T$  are required for frequency control, the oscillator output pulse width may still be increased by applying a shunt capacitance of up to 100 pF from pin 3 to ground. If still greater dead-time is required, it should be accomplished by limiting the maximum duty cycle by clamping the output of the error amplifier. This can easily be done with the circuit in [Figure 5](#).

## SYNCHRONOUS OPERATIONS

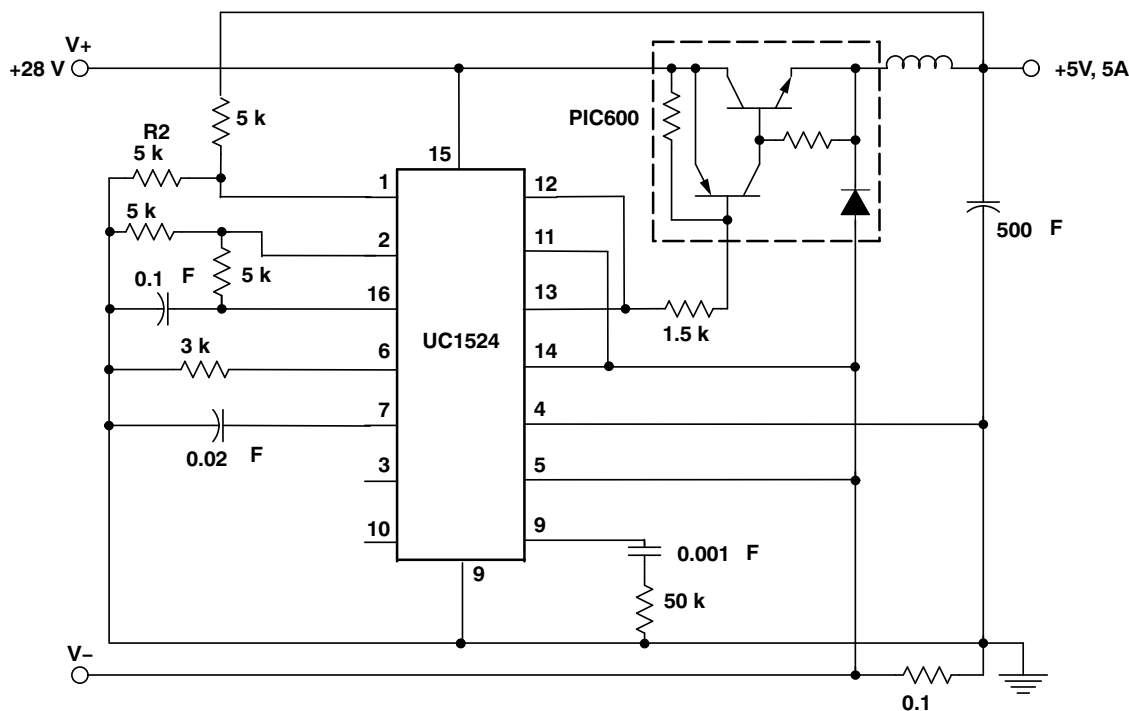
When an external clock is desired, a clock pulse of approximately 3 V can be applied directly to the oscillator output terminal. The impedance to ground at this point is approximately 2 k $\Omega$ . In this configuration R<sub>T</sub> C<sub>T</sub> must be selected for a clock period slightly greater than that of the external clock.

If two or more UC1524 regulators are to be operated synchronously, all oscillator output terminals should be tied together, all  $C_T$  terminals connected to single timing capacitor, and the timing resistor connected to a single  $R_T$  terminal.



### Figure 5. Error Amplifier Clamp

The other R<sub>T</sub> terminals can be left open or shorted to V<sub>REF</sub>. Minimum lead lengths should be used between the C<sub>T</sub> terminals.



### Figure 6. Single-Ended LC Switching Regulator Circuit

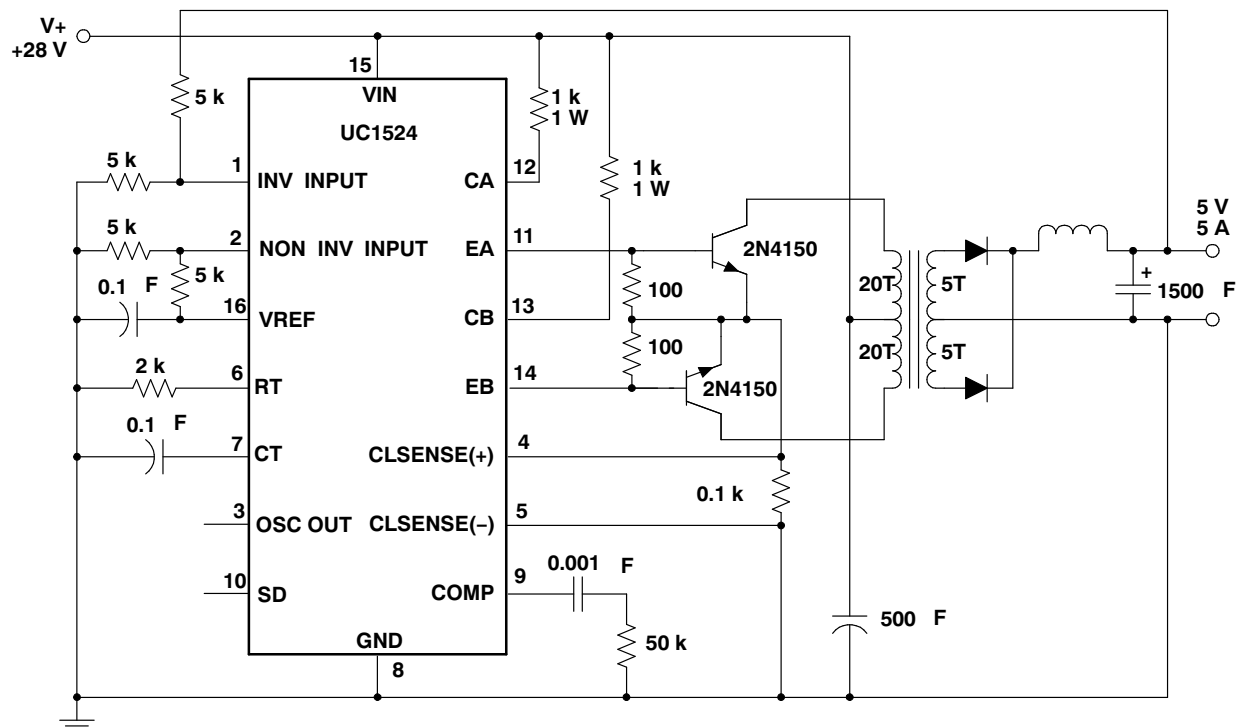


Figure 7. Push-Pull Transformer Coupled Circuit

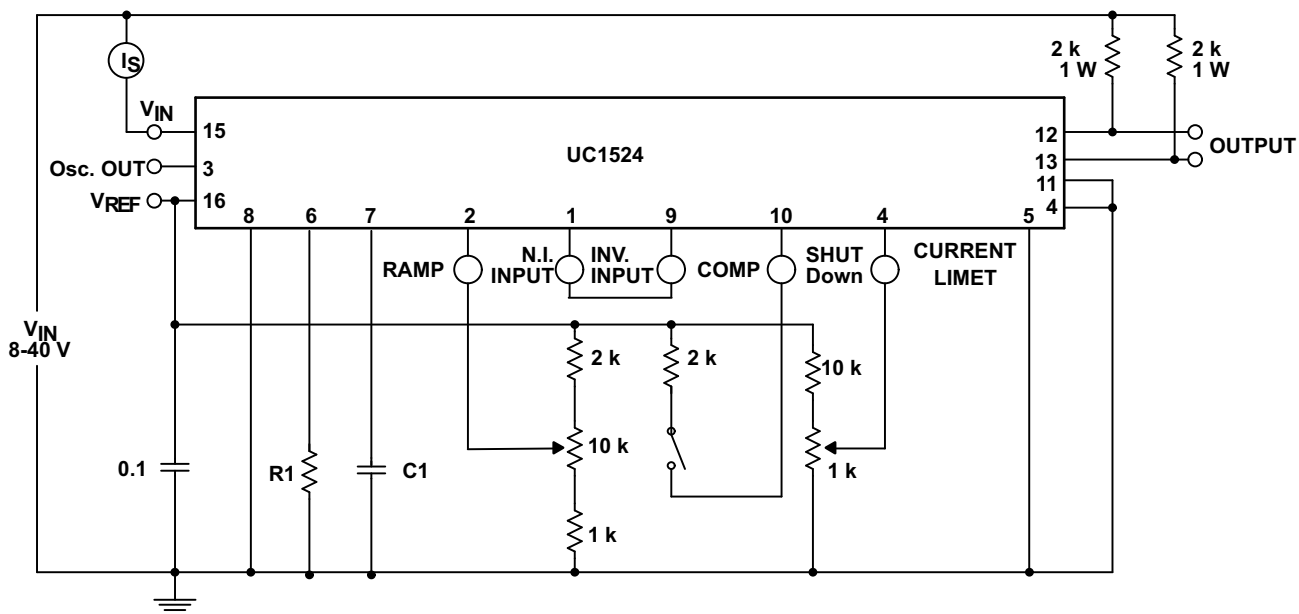


Figure 8. Open Loop Test Circuit

## PACKAGING INFORMATION

| Orderable part number      | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|----------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">UC2524DW</a>   | Obsolete      | Production           | SOIC (DW)   16 | -                     | -           | Call TI                              | Call TI                           | -25 to 85    | UC2524DW            |
| <a href="#">UC3524D</a>    | NRND          | Production           | SOIC (D)   16  | 40   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | 0 to 70      | UC3524D             |
| UC3524D.A                  | NRND          | Production           | SOIC (D)   16  | 40   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | 0 to 70      | UC3524D             |
| <a href="#">UC3524DW</a>   | Active        | Production           | SOIC (DW)   16 | 40   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | 0 to 70      | UC3524DW            |
| UC3524DW.A                 | Active        | Production           | SOIC (DW)   16 | 40   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | 0 to 70      | UC3524DW            |
| <a href="#">UC3524DWTR</a> | NRND          | Production           | SOIC (DW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | 0 to 70      | UC3524DW            |
| UC3524DWTR.A               | NRND          | Production           | SOIC (DW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | 0 to 70      | UC3524DW            |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.





## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| UC3524DWTR | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |

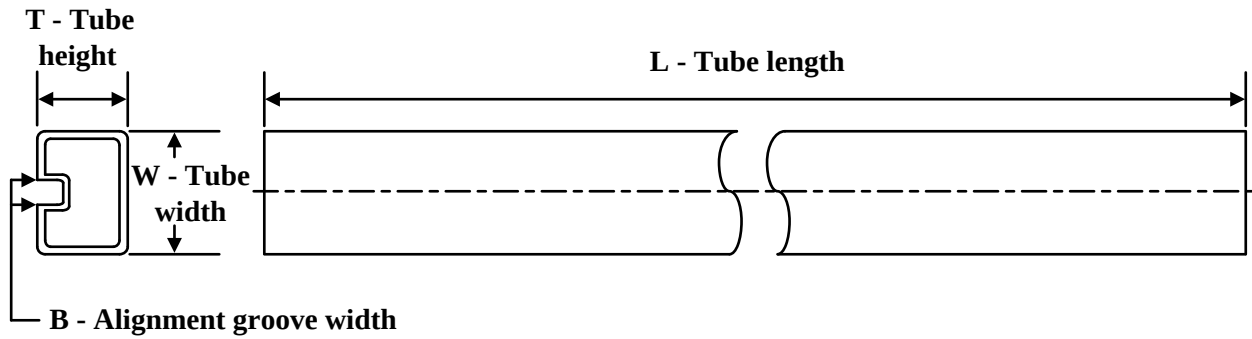
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| UC3524DWTR | SOIC         | DW              | 16   | 2000 | 353.0       | 353.0      | 32.0        |

## TUBE

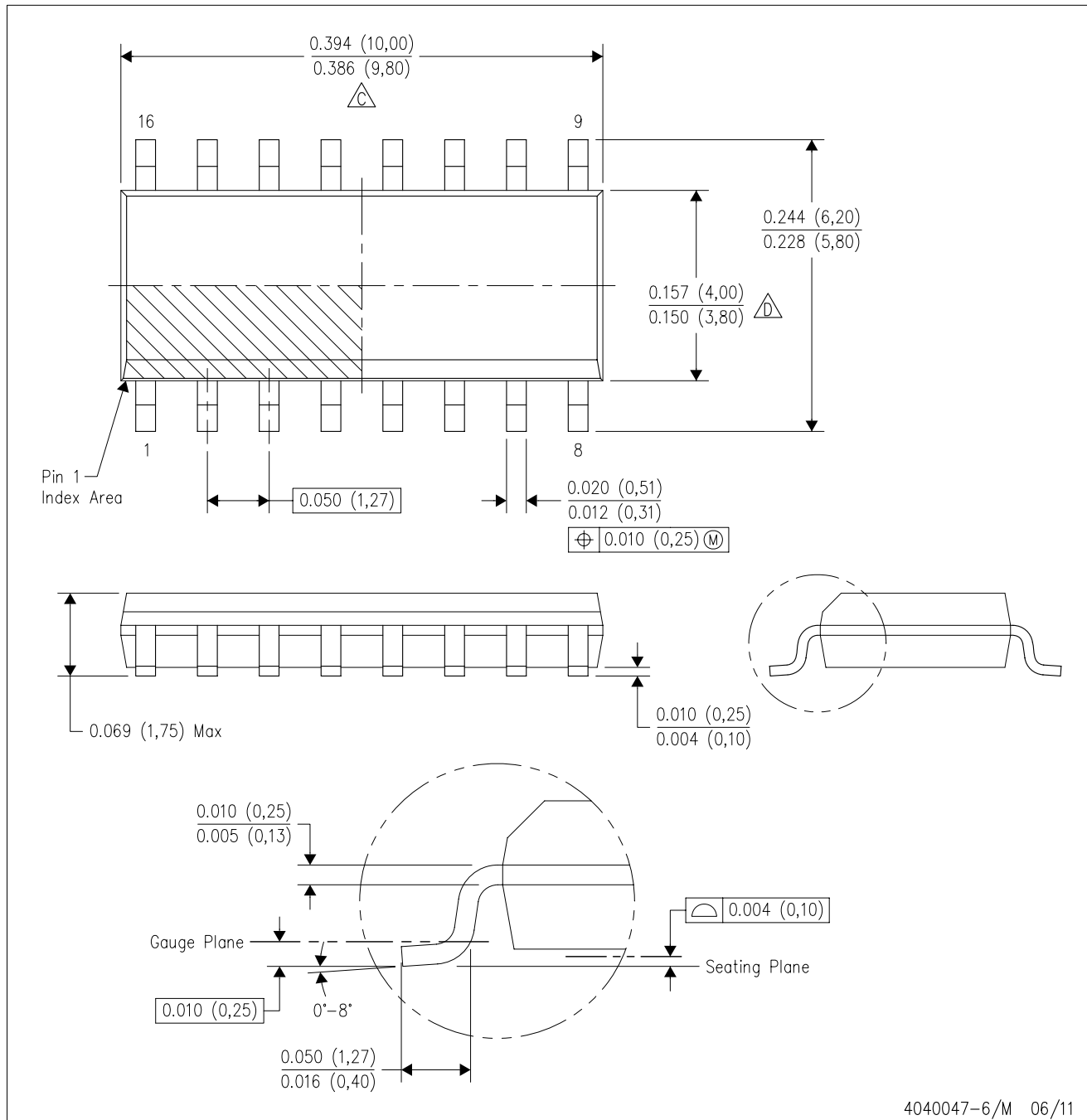


\*All dimensions are nominal

| Device     | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| UC3524D    | D            | SOIC         | 16   | 40  | 506.6  | 8      | 3940   | 4.32   |
| UC3524D.A  | D            | SOIC         | 16   | 40  | 506.6  | 8      | 3940   | 4.32   |
| UC3524DW   | DW           | SOIC         | 16   | 40  | 507    | 12.83  | 5080   | 6.6    |
| UC3524DW.A | DW           | SOIC         | 16   | 40  | 507    | 12.83  | 5080   | 6.6    |

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

## GENERIC PACKAGE VIEW

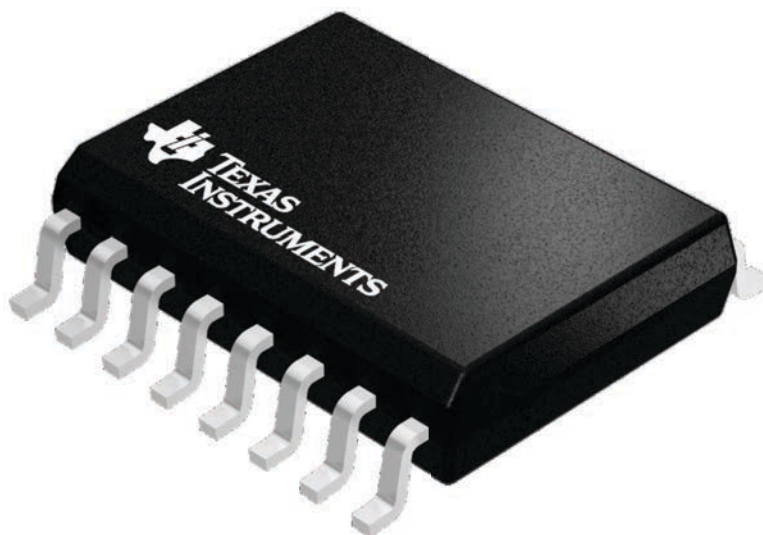
**DW 16**

**SOIC - 2.65 mm max height**

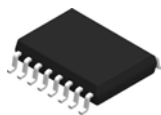
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224780/A

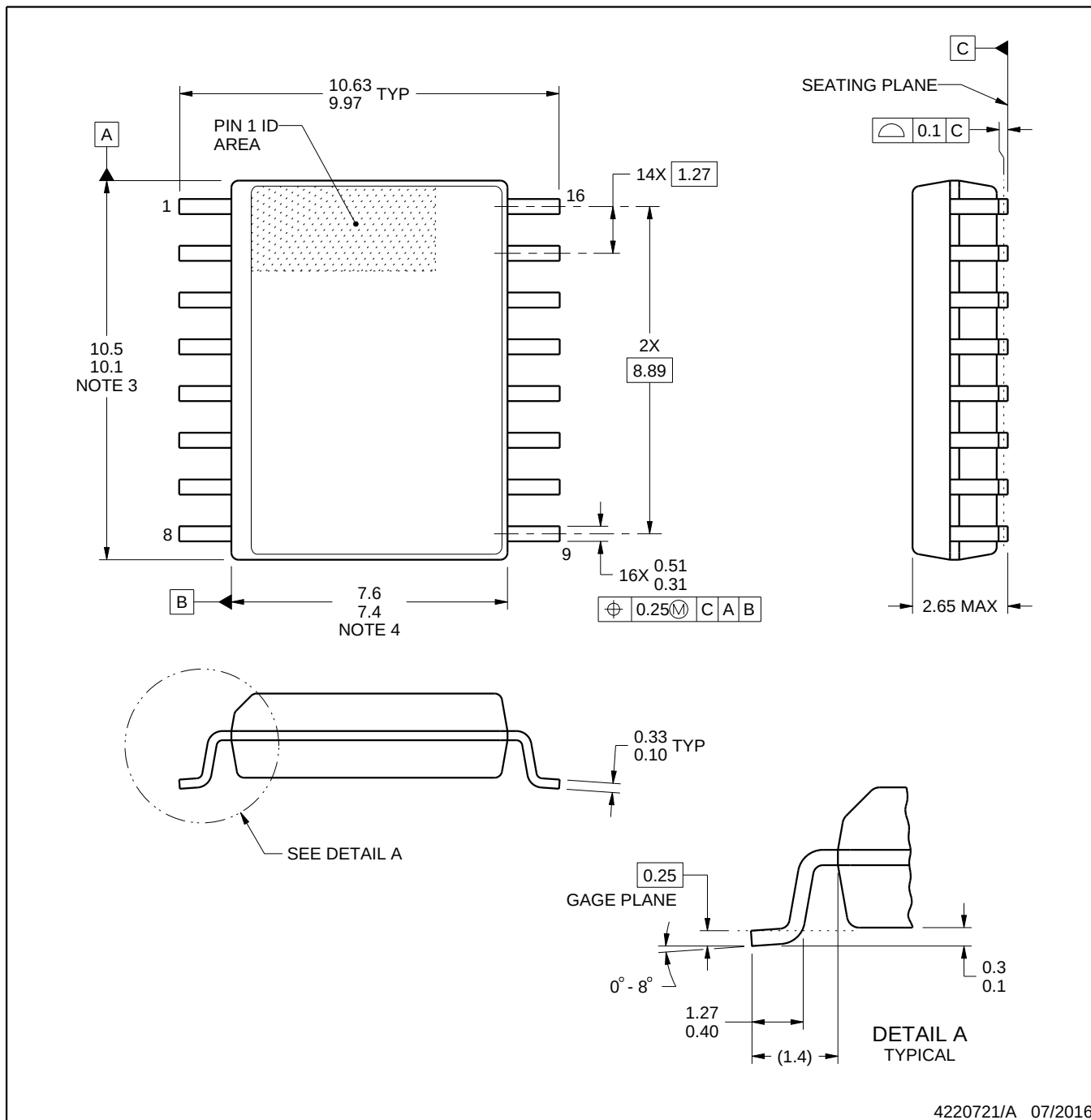


DW0016A

# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

### NOTES:

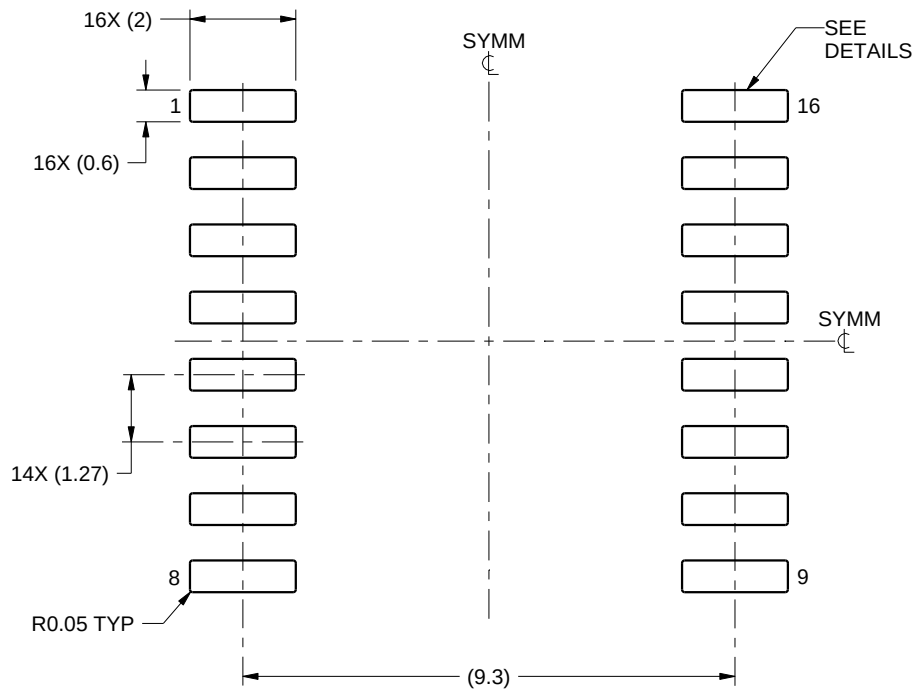
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

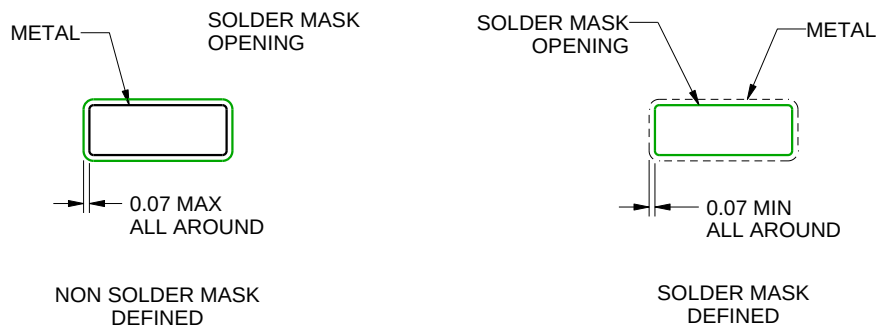
DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:7X



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

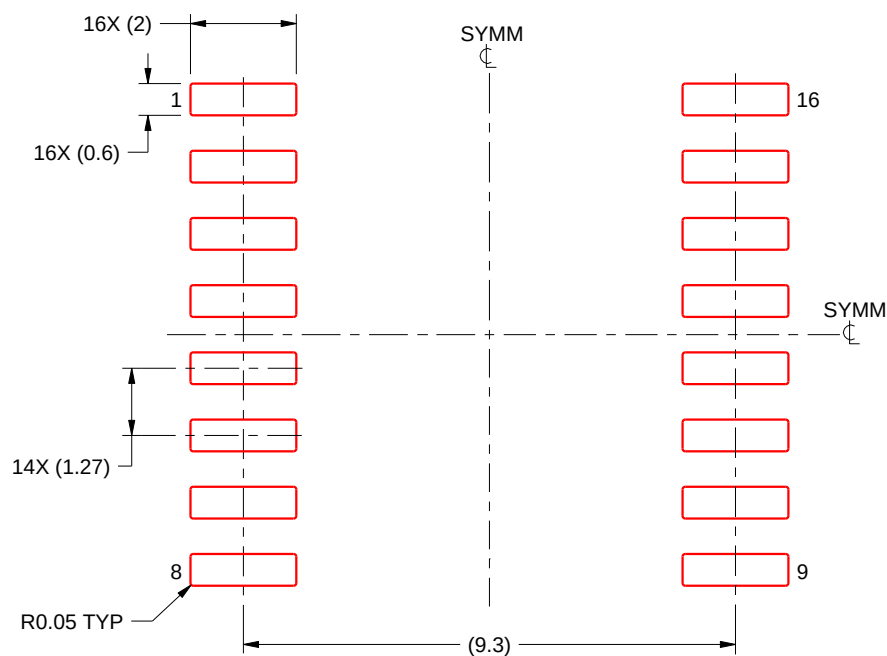


# EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025