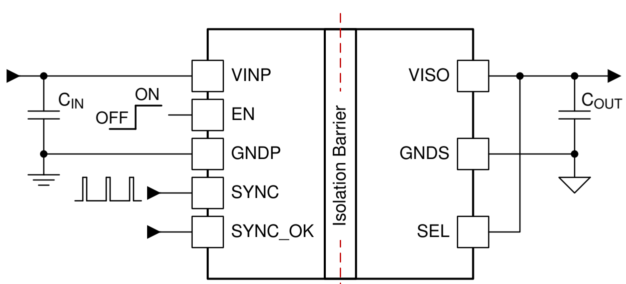
# UCC12040 High-Density, Low-EMI, 3-kV$_{RMS}$ Basic Isolation DC/DC Module

## 1 Features

- High-density DC/DC module with optimized integrated transformer technology
- Input voltage range: 4.5 V to 5.5 V
- Output voltages (selectable): 5.4 V, 5.0 V, 3.7 V, 3.3 V
- Output power: 500 mW
- Peak efficiency: 60%
- Line regulation (typical): 1%
- Load regulation (typical): 1.5%
- Meets CISPR32 Class B EMI limits without ferrite beads on a 2-layer PCB
- Spread spectrum modulation (SSM)
- Robust isolation barrier:
  - Isolation rating: 3 kV$_{RMS}$
  - Surge capability: 6.5 kV$_{PK}$
  - Working voltage: 850 V$_{RMS}$
  - CMTI (typical): ±100 V/ns
- Short circuit recovery
- Thermal shutdown
- 16-pin wide-body SOIC package with > 8-mm creepage and clearance
- Extended temperature range: –40°C to 125°C
- Safety-related certifications:
  - 5657-V$_{PK}$ basic isolation per DIN V VDE V 0884-11:2017- 01
  - 3000-V$_{RMS}$ isolation for 1 minute per UL 1577
  - UL certification per IEC 60950-1, IEC 62368- 1 and IEC 60601-1 end equipment standards
  - CQC approval per GB4943.1-2011




**Simplified Application**

## 2 Applications

- PLC analog input & output modules
- Grid protection relays & smart breakers
- Medical patient monitors
- Isolated bias for digital isolators
- Isolated bias for RS-485/RS-422/CAN transceivers
- Isolated bias for voltage and current sensors

## 3 Description

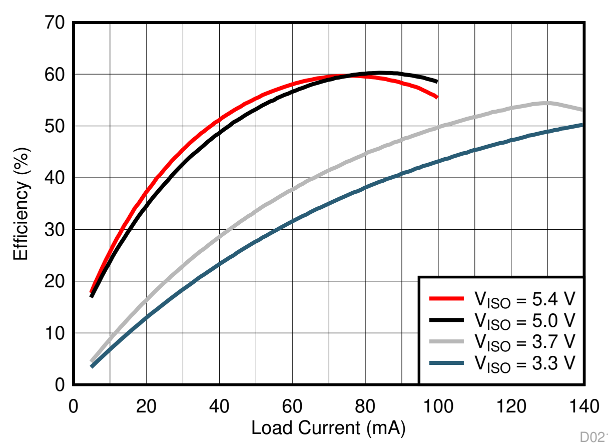
UCC12040 is a DC/DC power module with 3-kV$_{RMS}$ basic isolation rating designed to provide efficient, isolated power to isolated circuits that require a bias supply with a well-regulated output voltage. The device integrates a transformer and DC/DC controller with a proprietary architecture to provide 500 mW (typical) of isolated power with low EMI.

The UCC12040 integrates protection features for increased system robustness. The device also has an enable pin, synchronization capability, and regulated 5-V or 3.3-V output options with headroom. The UCC12040 is a low-profile, miniaturized solution offered in a wide-body SOIC package with 2.65-mm height.

**Device Information**(1)

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| UCC12040 | DVE SOIC (16) | 10.30 mm × 7.50 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.




V$_{INP}$ = 5.0 V T$_A$ = 25°C

**Typical Efficiency vs. Load**

## Table of Contents



## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision A (April 2020) to Revision B (May 2021)** — **Page**

- Added Safety Certification Information. .......... 1
- Updated ESD values. .......... 4
- Updated voltage isolation specs per DIN V VDE V 0884-11:2017-01 .......... 5
- Updated Switching Characteristics (non-sync) .......... 8

**Changes from Revision * (December 2019) to Revision A (April 2020)** — **Page**

- Updated $I_{VINO}$ Typical Values in *Electrical Characteristics* Table .......... 7

# 5 Pin Configuration and Functions

### DVE Package 16-Pin SOIC Top View

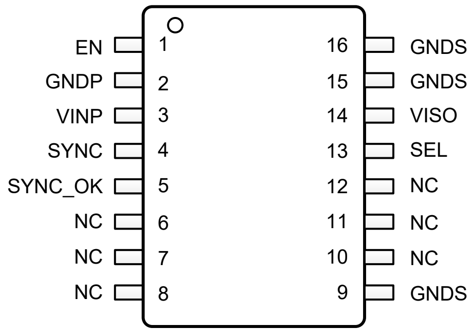



**Table 5-1. Pin Functions**

| PIN | | TYPE (1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| EN | 1 | I | Enable pin. Forcing EN low disables the device. Pull high to enable normal device functionality. |
| GNDP | 2 | P | Power ground return connection for VINP. |
| GNDS | 9 | P | Connect to GNDS plane on printed circuit board. Do not use as only ground connection for VISO. Ensure pin 15 is connected to circuit ground. |
| | 16 | | |
| GNDS | 15 | P | Secondary side ground return connection for VISO. Connect bypass capacitor from VISO to this pin. |
| NC | 6 | — | Pins internally connected together. No other electrical connection. Pins belong to primary-side voltage domain. Connect to GNDP on printed circuit board. |
| | 7 | | |
| | 8 | | |
| | 10 | — | No internal connection. Pin belongs to isolated voltage domain. Connect to GNDS on printed circuit board. |
| | 11 | | |
| | 12 | | |
| SYNC | 4 | I | Synchronous clock input pin. Provide a clock signal to synchronize multiple devices or connect to GNDP for standalone operation using the internal oscillator. If the SYNC pin is left open make sure to it separate it from any switching noise to avoid false clock coupling. |
| SYNC_OK | 5 | O | Active-low, open-drain diagnostic output. Pin is asserted LOW if there is no external SYNC clock or one that is outside of the operating range of the UCC12040 is detected. In this state, the external clock is ignored and the DC-DC converter is clocked by the internal oscillator. The pin is in high-impedance if a clock is applied on SYNC. |
| SEL | 13 | I | $V_{ISO}$ selection pin. $V_{ISO}$ setpoint is 5.0 V when SEL is shorted to $V_{ISO}$, 5.4 V when SEL is connected to $V_{ISO}$through a 100-kΩ resistor, 3.3 V when SEL is shorted to GNDS, and 3.7 V when SEL is connected to GNDS through a 100-kΩ resistor. For more information see the *Section 7.4* section. |
| VINP | 3 | P | Primary side input supply voltage pin. A 10-µF ceramic capacitor to GNDP on pin 2, placed close to the device pins, is required. |
| VISO | 14 | P | Isolated supply voltage pin. A 10-µF ceramic capacitor to GNDS on pin 15, placed close to the device pins, is required. See *Section 8.2.2.1* section. |

(1) P = Power, G = Ground, I = Input, O = Output

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

| | MIN | MAX | UNIT |
|---|---|---|---|
| VINP to GNDP | –0.3 | 6.0 | V |
| EN, SYNC, SYNC_OK, to GNDP | –0.3 | VINP + 0.3, ≤ 6.0 | V |
| VISO to GNDS | –0.3 | 6.0 | V |
| SEL to GNDS | –0.3 | VISO + 0.3, ≤ 6.0 | V |
| $V_{ISO}$ output power at $T_a$ = 25°C, $P_{OUT\_MAX}$ [(2)] | | 675 | mW |
| Operating junction temperature range, $T_J$ | –40 | 150 | °C |
| Storage temperature, $T_{stg}$ | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) See the Section 7.3.3 section for maximum rated values across temperature and $V_{INP}$ conditions for each different $V_{ISO}$ output mode.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)] | ±3000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)] | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{INP}$ | Primary side supply voltage | 4.5 | 5.0 | 5.5 | V |
| $V_{EN}$ | EN pin input voltage | 0 | | 5.5 | V |
| $V_{SYNC}$ | SYNC pin input voltage | 0 | | 5.5 | V |
| $V_{SYNC-OK}$ | SYNC_OK pen drain pin voltage | 0 | | 5.5 | V |
| $V_{ISO}$ | Isolated power supply voltage | 0 | | 5.7 | V |
| $V_{SEL}$ | Input voltage | 0 | | 5.7 | V |
| $f_{SYNC}$ | External DC/DC converter synchronization signal frequency | 14.4 | 16.0 | 17.6 | MHz |
| $P_{VISO}$ | $V_{ISO}$ output power at $T_a$ = 25°C [(1)] | | | 500 | mW |
| $T_a$ | Ambient temperature | –40 | | 125 | °C |
| $T_J$ | Junction temperature | –40 | | 150 | °C |

(1) See the Section 7.3.3 section for maximum rated values across temperature and $V_{INP}$ conditions for each different $V_{ISO}$ output mode.

## 6.4 Thermal Information

| THERMAL METRIC[(1)] | | DVE (SOIC) 16 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 63.8 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 21.4 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 38.5 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 10.2 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 37.2 | °C/W |

| THERMAL METRIC(1) | | DVE (SOIC) 16 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | — | °C/W |

(1) The value of $R_{\theta JA}$ given in this table is only valid for comparison with other packages and can not be used for design purposes. This value was calculated in accordance with JESD 51-7, and simulated on a 4-layer JEDEC board when $P_{DP}$ = 129 mW, $P_{DC}$ = 142 mW and $P_{DT}$ = 129 mW. The board temperature is taken from Pin 12. For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Power Ratings

$V_{INP}$ = 5.0V, $C_{INP}$ = $C_{OUT}$ = 10 uF, $T_J$ = 150°C, Internal Clock mode

| PARAMETER | | TEST CONDITIONS | VALUE | UNIT |
|---|---|---|---|---|
| $P_D$ | Power dissipation | SEL connected to GNDS (3.3-V $V_{ISO}$ output mode), $I_{ISO}$ = 135 mA | 460 | mW |
| $P_{DP}$ | Power dissipation by driver side (primary) | | 148 | mW |
| $P_{DS}$ | Power dissipation by rectifier side (secondary) | | 164 | mW |
| $P_{DT}$ | Power dissipation by transformer | | 148 | mW |

## 6.6 Insulation Specifications

| PARAMETER | | TEST CONDITIONS | VALUE | UNIT |
|---|---|---|---|---|
| **GENERAL** | | | | |
| CLR | External clearance(1) | Shortest terminal-to-terminal distance through air | > 8 | mm |
| CPG | External creepage(1) | Shortest terminal-to-terminal distance across the package surface | > 8 | mm |
| DTI | Distance through the insulation | Minimum internal gap (internal clearance) | > 120 | µm |
| CTI | Comparative tracking index | DIN EN 60112 (VDE 0303-11); IEC 60112 | > 600 | V |
| | Material group | According to IEC 60664-1 | I | |
| | Overvoltage Category | Rated mains voltage ≤ 300 $V_{RMS}$ | I-IV | |
| | | Rated mains voltage ≤ 600 $V_{RMS}$ | I-IV | |
| | | Rated mains voltage ≤ 1000 $V_{RMS}$ | I-III | |
| **DIN V VDE V 0884-11:2017-01**(2) | | | | |
| $V_{IORM}$ | Maximum repetitive peak isolation voltage | AC voltage (bipolar) | 1202 | $V_{PK}$ |
| $V_{IOWM}$ | Maximum working isolation voltage | AC voltage (sine wave) Time dependent dielectric breakdown (TDDB) test | 850 | $V_{RMS}$ |
| | | DC voltage | 1202 | $V_{DC}$ |
| $V_{IOTM}$ | Maximum transient isolation voltage | $V_{TEST}$ = $V_{IOTM}$, t = 60s (qualification);<br>$V_{TEST}$ = 1.2 × $V_{IOTM}$, t = 1s (100% production) | 4243 | $V_{PK}$ |
| $V_{IOSM}$ | Maximum surge isolation voltage(3) | Test method per IEC 62368-1, 1.2/50 µs waveform,<br>$V_{TEST}$ = 1.3 × $V_{IOSM}$ = 6500 $V_{PK}$ (qualification) | 5000 | $V_{PK}$ |
| $q_{pd}$ | Apparent charge(4) | Method a: After I/O safety test subgroup 2/3,<br>$V_{ini}$ = $V_{IOTM}$, $t_{ini}$ = 60 s;<br>$V_{pd(m)}$ = 1.2 × $V_{IORM}$ = 1442 $V_{PK}$, $t_m$ = 10 s | ≤ 5 | pC |
| | | Method a: After environmental tests subgroup 1,<br>$V_{ini}$ = $V_{IOTM}$, $t_{ini}$ = 60 s;<br>$V_{pd(m)}$ = 1.2 × $V_{IORM}$ = 1442 $V_{PK}$, $t_m$ = 10 s | ≤ 5 | |
| | | Method b1: At routine test (100% production) and preconditioning (type test)<br>$V_{ini}$ = 1.2 × $V_{IOTM}$, $t_{ini}$ = 1 s;<br>$V_{pd(m)}$ = 1.5 × $V_{IORM}$ = 1803 $V_{PK}$, $t_m$ = 1 s | ≤ 5 | |
| $C_{IO}$ | Barrier capacitance, input to output(5) | $V_{IO}$ = 0.4 sin (2πft), f = 1 MHz | ~3.5 | pF |
| $R_{IO}$ | Isolation resistance, input to output(5) | $V_{IO}$ = 500 V, $T_A$ = 25°C | > $10^{12}$ | Ω |
| | | $V_{IO}$ = 500 V, 100°C ≤ $T_A$ ≤ 125°C | > $10^{11}$ | |
| | | $V_{IO}$ = 500 V at $T_S$ = 150°C | > $10^9$ | |
| | Pollution degree | | 2 | |
| | Climatic category | | 40/125/21 | |
| **UL 1577** | | | | |

| PARAMETER | | TEST CONDITIONS | VALUE | UNIT |
|---|---|---|---|---|
| $V_{ISO}$ | Withstand isolation voltage | $V_{TEST}$ = $V_{ISO}$ = 3000 $V_{RMS}$, t = 60 s (qualification); $V_{TEST}$ = 1.2 × $V_{ISO}$ = 3600 $V_{RMS}$, t = 1 s (100% production) | 3000 | $V_{RMS}$ |

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the maximum operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-terminal device

## 6.7 Safety-Related Certifications

| VDE | UL | | | CQC |
|---|---|---|---|---|
| Certified according to DIN V VDE V 0884-11:2017- 01 | Certified according to IEC 60601-1 | Certified according to IEC 60950-1 and IEC 62368- 1 | Recognized under UL 1577 Component Recognition Program | Certified according to GB4943.1-2011 |
| Basic insulation Maximum transient isolation voltage, 4243 VPK; Maximum repetitive peak isolation voltage, 1202 VPK; Maximum surge isolation voltage, 5000 VPK | Basic insulation per UL 60601- 1:14 and IEC 60601-1 Ed.3+A1,AAMI ES 60601-1:2005/(R)2012 and A1:2012, C1:2009/(R)2012 and A2:2010/(R)2012 CSA C22.2 No. 60601-1:2014 IEC 60601-1:2012, 1 MOPP (Means of Patient Protection), 250 VRMS maximum working voltage | Basic insulation per UL 60950-1-07+A1+A2, IEC 60950-1 2nd Ed.+A1+A2, UL 62368-1- 14 and IEC 62368-1 2nd Ed., 850 VRMS maximum working voltage (pollution degree 1, material group I) | Single protection, 3000 VRMS | Basic insulation, Altitude ≤ 5000 m, Tropical Climate, 800 VRMS maximum working voltage |
| Certificate number: 40047657 | Certificate number: US-36773-A1-UL | Certificate number: US-36706-UL, US-36707-UL | File number: E181974 | Certificate number: CQC20001268791 |

## 6.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

| PARAMETER | | TEST CONDITIONS | MAX | UNIT |
|---|---|---|---|---|
| $I_S$ | Safety input current (1) | $R_{\theta JA}$ = 63.8°C/W, $V_I$ = 5.5 V, $T_J$ = 150°C, $T_A$ = 25°C | 356 | mA |
| | | $R_{\theta JA}$ = 63.8°C/W, $V_I$ = 4.5 V, $T_J$ = 150°C, $T_A$ = 25°C | 435 | |
| $P_S$ | Safety input power | $R_{\theta JA}$ = 63.8°C/W, $T_J$ = 150°C, $T_A$ = 25°C | 1960 | mW |
| $T_S$ | Safety temperature (1) | | 150 | °C |

(1) The maximum safety temperature, $T_S$, has the same value as the maximum junction temperature, $T_J$, specified for the device. The $I_S$ and $P_S$ parameters represent the safety current and safety power respectively. The maximum limits of $I_S$ and $P_S$ should not be exceeded. These limits vary with the ambient temperature, $T_A$. The junction-to-air thermal resistance, $R_{\theta JA}$, in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter: $T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device. $T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature. $P_S = I_S \times V_I$, where $V_I$ is the maximum input voltage.

## 6.9 Electrical Characteristics

Over operating temperature range ($T_J$ = –40°C to 150°C), $V_{INP}$ = 4.5V to 5.5V, $C_{INP}$ = $C_{OUT}$ = 10 µF, SEL connected to $V_{ISO}$, internal clock mode, unless otherwise noted. All typical values at $T_J$ = 25°C and $V_{INP}$ = 5.0V.

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **INPUT SUPPLY** | | | | | | |
| $I_{VINQ}$ | VINP quiescent current,disabled | EN=LOW | | | 100 | uA |
| $I_{VINO}$ | VINP operating current, no load | EN=HI; SEL shorted to VISO (5.0V output) | | 50 | | mA |
| | | EN=HI; SEL 100kΩ to VISO (5.4V output) | | 45 | | mA |
| | | EN=HI; SEL shorted to GNDS (3.3V output) | | 90 | | mA |
| | | EN=HI; SEL 100kΩ to GNDS (3.7V output) | | 80 | | mA |
| $I_{VIN\_SC}$ | DC current from VINP supplyunder short circuit on VISO | VISO short to GNDS | | 245 | | mA |
| $V_{UVPR}$ | VINP under-voltage lockout rising threshold | | | 4.2 | | V |
| $V_{UVPF}$ | VINP under-voltage lockout falling threshold | | | 3.7 | | V |
| $V_{UVPH}$ | VINP under-voltage lockout hysteresis | | | 0.5 | | V |
| **EN, SYNC INPUT PINS** | | | | | | |
| $V_{IR}$ | Input voltage threshold, logic HIGH | Rising edge | | | 2.2 | V |
| $V_{IF}$ | Input voltage threshold, logic LOW | Falling edge | 0.8 | | | V |
| $I_{EN}$ | Enable Pin Input Current | $V_{EN}$ = 5.0 V | | 5 | 10 | uA |
| $I_{SYNC}$ | SYNC Pin Input Current | $V_{SYNC}$ = 5.0 V | | 0.02 | 1 | uA |
| **SYNC_OK PIN** | | | | | | |
| $V_{OL}$ | SYNC_OK output low voltage | $I_{SYNC\_OK}$ = - 2 mA | | 0.15 | | V |
| $I_{LKG\_SYNC\_OK}$ | SYNC_OK pin leakage current | $V_{SYNC\_OK}$ = 5.0 V | | | 1 | uA |
| **DC/DC CONVERTER** | | | | | | |
| $V_{ISO}$ | Isolated supply output voltage | SEL shorted to VISO (5.0V output); $I_{ISO}$ = 55 mA [(2)] | 4.7 | 5 | 5.3 | V |
| | | SEL 100kΩ to VISO (5.4 V output); $I_{ISO}$ = 45 mA [(2)] | 5.1 | 5.4 | 5.7 | V |
| | | SEL shorted to GNDS (3.3V output); $I_{ISO}$ = 100 mA [(2)] | 3.1 | 3.3 | 3.5 | V |
| | | SEL 100kΩ to GNDS (3.7 V output); $I_{ISO}$ = 90 mA [(2)] | 3.5 | 3.7 | 3.9 | V |
| $V_{ISO(RIP)}$ | Voltage ripple on isolated supply output (pk-pk) | 20-MHz bandwidth, CLOAD = 10 uF \|\| 0.1 uF, SEL shorted to VISO (5.0V output); $I_{ISO}$ = 100 mA | | 50 | | mV |
| | | 20-MHz bandwidth, CLOAD = 10 uF \|\| 0.1 uF, SEL 100kΩ to VISO (5.4V output); $I_{ISO}$ = 90 mA | | 50 | | mV |
| | | 20-MHz bandwidth, CLOAD = 10 uF \|\| 0.1 uF, SEL shorted to GNDS (3.3V output); $I_{ISO}$ = 145 mA | | 50 | | mV |
| | | 20-MHz bandwidth, CLOAD = 10 uF \|\| 0.1 uF, SEL shorted to GNDS (3.7V output); $I_{ISO}$ = 130 mA | | 50 | | mV |
| $V_{ISO(LINE)}$ | $V_{ISO}$ DC line regulation | SEL shorted to VISO (5.0 V output); $I_{ISO}$ = 50 mA, VINP = 4.5 V to 5.5 V | | 1% | | |
| | | SEL shorted to GNDS (3.3 V output); $I_{ISO}$ = 75 mA, VINP = 4.5 V to 5.5 V | | 1% | | |

Over operating temperature range ($T_J$ = –40°C to 150°C), $V_{INP}$ = 4.5V to 5.5V, $C_{INP}$ = $C_{OUT}$ = 10 µF, SEL connected to $V_{ISO}$, internal clock mode, unless otherwise noted. All typical values at $T_J$ = 25°C and $V_{INP}$ = 5.0V.

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{ISO(LOAD)}$ | $V_{ISO}$ DC load regulation | SEL shorted to VISO (5.0 V output); $I_{ISO}$ = 0 to 100 mA | | 1.5% | | |
| | $V_{ISO}$ DC load regulation | SEL shorted to GNDS (3.3 V output); $I_{ISO}$ = 0 to 145 mA | | 1.5% | | |
| EFF | Efficiency at maximum recommended load (1) | SEL shorted to VISO (5.0 V output); $I_{ISO}$ = 100 mA | | 60% | | |
| | | SEL 100kΩ to VISO (5.4V output); $I_{ISO}$ = 90 mA | | 60% | | |
| | | SEL shorted to GNDS (3.3V output); $I_{ISO}$ = 145 mA | | 50% | | |
| | | SEL 100kΩ to GNDS (3.7V output); $I_{ISO}$ = 130 mA | | 53% | | |
| $t_{RISE}$ | VISO rise time, 10% - 90% | EN = change from LO to HI, SEL shorted to VISO (5.0V output); $I_{ISO}$ = 1 mA | | 750 | | µs |
| | | EN = change from LO to HI, SEL 100kΩ to GNDS (3.3V output); $I_{ISO}$ = 1 mA | | 300 | | µs |
| **THERMAL SHUTDOWN** | | | | | | |
| $TSD_{THR}$ | Thermal shutdown threshold | Junction Temperature, Rising | | 165 | | °C |
| $TSD_{HYST}$ | Thermal shutdown hysteresis | Junction Temperature, Falling | | 27 | | °C |

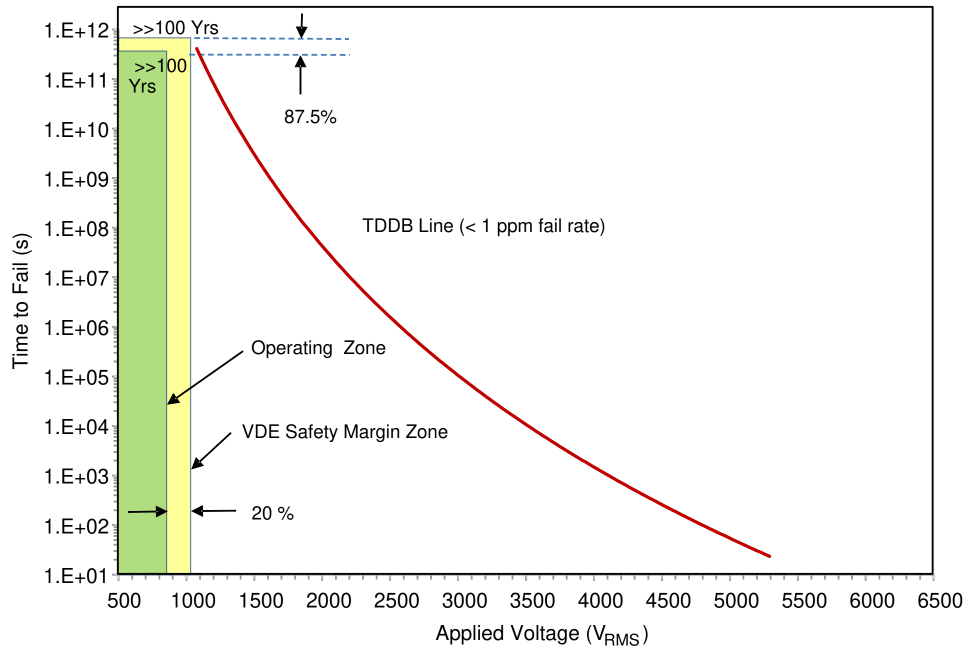
(1) Efficiency calculation: EFF = ($V_{ISO}$ x $I_{ISO}$) / ($V_{INP}$ x $I_{INP}$)
(2) See the Section 7.3.3 section for discussion of $V_{ISO}$ regulation across load and temperature conditions for all output voltage settings.

## 6.10 Switching Characteristics

Over operating temperature range ($T_J$ = –40°C to 150°C), $V_{INP}$ = 4.5V to 5.5V, $C_{INP}$ = $C_{OUT}$ = 10 µF, SEL connected to $V_{ISO}$, internal clock mode, unless otherwise noted. All typical values at $T_J$ = 25°C and $V_{INP}$ = 5.0V.

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{SW\_INT}$ | DC/DC Converter Clock | Internal clock mode | 7.2 | 8 | 8.8 | MHz |
| CMTI | Static common-mode transient immunity | Slew Rate of GNDP versus GNDS, $V_{CM}$ = 1000 V | | 100 | | V/ns |

## 6.11 Insulation Characteristics Curves




Working isolation voltage = 850 $V_{RMS}$

Projected insulation lifetime = 11840 years

$T_A$ up to 150°C

Applied voltage frequency = 60 Hz

**Figure 6-1. Insulation Lifetime Projection Data**

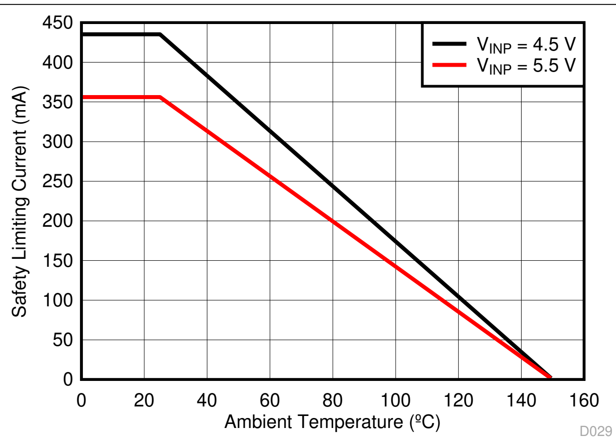



**Figure 6-2. Thermal Derating Curve for Safety Limiting Current per VDE**

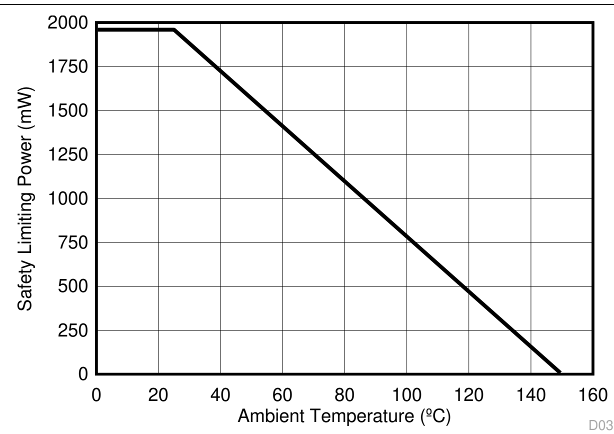
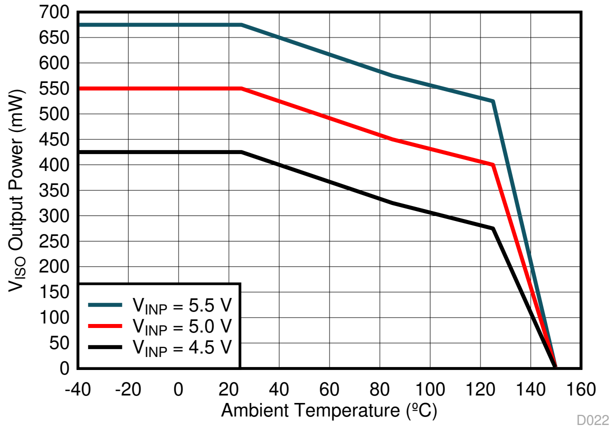


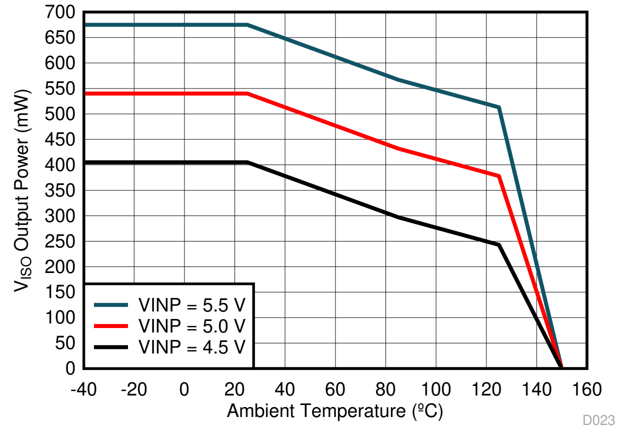

**Figure 6-3. Thermal Derating Curve for Safety Limiting Power per VDE**

## 6.12 Typical Characteristics



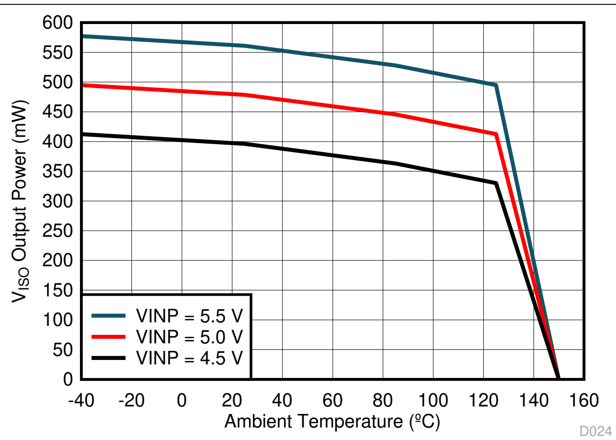

$V_{ISO}$ = 5.0 V

**Figure 6-4. Maximum $V_{ISO}$ Output Power vs. Temperature**



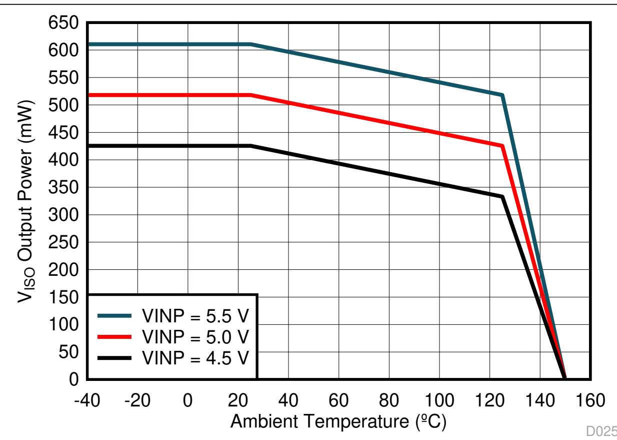

$V_{ISO}$ = 5.4 V

**Figure 6-5. Maximum $V_{ISO}$ Output Power vs. Temperature**



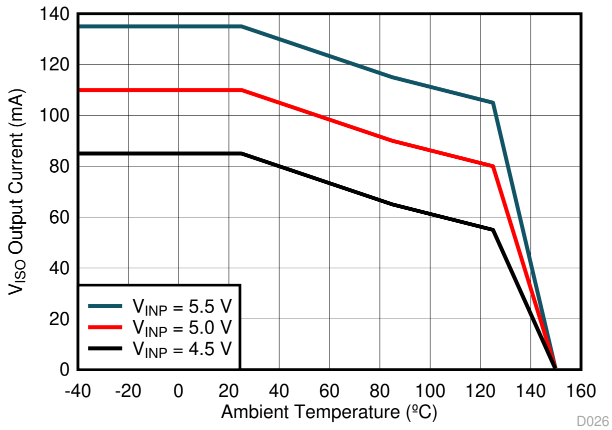

$V_{ISO}$ = 3.3 V

**Figure 6-6. Maximum $V_{ISO}$ Output Power vs. Temperature**



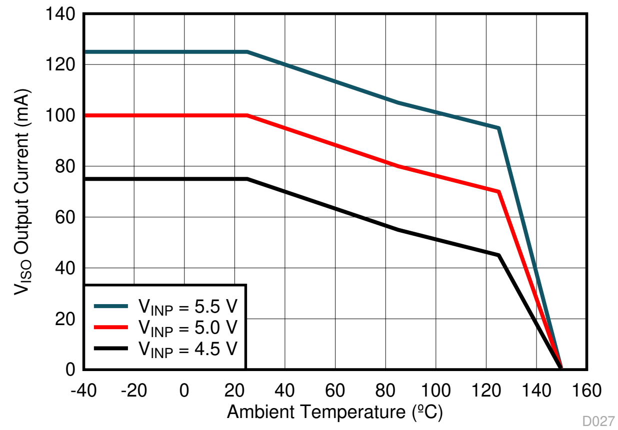

$V_{ISO}$ = 3.7 V

**Figure 6-7. Maximum $V_{ISO}$ Output Power vs. Temperature**



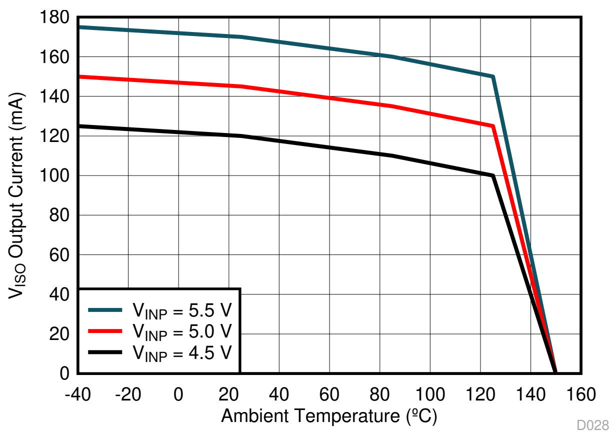

$V_{ISO}$ = 5.0 V

**Figure 6-8. Maximum $V_{ISO}$ Output Current vs. Temperature**



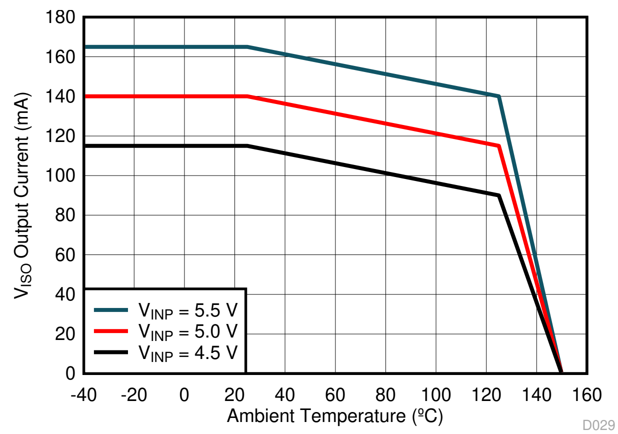

$V_{ISO}$ = 5.4 V

**Figure 6-9. Maximum $V_{ISO}$ Output Current vs. Temperature**



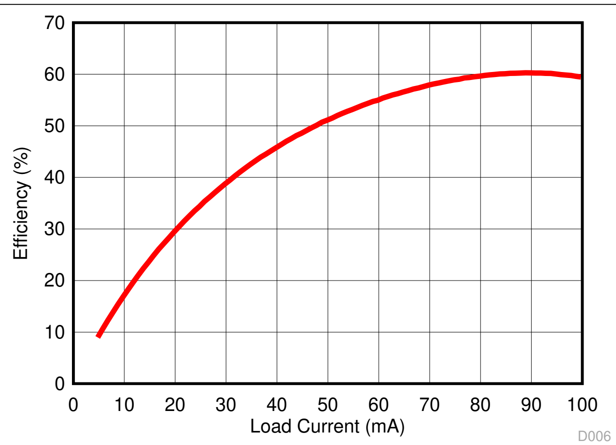

$V_{ISO}$ = 3.3 V

**Figure 6-10. Maximum $V_{ISO}$ Output Current vs. Temperature**



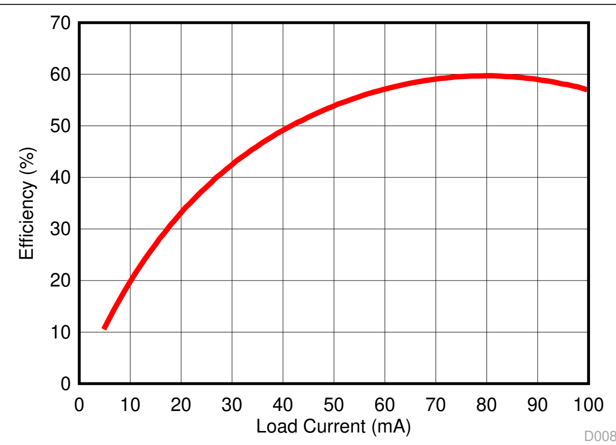

$V_{ISO}$ = 3.7 V

**Figure 6-11. Maximum $V_{ISO}$ Output Current vs. Temperature**



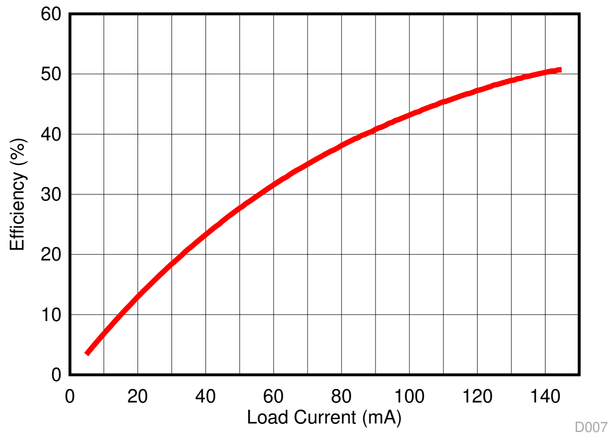

$V_{INP}$ = 5.0 V $V_{ISO}$ = 5.0 V $T_A$ = 25°C

**Figure 6-12. Power Supply Efficiency vs Load Current ($I_{ISO}$)**



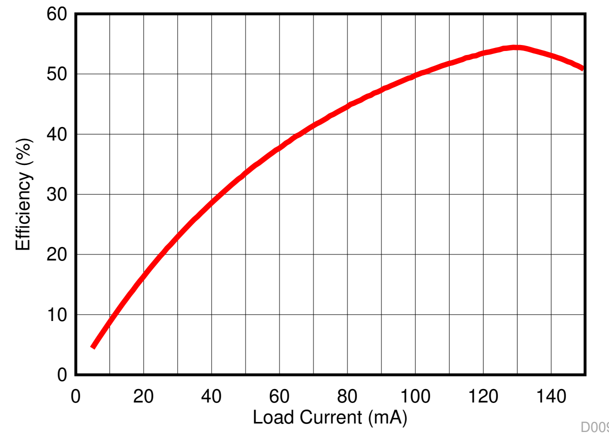

$V_{INP}$ = 5.0 V $V_{ISO}$ = 5.4 V $T_A$ = 25°C

**Figure 6-13. Power Supply Efficiency vs Load Current ($I_{ISO}$)**



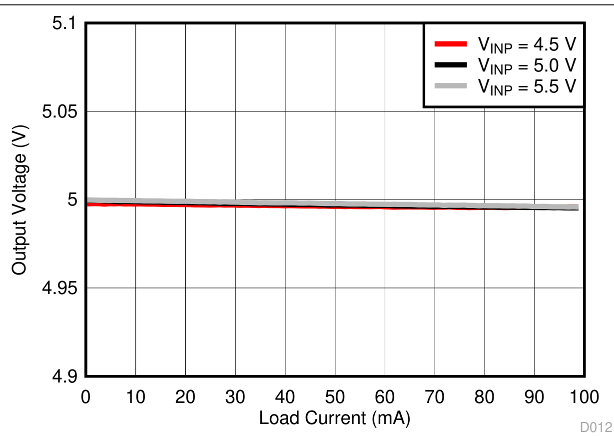

$V_{INP}$ = 5.0 V $V_{ISO}$ = 3.3 V $T_A$ = 25°C

**Figure 6-14. Power Supply Efficiency vs Load Current ($I_{ISO}$)**



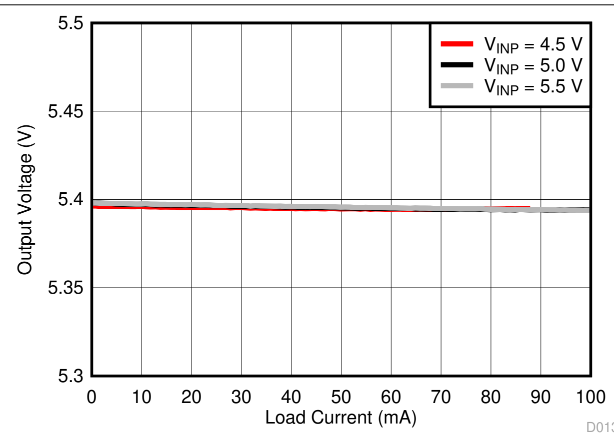

$V_{INP}$ = 5.0 V $V_{ISO}$ = 3.7 V $T_A$ = 25°C

**Figure 6-15. Power Supply Efficiency vs Load Current ($I_{ISO}$)**



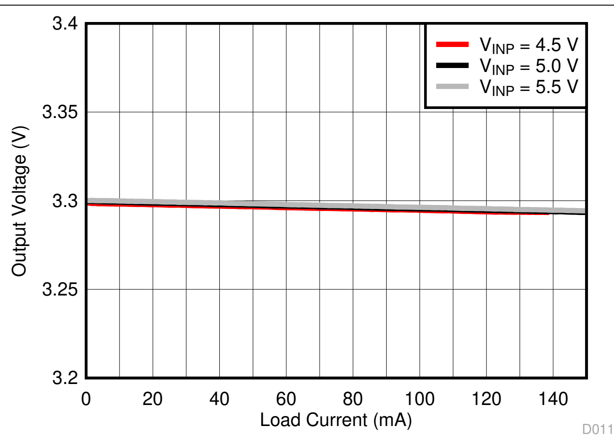

$V_{ISO}$ = 5.0 V $T_A$ = 25°C

**Figure 6-16. Isolated Supply Voltage ($V_{ISO}$) vs Load Current ($I_{ISO}$)**



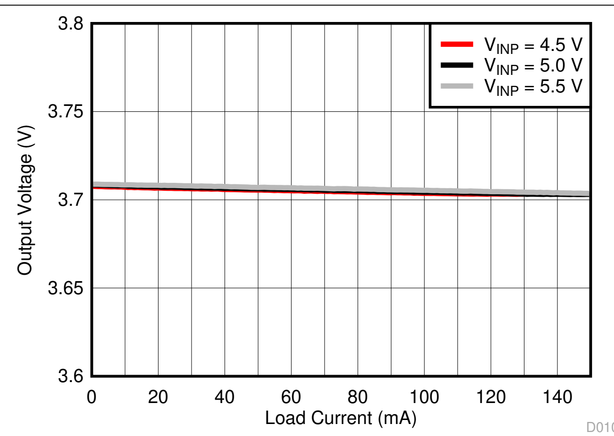

$V_{ISO}$ = 5.4 V $T_A$ = 25°C

**Figure 6-17. Isolated Supply Voltage ($V_{ISO}$) vs Load Current ($I_{ISO}$)**



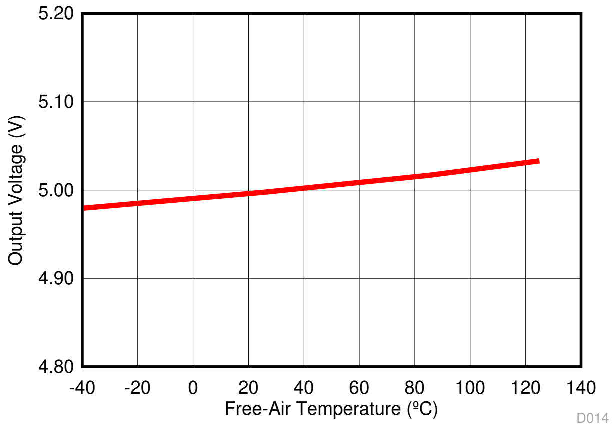

$V_{ISO}$ = 3.3 V $T_A$ = 25°C

**Figure 6-18. Isolated Supply Voltage ($V_{ISO}$) vs Load Current ($I_{ISO}$)**



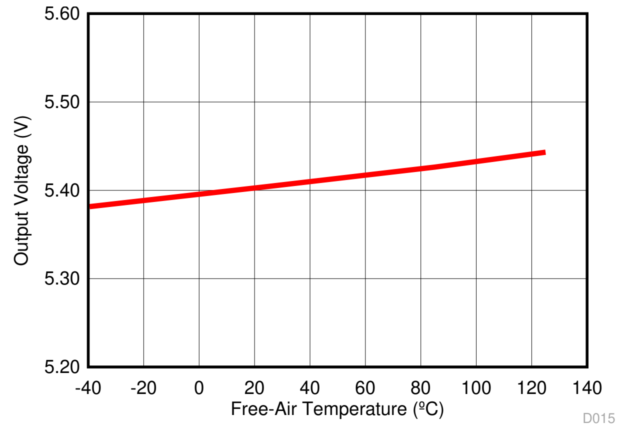

$V_{ISO}$ = 3.7 V $T_A$ = 25°C

**Figure 6-19. Isolated Supply Voltage ($V_{ISO}$) vs Load Current ($I_{ISO}$)**



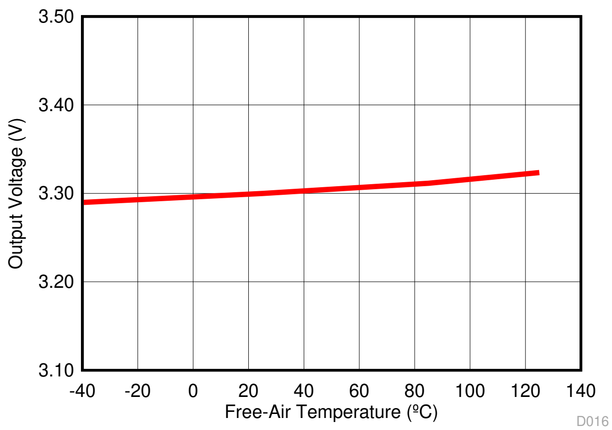

$V_{INP}$ = 5.0 V $V_{ISO}$ = 5.0 V $I_{ISO}$ = 50 mA

**Figure 6-20. Isolated Supply Voltage ($V_{ISO}$) vs Free-Air Temperature**



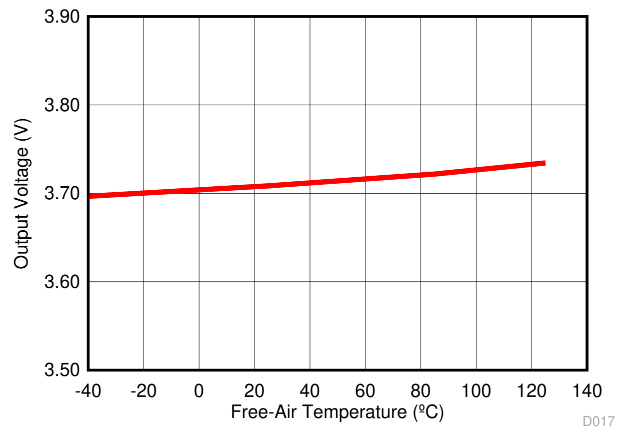

$V_{INP}$ = 5.0 V $V_{ISO}$ = 5.4 V $I_{ISO}$ = 50 mA

**Figure 6-21. Isolated Supply Voltage ($V_{ISO}$) vs Free-Air Temperature**



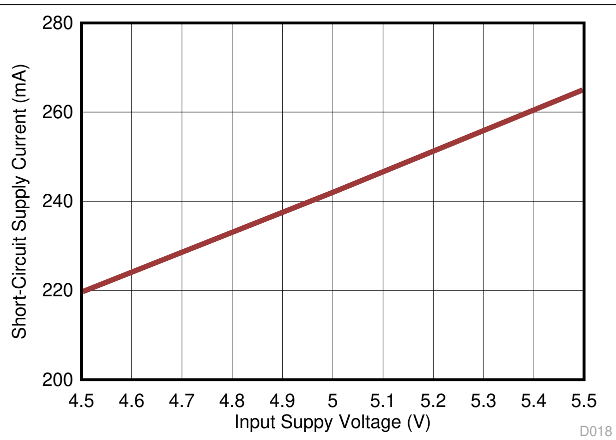

$V_{INP}$ = 5.0 V $V_{ISO}$ = 3.3 V $I_{ISO}$ = 75 mA

**Figure 6-22. Isolated Supply Voltage ($V_{ISO}$) vs Free-Air Temperature**



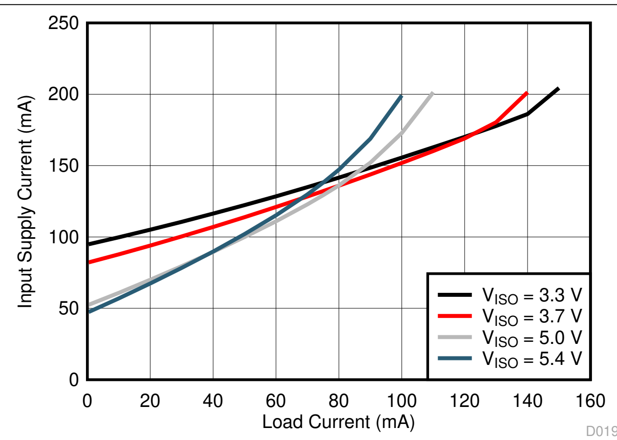

$V_{INP}$ = 5.0 V $V_{ISO}$ = 3.7 V $I_{ISO}$ = 75 mA

**Figure 6-23. Isolated Supply Voltage ($V_{ISO}$) vs Free-Air Temperature**




$T_A$ = 25°C

**Figure 6-24. Short-Circuit Supply Current ($I_{VIN\_SC}$) vs Supply Voltage ($V_{INP}$)**




$V_{INP}$ = 5.0 V $T_A$ = 25°C

**Figure 6-25. Input Supply Current ($I_{VINP}$) vs Load Current ($I_{ISO}$)**

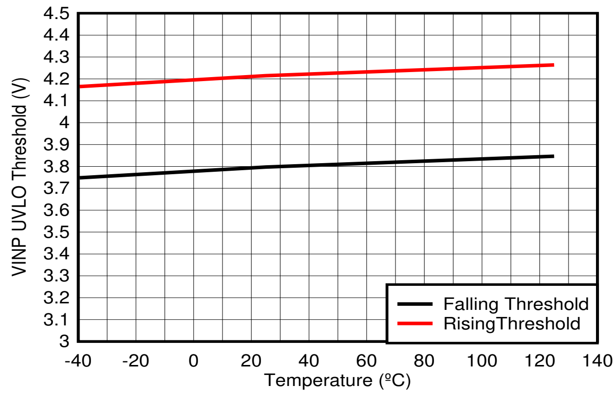



**Figure 6-26. Typical $V_{INP}$ UVLO Threshold vs Junction Temperature ($T_J$)**

# 7 Detailed Description

## 7.1 Overview

The UCC12040 device integrates a high-efficiency, low-emissions isolated DC/DC converter. This approach provides typically 500 mW of clean, steady power across a 3000$V_{RMS}$ basic isolation barrier.

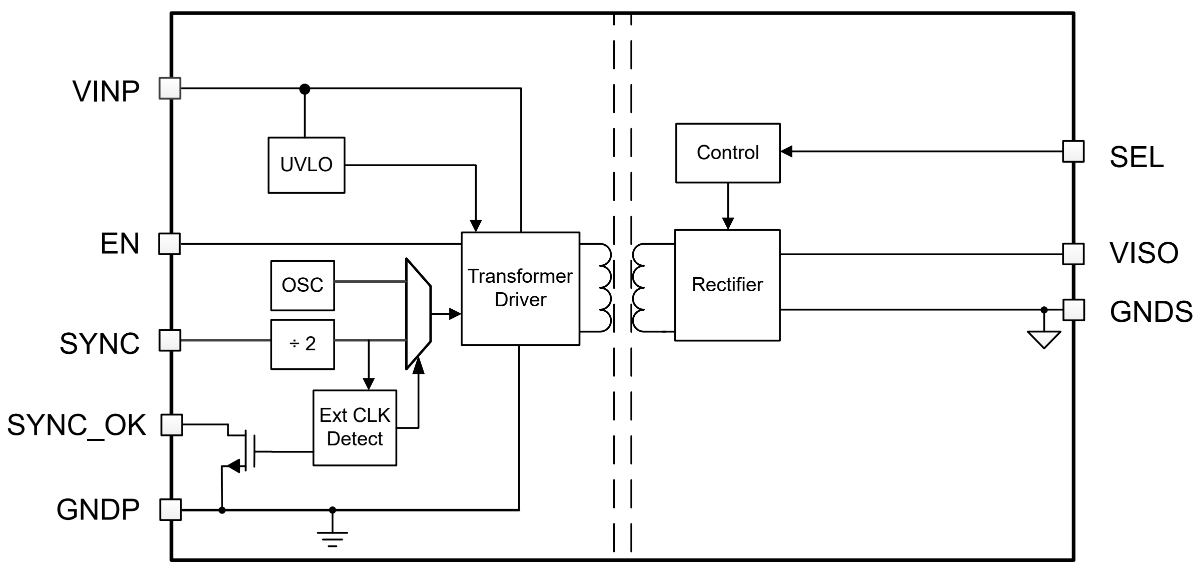
The integrated DC/DC converter uses switched mode operation and proprietary circuit techniques to reduce power losses and boost efficiency. Specialized control mechanisms, clocking schemes, and the use of an on-chip transformer provide high efficiency and low radiated emissions.

The VINP supply is provided to the primary power controller that switches the power stage connected to the integrated transformer. Power is transferred to the secondary side, rectified, and regulated to a level set by the SEL pin condition.

A fast feedback control loop monitors VISO and the output load, and ensures low overshoots and undershoots during load transients. Undervoltage lockout (UVLO) with hysteresis is integrated on the VINP supply, which ensures robust system performance under noisy conditions.

UCC12040 is suitable for applications that have limited board space and require more integration. These devices are also suitable for very-high voltage applications, where power transformers meeting the required isolation specifications are bulky and expensive.

## 7.2 Functional Block Diagram




## 7.3 Feature Description

### 7.3.1 Enable and Disable

Forcing EN low disables the device, which greatly reduces the VINP power consumption. Pull the EN pin high to enable normal device functionality. The EN pin has a weak internal pull-down resistor, so the device floats to the disable state if the pin is left open.

### 7.3.2 UVLO, Power-Up, and Power-Down Behavior

The UCC12040 has an undervoltage lockout (UVLO) on the VINP power supply. Upon power-up, while the VINP voltage is below the threshold voltage $V_{UVPR}$, the primary side transformer driver is disabled, and VISO output is off. The output powers up once the threshold is met. Likewise, if VINP falls below $V_{UVPF}$, the converter is disabled and there is no output at VISO. Both UVLO threshold voltages have hysteresis to avoid chattering.

### 7.3.3 $V_{ISO}$ Load Recommended Operating Area

Figure 7-1 depicts the device $V_{ISO}$ regulation behavior across the output load range, including when the output is overloaded. For proper device operation, ensure that the device VISO output load does not exceed the maximum output current ($I_{OUT\_MAX}$). The value for $I_{OUT\_MAX}$ over different temperature and $V_{INP}$ conditions are shown from Figure 6-8 to Figure 6-11. The following protection mechanisms will be engaged if the UCC12040 is loaded beyond the recommended operating area:

1. The device limits the maximum output power. If a load exceeding $I_{OUT\_MAX}$ is applied, $V_{ISO}$ drops accordingly to meet the maximum power limit.
2. If $V_{ISO}$ drops below nominal 3.8 V while operating in the constant power limit region, the over-power fold-back feature will switch the power converter from active rectification to passive rectification, and the built-in recovery hysteresis will ensure the UCC12040 recovers at a lower output power. The device returns to active rectification when load drops and $V_{ISO}$ increases above nominal 4.3V.
3. The device triggers a soft-start reset if $V_{ISO}$ drops below the nominal 1.8-V threshold. This reset is designed to protect the device during $V_{ISO}$ short-circuit conditions.
4. Thermal shutdown protection disables the converter if the device is operated in any of the above regions long enough to raise the silicon junction temperature above the thermal shutdown threshold. See the Section 7.3.4 section for more details on this device feature.

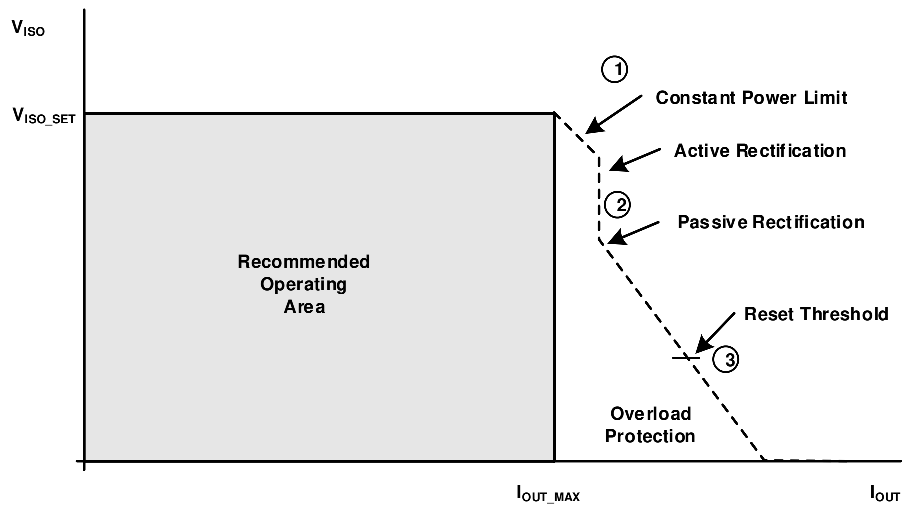



**Figure 7-1. $V_{ISO}$ Load Recommended Operating Area Description**

### 7.3.4 Thermal Shutdown

Thermal protection is also integrated to help prevent the device from getting damaged during overload and short-circuit conditions on the isolated output. Under these conditions, the device temperature starts to increase. When the silicon junction temperature $T_j$ sensed at the primary side die goes above the threshold $TSD_{THR}$(typical 165°C), thermal shutdown activates and the primary controller turns off which removes the energy supplied to the $V_{ISO}$ load, which causes the device to cool off. When the junction temperature drops approximately 27°C ($TSD_{HYST}$) from the shutdown point, the device starts to function normally. If an overload or output short-circuit condition prevails, this protection cycle is repeated. Make sure the design prevents the device junction temperatures from reaching such high values.

### 7.3.5 External Clocking and Synchronization

The UCC12040 has an internal oscillator trimmed to drive the transformer at 8.0 MHz. An external clock may be applied at the SYNC pin to override the internal oscillator. This external clock will be divided by 2, so the target range for the external clock signal at SYNC is 16 MHz ±10%. When a valid external clock signal is detected, the internal spread spectrum modulation (SSM) algorithm is disabled. This allows an external clock signal with a unique SSM to be applied. The depth and frequency of SSM is a tradeoff verses low frequency modulated VISO voltage ripple. The SYNC_OK pin is asserted LOW if there is no external SYNC clock or one that is outside of the operating range of the device is detected. In this state, the external clock is ignored and the DC/DC converter is clocked by the internal oscillator. The pin is in high impedance if a valid clock is applied on SYNC.

#### 7.3.6 $V_{ISO}$ Output Voltage Selection

The SEL pin is monitored during power-up — within the first 1 ms after applying VINP above the UVLO rising threshold or enabling via the EN pin — to detect the desired regulation voltage for the VISO output. Note that after this initial monitoring, the SEL pin no longer affects the VISO output level. In order to change the output mode selection, either the EN pin must be toggled or the VINP power supply must be cycled off and back on. Section6.4 provides more details on the SEL pin functionality.

#### 7.3.7 Electromagnetic Compatibility (EMC) Considerations

UCC12040 devices use spread spectrum modulation algorithm for the internal oscillator and advanced internal layout scheme to minimize radiated emissions at the system level.

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 32. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the device incorporates many chip-level design improvements for overall system robustness.

## 7.4 Device Functional Modes

Table 7-1 lists the supply functional modes for this device.

**Table 7-1. Device Functional Modes**

| INPUTS | | Isolated Supply Output Voltage ($V_{ISO}$) Setpoint |
|---|---|---|
| **EN** | **SEL** | |
| HIGH | Shorted to VISO | 5.0 V |
| HIGH | 100 kΩ to VISO | 5.4 V |
| HIGH | Shorted to GNDS | 3.3 V |
| HIGH | 100 kΩ to GNDS | 3.7 V |
| HIGH | OPEN(1) | UNSUPPORTED |
| LOW | X | 0 V |

(1) The SEL pin has an internal weak pull-down resistance to ground, but leaving this pin open is not recommended.

# 8 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 8.1 Application Information

The UCC12040 device is suitable for applications that have limited board space and desire more integration. This device is also suitable for very high voltage applications, where power transformers meeting the required isolation specifications are bulky and expensive.

## 8.2 Typical Application

Figure 8-1 shows the typical application schematic for the UCC12040 device supplying an isolated load.

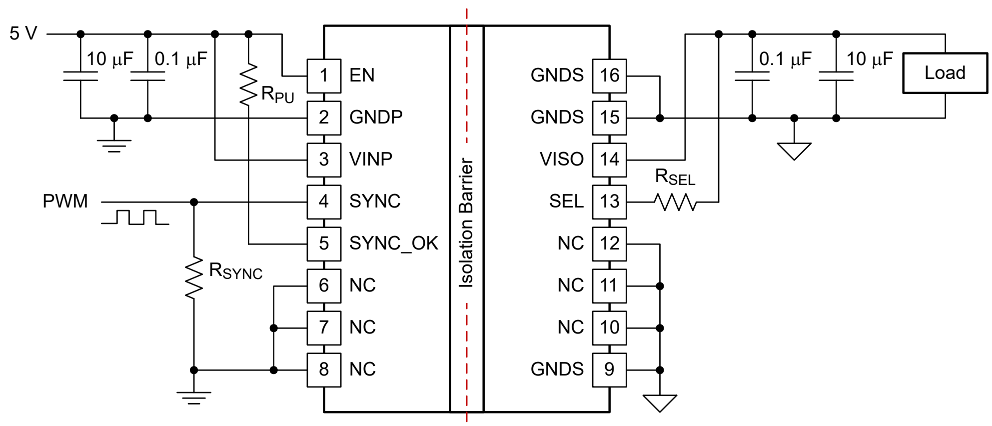



**Figure 8-1. Typical Application**

### 8.2.1 Design Requirements

To design using UCC12040, a few simple design considerations must be evaluated. Table 8-1 shows some recommended values for a typical application. See Section 9 and Section 10 sections to review other key design considerations for the UCC12040.

**Table 8-1. Design Parameters**

| PARAMETER | RECOMMENDED VALUE |
|---|---|
| Input supply voltage, $V_{INP}$ | 4.5 V to 5.5 V |
| Decoupling capacitance between $V_{INP}$ and GNDP | 10 µF, 16 V, ± 10%, X7R |
| Decoupling capacitance between $V_{ISO}$ and GNDS (1) | 10 µF, 16 V, ± 10%, X7R |
| Optional additional capacitance on VISO or VINP to reduce high-frequency ripple | 0.1 µF, 50 V,± 10%, X7R |
| Pull-up resistor from SYNC_OK to $V_{INP}$, $R_{PU}$ | 100 kΩ |
| Pull-up resistor from SEL to $V_{ISO}$ for 5.0V output voltage mode, $R_{SEL}$ | 0 Ω |
| Pull-up resistor from SEL to $V_{ISO}$ for 5.4V output voltage mode, $R_{SEL}$ | 100 kΩ |
| Optional SYNC signal impedance-matching resistor, $R_{SYNC}$ | Match source — typical values are 50 Ω, 75 Ω, 100 Ω, or 1 kΩ |
| External clock signal applied on SYNC | 16 MHz |

(1) See Section 8.2.2.1 section.

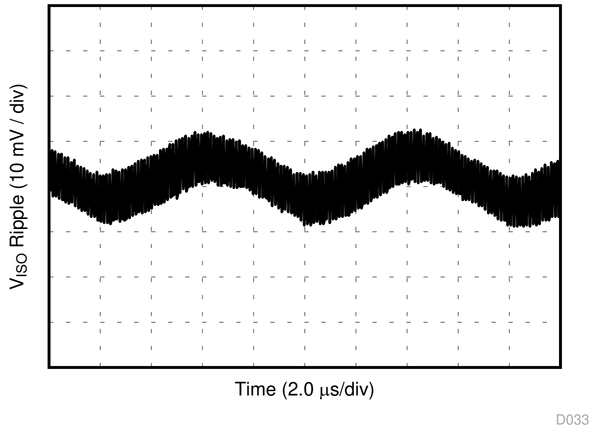
### 8.2.2 Detailed Design Procedure

Place ceramic decoupling capacitors as close as possible to the device pins. For the input supply, place the capacitor(s) between pin 3 (VINP) and pin 2 (GNDP). For the isolated output supply, place the capacitor(s) between pin 14 (VISO) and pin 15 (GNDS). This location is of particular importance to the input decoupling capacitor, because this capacitor supplies the transient current associated with the fast switching waveforms of the power drive circuits. The recommended capacitor value is 10 µF. Ensure the capacitor dielectric material is compatible with the target application temperature.

#### *8.2.2.1 VISO Output Capacitor Selection*

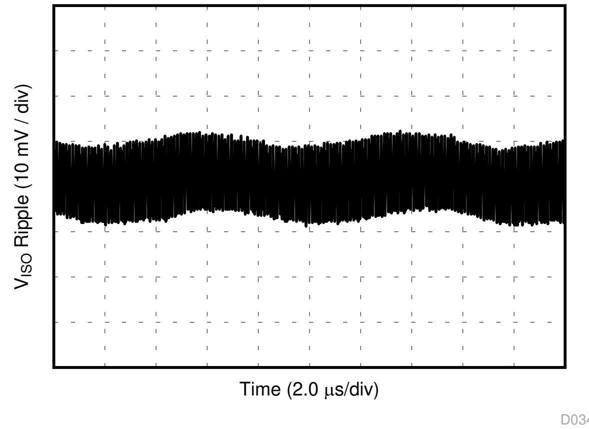
The UCC12040 is optimized to run with an effective output capacitance of 5 µF to 20 µF. A ceramic capacitor is recommended. Ceramic capacitors have DC-Bias and temperature derating effects, which both have influence the final effective capacitance. Choose the right capacitor carefully in combination with considering its package size, dielectric and voltage rating. It is good design practice to include one 0.1-µF capacitor close to the device for high-frequency noise reduction.

### 8.2.3 Application Curves



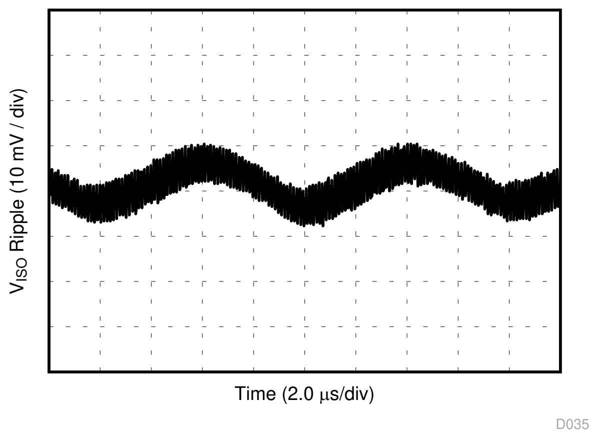

$V_{INP}$ = 5.0 V $V_{ISO}$ = 5.4 V Bandwidth = 20 MHz

**Figure 8-2. $V_{ISO}$ Ripple, 5.4-V Output, 10% Load**



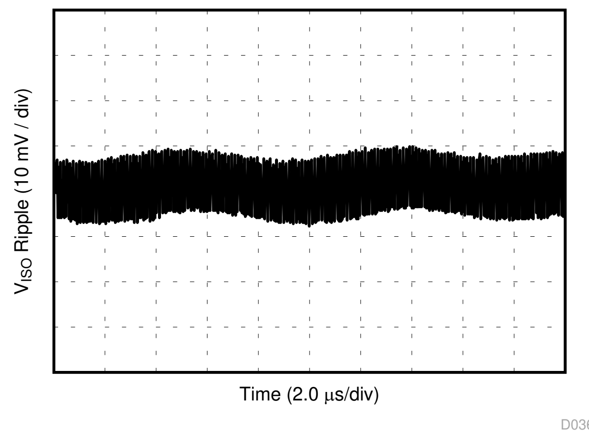

$V_{INP}$ = 5.0 V $V_{ISO}$ = 5.4 V Bandwidth = 20 MHz

**Figure 8-3. $V_{ISO}$ Ripple, 5.4-V Output, 90% Load**



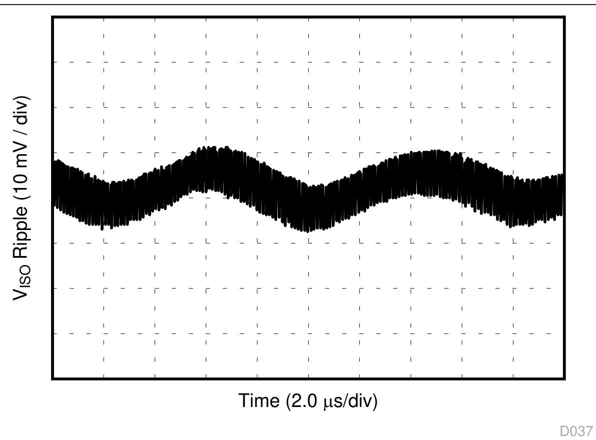

$V_{INP}$ = 5.0 V $V_{ISO}$ = 5.0 V Bandwidth = 20 MHz

**Figure 8-4. $V_{ISO}$ Ripple, 5.0-V Output, 10% Load**



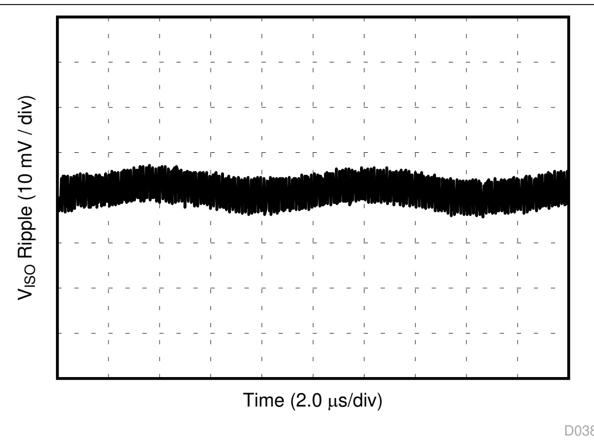

$V_{INP}$ = 5.0 V $V_{ISO}$ = 5.0 V Bandwidth = 20 MHz

**Figure 8-5. $V_{ISO}$ Ripple, 5.0-V Output, 90% Load**



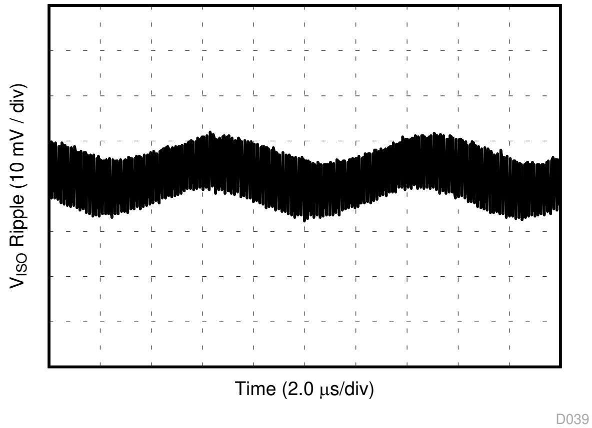

$V_{INP}$ = 5.0 V $V_{ISO}$ = 3.7 V Bandwidth = 20 MHz

**Figure 8-6. $V_{ISO}$ Ripple, 3.7-V Output, 10% Load**



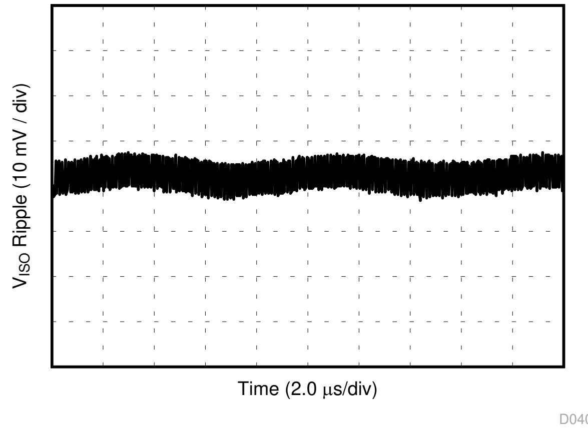

$V_{INP}$ = 5.0 V $V_{ISO}$ = 3.7 V Bandwidth = 20 MHz

**Figure 8-7. $V_{ISO}$ Ripple, 3.7-V Output, 90% Load**




$V_{INP}$ = 5.0 V    $V_{ISO}$ = 3.3 V    Bandwidth = 20 MHz

**Figure 8-8. $V_{ISO}$ Ripple, 3.3-V Output, 10% Load**




$V_{INP}$ = 5.0 V    $V_{ISO}$ = 3.3 V    Bandwidth = 20 MHz

**Figure 8-9. $V_{ISO}$ Ripple, 3.3-V Output, 90% Load**

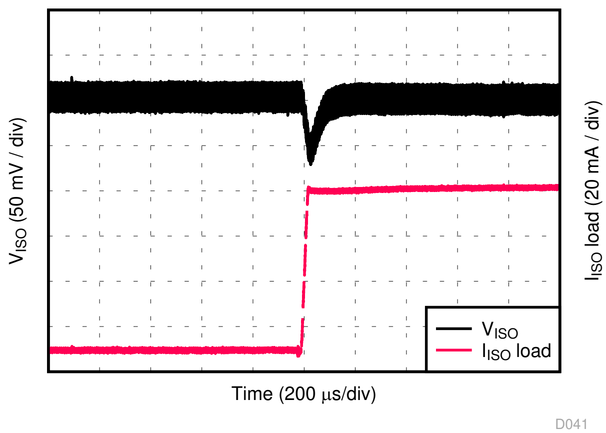



**Figure 8-10. $V_{ISO}$ Load Transient Response, 10% to 90% Load Step, 5.0-V Input, 5.4-V Output**

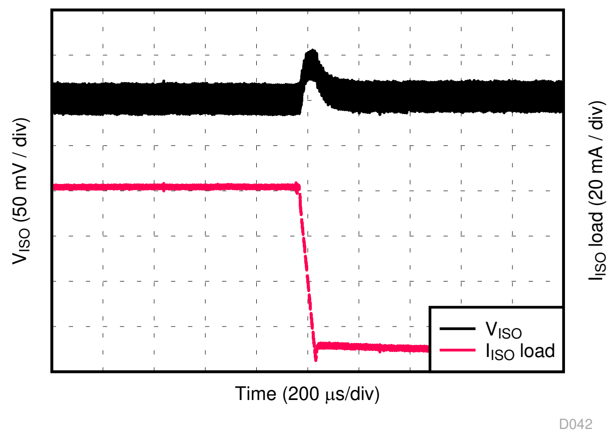



**Figure 8-11. $V_{ISO}$ Load Transient Response, 90% to 10% Load Step, 5.0-V Input, 5.4-V Output**

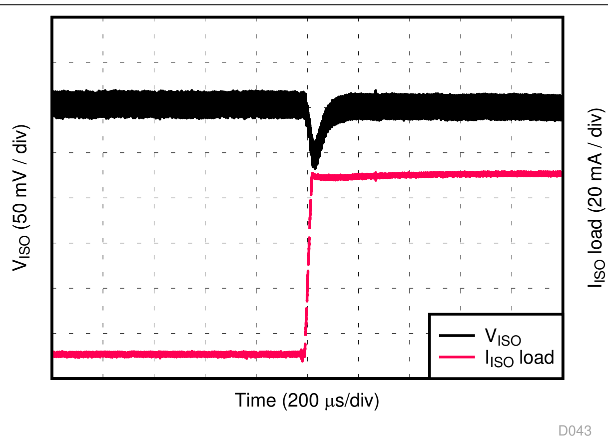



**Figure 8-12. $V_{ISO}$ Load Transient Response, 10% to 90% Load Step, 5.0-V Input, 5.0-V Output**

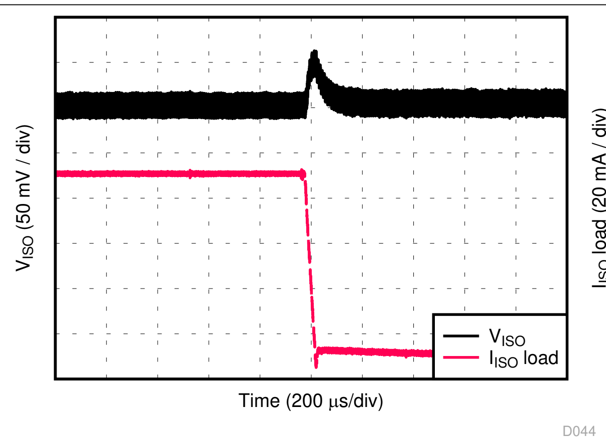



**Figure 8-13. $V_{ISO}$ Load Transient Response, 90% to 10% Load Step, 5.0-V Input, 5.0-V Output**

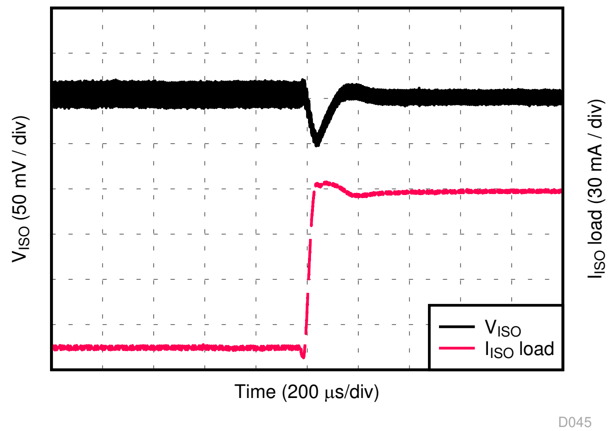



**Figure 8-14. $V_{ISO}$ Load Transient Response, 10% to 90% Load Step, 5.0-V Input, 3.7-V Output**

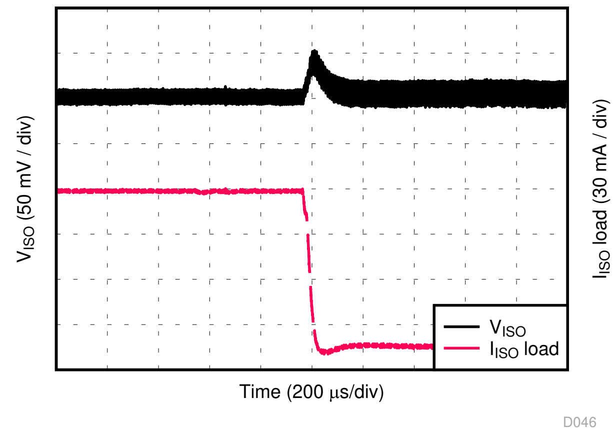



**Figure 8-15. $V_{ISO}$ Load Transient Response, 90% to 10% Load Step, 5.0-V Input, 3.7-V Output**

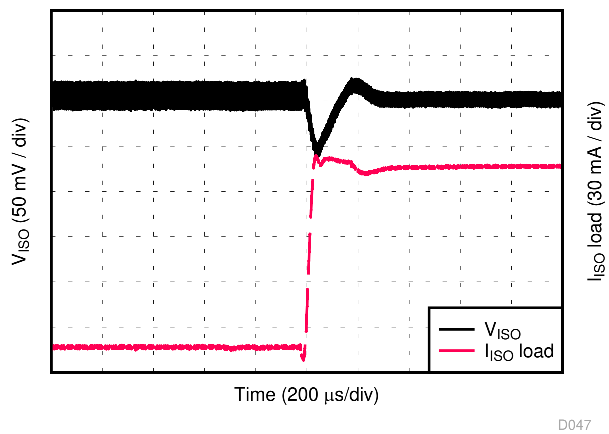



**Figure 8-16. $V_{ISO}$ Load Transient Response, 10% to 90% Load Step, 5.0-V Input, 3.3-V Output**

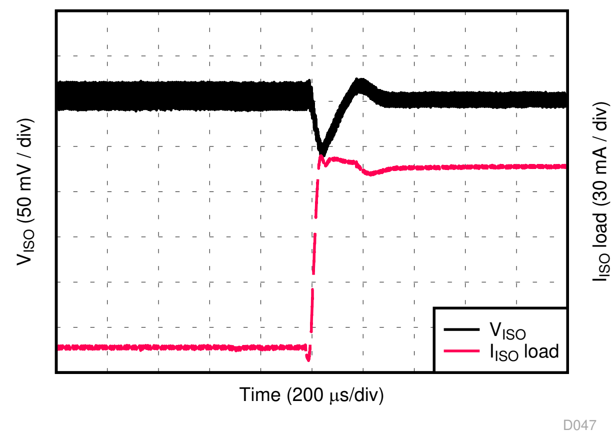



**Figure 8-17. $V_{ISO}$ Load Transient Response, 90% to 10% Load Step, 5.0-V Input, 3.3-V Output**

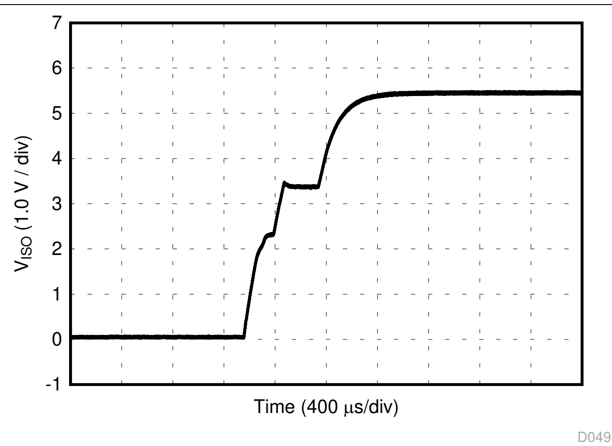



**Figure 8-18. $V_{ISO}$ Soft Start at 10% Rated Load, 5.0-V Input, 5.4-V Output**

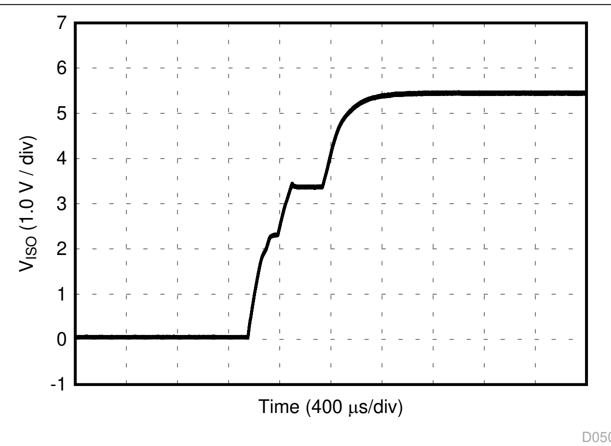



**Figure 8-19. $V_{ISO}$ Soft Start at 90% Rated Load, 5.0-V Input, 5.4-V Output**

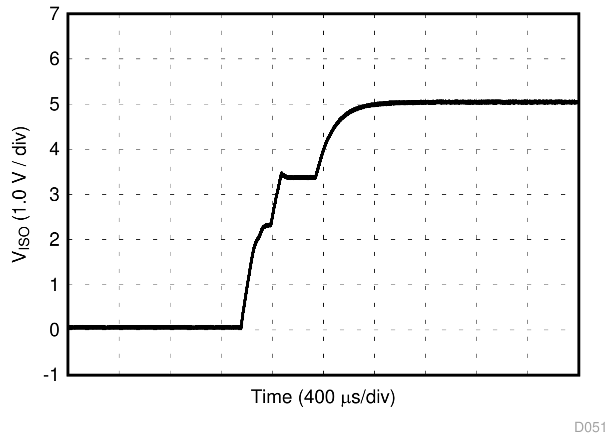



**Figure 8-20. $V_{ISO}$ Soft Start at 10% Rated Load, 5.0-V Input, 5.0-V Output**

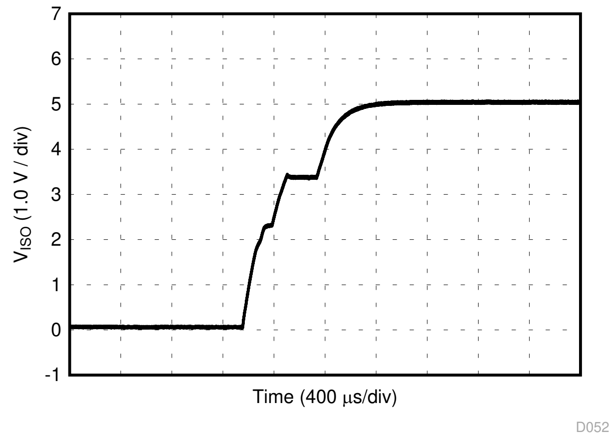



**Figure 8-21. $V_{ISO}$ Soft Start at 90% Rated Load, 5.0-V Input, 5.0-V Output**

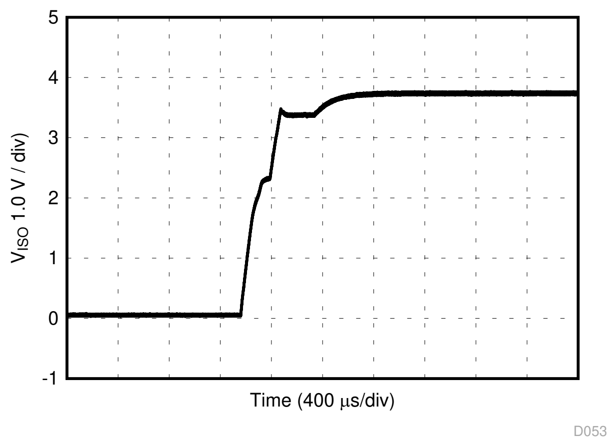



**Figure 8-22. $V_{ISO}$ Soft Start at 10% Rated Load, 5.0-V Input, 3.7-V Output**

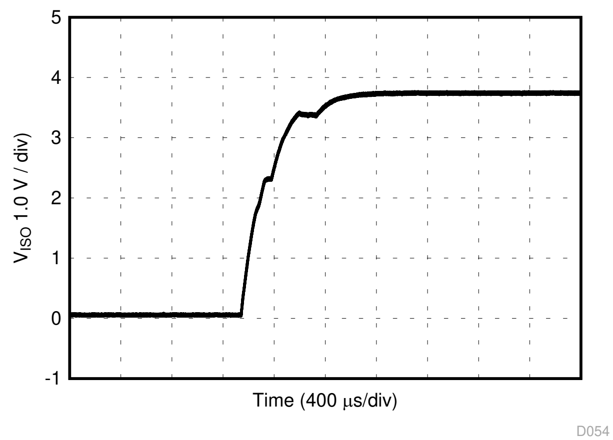



**Figure 8-23. $V_{ISO}$ Soft Start at 90% Rated Load, 5.0-V Input, 3.7-V Output**

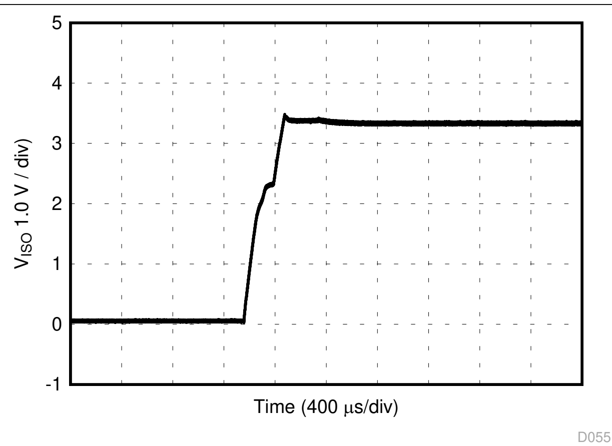



**Figure 8-24. $V_{ISO}$ Soft Start at 10% Rated Load, 5.0-V Input, 3.3-V Output**

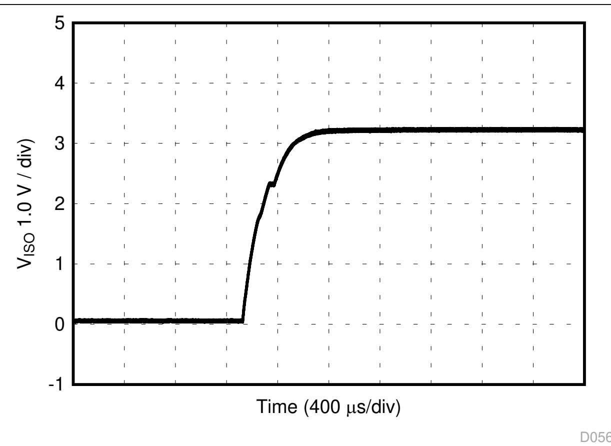



**Figure 8-25. $V_{ISO}$ Soft Start at 90% Rated Load, 5.0-V Input, 3.3-V Output**

# 9 Power Supply Recommendations

The recommended input supply voltage (VINP) for the UCC12040 is between 4.5 V and 5.5 V. To help ensure reliable operation, adequate decoupling capacitors must be located as close to supply pins as possible. Place local bypass capacitors between the VINP and GNDP pins at the input, and between VISO and GNDS at the isolated output supply. Low ESR, ceramic surface mount capacitors are recommended. It is further suggested that one place two such capacitors: one with a value of 10 µF for supply bypassing, and an additional 100-nF capacitor in parallel for high frequency filtering. The input supply must have an appropriate current rating to support output load required by the end application.

# 10 Layout

## 10.1 Layout Guidelines

The UCC12040 integrated isolated power solution simplifies system design and reduces board area usage. Proper PCB layout is important in order to achieve optimum performance. Here is a list of recommendations:

1. Place decoupling capacitors as close as possible to the device pins. For the input supply, place the capacitor(s) between pin 3 (VINP) and pin 2 (GNDP). For the isolated output supply, place the capacitor(s) between pin 14 (VISO) and pin 15 (GNDS). This location is of particular importance to the input decoupling capacitor, because this capacitor supplies the transient current associated with the fast switching waveforms of the power drive circuits.
2. Because the device does not have a thermal pad for heat-sinking, the device dissipates heat through the respective GND pins. Ensure that enough copper (preferably a connection to the ground plane) is present on all GNDP and GNDS pins for best heat-sinking.
3. If space and layer count allow, it is also recommended to connect the VINP, GNDP, VISO and GNDS pins to internal ground or power planes through multiple vias of adequate size. Alternatively, make traces for these nets as wide as possible to minimize losses.
4. TI also recommends grounding the no-connect pins (NC) to their respective ground planes. For pins 6, 7, and 8, connect to GNDP. For pins 10, 11, and 12, connect to GNDS. This will allow more continuous ground planes and larger thermal mass for heat-sinking.
5. A minimum of four layers is recommended to accomplish a low-EMI PCB design. Inner layers can be spaced closer than outer layers and used to create a high-frequency bypass capacitor between GNDP and GNDS to reduce radiated emissions. Ensure proper spacing, both inter-layer and layer-to-layer, is implemented to avoid reducing isolation capabilities. These spacings will vary based on the printed circuit board construction parameters, such as dielectric material and thickness.
6. Pay close attention to the spacing between primary ground plane (GNDP) and secondary ground plane (GNDS) on the PCB outer layers. The effective creepage and or clearance of the system will be reduced if the two ground planes have a lower spacing than that of the device package.
7. To ensure isolation performance between the primary and secondary side, avoid placing any PCB traces or copper below the UCC12040 device on the outer copper layers.

### 10.2 Layout Example

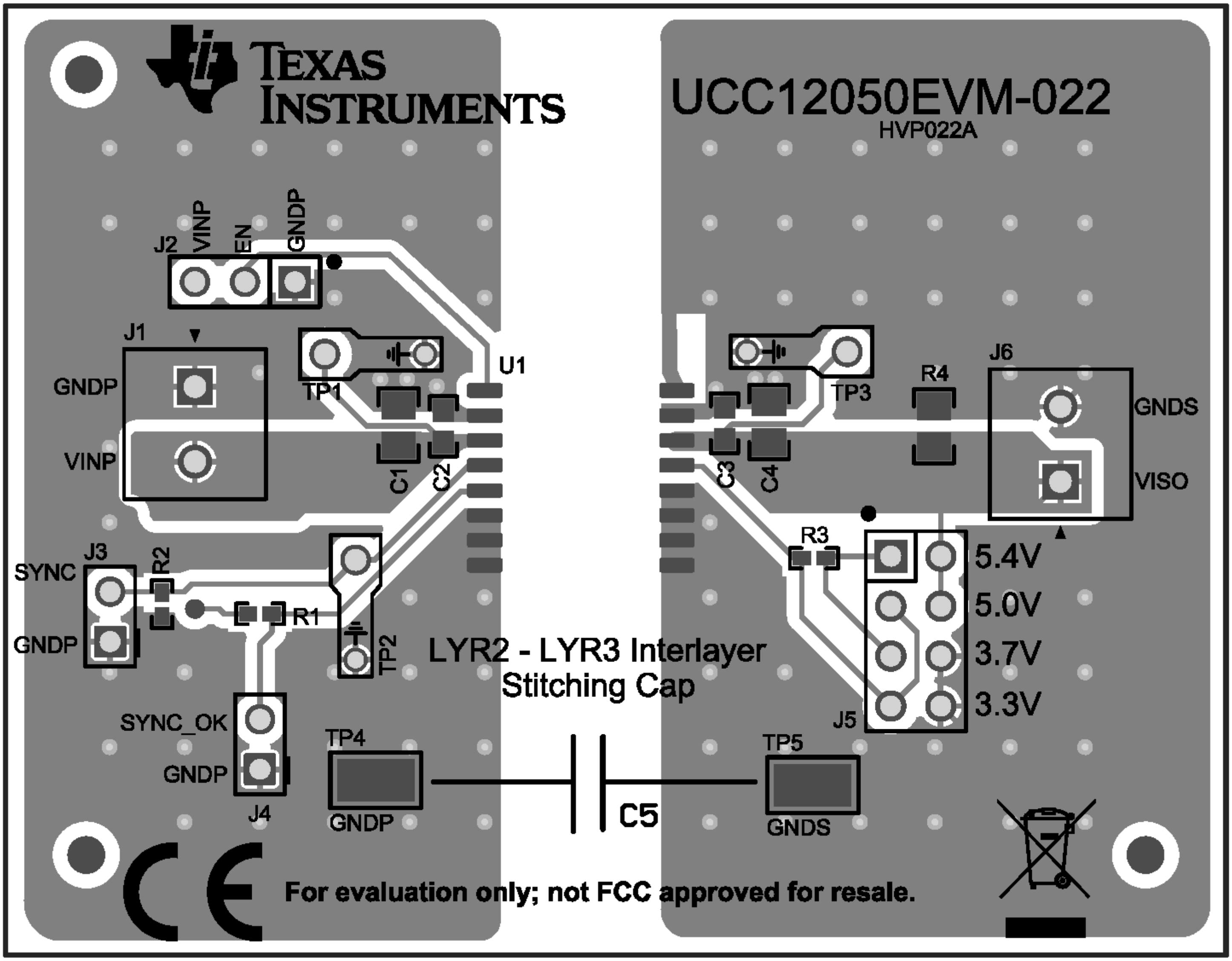



**Figure 10-1. Layout Example**

# 11 Device and Documentation Support

## 11.1 Device Support

### 11.1.1 Development Support

For development support, refer to:

- High-efficiency, low-emission, isolated DC/DC converter-based analog input module reference design
- Isolated delta-sigma modulator based AC/DC voltage and current measurement module reference design
- Isolated power architecture reference design for communication and analog input/output modules

## 11.2 Documentation Support

### 11.2.1 Related Documentation

For related documentation see the following:

- UCC12050 Evaluation Module User Guide
- Isolation Glossary
- A Reinforced-isolated Analog Input Chain for Space-constrained Applications

## 11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 11.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 11.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.7 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 12 Mechanical and Packaging Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| UCC12040DVE | Active | Production | SO-MOD (DVE) \| 16 | 40 \| TUBE | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | UCC12040 |
| UCC12040DVE.A | Active | Production | SO-MOD (DVE) \| 16 | 40 \| TUBE | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | UCC12040 |
| UCC12040DVEG4 | Active | Production | SO-MOD (DVE) \| 16 | 40 \| TUBE | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | UCC12040 |
| UCC12040DVEG4.A | Active | Production | SO-MOD (DVE) \| 16 | 40 \| TUBE | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | UCC12040 |
| UCC12040DVER | Active | Production | SO-MOD (DVE) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | UCC12040 |
| UCC12040DVER.A | Active | Production | SO-MOD (DVE) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | UCC12040 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

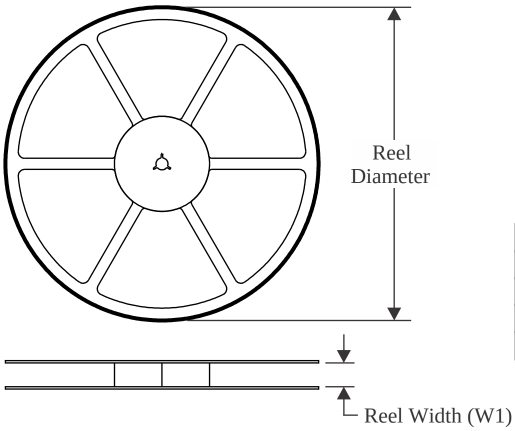
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

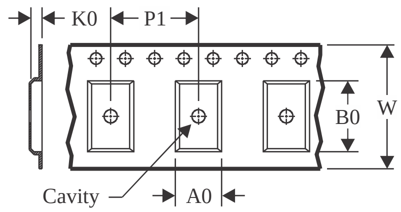
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

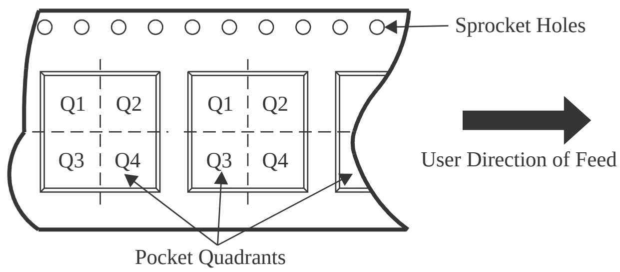



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

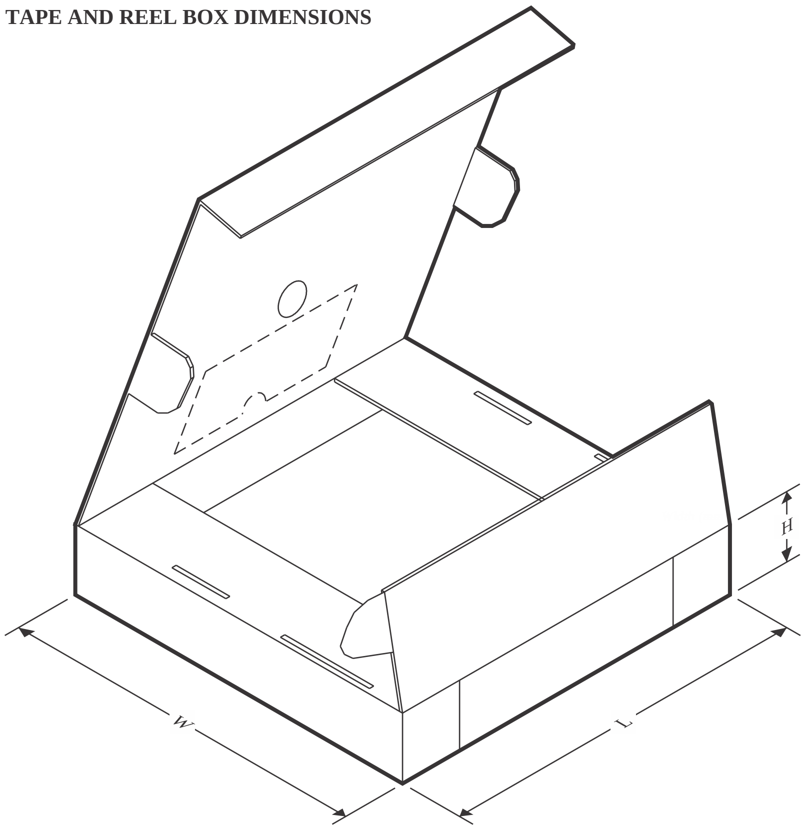
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| UCC12040DVER | SO-MOD | DVE | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |

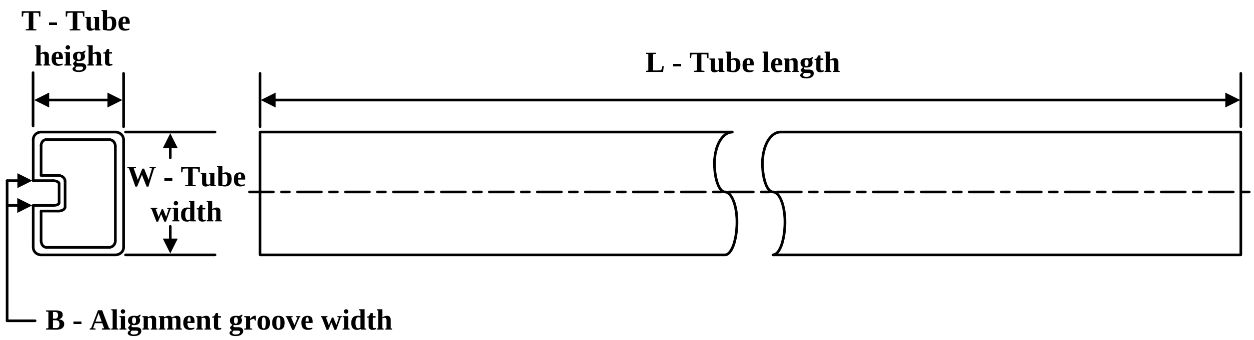
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

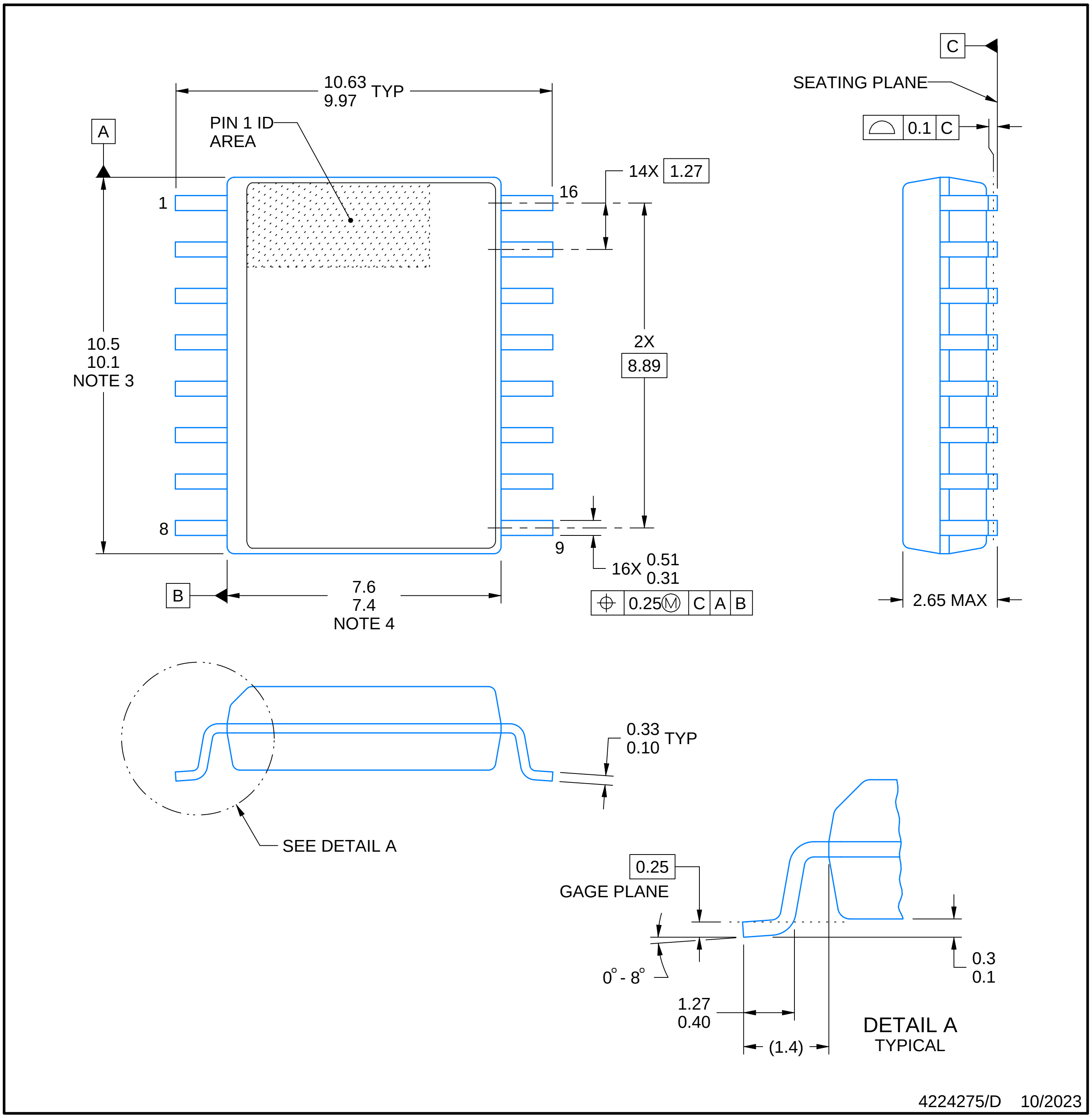
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| UCC12040DVER | SO-MOD | DVE | 16 | 2000 | 350.0 | 350.0 | 43.0 |

## TUBE



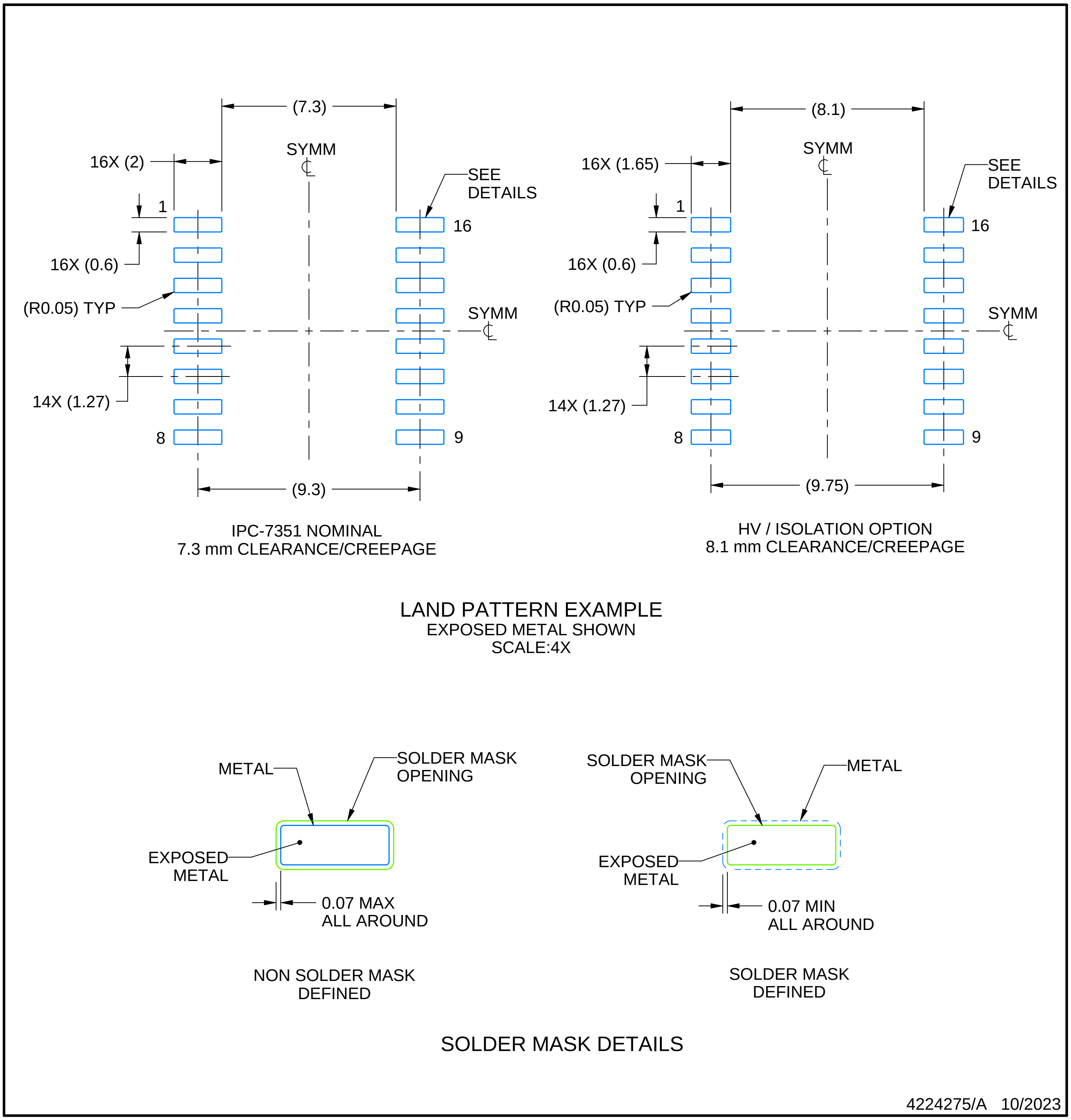

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| UCC12040DVE | DVE | SO-MOD | 16 | 40 | 506.98 | 12.7 | 4826 | 6.6 |
| UCC12040DVE.A | DVE | SO-MOD | 16 | 40 | 506.98 | 12.7 | 4826 | 6.6 |
| UCC12040DVEG4 | DVE | SO-MOD | 16 | 40 | 506.98 | 12.7 | 4826 | 6.6 |
| UCC12040DVEG4.A | DVE | SO-MOD | 16 | 40 | 506.98 | 12.7 | 4826 | 6.6 |



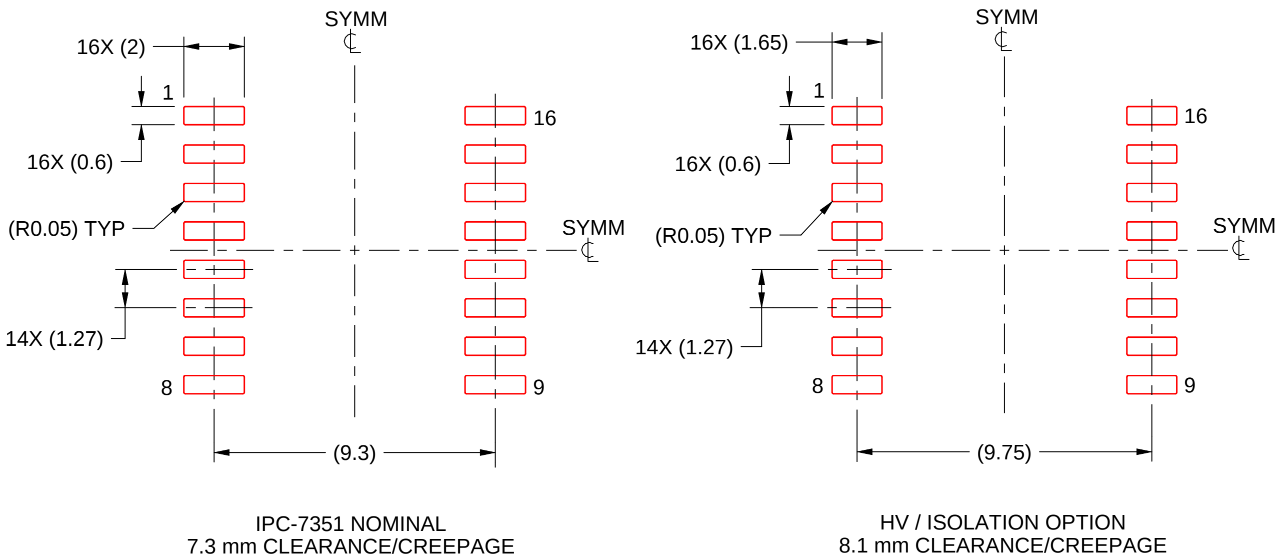

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.




NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4224275/D 10/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.