

UCC218302-Q1 15A Adjustable Drive Strength Reinforced Isolated Single Channel Gate Driver for SiC/IGBT with Advanced Protection

1 Features

- 5kV_{RMS} single channel isolated gate driver
- AEC-Q100 qualified for automotive applications
- Optimized for SiC MOSFETs and IGBTs switching up to 1500V_{pk}
- 30V maximum output drive voltage (VDD-VEE)
- Dual split outputs with on-the-fly drive strength selection
 - ±10A and ±5A drive current outputs
 - Digital input GD_SEL selects drive strength
- 500V/ns minimum CMTI
- 200ns response time fast DESAT protection with 9V threshold
- Dedicated Soft Shut Down (SSD) pin with 2.5A sinking capability. Shut down current is controllable by an external resistor.
- 4A internal active Miller clamp
- Overcurrent reporting on $\overline{\text{FLT}}$ and reset from $\overline{\text{RST/EN}}$
- Fast enable and disable response on $\overline{\text{RST/EN}}$
- 12V VDD UVLO with power good on RDY
- Overtemperature protection indicated on RDY
- Output voltage gate monitor with real-time output state feedback on OUT_FB.
- Active short circuit (ASC) input on secondary side to turn on power switch during system fault.
- Wide body package with creepage and clearance > 8mm
- AEC-Q100 qualified with the following results:
 - Device temperature grade 1: -40°C to +125°C ambient operating temperature

2 Applications

- [Traction inverter for EVs](#)
- [On-board charger and charging pile](#)
- [DC-DC converter for HEV/EVs](#)

3 Description

The UCC218302-Q1 is a galvanically isolated single-channel gate driver with advanced protection features, best-in-class dynamic performance, and robustness designed for SiC MOSFETs and IGBTs up to 1500V DC operating voltage. The UCC218302-Q1 has dual outputs up to ±10A and ±5A peak source and sink current.

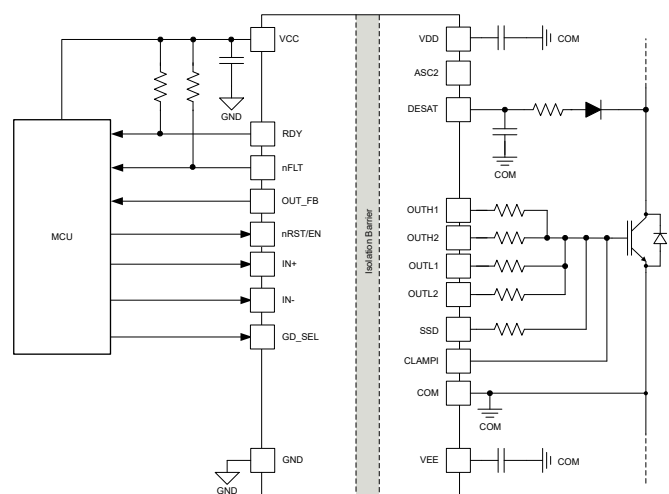
The input side is isolated from the output side with SiO₂ isolation technology, supporting up to 1.06kV_{RMS} working voltage and 10kV_{PK} surge immunity. The isolation barrier also provides low part-to-part skew, and >500V/ns common-mode noise immunity (CMTI).

The UCC218302-Q1 includes state-of-art protection features such as fast overcurrent and short-circuit detection, controlled soft shutdown after a fault, fault reporting, active Miller clamp, input and output side power supply UVLO to optimize SiC and IGBT switching behavior and robustness, active short circuit input on the secondary side, and output voltage gate monitoring.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
UCC218302B-Q1	DFP (SSOP 28)	7.6mm × 7.5mm

- (1) For all available packages, see [Section 10](#)
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic



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4 Pin Configuration and Functions

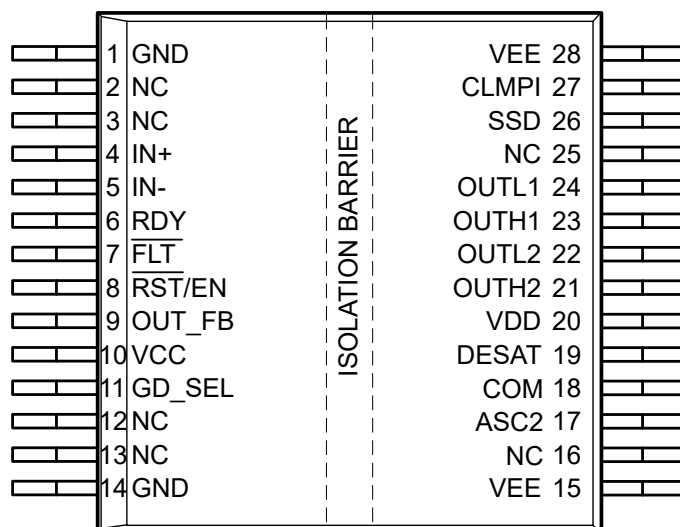


Figure 4-1. UCC218302-Q1 28 DFP Top View

Table 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
GND	1, 14	GND	Input power supply and logic ground reference.
NC	2, 3, 12, 13, 16, 25	—	No connection.
IN+	4	I	Non-inverting gate driver control input. Tie to VCC if unused.
IN-	5	I	Inverting gate driver control input. Tie to GND if unused.
RDY	6	O	Power good for VCC-GND, VDD-COM, and overtemperature. RDY is an open-drain output and can be paralleled with other RDY signals.
FLT	7	O	Active low fault alarm output upon overcurrent or short circuit. FLT is an open drain output and can be paralleled with other faults.
RST/EN	8	I	The RST/EN serves two purposes: 1) Enables or shuts down the output side. The FET is turned off by a regular turn-off if EN is set to low; 2) Resets the DESAT condition signaled on the FLT pin if RST/EN is set to low for more than 800ns. A reset of FLT is asserted at the rising edge of RST/EN.
OUT_FB	9	O	Real-time output voltage feedback. Leave floating if unused.
VCC	10	P	Input power supply from 3V to 5.5V. Bypass with a >1μF capacitor to GND. Place decoupling capacitor close to the pin.
GD_SEL	11	I	Gate drive strength selection input. Drive high to use both sets of outputs. Drive low to use only OUTx1 outputs.
VEE	15, 28	P	Negative supply rail for gate drive voltage. Bypass with a >10μF capacitor to COM. Place decoupling capacitor close to the pin.
ASC2	17	I	Active high secondary-side Active Short Circuit input to force output high during system failure events. Tie to COM if unused.
COM	18	P	Common ground reference. Connect to emitter pin for IGBTs and source pin for MOSFETs.
DESAT	19	I	Desaturation current protection input. Tie to COM if unused.
VDD	20	P	Positive supply rail for gate drive voltage. Bypass with a >10μF capacitor to COM. Place decoupling capacitor close to the pin.
OUTH2	21	O	High current gate driver output pullup.
OUTL2	22	O	High current gate driver output pulldown.
OUTH1	23	O	Low current gate driver output pullup.

Table 4-1. Pin Functions (continued)

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
OUTL1	24	O	Low current gate driver output pulldown.
SSD	26	O	Soft shutdown pull down for turning off after a DESAT fault. Connect a resistor from this pin to the gate of an IGBT or MOSFET to adjust the shutdown current. Leave floating or tie to VEE if unused.
CLMPI	27	O	Internal active Miller clamp. Connect this pin directly to the gate of the power transistor. Leave floating or tie to VEE if unused.

(1) I = input, O = output, P = power, GND = ground

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
VCC	VCC - GND	-0.3	6	V
VDD	VDD - COM	-0.3	36	V
VEE	VEE - COM	-17.5	0.3	V
V _{MAX}	VDD - VEE	-0.3	36	V
IN+, IN-, RST/EN, GD_SEL	DC	GND-0.3	VCC+0.3	V
FLT, RDY, OUT_FB	Voltage on primary-side output pins	GND-0.3	VCC	V
OUTH1, OUTH2, OUTL1, OUTL2, CLMPI	DC	VEE-0.3	VDD+0.3	V
	Transient, less than 100ns ⁽²⁾	VEE-5.0	VDD+5.0	V
DESAT	Voltage on DESAT, reference to COM	-0.3	VDD+0.3	V
ASC2	Voltage on ASC2, reference to COM	-0.3	6	V
I _{FLT} , I _{RDY}	FLT and RDY pin input current		20	mA
f _{MAX}	Maximum switching frequency		300	kHz
T _J	Junction temperature	-40	150	°C
T _{stg}	Storage temperature	-65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) Values are verified by characterization on bench.

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 ⁽¹⁾	±2000	V
		Charged device model (CDM), per AEC Q100-011	±750	
		Other pins	±500	V

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
VCC	VCC-GND	3	5.5	V
VDD	VDD-COM	13	30	V
VEE	VEE-COM	-16	0	V
V _{MAX}	VDD-VEE	13	30	V
IN+, IN-, RST/EN, GD_SEL	Reference to GND, High level input voltage	0.7 × VCC	VCC	V
	Reference to GND, Low level input voltage	0	0.3 × VCC	V
t _{RST/EN}	RST/EN pin pulse width that resets the fault	800		ns
ASC2	Reference to COM	0	5.5	V
T _A	Ambient temperature	-40	125	°C
T _J	Junction temperature	-40	150	°C

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		UCC218302	UNIT
		DFP (TSSOP)	
		28 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	77.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	36.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	20.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	42.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application note](#).

5.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation (both sides)	$T_a = 77^\circ\text{C}$		996		mW
P_{D1}	Maximum power dissipation by transmitter side			45		mW
P_{D2}	Maximum power dissipation by receiver side			951		mW

5.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	SPECIFIC ATION	UNIT
GENERAL				
CLR	External clearance ⁽¹⁾	Shortest terminal-to-terminal distance through air	> 8	mm
CPG	External Creepage ⁽¹⁾	Shortest terminal-to-terminal distance across the package surface	> 8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	> 17	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
	Material Group	According to IEC 60664–1	I	
	Overvoltage Category per IEC 60664–1	Rated mains voltage ≤ 300V _{RMS}	I-IV	
		Rated mains voltage ≤ 600V _{RMS}	I-III	
		Rated mains voltage ≤ 1000V _{RMS}	I-II	
DIN EN IEC 60747-17 (VDE 0884-17) ⁽²⁾				
V _{IORM}	AC voltage (bipolar)	AC voltage (bipolar)	1500	V _{PK}
V _{IOWM}	Maximum isolation working voltage	AC voltage (sine wave); time-dependent dielectric breakdown (TDDb) test; see Figure 1	1061	V _{RMS}
		DC voltage	1500	V _{DC}
V _{IOTM}	Maximum transient isolation voltage	V _{TEST} = V _{IOTM} , t = 60s (qualification test) V _{TEST} = 1.2 × V _{IOTM} , t = 1s (100% production test)	7071	V _{PK}
V _{IOSM}	Maximum surge isolation voltage ⁽³⁾	Test method per IEC 60065, 1.2/50μs waveform, V _{TEST} = 1.6 × V _{IOSM} = 11300V _{PK} (qualification)	10000	V _{PK}

5.6 Insulation Specifications (continued)

PARAMETER		TEST CONDITIONS	SPECIFIC ATION	UNIT
Q _{pd}	Apparent charge ⁽⁴⁾	Method a: After I/O safety test subgroup 2/3, V _{ini} = V _{IOTM} , t _{ini} = 60s; V _{pd(m)} = 1.2 × V _{IORM} , t _m = 10s	≤ 5	pC
		Method a: After environmental tests subgroup 1, V _{ini} = V _{IOTM} , t _{ini} = 60s; V _{pd(m)} = 1.6 × V _{IORM} , t _m = 10s	≤ 5	
		Method b1: At routine test (100% production) and preconditioning (type test), V _{ini} = V _{IOTM} , t _{ini} = 1s; V _{pd(m)} = 1.875 × V _{IORM} , t _m = 1s	≤ 5	
C _{IO}	Barrier capacitance, input to output ⁽⁵⁾	V _{IO} = 0.5 × sin (2πft), f = 1MHz	≅ 1.2	pF
R _{IO}	Insulation resistance, input to output ⁽⁵⁾	V _{IO} = 500V, T _A = 25°C	≥ 10 ¹²	Ω
		V _{IO} = 500V, 100°C ≤ T _A ≤ 125°C	≥ 10 ¹¹	
		V _{IO} = 500V at T _S = 150°C	≥ 10 ⁹	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V _{ISO}	Withstand isolation voltage	V _{TEST} = V _{ISO} = 5000V _{RMS} , t = 60s (qualification), V _{TEST} = 1.2 × V _{ISO} = 6000V _{RMS} , t = 1s (100% production)	5000	V _{RMS}

- (1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves and ribs on the PCB are used to help increase these specifications.
- (2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- (3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
- (4) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (5) All pins on each side of the barrier tied together creating a two-pin device.

5.7 Electrical Characteristics

VCC = 3.3V or 5.0V, 1μF capacitor from VCC to GND, VDD - COM = 20V, 18V or 15V, COM - VEE = 5V, 8V or 15V, C_L = 100pF, -40°C < T_J < 150°C (unless otherwise noted)⁽¹⁾⁽²⁾.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY QUIESCENT CURRENT						
I _{VCCQ}	VCC quiescent current	OUT = Low, f _s = 0Hz		3.5	5.6	mA
		OUT = High, f _s = 0Hz		6	8.4	mA
I _{VDDQ}	VDD quiescent current	OUT = High, f _s = 0Hz		7	8.1	mA
		OUT = Low, f _s = 0Hz		4	4.8	mA
I _{VEEQ}	VEE quiescent current	OUT = High, f _s = 0Hz, VEE = -5V	-7.5	-6.4		mA
		OUT = Low, f _s = 0Hz, VEE = -5V	-4.25	-3.7		mA
POWER SUPPLY PROTECTION						
V _{VCC_ON}	VCC UVLO rising threshold	Reference to GND	2.55	2.68	2.85	V
V _{VCC_OFF}	VCC UVLO falling threshold	Reference to GND	2.35	2.51	2.65	V
V _{VCC_HYST}	VCC UVLO hysteresis			170		mV
t _{VCCFIL}	VCC UVLO deglitch time			3		μs
t _{VCC+ to OUT}	VCC UVLO on delay to output high	IN+ = VCC, IN- = GND		7	16	μs
t _{VCC- to OUT}	VCC UVLO off delay to output low			6	9	μs
t _{VCC+ to RDY}	VCC UVLO on delay to RDY high	RST/EN = VCC		8	16	μs
t _{VCC- to RDY}	VCC UVLO off delay to RDY low			7	10	μs

5.7 Electrical Characteristics (continued)

VCC = 3.3V or 5.0V, 1μF capacitor from VCC to GND, VDD - COM = 20V, 18V or 15V, COM - VEE = 5V, 8V or 15V, C_L = 100pF, -40°C < T_J < 150°C (unless otherwise noted)⁽¹⁾⁽²⁾.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{VDD_UVLO_ON}	VDD UVLO rising threshold		11.4	12	12.6	V
V _{VDD_UVLO_OFF}	VDD UVLO falling threshold		10.45	11	11.55	V
V _{VDD_HYST}	VDD UVLO hysteresis			1		V
t _{VDDFIL}	VDD UVLO deglitch time			5		μs
t _{VDD+ to OUT}	VDD UVLO on delay to output high	IN+ = VCC, IN- = GND		5	8	μs
t _{VDD- to OUT}	VDD UVLO off delay to output low			5	10	μs
t _{VDD+ to RDY}	VDD UVLO on delay to RDY high	RST/EN = FLT = VCC		5	8	μs
t _{VDD- to RDY}	VDD UVLO off delay to RDY low			10	17	μs
PRIMARY SIDE LOGIC INPUTS (INx, RST/EN, GD_SEL)						
V _{INH}	Logic-high input threshold voltage (% of VCC)			57	70	%
V _{INL}	Logic-low input threshold voltage (% of VCC)		30	42		%
V _{INHYS}	Input threshold hysteresis (% of VCC)			15		%
I _{IH}	Input high level input leakage current	V _{IN} = VCC		50		uA
I _{IL}	Input low level input leakage current	V _{IN} = GND		-50		uA
R _{IND}	Input pins pull down resistance	IN+, RST/EN, GD_SEL		100		kΩ
R _{INU}	Input pins pull up resistance	IN-, RDY, FLT		100		kΩ
t _{INFIL}	INx, and RST/EN deglitch (ON and OFF) filter time	f _S = 50kHz	16	25	50	ns
t _{RSTFIL}	Deglitch filter time to reset FLT			500	800	ns
t _{GDSU}	Setup time for GD_SEL pin				50	ns
GATE DRIVER STAGE						
I _{OUTH1}	Peak source current	C _L = 0.22μF		5		A
I _{OUTH2}	Peak source current	C _L = 0.22μF		10		A
I _{OUTL1}	Peak sink current	C _L = 0.22μF		5		A
I _{OUTL2}	Peak sink current	C _L = 0.22μF		10		A
R _{OUTH1}	Output pull-up resistance	I _{OUTH1} = -100mA		0.725	1.35	Ω
R _{OUTH2}	Output pull-up resistance	I _{OUTH2} = -100mA		0.445	0.775	Ω
R _{OUTL1}	Output pull-down resistance	I _{OUTL1} = 100mA		0.725	1.35	Ω
R _{OUTL2}	Output pull-down resistance	I _{OUTL2} = 100mA		0.445	0.775	Ω
ACTIVE PULLDOWN						
V _{OUTPD}	Output active pull down on OUTLx	I _{OUTLx} = 100mA, VDD=OPEN, VEE=COM	1.0	1.4	1.85	V
INTERNAL MILLER CLAMP						
V _{CLMPH}	Miller clamp threshold voltage	Reference to VEE	1.5	2.1	2.5	V
I _{CLMPI}	Output low clamp current	V _{CLMPI} = 0V, VEE = -4V		4		A
R _{CLMPI}	Miller clamp pull down resistance	I _{CLMPI} = 0.1A		0.6	1.2	Ω
t _{DCLMPI}	Miller clamp ON delay time	C _L = 1.0nF		33	50	ns
SHORT CIRCUIT CLAMPING						
V _{CLP-OUTH1}	V _{OUTH1} - VDD	OUT = Low, I _{OUTH} = 100mA, t _{CLP} =10us		0.8	1.0	V
V _{CLP-OUTH2}	V _{OUTH2} - VDD	OUT = Low, I _{OUTH} = 100mA, t _{CLP} =10us		0.75	1.0	V

5.7 Electrical Characteristics (continued)

VCC = 3.3V or 5.0V, 1μF capacitor from VCC to GND, VDD - COM = 20V, 18V or 15V, COM - VEE = 5V, 8V or 15V, CL = 100pF, -40°C < TJ < 150°C (unless otherwise noted)⁽¹⁾⁽²⁾.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VCLP-OUTL1	VOUTL1 - VDD	OUT = High, IOUTL = 100mA, tCLP=10us		1.0	1.5	V
VCLP-OUTL2	VOUTL2 - VDD	OUT = High, IOUTL = 100mA, tCLP=10us		0.95	1.25	V
DESAT PROTECTION						
ICHG	Blanking capacitor charge current	VDESAT = 2.0V	420	540	580	μA
IDCHG	Blanking capacitor discharge current	VDESAT = 6.0V	18	20		mA
VDESATTH	Detection threshold		8.5	9	9.5	V
tDESATLEB	Leading edge blank time		160	200	280	ns
tDESATFIL	DESAT deglitch filter		60	125	150	ns
tDESATOFF	DESAT propagation delay to OUT 90%	VDESAT > VDESATTH		200	300	ns
tDESATFLT	DESAT to FLT low delay				1	μs
SOFT SHUTDOWN (SSD)						
ISSD	Peak sink soft shutdown peak current	CL = 0.22μF, fS = 1kHz		2.5		A
RSSD	Soft shutdown pull-down resistance	ISSD = 0.1A		1		Ω
tSSD	Soft shutdown ON time			25		μs
OUTPUT GATE VOLTAGE MONITOR						
VGMHI	Gate monitor threshold referenced to VDD	IN+ = high and IN- = low.		-3		V
VGMLO	Gate monitor threshold referenced to VEE	IN+ = low and IN- = X.		3		V
tGMFIL	Deglitch filter on gate monitor		0.9	1.2	1.6	μs
tGMFB	OUT to OUT_FB delay			1.7	2.4	μs
VGMFBOL	GM_FB output low voltage level	IGMFB = 10mA. Reference to GND			245	mV
VGMFBOH	GM_FB output high voltage level (offset below VCC)	IGMFB = 10mA			0.78	V
ACTIVE SHORT CIRCUIT (ASC)						
VASC2L	ASC2 input low threshold referenced to COM		1.2	1.45	1.7	V
VASC2H	ASC2 input high threshold referenced to COM		2.3	2.7	3.1	V
RASC2D	ASC2 input pulldown resistance			100		kΩ
tASC2FIL	ASC2 deglitch filter time		400		700	ns
tASC2_r	ASC2 on delay to output high				1	μs
tASC2_f	ASC2 off delay to output low				1	μs
OVERTEMPERATURE PROTECTION						
TSDTH	Thermal shutdown rising threshold		155		185	°C
TSDHYST	Thermal shutdown hysteresis			20		°C
FAULT REPORTING (FLT, RDY)						
tRDYHLD	UVLO RDY low minimum holding time		0.55		1	ms
tFLTMUTE	Output mute time on overcurrent fault	Reset fault through RST/EN	0.55		1	ms
RODON	Open drain output on resistance	IODON = 10mA. Reference to GND		25		Ω
VODL	Open drain low output voltage				0.4	V

5.7 Electrical Characteristics (continued)

VCC = 3.3V or 5.0V, 1μF capacitor from VCC to GND, VDD - COM = 20V, 18V or 15V, COM - VEE = 5V, 8V or 15V, C_L = 100pF, -40°C < T_J < 150°C (unless otherwise noted)⁽¹⁾⁽²⁾.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
COMMON MODE TRANSIENT IMMUNITY						
CMTI	CMTI noise immunity	V _{CM} = 1200V	500			V/ns

(1) Currents are positive into and negative out of the specified terminal.

(2) All voltages are referenced to COM unless otherwise noted

5.8 Switching Characteristics

VCC = 5.0V, 1μF capacitor from VCC to GND, VDD - COM = 20V, 18V or 15V, COM - VEE = 3V, 5V or 8V, C_L = 100pF, -40°C < T_J < 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PDLH}	Propagation delay time low-to-high	C _L = 1.0nF, R _G =0Ω		90	130	ns
t _{PDHL}	Propagation delay time high-to-low	C _L = 1.0nF, R _G =0Ω		90	130	ns
PWD	Pulse width distortion t _{PDHL} -t _{PDLH}				30	ns
t _{sk-pp}	Part to part skew	Rising or falling propagation delay			30	ns
t _r	Driver output rise time	C _L = 1.0nF, R _G =0Ω, VDD = 20V, VEE = 0V		13		ns
t _f	Driver output fall time	C _L = 1.0nF, R _G =0Ω, VDD = 20V, VEE = 0V		12		ns

6 Detailed Description

6.1 Overview

The UCC218302-Q1 is an advanced isolated gate driver with adjustable drive strength and state-of-art protection for SiC MOSFETs and IGBTs. The dual $\pm 10\text{A}$ and $\pm 5\text{A}$ peak sink and source currents of the device can drive SiC MOSFET modules and IGBT modules directly without an extra buffer. The driver can also be used to drive higher power modules or parallel modules with an external buffer stage.

The input side is isolated from the output side with a reinforced isolation barrier based on SiO_2 isolation technology, supporting up to $1.06\text{kV}_{\text{RMS}}$ working voltage and 10kV_{PK} surge immunity. The isolation technology supports 500V/ns minimum CMTI to maintain the reliability of the system with fast switching speeds. A short propagation delay and small part-to-part skew can minimize the dead time setting helping to reduce conduction losses.

The device includes extensive protection and monitor features to increase the reliability and robustness of SiC MOSFET and IGBT based systems. Primary and secondary-side supply UVLOs protect the system from operating when the supply voltage levels are too low. The active Miller clamp feature prevents the false turn on caused by Miller current during fast switching. The device has state-of-art DESAT detection time, as well as fault reporting to the low voltage side DSP/MCU. Soft shut down is triggered when the DESAT fault is detected, minimizing the short circuit energy while reducing the overshoot voltage on the switches. The device also has an active-short circuit input on the high-voltage side to force the power switch on during certain system fault conditions. Additionally, the device features an output voltage gate monitor to verify the output is following the input.

6.2 Functional Block Diagram

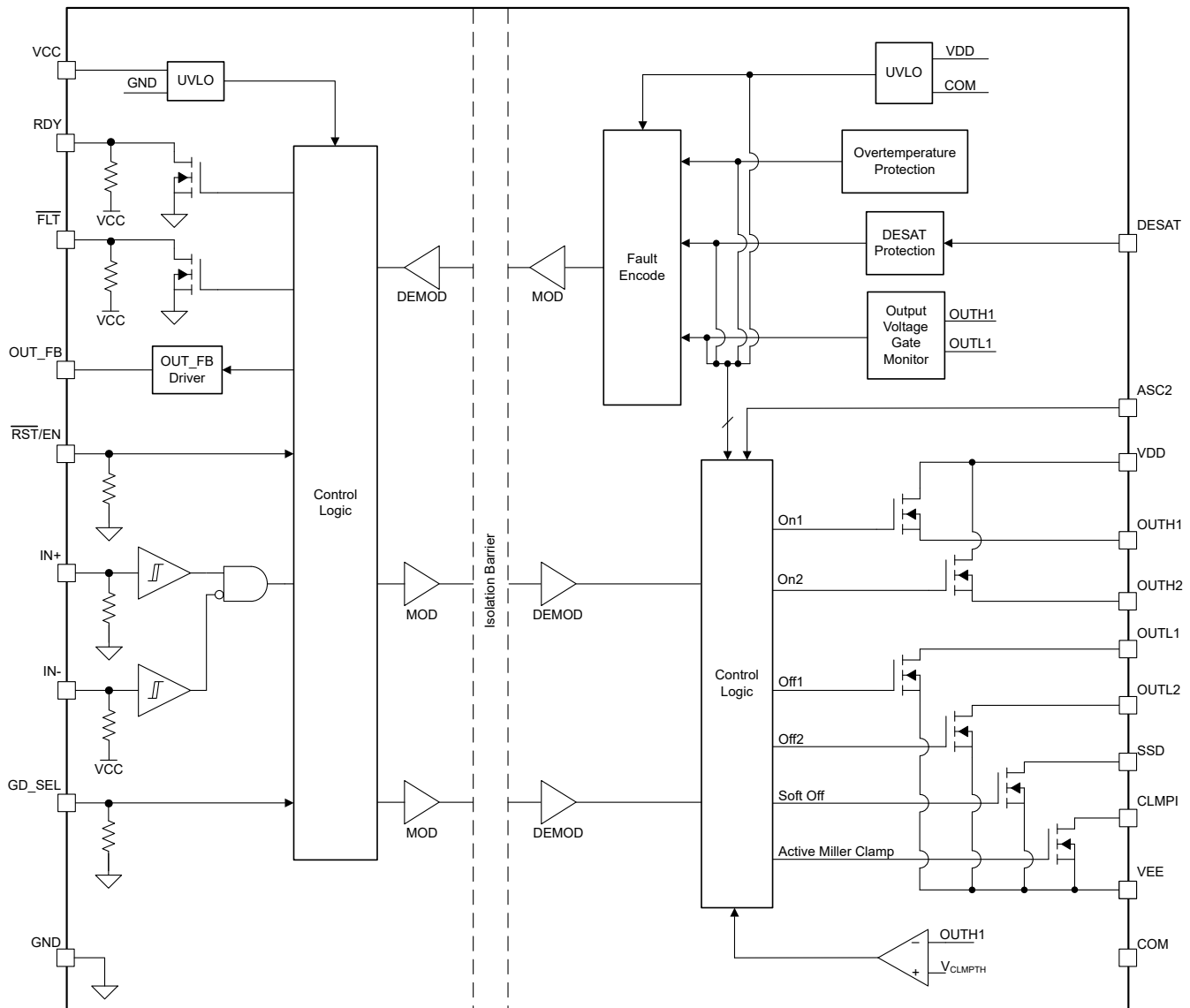


Figure 6-1. Functional Block Diagram of UCC218302-Q1

6.3 Feature Description

6.3.1 Power Supply

The input-side power supply VCC can support a wide voltage range from 3V to 5.5V to support both 3.3V and 5V controller signaling. An undervoltage comparator monitors VCC to verify valid operation. See [Section 6.3.2](#) for more information about the VCC undervoltage lockout protection.

The output-side power supply, VDD to VEE, can support a wide range up to 30V. The negative power supply, VEE, with respect to source or emitter, COM, is typically adopted to avoid false turn on when the other switch in the phase leg is turned on. Negative voltage is important for SiC MOSFETs because of the fast switching speeds of SiC MOSFETs, as well as for IGBTs, when not using an active Miller clamp. VDD is monitored by an undervoltage comparator to ensure valid operation. See [Section 6.3.2](#) for more information about the VDD undervoltage lockout protection.

6.3.2 VCC Undervoltage Lockout (UVLO)

The UCC218302-Q1 implements UVLO protection features for VCC. When the supply voltage is lower than the threshold voltage, the driver output is held low. The driver output does not turn on, and the RDY pin is held low until all of the supplies are above the UVLO thresholds. The UVLO protection feature reduces the power consumption of the driver during low voltage power supply conditions and increases the efficiency of the power stage. For SiC MOSFETs and IGBTs, the on-resistance reduces while the gate-source voltage or gate-emitter voltage increases. If the power semiconductor is turned on with a low VDD value, the conduction loss increases significantly and can lead to a thermal issue and efficiency reduction of the power stage.

The UVLO protection blocks feature comparator thresholds with hysteresis and deglitch filters on the inputs to help improve noise immunity of the power supply. During the turn-on and turn-off switching transients, the driver sources and sinks a peak transient current from the power supply, which can result in sudden voltage drop of the power supply. With hysteresis and UVLO deglitch filters, the internal UVLO protection blocks ignores small disturbance during the normal switching transients.

The RDY pin on the input side is used to indicate power good condition. The RDY pin is open drain. During UVLO conditions, the RDY pin is held low and connected to GND. Normally the pin is pulled up externally to VCC to indicate power is good.

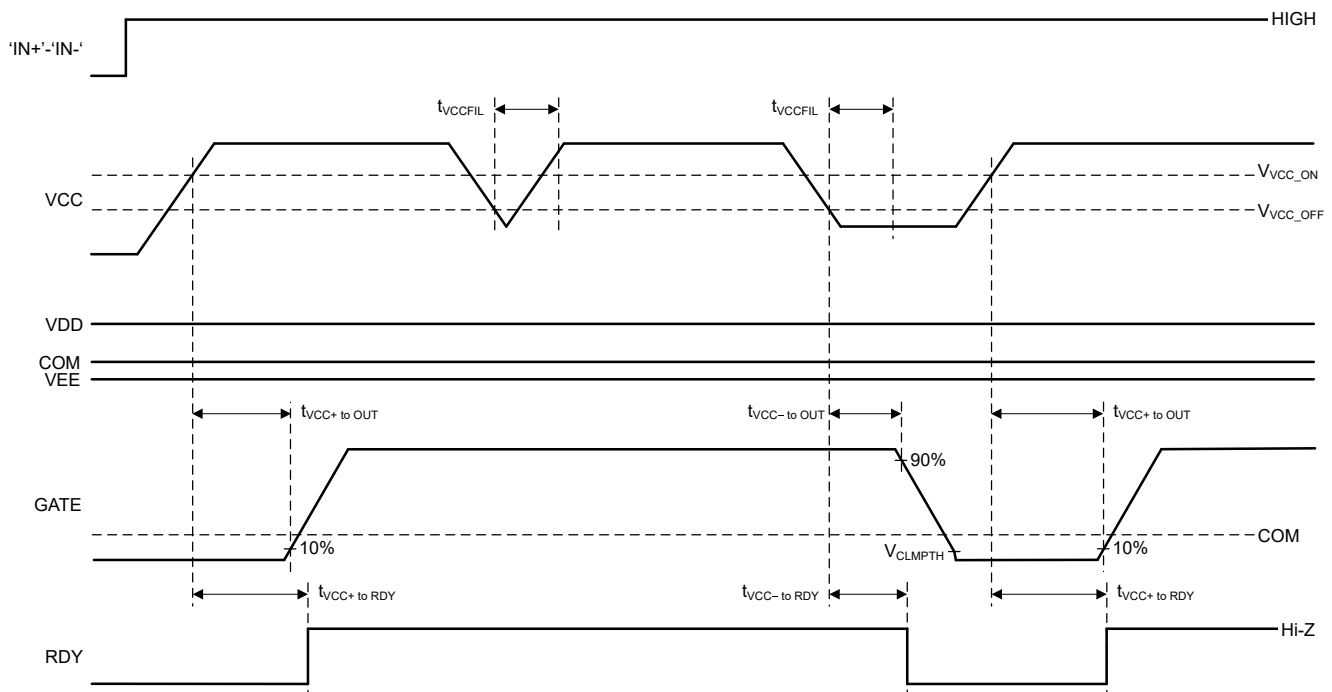


Figure 6-2. VCC Protection Timing Diagram

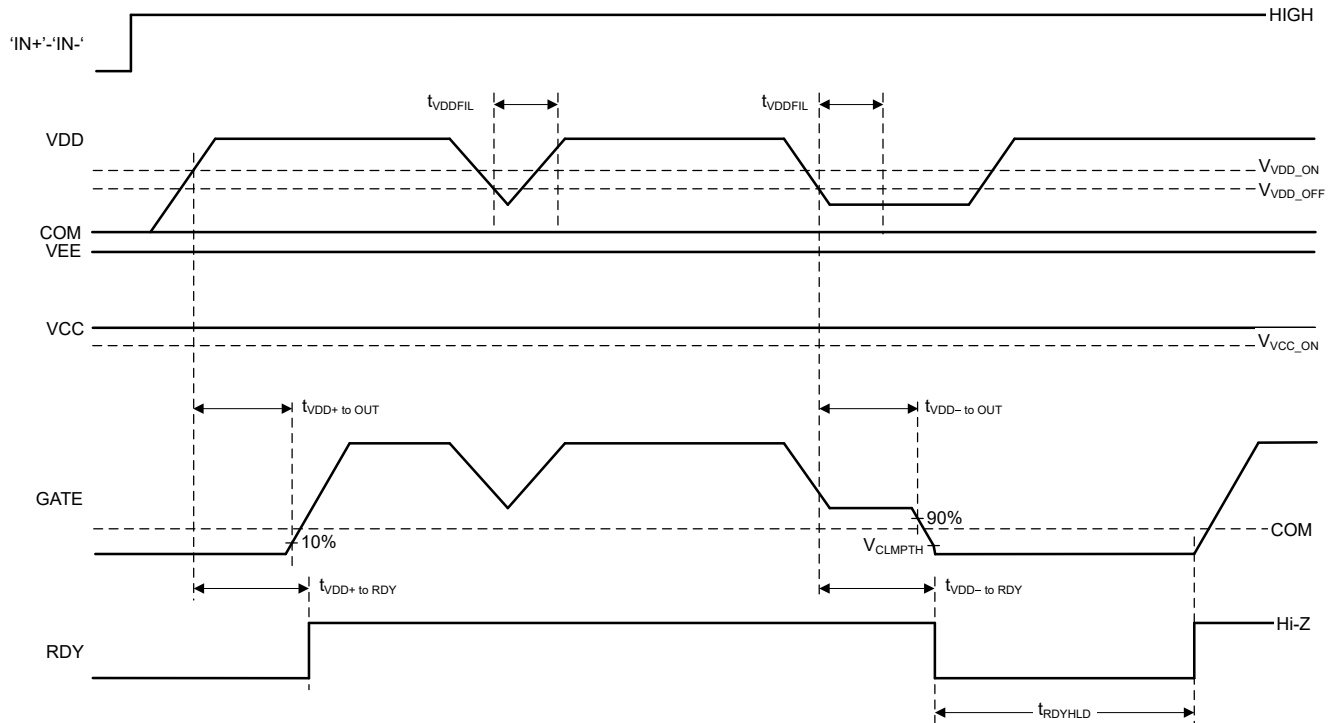


Figure 6-3. VDD Protection Timing Diagram

6.3.3 Input Filters for IN+, IN-, and $\overline{\text{RST/EN}}$

The input pins to the UCC218302-Q1 are both 3.3V and 5V logic compatible. The IN+ and $\overline{\text{RST/EN}}$ pins have internal pulldown resistors, and the IN- pin has an internal pullup resistor. If any of these pins are left floating, the driver is disabled unless active short circuit is activated. The driver has both inverting and non-inverting PWM input pins. If using only the non-inverting IN+ input, tie IN- to GND. If using only the inverting IN- input, tie IN+ to VCC. Both IN+ and IN- are useable for PWM interlocking with the other driver in a half-bridge configuration to prevent phase leg shoot-through.

The device features internal deglitch filters on the IN+, IN-, and $\overline{\text{RST/EN}}$ pins to protect against unintentional switching due to noise transients or narrow PWM pulses. Any signal less than t_{INFIL} is filtered out and not passed through. For noisy systems, add external low-pass filters externally to the input pins to further increase noise immunity. When selecting low-pass filter components, consider both noise immunity and delay time, according to system requirements. [Figure 6-4](#) shows the impact of the deglitch filters with narrow pulses on IN+, IN-, and $\overline{\text{RST/EN}}$.

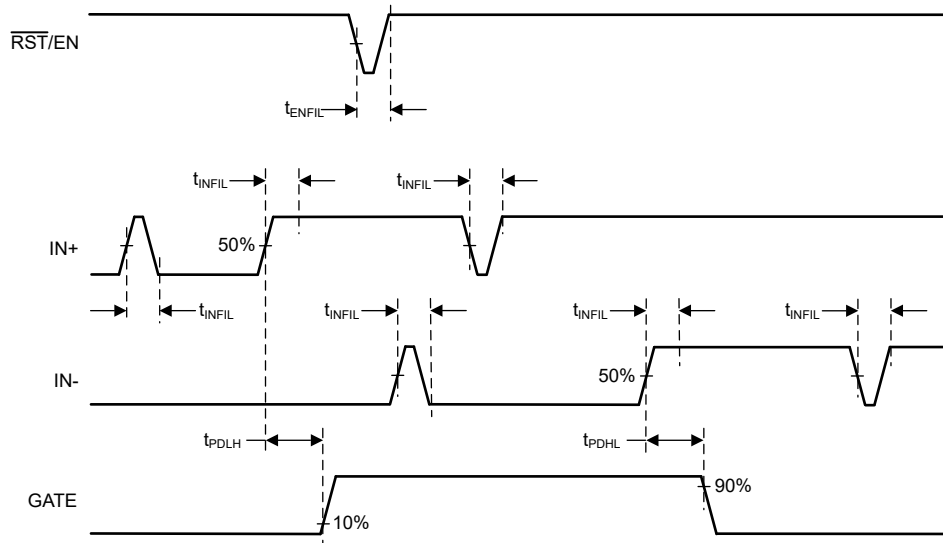


Figure 6-4. Impact of Deglitch Filters

6.3.4 Active Pulldown

UCC218302-Q1 implements an active pulldown feature to verify the OUTLx pins are clamped to VEE when VDD is open. The OUTLx pins are in high-impedance state when VDD is open. However, if voltage is present on the OUTLx pins external to the gate driver, the voltage drives the pull-down FET through R_a and pulls down the output preventing the device from turning on, as Figure 6-5 shows.

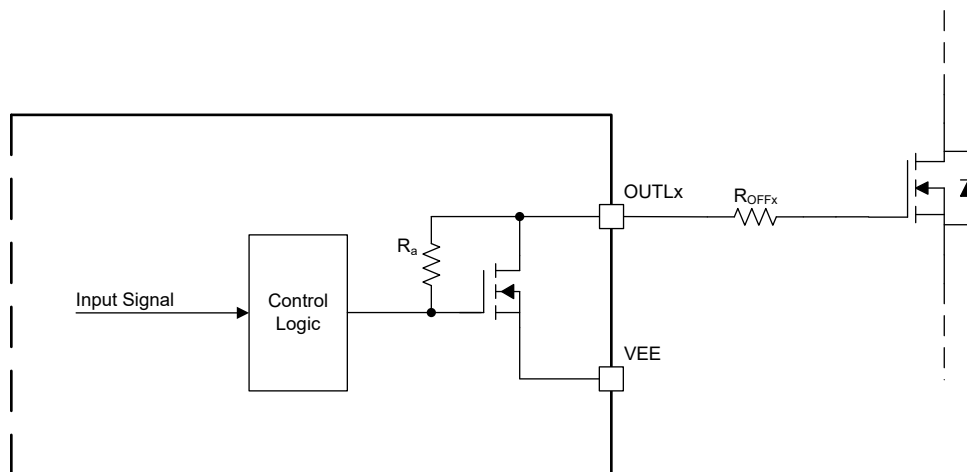


Figure 6-5. Active Pulldown

6.3.5 Short Circuit Clamping

The UCC218302-Q1 has integrated diodes to prevent OUTHx and OUTLx from exceeding VDD. The short circuit clamping function clamps the voltages at the driver outputs to be slightly higher than VDD during power switch short circuit conditions.

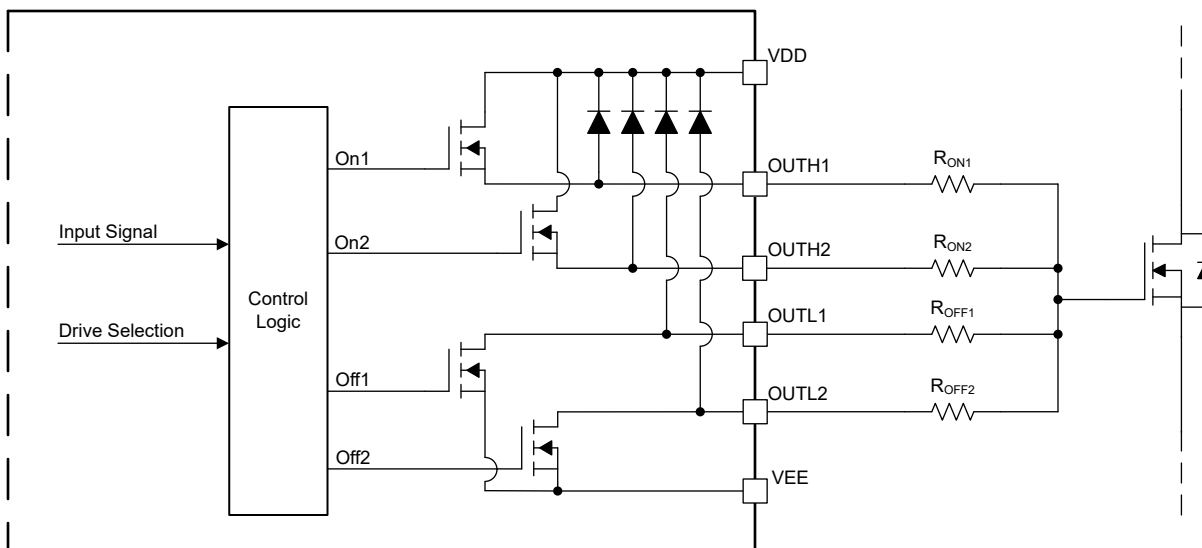


Figure 6-6. Short Circuit Clamping

6.3.6 Internal Active Miller Clamp

The UCC218302-Q1 has an active Miller clamp function to add an additional low impedance path to prevent unintentional turn-on while the driver is in the OFF state. In half-bridge applications, the body diode of the power semiconductor device can conduct while the driver is in the OFF state during dead time. When this occurs, and the other power semiconductor device in the phase leg turns on, the drain-to-source or collector-to-emitter voltage increases rapidly, causing high dV/dt across the Miller capacitance. This high dV/dt induces a current spike that can charge the gate capacitance and cause shoot-through if the main turn-off path is not strong enough due to an external turn-off resistor, long PCB routing traces, or both.

The internal active Miller clamp function provides an internal strong pull-down FET. The FET turns on when the power semiconductor device gate voltage is less than the Miller clamp threshold, V_{CLMPH} . The gate voltage is sensed through the OUTH1 pin. Figure 6-7 shows a simplified block diagram and Figure 6-8 shows a timing diagram.

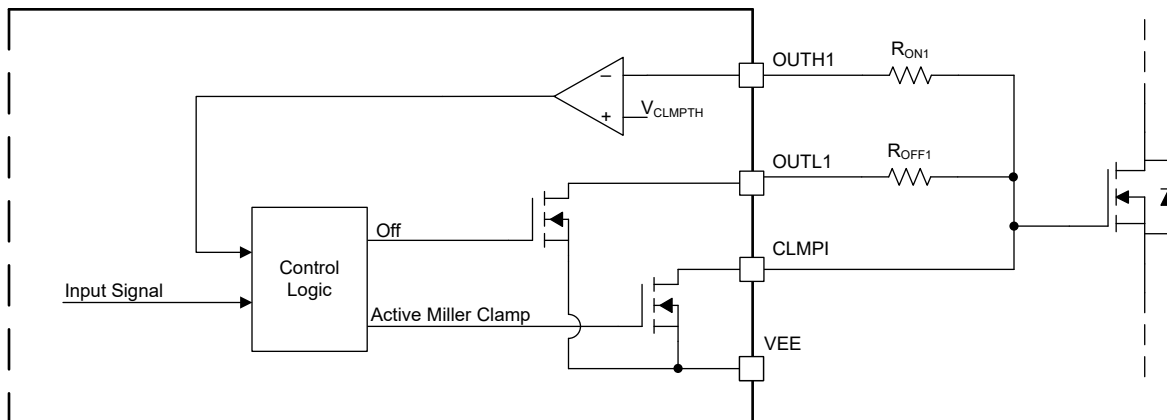


Figure 6-7. Internal Active Miller Clamp

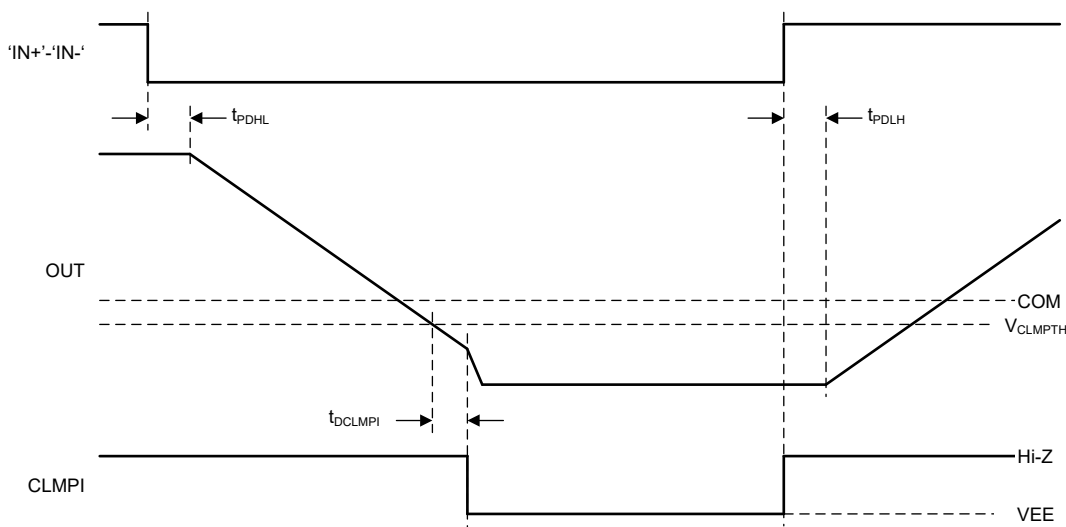


Figure 6-8. Internal Active Miller Clamp Timing Diagram

6.3.7 Desaturation (DESAT) Protection

The UCC218302-Q1 implements a fast overcurrent and short-circuit protection feature to protect the power semiconductor device from catastrophic breakdown during a fault. The DESAT pin threshold, V_{DESATTH} , is with respect to COM, the source or emitter of the power semiconductor device. When the driver is in the off state, an internal MOSFET pulls down the DESAT pin to prevent DESAT from false triggering. When the driver is in the on state, an internal current source activates to charge an external capacitor. The UCC218302-Q1 features an internal leading edge blanking time after OUTHx switches to the on state to avoid false triggers from noise during the switching transient. During the leading edge blanking time period, the DESAT pin is pulled-down by the internal pulldown MOSFET. When the driver turns off, the internal pulldown MOSFET discharges the voltage of the DESAT pin. [Figure 6-9](#) shows a simplified block diagram of the DESAT circuit. [Figure 6-10](#) shows timing diagrams showing a DESAT fault, soft shutdown, fault reporting, and fault reset.

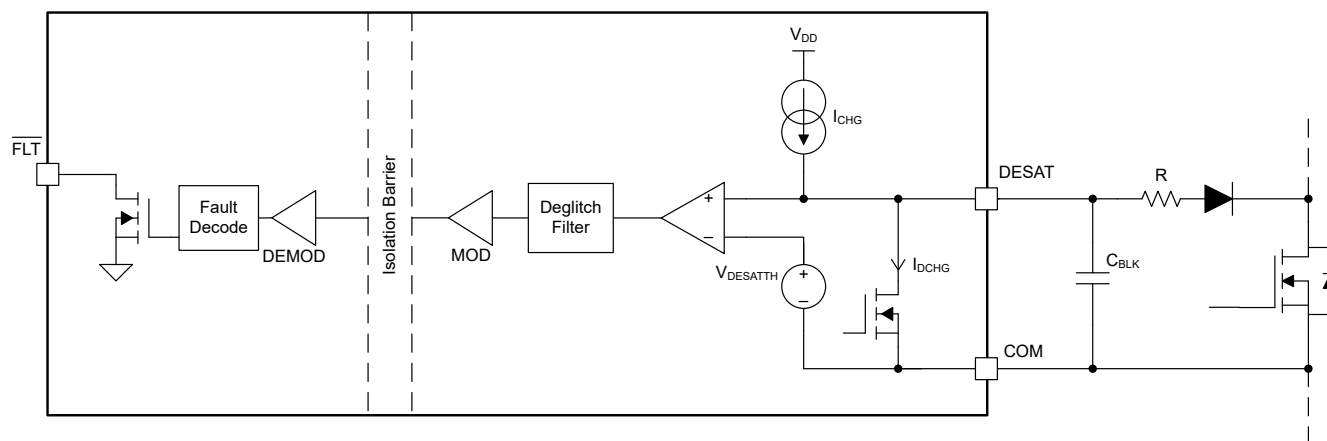


Figure 6-9. DESAT Protection

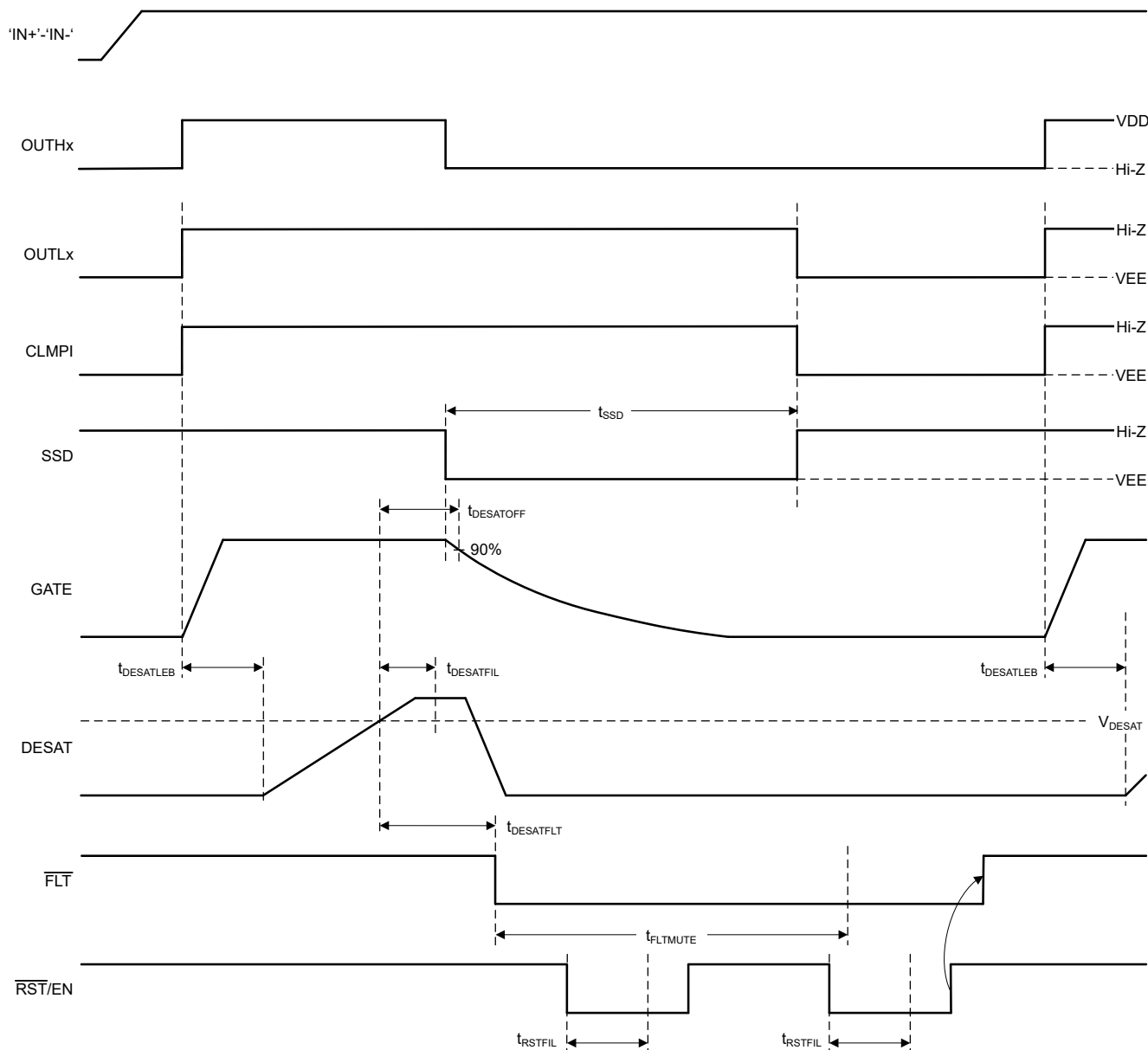


Figure 6-10. DESAT Protection Timing Diagram with Soft Shutdown

6.3.8 Soft Shutdown (SSD)

When detecting a DESAT fault, the UCC218302-Q1 initiates a soft shutdown (SSD) to protect the power semiconductor device. When an overcurrent or short circuit event occurs, the SSD feature slowly discharges the gate voltage to limit the overshoot voltage on the switching device created by high di/dt due to the channel current. A tradeoff occurs between the overshoot voltage and the short-circuit energy. The turn-off speed must be slow enough to limit the overshoot voltage, but the shutdown time must not be too long that the large energy dissipation in the device can cause breakdown. The UCC218302-Q1 provides an internal pulldown FET that can be used with an external resistor to optimize the discharge current of the gate. When a DESAT fault is detected, OUTHx and OUTLx are Hi-Z so that the gate is not driven by the main driver outputs. The internal pulldown MOSFET on the SSD pin turns on for t_{SSD} to let the gate discharge. After this time, CLMPI and OUTLx are driven low to hold the power semiconductor device off. [Figure 6-11](#) shows a simplified block diagram and [Figure 6-10](#) shows a timing diagrams.

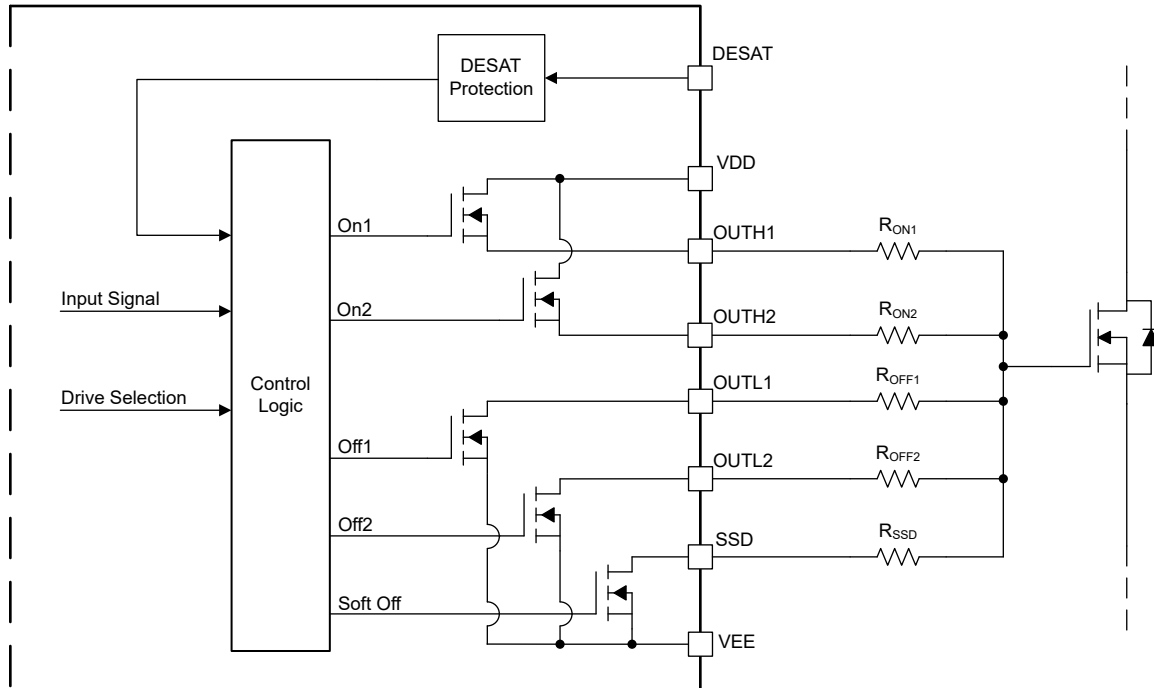


Figure 6-11. Soft Shutdown

6.3.9 Fault ($\overline{\text{FLT}}$), Reset, and Enable ($\overline{\text{RST/EN}}$)

The $\overline{\text{FLT}}$ pin is open drain and can report a fault signal to the DSP/MCU when the DESAT pin detects a fault. The $\overline{\text{FLT}}$ pin pulls down to GND after detecting a fault, and is held low until receiving a reset signal from $\overline{\text{RST/EN}}$. The device has a fault mute time t_{FLTMUTE} , within which the device ignores any reset signal.

The $\overline{\text{RST/EN}}$ pin is pulled down internally and is thus disabled by default when this pin is floating. The pin must be pulled up externally to enable the driver. The pin has two purposes:

- To enable and shut down the device. If the $\overline{\text{RST/EN}}$ pin pulls low for longer than t_{INFIL} , the driver disables and depending on GD_SEL logic level, OUTLx activates to turn off the gate of the IGBT or SiC MOSFET.
- To reset the DESAT fault signaled on the $\overline{\text{FLT}}$ pin. If the $\overline{\text{RST/EN}}$ pin pulls low for more than t_{RSTFIL} after the mute time t_{FLTMUTE} , then the fault signal is reset and $\overline{\text{FLT}}$ returns to a high-impedance state upon the next rising edge applied to the $\overline{\text{RST/EN}}$ pin. Figure 6-10 shows a timing diagram.

6.3.10 Output Gate Voltage Monitor

Output gate voltage monitoring is implemented to make sure the gate driver output matches the inputs, IN+ and IN-. When the PWM signal ('IN+' - 'IN-') is high, the output is compared to the V_{GMHI} reference. When the PWM signal is low, the output is compared to the V_{GMLO} reference. Real-time gate monitor feedback is provided on the low-voltage side OUT_FB pin. The output status given on the OUT_FB pin can be compared to the PWM input by the MCU to determine if the system is operating properly or if a fault condition exists. See Figure 6-12 for a block diagram, Figure 6-13 for a timing diagram, and Table 6-1 for a truth table of the output gate voltage monitor feature.

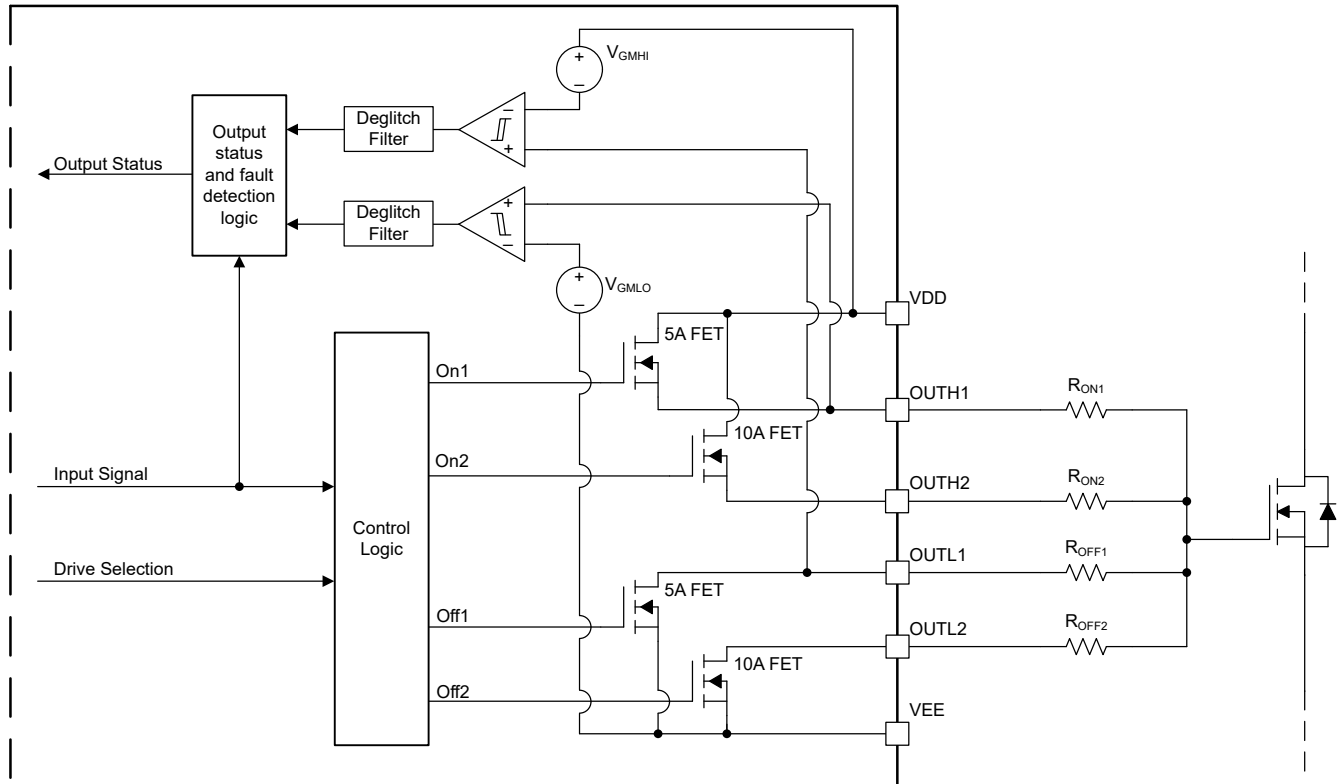


Figure 6-12. Output Gate Voltage Monitor

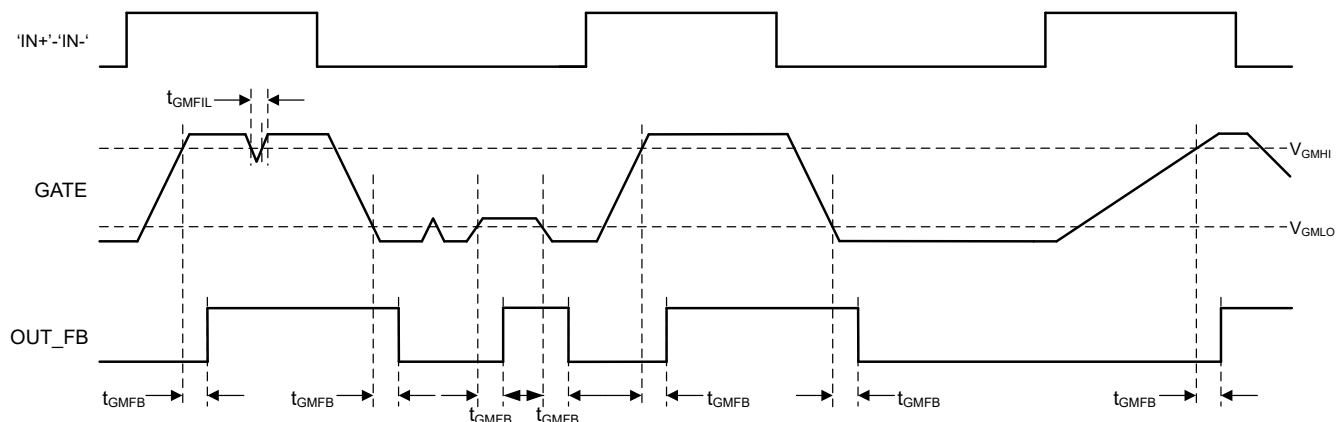


Figure 6-13. Output Gate Voltage Monitor Timing Diagram

Table 6-1. Output Gate Voltage Monitor Steady State Truth Table

PWM ('IN+' - 'IN-')	GATE VOLTAGE	OUT_FB
L	$V_{GATE} < V_{GMLO}$	L
L	$V_{GATE} > V_{GMLO}$	H
H	$V_{GATE} < V_{GMHI}$	L
H	$V_{GATE} > V_{GMHI}$	H

6.3.11 Active Short Circuit (ASC) Support

The active short circuit (ASC) function allows the system to force the state of the power transistor on regardless of the PWM input. This is important in traction inverter applications where the motor can lose control and feed

energy back to the battery. Overvoltage of the battery can cause battery break down and can even be a fire hazard. For this scenario, use the ASC function to protect the system by forcing the output on, turning on the power switch, and creating an active short circuit loop between the motor phases to bypass the battery. The UCC218302-Q1 has a secondary-side input (ASC2) referenced to COM. When the ASC2 input pin is high, the driver output is forced on. The GD_SEL input at the time of ASC2 going high determines the OUTx1/OUTx2 output selection. The ASC2 input has higher priority than VCC UVLO and primary-side inputs. Secondary-side supply UVLOs, DESAT, and output gate voltage monitor faults are higher priority than the ASC2 input. [Figure 6-14](#) [Figure 6-15](#) and [Figure 6-16](#) show timing diagrams of ASC2 support with VCC UVLO, VDD UVLO, and DESAT.

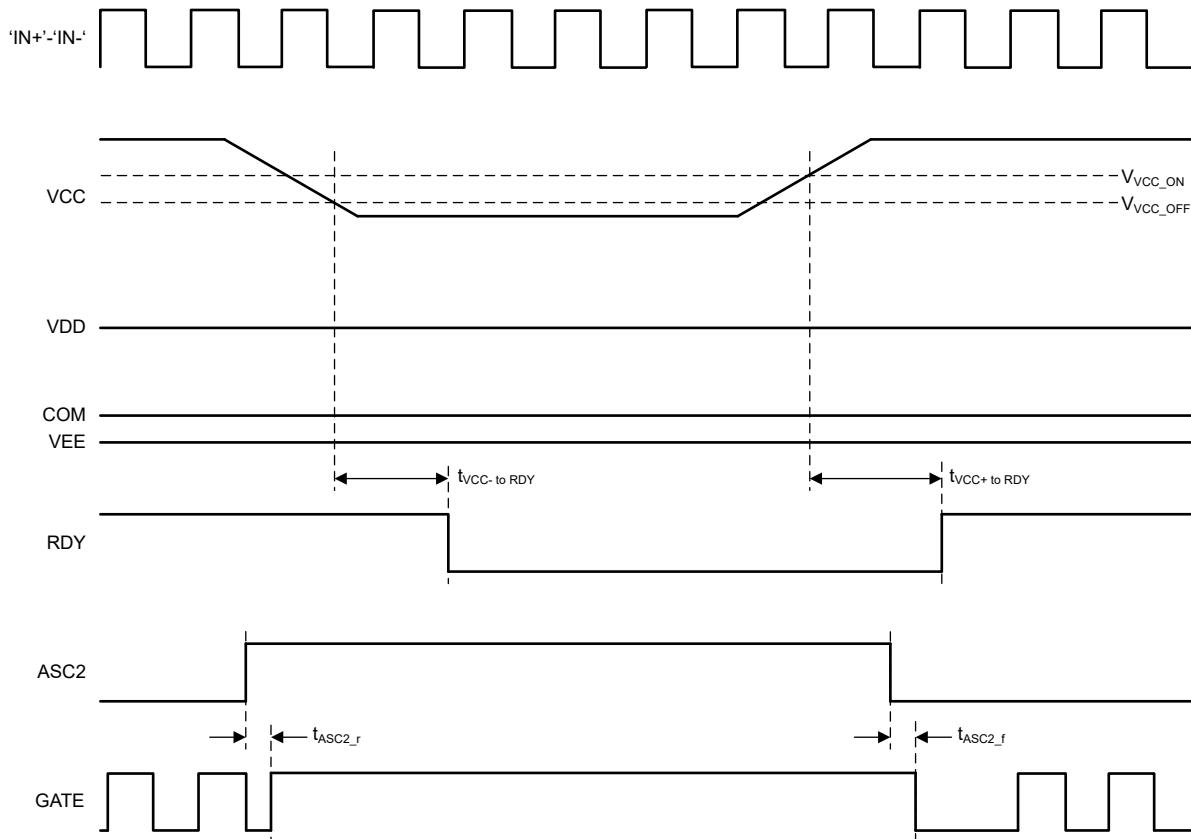


Figure 6-14. ASC2 Support with VCC UVLO

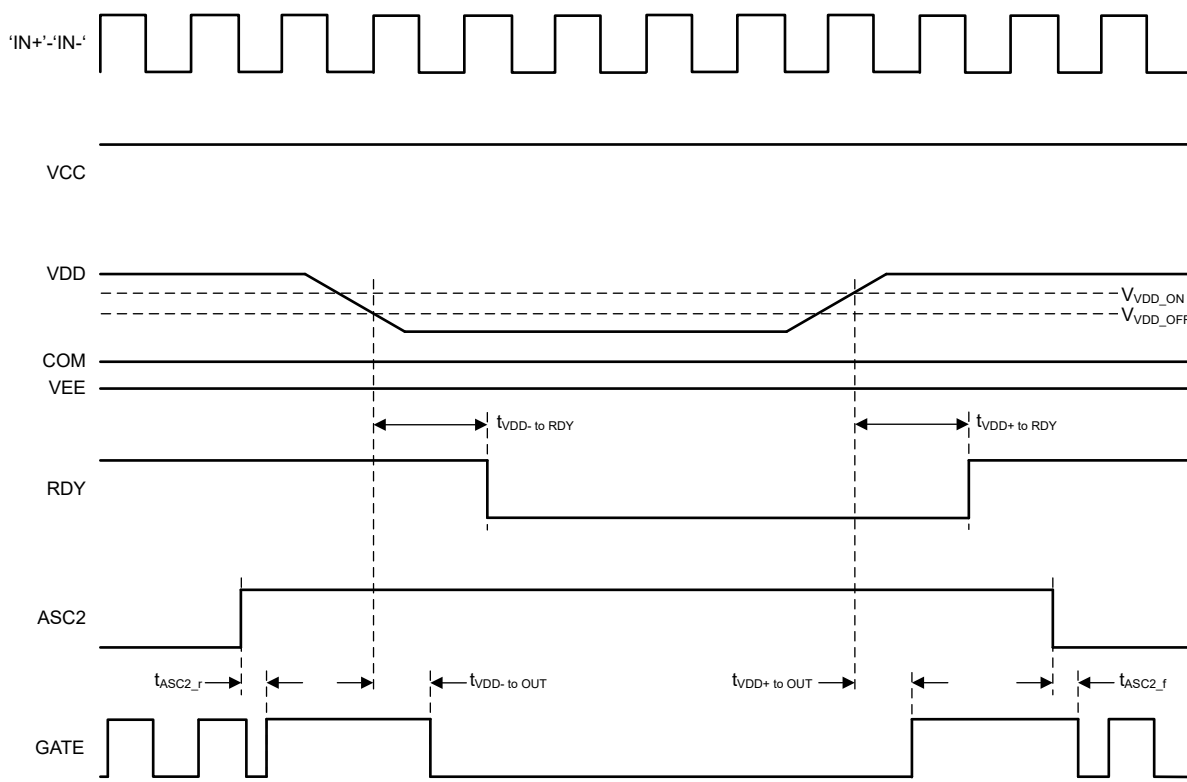


Figure 6-15. ASC2 Support with VDD UVLO

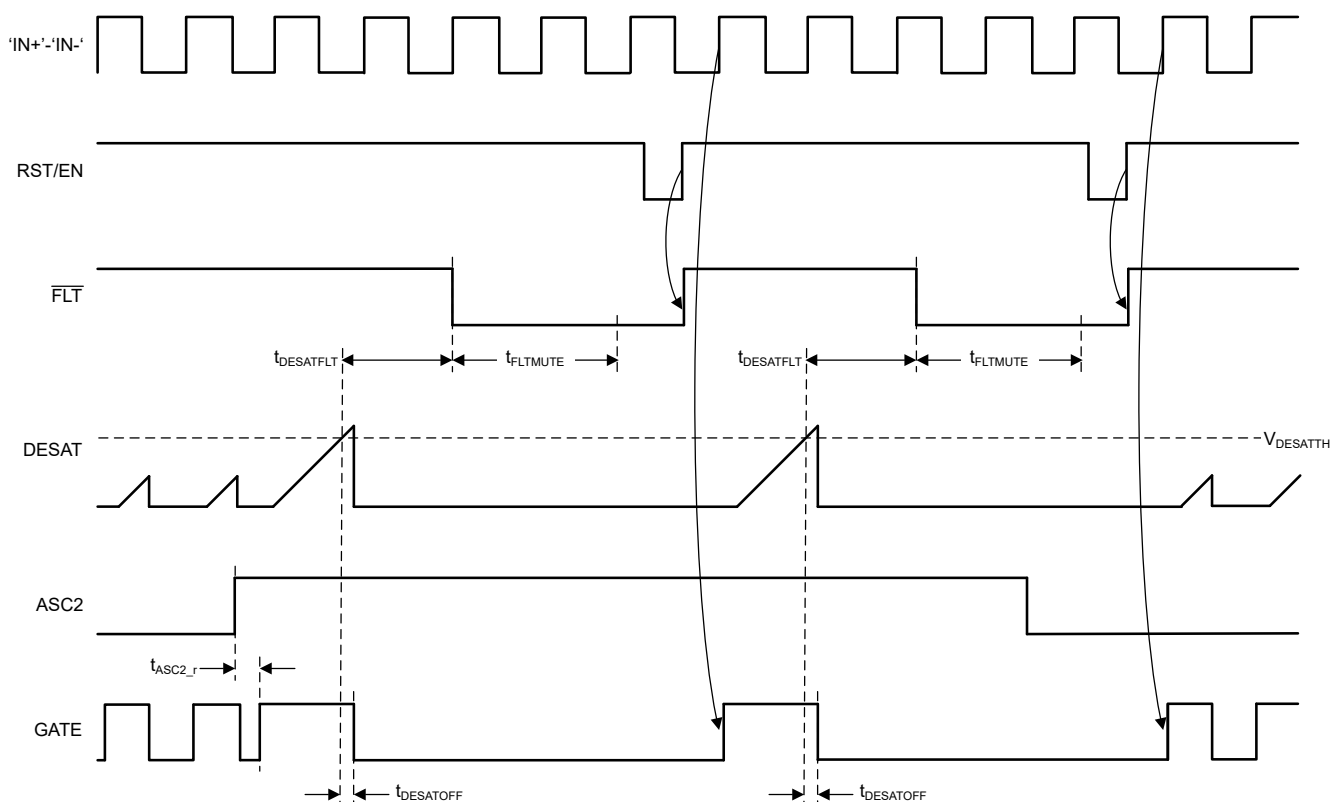


Figure 6-16. ASC2 Support with DESAT Fault

6.3.12 Overtemperature Protection

The silicon junction temperature is monitored to protect the driver IC from damage during overheating conditions. When the device temperature exceeds the thermal shutdown rising threshold, T_{TSDTH} , the driver output is turned off. The driver output holds the output off until the temperature recovers to $T_{TSDHYST}$ below the thermal shutdown rising threshold. While the driver is in thermal shutdown, the RDY pin on the input side is held low and connected to GND.

6.4 Device Functional Modes

[Table 6-2](#) lists the device functional modes in steady-state. For transient behavior including detection of faults see the [Feature Description](#).

Table 6-2. Function Table

SUPPLIES ⁽¹⁾			INPUTS				OUTPUTS				NOTE
VCC	VDD	VEE	IN+	IN-	RST/EN	ASC2	RDY	FLT	OUTHx/ OUTLx	CLMPI	
PD	PU	PU	X	X	X	L	L	Hi-Z	L	L	Supply UVLO
PU	PD	PU	X	X	X	X	L	Hi-Z	L	L	
PU	Open	PU	X	X	X	X	L	Hi-Z	L	Hi-Z	Supply open
PU	PU	Open	X	X	X	X	L	Hi-Z	L	L	
PU	PU	PU	X	X	L	L	Hi-Z	Hi-Z	L	L	Disabled
PU	PU	PU	L	X	H	L	Hi-Z	Hi-Z	L	L	Input controlled
PU	PU	PU	H	H	H	L	Hi-Z	Hi-Z	L	L	
PU	PU	PU	H	L	H	L	Hi-Z	Hi-Z	H	Hi-Z	
PU	PU	PU	X	X	X	L	Hi-Z	Hi-Z	H	Hi-Z	ASC
X	PU	PU	X	X	X	H	X	X	H	Hi-Z	
PU	PU	PU	X	X	X	X	L	Hi-Z	L	L	Overtemperature fault
PU	PU	PU	X	X	X	X	Hi-Z	L	L	L	DESAT fault (after SSD and before RST)

(1) PU: Power Up (Supply greater than UVLO threshold); PD: Power Down (Supply less than UVLO threshold); X: Irrelevant; H = High; L = Low; Hi-Z: High Impedance

7 Applications and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The device is very versatile because of the adjustable strong drive strength, wide range of output power supply, high isolation ratings, high CMTI and quality protection and sensing features. The 1.061kV_{RMS} working voltage and 10kV_{PK} surge immunity can support up both SiC MOSFET and IGBT modules with DC bus voltage up to 1500V. Use the device in both low-power and high-power applications, such as

- Traction inverter in HEV/EV
- On-board charger and charging pile
- Motor driver
- Solar inverter
- Industrial power supplies

The device can drive high-power SiC MOSFET module, IGBT module or paralleled discrete device directly. The input side can support power supply and microcontroller signal from 3.3V to 5V, and the device level shifts the signal to output side through reinforced isolation barrier. The device has wide output power supply range from 13V to 30V and supports wide range of negative power supply. As a result, use the driver in SiC MOSFET applications, IGBT application, and many others. The 12V VDD UVLO benefits the power semiconductor with lower conduction loss and improves the system efficiency. As a reinforced isolated single channel driver, the device can be used to drive either a low-side or a high-side switch.

The device features extensive protection and monitoring features, which can monitor, report and protect the system from various fault conditions.

- Fast detection and protection for the overcurrent and short-circuit fault. The semiconductor is shut down when the fault is detected and $\overline{\text{FLT}}$ pin pulls down to indicate the fault detection. The device latches unless receiving a reset signal from the $\overline{\text{RST/EN}}$ pin.
- Soft turn-off feature on the dedicated shutdown pin controllable by the SSD resistor, to protect the power semiconductor from catastrophic breakdown during overcurrent and short circuit fault. The shut-down energy is controllable while the overshoot of the power semiconductor is limited.
- UVLO detection to protect the semiconductor from excessive conduction loss. Once the device is detected to be in UVLO mode, the output pulls down and RDY pin indicates the power supply is lost. The device is back to normal operation mode once the power supply is out of the UVLO status. Monitor the power good status from the RDY pin.
- The active Internal Miller clamp feature protects the power semiconductor from false turn on due to miller capacitance with 4A internal pull down strength.
- Active short circuit (ASC) can force the output signal high to create an active short circuit loop between the phases
- Output voltage gate monitor with real-time output state feedback on OUT_FB
- Enable and disable function through the $\overline{\text{RST/EN}}$ pin
- Short circuit clamping
- Active pulldown

7.2 Typical Application

Figure 7-1 shows the typical application of three half-bridges using six isolated gate drivers. The half-bridge is a basic element in various power electronics applications such as traction inverter in HEV/EV to convert the DC current of the battery of the electric vehicle to the AC current to drive the electric motor in the propulsion system. Use the topology in motor drive applications to control the operating speed and torque of the AC motors.

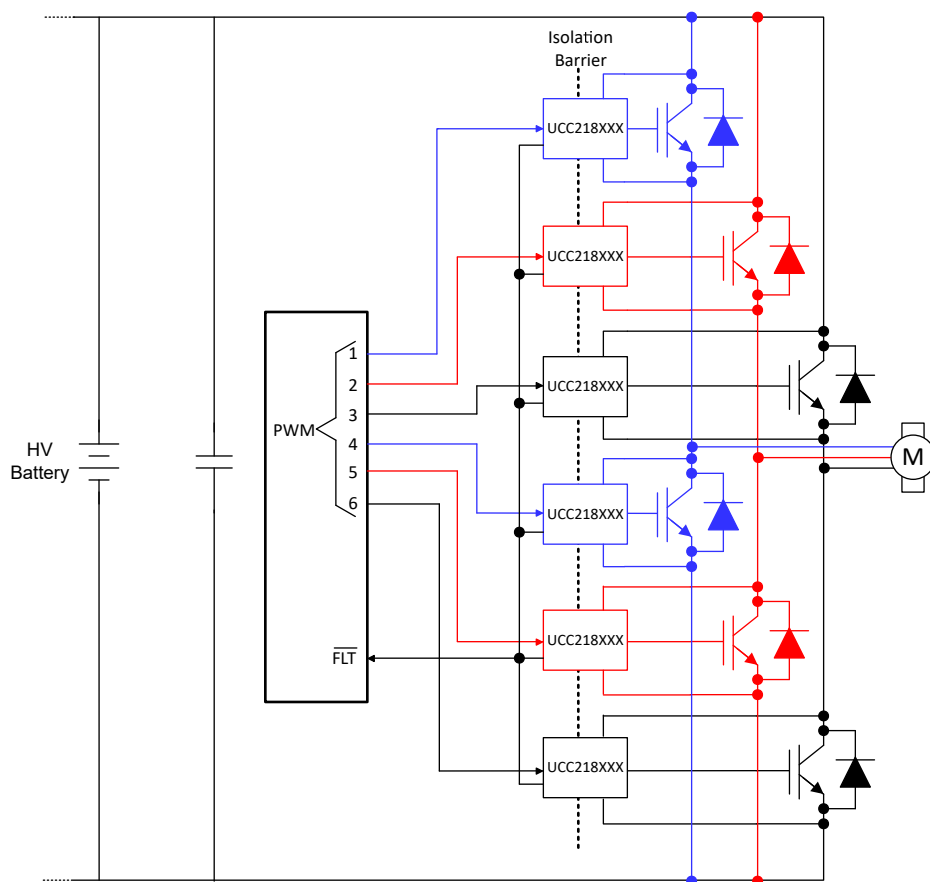


Figure 7-1. Typical Application Schematic in a Three Half-bridge Motor Drive System

7.2.1 Application Schematic

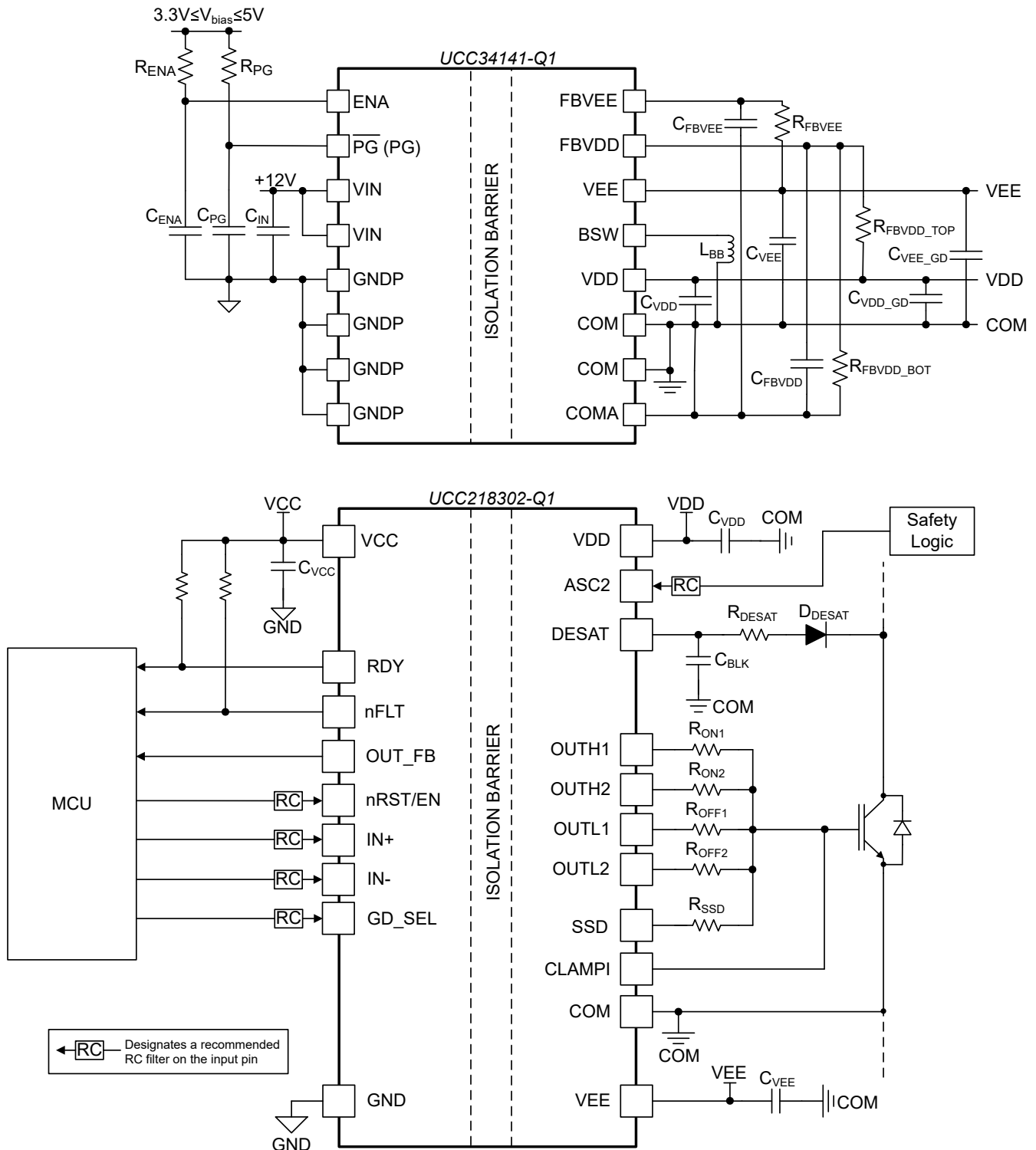


Figure 7-2. Typical Application Circuit

7.2.2 Design Requirements

The design of the power system for end equipment must consider some design requirements to support the reliable operation of the device through the load range. The design considerations include the peak source and sink current, power dissipation, short-circuit protection, fault feedback, and so forth.

This subsection include a design example based on IGBTs. The design parameters are show in [Table 7-1](#).

Table 7-1. Design Parameters

PARAMETER	VALUE
VCC	5V
Inputs	Non-inverting
VDD	15V
VEE	-5V
Switching Frequency	30kHz
Switch Type	IGBT Module

7.2.3 Detailed Design Procedure

7.2.3.1 Input Filters for IN+, IN-, and RST/EN

The input pins to the UCC218302-Q1 are both 3.3V and 5V logic compatible. The IN+ and $\overline{\text{RST/EN}}$ pins have internal pulldown resistors, and the IN- pin has an internal pullup resistor. If any of these pins are left floating, the driver is disabled unless active short circuit is activated. The driver has both inverting and non-inverting PWM input pins. If using only the non-inverting IN+ input, tie IN- to GND. If using only the inverting IN- input, tie IN+ to VCC. Both IN+ and IN- are useable for PWM interlocking with the other driver in a half-bridge configuration to prevent phase leg shoot-through.

The device features internal deglitch filters on the IN+, IN-, and $\overline{\text{RST/EN}}$ pins to protect against unintentional switching due to noise transients or narrow PWM pulses. Any signal less than t_{INFIL} is filtered out and not passed through. For noisy systems, add external low-pass filters externally to the input pins to further increase noise immunity. When selecting low-pass filter components, consider both noise immunity and delay time, according to system requirements. [Figure 7-3](#) shows the impact of the deglitch filters with narrow pulses on IN+, IN-, and $\overline{\text{RST/EN}}$.

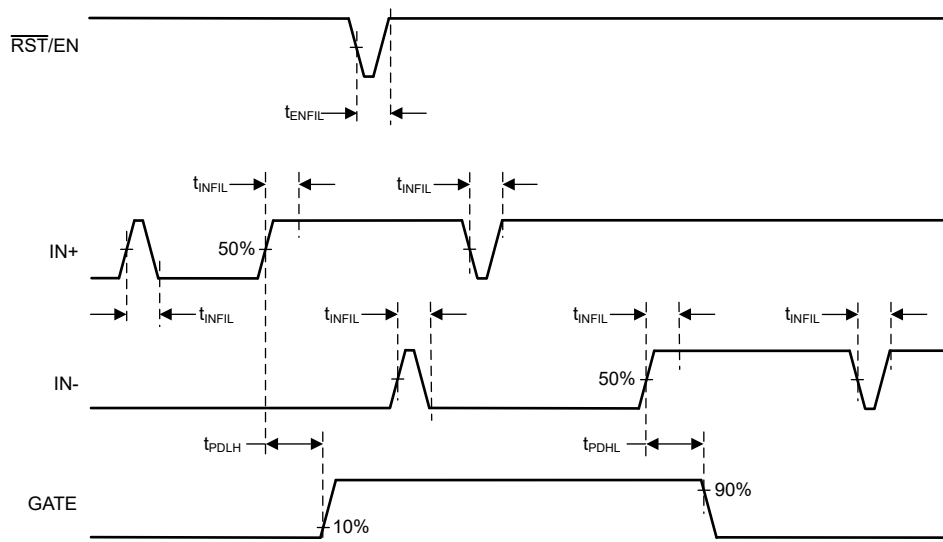


Figure 7-3. Impact of Deglitch Filters

7.2.3.2 $\overline{\text{FLT}}$, RDY, and $\overline{\text{RST/EN}}$ Pin Circuitry

The $\overline{\text{FLT}}$ and RDY pins are open-drain outputs. Typically, use a 5k Ω resistor as pullup resistor for the $\overline{\text{FLT}}$, RDY, and $\overline{\text{RST/EN}}$ pins.

To improve the noise immunity due to the parasitic coupling and common mode noise, add low-pass filters between the $\overline{\text{FLT}}$, RDY, $\overline{\text{RST/EN}}$ pins, and the microcontroller, respectively. Typically, add a filter capacitor from 100pF to 300pF.

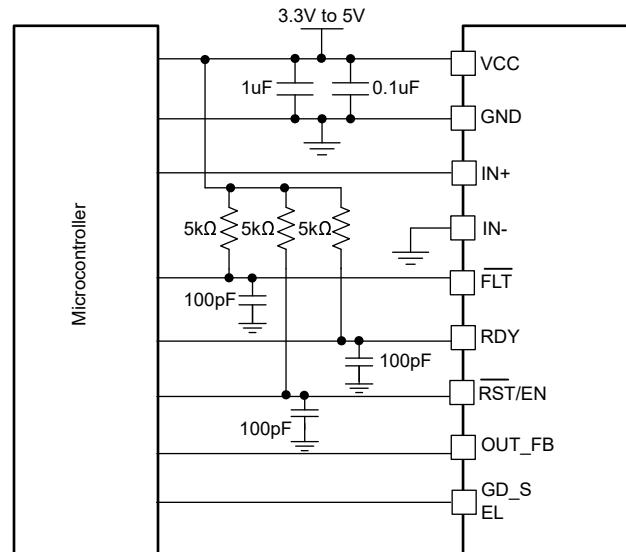


Figure 7-4. $\overline{\text{FLT}}$ Pin, RDY Pin and $\overline{\text{RST/EN}}$ Pin Circuitry

7.2.3.3 Gate Driver Output Resistors

The device features dual split outputs OUTH1, OUTH2, OUTL1 and OUTL2, which enables the independent control of the turn-on and turn-off switching speeds. The turn-on and turn-off resistances determine the peak source and sink current, which control the switching speed. Meanwhile, consider the power dissipation in the gate driver to establish the device is in the thermal limit. OUTH1 and OUTL1 can source and sink $\pm 5\text{A}$ peak current. OUTH2 and OUTL2 can source and sink $\pm 10\text{A}$ peak current. At first, calculate the peak source and sink current as:

$$I_{\text{Source_Pk_OUTH1}} = \min[5\text{A}, (V_{\text{DD}} - V_{\text{EE}}) / (R_{\text{OUTH1}} + R_{\text{ON1}} + R_{\text{G_Int}})] \quad (1)$$

$$I_{\text{Sink_Pk_OUTL1}} = \min[5\text{A}, (V_{\text{DD}} - V_{\text{EE}}) / (R_{\text{OUTL1}} + R_{\text{OFF1}} + R_{\text{G_Int}})] \quad (2)$$

$$I_{\text{Sink_Pk_OUTH2}} = \min[10\text{A}, (V_{\text{DD}} - V_{\text{EE}}) / (R_{\text{OUTH2}} + R_{\text{ON2}} + R_{\text{G_Int}})] \quad (3)$$

$$I_{\text{Sink_Pk_OUTL2}} = \min[10\text{A}, (V_{\text{DD}} - V_{\text{EE}}) / (R_{\text{OUTL2}} + R_{\text{OFF2}} + R_{\text{G_Int}})] \quad (4)$$

Where

- R_{OUTH1} is the internal pullup resistance of OUTH1
- R_{OUTH2} is the internal pullup resistance of OUTH2
- R_{OUTL1} is the internal pulldown resistance of OUTL1
- R_{OUTL2} is the internal pulldown resistance of OUTL2
- R_{ON1} is the external turn on gate resistance of OUTH1
- R_{ON2} is the external turn on gate resistance of OUTH2
- R_{OFF1} is the external turn off gate resistance of OUTL1
- R_{OFF2} is the external turn off gate resistance of OUTL2
- $R_{\text{G_Int}}$ is the internal resistance of the SiC MOSFET or IGBT module

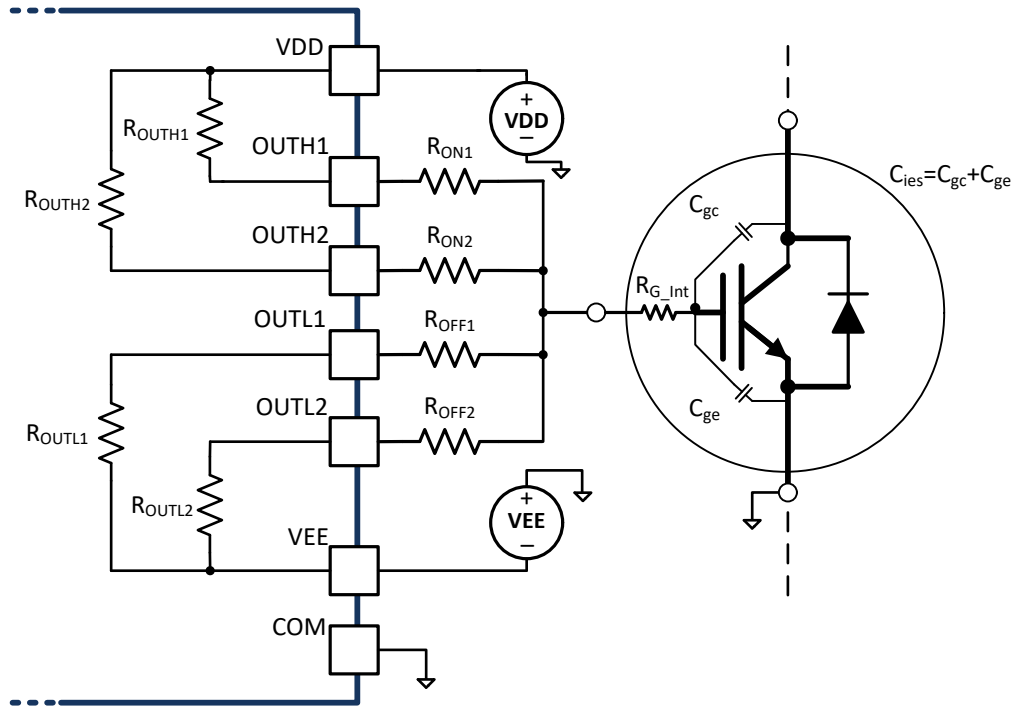


Figure 7-5. Output Model for Calculating Peak Gate Current

The following example of calculation, uses the maximum values for the internal pullup and pulldown resistances. See also [Electrical Characteristics](#) for more information. For an IGBT module based system with the following parameters:

- $Q_g = 3300\text{nC}$
- $R_{G_Int} = 1.7\Omega$
- $R_{ON1} = R_{OFF1} = 1.0\Omega$
- $R_{ON2} = R_{OFF2} = 0.5\Omega$
- $VDD = 15\text{V}$
- $VEE = -5\text{V}$

The peak source and sink current in this case are:

$$I_{\text{Source_Pk_OUTH1}} = (VDD - VEE) / (R_{\text{OUTH1}} + R_{\text{ON1}} + R_{G_Int}) = 5\text{A} \quad (5)$$

$$I_{\text{Sink_Pk_OUTL1}} = (VDD - VEE) / (R_{\text{OUTL1}} + R_{\text{OFF1}} + R_{G_Int}) = 5\text{A} \quad (6)$$

$$I_{\text{Source_Pk_OUTH2}} = (VDD - VEE) / (R_{\text{OUTH2}} + R_{\text{ON2}} + R_{G_Int}) = 6.7\text{A} \quad (7)$$

$$I_{\text{Sink_Pk_OUTL2}} = (VDD - VEE) / (R_{\text{OUTL2}} + R_{\text{OFF2}} + R_{G_Int}) = 6.7\text{A} \quad (8)$$

Using 1Ω external gate resistance, the peak source/sink current on OUT1 is 4A, the peak source/sink current on OUT2 is 6.7A. By setting the GD_SEL pin low or high, the device can provide a weak drive strength using only OUT1, or a strong drive strength using both OUT1 and OUT2. The weak and strong drive currents in this case are:

$$I_{\text{Source_Pk_Weak}} = I_{\text{Source_Pk_OUTH1}} = 5\text{A} \quad (9)$$

$$I_{\text{Sink_Pk_Weak}} = I_{\text{Sink_Pk_OUTL1}} = 5\text{A} \quad (10)$$

$$I_{\text{Source_Pk_Strong}} = I_{\text{Source_Pk_OUTH1}} + I_{\text{Source_Pk_OUTH2}} = 11.7\text{A} \quad (11)$$

$$I_{\text{Sink_Pk_Strong}} = I_{\text{Sink_Pk_OUTL1}} + I_{\text{Sink_Pk_OUTL2}} = 11.7\text{A} \quad (12)$$

The gate current at the Miller plateau voltage dominates the collector-to-emitter dV/dt during the turn-on switching transient. The pullup structure verifies the peak source current at the Miller plateau voltage, unless the turn-on gate resistor is too high. The faster the collector-to-emitter, V_{ce} , voltage rises to V_{DC} , the smaller the turn-on switching loss. Estimate the dV/dt as $Q_{gc}/I_{\text{source_pk}}$. For the turn-off switching transient, unless the turn-off gate resistor is too high, the load current dominates the drain-to-source dV/dt . After V_{ce} reaches the DC bus voltage, the power semiconductor is in saturation mode and V_{ge} controls the channel current. The peak sink current determines the dI/dt , which dominates the V_{ce} voltage overshoot accordingly. If using relatively large turn-off gate resistance and weak drive selection, limit the V_{ce} overshoot. Estimate the overshoot using:

$$\Delta V_{ce} = L_{\text{stray}} \times I_{\text{load}} / \left[(R_{\text{OFF1}} + R_{\text{OUTL1}} + R_{G_Int}) \times C_{ies} \times \ln(V_{\text{plat}} / V_{th}) \right] \quad (13)$$

Where

- L_{stray} is the stray inductance in power switching loop, as shown in [Figure 7-6](#)
- I_{load} is the load current, which is the turn off current of the power semiconductor
- C_{ies} is the input capacitance of the power semiconductor
- V_{plat} is the plateau voltage of the power semiconductor
- V_{th} is the threshold voltage of the power semiconductor


$$P_{DR} = P_Q + P_{SW} \quad (14)$$
$$P_{SWOUTx1} = \frac{1}{2} \times \left(\frac{R_{OUTH1}}{R_{OUTH1} + R_{ON1} + R_{G_Int}} + \frac{R_{OUTL1}}{R_{OUTL1} + R_{OFF1} + R_{G_Int}} \right) \times (V_{DD} - V_{EE}) \times f_{sw} \times \frac{1}{3} \times Q_g \quad (15)$$

$$P_{SWOUTx2} = \frac{1}{2} \times \left(\frac{R_{OUTH2}}{R_{OUTH1} + R_{ON2} + R_{G_Int}} + \frac{R_{OUTL2}}{R_{OUTL2} + R_{OFF2} + R_{G_Int}} \right) \times (VDD - VEE) \times f_{sw} \times \frac{2}{3} \times Q_g \quad (16)$$

Where

- Q_g is the gate charge required at the operation point to fully charge the gate voltage from VEE to VDD
- f_{sw} is the switching frequency (30kHz)

In this example, by selecting the strong drive, calculate the P_{SW} as:

$$P_{SW} = P_{SWOUTx1} + P_{SWOUTx2} = 0.14 + 0.34 = 0.48W \quad (17)$$

Thus, the total power loss is:

$$P_{DR} = P_Q + P_{SW} = 0.14W + 0.56W = 0.70W \quad (18)$$

When the board temperature is 120°C, estimate the junction temperature as:

$$T_j = T_b + \Psi_{JB} \times P_{DR} \approx 150^\circ C \quad (19)$$

Therefore, for the application in this example, with 120°C board temperature, the maximum switching frequency is approximately 30kHz to keep the gate driver in the thermal limit. By using a lower switching frequency or increasing external gate resistance, operate the gate driver at a higher board temperature.

7.2.3.4 Overcurrent and Short Circuit Protection With DESAT

Apply a standard desaturation circuit to the DESAT pin. If the voltage of the DESAT pin is higher than the threshold V_{DESAT} , the soft shutdown initiates. A fault is reported to the input side to DSP/MCU. The output is held to LOW after detecting the fault, and can only be reset by the $\overline{RST}/EN$ pin. The state-of-art overcurrent and short circuit detection time helps to maintain a short shutdown time for SiC MOSFET and IGBT.

If DESAT pin is not in use, tie the pin to COM to avoid overcurrent fault false triggering.

- Fast reverse recovery high voltage diode is recommended in the desaturation circuit. A resistor is recommended in series with the high voltage diode to limit the inrush current.
- A Schottky diode is recommended from COM to DESAT to prevent driver damage caused by negative voltage.
- A Zener diode is recommended from COM to DESAT to prevent driver damage caused by positive voltage.

7.2.4 Application Curves

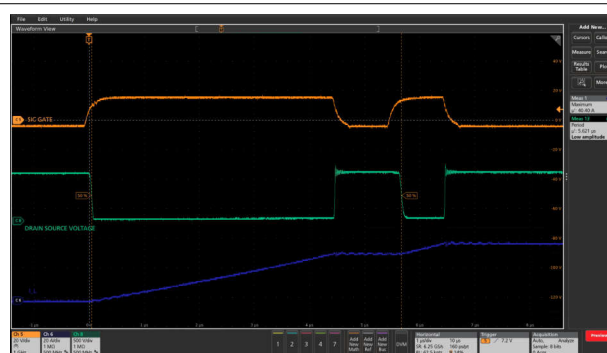


Figure 7-7. Double Pulse Test Example Waveform

7.3 Power Supply Recommendations

During the turn-on and turn-off switching transient, the VDD and VEE power supply provide the peak source and sink current. The large peak current is possible to drain the VDD and VEE voltage level and cause a voltage droop on the power supplies. To stabilize the power supply and maintain a reliable operation, a set of decoupling capacitors are recommended at the power supply pins. Considering the device has $\pm 15A$ peak drive strength and can generate high dV/dt , a 10 μF bypass cap is recommended between VDD and COM as well

as VEE and COM. A 1 μ F bypass cap is recommended between VCC and GND due to less current comparing with output side power supplies. A 0.1 μ F decoupling cap is also recommended for each power supply to filter out high-frequency noise. The decoupling capacitors must be low ESR and ESL to avoid high-frequency noise. Place the decoupling capacitors as close as possible to the VCC, VDD and VEE pins to prevent noise coupling from the system parasitics of PCB layout.

7.4 Layout

7.4.1 Layout Guidelines

To minimize noise in the gate path, take careful consideration into the PCB design. Below are some key points:

- Place the driver as close as possible to the power semiconductor to reduce the parasitic inductance of the gate loop on the PCB traces
- Place the decoupling capacitors of the input and output power supplies as close as possible to the power supply pins. The peak current generated at each switching transient can cause high di/dt and voltage spike on the parasitic inductance of PCB traces
- Connect the driver COM pin to the Kelvin connection the IGBT emitter or SiC MOSFET source. If the power device does not have a split Kelvin source or emitter, connect the COM pin as close as possible to the source or emitter terminal of the power device package to separate the gate loop from the high power switching loop
- Use a ground plane on the input side to shield the input signals. The high-frequency noise the output side switching transients generates can distort the input signals. The ground plane provides a low-inductance filter for the return current flow
- If using the gate driver for the low side switch which the COM pin connects to the DC bus negative, use the ground plane on the output side to shield the output signals from the noise the switch node generates. If using the gate driver for the high side switch, in which the COM pin connects to the switch node, ground plane is not recommended
- If ground plane is not used on the output side, separate the return path of the DESAT ground loop from the gate ground loop which has large peak source and sink current of 15A
- Pay attention to any copper or PCB traces routed underneath the gate driver to make sure the isolation integrity, especially creepage and clearance, is maintained. Any traces under the gate driver must have the corresponding ground plane extended to shield the traces.

7.4.2 Layout Example

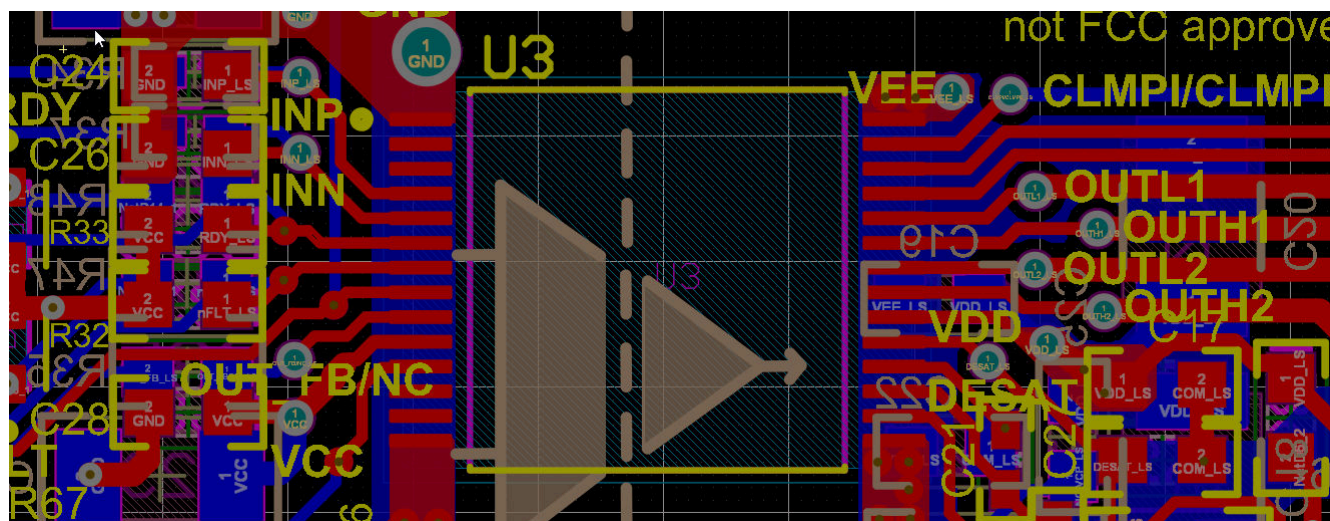


Figure 7-8. Layout Example

8 Device and Documentation Support

8.1 Third-Party Products Disclaimer

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8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following:

- [Isolation Glossary](#)

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

[TI Glossary](#)

This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

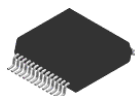
DATE	REVISION	NOTES
September 2026	*	Advance Information Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

10.1 Mechanical Data

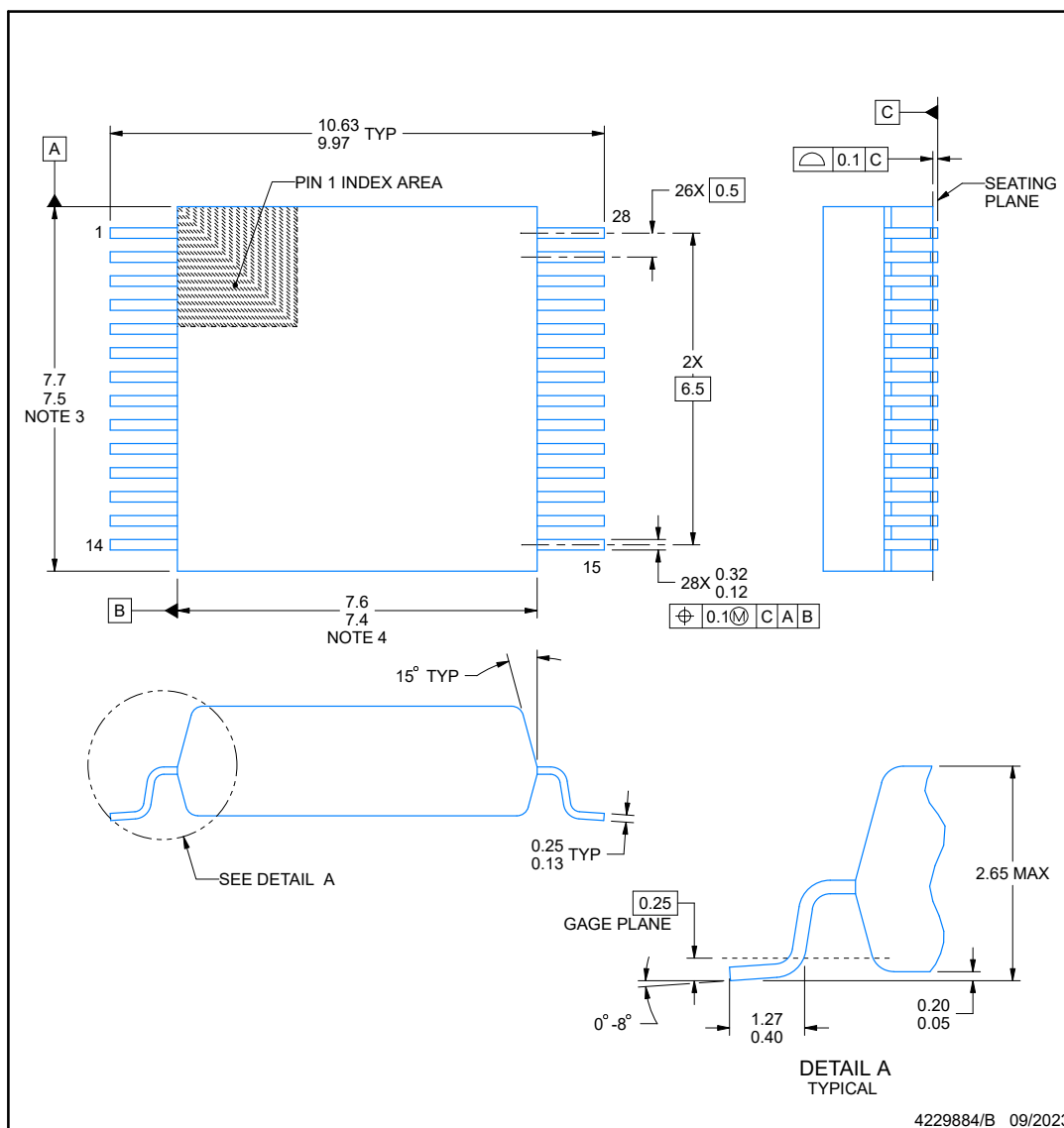
DFP0028A



PACKAGE OUTLINE

SSOP - 2.65 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.

SSOP - 2.65 mm max height

28X (0.3)

1

28X (1.3)

SYMM

(R0.05) TYP

28

26X (0.5)

SYMM

14

15

(9.6)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK OPENING

METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK OPENING

EXPOSED METAL

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4229884/B 09/2024

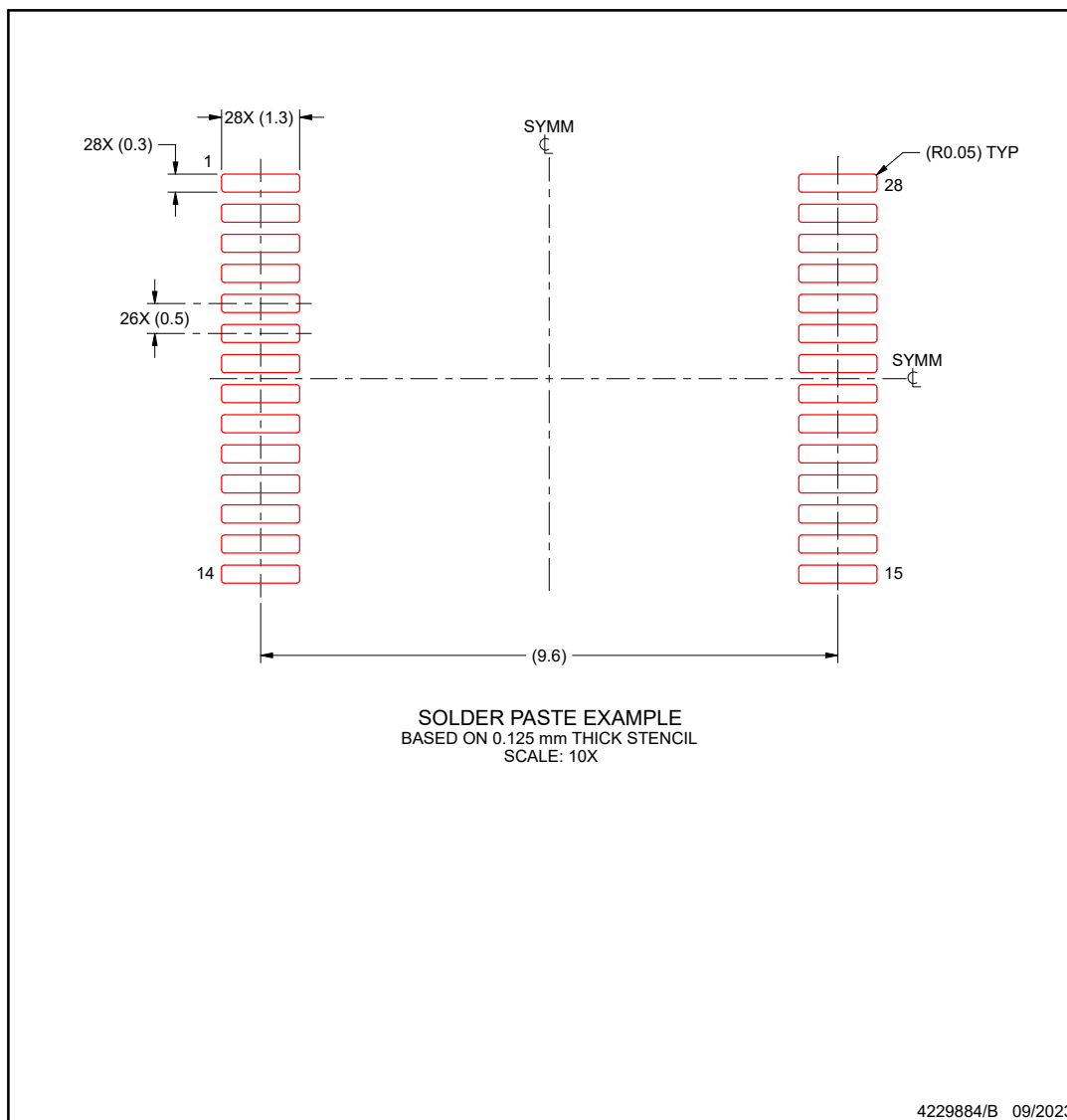
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DFP0028A

SSOP - 2.65 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC218302BQDFPRQ1	Active	Production	SSOP (DFP) 28	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	U218302BQ

- (1) **Status:** For more details on status, see our [product life cycle](#).
- (2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- (3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- (4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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