UCC25661x Family 750kHz Wide V_{IN}/V_{OUT} Range LLC Controller Optimized for Light-Load Efficiency

1 Features

- Full-load switching frequency: 50kHz to 750kHz
- Input Power Proportional Control (IPPC) for wide LLC
- Enhanced light load management (standby power and audible noise):
  - High frequency and audible frequency pulse skip
  - Low frequency burst (all except UCC256616)
  - Integrated PFC on/off (UCC256614)
  - Soft in and out of burst mode (UCC256610)
- Internal resonant-capacitor voltage synthesizer for signal reliability and high-frequency start-up
- Zero current switching (ZCS) avoidance to eliminate capacitive region operation
- Adaptive soft start with minimized inrush current and eliminating reverse recovery at start-up
- Integrated gate drive: +0.6/-1.2A
- Integrated high-voltage start-up (UCC25661x family except UCC256613)
- X-capacitor discharge (UCC256610, UCC256611, UCC256614)
- Extended Gain Range (UCC256610 and UCC256614)
- 50ns overcurrent protection (OCP), cycle-by-cycle current limit
- Overvoltage protection (OVP), OVP latch (UCC256611, UCC256616
- Internal and external OTP
- Input and VCCP UVLO with internal 19V VCCP Clamp
- Independently configured OCP and overload protection (OLP/OPP) (UCC25661x family except UCC256616)
- SOIC-14 package with removed pins for high-voltage clearance

2 Applications

- SMPS power supply for TV
- Industrial AC/DC adapters
- Power tools
- Medical power supply
- Multifunctional printer
- Enterprise and cinema projector
- PC power supply
- Gaming console power supply
- Lighting

3 Description

The UCC25661x family is a high-frequency LLC controller implementing input-power proportional control (IPPC) scheme, along with enhanced light-load management and multiple protection features. IPPC widens the control range of the LLC converter and simplifies the design of wide input or output-voltage range applications such as LED drivers and battery chargers. IPPC works without a PFC for non-universal input applications.

The UCC25661x family has enhanced light-load management that improves the efficiency while minimizing audible noise. To minimize standby power, the UCC25661x family directly disables the PFC controller when operating in burst mode.

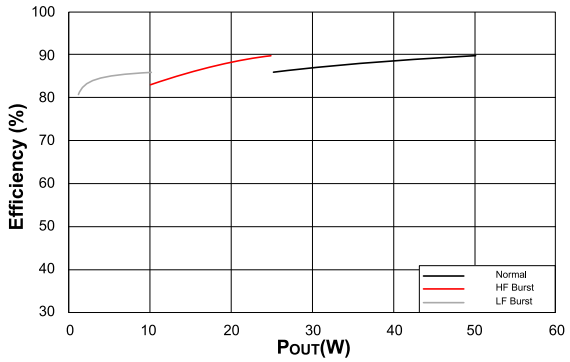
The automatic capacitive region avoidance scheme along with the adaptive soft start with reverse recovery avoidance scheme verifies that the device never works in a mode where there is a potential to damage the FETs. The automatic capacitive region avoidance scheme makes the controller appropriate for working with a prebiased load.

The UCC25661x family comes with robust protection to help users design a reliable power supply. The UCC25661x family has options supporting high-voltage start-up, X-capacitor (X-cap) discharge, OVP, and extended gain range (EGR). See details in the Device Comparison table.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
UCC25661x family	DDB (SOIC, 16)	9.9mm × 3.9mm

(1) For all available packages, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Efficiency Curve

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4 Device Comparison Table

FEATURE	UCC256610	UCC256611	UCC256612	UCC256613	UCC256614	UCC256616
Integrated high voltage start-up	●	●	●		●	●
Integrated X-capacitor discharge	●	●			●	
Extended gain range (EGR)	●				●	
Output - voltage (OVP) latch		●				●
Burst Mode Retention	●					
Soft on/off burst mode	●					
OCP/OLP decoupling	●	●	●	●	●	
PFC on/off during LF Burst					●	
OLP detection time	100ms	100ms	100ms	100ms	100ms	100ms

5 Pin Configuration and Functions

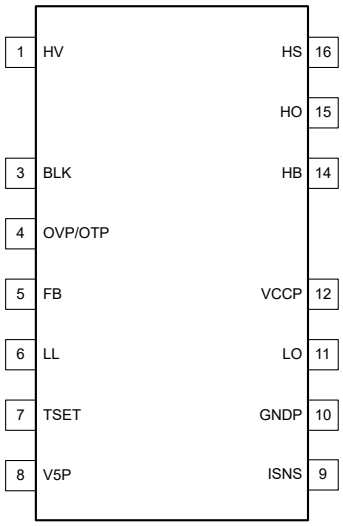

Figure 5-1. DDB Package, 16-Pin SOIC; Pins 2 and 13 Removed (Top View)

Table 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
	2	—	Missing. HV spacer for creepage between high voltage and low voltage pins
	13	N/A	Missing pin. High-voltage spacer for creepage between high-voltage and low-voltage pins.
BLK	3	I	Bulk DC voltage sensing and input for feedforward control. Connect BLK through a resistor divider between positive terminal of bulk capacitor and GNDP to set the LLC converter start and stop voltage thresholds. See Section 7.3.5.1 for more details.
FB	5	I	Feedback control input. Connect FB to the collector pin of an optocoupler in the isolated feedback network. See Section 7.3.3 for more details.
GNDP	10	P	Ground reference pin. Connect GNDP to primary-side bulk capacitor negative terminal.
HB	14	P	High-side gate driver bias input. Connect a capacitor (minimum of 0.1µF, maximum of 5µF) between HB and HS pins. See Section 8.3.2 for more details.
HO	15	O	High-side switch gate driver output. Connect to high-side switch gate terminal with a minimal gate drive circuit loop area.
HS	16	P	High-side gate driver return path and switching node connection input. Connect to the switching node of the half-bridge structure of the LLC converter. The voltage at this pin used to determine the adaptive dead time. See Section 7.3.4 for more details.
HV	1	I	High-voltage (HV) start-up and X-capacitor discharge. The HV pin is used to perform HV start-up. After start-up is completed, the HV pin is used for AC presence detection and X-capacitor discharge. This pin is connected to the rectified AC line (UCC256610, UCC256611, UCC256614 , UCC256616) or input bulk capacitor (UCC256612 and UCC256613).

Table 5-1. Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
ISNS	9	I	Resonant Circuit Current Sense Input. Connect ISNS pin to resonant capacitor through a series differentiator capacitor and a current sense resistor to GNDP. This pin senses the differentiated resonant capacitor voltage. This signal is internally used to: • Generate the control signal • OCP and cycle-by-cycle current limiting • Capacitive region avoidance See Section 8.2.2.17 for more details.
LL	6	I	Light load operation and burst mode threshold setting input. Connect LL to the center node of resistor divider between V5P an GNDP. The impedance and voltage at LL pin is used to select the thresholds for high frequency and low frequency burst mode operation. See Section 7.5.3 for more details.
LO	11	O	Low-side switch gate driver output. Connect to low-side switch gate terminal with a minimal gate drive circuit loop area.
OVP/OTP	4	I	Overvoltage protection and external over-temperature protection input. Connect OVP/OTP to GNDP through an NTC resistor and to VCCP through zener diode. See Section 7.3.5.3 for more details.
TSET	7	I/O	VCR synthesizer time constants setting input and PFC on/off output (UCC256614). TSET is used to set the minimum VCR time constants and the minimum switching frequency in IPPC mode by using a resistor divider as defined in Section 8.2.2.18. It also dual functions at the PFC disable pin with the UCC256614and as an input to enforce low-frequency burst mode with the UCC256610. See Section 8.2.2.18 for details.
V5P	8	P	5V Internal Regulator Output. Connect a decoupling capacitor (recommend 1uF to 4.7uF) from V5P to GNDP. Place this capacitor close to the V5P. Chose the dielectric based on application need.
VCCP	12	P	IC supply voltage pin. Connect a low-ESR ceramic 2.2µF decoupling capacitor between VCCP and GNDP. A parallel combination of energy storage electrolytic and filter capacitors are typically used in addition. For applications including an auxiliary bias winding on the LLC transformer, the VCCP pin is connected through a diode to the bias winding. For applications where HV start-up is disabled, VCCP is supplied by an auxiliary bias supply. VCCP pin is internally clamped to 19V.

(1) I = input, O = output, P = power, I/O = bidirectional, N/A = not applicable

Refer to Section 8.2 for more details.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted), all voltages are with respect to GND, currents are positive into and negative out of the specified terminal.(1)

		MIN	MAX	UNIT
Input voltage	HV, HB	-0.3	700	V
	ISNS	-6.5	6.5	V
	BLK, LL, TSET	-0.55	5.5	V
	HB - HS	-0.3	25	V
	VCCP	-0.55	30	V
	OVP/OTP	-0.55	5.5	V
5V	DC	-0.55	5.5	V
HO output voltage	DC	HS – 0.3	HB + 0.3	V
	Transient, less than 100 ns	HS – 2	HB + 0.3	
LO output voltage	DC	-0.3	VCCP+ 0.3	V
	Transient, less than 100 ns	-2	VCCP + 0.3	
Floating ground slew rate	dV_{HS}/dt	-200	200	V/ns
HO, LO pulsed current	I_{OUT_PULSED}	-0.6	1.2	A
Junction temperature range	T_J	-40	150	°C
Storage temperature range, T_{stg}	T_{stg}	-65	150	
Lead temperature	Soldering, 10 second		300	
	Reflow		260	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, HV, HO, HS, HB pins(1)	±1000	V
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all other pins(1)	±2000	
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

All voltages are with respect to GND, -40°C < T_J = T_A < 125°C, currents are positive into and negative out of the specified terminal, unless otherwise noted.

		MIN	NOM	MAX	UNIT
HV, HS	Input voltage			640	V
V_{VCCP}	Supply voltage		15	18.5	V
HB - HS	Driver bootstrap voltage	10	14	17.5	V
C_B	Ceramic bypass capacitor from HB to HS	0.1		5	µF
C_{VCCP}	VCCP pin decoupling capacitor	33		470	µF
$I_{VCCPMAX}$	Maximum input current of VCCP			100	mA
T_A	Operating ambient temperature	-40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		UCC25661x D (SOIC) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	74.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	30.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	31.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	31.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

6.5 Electrical Characteristics

All voltages are with respect to GND, -40°C < T_J < 125°C, VCC = 15V, currents are positive into and negative out of the specified terminal, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
VCC_{Short}	Below this threshold, use reduced start up current		0.6	1	1.4	V
$VCC_{ReStartJfet}$	Below this threshold, re-enable JFET.			10.2		V
$VCC_{ReStart}$	HV startup is re-enabled when VCC is below this level during startup phase		12.5	13	13.5	V
$VCC_{StartSelf}$	Startup when VCC is above this level		13.5	14	14.5	V
$VCC_{StartExt}$	Startup when VCC is above this level		10.5	10.9	11.3	V
$VCC_{StopSwitching}$	Switching Stopped below this threshold		9	9.5		V
VCC_{UVLOr}	VCC undervoltage lockout voltage (rising)		7.25	7.5	7.82	V
VCC_{UVLOf}	VCC undervoltage lockout voltage hysteresis		6.5	6.8	7.1	V
VCC_{Hold_r}	Jfet Stop voltage during startup programming phase		7.9	8.2	8.5	V
VCC_{Hold_f}	Jfet Start voltage during startup programming phase		7.65	7.9	8.15	V
VCC_{Shunt}	VCC internal clamp voltage			19		V
$IVCC_{Clamp}$	VCC internal clamp current			15		mA
VCC_OV	VCC OVP threshold			20.5		V

6.5 Electrical Characteristics (continued)

All voltages are with respect to GND, -40°C < T_J < 125°C, VCC = 15V, currents are positive into and negative out of the specified terminal, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
$I_{CCSleep}$	Current drawn from VCC rail during burst off period			800		µA
I_{CCRun}	Current drawn from VCC Pin while gate is switching. Excluding Gate Current	Dead time = 1µs maximum dead time		8		mA
$I_{CCLatchFault}$	Current drawn from VCC pin in latched fault state(1)	Only applicable for UCC256611			1	mA
REGULATED SUPPLY						
V5P	Regulated supply voltage (1)	no load	4.75	5	5.25	V
	Regulated supply voltage	10mA load	4.75	5	5.25	V
$V5P_{UVLO}$	V5P undervoltage lock out voltage (1)			4		V
$I_{V5PStartupCurrLimit}$	Max current that can be drawn on the pin when VCCP< $VCC_{StartSelf}$ (1)	VCCP = 15V		6		mA
$I_{V5PCurrLimit}$	V5P at IV5P = 15mA	VCCP = 15V	10.2			mA
HIGH VOLTAGE STARTUP						
$I_{VCC\_Charge\_Low}$	Reduced VCCP charge current from HV Pin	V_{HV} = 20V, VCC = 0V, For UCC256610, UCC256611, UCC256612, UCC256614, UCC256616	0.23	0.44	0.65	mA
$I_{VCC\_Charge\_High}$	Full VCCP charge current	V_{HV} = 20V, VCC = 4V, For UCC256610, UCC256611, UCC256612, UCC256614,UCC256616	7.5	10	13.8	mA
I_{HVZCD}	Highest AC zero-crossing detection test current	UCC256610, UCC256611, UCC256614		0.625		mA
$I_{XCAPDischarge}$	X-cap discharge current	UCC256610, UCC256611, UCC256614	8.7	11.5	14.3	mA
$V_{zero\text{-}crossing}$	HV pin voltage threshold that zero-crossing is detected	UCC256610, UCC256611, UCC256614	8	9	11	V
$t_{XCAPZCD}$	AC zero-crossing detection window length for first four test current stage (1)	UCC256610, UCC256611, UCC256614	10	12	14	ms
$t_{XCAPZCDLast}$	AC zero-crossing detection window length for final test current stage (1)	UCC256610, UCC256611, UCC256614		36		ms
$t_{XCAPIdle}$	AC zero-crossing detection idle period length (1)	UCC256610, UCC256611, UCC256614		700		ms
$t_{XCAPDischarge}$	Time for X-cap discharge current active (1)	UCC256610, UCC256611, UCC256614	327	360	390	ms
$t_{XCAPJFETON}$	Time of first X-cap detection after JFETON (1)	UCC256610, UCC256611, UCC256614		12		ms
I_{XCAP_I0}	X-Cap test current I0	UCC256610, UCC256611, UCC256614		125		uA
I_{XCAP_Idel1}	X-Cap test current I1	UCC256610, UCC256611, UCC256614		125		uA
I_{XCAP_Idel1}	X-Cap test current I2	UCC256610, UCC256611, UCC256614		250		uA
I_{XCAP_Idel1}	X-Cap test current I3	UCC256610, UCC256611, UCC256614		375		uA
BULK VOLTAGE SENSE						
$V_{BLKStartHys}$	BLK voltage comparator hysteresis (1)	For UCC256610, UCC256614	0.04	0.05	0.06	V

6.5 Electrical Characteristics (continued)

All voltages are with respect to GND, -40°C < T_J < 125°C, VCC = 15V, currents are positive into and negative out of the specified terminal, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{BLKStartHys}$	BLK voltage comparator hysteresis (1)	For UCC256611, UCC256612, UCC256613,UCC256616	0.09	0.1	0.11	V
$V_{BLKStop}$	BLK voltage that forces LLC operation to stop		0.98	1	1.02	V
I_{BLKHys}	BLK hysteresis current (Bulk Brown Out Isink)	For UCC256610, UCC256614		1		µA
I_{BLKHys}	BLK hysteresis current (Bulk Brown Out Isink)	For UCC256611, UCC256612, UCC256613,UCC256616		5		µA
FEEDBACK PIN						
$R_{FBInternal}$	Internal pulldown resistor value	For UCC256610, UCC256611, UCC256614, UCC256616	85	100	115	kΩ
$R_{FBInternal}$	Internal pulldown resistor value	For UCC256612, UCC256613	42.5	50	57.5	kΩ
I_{FB}	FB internal current source	For UCC256610, UCC256611, UCC256614,UCC256616	68	80	92	µA
I_{FB}	FB internal current source	For UCC256612, UCC256613	136	160	184	µA
V_{FB}	FB pin voltage when FB pin sink current is at (I_{FB} - 50µA)	Iopto = 0.37 × IFB	3.3	3.5	3.7	V
ΔV_{FB}	FB pin voltage variation when FB pin sink current ranges from (Iopto = 0.37 × IFB to Iopto = 0.94 × IFB)				0.6	V
ΔV_{clamp}	FB pin voltage variation when FB pin sink current ranges from (Iopto = 0.94 × IFB) to (Iopto = 1.06 × IFB)	(Iopto = 0.94 × IFB) to (Iopto = 1.06 × IFB)	0.3			V
$I_{FBclamp}$	Maximum FB internal current source when FB is clamped	For UCC256610, UCC256611,UCC256616	75	87.5	100	µA
$I_{FBclamp}$	Maximum FB internal current source when FB is clamped	For UCC256612, UCC256613, UCC256614	150	175	200	µA
$\Delta V_{FBclamp}$	FB pin voltage variation when FB pin sink current ranges from (IIopto = 1.06IFB) to (IIopto = IFB + 0.94 × IFBClamp)	(IIopto = 1.06IFB) to (IIopto = IFB + 0.94 × IFBClamp)			0.5	V
f_{-3dB}	Feedback chain -3dB cutoff frequency (2)	VFBReplica from 4.5V to 0.5V	1			MHz
V_{FBOLP}	OLP protection(1)			4.75		V
$TOLP_{Fault}$	OLP protection time (1)			100		ms
RESONANT CURRENT SENSE						
V_{ISNS_OCP}	OCP threshold during steady state	For UCC25616, TSET option >2.5V (1)	3.9	4	4.1	V
V_{ISNS_OCP}	OCP threshold during steady state	For UCC256616, TSET option <2.5V	3.4	3.5	3.6	V
V_{ISNS_OCP}	OCP threshold during steady state	For UCC256610, UCC256611, UCC256612, UCC256613, UCC256614	3.4	3.5	3.6	V
$V_{ISNS\_OCP\_SS}$	OCP threshold during soft start		2.9	3	3.1	V
n_{OCP}	Number of OCP cycles before OCP fault is tripped (1)			7		
n_{OCP_SS}	Number of OCP cycles before OCP fault is tripped at startup(2)			50		
$V_{IpolarityHyst}$	ISNS Polarity comparator hystereses			40		mV
V_{ISNS_ZCS}	ZCS comparator +Ve threshold after Soft Start	For UCC256616		100		mV

6.5 Electrical Characteristics (continued)

All voltages are with respect to GND, -40°C < T_J < 125°C, VCC = 15V, currents are positive into and negative out of the specified terminal, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ISNS_ZCSn}	ZCS comparator -Ve threshold, after Soft Start	For UCC256616		-100		mV
V_{ISNS_ZCS}	ZCS comparator +Ve threshold after Soft Start	For UCC256610, UCC256611, UCC256612, UCC256613, UCC256614		150		mV
V_{ISNS_ZCSn}	ZCS comparator -Ve threshold, after Soft Start	For UCC256610, UCC256611, UCC256612, UCC256613, UCC256614		-150		mV
$V_{ISNS\_MINCURR\_SS}$	+Ve ISNS threshold during Soft Start			50		mV
$V_{ISNS\_MINCURR\_SSn}$	-Ve ISNS threshold during Soft Start			-50		mV
t_{leb}	Leading edge blanking for ZCS and OCP comparators(1)			250		nS
$TZCS_{Fault}$	Fault detected when ZCS event persists for the indicated time(2)	ZCS Event persists		10		mS
GATE DRIVER						
V_{LOL}	LO output low voltage	I_{sink} = 20mA			0.12	V
V_{RVCC} - V_{LOH}	LO output high voltage	I_{source} = 20mA			0.3	V
V_{HOL} - V_{HS}	HO output low voltage	I_{sink} = 20mA			0.12	V
V_{HB} - V_{HOH}	HO output high voltage	I_{source} = 20mA			0.35	V
$V_{HB-HSUVLOFall}$	High side gate driver UVLO falling threshold		6.4	7.25	8	V
$V_{HB-HSUVLOHys}$	High side gate driver UVLO threshold hysteresis		0.78	0.9	1.05	V
$I_{source\_pk\_HO}$	HO peak source current (2)	At VCCP = 12V		-0.6		A
$I_{source\_pk\_LO}$	LO peak source current (2)	At VCCP = 12V		-0.6		A
$I_{sink\_pk\_HO}$	HO peak sink current (2)	At VCCP = 12V		1.2		A
$I_{sink\_pk\_LO}$	LO peak sink current (2)	At VCCP = 12V		1.2		A
BOOTSTRAP						
$I_{BOOT\_QUIESCENT}$	(HB - HS) quiescent current	HB - HS = 12V		60	70	µA
I_{BOOT_LEAK}	HB to GND leakage current	V_{HB} = 600V		0.045	20	µA
$t_{ChargeBoot}$	Length of charge boot state(1)		230	265	300	µs
SOFT START						
SSRamp	Soft Start Ramp time(1)			25		ms
OVP/OTP						
Vclamp_otp1	Clamp Voltage at 0mA(1)	At 0mA current flowing through the clamp	1.35	1.5	1.65	V
Vclamp_otp2	Clamp Voltage at 1mA(1)	At 1mA current flowing through the clamp	2.9	3.5	4.1	V
I_{OTP}	Current source on the BW/OTP pin			100		uA
V_{OVPpos}	Output voltage OVP - Threshold rising			3.5		V
$VOTP_{Neg}$	OTP - Threshold falling			0.8		V
$OTP_{CompHys}$	OTP comparator hysteresis		60	90	130	mV
$OVP_{CompHys}$	OVP comparator hysteresis		60	100	145	mV
$OTPBlanking_{startup}$	OTP blanking time at startup			50		ms

6.5 Electrical Characteristics (continued)

All voltages are with respect to GND, -40°C < T_J < 125°C, VCC = 15V, currents are positive into and negative out of the specified terminal, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$TOTP_{Fault}$	OTP Fault detection time			330		uS
$TOVP_{Fault}$	OVP Fault detection time(2)			40		uS
TSET						
$I_{TSETPrgm}$	TSET pin sourcing current for programming			10		uA
LL						
I_{LLPrgm}	LL pin sourcing current for Burst mode transition threshold programming(2)			10		uA
t_{LLPrgm}	Burst mode transition threshold programming time(2)			2		ms
ADAPTIVE DEADTIME						
dV_{HS}/dt	Detectable slew rate (falling slope) (2)		0.1		200	V/ns
FAULT RECOVERY						
$t_{PauseTimeOut}$	Paused timer(1)			1		s
THERMAL SHUTDOWN						
T_{J_r}	Thermal shutdown temperature (1)	Temperature rising	125	150		°C
T_{J_H}	Thermal shutdown hysteresis (1)			20		°C

(1) Not tested in production. Established by characterization
(2) Not tested in production. Established by design

6.6 Switching Characteristics

All voltages are with respect to GND, -40°C< T_J =T_A < 125°C, VCC = 15V, currents are positive into and negative out of the specified terminal, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{r(LO)}$	Rise time	10% to 90%, 1nF load		30	60	ns
$t_{f(LO)}$	Fall time	10% to 90%, 1nF load		20	30	ns
$t_{r(HO)}$	Rise time	10% to 90%, 1nF load		30	60	ns
$t_{f(HO)}$	Fall time	10% to 90%, 1nF load		15	50	ns
$t_{DT(min)}$	Minimum dead time (1)			50		ns
$t_{DT(max)}$	Maximum dead time (dead time fault) (1)	ZCS threshold is NOT detected		1		µs
$t_{DT(max\_ZCS)}$	Maximum dead time (dead time fault) (1)	ZCS threshold is detected		1.1		µs
$t_{ON(min)}$	Minimum gate on time			250		ns
$t_{ON(max)}$	Maximum gate on time			10		µs
$t_{Ipol(ZCS)}$	Blanking time after which the IPOL signal can be used to terminate DT	ZCS threshold is detected		500		ns

(1) Not tested in production. Established by design

6.7 Typical Characteristics

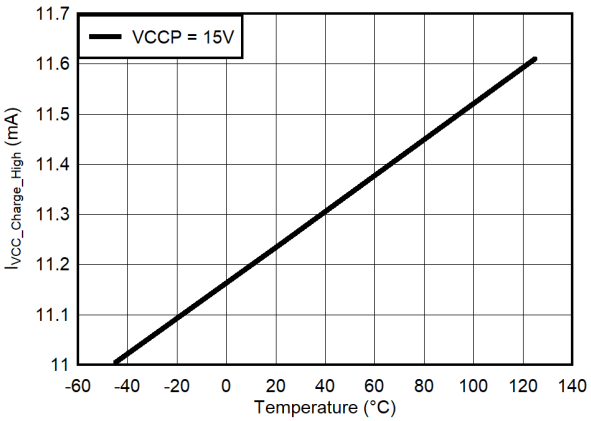

Figure 6-1. $I_{VCC\_Charge\_High}$ vs Temperature

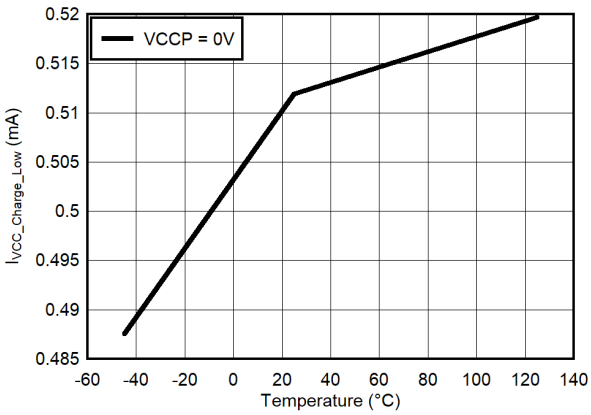

Figure 6-2. $I_{VCC\_Charge\_low}$ vs Temperature

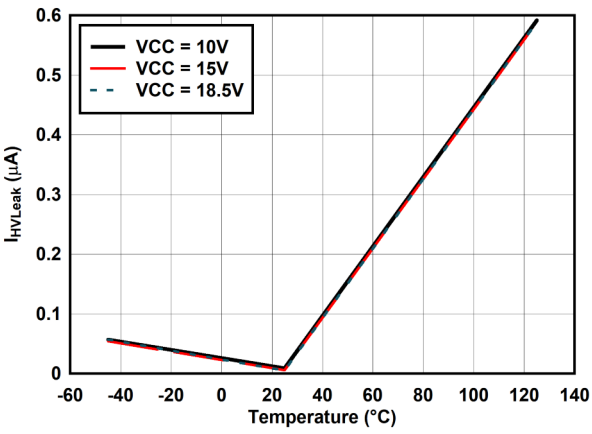

Figure 6-3. I_{HVLeak} vs Temperature

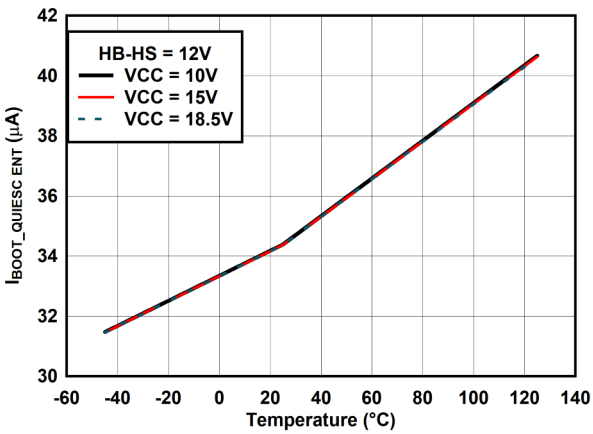

Figure 6-4. $I_{BOOT\_QUIESCENT}$ vs Temperature

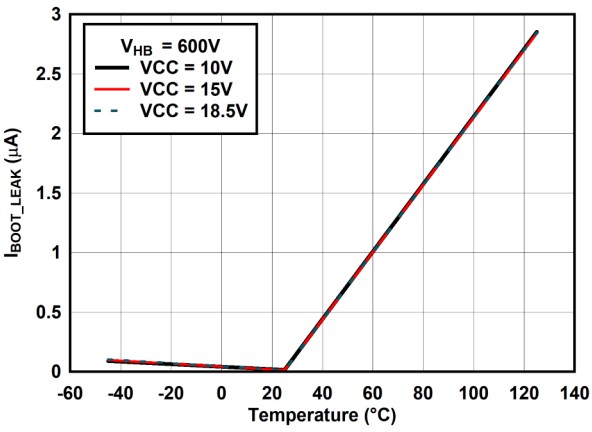

Figure 6-5. I_{BOOT_LEAK} vs Temperature

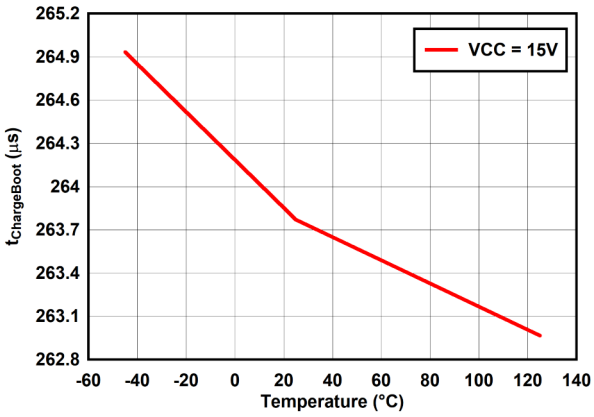

Figure 6-6. $t_{ChargeBoot}$ vs Temperature

6.7 Typical Characteristics (continued)

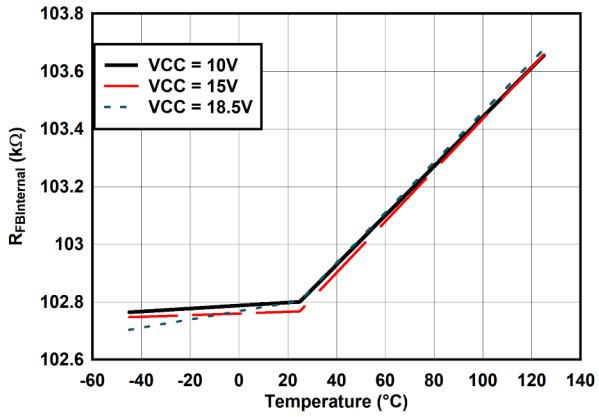

Figure 6-7. $R_{FBInternal}$ vs Temperature

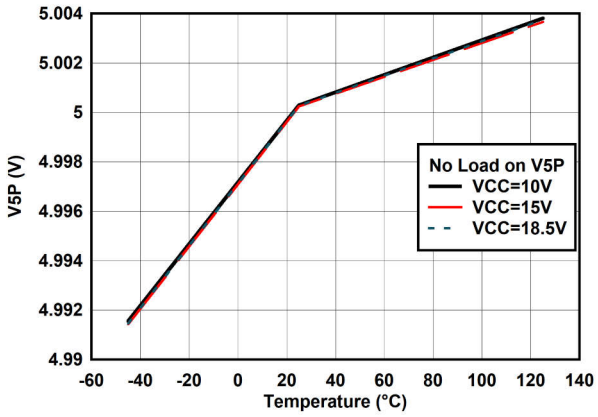

Figure 6-8. V5P (no load) vs Temperature

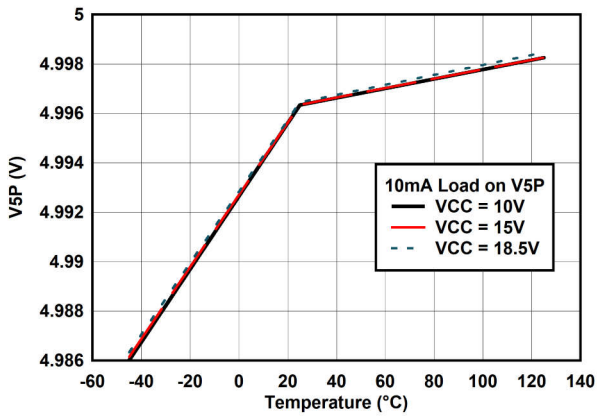

Figure 6-9. V5P (10mA Load)vs Temperature

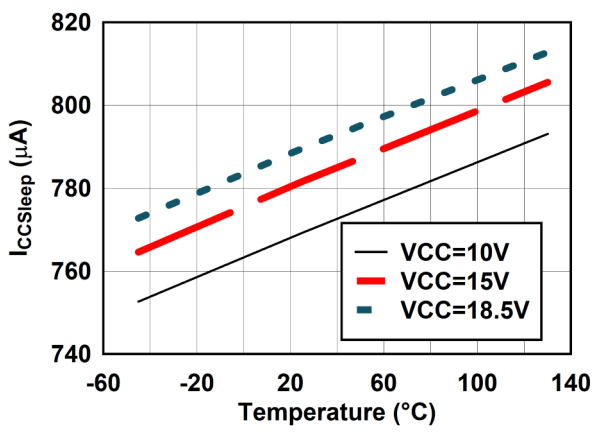

Figure 6-10. $I_{CCSleep}$ vs Temperature

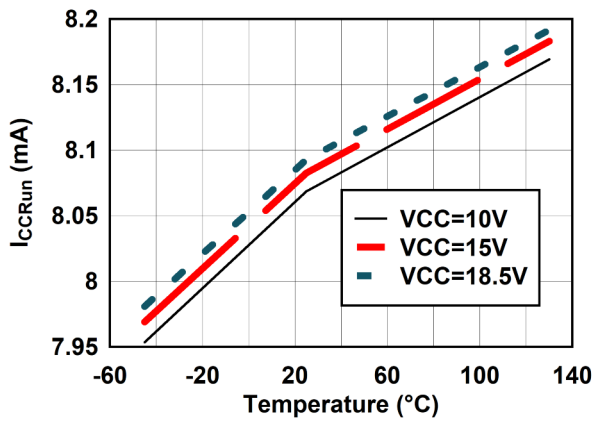

Figure 6-11. I_{CCRun} vs Temperature

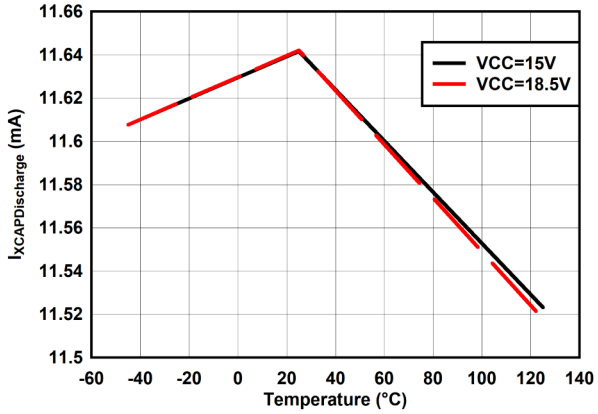

Figure 6-12. $I_{XCAPDischarge}$ vs Temperature

6.7 Typical Characteristics (continued)

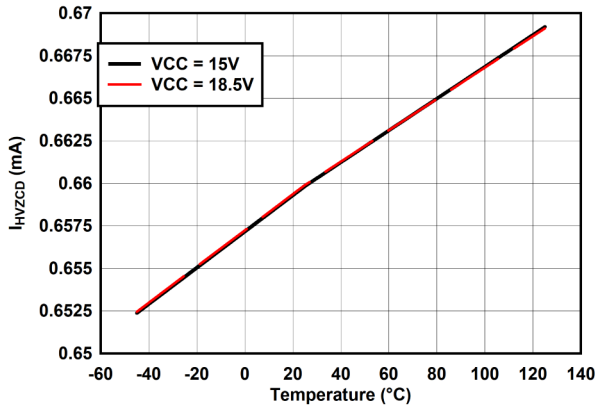

Figure 6-13. I_{HVZCD} vs Temperature

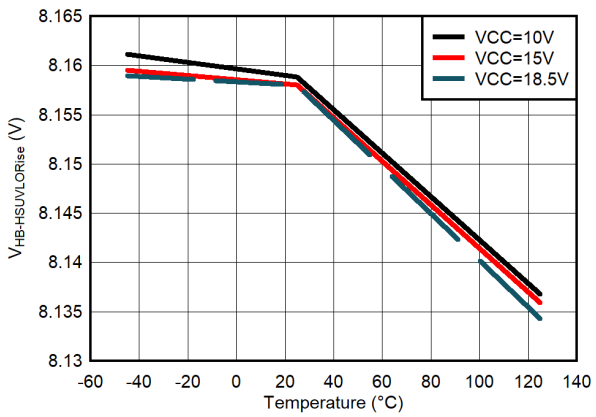

Figure 6-14. $V_{HB-HSUVLORise}$ vs Temperature

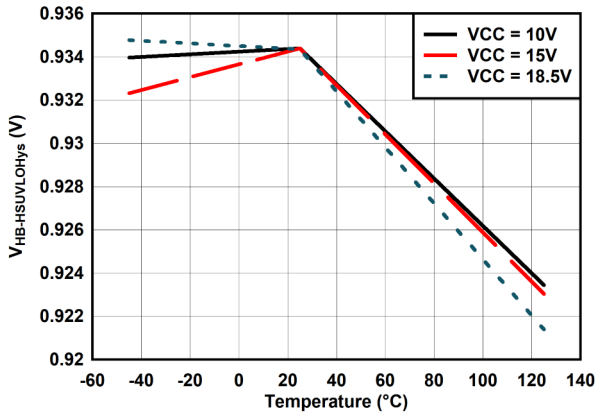

Figure 6-15. $I_{HB-HSUVLOHys}$ vs Temperature

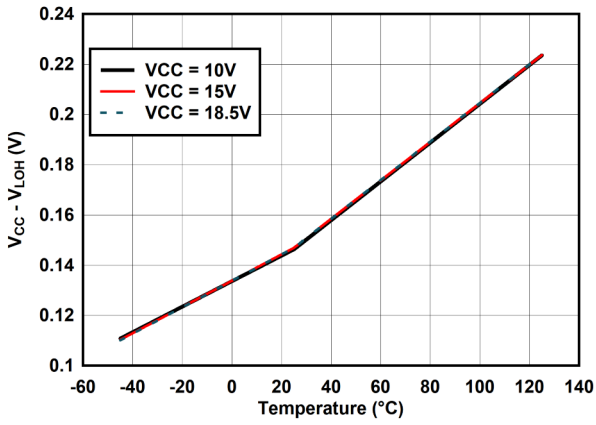

Figure 6-16. (V_{RVCC}- V_{LOH}) vs Temperature

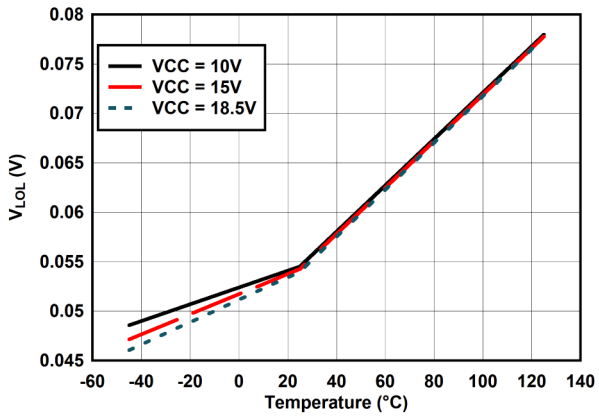

Figure 6-17. V_{LOL} vs Temperature

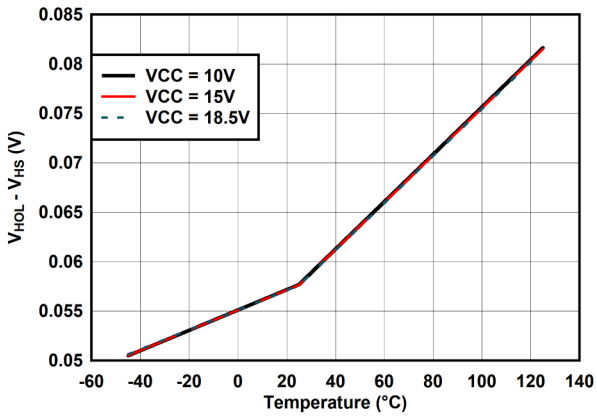

Figure 6-18. (V_{HOL}- V_{HS}) vs Temperature

6.7 Typical Characteristics (continued)

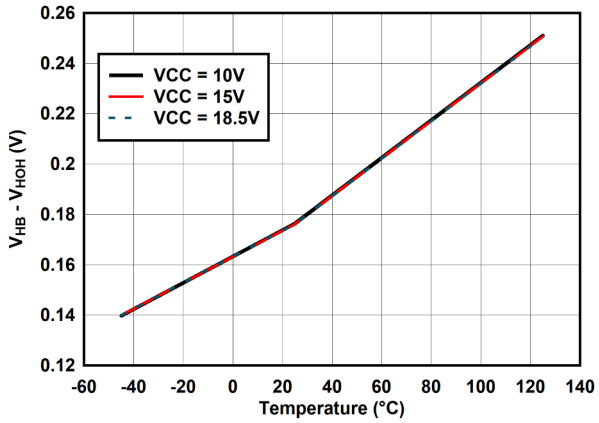

Figure 6-19. (V_{HB} - V_{HOH}) vs Temperature

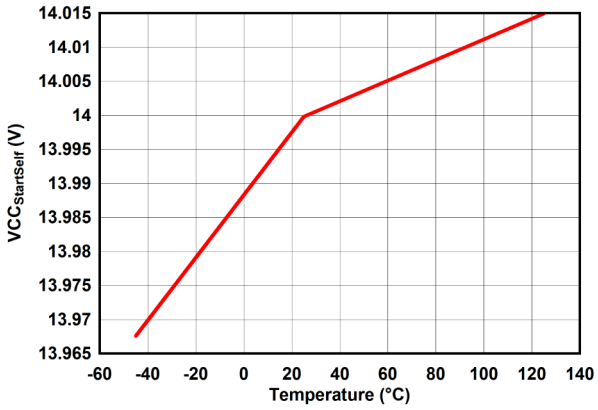

Figure 6-20. $VCC_{StartSelf}$ vs Temperature

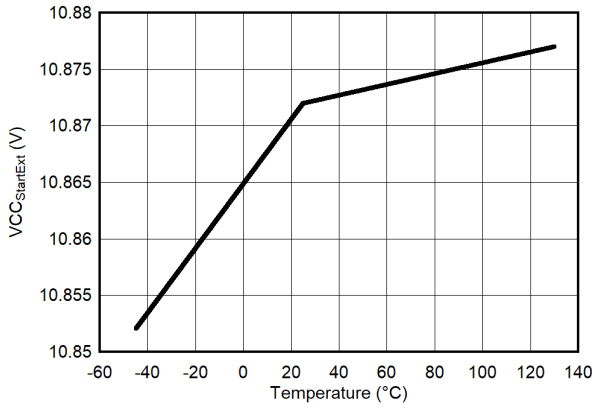

Figure 6-21. $VCC_{StartEXT}$ vs Temperature

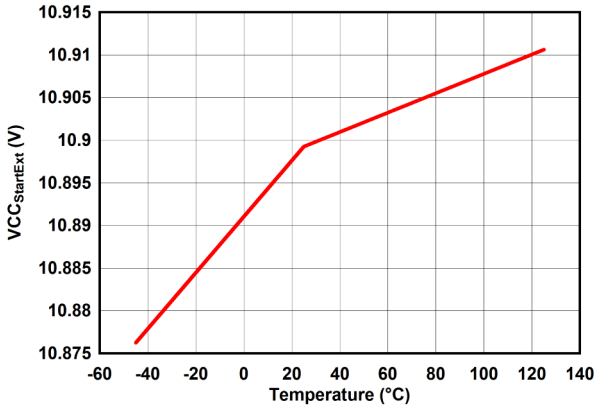

Figure 6-22. $VCC_{StartExt}$ vs Temperature

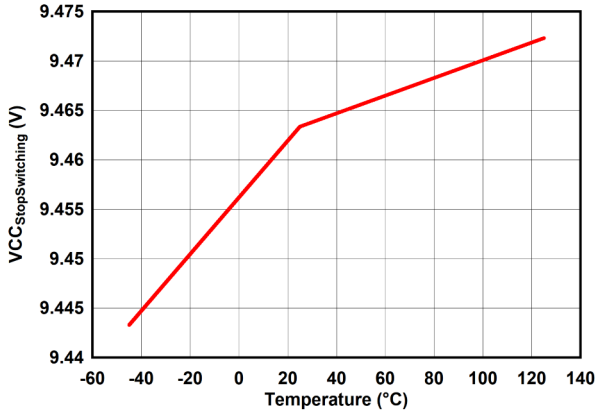

Figure 6-23. $VCC_{StopSwitching}$ vs Temperature

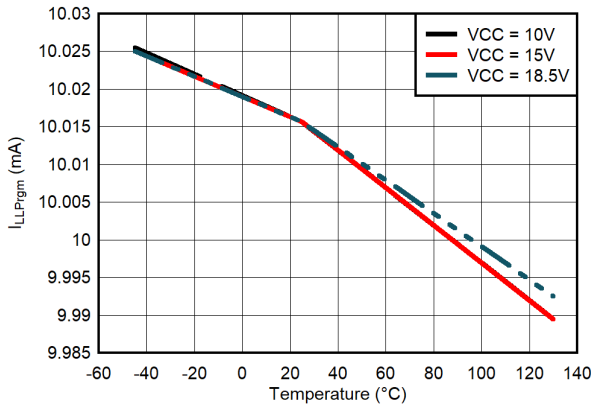

Figure 6-24. I_{LLPrgm} vs Temperature

7 Detailed Description

7.1 Overview

The UCC25661x family is a fully featured LLC resonant controller for isolated power supplies. UCC25661x family incorporates high levels of integration and several design features to accommodate wide input and output voltage operation, high power density, and increased reliability of the LLC power stage.

The device novel control scheme input power proportional control (IPPC) offers excellent transient performance inherent in the current mode controls, while enabling a linear relationship between input power and control signal across wide input and output voltage variation. The IPPC control enables consistent light load, burst mode performance operation across a wide input and output voltage variation.

Some of the new features in UCC25661x family are specified below:

- IPPC Control enables more stable burst mode and dynamic response under wide input/output voltage operation
- New operation modes to increase light load efficiency while reducing audible noise
  - High-frequency (HF) pulse skip for improved light load efficiency
  - Low-frequency (LF) burst mode for reduced stand by power consumption
  - Programmable light load/burst mode thresholds to balance output ripple and efficiency
  - Adaptive burst mode threshold adjustment to accommodate input voltage change
  - Wide burst mode hysteresis to prevent oscillating in and out of burst mode
  - Soft in and soft out of burst mode to further minimize audible noise plus option to force retention of burst mode
- Full-load switching frequency enables high power density designs: up to 750kHz
- Combined resonant current sensing with internal control voltage generation, improves control robustness
- Input voltage feed forward
- Benefits of Extended gain range (EGR) include:
  - Enable better support for wider input / output voltage range applications in addition to IPPC
  - Increases the minimum power that can be delivered across wide input voltage range for example when PFC is disabled
  - Helps to improve system efficiency at light loads by allowing PFC to be disabled while serving the load
- Integrated protections include:
  - Fast cycle-by-cycle current limiting: 50ns
  - OCP fault to protect under short circuit conditions
  - Over Power Protection (OPP) to limit peak input power
  - Zero Current Switching (ZCS) avoidance scheme to eliminate capacitive region operation
  - Adaptive soft start for reduced inrush current and eliminating reverse recovery at start-up
  - External OVP/OTP protection
  - Input and bias supply (VCCP) UVLO
  - Input voltage feed forward
  - OCP/OLP decoupling allows protection thresholds sets independently

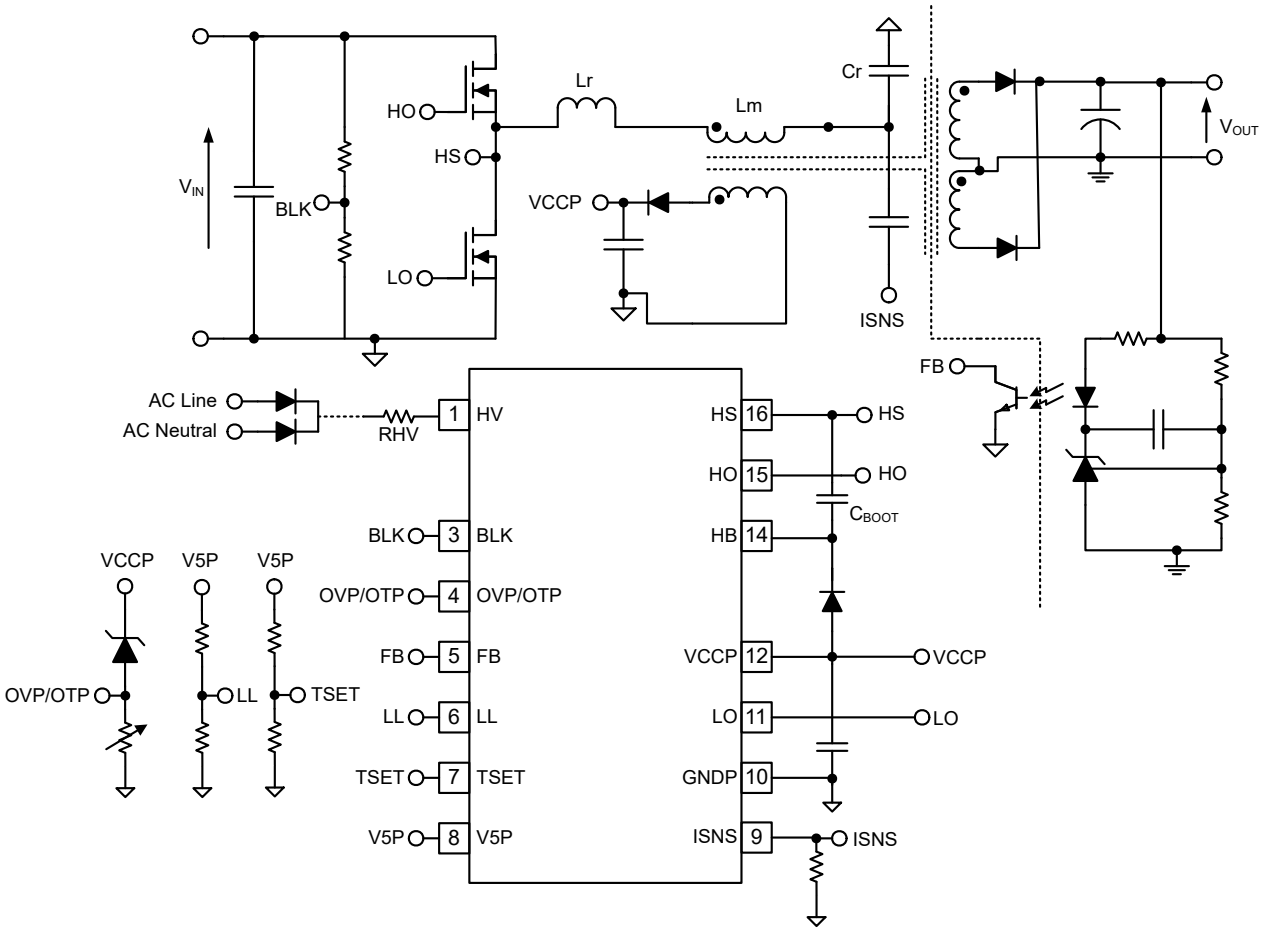

Figure 7-1. Simplified Application Schematic

7.2 Functional Block Diagram

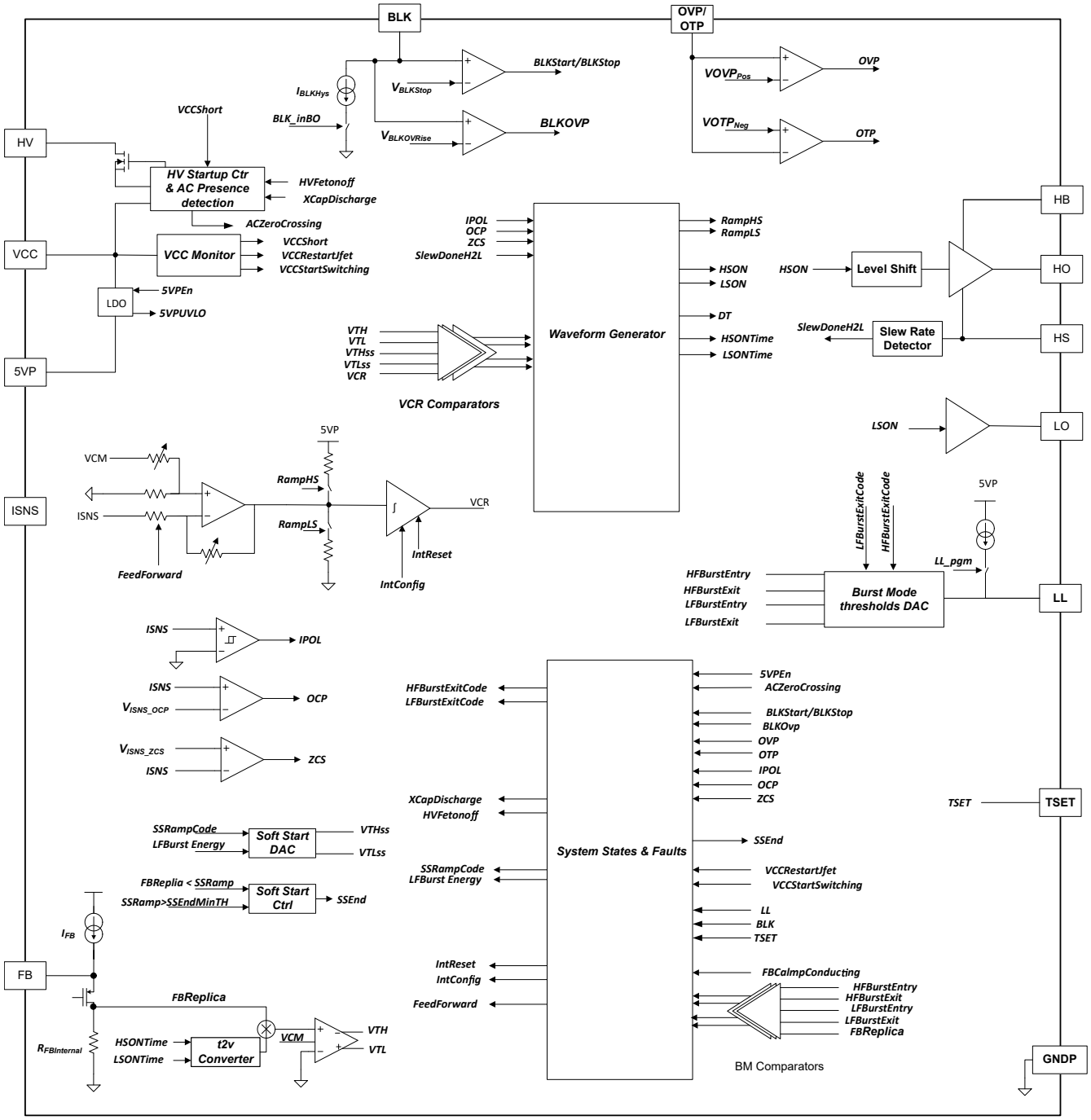

Figure 7-2. Functional Block Diagram

7.3 Feature Description

7.3.1 Input Power Proportional Control

The previous generation of TI LLC controllers use a version of charge control called hybrid hysteresis control (HHC). An improved version of HHC, called input power proportional control (IPPC), is used in the UCC25661x family LLC controller. Compared to traditional direct frequency control, where the control signal is proportional to the switching frequency, traditional charge control methods deliver faster transient response while simplifying

compensator design as the power stage transfer function becomes a first order system. In traditional charge control both input current and switching frequency determine the control signal. IPPC significantly reduces the control signals dependency on switching frequency, thereby minimizing the impact of input and output voltage variations.

IPPC brings in the following advantages:

- Makes control signal proportional to input power
- Consistent burst mode and over load performance in wide LLC (WLLC) operation application
- Retains faster load transient performance and improves line transient performance

The UCC25661x family measures the resonant tank current on the ISNS pin through an external differentiator formed by capacitor C_{ISNS} and resistor R_{ISNS}. The voltage on the ISNS pin is integrated in the VCR synthesizer block to form an internal VCR signal *VCR_synth*. The VCR synthesizer block applies feed forward gain based on the BLK pin voltage, applies ramp compensation to generate the compensated internal VCR signal. The compensated internal VCR signal then compares with two sets of thresholds to control the high side switch turn-off (V_{TH}) and low side switch turn-off (V_{TL}). The thresholds V_{TH} and V_{TL} generate from the internal control signal FBReplica and the high-side and low-side switch on-time from the previous half switching cycle. During the soft start, the V_{TH} and V_{TL} thresholds generate based on the internal soft start ramp to minimize the resonant tank inrush current during start-up.

In Figure 7-3, the high-side and low-side switches are controlled based on the internal VCR signal and comparator thresholds V_{TH} and V_{TL}. When the VCR is higher than V_{TH}, the high-side switch is turned off. When VCR is lower than V_{TL}, the low-side switch is turned off.

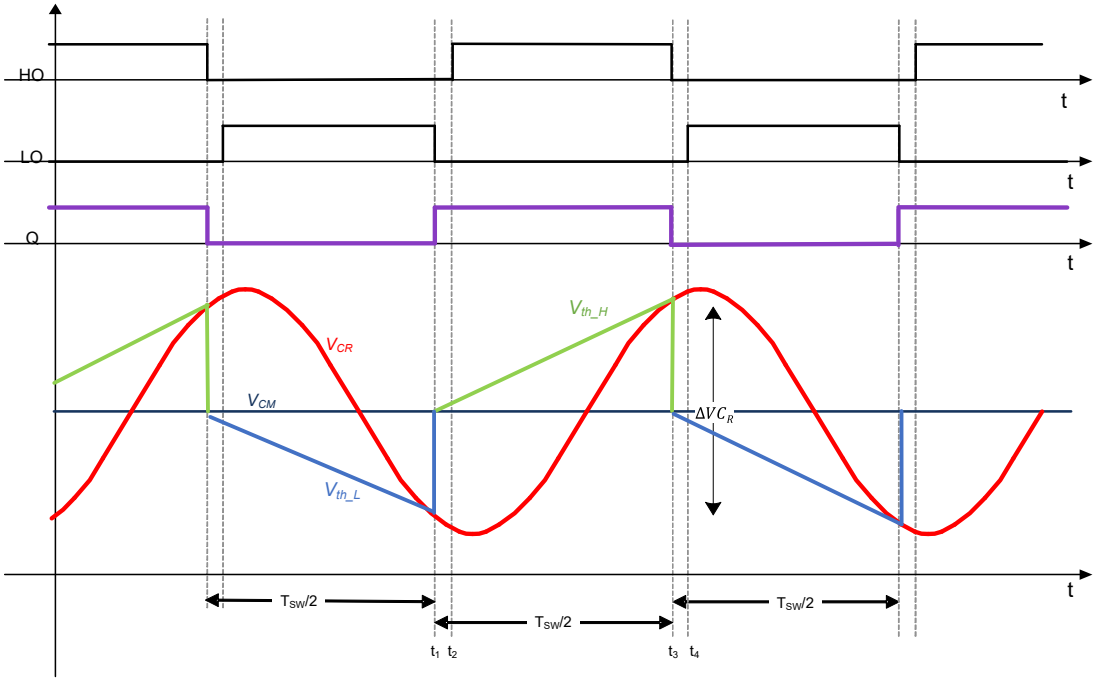

Figure 7-3. IPPC Basic waveforms

Calculate the comparator thresholds V_{TH} and V_{TL} using the equations below. FBReplica is the internal voltage representation of the feedback pin (FB) current. Section 7.3.3 defines the feedback chain.

- T_{sw} = period of a switching cycle
- k = constant

$$V_{TH} = (V_{CM} + k \times FBReplica \times Tsw \div 2) \quad (1)$$

$$V_{TL} = (V_{CM} - k \times FBReplica \times Tsw \div 2) \quad (2)$$

$$V_{TH} - V_{TL} = \Delta V_{CR} = k \times FBReplica \times Tsw \quad (3)$$

7.3.1.1 Voltage Feedforward

By implementing input voltage feed forward, the FBReplica is proportional to the input power and inversely proportional to the magnitude of the resonant tank capacitance. Rewriting the Equation 4 with input voltage feedforward applied.

$$FBReplica = \frac{2}{C_r} \times K_1 \times Pin_{avg} + K_2 \times I_{RAMP} \quad (4)$$

Where K_1 and K_2 are internal synthesizer gains. The input voltage to the LLC power stage is periodically sensed on the BLK pin. A periodic average of the input voltage is used to adjust the feed forward gain to make the control signal proportional to input power. More details are found in Section 7.3.2.

7.3.2 VCR Synthesizer

The UCC25661x family implements a VCR synthesizer which integrates the resonant tank current to form a internal representation of the resonant capacitor voltage. By implementing the VCR synthesizer internally, the UCC25661x family provides for the ability to support very-high-frequency start-up with controlled inrush currents and feed forward gain stage. The internal VCR synthesizer also makes the controller less susceptible to external noise picked up on the ISNS pin, making the controller more robust.

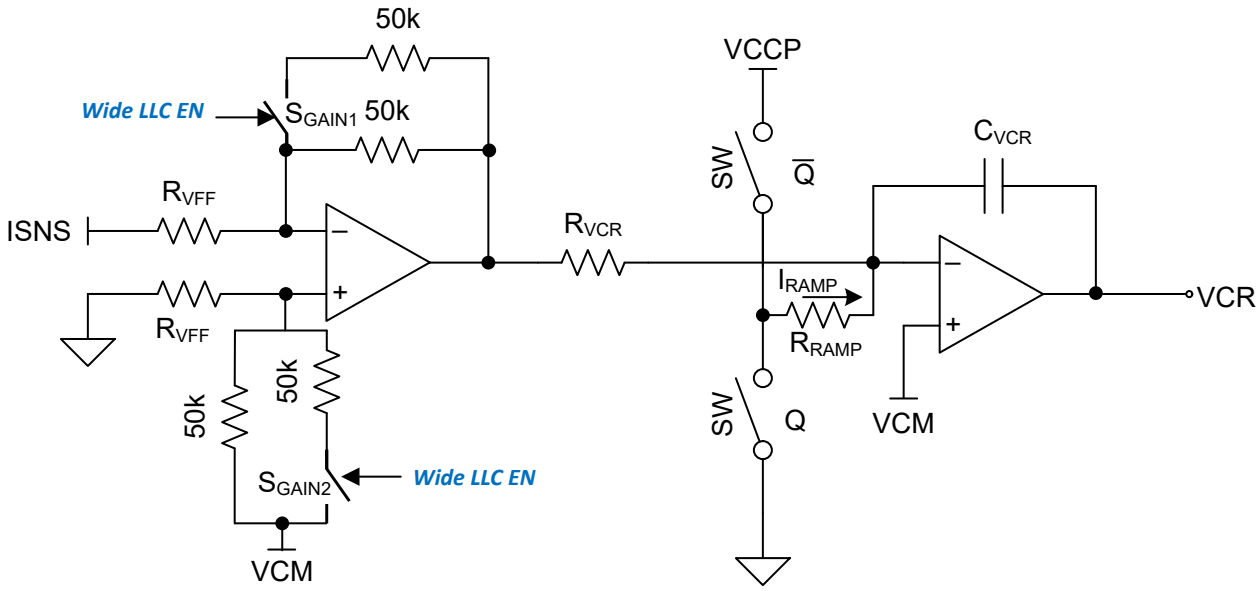

Figure 7-4. VCR Synthesizer Block Diagram

The first stage of the VCR synthesizer consists of a programmable gain stage, used to implement the input voltage feed forward function. The UCC256610 and UCC256614 have extended gain range (EGR) enabled. The EGR feature helps to reduce the FBReplica variation when input voltage of the LLC changed over a wide range (3:1). This variation reduction is achieved by reducing the gain of the programmable gain stage of the VCR synthesizer by factory programming the switches S_{GAIN1} and S_{GAIN2} on.

The second stage consists of a programmable integrator with ramp compensation. To accommodate a wide frequency range of LLC power stages, the time constant of the integrator is externally configurable at start-up to meet the needs of the design using the TSET pin. During start-up, an external resistor divider connected between V5P and GNDP programs the TSET. Connect the center node of the external divider to TSET pin. During the programming phase, a constant current $I_{TSETPrgm}$ is fed to the TSET pin and ADC (V_{TSETA}) measures the resulting voltage. After, $I_{TSETPrgm}$ turns off and the voltage of the TSET resistor divider is measured (V_{TSETB}).

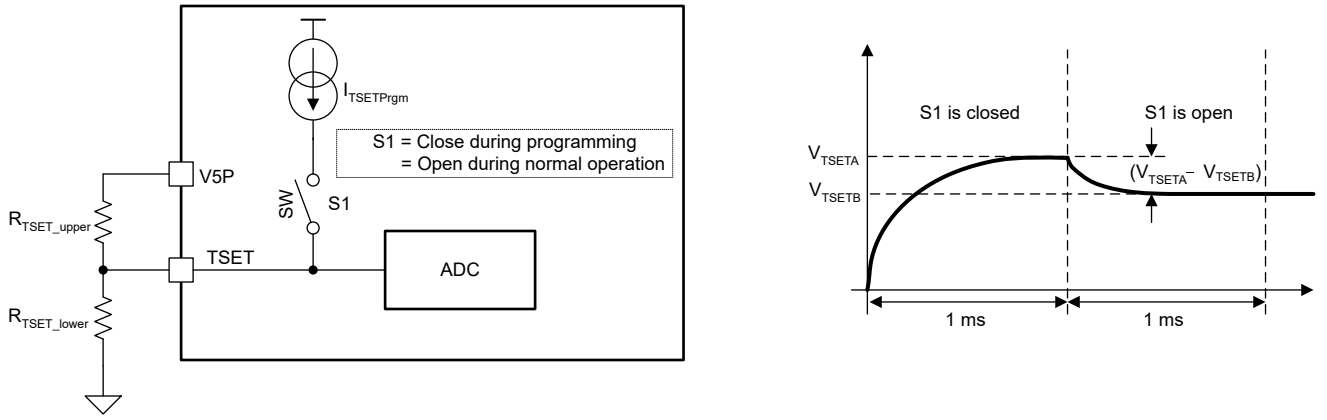

Figure 7-5. TSET Pin Programming

7.3.2.1 TSET Programming

The voltage programmed for VTSETB voltage configures the minimum operating frequency for IPPC operation and the maximum dead time. In the table TSET voltage values indicated are nominal values. Maximum and minimum range used for each TSET setting is within ± 48mV from nominal value.

Table 7-1. TSET Programming Options to select minimum frequency for IPPC operation

TSET OPTION NUMBER	TSET VOLTAGE (V_{SETB}) (V) FOR 3.5V OCP	MINIMUM FREQUENCY FOR IPPC OPERATION (kHz)	MAXIMUM DEAD-TIME (µs)
17	2.295	698.6	0.5
16	2.168	591.6	0.5
15	2.041	501	0.5
14	1.914	424.3	0.5
13	1.787	359.3	1
12	1.66	304.3	1
11	1.533	256.7	1
10	1.416	218.2	1
9	1.299	184.8	1
8	1.182	156.5	1
7	1.074	132.5	1
6	0.967	112.2	1
5	0.850	95	1
4	0.742	80.5	1
3	0.644	68.1	1
2	0.547	57.7	1
1	0.450	48.9	1
X(1)	< 0.392	—	—

(1) Not recommended for use.

The difference between VTSETA and VTSETB configures the integrator time constants that set the FBReplica magnitude for a given power output, enabling setting the overload power (OLP) thresholds.

Table 7-2. TSET Programming Options to Select Integrator Time Constant

TSET OPTION NUMBER	TSET VOLTAGE(V_{TSETA}-V_{TSETB}) (V) FOR 3.5V OCP	INTEGRATOR TIME CONSTANT (ns)
17	2.295	68
16	2.168	80
15	2.041	93

Table 7-2. TSET Programming Options to Select Integrator Time Constant (continued)

TSET OPTION NUMBER	TSET VOLTAGE(V_{TSETA}-V_{TSETB}) (V) FOR 3.5V OCP	INTEGRATOR TIME CONSTANT (ns)
14	1.914	112
13	1.787	132
12	1.66	156
11	1.533	184
10	1.416	214
9	1.299	257
8	1.182	304
7	1.074	359
6	0.967	424
5	0.850	490
4	0.742	588
3	0.644	694
2	0.547	820
1	0.450	968
X(1)	< 0.392	X

1. Not recommended for use.

7.3.2.2 TSET Programming for UCC256616

In the case of UCC256616, only the V_{TSETB} voltage configures the TSET settings. Based on the V_{TSETB}, not only the time constant but the OCP threshold can be selected. Once the time constant is selected, the maximum dead-time is also configured. Column 2 in Section 7.3.2.2 indicates the minimum frequency down to which the IPPC operation is maintained. Below this frequency, the controller still maintains closed-loop operation and works in conventional current mode control.

In TSET Programming Options Table for UCC256616, the TSET voltage values indicated are nominal values. Maximum and minimum range used for each TSET setting is within ±48mV from the nominal value.

Table 7-3. TSET Programming Options Table for UCC256616

TSET OPTION NUMBER	TSET VOLTAGE (V) FOR 3.5V OCP	TSET VOLTAGE (V) FOR 4V OCP	MINIMUM FREQUENCY FOR IPPC OPERATION (kHz)	INTEGRATOR TIME CONSTANT (ns)	MAXIMUM DEAD-TIME (µs)
17	2.295	2.675	698.6	68	0.5
16	2.168	2.802	591.6	80	0.5
15	2.041	2.929	501	93	0.5
14	1.914	3.056	424.3	112	0.5
13	1.787	3.183	359.3	132	1
12	1.66	3.310	304.3	156	1
11	1.533	3.427	256.7	184	1
10	1.416	3.554	218.2	214	1
9	1.299	3.681	184.8	257	1
8	1.182	3.798	156.5	304	1
7	1.074	3.906	132.5	359	1
6	0.967	4.013	112.2	424	1
5	0.850	4.130	95	490	1
4	0.742	4.238	80.5	588	1
3	0.644	4.336	68.1	694	1

Table 7-3. TSET Programming Options Table for UCC256616 (continued)

TSET OPTION NUMBER	TSET VOLTAGE (V) FOR 3.5V OCP	TSET VOLTAGE (V) FOR 4V OCP	MINIMUM FREQUENCY FOR IPPC OPERATION (kHz)	INTEGRATOR TIME CONSTANT (ns)	MAXIMUM DEAD-TIME (µs)
2	0.547	4.433	57.7	820	1
1	0.450	4.532	48.9	968	1
X(1)	< 0.392	> 4.589	—	X	—

(1) Not recommended to use.

7.3.3 Feedback Chain (Control Input)

Control of the output voltage is provided by a voltage regulator circuit located on the secondary side of the isolation barrier. The demand signal from the secondary-side regulator circuit is transferred across the isolation barrier using an optocoupler.

A constant current source I_{FB} is generated from VCCP voltage and connected to FB pin. A resistor RFB is also connected to the constant source current source with a PMOS in series. During normal operation, the PMOS is always on so that the FB pin voltage is equal to the Zener diode reference voltage plus the voltage drop on the PMOS source to gate.

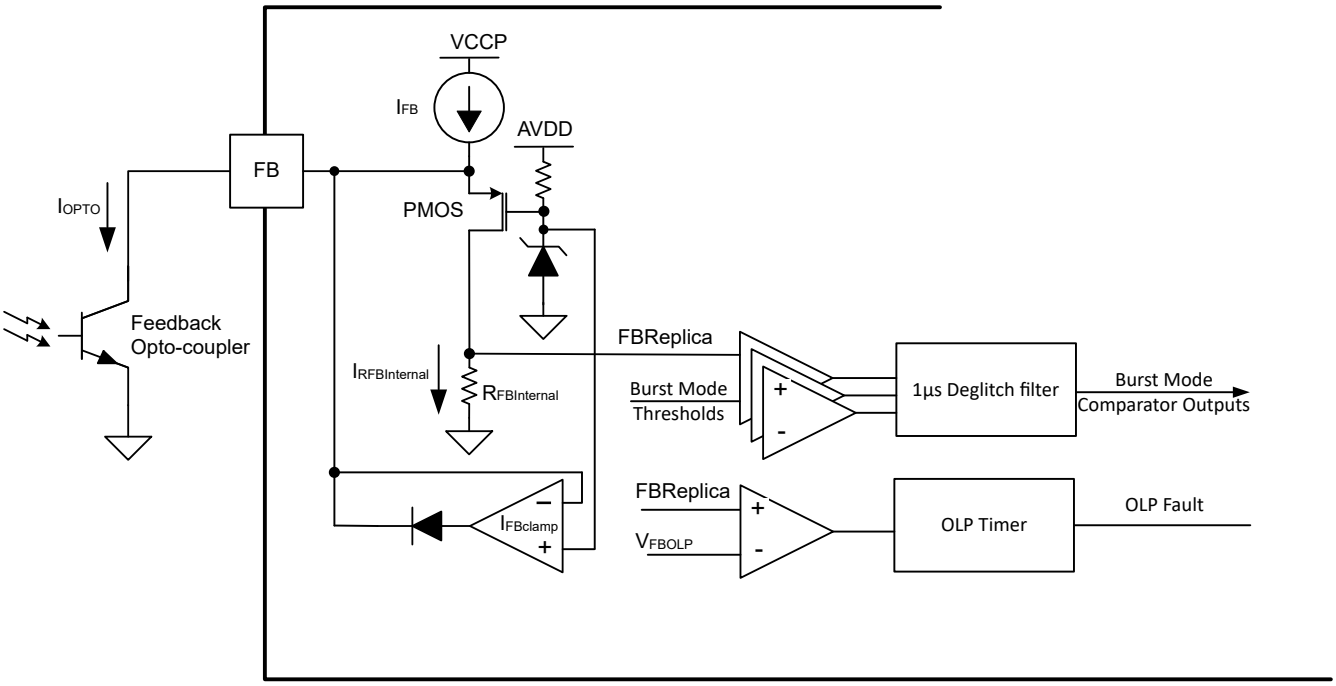

Figure 7-6. Feedback Chain Block Diagram

$$I_{R_{FBInternal}} = I_{FB} - I_{OPTO} \quad (5)$$

The control signal *FBReplica* is depicted using Equation 6.

$$FBReplica = I_{R_{FBInternal}} \times R_{FBInternal} \quad (6)$$

From Equation 6, when I_{OPTO} increases, $I_{RFBInternal}$ decreases, decreasing the *FBReplica*. In this way, the control signal is inverted. When I_{OPTO} continues to increase and reaches the value of I_{FB}, the FB pin voltage starts to drop because there is not enough current flow through the PMOS. FB pin pulled low impacts the system transient response, due to the extra delay introduced by charging the parasitic capacitor of the optocoupler to

pull up the FB pin voltage. A FB pin voltage clamp circuit is used to prevent this scenario. When FB pin voltage drops below the FB pin clamp voltage threshold, an extra current source is turned on to clamp the FB voltage. The clamp strength is $I_{FBClamp}$. The FB pin clamp circuit improves the system transient performance from light load to heavy load. The FB pin clamp operation is shown in the figure below.

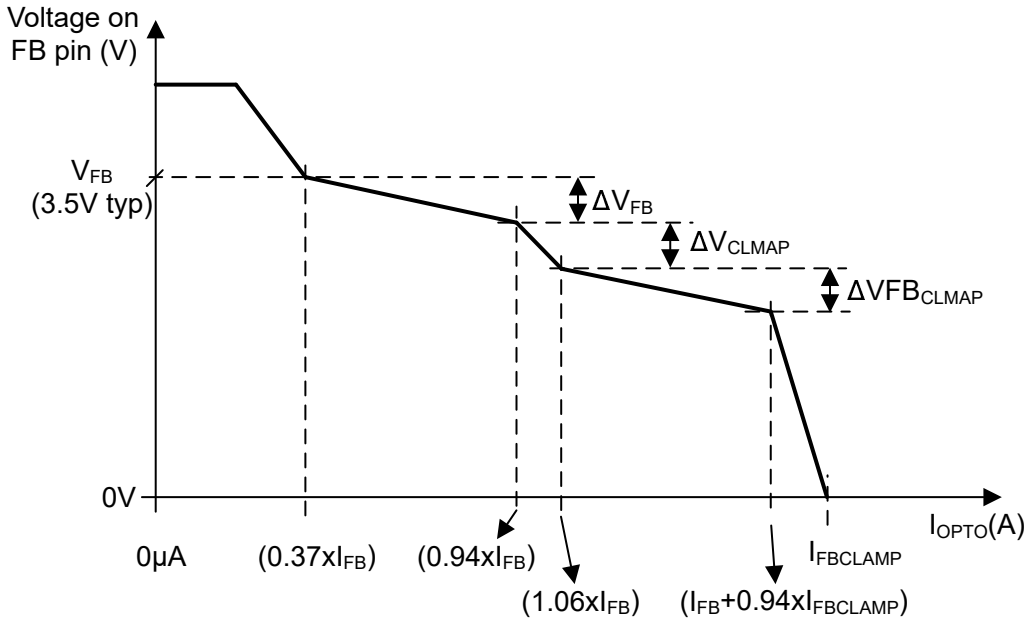

Figure 7-7. FB Pin Voltage versus FB Pin Current

7.3.4 Adaptive Dead-Time

The UCC25661x family implements a high-speed, low latency, slew-rate detection block to optimize the dead time between high-side and low-side pulses. The adaptive dead-time block adjusts the dead time to prevent shoot-through and excessive body diode conduction.

At the core of the adaptive dead time block is the slew rate detector block, capable of detecting slew rates up to 200V/ns, making UCC25661x family an excellent choice for use in high frequency resonant converters.

In burst mode, during a ZCS prevention operation or in power stages where the slew rate can be slow, the resonant tank current polarity signal (Ipolarity comparator output) is used to augment the slew rate detector.

Taking advantage of the natural symmetric operation of LLC, the slew rate detector determines only the dead time between high-side switch turn off and low-side switch turn on. This dead time is copied and applied to the dead time between low-side MOSFET turn off and high-side MOSFET turn on. There are a few exceptions where the dead time is not copied. The conditions are listed below:

- Missing slew rate detector signal in the previous *High* to *Low* transition
- ZCS detection in the previous cycle

Under the above-mentioned conditions, the Ipolarity comparator based on the ISNS signal is used to adjust the dead time during low to high transitions.

7.3.5 Input Voltage Sensing

The input voltage sensing through BLK pin is used to implement multiple functions listed below:

- Input voltage brown-in and brown-output
- Input feedforward (explained in Section 7.3.1)
- Input voltage OVP

7.3.5.1 Brownin and Brownout Thresholds and Options

UCC25661x family provides programmable brownin and brownout thresholds. When the voltage on the BLK pin falls below $V_{BLKStop}$, the controller enters brownout state and stops switching. In the brownout state, an additional current sink is turned on to draw I_{BLKHys} form the BLK pin. Program the actual brownin voltage by changing the equivalent resistance externally connected to the pin externally.

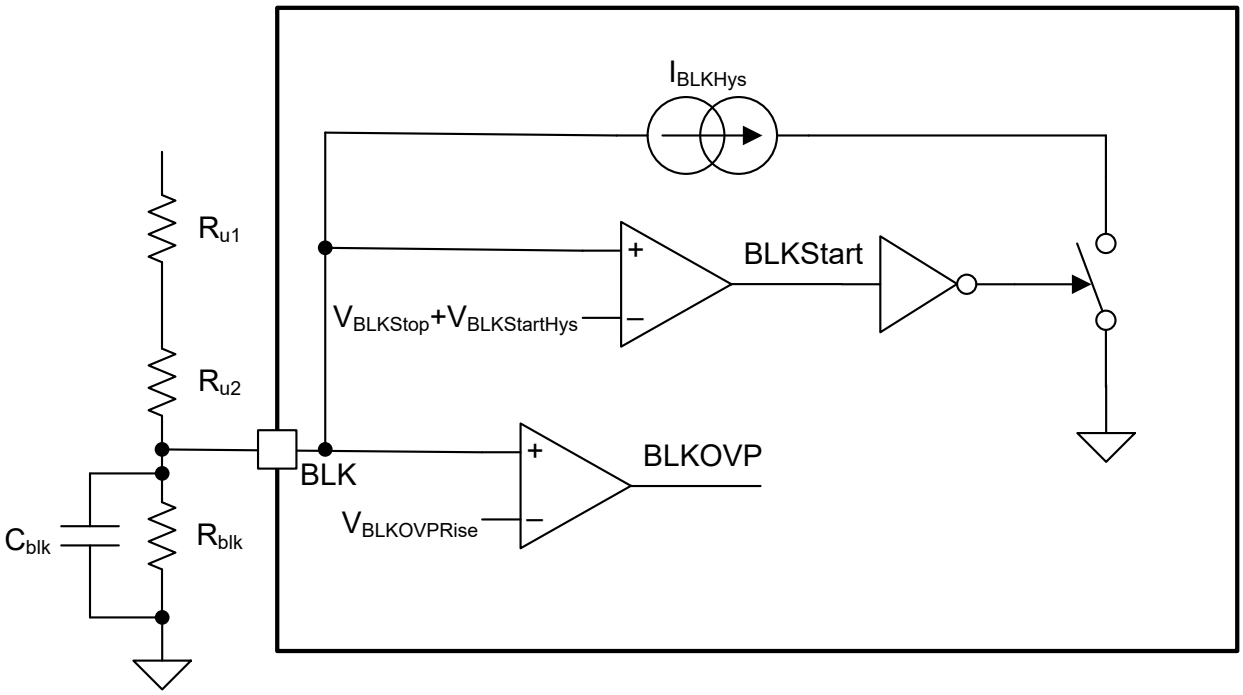

Figure 7-8. BLK Pin Input Voltage Sensing Architecture

When brownout is detected, the controller stops switching. If BLK voltage rises above the brownin voltage, the controller immediately begins soft start and does not wait for fault idle time.

7.3.5.2 AC Input Zero Crossing Detection

Input zero crossing detection is only enabled when AC brownout option is selected for BLK pin sensing. With this option, the BLK pin detects the HV pin voltage through a resistor divider. The expected waveform is the divided down rectified AC voltage. Below shows an example using 8MΩ and 100kΩ for the BLK resistor divider at 70Vac input and 265Vac input.

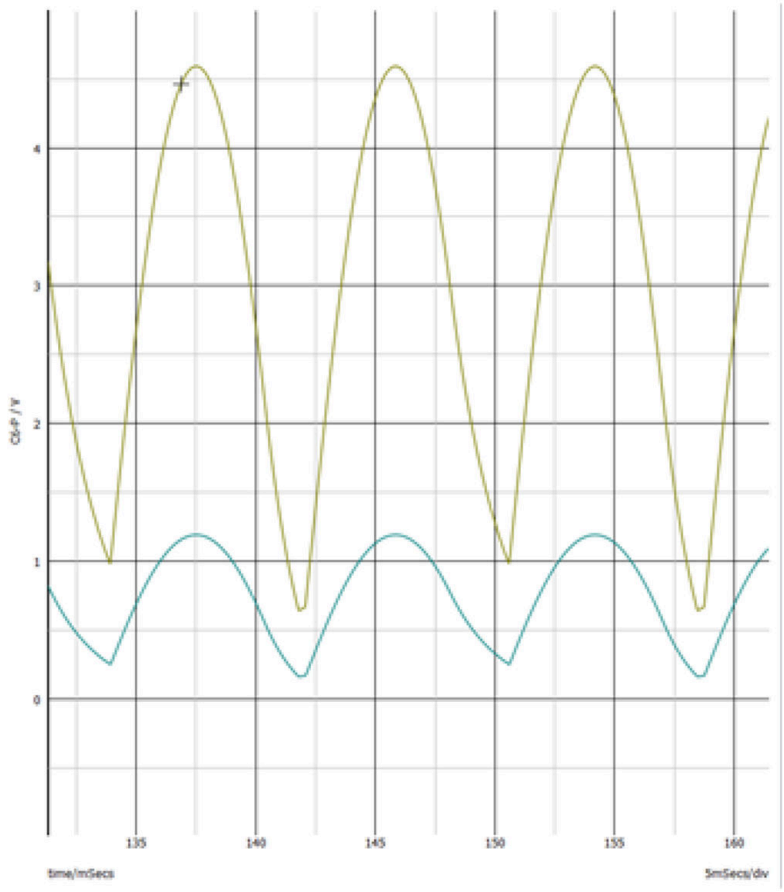

Figure 7-9. Input AC Zero Cross Detection Using BLK pin

The method to determine AC presence uses a comparator that looks at the instantaneous BLK voltage and ½ of the BLK peak detector output. If the instantaneous BLK voltage falls below ½ the peak BLK voltage and then rises above ½ BLK peak voltage (with a hysteresis), AC presence is detected. Effectively, the X-capacitor discharge algorithm is looking for a rising edge on the BLK comparator output (blk_zcd) to detect the presence of AC.

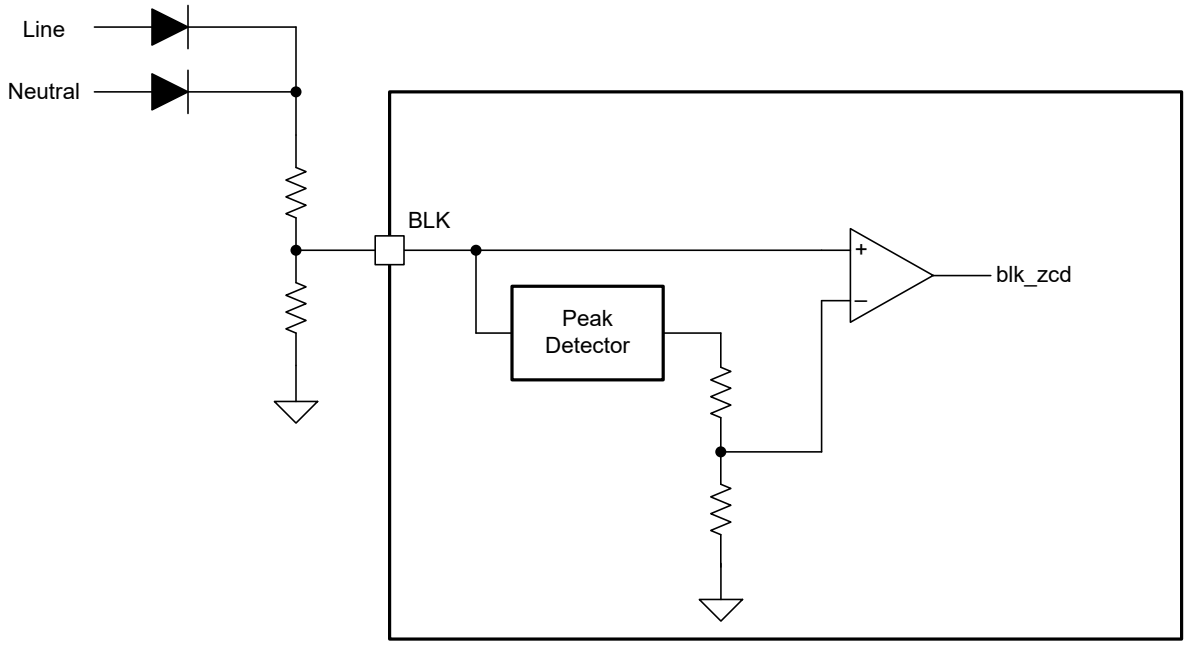

Figure 7-10. BLK ZCD Detection Block Diagram

7.3.5.3 Output OVP and External OTP

UCC25661x family uses a multifunction pin (OVP/OTP) to monitor for output overvoltage and external over-temperature conditions. Reflected voltage on bias winding and supply voltage VCCP monitors the output voltage.

A Zener diode connects between the VCCP and the OVP/OTP pin. Under normal operating conditions, the Zener does not conduct and the OVP/OTP pin voltage is the result of the NTC resistance and I_{OTP} source current. If VCCP rises high enough to exceed the Zener breakdown voltage, the voltage on the OVP/OTP pin is pulled high because of the Zener current. If the voltage on OVP/OTP exceeds the $VOVP_{pos}$ threshold for 40us the controller detects a fault and stops switching.

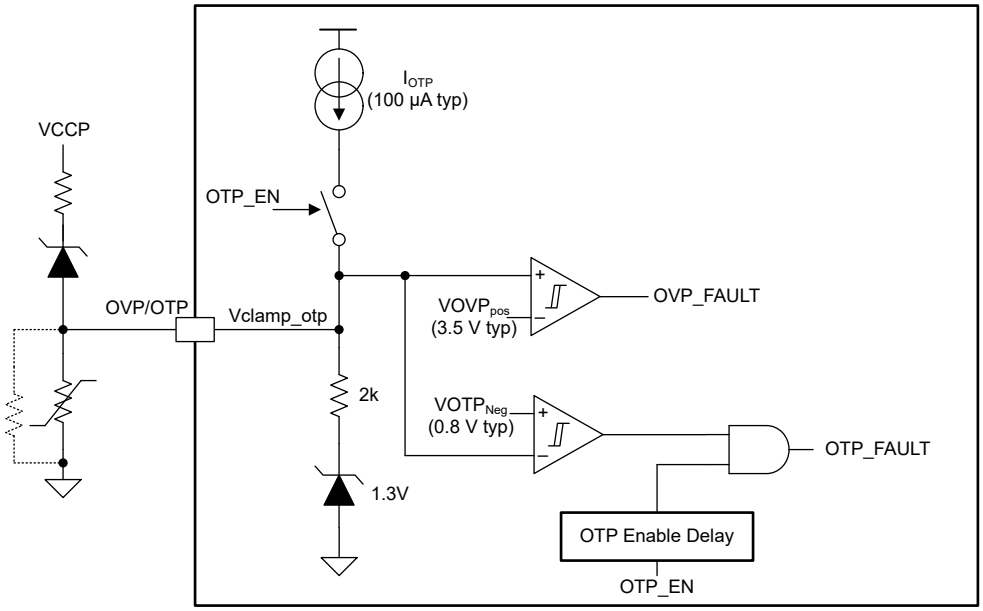

Figure 7-11. OVP/OTP Protection Architecture

A NTC is connected from OVP/OTP to GNDP. An internal current source, I_{OTP}, flows out of the OVP/OTP pin and into the NTC resistor. Based on the temperature of the NTC, the resulting voltage on the pin is compared to $VOTP_{Neg}$ to determine if an external over-temperature fault occurs. Upon detection of external over-temperature protection, UCC25661x family moves to the fault state. After the 1s wait period, UCC25661x family checks the OVP/OTP pin voltage. If the OVP/OTP pin voltage is higher than $VOVP_{Pos}$, the UCC25661x family attempts to restart. If restarting is not possible, the UCC25661x family continues to wait in fault idle state. During burst mode, the over-temperature protection is disabled to minimize quiescent current. When transitioning from burst mode to normal switching, the OTP function is re-enabled.

7.3.6 Resonant Tank Current Sensing

The ISNS pin senses the resonant tank current through a differentiator. Besides serving as over current protection pin, the ISNS pin is also an essential part of the control functions.

The ISNS pin has the following functions

- Input to the integrator that develops the control voltage, used for IPPC control
- OCP (cycle-by-cycle) protection
- Resonant current polarity detection
- ZCS prevention and dead-time management
- Reverse recovery avoidance at start-up

7.4 Protections

7.4.1 Zero Current Switching (ZCS) Protection

ZCS protection is a necessary function for LLC converters to avoid crossing over into the capacitive region of operation. In the capacitive region, the MOSFETs can be damaged due the reverse recovery of the body diode allowing both switches to briefly conduct current. In addition, the gain vs frequency relationship inverts in the capacitive region and can cause the converter to completely lose regulation of the power stage. The goal of the ZCS protection is to make sure that the MOSFET can be turned off before the current inverts thereby eliminating possibility of a hard reverse recovery of the MOSFET body diode. This can increase the reliability of the power stage. The minimum turn-off current is set at a threshold which can increase the chances of achieving ZVS or close to ZVS switching for switches under this condition. Coupled with the dead time engine which looks at both the slew done signal and the IPOL signal, users can confirm that the opposite MOSFET turns-on at the valley point of the V_{DS} voltage, minimizing switching losses.

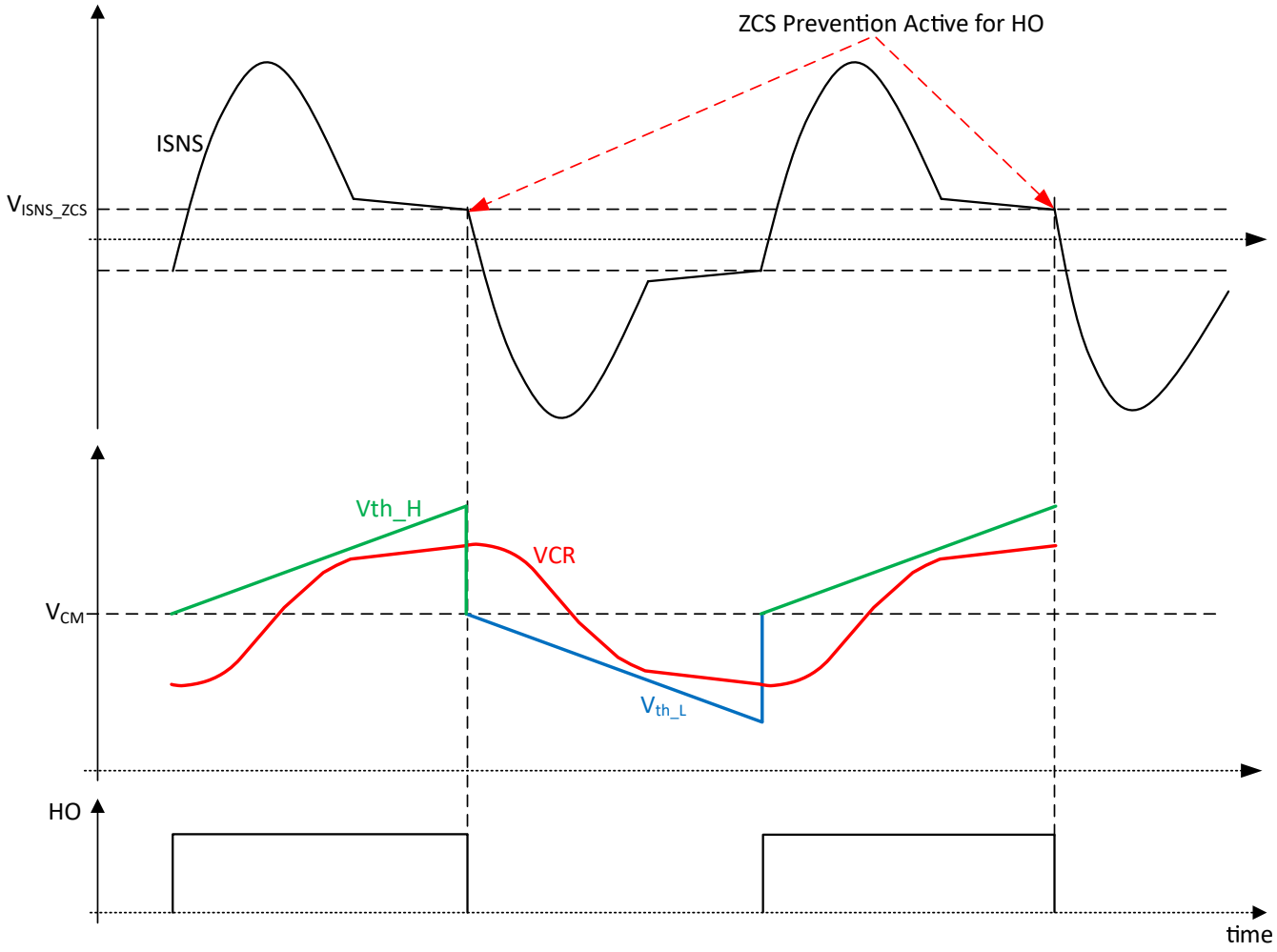

Figure 7-12. ZCS Protection

When operation nears the inductive/capacitive boundary, the resonant current decreases before the gate is turned off. If the ISNS waveform is less than the V_{ISNS_ZCS} threshold, the gate pulse HO is terminated early instead of waiting for the VCR waveform to cross the VTH boundary. This early gate termination scheme is capable of leaving enough resonant current at the gate turn-off edge to drive the ZVS transition during the dead-time. Similar explanation holds good for the LO gate pulse.

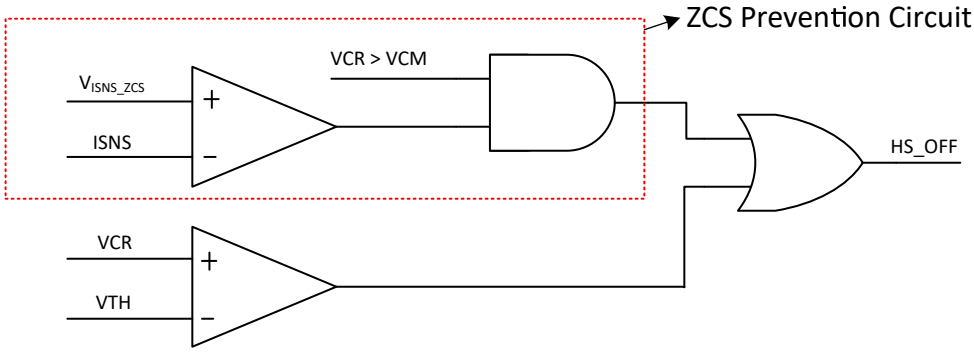

Figure 7-13. ZCS Prevention Scheme When the High-Side MOSFET is On

The shape of the resonant current well below the resonant frequency poses some challenge for detecting the correct falling edge of the resonant current waveform. The UCC25661x family implements additional logic

to make sure that the correct falling edge of the ISNS signal is detected to avoid false tripping. To improve robustness against noise, the ISNS ZCS comparators are blanked at the rising edge of HO or LO gate. The same blanking time is used for both the VCR comparators and the ISNS ZCS comparators. When a ZCS event is detected, the internal soft start ramp voltage is slowly reduced. When the internal soft start ramps down, the switching frequency is also forced to increase, forcing the converter out of capacitive region. In the event of a persistent ZCS condition for a period of TZCSFault the UCC25661x family controller ceases switching and move to the fault state.

7.4.2 Minimum Current Turn-off During Soft Start

During start-up and for the first few switching cycles, the MOSFET on the primary side can experience body diode reverse recovery and hard switching. The experience is mainly due to the fact that at start-up the resonant capacitor can have DC bias voltage which is off from the steady state operating voltage of Vin/2. This leads to a asymmetry in the resonant tank current at start-up. In the first few cycles, asymmetry can be high enough that the current at the point of switch turn-off is in the wrong polarity.

For example, refer to Figure 7-14.

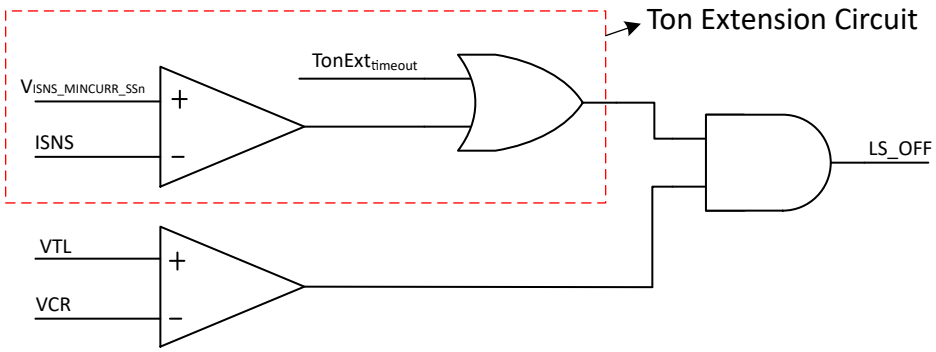

Figure 7-14. Ton Extension Scheme

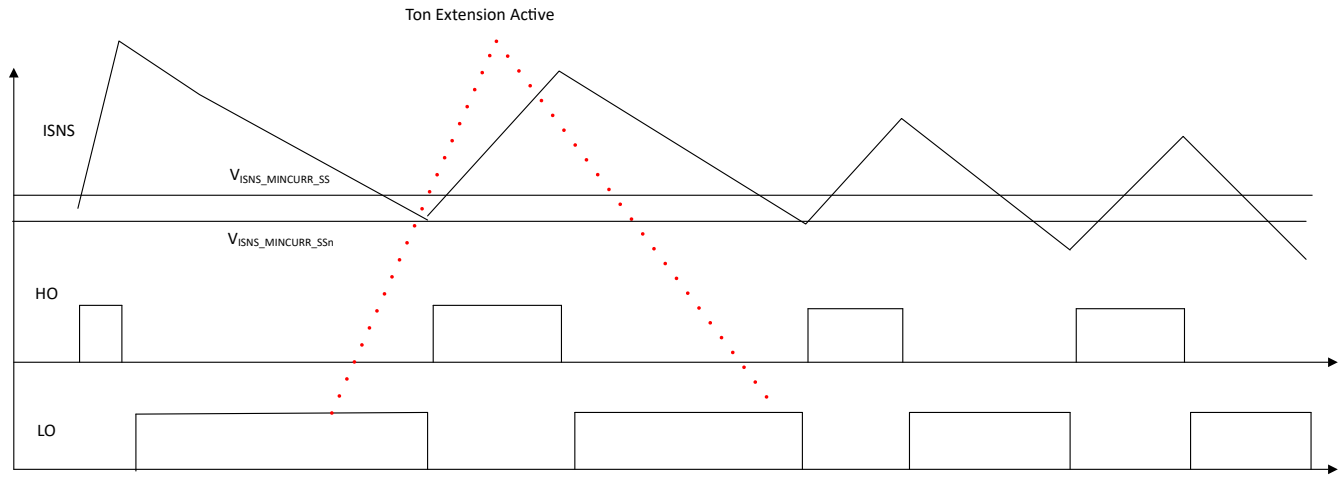

Figure 7-15. ZCS Prevention During Startup

7.4.3 Cycle by Cycle Current Limit and Short Circuit Protection

The OCP and cycle-by-cycle current limiting feature in the UCC25661x family provides a fast (<50ns) response to short circuit. The cycle-by-cycle protection helps to limit the peak stress in the power stage. When the ISNS voltage becomes greater than V_{ISNS_OCP}, the present HO gate pulse is terminated. Correspondingly, during the second half cycle, the present LO pulse is terminated when the corresponding overcurrent limit is detected. If OCP is detected in 7 consecutive switching cycles (n_{OCP}), the device moves to the fault state. During startup, if OCP condition is detected in 50 consecutive switching cycles (n_{OCP_SS}), the device moves to fault state.

7.4.4 Overload (OLP) Protection

IPPC with feed forward creates a strong correlation between Pout versus the internal control signal FBReplica.

When the FBReplica goes above the V_{FBOLP} (for example, I_{opto} reduces to 0µA), the system starts to limit the input power and the OLP timer count increases. If the FBReplica stays above V_{FBOLP} for > (T_{OLP}), the OLP fault is detected and the system enters into the fault restart sequence.

7.4.5 VCC OVP Protection

An internal current limited clamp on the VCCP pin protects the VCCP pin and clamps the gate drive output voltage when the voltage applied to the VCCP pin exceeds the recommended max voltage. The clamp has maximum sink current $IVCC_{Clamp}$. If the current going through the VCC_{Shunt} exceeds $IVCC_{Clamp}$, the result is the further increase in the VCCP pin voltage above VCC_OV. If the increase occurs, UCC25661x moves to fault condition and retries after the 1s fault idle time.

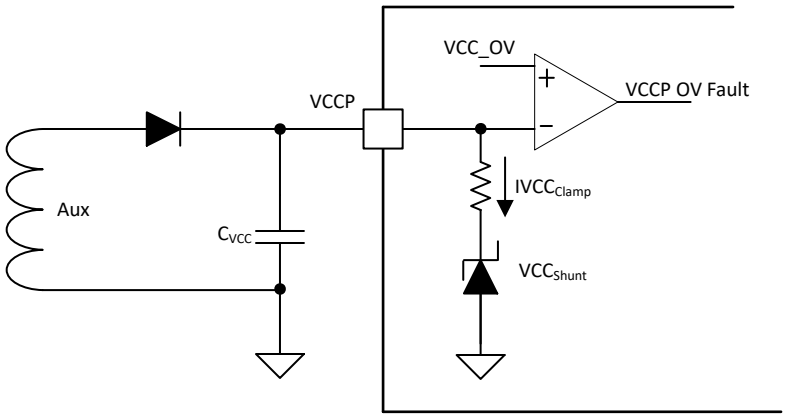

Figure 7-16. VCC Clamp

7.5 Device Functional Modes

7.5.1 Startup

7.5.1.1 With HV Start-up

7.5.1.1.1 First Time Start-up Sequence

1. When AC is plugged in, voltage is applied on HV pin. If VCCP voltage is below VCC_{Short}, VCCP pin is charged with $I_{VCC\_Charge\_Low}$. If VCCP voltage is higher than VCC_{Short}, VCCP pin is charged with $I_{VCC\_Charge\_High}$.
2. When VCCP voltage is higher than VCC_{UVLOr}, an internal LDO regulates the V5P voltage until the device initialization is complete.
3. V5P is established. LL pin and TSET pin are used for burst mode and internal VCR Synthesizer programming.
4. If the HV start-up option is enabled, the TSET pin outputs high (means PFC OFF) to prevent PFC from turning on before VCCP is full established.
5. When VCCP is higher than $VCC_{StartSelf}$, HV charge current stops. LLC start-up process begins. TSET voltage is kept lower than 1V, allowing PFC to startup.
6. If during stages 3 and 4, VCCP voltage drops below $VCC_{ReStartJfet}$, HV charge current enables again and VCCP gets charged with $I_{VCC\_Charge\_High}$
7. Once LLC finishes start-up, HV charge current is disabled until VCCP drops below $VCC_{ReStartJfet}$.
8. During normal operation if the VCCP voltage falls below $VCC_{StopSwitching}$, a fault occurs and UCC25661x family shuts down. Normal restart sequence is then followed.

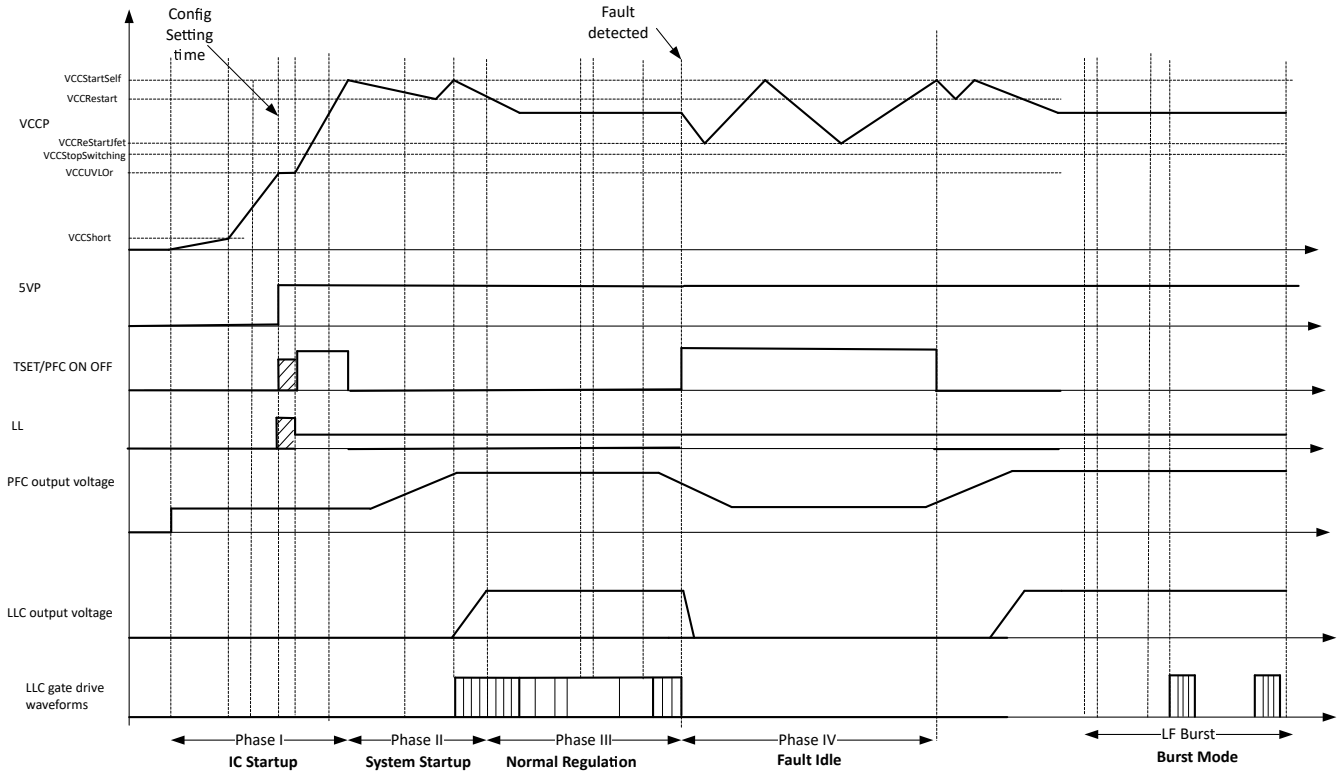

Figure 7-17. Startup Sequence for *HV Startup* Feature Enabled

7.5.1.1.2 Restart Sequence

1. After a fault is detected, UCC25661x family shuts down. For fault retry mode, after 1s idle time, UCC25661 retries (TSET outputs high when VCCP is still higher than VCC_{UVLOf}).
2. If VCCP voltage is below VCC_{Short}, VCCP pin is charged with $I_{VCC\_Charge\_Low}$. If VCCP voltage is higher than VCC_{Short}, VCCP pin is charged with $I_{VCC\_Charge\_High}$. If VCCP pin voltage is higher than $VCC_{StartSelf}$, HV startup is not enabled (Phase I is skipped). V5P is established and LL pin is released for burst mode programming.

7.5.1.2 Without HV Startup

When HV startup is disabled, the PFC on/off signal is disabled as well. The startup sequence is as follows:

1. When VCCP voltage is higher than VCC_{UVLOr}, V5P is established
2. LL pin and TSET pin are used for burst mode and internal VCR integrator programming.
3. When VCC drops below VCC_{UVLOf}, V5P turns off and system shuts down.

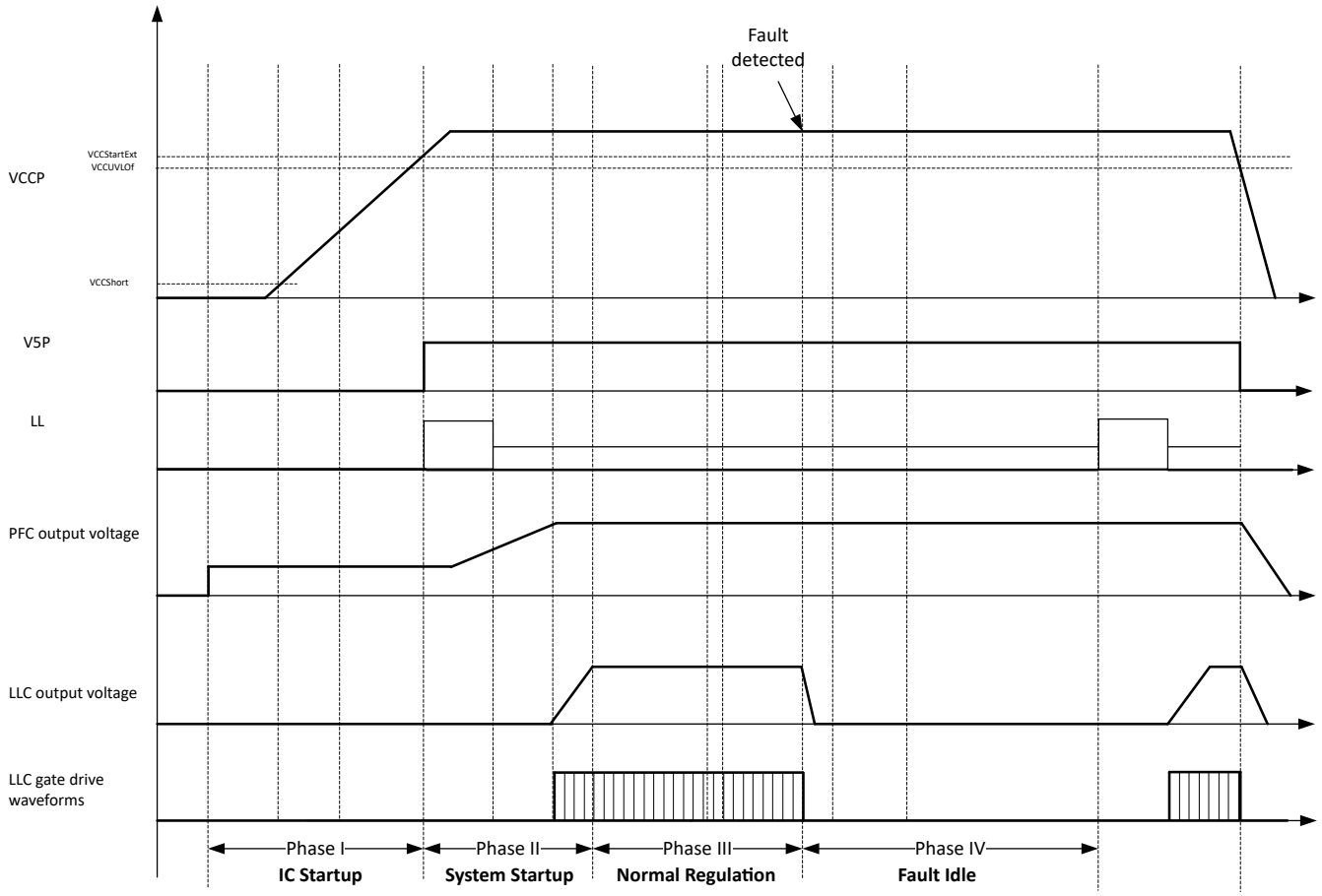

Figure 7-18. Startup Sequence for "HV Startup" Feature Disabled

7.5.2 Soft Start Ramp

The soft start ramp is internally generated in the UCC25661x family. A fixed maximum soft start time of 25ms is internally generated to reduce inrush current at start-up, while allowing a fast output-voltage ramp up.

7.5.2.1 Startup Transition to Regulation

In UCC25661x family, a new soft start is implemented to control the inrush current at startup. The new scheme helps avoiding any premature soft start termination and establishes smooth transition between soft start and closed loop regulation.

At start-up, internal soft start voltage (*SSRamp*) ramps up using a defined slope and the *FBReplica* is high as the output voltage is below the regulation voltage. A pick lower block identifies the two signals and uses the one that is lower of the two to control the turn-off of the power stage switches.

The soft start is exited only after the *SSRamp* is above a minimum threshold, avoiding any premature soft start exit, as shown in Figure 7-19.

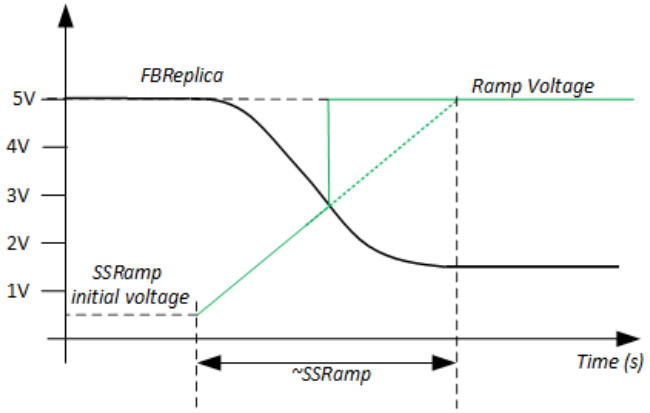

Figure 7-19. Soft Start Operation

7.5.3 Light Load Management

7.5.3.1 Operating Modes (Burst Pattern)

UCC25661x family burst mode algorithm minimizes audible noise, while improving light load efficiency. This is accomplished by maintaining the burst packet frequency to either be above the audible range (> 25kHz) or to maintain the burst packet frequency to be at the very low end of the audible region (< 400Hz). UCC25661x family employs two burst mode patterns; high-frequency (HF) pulse skip and low-frequency (LF) burst.

HF burst packet includes a fixed number of LO and HO pulses. The purpose of HF burst is to maintain the burst frequency higher than the audible frequency range. In the below image, the low-side gate is enabled on the 2nd valley of the switch node to begin delivery of the next HF burst packet.

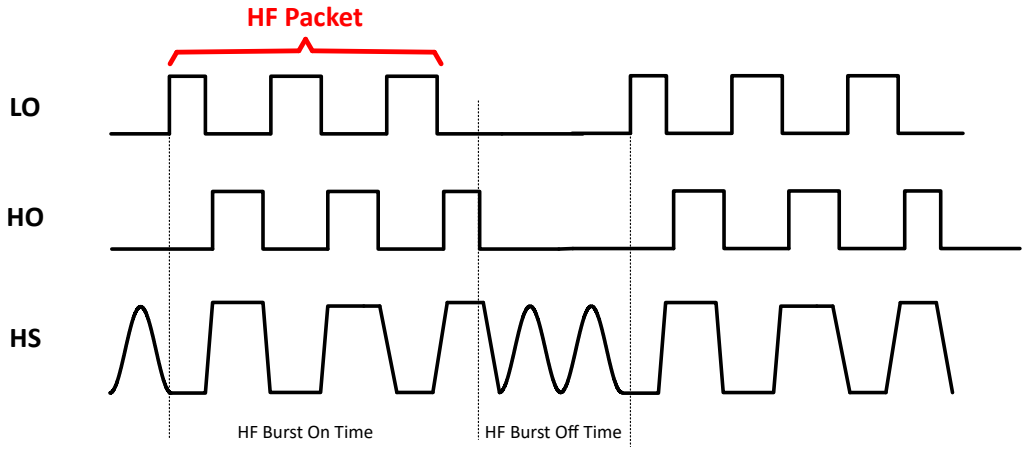

Figure 7-20. High Frequency Pulse Skip Packet

LF burst includes several HF burst packets and a LF burst off period.

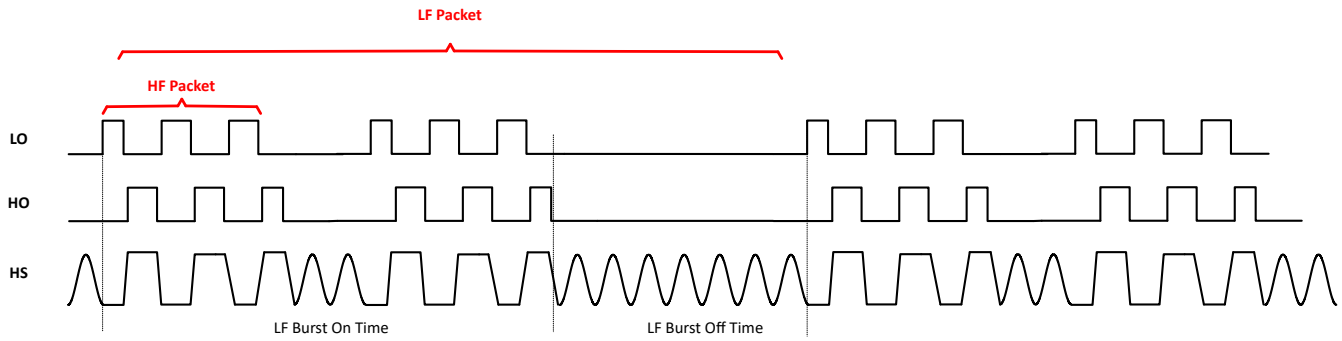

Figure 7-21. Low Frequency Burst Packet

The number of HF burst packet is calculated to maintain the LF burst frequency within a frequency range. A set of target frequency range is internally provided, the default option is to regulate the LF burst around 200Hz.

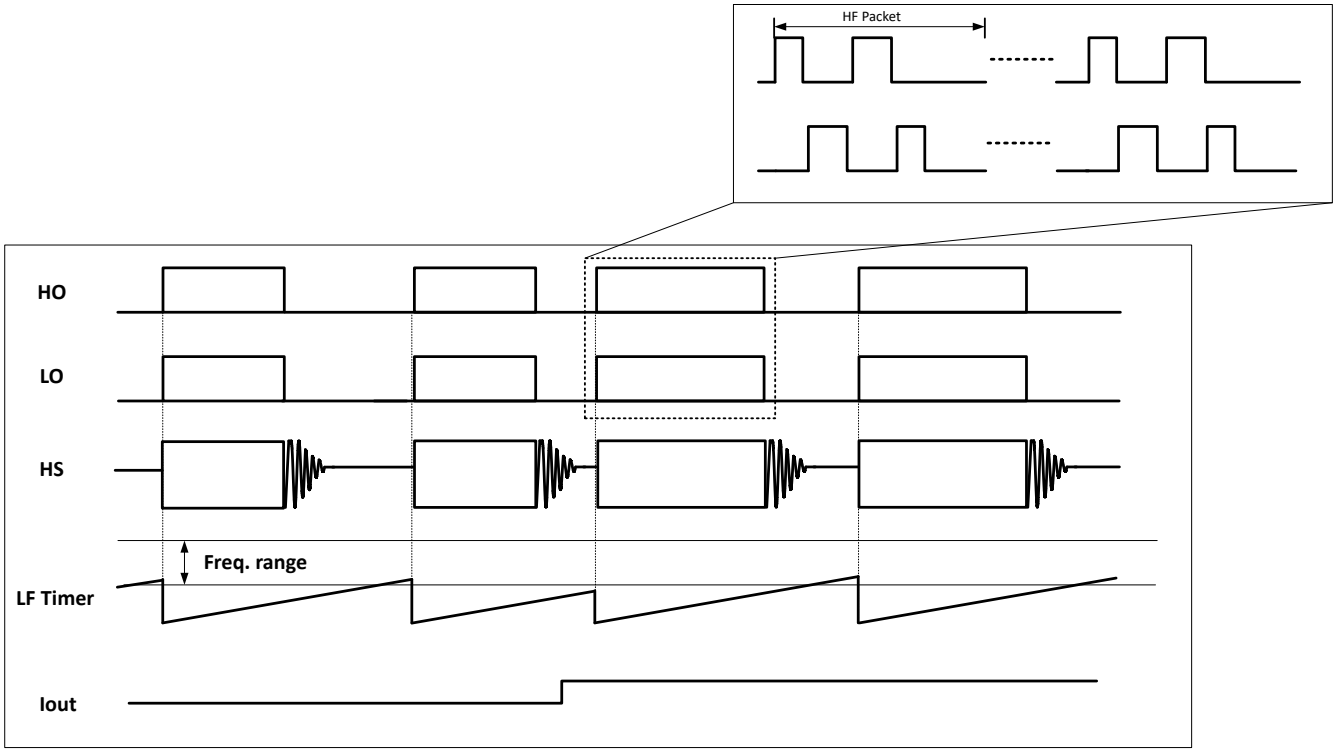

Figure 7-22. Packet Size Regulation Inside LF Burst

7.5.3.2 Mode Transition Management

Using the LL pin, the user configure the power level at which the UCC25661x family enters the HF pulse skip and LF Burst mode. The two thresholds that can be set are the *HFBurstEntry* and *LFBursttEntry*. More details on how to configure the power level are in Section 7.5.3.3.

Figure 7-23 describes the entry and exit behavior of UCC25661 in burst mode.

- The *HFBurstEntry*, corresponds to the *FBReplica* voltage at the desired power level where the system enters HF Pulse skip.
- The *LFBurstEntry* corresponds to a modified *FBReplica* voltage at which the system enters LF Burst.
- When *FBreplica* is higher than HFBurstEntry, UCC25661x family operates in normal switching.
- When *FBreplica* is less than *HFBurstEntry* but greater than *LFBurstEntry*, UCC25661x family operates in HF pulse skip mode. In the HF pulse skip mode, the energy in each packet is still controlled by the control signal *FBReplica*.

- When *FBreplica* is less than *LFBurstEntry*, UCC25661x family operates in LF burst mode. In the LF Burst mode, the energy in each packet is fixed at *LFBurstEntry* threshold.
- While operating in LF Burst mode, a new LF Burst segment is started when the *FBReplica* rises above the *LFBurstEntry* threshold. The segment is terminated when the desired number of packets are delivered and the *FBReplica* is below the *PacketStop* threshold.
- The desired number of packets in a LF Burst segment is computed to regulate the LF Burst operating frequency within 200Hz to 400Hz.
- In case of a sudden load drop, the LF Burst segment is immediately terminated to avoid output over voltage condition.
- Once in LFBurst, the *LFBurstExit* and *HFBurstExit* thresholds are continually calculated. The Equation 7 and Equation 8 describes this.
- As the *FBReplica* increases above the *LFBurstExit*, the UCC25661x family goes back to working in HF Burst Mode.
- When the *FBReplica* rises above the *HFBurstExit*, the UCC25661x family exits HFBurst and enters to normal switching.
- Every time the controller exits the HFBurst, a blanking time of 2ms is added to verify that the controller does not reenter into Burst mode. During the blanking period, if the *FBReplica* falls below the PacketStop threshold, the controller reenters LFBurst.

$$\text{LFBurstExit} = \text{LFBurstEntry} \times \frac{(\text{LF Burst On Time} + \text{LF Burst Off Time})}{(\text{LF Burst On Time})} \quad (7)$$

$$\text{HFBurstExit} = \text{HFBurstEntry} \times \frac{(\text{HF Burst On Time} + \text{HF Burst Off Time})}{(\text{HF Burst On Time})} \quad (8)$$

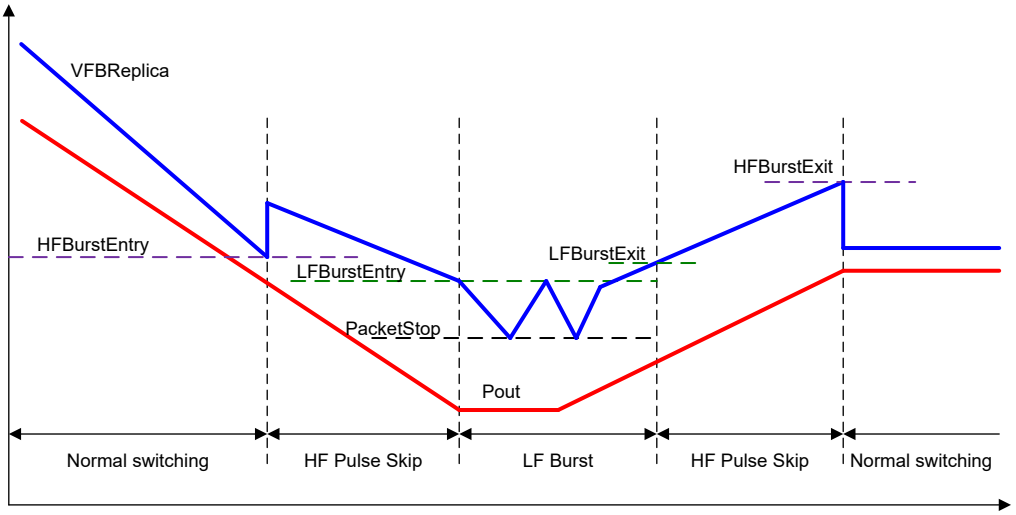

Figure 7-23. Burst Mode Determination from *FBReplica* Comparators

7.5.3.3 Burst Mode Thresholds Programming

Burst mode threshold programming is done by an external resistor divider connected between V5P and GNDP. Connect the center node of the external divider to LL pin. During the programming phase, a constant current I_{LLPrgm} is fed to the LL pin, and the resulting voltage is measured through ADC (V_{LLA}) at time T_{LLPrgm}. After T_{Prgm}, I_{LLPrgm} is turned off and the voltage of the LL resistor divider is measured (V_{LLB}).

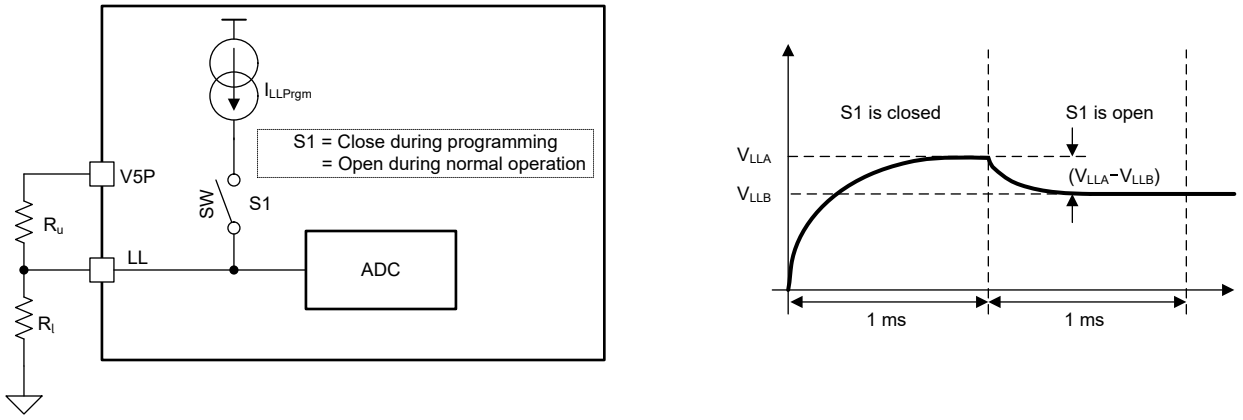

Figure 7-24. LL pin Programming

The voltage on the LL pin after switch S1 is turned off (V_{LLB}) is directly used to set the input power at which the system stops the LF Burst segment (*PacketStop* = V_{LLB}).

Determine the *FBReplica* voltage at which the controller enters HF Burst based on the measured V_{LLB} voltage and the difference in voltage between V_{LLA} and V_{LLB}. See the design calculator for more details.

The *FBReplica* at which the controllers starts the LF Burst segment is calculated using Equation 9.

$$\text{LFBurstEntry} = \text{PacketStop} \div 0.6 \quad (9)$$

HFBurstexit and *LFBurstexit* thresholds have hysteresis from *HFBurstentry* and *LFBurstentry* respectively. The two hystereses are not user defined parameters. These two hystereses are dynamically estimated internally based on the operating point of the converter.

Burst mode feature can be disabled by appropriately programming the (V_{LLA} - V_{LLB}).

Table 7-4. Burst Mode Externally Programmable Settings

(VLLA- VLLB) (V)	a = (PacketStop ÷ HFBurstEntry) RATIO	COMMENT
> 2.41	N/A	Burst disable
2.185	0.45	LF frequency range from 200Hz to 400Hz
1.754	0.50	LF frequency range from 200Hz to 400Hz
1.391	0.55	LF frequency range from 200Hz to 400Hz
1.087	0.60	LF frequency range from 200Hz to 400Hz
0.833	0.65	LF frequency range from 200Hz to 400Hz
0.617	0.70	LF frequency range from 200Hz to 400Hz
0.441	0.75	LF frequency range from 200Hz to 400Hz
0.176	0.80	LF frequency range from 200Hz to 400Hz

The ability to directly set the input power at which the system goes into various low power modes, dynamically disabling the burst mode enables an extra degree of freedom in the system design.

7.5.3.4 TSET Pin Alternate Function in Burst Mode

7.5.3.4.1 PFC On/Off

In UCC256614, the TSET pin can be used as PFC on/off logic. After the initial programming phase, TSET becomes a logic output pin expected to drive a small signal MOSFET (2N7002 for example). When UCC256614 operates in LF Burst mode, the PFC on/off signal goes high. TSET pin voltage goes low when the controller exits LF Burst mode. This can be used either turn-off the PFC or adjusting the burst mode threshold on the PFC controller to enable a low standby power mode.

7.5.3.4.2 Forced Burst-Mode

In UCC256610, the low frequency burst mode has a soft-on and soft-off wave shaping. This enables a low audible noise standby mode. Without forced burst-mode, as the load increases slightly the controller can frequently exit burst mode and resume normal switching operation, then frequently re-enter burst mode. This frequent mode jumping resulting from the additional soft-on and soft-off packets can increase audible noise.

To avoid this, in the UCC256610 the TSET pin functions as a input pin after startup. By pulling TSET low (to GND), the controller remains in the low frequency burst mode operation with soft-on and soft-off shaping of the burst packet. This enables a continued operation in low audible noise mode. Once the TSET pin is released from pull down, the controller resumes the operating mode based on the load condition.

7.5.3.5 Soft On/Off

When soft on/off is enabled, the 1st and the last two HF packets in the LF packet use lower voltage for the switching thresholds.

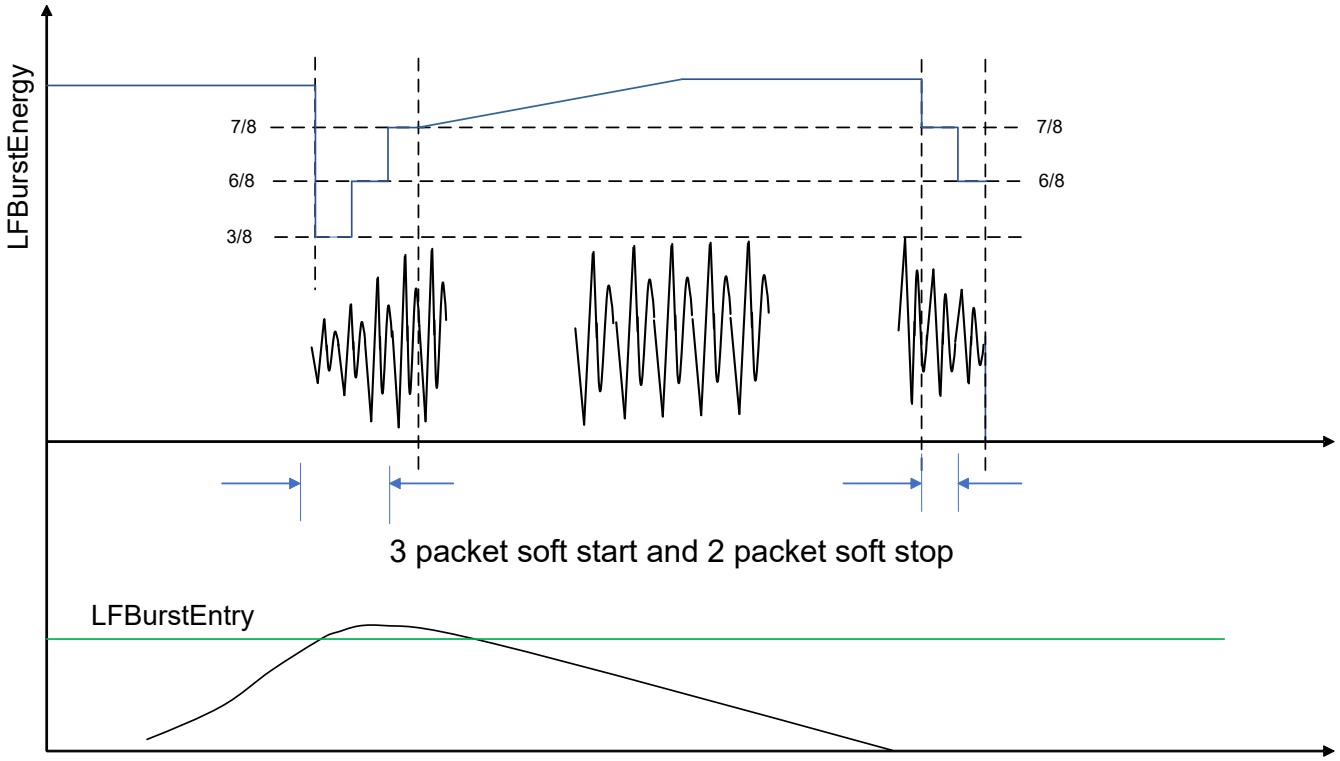

Figure 7-25. Low Frequency Burst packet with Soft-on and Soft-off

7.5.4 X-Capacitor Discharge

The HV pin is used for AC presence detection and X-Cap discharge.

7.5.4.1 Detecting Through HV Pin Only

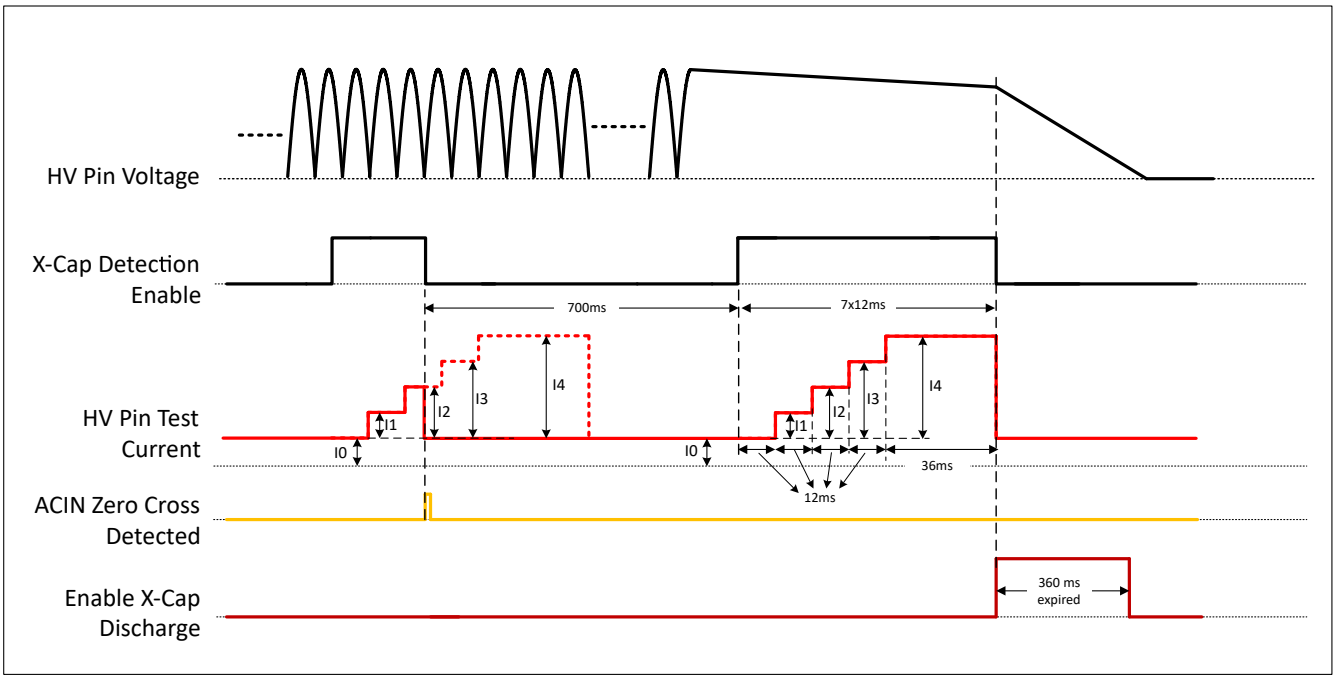

Figure 7-26. Zero Cross Detection Sequence HV Pin Only

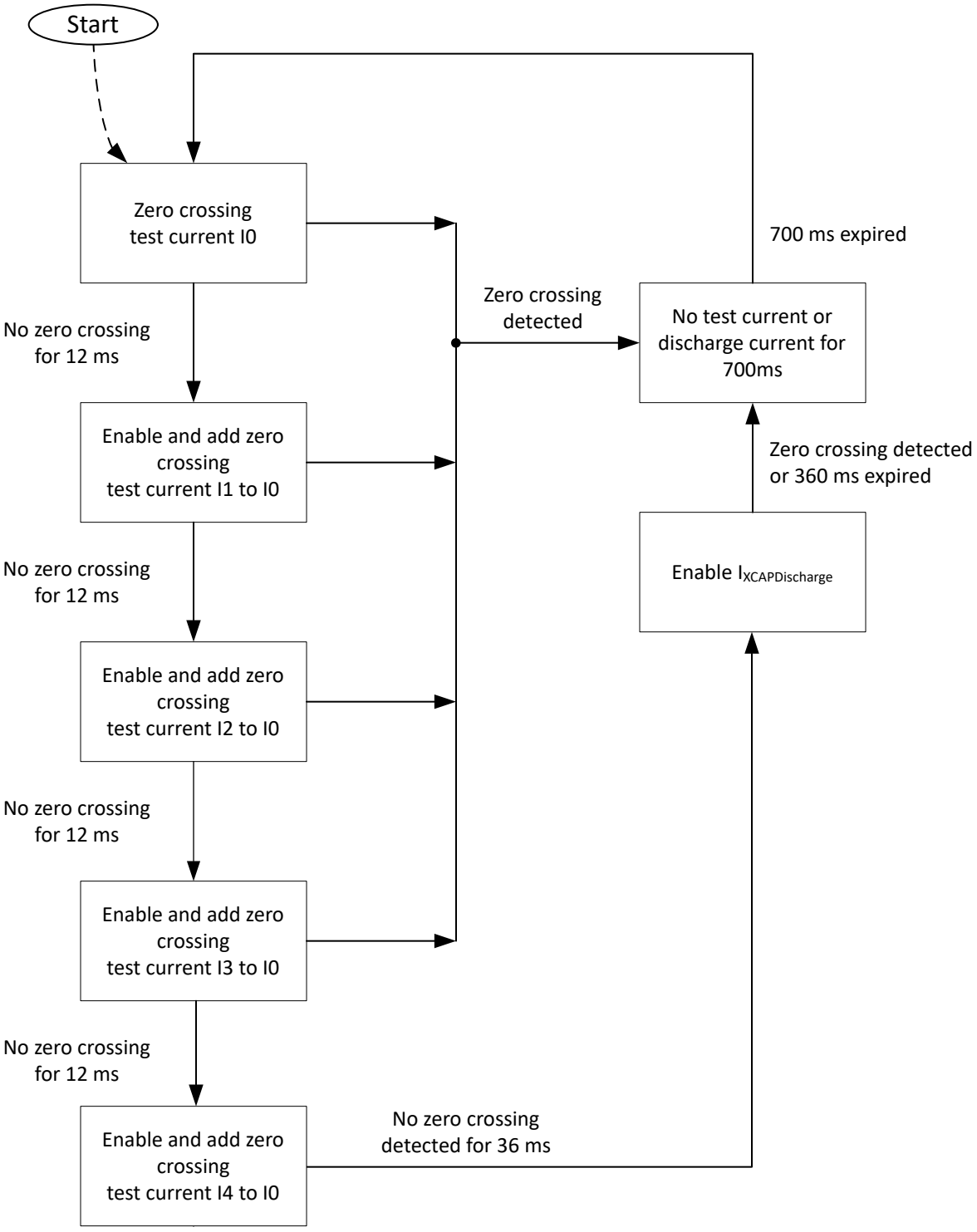

Figure 7-27. AC ZCD and X-Capacitor Discharge Flow Chart

1. Once every 700ms, the HV pin zero cross detection circuit gets engaged.
2. At first, HV pin test current is I0 and the duration is 12ms. HV pin voltage is checked to see if the voltage is less than 9V threshold
3. If HV pin voltage does not falls below 9V, add test current I1 to I0, and check again if HV pin voltage is less than 9V threshold
4. If HV pin voltage still not falls below 9V, continue to increase and add test current to I2 and then I3, I4 to I0.

5. The maximum on time for I4 test current is 36ms
6. If the HV pin voltage does not fall below 9V even after I4, the X-Cap discharge circuit is enabled for 360ms.
7. The minimal interval between two test current events is 700ms

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

Use the UCC25661x family in a wide range of applications that implement LLC topology. For ease of use, use the following list of materials to demonstrate the features of the device:

- Full featured EVM hardware
- An excel design calculator
- A Simplis model

In the following sections present a typical design example.

8.2 Typical Application

Figure 8-1 shows a typical half bridge LLC application using UCC256611 as the controller.

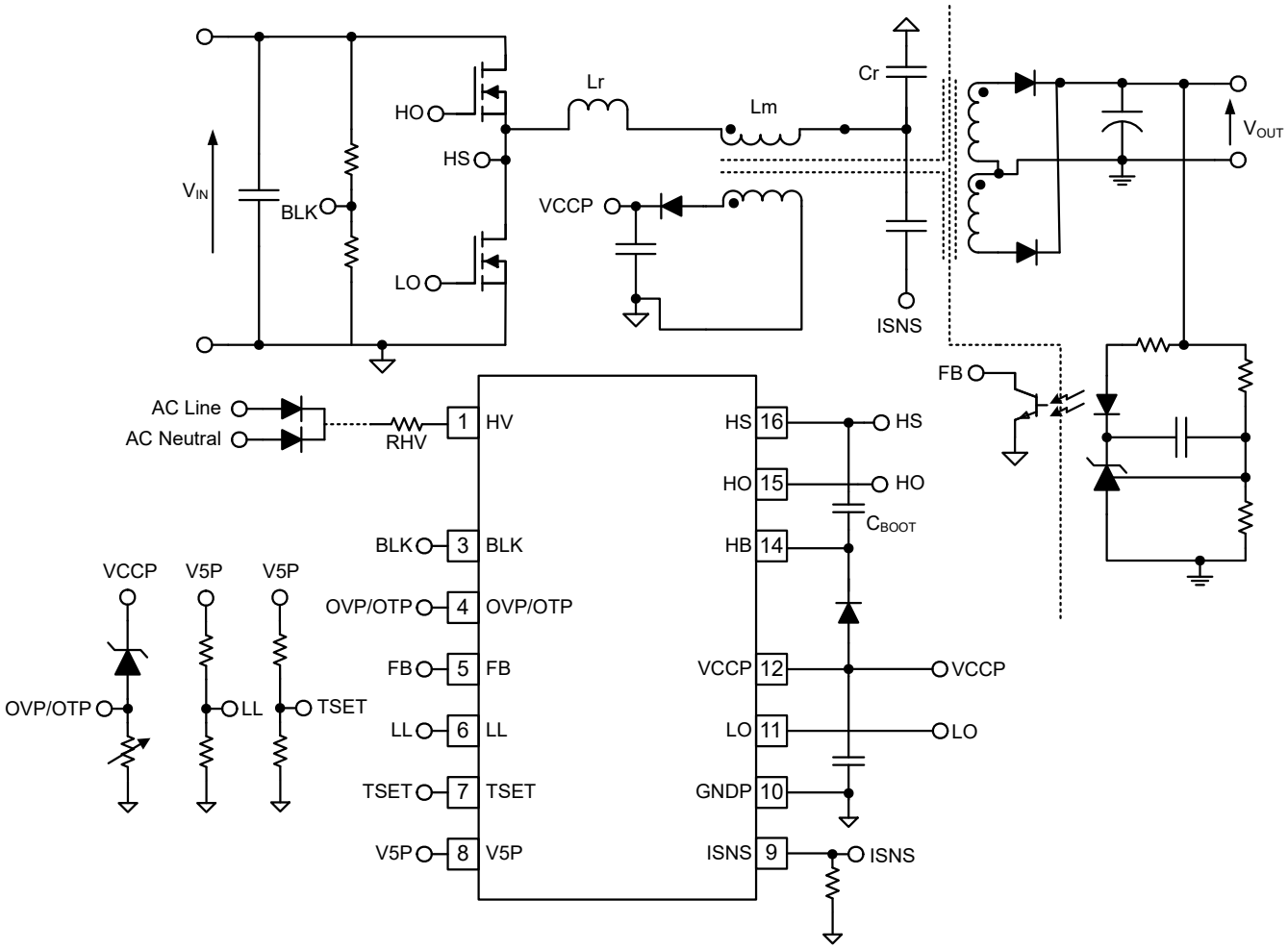

Figure 8-1. Typical Application Diagram

8.2.1 Design Requirements

The design specifications are summarized in Table 8-1.

Table 8-1. System Design Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS					
DC voltage range		365	390	410	VDC
AC voltage range		85		264	VAC
AC voltage frequency		47		63	Hz
Input DC UVLO on			365		VDC
Input DC UVLO off			315		VDC
OUTPUT CHARACTERISTICS					
Output voltage, VOUT	No load to full load		12		VDC
Output load current, IOUT	360VDC to 410VDC			15	A
Output voltage ripple	390VDC and full load = 15A		120		mVpp
SYSTEMS CHARACTERISTICS					
Resonant frequency			100		kHz
Peak efficiency	390VDC		92		
Operating temperature	Natural convection		25		°C

8.2.2 Detailed Design Procedure

8.2.2.1 LLC Power Stage Requirements

Start the design by setting the LLC power stage component values. The LLC power stage design procedure outlined here follows the one given in the *Designing an LLC Resonant Half-Bridge Power Converters* application note. The application note contains a full explanation of the origin of each of the equations used. The equations given below are based on the First Harmonic Approximation (FHA) method commonly used to analyze the LLC topology. This method gives a good starting point for any design, but a final design requires an iterative approach combining the FHA results, circuit simulation, and hardware testing. An alternative design approach is in the *LLC Design for UCC29950* application note.

8.2.2.2 LLC Gain Range

First, determine the transformer turns ratio by the nominal input and output voltages.

$$N_{PS} = \frac{V_{IN(nom)} \div 2}{V_{OUT(nom)}} = \frac{390 \div 2}{12} = 16.25 \Rightarrow 16.5 \tag{10}$$

Then determine the LLC gain range $M_{G(min)}$ and $M_{G(max)}$. Assume there is a 0.5V due to other losses (V_{loss}) and a 0.5V drop in the rectifier diodes (V_f) if a synchronous rectifier is not used.

$$M_{G(min)} = N_{PS}\frac{V_{OUT(min)} + V_f}{V_{IN(min)} \div 2} = 16.5\frac{12 + 0.5}{410 \div 2} = 1.006 \tag{11}$$

$$M_{G(max)} = N_{PS}\frac{V_{OUT(max)} + V_f + V_{loss}}{V_{IN(min)} \div 2} = 16.5\frac{12 + 0.5 + 0.5}{365 \div 2} = 1.175 \tag{12}$$

8.2.2.3 Select L_n and Q_e

L_N is the ratio between the magnetizing inductance and the resonant inductance.

$$L_N = \frac{L_M}{L_R} \tag{13}$$

Q_E is the quality factor of the resonant tank.

$$Q_E = \frac{\sqrt{L_R \div C_R}}{R_E} \quad (14)$$

In Equation 14, R_E is the equivalent load resistance.

Selecting L_N and Q_E values results in an LLC gain curve that intersects with $M_{G(min)}$ and $M_{G(max)}$ traces. The peak gain of the resulting curve is larger than $M_{G(max)}$. Details of how to select L_N and Q_E are not discussed here and are available in the design calculator.

The selected L_N and Q_E values are:

- L_N = 6
- Q_E = 0.3

8.2.2.4 Determine Equivalent Load Resistance

Determine the equivalent load resistance by Equation 15.

$$R_E = \frac{8 \times {N_{PS}}^2}{\pi^2} \times \frac{V_{OUT(nom)}}{I_{OUT(nom)}} = \frac{8 \times {16.5}^2}{\pi^2} \times \frac{12}{15} = 176.5\Omega \quad (15)$$

8.2.2.5 Determine Component Parameters for LLC Resonant Circuit

Before determining the resonant tank component parameters, select a nominal switching frequency (resonant frequency). In this design, 100kHz is selected as the resonant frequency.

- f_0 = 100kHz

Calculate the resonant tank parameters using Equation 16, Equation 17, and Equation 18.

$$C_R = \frac{1}{2\pi \times Q_E \times f_0 \times R_E} = \frac{1}{2\pi \times 0.3 \times 100\text{kHz} \times 176.5\Omega} = 30.0\text{nF} \quad (16)$$

$$L_R = \frac{1}{(2\pi \times f_0)^2 C_R} = \frac{1}{(2\pi \times 100\text{kHz})^2 \times 30.0\text{nF}} = 84.4\mu\text{H} \quad (17)$$

$$L_M = L_N \times L_R = 6 \times 84.4\mu\text{H} = 506.4\mu\text{H} \quad (18)$$

After selecting the preliminary parameters, find the closest actual component value that is available, and reassess the gain curve with the selected parameters, and then run time domain simulation to verify the circuit operation.

The following resonant tank parameters are:

$$C_R = 30\text{nF} \quad (19)$$

$$L_R = 85\mu\text{H} \quad (20)$$

$$L_M = 510\mu\text{H} \quad (21)$$

Based on the final resonant tank parameters, calculate the resonant frequency:

$$f_0 = \frac{1}{2\pi\sqrt{L_R C_R}} = \frac{1}{2\pi\sqrt{30\text{nF} \times 85\mu\text{H}}} = 99.7\text{kHz} \quad (22)$$

Based on the new LLC gain curve, the normalized switching frequency at maximum and minimum gain calculated using:

- $f_{N(Mgmax)}$ = 0.7
- $f_{N(Mgmin)}$ = 1.0

$$f_{N(Mgmax)} = 0.7 \quad (23)$$

$$f_{N(Mgmin)} = 1.0 \quad (24)$$

The maximum and minimum switching frequencies are:

$$f_{SW(Mgmax)} = 69.8\text{kHz} \quad (25)$$

$$f_{SW(Mgmin)} = 99.7\text{kHz} \quad (26)$$

8.2.2.6 LLC Primary-Side Currents

The primary-side currents are calculated for component selection purposes. The currents are calculated based on a 110% overload condition.

The primary side RMS load current are calculated using:

$$I_{OE} = \frac{\pi}{2\sqrt{2}} \times \frac{I_O}{n} = \frac{\pi}{2\sqrt{2}} \times \frac{1.1 \times 15\text{A}}{16.5} = 1.111\text{A} \quad (27)$$

The RMS magnetizing current at minimum switching frequency is calculated using:

$$I_M = \frac{\pi}{2\sqrt{2}} \times \frac{N_{PS} V_{OUT}}{\omega L_M} = \frac{\pi}{2\sqrt{2}} \times \frac{16.5 \times 12}{2\pi \times 64.8\text{kHz} \times 510\mu\text{H}} = 0.797\text{A} \quad (28)$$

The total current in resonant tank is calculated using:

$$I_R = \sqrt{{I_M}^2 + {I_{OE}}^2} = \sqrt{(1.111\text{A})^2 + (0.797\text{A})^2} = 1.367\text{A} \quad (29)$$

8.2.2.7 LLC Secondary-Side Currents

The total secondary side RMS load current is the current referred from the primary side current (I_{OE}) to the secondary side.

$$I_{OES} = N_{PS} \times I_{OE} = 16.5 \times 1.111\text{A} = 18.327\text{A} \quad (30)$$

In this design, the transformer secondary side has a center-tapped configuration. The current of each secondary transformer winding is calculated using:

$$I_{WS} = \frac{\sqrt{2} \times I_{OES}}{2} = \frac{\sqrt{2} \times 18.327\text{A}}{2} = 12.959\text{A} \quad (31)$$

The corresponding half-wave average current is:

$$I_{SAV} = \frac{\sqrt{2} \times I_{OES}}{\pi} = \frac{\sqrt{2} \times 18.327\text{A}}{\pi} = 8.250\text{A} \quad (32)$$

8.2.2.8 LLC Transformer

To maximize efficiency, use a bias winding to use the HV start-up function. Design the bias winding so that the VCCP voltage is greater than 12V.

Built or purchase the transformer according to these specifications:

- Turns ratio: Primary:Secondary:Bias = 33:2:3
- Primary terminal voltage: 450V_{pk}
- Primary magnetizing inductance: L_M = 510µH
- Primary side winding rated current: I_R = 1.367A
- Secondary terminal voltage: 36V_{pk}

- Secondary winding rated current: I_{WS} = 12.959A
- Minimum switching frequency: 69.8kHz
- Maximum switching frequency: 99.7kHz
- Insulation between primary and secondary sides: IEC60950 reinforced insulation

For some applications that operate at a wide input LLC where the PFC is potentially shut off in standby mode, the operating frequency can be lower during heavy load shutdown and the LLC operates at just above the ZCS boundary, which is a lower frequency. Rate the magnetic components in the resonant circuit, transformer inductor, and resonant inductor to operate at the lower frequency.

The bias voltage is obtained as 18V as per the turns ratio. To reduce the controller voltage to 15V, use a voltage regulator circuit like in the UCC25661EVM-128 before supplying to VCCP of the controller.

8.2.2.9 LLC Resonant Inductor

The AC voltage across the resonant inductor is calculated using AC voltage impedance multiplied by current:

$$V_{L_R} = \omega L_R I_R = 2\pi \times 69.8\text{kHz} \times 85\mu\text{H} \times 1.367\text{A} = 50.946\text{V} \quad (33)$$

Build or purchase the inductor according to the following specifications:

- Inductance: L_R = 85µH
- Rated current: I_R = 1.367A
- Terminal AC voltage: 50.946V
- Frequency range: 69.8kHz to 99.7kHz

Some designs use the leakage inductance of the transformer as the resonant inductance and do not require an external resonant inductor.

8.2.2.10 LLC Resonant Capacitor

The LLC resonant capacitor carries the full-primary current at the switching frequency. Use a low dissipation factor capacitor to prevent overheating.

The AC voltage across the resonant capacitor is calculated using the AC voltage impedance multiplied by the current.

$$V_{CR} = \frac{I_R}{\omega C_R} = \frac{1.367\text{A}}{2\pi \times 69.8\text{kHz} \times 30\text{nF}} = 104.0\text{V} \quad (34)$$

$$V_{CR(RMS)} = \sqrt{\left(\frac{V_{IN[max]}}{2}\right)^2 + {V_{CR}}^2} = \sqrt{\left(\frac{410}{2}\right)^2 + {104.0}^2} = 229.9\text{V} \quad (35)$$

Peak voltage:

$$V_{CR(peak)} = \frac{V_{IN(max)}}{2} + \sqrt{2}V_{CR} = \frac{410}{2} + \sqrt{2} \times 104.0 = 352.0\text{V} \quad (36)$$

Valley voltage:

$$V_{CR(valley)} = \frac{V_{IN(max)}}{2} - \sqrt{2}V_{CR} = \frac{410}{2} - \sqrt{2} \times 104.0 = 58.0\text{V} \quad (37)$$

Rated current:

$$I_R = 1.367\text{A} \quad (38)$$

8.2.2.11 LLC Primary-Side MOSFETs

Each MOSFET sees the input voltage as the maximum applied voltage. Set the MOSFET voltage rating as 1.5 times of the maximum bulk voltage:

$$V_{QLLC(peak)} = 1.5 \times V_{IN(max)} = 615V \quad (39)$$

Set the MOSFET current rating as 1.1 times of the maximum primary side RMS current:

$$I_{QLLC} = 1.1 \times I_R = 1.504A \quad (40)$$

8.2.2.12 Design Considerations for Adaptive Dead-Time

After designing the resonant tank and selecting the primary side MOSFET, double-check the ZVS operation of the converter. ZVS is only achieved when there is enough energy left in the resonant inductor at the gate turn off edge to discharge the switch node capacitance or LI^2 is greater than C_{OSS} V^2. C_{OSS} is the effective drain to source capacitance of the two switch-stage MOSFETs. UCC25661 implements adaptive dead-time based on the slewing of the switch node. The slew detection circuit has a detection range from 0.1V/ns to 200V/ns.

To check the ZVS operation, the controller conducts a series of time domain simulations, and the resonant current at the gate turn off edges are captured as shown in Figure 8-2.

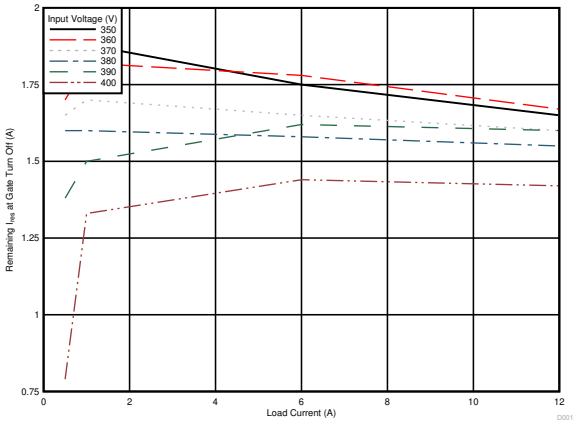

Figure 8-2. Adaptive Dead-Time

Figure 8-2 above assumes the maximum switching frequency occurs at 5% load and the system starts to burst at 5% load.

Using Figure 8-2, the minimum resonant current left in the tank is I_{min} = 0.8A, in the operation range of interest. Know the primary side switch node parasitic capacitance to calculate the slew rate. Estimate the slew rate from the value of C_{OSS} given in the MOSFET data sheet. In this case, the total $C_{switchnode}$ = 400pF because each MOSFET has 200pF. The minimum slew rate is calculated using:

$$\frac{I_{MIN}}{C_{switchnode}} = \frac{0.8A}{400pF} = 2V/ns \quad (41)$$

8.2.2.13 LLC Rectifier Diodes

The voltage rating of the output diodes is calculated using:

$$V_{DD} = 1.2 \times \frac{V_{IN(max)}}{N_{PS}} = 1.2 \times \frac{410}{16.5} = 29.82V \quad (42)$$

The current rating of the output diodes is calculated using:

$$I_{SAV} = \frac{\sqrt{2} \times I_{OES}}{\pi} = \frac{\sqrt{2} \times 18.329}{\pi} = 8.250A \quad (43)$$

8.2.2.14 LLC Output Capacitors

The LLC converter topology does not require an output filter. Use a small second stage filter inductor to reduce peak-to-peak output ripple. Assuming that the output capacitors carry the full wave output current of the rectifier, the capacitor ripple current rating is:

$$I_{RECT} = \frac{\pi}{2\sqrt{2}} I_{OUT} = \frac{\pi}{2\sqrt{2}} \times 15 = 16.66A \quad (44)$$

Use a 20V rating for a 12V output voltage:

$$V_{LLCcap} = 20V \quad (45)$$

The capacitor RMS current rating is:

$$I_{C(out)} = \sqrt{\left(\frac{\pi}{2\sqrt{2}} I_{OUT}\right)^2 - {I_{OUT}}^2} = \sqrt{\left(\frac{\pi}{2\sqrt{2}} \times 15\right)^2 - 15^2} = 7.251A \quad (46)$$

Solid aluminum capacitors with conductive polymer technology have high ripple-current ratings and are a good choice, especially if the design is required to operate at colder temperatures. Connect multiple capacitors in parallel if the ripple-current rating for a single capacitor is insufficient.

The ripple voltage at the output of the LLC stage is a function of the amount of AC current that flows in the capacitors. To estimate the ripple voltage, assume that all the current, including the DC current in the load, flows in the filter capacitors.

$$ESR_{max} = \frac{V_{OUT(pk-pk)}}{I_{RECT(pk)}} = \frac{0.12v}{2\frac{\pi}{4} \times 15A} = 5.1m\Omega \quad (47)$$

The capacitor specifications are:

- Voltage rating: 20V
- Ripple current rating: 7.251A
- Effective ESR: < 5.1mΩ

8.2.2.15 HV Pin Series Resistors

Multiple resistors are connected in series with HV pin to limit the power dissipation of each resistor. The typical series resistor with HV pin is 5kΩ, optimization of series resistor value for each application will be necessary. For example, choose a higher value of series resistor when using a higher bus voltage.

8.2.2.16 BLK Pin Voltage Divider

BLK pin senses the LLC DC input voltage and determines when to turn on and off the LLC converter. Also, BLK pin voltage is used for feedforward compensation.

The power budget of the BLK pin resistor divider for UCC25661EVM-128 is 15mW. The BLK sense resistor total value is calculated using:

$$R_{BLKsns} = R_{BLKupper} + R_{BLKlower} = \frac{{V_{IN(nom)}}^2}{P_{BLKsns}} = \frac{390^2}{0.015} = 10M\Omega \quad (48)$$

Choose LLC start-up voltage as 365V. Then $V_{BLKStart}$ related to $V_{BLKStop}$, $V_{BLKStartHys}$, $I_{BLKSink}$ as below:

$$V_{BLKStart} = 365\left(\frac{R_{BLKlower}}{R_{BLKupper} + R_{BLKlower}}\right) = V_{BLKStop} + V_{BLKStartHys} + I_{BLKsink}\left(\frac{R_{BLKupper}R_{BLKlower}}{R_{BLKupper} + R_{BLKlower}}\right) \quad (49)$$

For $V_{BLKStop}$= 1V, $V_{BLKStartHys}$= 0.1V, $I_{BLKSink}$= 5µA, $R_{BLKupper}$ is 10MΩ and $R_{BLKlower}$ is 35.4kΩ.

A standard value of 35.4kΩ is selected for $R_{BLKlower}$ and a standard value of ×3 3.3MΩ in series is selected for $R_{BLKupper}$.

The actual start-up voltage is calculated using

$$\begin{aligned} V_{BLKStart}\left[\frac{R_{BLKupper}+R_{BLKlower}}{R_{BLKlower}}\right] \\ = \left[V_{BLKStop}+V_{BLKStartHys}+I_{BLKSink}\left(\frac{R_{BLKupper}R_{BLKlower}}{R_{BLKupper}+R_{BLKlower}}\right)\right]\times\left[\frac{R_{BLKupper}+R_{BLKlower}}{R_{BLKlower}}\right] \\ = 358V \end{aligned} \quad (50)$$

The power consumption in BLK resistors are calculated using

$$P_{BLKsns}=\frac{V_{IN(nom)}{}^2}{\left(R_{BLKupper}+R_{BLKlower}\right)}=\frac{390^2}{(10M\Omega+35.4k\Omega)}=15.3mW \quad (51)$$

The LLC turn off voltage is calculated using

$$V_{BLKStop}\left(\frac{R_{BLKupper}+R_{BLKlower}}{R_{BLKlower}}\right)=280.6V \quad (52)$$

8.2.2.17 ISNS Pin Differentiator

The ISNS pin senses the resonant current through a Differentiator. The ISNS pin together with TSET, BLK pin resistors set the overload protection level. The typical threshold voltage of overload protection (V_{FBOLP}) is 4.75V. The ISNS pin also sets the over current protection level (OCP1). The threshold value of OCP1 is either 3.5V or 4V depending on the TSET pin resistors and the variant being used. For the EVM, UCC256611 is being used. So, for this variant, OCP1 threshold value is 3.5V.

The peak resonant inductor current at full load

$$I_{R\_PEAK}=\sqrt{2}I_R=\sqrt{2}\times1.367=1.933A \quad (53)$$

Select a current sense capacitor first, since there are less high voltage capacitor choices than resistors:

$$C_{ISNS}=150pF \quad (54)$$

For this design, UCC256611 is being used. So, for this variant, OCP1 threshold value is 3.5V.

$$OCP1\_Threshold=3.5V \quad (55)$$

Then calculate the required ISNS resistor value:

$$R_{ISNS}<\frac{OCP1\_Threshold\cdot C_r}{I_{R\_PEAK}\cdot C_{ISNS}}=\frac{3.5V\cdot30nF}{1.933A\cdot150pF}=329\Omega \quad (56)$$

$$R_{ISNS}=226\Omega \quad (57)$$

Equation 57 is selected.

The peak resonant current at OCP1 level is calculated using:

$$I_{R\_PEAK\_OCP1}=\frac{OCP1\_Threshold\times C_r}{R_{ISNS}\times C_{ISNS}}=\frac{3.5\times30nF}{226\times150pF}=3.097A \quad (58)$$

8.2.2.18 TSET Pin

The TSET pin resistors set the VCR integrator time constants (Timer gain [k_s] , R_{VCR}, R_{RAMP}, C_{VCR}) and the minimum switching frequency in IPPC mode. The TSET pin resistors also determine the $V_{FBreplica}$ voltage for a given output power.

The following information is for devices with *OCP/OLP decoupling* enabled.

Choose V_{TSETB} voltage option based on $f_{SW(Mgmin)}$ and the full load operating frequency at the minimum input voltage and maximum output power. For this design, option 4 is selected in the design calculator because the observed full load operating frequency is 89kHz at the minimum input voltage of 365V and at the rated output power. For option #4, V_{TSETB} voltage must be between 0.742V and 48mV, as provided in Table 7-1.

Choose (V_{TSETA}-V_{TSETB}) voltage to set the FBReplica magnitude for a given power output. Choose the difference voltage so that, at maximum output power, the FBReplica magnitude is below V_{FBOLP}, as shown in Figure 8-3 with the required margin as the worst case. For this design, option #5 is selected from the Table 7-1 table so that VCR integrator time constants along with chosen ISNS and BLK resistors makes the FBReplica magnitude close to 4V at the maximum input power and set the (V_{TSETA}-V_{TSETB}) voltage between 0.850V and 48mV.Table 7-1.

$$V_{TSETB} = \frac{R_{TSET\_lower} \cdot V5P}{R_{TSET\_lower} + R_{TSET\_upper}} \tag{59}$$

$$V_{TSETA} = V_{TSETB} + \frac{R_{TSET\_lower} \cdot R_{TSET\_upper}}{R_{TSET\_lower} + R_{TSET\_upper}} \cdot I_{TSETPrgm} \tag{60}$$

By solving Equation 59 and Equation 60, R_{TSET_upper} is 572.78kΩ and R_{TSET_lower} is 99.81kΩ.

Finally, R_{TSET_upper} = 576kΩ and R_{TSET_lower} = 100kΩ are chosen.

Final V_{TSETB} and (V_{TSETA}-V_{TSETB}) are calculated using Equation 61 and Equation 62:

$$V_{TSETB} = \frac{100k \cdot 5V}{100k + 576k} = 0.74V \tag{61}$$

$$\left(V_{TSETA} - V_{TSETB}\right) = \frac{100k \cdot 576k}{100k + 576k} \cdot 10\mu A = 0.852V \tag{62}$$

Figure 8-3 shows the FBReplica voltage regarding the input power of the LLC.

To calculate P_{in}, 92% efficiency is used in the following equation.

$$P_{in} = \frac{P_{out}}{\eta} \tag{63}$$

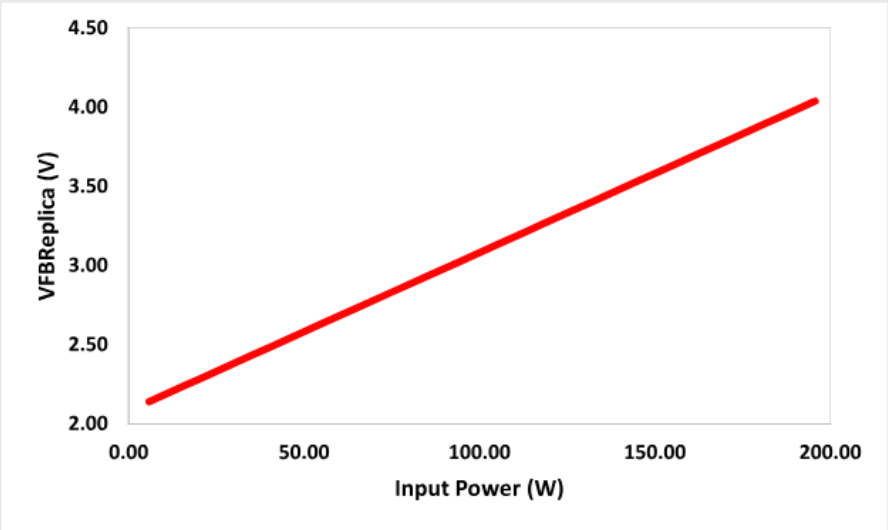

Figure 8-3. FBReplica versus P_{in}

Measure the FBReplica voltage by inserting a 10kΩ resistor between the feedback optocoupler emitter and ground. Assume the voltage measured on the 10kΩ resistor is V_{10k}. Use Equation 64 to calculate the FBReplica voltage:

$$\mathrm{FBReplica} = \left(I_{FB} - \frac{V_{10k\Omega}}{10k\Omega}\right) \times R_{FBInternal} \tag{64}$$

8.2.2.19 OVP/OTP Pin

The OVP/OTP pin is used to protect the power stage from overvoltage. The OVP/OTP pin is used for over temperature protection using negative temperature coefficient (NTC) thermistor. As the bias winding voltage is the mirror image of the output voltage through the turns ratio of the transformer, pulling up the pin with a zener diode is a convenient approach to set the OVP on the primary side. In this design, the nominal output voltage is 12V. The bias winding to the secondary side winding turns ratio is 1.5, based on the ration of the output voltage and recommended bias voltage. If rectifier diodes are present, assume there is a 0.5V drop (Vf). If synchronous rectification is used, only a 0.5V drop due to other losses (Vloss) can be estimated, so the nominal voltage of the bias winding is calculated using:

$$V_{BiasWindingNom} = (12 + 0.5 + 0.5) \times \frac{N_{aux}}{N_2} = (12 + 0.5 + 0.5) \times \frac{3}{2} = 19.5V \tag{65}$$

The desired OVP threshold in this design is 140% of the nominal value. The OVP threshold level (V_{OVPpos}) in UC25661 device is 3.5V. The required voltage rating of the Zener diode is calculated using:

$$V_z = (1.4 \times V_{out} + V_{drop}) \times \frac{N_{aux}}{N_2} - V_{OVPpos} = (1.4 \times 12 + 0.5 + 0.5) \times \frac{3}{2} - 3.5 = 23.2V \tag{66}$$

Assume actual voltage rating of Zener used is 23V. The actual output voltage at which OVP is triggered is:

$$V_{out\_ovp} = (V_z + V_{OVPpos}) \times \frac{N_2}{N_{aux}} - V_{drop} = (23 + 3.5) \times \frac{2}{3} - 1 = 16.67V = 139\% \times V_{out} \tag{67}$$

During normal operation, the standard voltage of the OVP/OTP pin is within the working window of 0.8V to 3.5V. For over temperature protection, pull down the OVP/OTP pin below OTP threshold of 0.8V. At room temperature, the OVP/OTP pin voltage is considered as 1.4V. At room temperature, the effective resistance value at this pin is:

$$R_{OVP/OTP\_25} = \frac{1.4V}{I_{OVP\_OTP}} = \frac{1.4V}{100 \times 10^{-6}A} = 14k\Omega \quad (68)$$

$$R_{OVP/OTP\_25} = \frac{R_{ext} \times R_{NTC\_25}}{R_{ext} + R_{NTC\_25}} = 14k\Omega \quad (69)$$

R_{ext} is external resistor that is in parallel with the thermistor. R_{NTC_25} is resistance value of the thermistor at the room temperature.

For this design, over temperature protection is set at the 110°C. Based on the availability and temperature coefficient of NTCs, choose Equation 70.

$$\frac{R_{NTC\_110}}{R_{NTC\_25}} = 0.035263 \quad (70)$$

Refer to the B57371V2474J060 data sheet. Here, R_{NTC_110} is the resistance of the thermistor at the 110°C.

For OTP trigger, verify that the OVP/OTP pin voltage is below 0.8V.

$$R_{OVP/OTP\_110} = \frac{0.8V}{I_{OVP\_OTP}} = \frac{0.8V}{100 \times 10^{-6}A} = 8k\Omega \quad (71)$$

$$R_{OVP/OTP\_110} = \frac{R_{ext} \times R_{NTC\_110}}{R_{ext} + R_{NTC\_110}} = 8k\Omega \quad (72)$$

From Equation 69, Equation 70, and Equation 72, R_{NTC_25} is 510kΩ and R_{ext} is 14.4kΩ. R_{NTC_25} = 470kΩ (manufacturer part number: B57371V2474J060) and R_{ext}=15kΩ are chosen.

At room temperature, with new chosen resistors, the OVP/OTP voltage is calculated using:

$$R_{OVP/OTP\_25} \times I_{OVP\_OTP} = \left(\frac{15k \times 470k}{15k + 470k}\right) \times 100 \times 10^{-6} = 1.454V \quad (73)$$

At 110^0C, the OVP/OTP voltage is calculated using:

$$R_{OVP/OTP\_110} \times I_{OVP\_OTP} = \left(\frac{15k \times (470k \times 0.035263)}{15k + (470k \times 0.035263)}\right) \times 100 \times 10^{-6} = 0.78V \quad (74)$$

8.2.2.20 Burst Mode Programming

The LL pin voltage (VLLB) and the resistor divider that connects to the LL pin allow the user to set the HFBurstEntry and LFBurstEntry thresholds as shown below.

$$VLLB = \frac{R_{LL\_lower} \cdot V5P}{R_{LL\_upper} + R_{LL\_lower}} \quad (75)$$

$$VLLA = VLLB + \frac{R_{LL\_lower}R_{LL\_upper}}{R_{LL\_upper} + R_{LL\_lower}} \cdot I_{LLPrgm} \quad (76)$$

As shown in Table 7-1, (V_{LLA} – V_{LLB}) voltage determines the V_{LLB}/HFBurstEntry ratio

For this design, (V_{LLB}/HFBurstEntry) = 0.55 is considered. Confirm that the (V_{LLA}-V_{LLB}) value is between 1.087V and 1.391V.

Then HFBurstEntry is related to LL pin voltage as below:

$$HFBurstEntry = \frac{VLLB}{0.55} = 1.818 \cdot VLLB \quad (77)$$

The LFBurstEntry is always related to LL pin voltage as below:

$$\text{LFBurstEntry} = \frac{\text{VLLB}}{0.6} = 1.667 \cdot \text{VLLB} \quad (78)$$

Based on curve and hardware testing, adjust V_{LLB} and (V_{LLA} – V_{LLB}) to meet the desired performance.

For this design, VLLB = 1.2V and VLLA = (Max voltage of (VLLA – VLLB)) – 0.1V are considered. By substituting these values in Equation 75, Equation 76, $R_{LLupper}$ is 538k and $R_{LLlower}$ is 170k.

Finally $R_{LLupper}$ = 536kΩ and $R_{LLlower}$ = 169kΩ are chosen for this design.

The final burst entries are calculated as:

$$\text{VLLB} = \frac{169\text{k} \cdot 5}{169\text{k} + 536\text{k}} = 1.199\text{V} \quad (79)$$

$$\text{VLLA} = 1.199\text{V} + \frac{169\text{k} \cdot 536\text{k}}{169\text{k} + 536\text{k}} \cdot 10\mu\text{A} = 2.483\text{V} \quad (80)$$

$$\text{VLLA} - \text{VLLB} = 1.285\text{V} \quad (81)$$

$$\text{HFBurstEntry} = 1.818 \cdot 1.199 = 2.179\text{V} \quad (82)$$

$$\text{LFBurstEntry} = 1.667 \cdot 1.199 = 1.998\text{V} \quad (83)$$

8.2.3 Application Curves

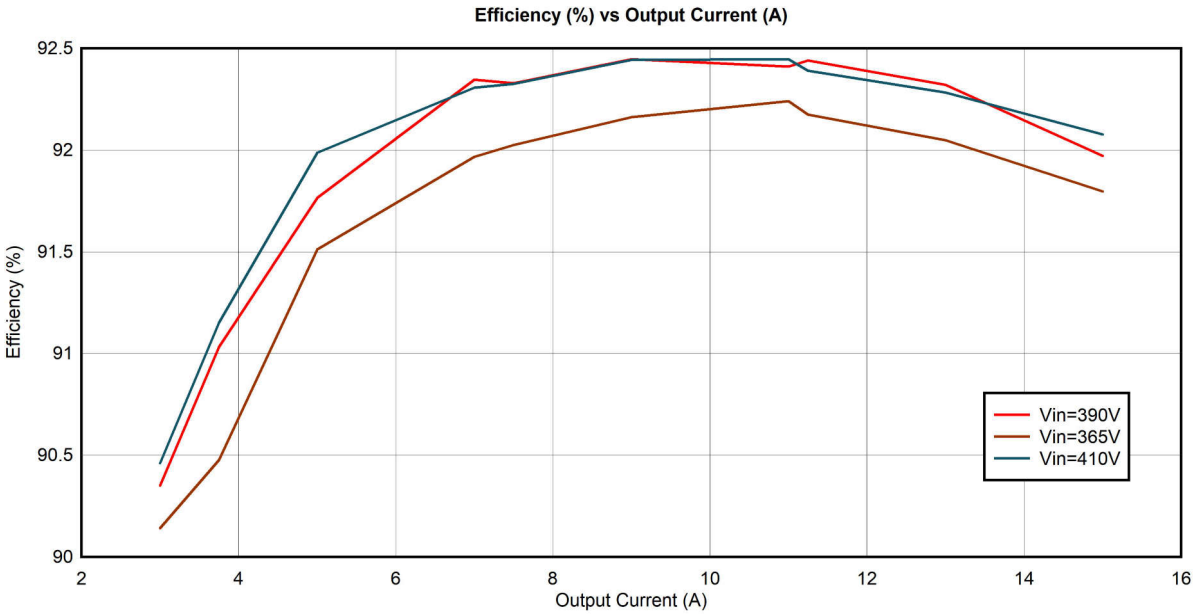

Figure 8-4. Efficiency

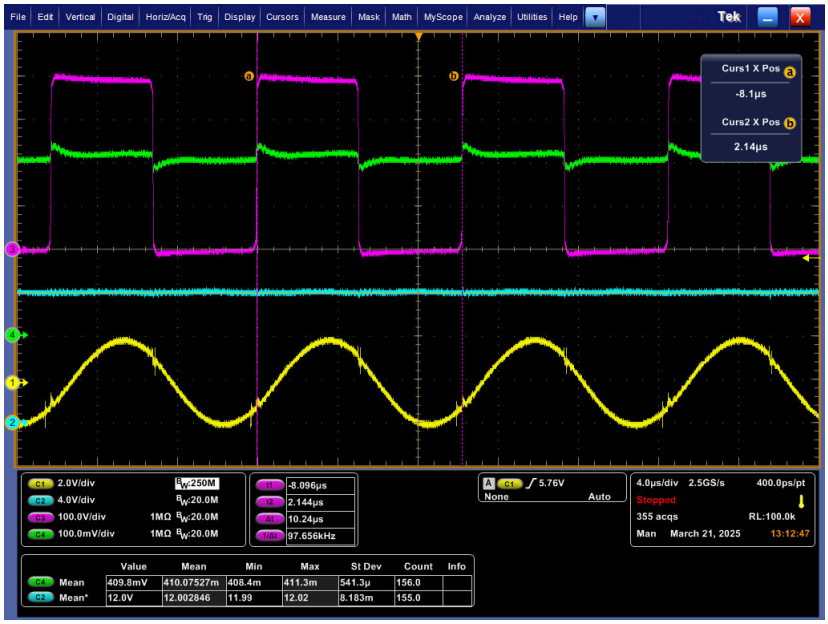

Figure 8-5. Steady State Waveforms at 15A Load at 390V Input (Ch1= ISNS; Ch2 = Vout; Ch3 = SW; Ch4 = I_OPT)

8.3 Power Supply Recommendations

8.3.1 VCCP Pin Capacitor

Select the VCCP capacitor with a value high enough for support during the LF Burst operation making sure VCCP does not fall below the $VCC_{StopSwitching}$ level.

Choose a capacitor or a combination of capacitors that provide at least 100µF capacitance. Verify that the capacitors on VCCP pin support the quiescent current during LF burst operation, as well as low impedance path for high frequency currents on VCCP. Consider derating of ceramic capacitors with DC-bias voltage using the manufacturer data sheet while selecting capacitors.

8.3.2 Boot Capacitor

During LF burst off period, power consumed by the high-side gate driver from the HB pin must be drawn from C_{BOOT} and causes the bootstrap capacitor voltage to decay. At the start of the next burst period there must be sufficient voltage remaining on C_{BOOT} to power the high-side gate driver (HO) until the conduction period of the low-side gate driver (LO) allows it to be replenished from C_{VCCP}. The power consumed by the high-side driver during this burst off period will therefore have a direct impact on the size and cost of capacitors that must be connected to HB and VCCP.

Assume the system has a maximum burst off period of 150ms and the bootstrap diode has a forward voltage drop of 1V. Target a minimum bootstrap voltage of 8V to avoid UVLO fault. The maximum allowable voltage drop on the boot capacitor is:

$$V_{bootmaxdrop} = V_{VCCP} - V_{bootforwarddrop} - 8V = 12V - 1V - 8V = 3V \quad (84)$$

Boot capacitor can then be sized:

$$C_B = \frac{I_{BOOT\_QUIESCENT}}{V_{bootmaxdrop}} = \frac{60\mu A \times 150ms}{3V} = 3uF \quad (85)$$

Choose a low leakage, low-ESR ceramic capacitor. Derating of ceramic capacitors with DC-bias voltage must be considered using the manufacturer data sheet while selecting the capacitors.

8.3.3 V5P Pin Capacitor

Verify that the V5P pin is connected to a decoupling capacitor to GND. Because the load on this pin is very small, a small decoupling capacitor between 0.1µF and 4.7µF is recommended.

8.4 Layout

8.4.1 Layout Guidelines

- Connect a 2.2µF ceramic capacitor on VCCP pin in addition to the energy storage electrolytic capacitor. Place the 2.2µF ceramic capacitor as close as possible to the VCCP pin.
- Add necessary filtering capacitors on the VCCP pin to filter out the high spikes on the bias winding waveform.
- Minimum recommended boot capacitor, C_B, is 0.1µF. Please calculate as described in section 8.3.2 and refer to the I_{BOOT_LEAK} (boot leakage current) in the electrical table.
- It's recommended to connect signal ground and power ground at single-point. Power ground is recommended to connect to the negative terminal of the LLC converter input bulk capacitor.
- Place the filter capacitors for ISNS (100pF), BLK (10nF), LL(330pF), TSET (220pF), OVP/OTP(100pF) as close as possible to the respective pins.
- Keep the FB trace as short as possible and route the FB trace away from high dv/dt traces.
- Use film capacitors or C0G, NP0 ceramic capacitors for the ISNS capacitor for low distortion
- Keep necessary high voltage clearance and creepage.
- If 2kV HBM ESD rating is needed on HV pin, place a 100pF capacitor from the HV pin to ground to pass up to 2kV HBM ESD.

8.4.2 Layout Example

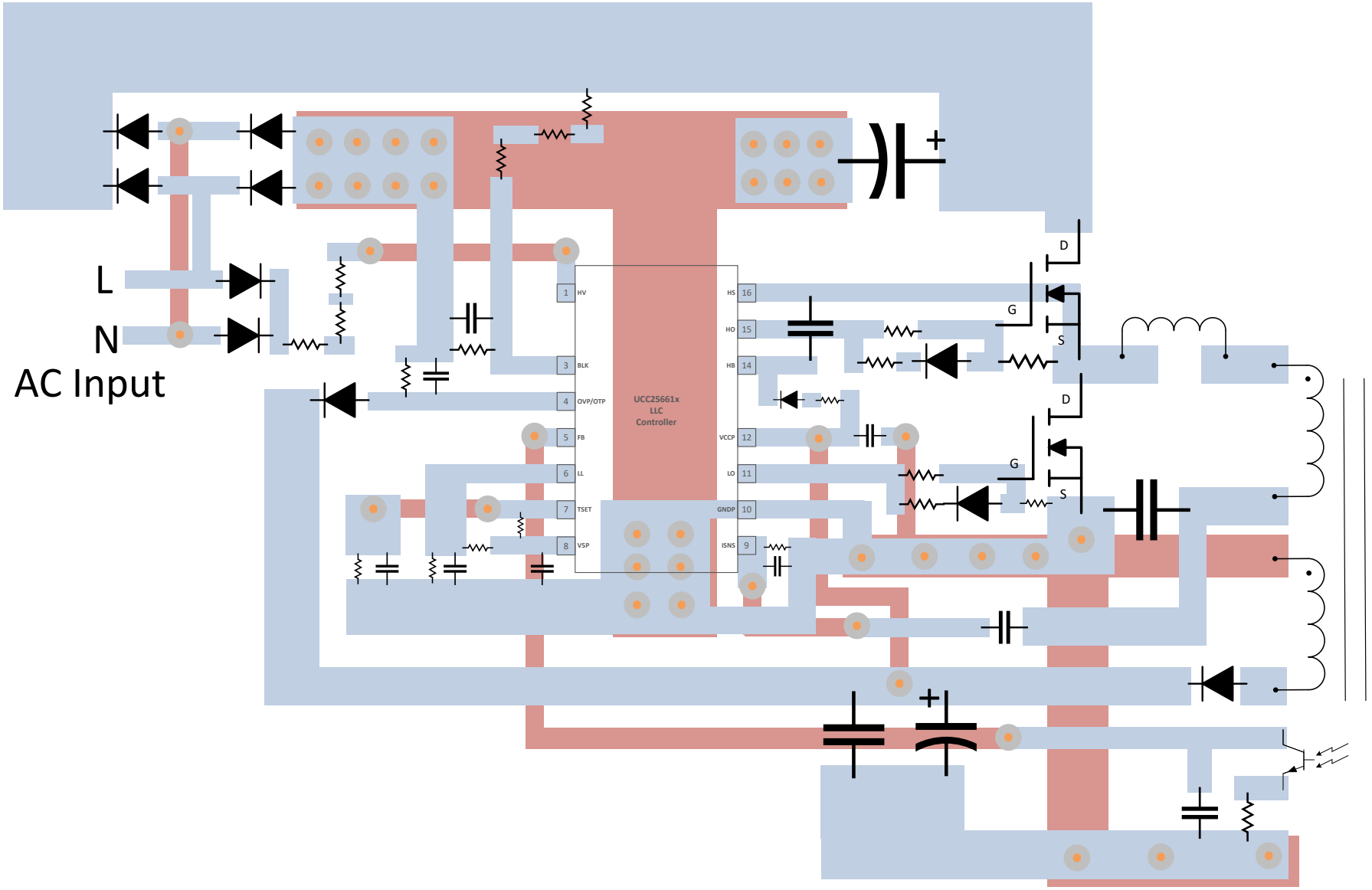

Figure 8-6. UCC25661x Layout Example for 2 layer board

8.4.2.1 Schematics

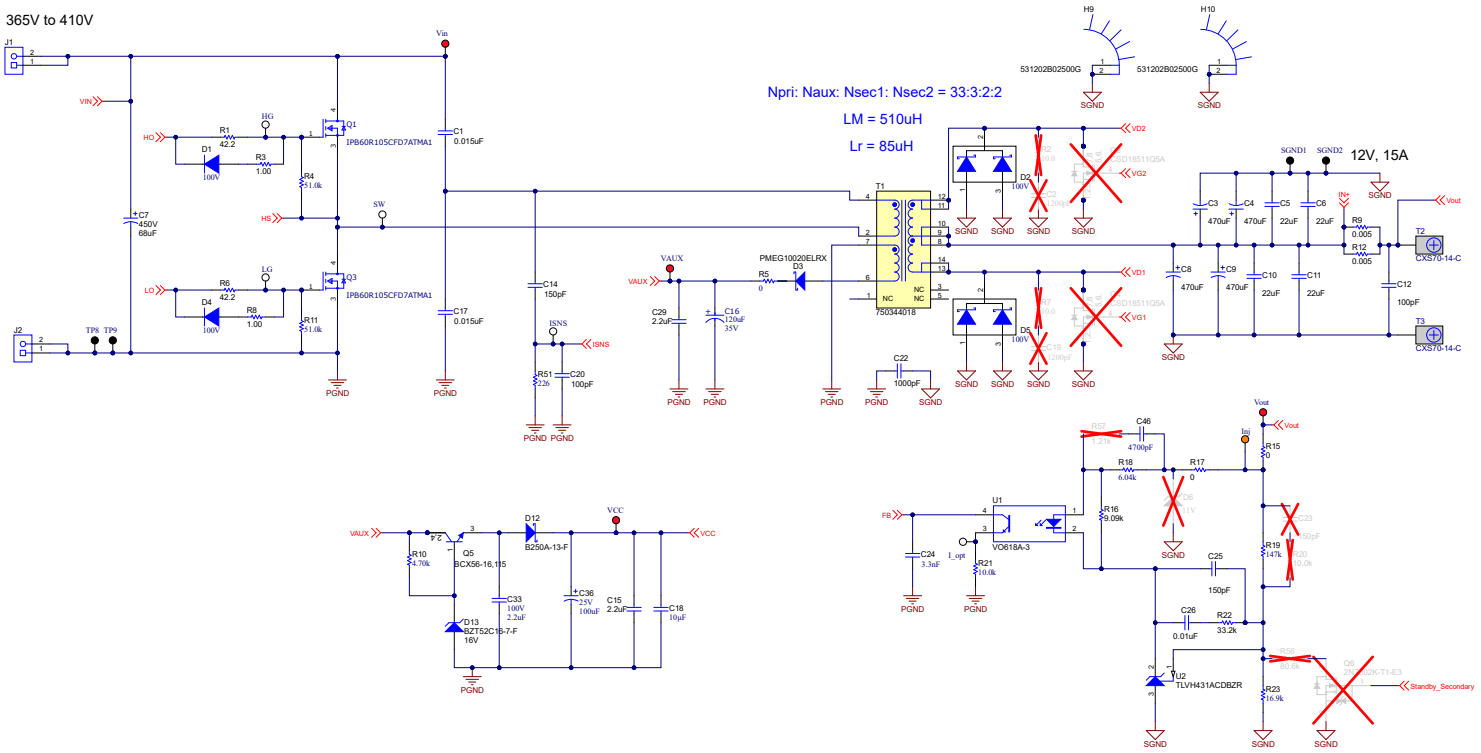

Figure 8-7. UCC25661EVM-128 Power Stage Schematic

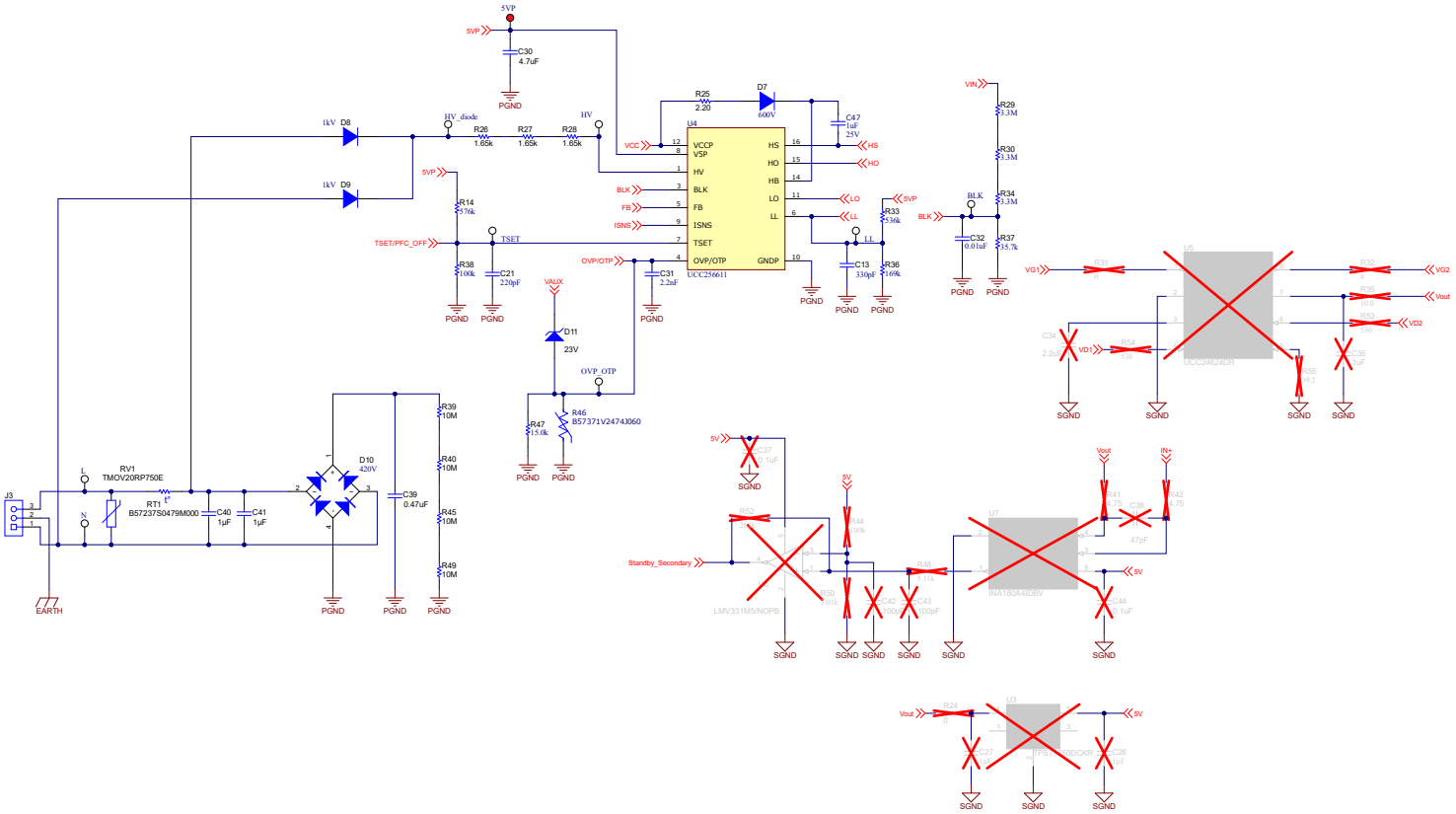

Figure 8-8. UCC25661EVM-128 Control Schematic

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

- TDK Electronics, *NTC thermistors for temperature measurement*
- Texas Instruments, *LLC Design for UCC29950* application note

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (January 2026) to Revision C (August 2026)	Page
• Updated Extended Gain Range device from UCC256611 to UCC256610	1
• Updated *Device Comparison* table	3
• Updated *TSET Programming* section to split Table 7-1	21

Changes from Revision A (September 2025) to Revision B (January 2026)	Page
• Updated the numbering format for tables, figures, equations, and cross-references throughout the document	1
• Added *X-capacitor discharge* and *Extended Gain Range* to features section	1
• Changed from: UCC25661 to: UCC25661x Family throughout the document	1
• Updated *Device Comparison* table	3
• Added UCC256611, UCC256612, UCC256613, UCC256614, and UCC256616, orderable options to the specification tables	6
• Added *Benefits of Extended gain range (EGR)* to detailed description overview	16

- Added *EGR information* in VCR Synthesizer section.....20
- Added *TSET Programming for UCC256616* section.....22
- Added *TSET Pin Alternate Function in Burst Mode*, *PFC On/Off*, *TSET-Enforced Low audible noise standby mode*, *X-Capacitor Discharge*, and *Detecting Through HV Pin Only* sections.....37

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/Ball material (4)	MSL rating/Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC256610DDBR	Active	Production	SOIC (DDB) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC256610
UCC256611DDBR	Active	Production	SOIC (DDB) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC256611
UCC256612DDBR	Active	Production	SOIC (DDB) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC256612
UCC256613DDBR	Active	Production	SOIC (DDB) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC256613
UCC256614DDBR	Active	Production	SOIC (DDB) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC256614
UCC256616DDBR	Active	Production	SOIC (DDB) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC256616

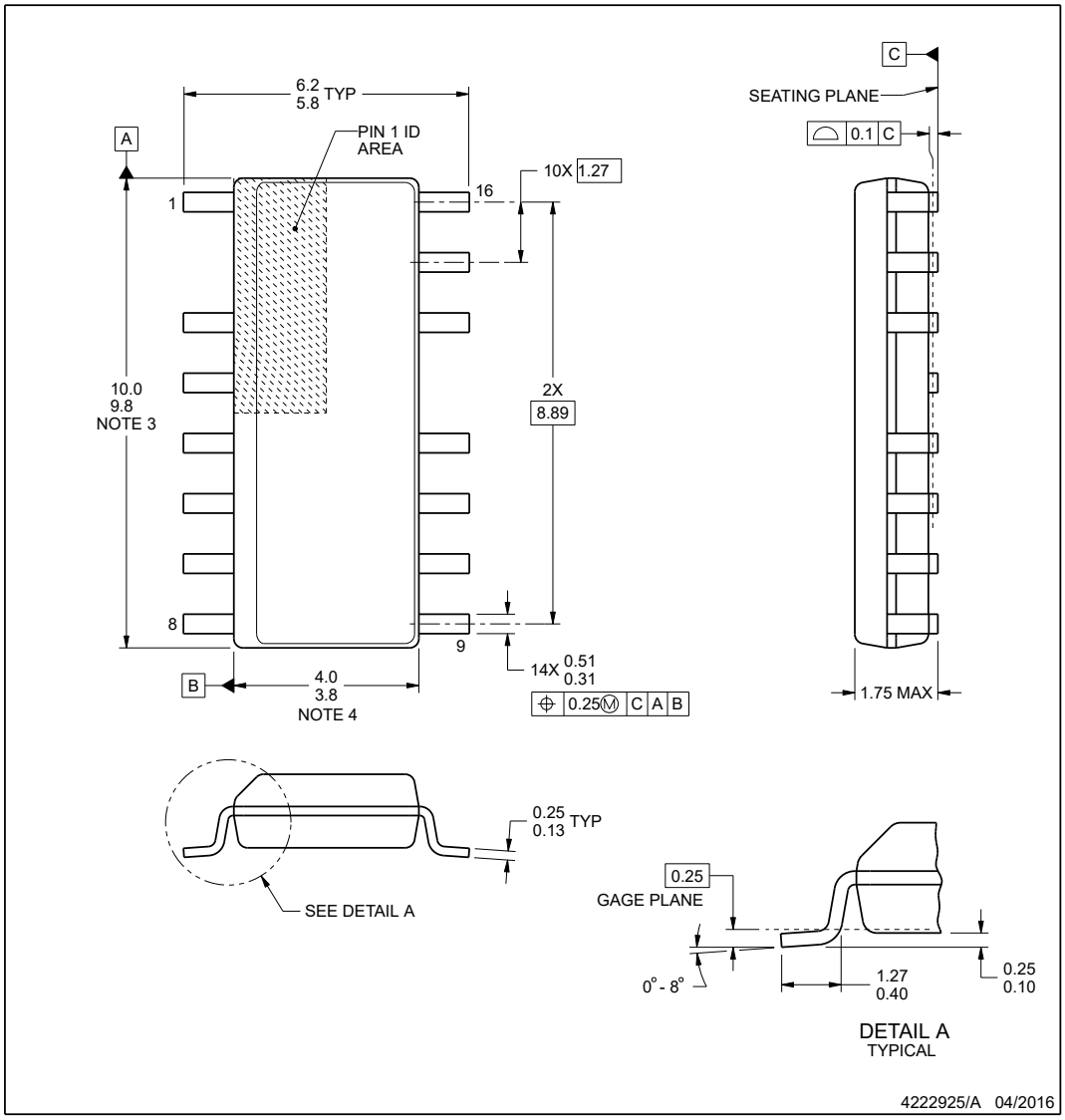
(1) **Status:** For more details on status, see our product life cycle.
(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

11.1 Mechanical Data

PACKAGE OUTLINE

DDB0014A — **SOIC - 1.75 mm max height**

SOIC



NOTES:

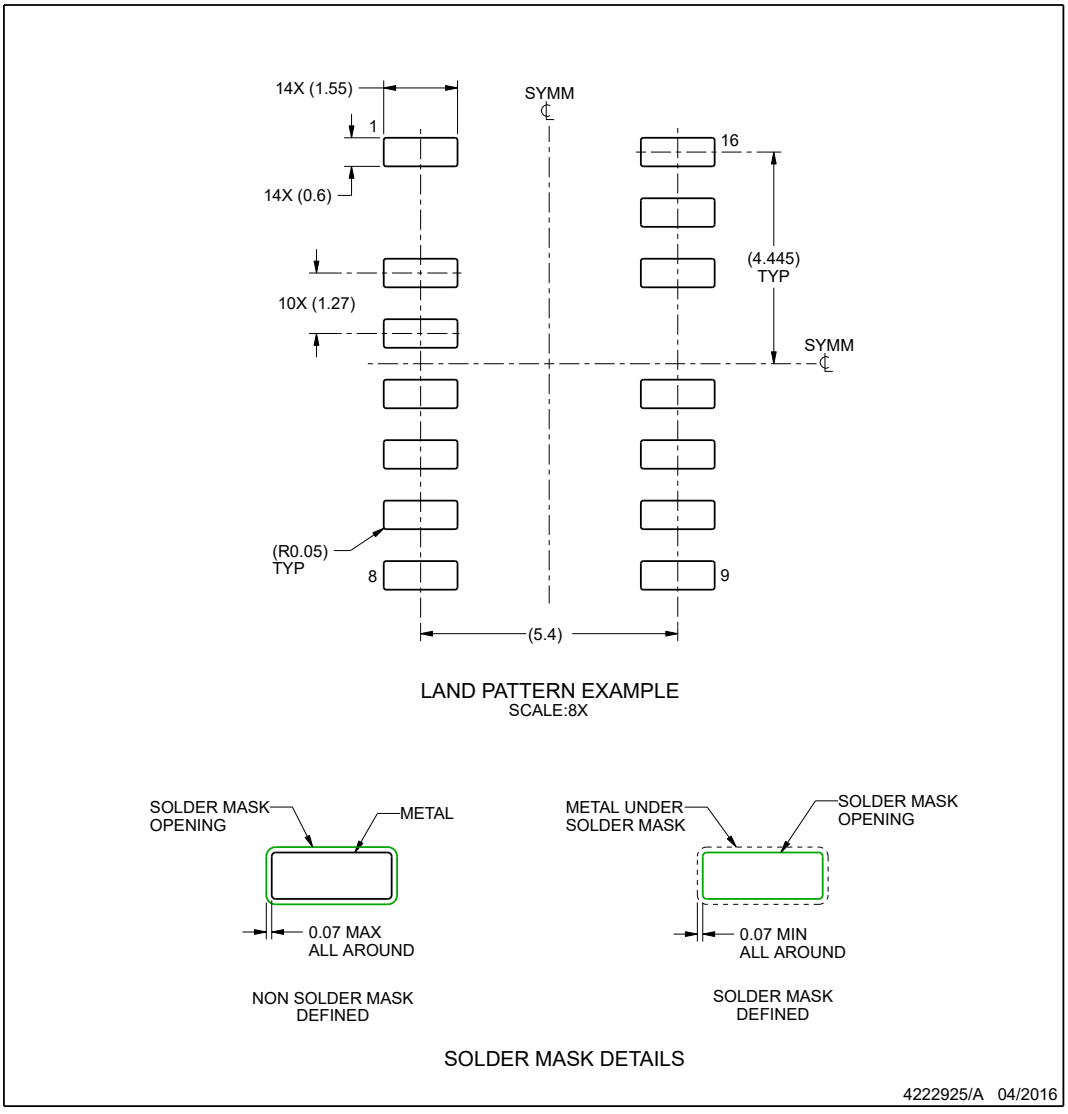
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-012, variation AC.

EXAMPLE BOARD LAYOUT

DDB0014A

SOIC - 1.75 mm max height

SOIC



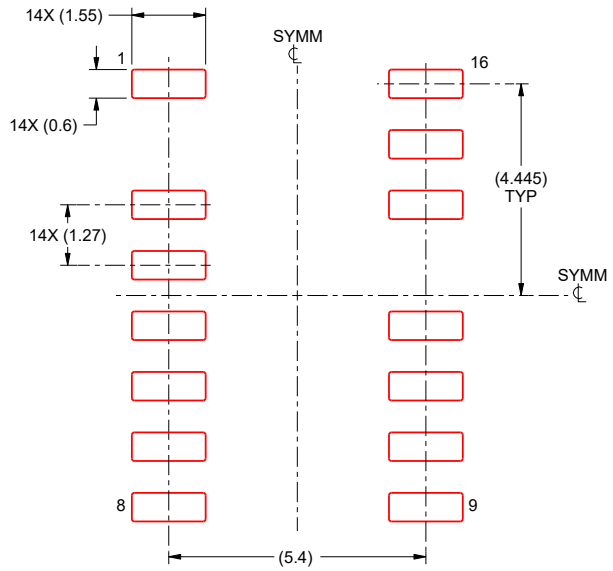
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDB0014A — **SOIC - 1.75 mm max height**

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4222925/A 04/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025