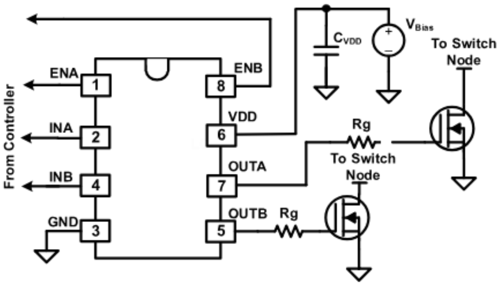
UCC27624V 30V, 5A, Dual-Channel, 8V-UVLO, Low-Side Gate Driver with –10V Input Capability

1 Features

- Typical 5A peak source and sink drive current for each channel
- Input and enable pins capable of handling –10V
- Output capable of handling –2V transients
- Absolute hhhhmaximum VDD voltage: 30V
- Wide VDD operating range from 9.5V to 26V with UVLO
- Two independent gate drive channels
- Independent enable function for each output
- Hysteretic-logic thresholds for high noise immunity
- VDD independent input thresholds (TTL compatible)
- Fast propagation delays (17ns typical)
- Fast rise and fall times (6ns and 10ns typical)
- 1ns typical delay matching between the two channels
- Two channels can be paralleled for higher drive current
- SOIC8 PowerPAD™ and VSSOP8 PowerPAD™ package options
- Operating junction temperature range of –40°C to 150°C

2 Applications

- Switched-mode power supplies (SMPS)
- Power factor correction (PFC) circuits
- DC/DC converter
- Motor drives
- Solar power supplies
- Pulse transformer driver



Simplified Application Diagram

3 Description

The UCC27624V is a dual-channel, high-speed, low-side gate driver that effectively drives MOSFET, IGBT and SiC power switches. UCC27624V has a typical peak drive strength of 5A, which reduces rise and fall times of the power switches, lowers switching losses, and increases efficiency. The device's fast propagation delay (17ns typical) yields better power stage efficiency by improving the deadtime optimization, pulse width utilization, control loop response, and transient performance of the system.

UCC27624V can handle –10V at its inputs, which improves robustness in systems with moderate ground bouncing. The inputs are independent of supply voltage and can be connected to most controller outputs for maximum control flexibility. An independent enable signal allows the power stage to be controlled independently of main control logic. In the event of a system fault, the gate driver can quickly shut-off by pulling enable low. Many high-frequency switching power supplies exhibit noise at the gate of the power device, which can get injected into the output pin on the gate driver and can cause the driver to malfunction. The device's transient reverse current and reverse voltage capability allow it to tolerate noise on the gate of the power device or pulse-transformer and avoid driver malfunction.

The UCC27624V also features undervoltage lockout (UVLO) for improved system robustness. When there is not enough bias voltage to fully enhance the power device, the gate driver output is held low by the strong internal pull down MOSFET.

Package Information

PART NUMBER	PACKAGE[1]	PACKAGE SIZE (NOM)
UCC27624V	D (SOIC 8)	4.90mm × 3.91mm
UCC27624V	DDA (SOIC 8)	4.90mm x 3.91mm
UCC27624V	DGK (VSSOP 8)	3.00mm x 3.00 mm
UCC27624V	DGN (VSSOP 8)	3.00mm × 3.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Table of Contents

4 Pin Configuration and Functions

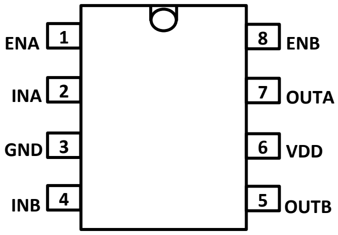


Figure 4-1. D Package 8-Pin SOIC Top View

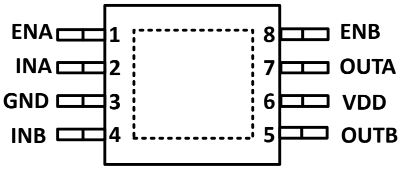


Figure 4-2. DGN Package 8-Pin VSSOP Top View

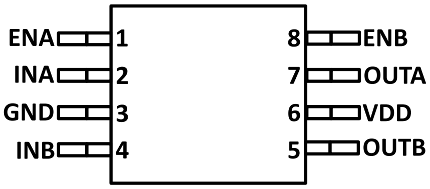


Figure 4-3. DGK Package 8-Pin VSSOP Top View

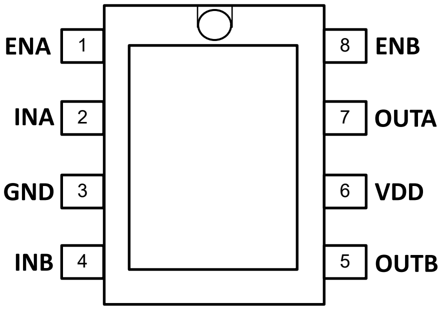


Figure 4-4. DDA Package 8-Pin SOIC Top View

Table 4-1. Pin Functions

PIN			TYPE[(1)]	DESCRIPTION
NAME	DGN,DDA	D,DGK		
ENA	1	1	I	Enable input for Channel A. Biasing ENA, LOW will disable Channel A output regardless of the state of INA. Pulling ENA, HIGH enables the Channel A output. If ENA is left floating, Channel A is enabled by default due to an internal pullup resistor. It is recommended to connect this pin to VDD if unused.
ENB	8	8	I	Enable input for Channel B. Biasing ENB, LOW disables Channel B output regardless of the state of INB. Pulling ENB, HIGH enables the Channel B output. If ENB is left floating, Channel B is enabled by default due to an internal pullup resistor. It is recommended to connect this pin to VDD if unused.
GND	3	3	—	Ground: All signals are referenced to this pin.
INA	2	2	I	Input to Channel A. INA is the non-inverting input of the UCC27624V device. OUTA is held LOW if INA is unbiased or floating by default due to an internal pulldown resistor. Connect this pin to GND if unused.

Table 4-1. Pin Functions (continued)

PIN			TYPE[1]	DESCRIPTION
NAME	DGN,DDA	D,DGK		
INB	4	4	I	Input to Channel B. INB is the non-inverting input of the UCC27624V device. OUTB is held LOW if INB is unbiased or floating by default due to an internal pulldown resistor. Connect this pin to GND if unused.
OUTA	7	7	O	Channel A Output
OUTB	5	5	O	Channel B Output
VDD	6	6	I	Bias supply input. Bypass this pin with two ceramic capacitors, generally ≥ 1µF and 0.1µF, which are referenced to GND pin of this device.
	Thermal Pad	—	—	Connect to GND through large copper plane. This pad is not a low-impedance path to GND.

(1) I = Input; O = Output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2) (3)

		MIN	MAX	UNIT
Supply voltage, VDD		–0.3	30	V
Output Voltage, OUTA, OUTB	DC	–0.3	VDD +0.3	V
	200ns Pulse	–2	VDD +3	V
Input Voltage INA, INB, ENA, ENB		–10	30	V
Operating junction temperature, T_J		–40	150	°C
Lead temperature	Soldering, 10 sec.		300	°C
	Reflow		260	
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) All voltages are with respect to GND unless otherwise noted. Currents are positive into, negative out of the specified terminal. See Section 5.4 of the datasheet for thermal limitations and considerations of packages.

(3) These devices are sensitive to electrostatic discharge; follow proper device handling procedures.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range. All voltages are with reference to GND (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage, VDD	9.5	12	26	V
Input voltage, INA, INB, ENA, ENB	–10		26	V
Output Voltage, OUTA, OUTB	0		VDD	V
Operating junction temperature, T_J	–40		150	°C

5.4 Thermal Information

THERMAL METRIC		UCC27624V				UNIT
		DGN	D	DDA	DGK	
		8 Pins	8 Pins	8 Pins	8 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	48.9	126.4	50.37	148.59	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	71.8	67.0	67.30	56.27	
$R_{\theta JB}$	Junction-to-board thermal resistance	22.3	69.9	23.80	79.67	
Ψ_{JT}	Junction-to-top characterization parameter	2.6	19.2	10.75	10.13	
Ψ_{JB}	Junction-to-board characterization parameter	22.3	69.1	23.95	78.89	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.5	N/A	9.04	N/A	

5.5 Electrical Characteristics

Unless otherwise noted, VDD = 12 V, T_A = T_J = –40°C to 150°C, 1-µF capacitor from VDD to GND, no load on the output. Typical condition specifications are at 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BIAS CURRENTS						
I_{VDDq}	VDD quiescent supply current	V_{INx} = 3.3 V, VDD = 3.4 V, ENx = VDD		300	450	µA
I_{VDD}	VDD static supply current	V_{INx} = 3.3 V, ENx = VDD		0.6	1.0	mA
I_{VDD}	VDD static supply current	V_{INx} = 0 V, ENx = VDD		0.7	1.0	mA
I_{VDDO}	VDD operating current	f_{SW} = 1000 kHz, ENx = VDD, V_{INx} = 0 V – 3.3 V PWM		3.2	3.8	mA
I_{DIS}	VDD disable current	V_{INx} = 3.3 V, ENx = 0 V		0.8	1.1	mA
UNDERVOLTAGE LOCKOUT (UVLO)						
V_{VDD_ON}	VDD UVLO rising threshold		8.0	8.5	9.0	V
V_{VDD_OFF}	VDD UVLO falling threshold		7.5	8.0	8.5	V
V_{VDD_HYS}	VDD UVLO hysteresis			0.5		V
INPUT (INA, INB)						
V_{INx_H}	Input signal high threshold	Output High, ENx = HIGH	1.8	2	2.3	V
V_{INx_L}	Input signal low threshold	Output Low, ENx = HIGH	0.8	1	1.2	V
V_{INx_HYS}	Input signal hysteresis			1		V
R_{INx}	INx pin pulldown resistor	INx = 3.3 V		120		kΩ
ENABLE (ENA, ENB)						
V_{ENx_H}	Enable signal high threshold	Output High, INx = HIGH	1.8	2	2.3	V
V_{ENx_L}	Enable signal low threshold	Output Low, INx = HIGH	0.8	1	1.2	V
V_{ENx_HYS}	Enable signal hysteresis			1		V
R_{ENx}	EN pin pullup resistance	ENx = 0 V		200		kΩ
OUTPUTS (OUTA, OUTB)						
I_{SRC} (1)	Peak output source current	VDD = 12 V, C_{VDD} = 10 µF, C_L = 0.1 µF, f = 1 kHz		5		A
I_{SNK} (1)	Peak output sink current	VDD = 12 V, C_{VDD} = 10 µF, C_L = 0.1 µF, f = 1 kHz		–5		A
R_{OH} (2)	Pullup resistance	I_{OUT} = –50 mA, See Section 6.3.4.		5	8.5	Ω
R_{OL}	Pulldown resistance	I_{OUT} = 50 mA		0.6	1.1	Ω

(1) Parameter not tested in production.
(2) Output pullup resistance in this table is a DC measurement that measures resistance of PMOS structure only (not N-channel structure).

5.6 Switching Characteristics

Unless otherwise noted, VDD = V_{EN} = 12 V, T_A = T_J = –40°C to 150°C, 1-μF capacitor from VDD to GND, no load on the output. Typical condition specifications are at 25°C (1).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{Rx}	Rise time	C_{LOAD} = 1.8 nF, 20% to 80%, Vin = 0 V – 3.3 V		6	10	ns
t_{Fx}	Fall time	C_{LOAD} = 1.8 nF, 90% to 10%, Vin = 0 V – 3.3 V		10	14	ns
t_{D1x}	Turn-on propagation delay	C_{LOAD} = 1.8 nF, V_{INx_H} of the input rise to 10% of output rise, Vin = 0 V – 3.3 V, Fsw = 500 kHz, 50% duty cycle, T_J = 125°C		17	27	ns
t_{D2x}	Turn-off propagation delay	C_{LOAD} = 1.8 nF, V_{INx_L} of the input fall to 90% of output fall, Vin = 0 V – 3.3 V, Fsw = 500 kHz, 50% duty cycle, T_J = 125°C		17	27	ns
t_{D3x}	Enable propagation delay	C_{LOAD} = 1.8 nF, V_{ENx_H} of the enable rise to 10% of output rise, Vin = 0 V – 3.3 V, Fsw = 500 kHz, 50% duty cycle, T_J = 125°C		17	27	ns
t_{D4x}	Disable propagation delay	C_{LOAD} = 1.8 nF, V_{ENx_L} of the enable fall to 90% of output fall, Vin = 0 V – 3.3 V, Fsw = 500 kHz, 50% duty cycle, T_J = 125°C		17	27	ns
t_M	Delay matching between two channels	C_{LOAD} = 1.8 nF, Vin = 0 V – 3.3 V, Fsw = 500 kHz, 50% duty cycle, INA = INB, $\|t_{RA} – t_{RB}\|$, $\|t_{FA} – t_{FB}\|$		1	2	ns
t_{PWmin}	Minimum input pulse width	C_L = 1.8 nF, Vin = 0 V – 3.3 V, Fsw = 500 kHz, Vo > 1.5 V		10	15	ns

(1) Switching parameters are not tested in production.

5.7 Timing Diagrams

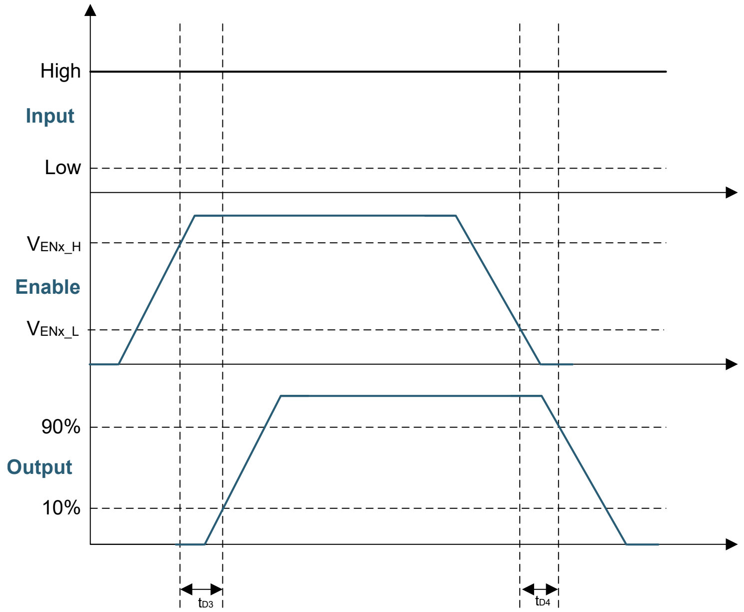


Figure 5-1. Enable Function

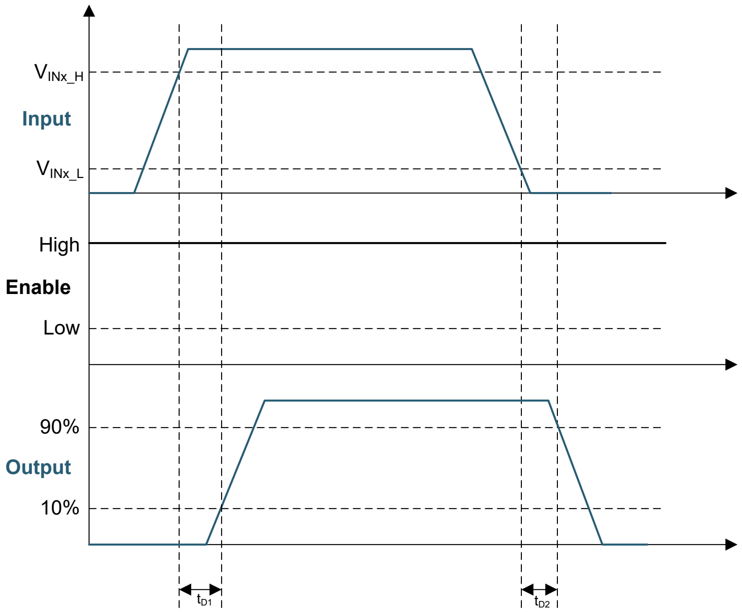


Figure 5-2. Input-Output Operation

5.8 Typical Characteristics

Unless otherwise specified, VDD=12V, INx=3.3V, ENx=3.3V, T_J = 25°C, no load

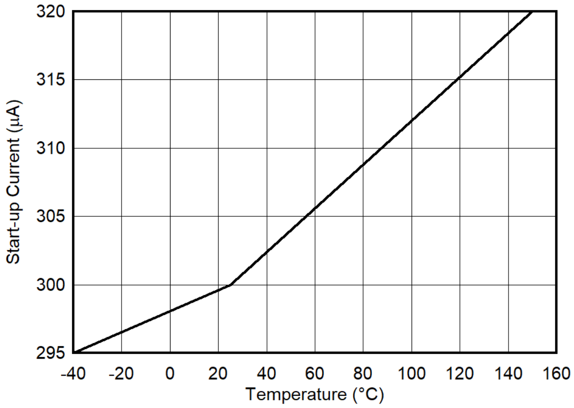


Figure 5-3. Start-Up and Quiescent Current

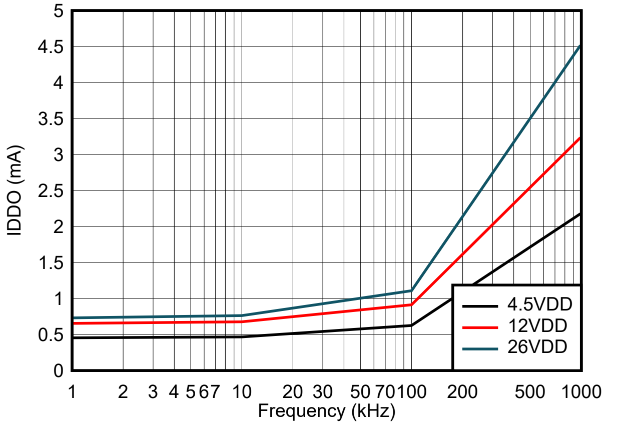


Figure 5-4. Operating Supply Current (both outputs switching)

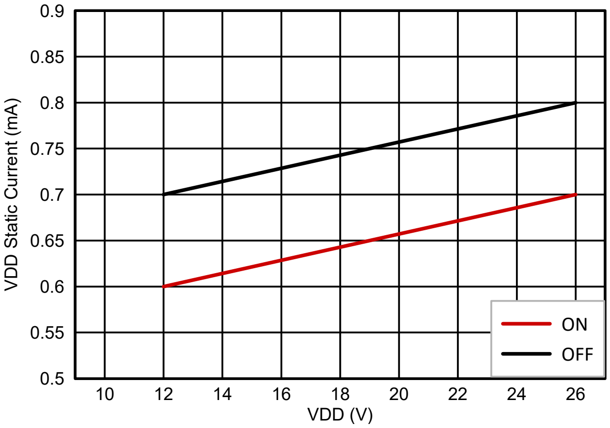


Figure 5-5. Static Supply Current (outputs in DC on or off condition)

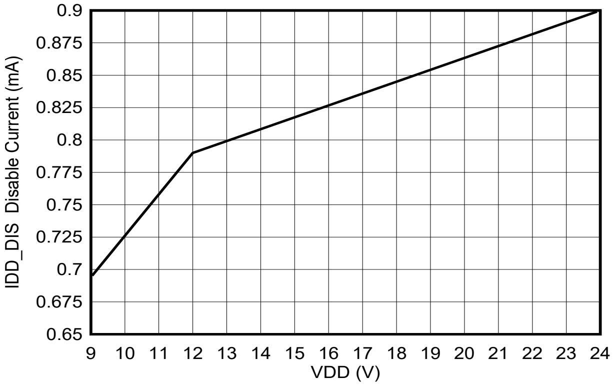


Figure 5-6. Disable Current (EN = 0V)

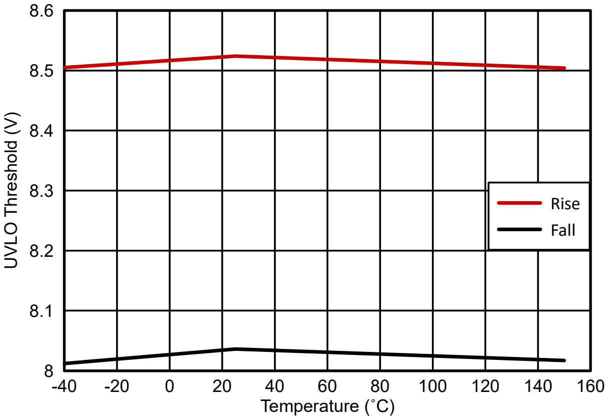


Figure 5-7. VDD UVLO Threshold

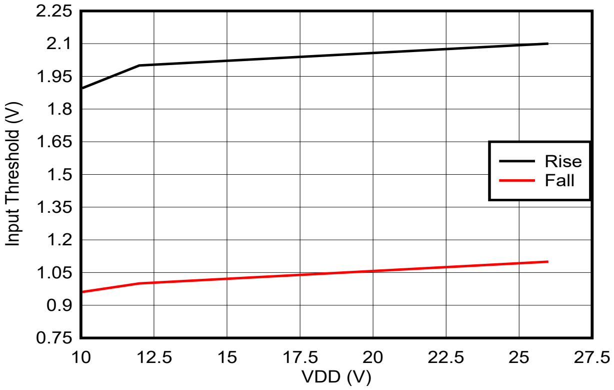


Figure 5-8. Input Thresholds

5.8 Typical Characteristics (continued)

Unless otherwise specified, VDD=12V, INx=3.3V, ENx=3.3V, T_J = 25°C, no load

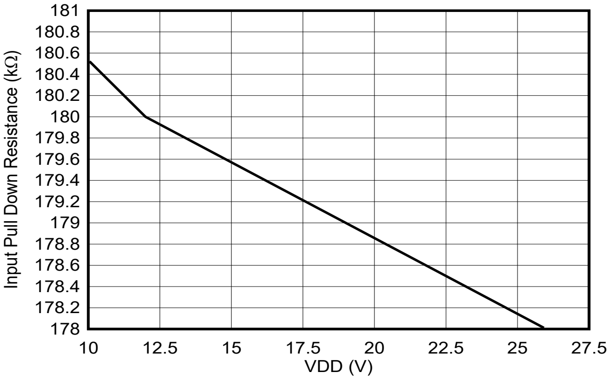


Figure 5-9. Input Pulldown Resistance

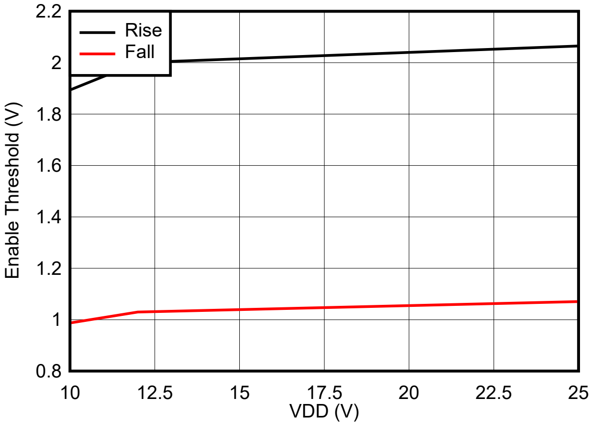


Figure 5-10. Enable Threshold

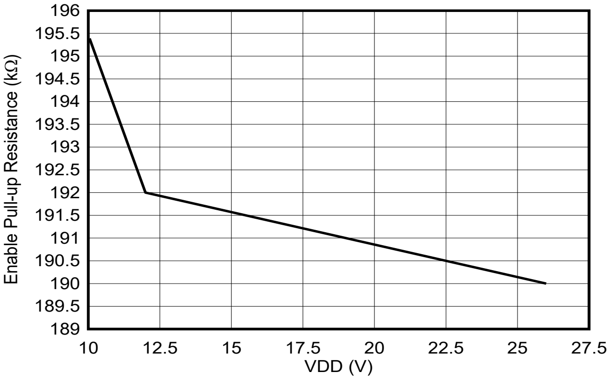


Figure 5-11. Enable Pullup Resistance

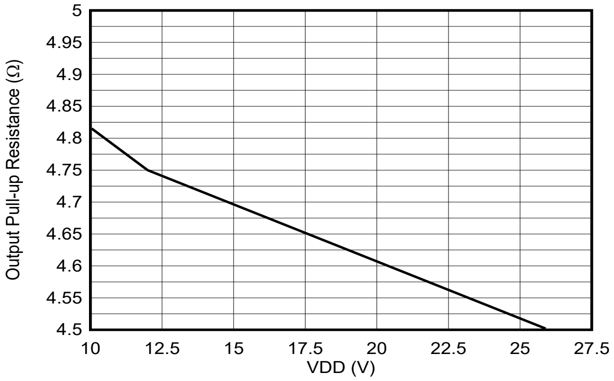


Figure 5-12. Output Pullup Resistance

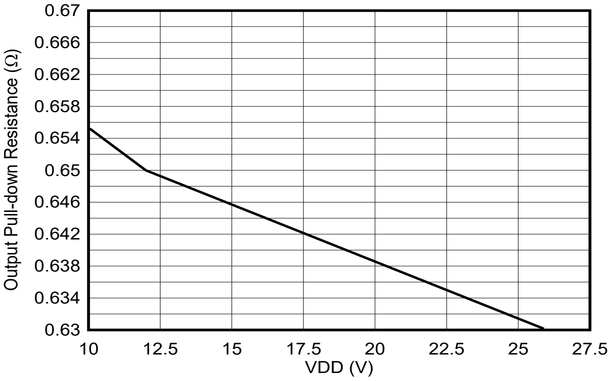
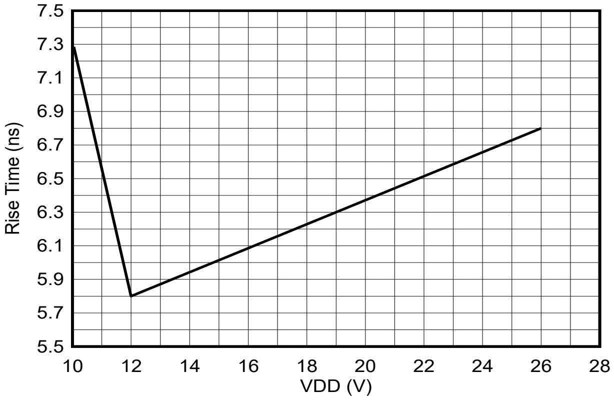


Figure 5-13. Output Pulldown Resistance

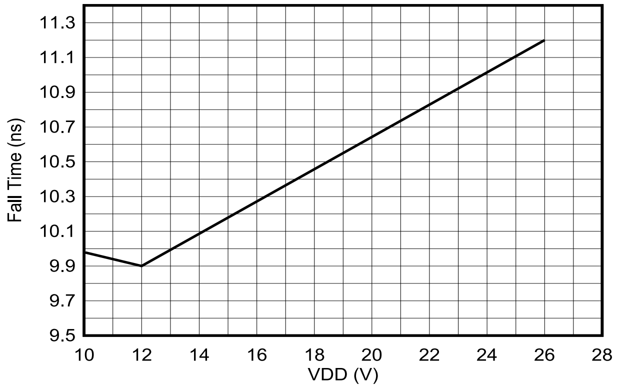


C_{LOAD} = 1.8 nF

Figure 5-14. Output Rise Time vs VDD

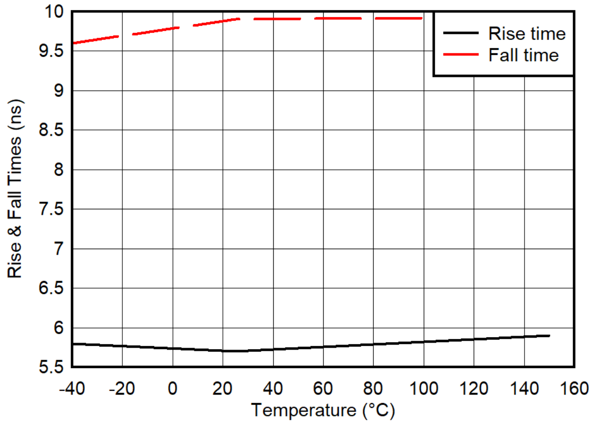
5.8 Typical Characteristics (continued)

Unless otherwise specified, VDD=12V, INx=3.3V, ENx=3.3V, T_J = 25°C, no load



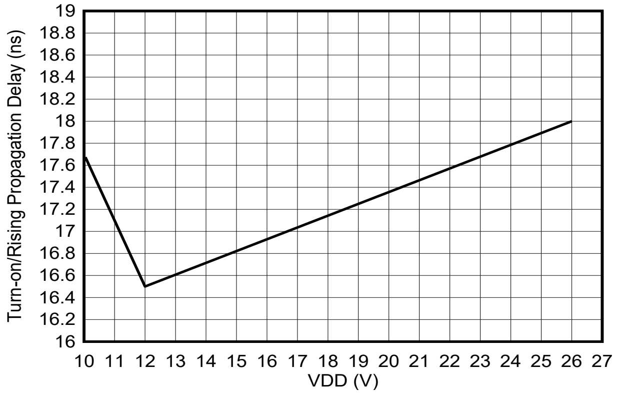
C_{LOAD} = 1.8 nF

Figure 5-15. Output Fall Time vs VDD



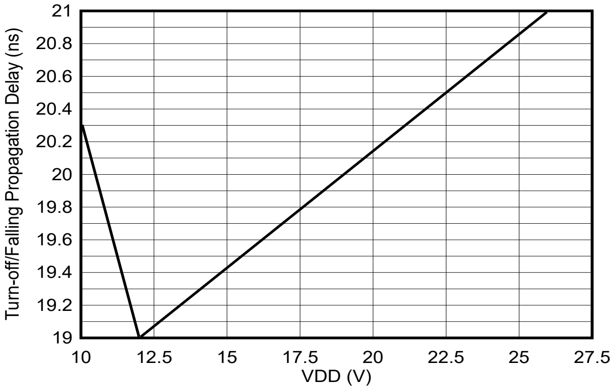
C_{LOAD} = 1.8 nF

Figure 5-16. Output Rise and Fall Time vs Temperature



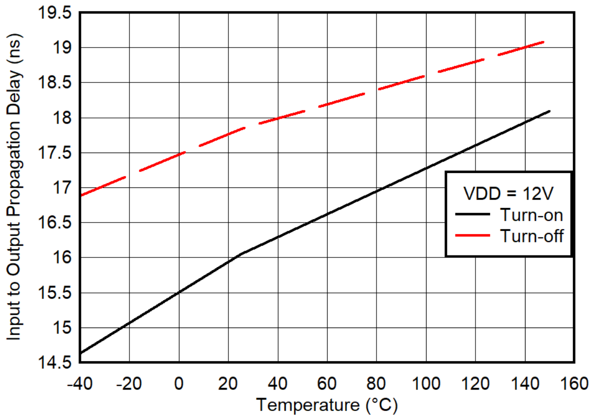
C_{LOAD} = 1.8 nF

Figure 5-17. Input to Output Rising (turn-on) Propagation Delay vs VDD



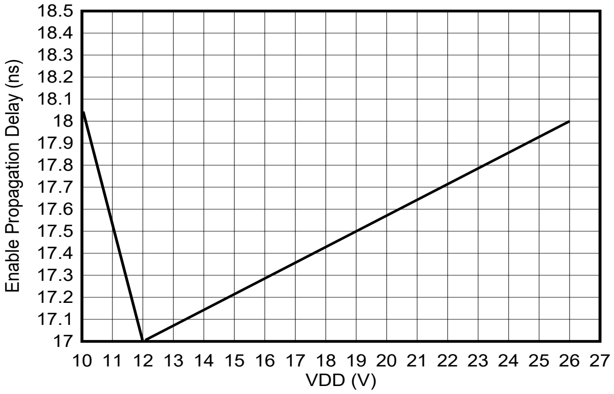
C_{LOAD} = 1.8 nF

Figure 5-18. Input to Output Falling (turn-off) Propagation Delay vs VDD



C_{LOAD} = 1.8 nF

Figure 5-19. Input Propagation Delay vs Temperature

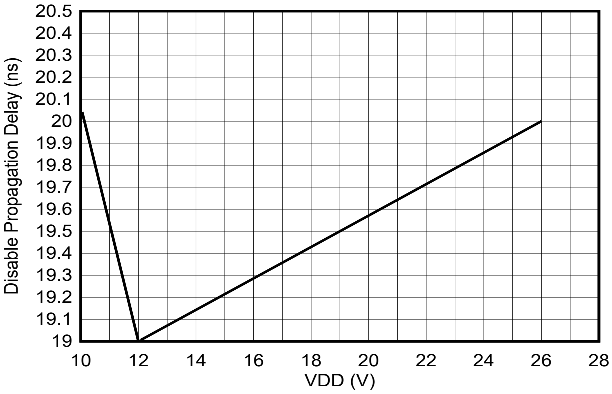


C_{LOAD} = 1.8 nF

Figure 5-20. Enable to Output Rising Propagation Delay

5.8 Typical Characteristics (continued)

Unless otherwise specified, VDD=12V, INx=3.3V, ENx=3.3V, T_J = 25°C, no load



C_{LOAD} = 1.8nF

Figure 5-21. Enable to Output Falling Propagation Delay

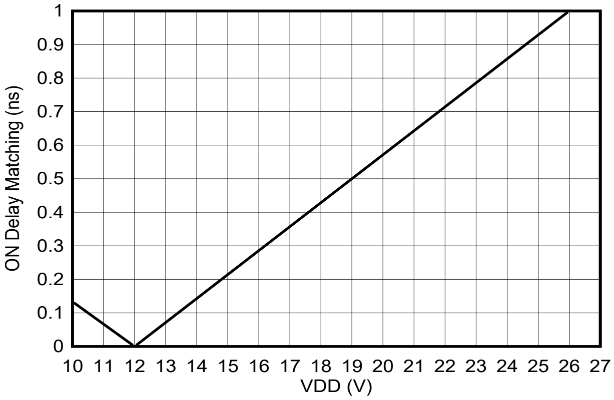


Figure 5-22. Turn-On/Rising Delay Matching

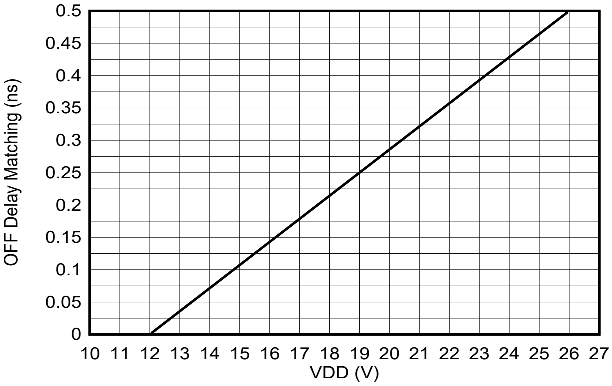


Figure 5-23. Turn-Off and Falling Delay Matching

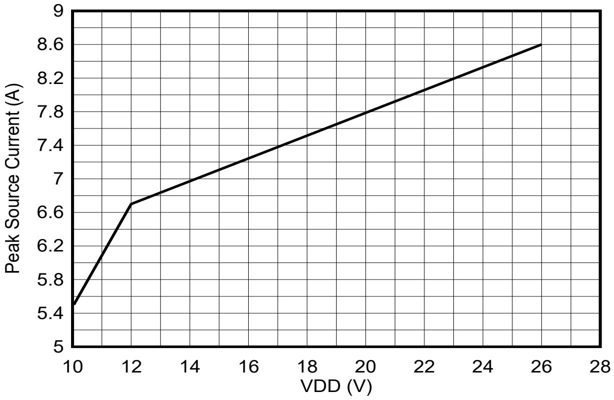


Figure 5-24. Peak Source Current vs VDD

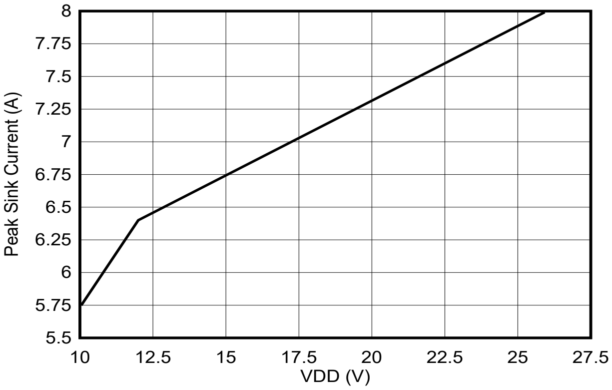


Figure 5-25. Peak Sink Current vs VDD

6 Detailed Description

6.1 Overview

The UCC27624V device represents TI's latest generation of dual-channel, low-side, high-speed, gate driver devices featuring 5A source and sink current capability, fast switching characteristics, and a host of other features. *UCC27624V Features and Benefits* details the advantages of the gate driver's features, which combine to ensure efficient, robust, and reliable operation in high-frequency switching power circuits. The robust inputs of UCC27624V can handle –10V, ensuring reliable operation in noisy environments. The driver has good transient handling capability on its output due to its reverse current handling, as well as rail-to-rail output drive, and a small propagation delay (typically 17ns). With this built-in robustness, the UCC27624V device can also be directly connected to a gate drive transformer.

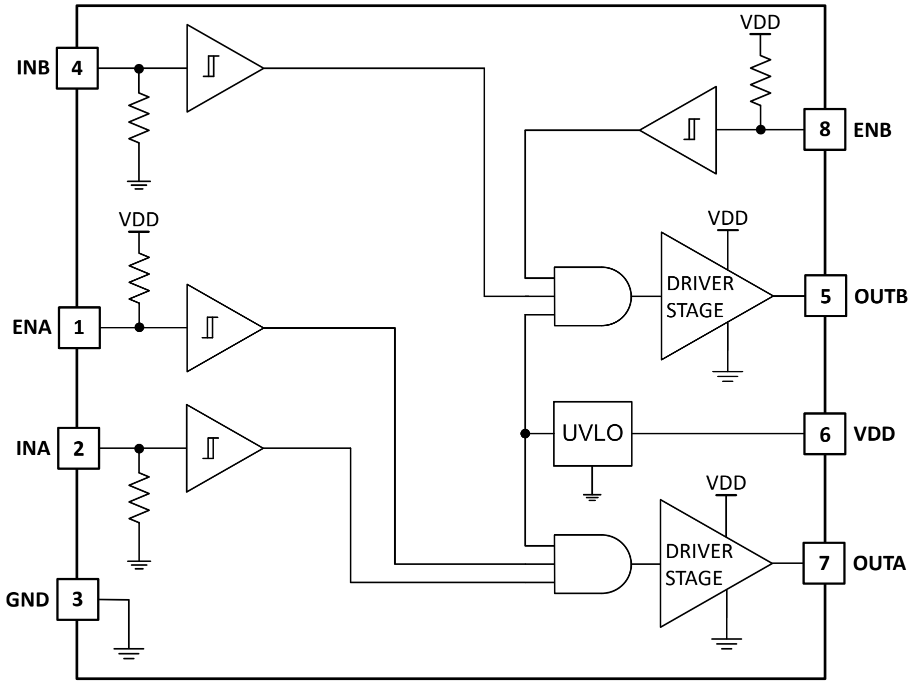
The input threshold of UCC27624V is compatible with TTL low-voltage logic, which is fixed and independent of VDD supply voltage. The driver can also work with CMOS-based controllers as long as the threshold requirement is met. The 1V typical hysteresis offers excellent noise immunity.

Each channel has an enable pin, ENx, with a fixed TTL compatible threshold. The ENx pins are internally pulled up. Pulling ENx low disables the corresponding channel, while leaving ENx open provides normal operation. The ENx pins can be used as an additional input with the same performance as the INx pins.

Table 6-1. UCC27624V Features and Benefits

FEATURE	BENEFIT
–10V IN and EN capability	Enhanced signal reliability and device robustness in noisy environments that experience ground bounce on the gate driver
17ns (typical) propagation delay	Extremely low-pulse transmission distortion
1ns (typical) delay matching between channels	Ease of paralleling outputs for higher (two times) current capability. This helps when driving parallel-power switches.
Expanded VDD operating range of 9.5V to 26V	Flexibility in system design. Covers a wide range of power switches
Expanded operating temperature range of –40°C to +150°C	Flexibility in system design. System robustness improvement
VDD UVLO protection	Outputs are held low in UVLO condition, which ensures predictable, glitch-free operation at power-up and power-down.
Outputs are held low when input pins (INx) are in floating condition.	Protection feature, especially useful in passing abnormal condition tests during safety certification
Outputs are enabled when enable pins (ENx) are in floating condition.	Pin-to-pin compatibility with legacy devices from Texas Instruments in designs where Pin 1 and Pin 8 are "No Connect" pins
Input and enable threshold with wide hysteresis	Enhanced noise immunity while retaining compatibility with microcontroller logic-level input signals (3.3V, 5V) optimized for digital power
Inputs independent of VDD	System simplification, especially related to auxiliary bias supply architecture

6.2 Functional Block Diagram



Typical ENx pullup resistance is 200kΩ and INx pulldown resistance is 120kΩ.

6.3 Feature Description

6.3.1 Operating Supply Current

The UCC27624V device features low quiescent I_{DD} currents. The typical operating supply current in UVLO state and fully-on state (under static and switching conditions) are summarized in the Electrical Characteristics table. The lowest quiescent current (I_{DD}) is achieved when the device is fully on and the outputs are in a static state (DC high or DC low). During this state, all of the internal logic circuits of the device are fully operational. The total supply current is the sum of the quiescent I_{DD} current, the average I_{OUT} current because of switching, and any current related to pullup resistors on the enable pins. Knowing the operating switching frequency (f_{SW}) and the MOSFET gate charge (Q_G) at the drive voltage being used, the average I_{OUT} current can be calculated as product of Q_G and f_{SW}.

Typical Characteristics provides a complete characterization of the I_{DD} current as a function of switching frequency at different V_{DD} bias voltages. The linear variation and close correlation with the theoretical value of the average I_{OUT} indicate a negligible shoot-through inside the gate driver device, displaying its high-speed characteristics.

6.3.2 Input Stage

The input pins of the UCC27624V gate driver device are based on a TTL compatible input threshold logic that is independent of the VDD supply voltage. With a high threshold of 2V and a low threshold of 1V, the logic level thresholds are conveniently driven with PWM control signals derived from 3.3V and 5V digital power controller devices. Wider hysteresis (1V typical) offers enhanced noise immunity compared to traditional TTL logic implementations, where the hysteresis is typically less than 0.5V. UCC27624V devices also feature tight control of the input pin threshold voltage levels, which eases system design considerations and ensures stable operation across temperature (refer to *Typical Characteristics*). The very low input capacitance on these pins reduces loading and increases switching speed.

The UCC27624V device features an important protection feature that holds the output of a channel low when the respective input pin is in a floating condition. This is achieved through the internal pulldown resistors to ground on both of the input pins (INA, INB), as shown in *Fuction Block Diagram*.

The input pins can handle wide range of slew rate. In most power supply applications, the gate driver is either driven by the output of a digital controller or logic gates. Therefore, in most applications the input signal slew rate is fast and is no concern for the UCC27624V family of devices. The wide hysteresis offered in UCC27624V alleviates the concern of chattering compared to many other drivers that have very small hysteresis at the input. If limiting the rise or fall times to the power device is the primary goal, then an external gate resistor is highly recommended between the output of the driver and the gate of the switching power device. This external resistor has the additional benefit of reducing part of the gate-charge related power dissipation in the gate driver device package and transferring it into the external resistor itself. In short, some of the power gets dissipated in the gate resistor rather than inside of the gate driver. Additionally, the input pins of UCC27624V are capable of handling –10V. This improves the system robustness in noisy (electrical) applications. This also enables the driver to directly connect to the output of a gate drive transformer without the use of rectifying diodes, which saves board space and BOM cost.

6.3.3 Enable Function

The enable function is an extremely beneficial feature in gate driver devices, especially for certain applications such as synchronous rectification where the driver outputs are disabled in light-load conditions to prevent negative current circulation and to improve light-load efficiency.

The UCC27624V device is equipped with independent enable pins (ENx) for exclusive control of each driver channel operation. The enable pins are based on a non-inverting configuration (active-high operation). Thus, when ENx pins are driven high, the drivers are enabled and when ENx pins are driven low, the driver outputs are disabled. Similar to the input pins, the enable pins are also based on a TTL compatible threshold logic that is independent of the supply voltage and are effectively controlled using logic signals from 3.3V or 5V controllers. The UCC27624V device also features tight control of the enable-function threshold-voltage levels which eases system design considerations and ensures stable operation across temperature. The ENx pins are internally pulled up to VDD using pullup resistors, as a result of which the outputs of the device are enabled in the default state. Hence even if the ENx pins are left floating the driver output is enabled. Essentially, this floating allows the UCC27624V device to be pin-to-pin compatible with TI's previous generation of drivers (UCC27324, UCC27424, UCC27524), where Pin 1 and Pin 8 are either ENx or N/C pins. If the channel A and channel B inputs and outputs are connected in parallel to increase the driver current capacity, ENA and ENB must be connected and driven together. The ENx pins of the UCC27624V are capable of handling –10V, which improves system robustness in noisy (electrical) applications.

6.3.4 Output Stage

The UCC27624V device output stage features a unique architecture on the pullup structure, which delivers the highest peak source current when it is most needed, during the Miller plateau region of the power switch turn-on transition (when the power switch drain or collector voltage experiences dV/dt). The device output stage features a hybrid pullup structure using a parallel arrangement of N-Channel and P-Channel MOSFET devices. By turning on the N-Channel MOSFET during a narrow instant when the output changes state from low to high, the gate driver device is able to deliver a brief boost in the peak sourcing current enabling fast turn-on. The on-resistance of this N-channel MOSFET (R_{NMOS}) is approximately 1.04Ω when activated.

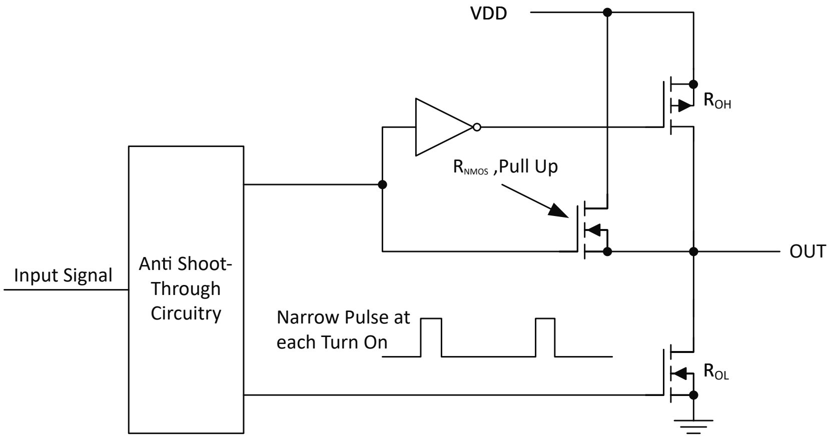


Figure 6-1. UCC27624V Gate Driver Output Structure

The R_{OH} parameter is a DC measurement and it is representative of the on-resistance of the P-Channel device only. This is because the N-Channel device is held in the off state in DC condition and is turned-on only for a narrow instant when output changes state from low to high. Note that effective resistance of the UCC27624V pull-up stage during the turn-on instance is much lower than what is represented by R_{OH} parameter.

The pull-down structure in the UCC27624V device is simply comprised of a N-Channel MOSFET. The R_{OL} parameter, which is also a DC measurement, is representative of the impedance of the pull-down stage in the device.

Each output stage in the UCC27624V device is capable of supplying 5A peak source and 5A peak sink current pulses. The output voltage swings between VDD and GND providing rail-to-rail operation, thanks to the MOS-output stage which delivers very low dropout. The presence of the MOSFET-body diodes also offers low impedance to transient overshoots and undershoots. The outputs of these drivers are designed to withstand 5A of peak reverse current transients without damage to the device.

The UCC27624V device is particularly suited for dual-polarity, symmetrical drive-gate transformer applications where the primary winding of transformer driven by OUTA and OUTB, with inputs INA and INB being driven complementary to each other. This is possible because of the extremely low dropout offered by the MOS output stage of these devices, both during high (V_{OH}) and low (V_{OL}) states along with the low impedance of the driver output stage. All of these allow alleviate concerns regarding transformer demagnetization and flux imbalance. The low propagation delays also ensure proper reset for high-frequency applications.

For applications that have zero voltage switching during power MOSFET turn-on or turn-off interval, the driver supplies high-peak current for fast switching even though the miller plateau is not present. This situation often occurs in synchronous rectifier applications because the body diode is generally conducting before power MOSFET is switched on.

6.3.5 Low Propagation Delays and Tightly Matched Outputs

The UCC27624V driver device features a very small, 17ns (typical) propagation delay between input and output, which offers the lowest level of pulse width distortion for high-frequency switching applications. For example, in synchronous rectifier applications, the SR MOSFETs are driven with very low distortion when a single driver device is used to drive the SR MOSFETs. Additionally, the driver devices also feature extremely accurate, 1ns (typical) matched internal propagation delays between the two channels, which is beneficial for applications that require dual gate drives with critical timing. For example, in a PFC application, a pair of paralleled MOSFETs can be driven independently using each output channel, with the inputs of both channels driven by a common control signal from the PFC controller. In this case, the 1ns delay matching ensures that the paralleled MOSFETs are driven in a simultaneous fashion, minimizing turn-on and turn-off delay differences. Another benefit of the tight matching between the two channels is that the two channels can be connected together to effectively double the drive current capability. That is, A and B channels may be combined into a single driver by connecting the INA and INB inputs together and the OUTA and OUTB outputs together; then, a single signal controls the paralleled power devices.

6.4 Device Functional Modes

Table 6-2. Device Logic Table

ENA	ENB	INA	INB	UCC27624V	
				OUTA	OUTB
H	H	L	L	L	L
			H	L	H
		H	L	H	L
			H	H	H
L	L	Any	Any	L	L
Any	Any	Float	Float	L	L
Float	Float	L	L	L	L
			H	L	H
		H	L	H	L
			H	H	H

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

High-current gate driver devices are required in switching power applications for a variety of reasons. In order to achieve fast switching of power devices and reduce associated switching-power losses, a powerful gate driver device is employed between the PWM output of control devices and the gates of the power semiconductor devices. Further, gate driver devices are indispensable when it is not feasible for the PWM controller device to directly drive the gates of the switching devices. With the advent of digital power, this situation is often encountered because the PWM signal from the digital controller is often a 3.3V logic signal which is not capable of effectively turning ON a power switch. A level-shifting circuitry is required to boost the 3.3V signal to the gate-drive voltage (such as 12V) in order to fully turn ON the power device and minimize conduction losses. Traditional buffer-drive circuits based on NPN/PNP bipolar transistors in a totem-pole arrangement, as emitter-follower configurations, prove inadequate with digital power because the traditional buffer-drive circuits lack level-shifting capability. Gate driver devices effectively combine both the level-shifting and buffer-drive functions. Gate driver devices also find other needs ,such as minimizing the effect of high frequency switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers and controlling floating power device gates, reducing power dissipation and thermal stress in controller devices by moving gate-charge power losses into the controller.

Finally, emerging wide band-gap power device technologies, such as SiC MOSFETs , which are capable of supporting very high switching frequency operation, are driving special requirements in terms of gate-drive capability. These requirements include a wide operating voltage range , low propagation delays, good delay matching, and availability in compact, low inductance packages with good thermal capability. In summary, gate driver devices are an extremely important component in switching power combining benefits of high performance, low cost, low component count, board space reduction, and simplified system design.

7.2 Typical Application

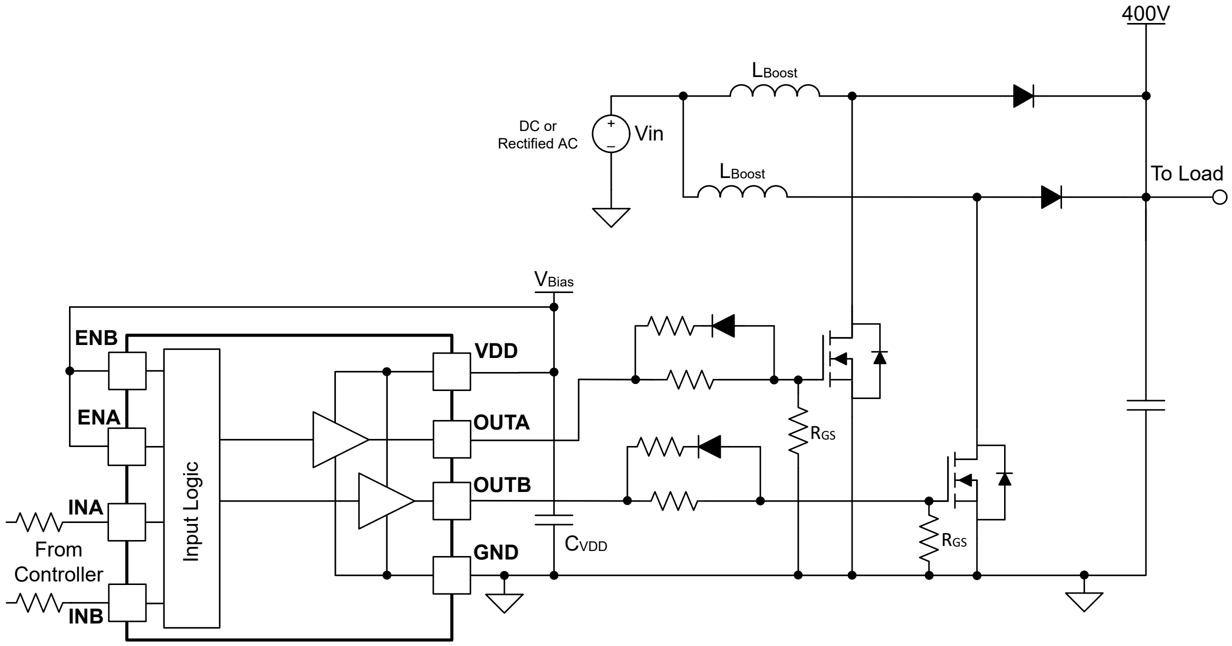


Figure 7-1. UCC27624V Typical Application Diagram

7.2.1 Design Requirements

When selecting and designing-in the gate driver device for an end application, some functional aspects must be considered and evaluated first, in order to make the most appropriate selection. Among these considerations are bias voltage, UVLO, drive current, and power dissipation.

7.2.2 Detailed Design Procedure

7.2.2.1 VDD and Undervoltage Lockout

The UCC27624V device has an internal undervoltage-lockout (UVLO) protection feature on the VDD pin supply circuit blocks. When VDD is rising and the level is still below UVLO threshold, this circuit holds the output low, regardless of the status of the inputs. The UVLO is typically 8V with 500mV typical hysteresis. This hysteresis prevents chatter when VDD supply voltages have noise, specifically at the lower end of the VDD operating range. UVLO hysteresis is also important to avoid any false tripping due to the bias noise generated because of fast switching transitions, where large peak currents are drawn from the bias supply bypass capacitors. The driver capability to operate at wide bias voltage range, along with good switching characteristics, is especially important in driving emerging power semiconductor devices, such as advanced low gate charge fast MOSFETs, and SiC MOSFETs.

At power-up, the UCC27624V driver device output remains low until the VDD voltage reaches the UVLO rising threshold, irrespective of the state of any other input pins such as INx and ENx. After the UVLO rising threshold, the magnitude of the OUT signal rises with V_{DD} until steady-state V_{DD} is reached.

For the best high-speed circuit performance and to prevent noise problems because the device draws current from the VDD pin to bias all internal circuits, use two VDD bypass capacitors. Also, use surface mount, low ESR capacitors. A 0.1µF ceramic capacitor should be located less than 1mm from the VDD to GND pins of the gate-driver device. In addition, a larger capacitor (≥1µF) must be connected in parallel (also as close to the driver IC as possible) to help deliver the high-current peaks required by the load. The parallel combination of capacitors presents a low impedance characteristic for the expected current levels and switching frequencies in the application.

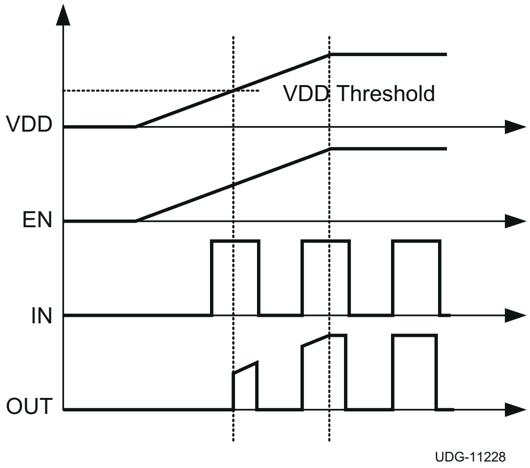


Figure 7-2. Power-Up Sequence

7.2.2.2 Drive Current and Power Dissipation

The UCC27624V driver is capable of delivering 5A of peak current to a switching power device gate (MOSFET, IGBT, SiC MOSFET) for a period of several-hundred nanoseconds at VDD = 12V. High peak current is required to turn ON the device quickly. Then, to turn the device OFF, the driver is required to sink a similar amount of current to ground, which repeats at the operating switching frequency of the power device. The power dissipated in the gate driver device package depends on the following factors:

- Gate charge of the power MOSFET (usually a function of the drive voltage V_{GS}, which is very close to input bias supply voltage V_{DD} due to low V_{OH} drop-out).
- Switching frequency
- External gate resistors

Because UCC27624V features low-quiescent currents and internal logic to eliminate any shoot-through in the output driver stage, their effect on the power dissipation within the gate driver is very small compared to the losses due to switching of the power device.

When a driver device is tested with a discrete capacitive load, calculating the power that is required from the bias supply is fairly simple. The following equation provides an example of the energy that must transfer from the bias supply to charge the capacitor.

$$E_G = \frac{1}{2} C_{LOAD} V_{DD}^2 \tag{1}$$

where

- C_{LOAD} is the load capacitor.
- V_{DD} is the bias voltage of the driver.

There is an equal amount of energy dissipated when the capacitor is discharged. This leads to a total power loss, as shown in the following equation example.

$$P_G = C_{LOAD} V_{DD}^2 f_{SW} \tag{2}$$

where

- f_{SW} is the switching frequency.

With V_{DD} = 12V, C_{LOAD} = 10nF and f_{SW} = 300kHz, the switching power loss is calculated as follows:

$$P_G = 10\,\text{nF} \times 12\,\text{V}^2 \times 300\,\text{kHz} = 0.432\,\text{W} \tag{3}$$

The switching load presented by a power MOSFET is converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Most manufacturers provide specifications that provide the typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Q_g, the power that must dissipate when charging a capacitor is determined, which by using the equivalence $Q_g = C_{LOAD}V_{DD}$ is shown in the following equation.

$$P_G = C_{LOAD} V_{DD}{}^2 f_{SW} = Q_g V_{DD} f_{SW} \tag{4}$$

Assuming that the UCC27624V device is driving power MOSFET with 60nC of gate charge (Q_g = 60nC at V_{DD} = 12V) on one output channel, the gate charge related power loss is calculated using the equation below.

$$P_G = 2\,\text{x}\,60\,\text{nC} \times 12\,\text{V} \times 300\,\text{kHz} = 0.432\,\text{W} \tag{5}$$

This power P_G is dissipated in the resistive elements of the circuit when the MOSFET turns on or turns off. Half of the total power is dissipated when the load capacitor is charged during turn-on, and the other half is dissipated when the load capacitor is discharged during turn-off. When no external gate resistor is employed between the driver and MOSFET/IGBT, this power is completely dissipated inside the driver package. With the use of external gate resistors, the power dissipation is shared between the internal resistance of driver and external gate resistor in accordance to the ratio of the resistances (more power dissipated in the higher resistance component). Based on this simplified analysis, the driver power dissipation during switching is calculated as follows:

$$P_{SW} = 0.5 \times Q_G \times \text{VDD} \times f_{SW} \times \left(\frac{R_{OFF}}{R_{OFF} + R_{GATE}} + \frac{R_{ON}}{R_{ON} + R_{GATE}} \right) \tag{6}$$

where

- $R_{OFF} = R_{OL}$
- $R_{ON} = R_{OH}$(effective resistance of pull-up structure)

The above equation is necessary when the external gate resistor is large enough to reduce the peak current of the driver. In addition to the above gate-charge related power dissipation, dissipation in the driver is related to the power associated with the quiescent bias current consumed by the device to bias all internal circuits such as input stage (with pullup and pulldown resistors), enable, and UVLO sections. As shown in the electrical characteristics table, the quiescent current is less than 1mA. The power loss due to DC current consumption of the driver internal circuit can be calculated as below.

$$P_Q = I_{DD} V_{DD} \tag{7}$$

Assuming total internal current consumption to be 0.6mA (typical) at bias voltage of 12V, the DC power loss in the driver is:

$$P_Q = 0.6\ \text{mA} \times 12\,\text{V} = 7.2\,\text{mW} \tag{8}$$

This power loss is insignificant compared to gate charge related power dissipation calculated earlier.

With a 12V supply, the bias current is estimated as follows, with an additional 0.6mA overhead for the quiescent consumption:

$$I_{DD} \sim \frac{P_G}{V_{DD}} = \frac{0.432\ \text{W}}{12\ \text{V}} = 0.036\ \text{A} \tag{9}$$

If the gate driver is used with inductive load, then special attention should be paid to the ringing on each pin of the gate driver device. The ringing should not exceed the recommended operating rating of the pin.

7.2.3 Application Curves

The figures below show the typical switching characteristics of the UCC27624V device used in high-voltage boost converter application. In this application, the UCC27624V is driving the IGBT switch that has a gate charge of 110nC.

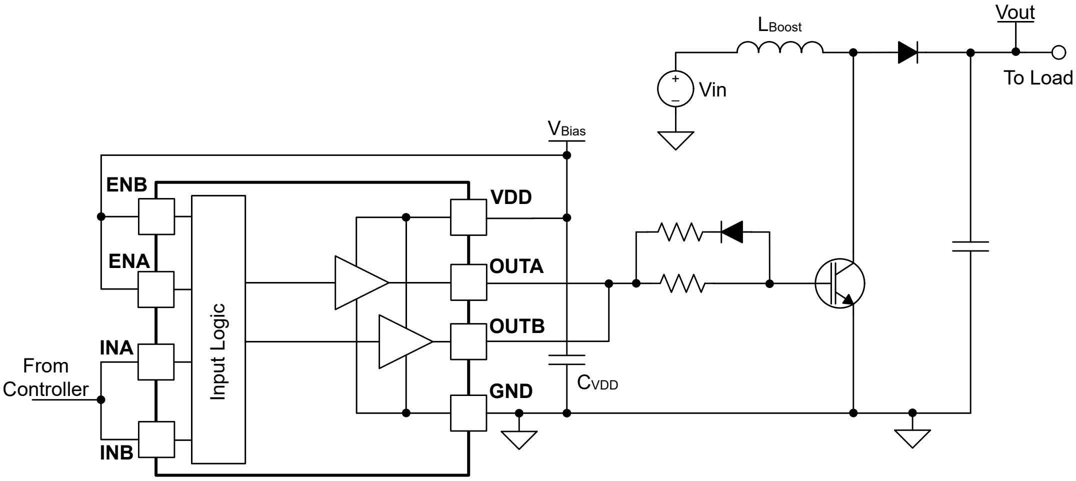
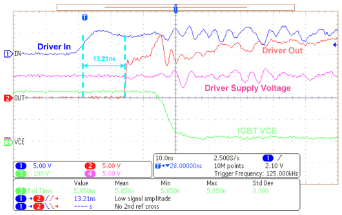


Figure 7-3. UCC27624V Used to Drive IGBT in the Boost Converter

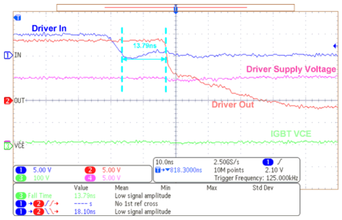


1 5.00 V 2 5.00 V
3 100 V 4 5.00 V
10.0ns 2.50GS/s 1 2.10 V
T→▼28.00000ns 10M points
Trigger Frequency: 125.000kHz

	Value	Mean	Min	Max	Std Dev
3 Fall Time	5.850ns	5.850n	5.850n	5.850n	0.000
1 → 2 ╱╱→	13.21ns	Low signal amplitude			
1 → 2 ╲╲→	---- s	No 2nd ref cross			

Vin = 210V, Vout = 235V, Iout = 1.14A, Fsw = 125kHz, driver supply voltage = 15V, gate resistor = 0Ω

Figure 7-4. Turn-On Propagation Delay Waveform



1 5.00 V 2 5.00 V
3 100 V 4 5.00 V
10.0ns 2.50GS/s 1 2.10 V
T→▼818.3000ns 10M points
Trigger Frequency: 125.000kHz

	Value	Mean	Min	Max	Std Dev
3 Fall Time	13.79ns	Low signal amplitude			
1 → 2 ╱╱→	---- s	No 1st ref cross			
1 → 2 ╲╲→	18.10ns	Low signal amplitude			

Vin = 210V, Vout = 235V, Iout = 1.14A, Fsw = 100kHz, driver supply voltage = 15V, gate resistor = 0Ω

Figure 7-5. Turn-Off Propagation Delay Waveform

7.3 Power Supply Recommendations

The bias supply voltage range for the UCC27624V device is rated to operate is from 9.5V to 26V. The lower end of this range is governed by the internal undervoltage-lockout (UVLO) protection feature on the V_{DD} pin supply circuit blocks. If the driver is in a UVLO condition when the V_{DD} pin voltage is below the VDD UVLO turn-on (rising) threshold, the UVLO protection feature holds the output low, regardless of the status of the inputs. The upper end of this range is driven by the 30V absolute maximum voltage rating of the VDD pin of the device (which is a stress rating). It is necessary to have sufficient margin from the absolute maximum rating of the device to realize full operating life of the device. Therefore, the upper limit of recommended voltage of the VDD pin is 26V.

The UVLO protection feature also has a hysteresis function. This means, when the VDD pin bias voltage exceeds the rising threshold voltage, the device begins to operate normally. If the VDD bias voltage drops below the rising threshold while on, the device continues to deliver normal functionality unless the voltage drop exceeds the hysteresis specification of the falling threshold. Therefore, while operating at or near the 9.5V, design engineer should ensure that the voltage ripple on the auxiliary power supply output is smaller than the hysteresis specification of the device. Otherwise, the device output may turn-off. During system shutdown, the device operation continues until the VDD pin voltage has dropped below the VDD turn-off (falling) threshold, which must be accounted for while evaluating system shutdown timing or sequencing requirements. At system startup, the device does not begin operation until the VDD pin voltage has exceeded VDD turn-on (rising) threshold.

The quiescent current consumed by the internal circuit blocks of the device is supplied through the VDD pin. Although this fact is well known, recognizing that the charge for source current pulses delivered by the OUTA/B pin is also supplied through the same VDD pin capacitor, is important. As a result, every time a current is sourced out of the output pins, a corresponding current pulse is delivered into the device through the VDD pin. Thus, ensure that the local bypass capacitors are provided between the VDD and GND pins and locate them as close to the device pins as possible for the purpose of decoupling. A low ESR, ceramic surface mount capacitor is required. TI recommends having two capacitors: a 0.1µF ceramic surface-mount capacitor placed less than 1mm from the VDD pin of the device and another larger ceramic capacitor (≥1µF) must be connected in parallel.

UCC27624V is a high-current gate driver. If the gate driver is placed far from the switching power device, such as a MOSFET, then that could create a large inductive loop. A large inductive loop may cause excessive ringing on any and all pins of the gate driver. This may result in stress that exceeds device recommended ratings. Therefore, place the gate driver as close to the switching power device as possible. Also, use an external gate resistor to damp any ringing due to the high switching currents and board parasitic elements.

7.4 Layout

7.4.1 Layout Guidelines

Proper PCB layout is extremely important in a high-current fast-switching circuit to provide appropriate device operation and design robustness. The UCC27624V gate driver incorporates small propagation delays and powerful output stages capable of delivering large current peaks with very fast rise and fall times at the gate of power MOSFET to facilitate very quick voltage transitions. Very high di/dt causes unacceptable ringing if the trace lengths and impedances are not well controlled. The following circuit layout guidelines are recommended when designing with these high-speed drivers.

- Place the driver IC as close as possible to the power device in order to minimize the length of high-current traces between the driver IC output pins and the gate of the switching power device.
- Place the VDD bypass capacitors between VDD and GND as close as possible to the driver IC with minimal trace length to improve the noise filtering. These capacitors support high peak current being drawn from VDD pin, during turn-on of power MOSFET. The use of low inductance surface-mounted-device (SMD) components such as 50V rated X7R chip capacitors are highly recommended.
- The turn-on and turn-off current loop paths (driver device, power MOSFET and VDD bypass capacitor) must be minimized as much as possible in order to keep the stray inductance to a minimum. High dI/dt is established in these loops at two instances, namely during turn-on and turn-off transients, which induces significant voltage transients on the output pin of the driver device and Gate of the power MOSFET.
- Wherever possible, parallel the source and return traces to take advantage of flux cancellation.
- Separate power traces and signal traces, such as output and input signals.
- To minimize switch node transients and ringing, adding some gate resistance and/or snubbers on the power devices may be necessary. These measures may also reduce EMI.
- Star-point grounding is a good way to minimize noise coupling from one current loop to another. The GND of the driver is connected to the other circuit nodes such as source of power MOSFET and ground of PWM controller at one, single point. The connected paths must be as short as possible to reduce inductance and be as wide as possible to reduce resistance.

- Use a ground plane to provide noise shielding. Fast rise and fall times at OUT pin of the driver IC may corrupt the input signals of the driver IC. The ground plane must not be a conduction path for any high current (power stage) loop. Instead the ground plane must be connected to the star-point with one single trace to establish the ground potential. In addition to noise shielding, the ground plane can help in power dissipation as well
- External gate resistor and parallel diode-resistor combination may come in handy when replacing any gate driver IC with UCC27624V device in existing or new designs, specifically if they do not have the same drive strength.

7.4.2 Layout Example

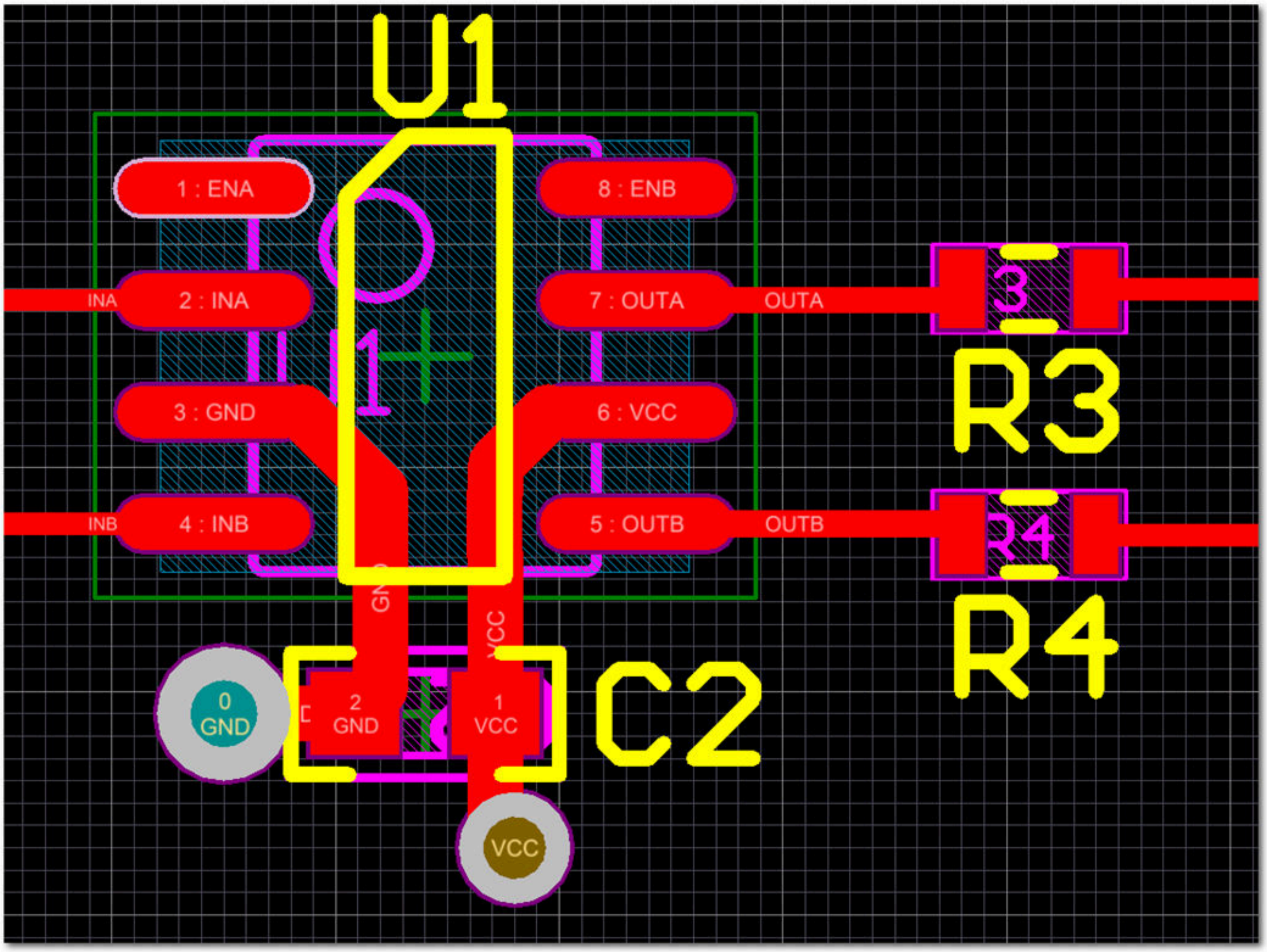


Figure 7-6. UCC27624V Layout Example

7.4.3 Thermal Considerations

The useful range of a driver is greatly affected by the drive power requirements of the load and the thermal characteristics of the device package. In order for a gate driver device to be useful over a particular temperature range, the package must allow for the efficient removal of the heat produced, while keeping the junction temperature within the specified limit. For detailed information regarding the thermal information table, please refer to the *Semiconductor and IC Package Thermal Metrics Application Note* (SPRA953).

Among the different package options available for the UCC27624V device, power dissipation capability of the DGN package is of particular mention. The VSSOP-8 (DGN) package offers thermal pad for removing the heat from the semiconductor junction through the bottom of the package. This pad is soldered to the copper on the printed circuit board directly underneath the device package, reducing the thermal resistance to a very low value. This allows a significant improvement in heat-sinking over the D package. The printed circuit board must be designed with thermal lands and thermal vias to complete the heat removal subsystem. Note that the exposed pads in the VSSOP-8 package are not directly connected to any leads of the package, however, PowerPAD is thermally connected to the substrate of the device. TI recommends to externally connect the exposed pads to GND pin of the driver IC in PCB layout.

8 Device and Documentation Support

8.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

PowerPAD™ is a trademark of Texas Instruments.
TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (March 2025) to Revision A (March 2026)	Page
• Added DDA and DGK packages to Package Information	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC27624VDGNR	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	624V
UCC27624VDGNR.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	624V
UCC27624VDR	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	27624V

[1] **Status:** For more details on status, see our product life cycle.

[2] **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

[3] **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

[4] **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[5] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF UCC27624V :

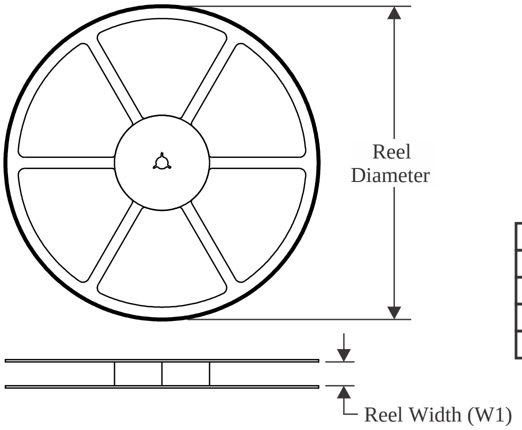
- Automotive : UCC27624V-Q1

NOTE: Qualified Version Definitions:

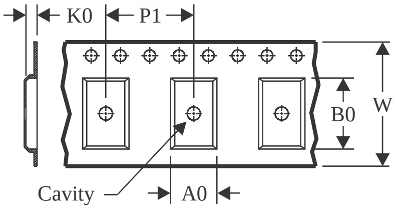
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

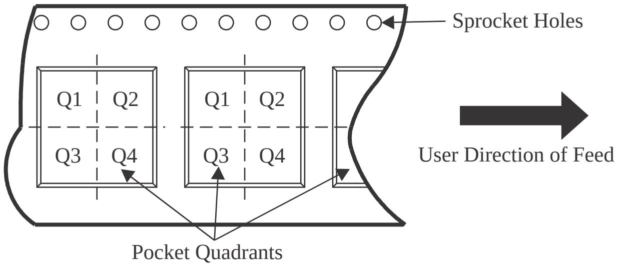


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

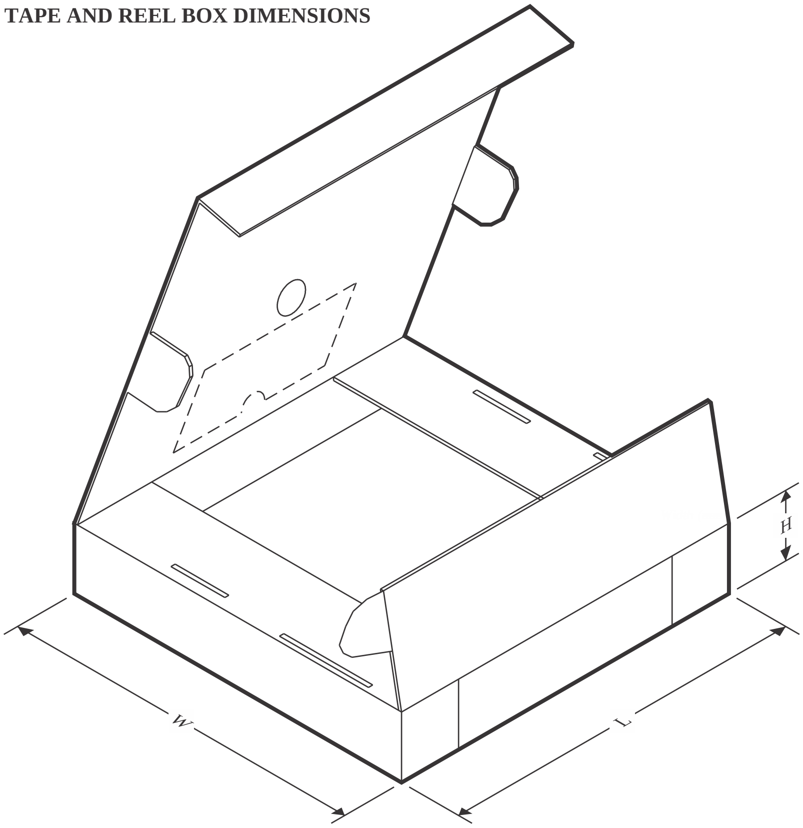
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27624VDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC27624VDR	SOIC	D	8	3000	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27624VDGNR	HVSSOP	DGN	8	2500	353.0	353.0	32.0
UCC27624VDR	SOIC	D	8	3000	340.5	336.1	25.0

GENERIC PACKAGE VIEW

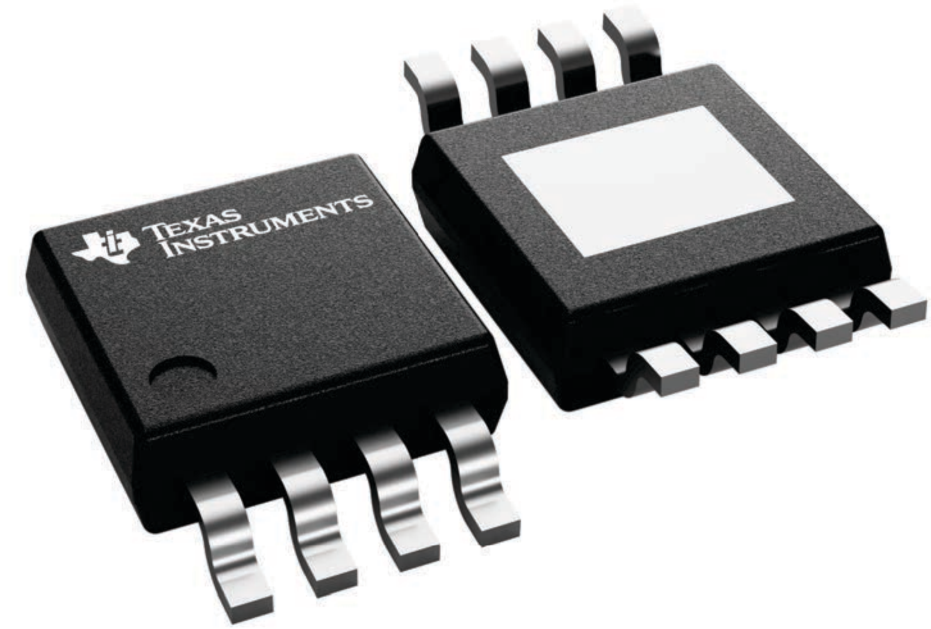
DGN 8

PowerPAD™ HVSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

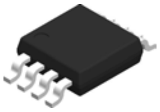
SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/B

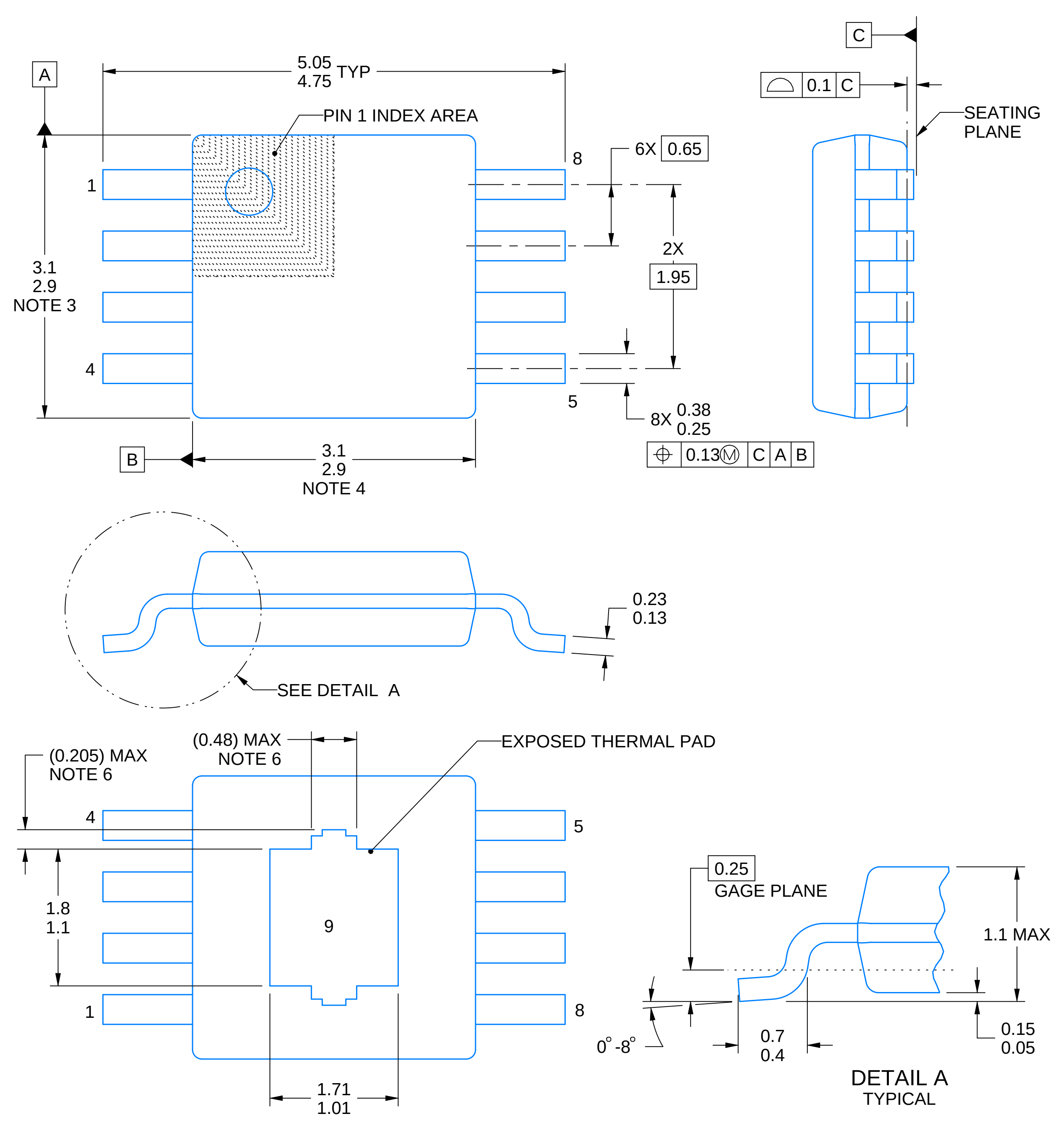
PACKAGE OUTLINE



DGN0008H

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

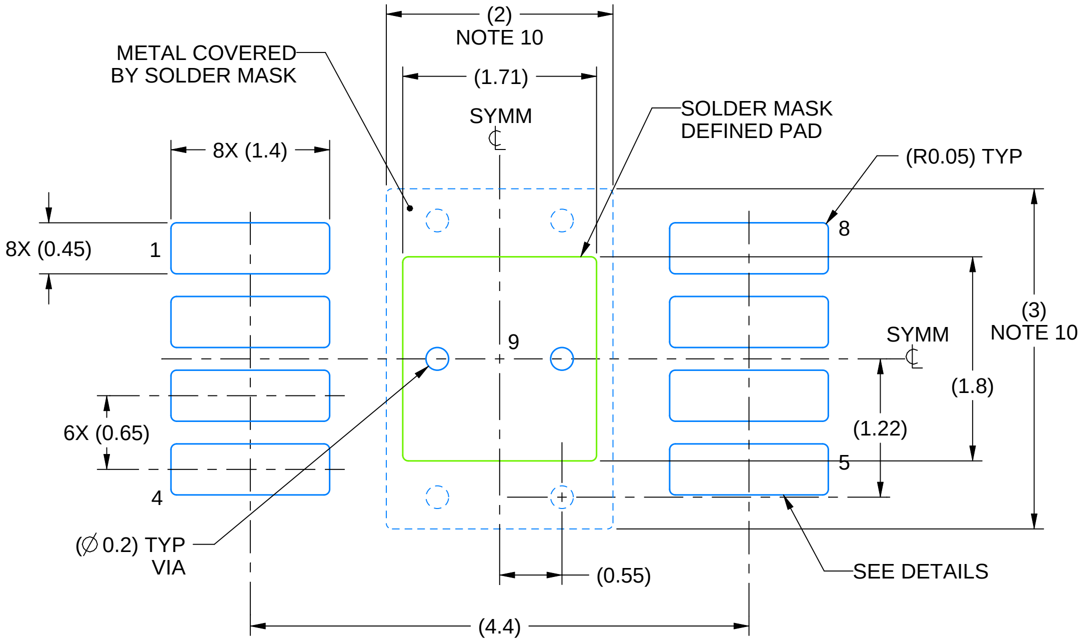


4229130/B 05/2024

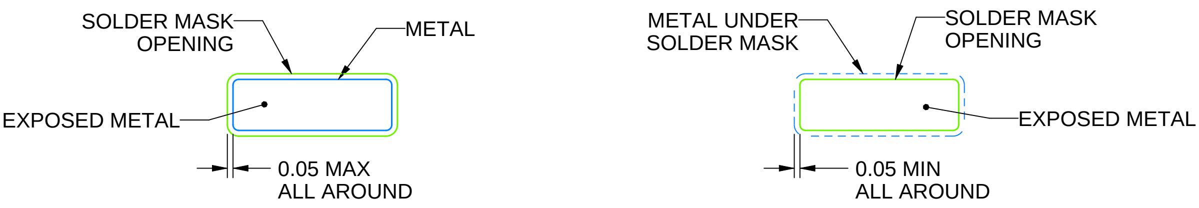
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.
6. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



NON-SOLDER MASK
DEFINED
(PREFERRED)

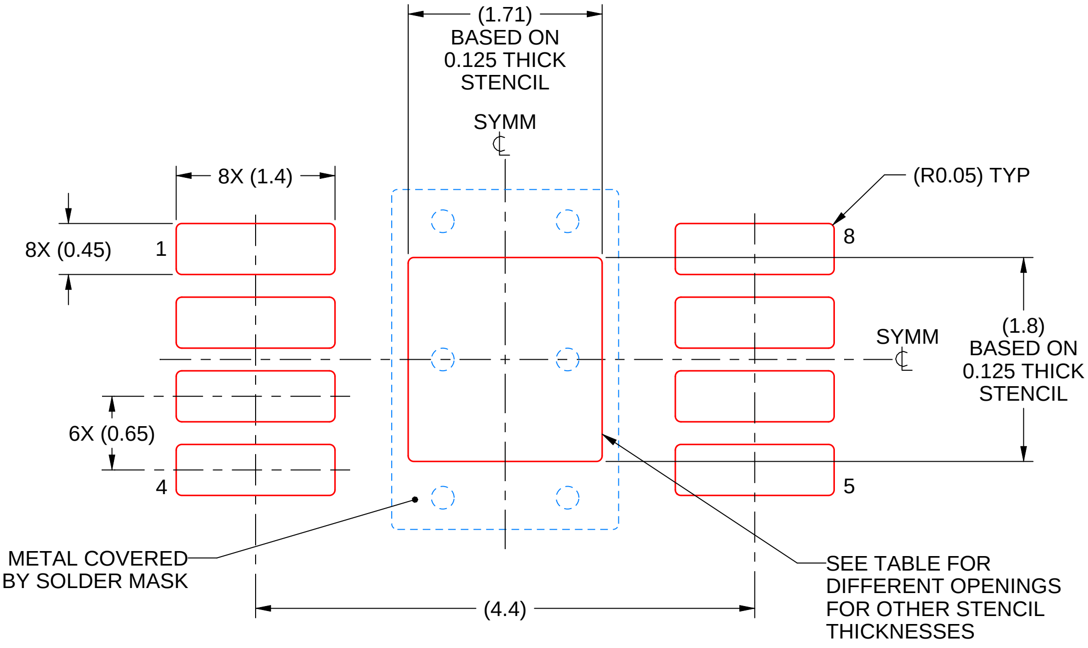
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4229130/B 05/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
9. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.

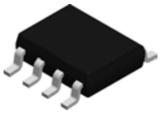


SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.91 X 2.01
0.125	1.71 X 1.80 (SHOWN)
0.15	1.56 X 1.64
0.175	1.45 X 1.52

NOTES: (continued)

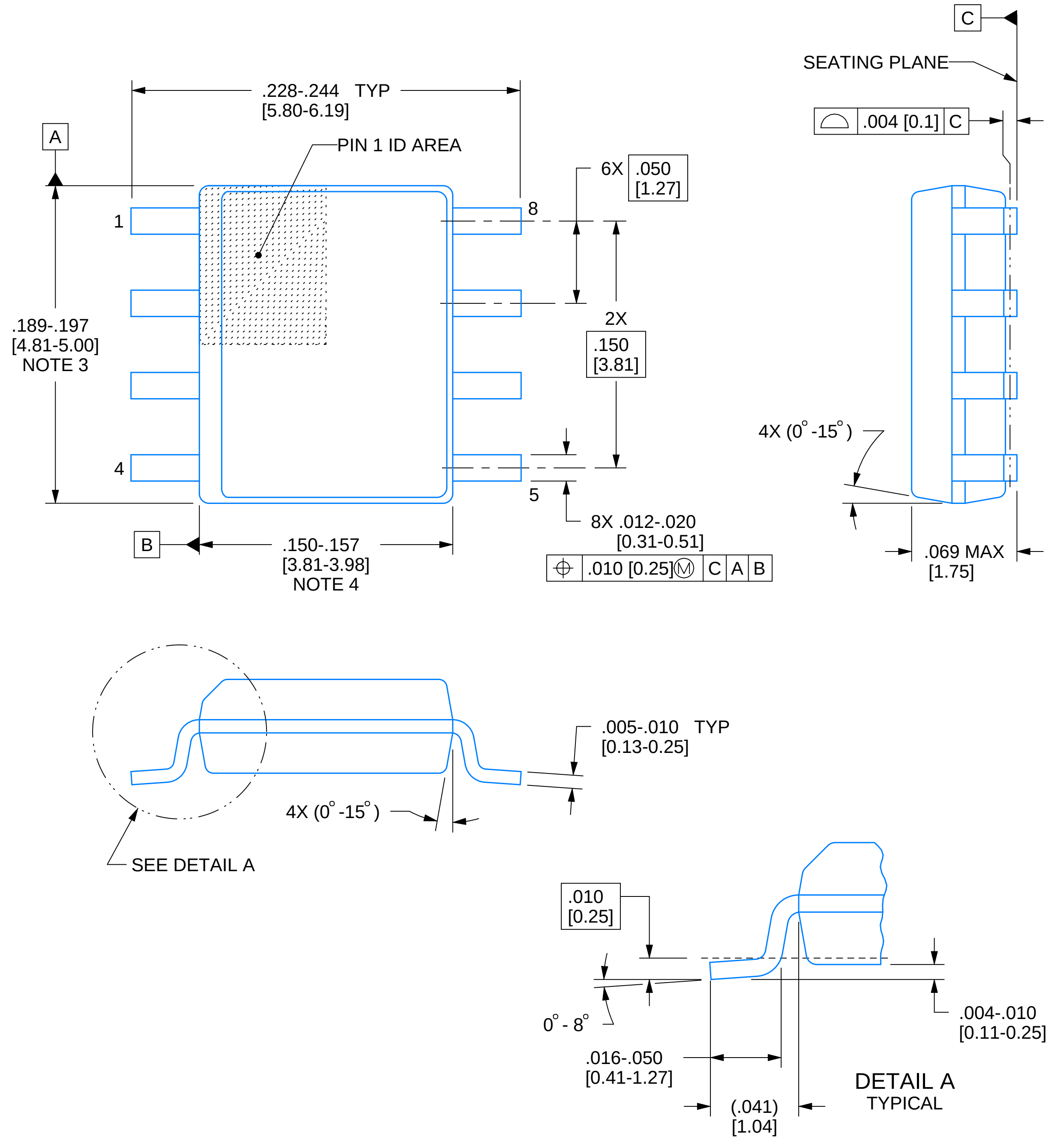
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.



PACKAGE OUTLINE

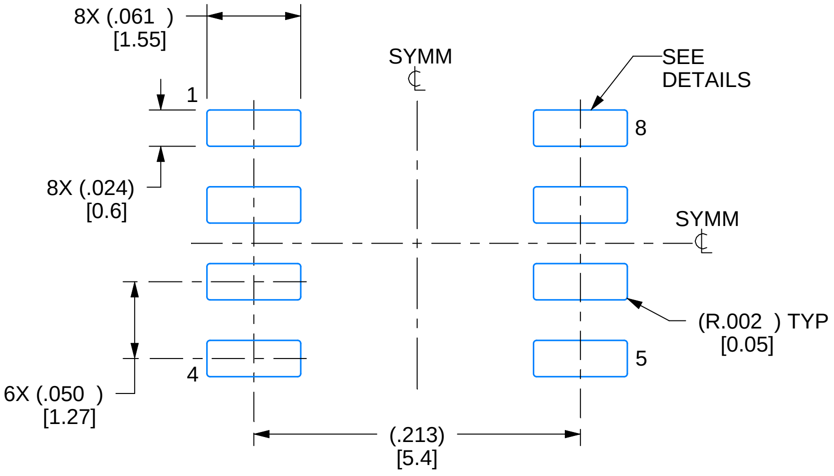
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

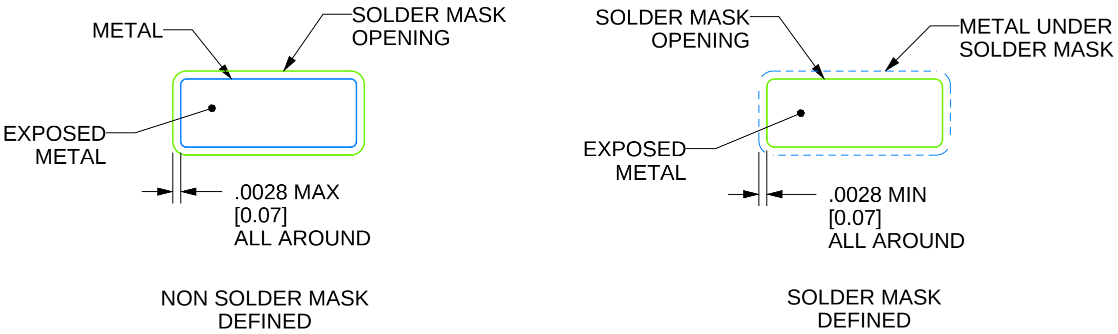


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

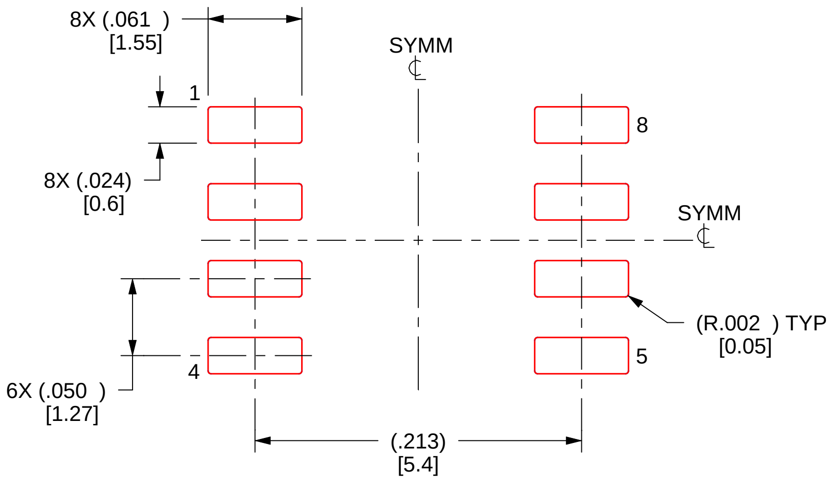


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025