UCC2808A-xEP Low-Power Current Mode Push-Pull PWM

1 Features

- Supports Defense and Aerospace applications
- Controlled baseline:
  - One assembly or test site, one fabrication site
- Extended product life cycle
- Product traceability
- Extended temperature performance: −55°C to +125°C
- Dual output drive stages in push-pull configuration
- Current-sense discharge transistor to improve dynamic response
- Typical starting current: 130µA
- Typical run current: 1mA
- Operation to 1MHz
- Internal soft-start
- On-chip error amplifier with 2MHz gain bandwidth product
- On-chip VDD clamping
- Output drive stages capable of 500mA peak-source current, 1A peak-sink current

2 Applications

- Aerospace and defense
- Industrial automation

3 Description

The UCC2808A-xEP is a family of BiCMOS push-pull, high-speed, low-power, pulse-width modulators. The UCC2808A-xEP contains all of the control and drive circuitry required for off-line or DC/DC fixed frequency current-mode switching power supplies with a minimal external parts count.

The UCC2808A-xEP dual output drive stages are arranged in a push-pull configuration. Both outputs switch at half the oscillator frequency using a toggle flip-flop. The dead time between the two outputs is typically 60ns to 200ns, depending on the values of the timing capacitor and resistors. The output stage duty cycle is limited to less than 50%.

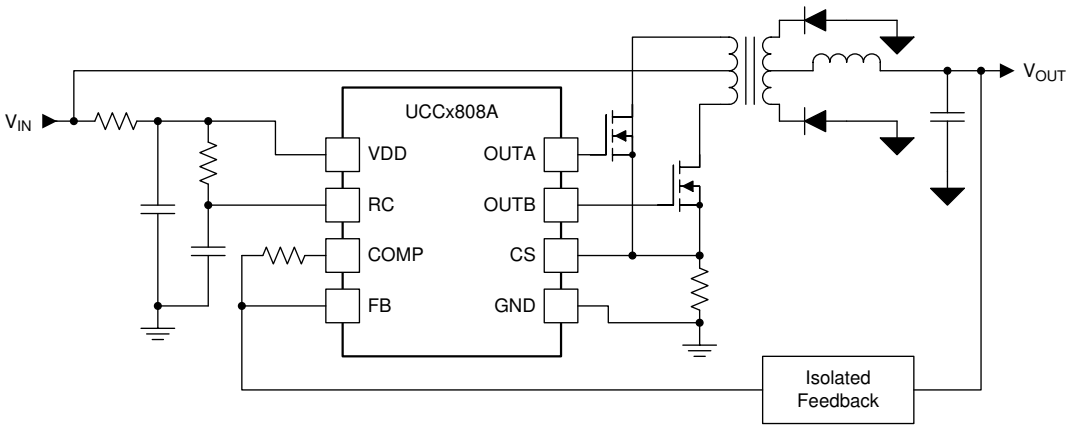
The UCC2808A-xEP family offers a variety of package options and choice of undervoltage lockout levels. The family has UVLO thresholds and hysteresis options for off-line and battery-powered systems. Thresholds are shown in Device Comparison Table.

The UCC2808A-xEP is an enhanced version of the UCC2808 family. The significant difference between families is that the *A* versions feature an internal discharge transistor from the CS pin to ground, which is activated each clock cycle during the oscillator dead time. The internal discharge transistor discharges any filter capacitance on the CS pin during each cycle and helps minimize filter capacitor values and current-sense delay.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
UCC2808A-1EP	D (SOIC, 8)	4.9mm × 6.0mm
UCC2808A-2EP		

(1) For all available packages, see the Mechanical, Packaging, and Orderable Information.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



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4 Device Comparison Table

DEVICE NAME	T_A	UVLO OPTION
UCC2808A-1EP	−40°C to +125°C	12.5V, 8.3V
UCC2808A-2EP	−40°C to +125°C	4.3V, 4.1V

5 Pin Configuration and Functions

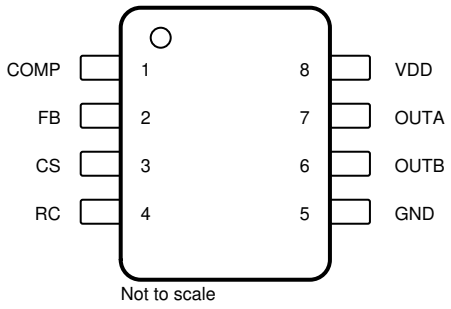


Figure 5-1. UCC2808A-xEP: D Package, 8-Pin SOIC (Top View)

Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
COMP	1	O	COMP is the output of the error amplifier and the input of the PWM comparator. The error amplifier in the UCC2808A-xEP is a true low-output impedance, 2MHz operational amplifier. As such, the COMP pin both sources and sinks current. However, the error amplifier is internally current limited, so that zero duty cycle is externally forced by pulling COMP to GND. The UCCx808A family features built-in full-cycle soft start. Soft start is implemented as a clamp on the maximum COMP voltage.
CS	3	I	The input to the PWM, peak current, and overcurrent comparators. The overcurrent comparator is only intended for fault sensing. Exceeding the overcurrent threshold causes a soft-start cycle. An internal MOSFET discharges the current sense filter capacitor to improve dynamic performance of the power converter.
FB	2	I	The inverting input to the error amplifier. For best stability, keep FB lead length as short as possible and FB stray capacitance as small as possible.
GND	5	G	Reference ground and power ground for all functions. Because of high currents, and high-frequency operation of the UCC2808A-xEP, a low-impedance circuit board ground plane is highly recommended.
OUTA	7	O	Alternating high current output stages. Both stages are capable of driving the gate of a power MOSFET. Each stage is capable of 500mA peak-source current and 1A peak-sink current. The output stages switch at half the oscillator frequency, in a push-pull configuration. When the voltage on the RC pin is rising, one of the two outputs is high, but during fall time, both outputs are off. This *dead time* between the two outputs, along with a slower output rise time than fall time, prevents the two outputs from simultaneous activity. This dead time is typically 60ns to 200ns and depends upon the values of the timing capacitor and resistor. The high-current-output drivers consist of MOSFET output devices, which switch from VDD to GND. Each output stage also provides a very low impedance to overshoot and undershoot. This configuration means that in many cases, external Schottky-clamp diodes are not required.
OUTB	6	O	Alternating high current output stages. Both stages are capable of driving the gate of a power MOSFET. Each stage is capable of 500mA peak-source current and 1A peak-sink current. The output stages switch at half the oscillator frequency, in a push-pull configuration. When the voltage on the RC pin is rising, one of the two outputs is high. During fall time, both outputs are off. The *dead time* between the two outputs and a slower output rise time than fall time, prevents the two outputs from simultaneous activity. This dead time is typically 60ns to 200ns and depends upon the values of the timing capacitor and resistor. The high-current output drivers consist of MOSFET output devices, which switch from VDD to GND. Each output stage also provides a very low impedance to overshoot and undershoot. This configuration means that in many cases, external Schottky-clamp diodes are not required.

Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
RC	4	O	The oscillator programming pin. The UCC2808A-xEP oscillator tracks VDD and GND internally so that variations in power supply rails minimally affect frequency stability. Section 7.2 shows the oscillator block diagram. Only two components are required to program the oscillator: a resistor (tied to the VDD and RC), and a capacitor (tied to the RC and GND). The approximate oscillator frequency is calculated in Section 7.3.1.6. The recommended range of timing resistors is between 10kΩ and 200kΩ and range of timing capacitors is from 100pF to 1000pF. Avoid timing resistors smaller than 10kΩ. For best performance, keep the timing capacitor lead to GND as short as possible, the timing resistor lead from VDD as short as possible, and the leads between timing components and RC as short as possible. Separate ground and VDD traces to the external timing network are encouraged.
VDD	8	P	The power input connection for this device. Although quiescent VDD current is very low, total supply current is higher, depending on OUTA and OUTB current and the programmed oscillator frequency. Total VDD current is the sum of quiescent VDD current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Qg), average OUT current is calculated in Section 7.3.1.7. To prevent noise problems, bypass VDD to GND with a ceramic capacitor as close to the chip as possible along with an electrolytic capacitor. A 1µF decoupling capacitor is recommended.

(1) P = Power, G = Ground, I = Input, O = Output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

			MIN	MAX	UNIT
	Supply voltage (IDD ≤ 10mA)			15	V
	Supply current			20	mA
	OUTA/OUTB source current (peak)			–0.5	A
	OUTA/OUTB sink current (peak)			1	A
	Analog inputs (FB, CS)		–0.3	VDD + 0.3 (not to exceed 6)	V
	Power dissipation at T_A = 25°C	D package		650	mW
T_J	Junction temperature		–55	150	°C
T_{stg}	Storage temperature		–65	150	°C
	Lead temperature (soldering, 10 sec.)			300	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Currents are positive into, negative out of the specified terminal. Consult the packaging section of the *Power Supply Control Products Data Book* for thermal limitations and considerations of packages.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{DD}	Supply voltage	UCC2808A-1EP	13	14	V
		UCC2808A-2EP	5	14	
T_J	Junction temperature	UCC2808A-xEP	–55	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	118.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	66	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	62.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

6.5 Electrical Characteristics

T_A = –40°C to +125°C for the UCC2808A-xEP, VDD = 10V(1), 1µF capacitor from VDD to GND, R = 22kΩ, C = 330pF, and T_A = T_J (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OSCILLATOR						
	Oscillator frequency		175	194	213	kHz
	Oscillator amplitude/VDD(2)		0.44	0.5	0.56	V/V
ERROR AMPLIFIER						
	Input voltage	COMP = 2V	1.95	2	2.05	V
	Input bias current		–1		1	µA
	Open loop voltage gain		60	80		dB
	COMP sink current	FB = 2.2V, COMP = 1V	0.3	2.5		mA
	COMP source current	FB = 1.3V, COMP = 3.5V	–0.2	–0.5		mA
PWM						
	Maximum duty cycle	Measured at OUTA or OUTB	48%	49%	50%	
	Minimum duty cycle	COMP = 0V			0%	
CURRENT SENSE						
	Gain(3)		1.9	2.2	2.5	V/V
	Maximum input signal	COMP = 5V(4)	0.45	0.5	0.55	V
	CS to output delay	COMP = 3.5V, CS from 0mV to 600mV		100	200	ns
	CS source current		–200			nA
	CS sink current	CS = 0.5V, RC = 5.5V(5)	4	10		mA
	Over current threshold		0.65	0.75	0.85	V
	COMP to CS offset	CS = 0V	0.35	0.8	1.2	V
OUTPUT						
	OUT low level	I = 100mA		0.5	1.1	V
	OUT high level	I = –50mA, VDD – OUT		0.5	1	V
	Rise time	C_L = 1nF		25	60	ns
	Fall time	C_L = 1nF		25	60	ns
UNDERVOLTAGE LOCKOUT						
	Start threshold	UCC2808A-1EP(1)	11.5	12.5	13.5	V
		UCC2808A-2EP	4.1	4.3	4.5	
	Minimum operating voltage after start	UCC2808A-1EP	7.6	8.3	9	V
		UCC2808A-2EP	3.9	4.1	4.3	
	Hysteresis	UCC2808A-1EP	3.5	4.2	5.1	V
		UCC2808A-2EP	0.1	0.2	0.3	
SOFT START						
	COMP rise time	FB = 1.8V, rise from 0.5V to 4V		3.5	20	ms
OVERALL						
	Start-up current	VDD < start threshold		130	260	µA
	Operating supply current	FB = 0V, CS = 0V(1) (6)		1	2	mA
	VDD zener shunt voltage	IDD = 10mA(7)	13	14	15	V

(1) For UCC2808A-1EP, set VDD above the start threshold before setting at 10V.
(2) Measured at RC. Signal amplitude tracks VDD.
(3) Gain is defined by: A = ΔV_{COMP} / ΔV_{CS}, 0V ≤ V_{CS} ≤ 0.4V.
(4) Parameter measured at trip point of latch with FB at 0V.
(5) The internal current sink on the CS pin is designed to discharge an external filter capacitor, and is not intended to be a DC sink path.
(6) Does not include current in the external oscillator network.
(7) Start threshold and zener shunt threshold track together.

6.6 Typical Characteristics

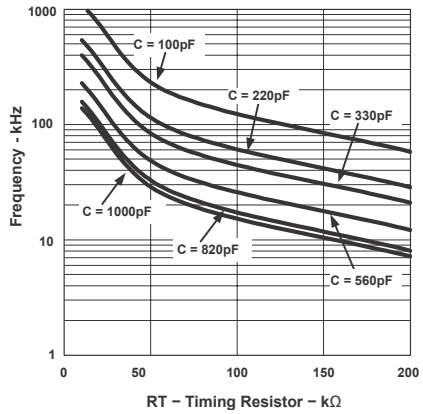


Figure 6-1. Oscillator Frequency vs External RC Values

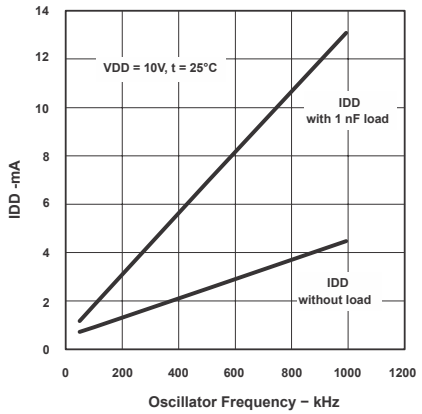


Figure 6-2. IDD vs Oscillator Frequency

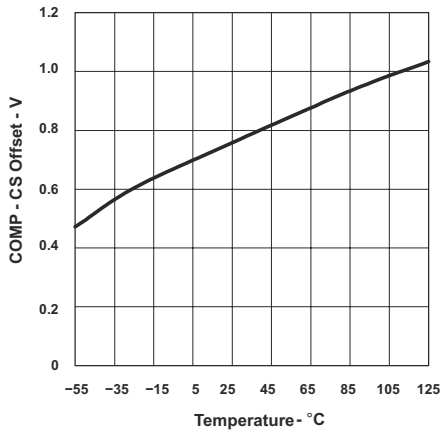


Figure 6-3. COMP to CS Offset vs Temperature

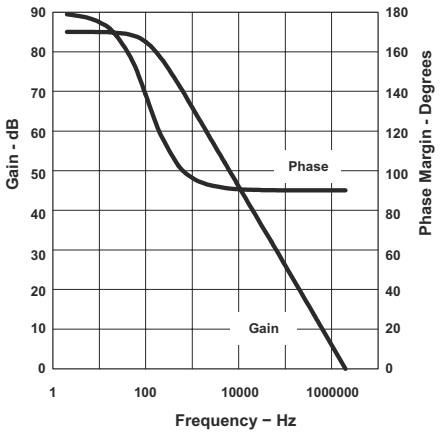


Figure 6-4. Error Amplifier Gain and Phase Response vs Frequency

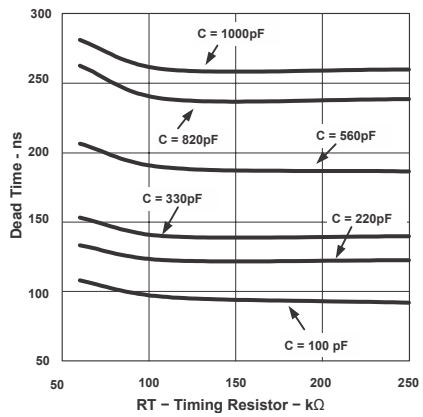


Figure 6-5. Output Dead Time vs External RC Values

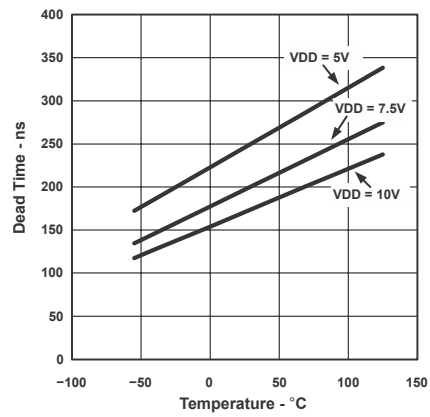


Figure 6-6. Dead Time vs Temperature

6.6 Typical Characteristics (continued)

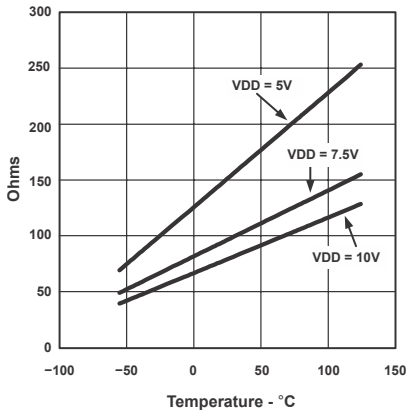


Figure 6-7. RC $R_{DS(on)}$ vs Temperature

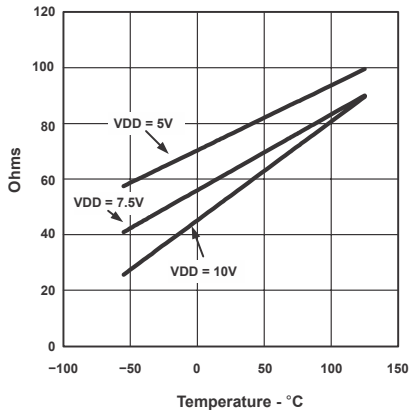


Figure 6-8. CS $R_{DS(on)}$ vs Temperature

7 Detailed Description

7.1 Overview

The UCC2808A-xEP device is a highly integrated, low-power current mode push-pull PWM controller. The controller employs low starting current and an internal control algorithm that offers accurate output voltage regulation in the presence of line and load variations. The UCC2808A-xEP family of parts has UVLO thresholds and hysteresis options for off-line and battery-powered systems.

Table 7-1. Undervoltage Lockout Levels

PART NUMBER	TURNON THRESHOLD	TURNOFF THRESHOLD
UCC2808A-1EP	12.5	8.3
UCC2808A-2EP	4.3	4.1

7.2 Functional Block Diagrams

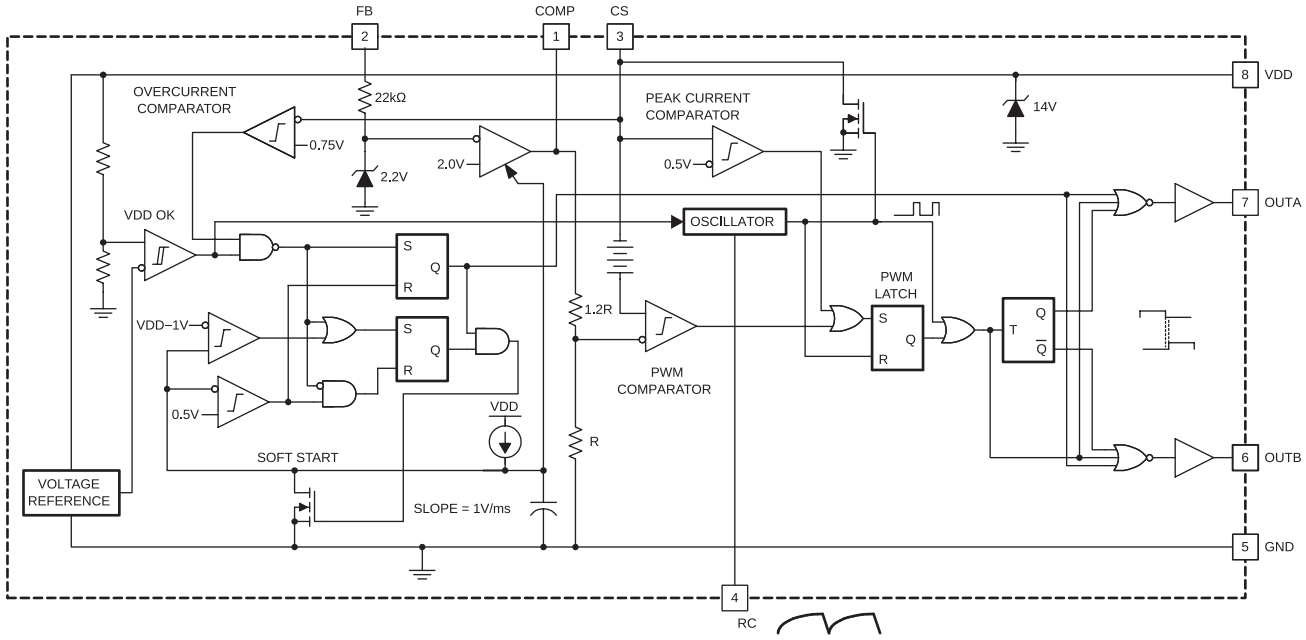
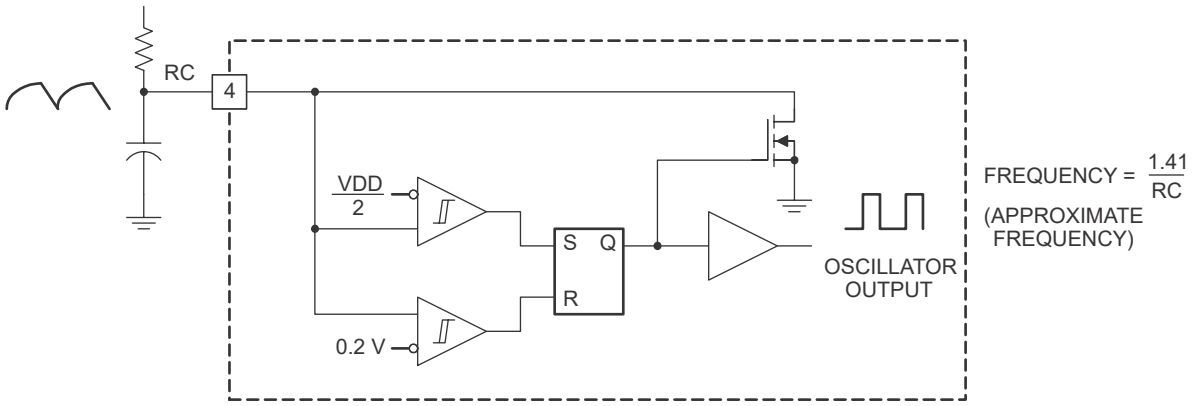


Figure 7-1. Block Diagram



Note: The oscillator generates a sawtooth waveform on RC. During the RC rise time, the output stages alternate on time, but both stages are off during the RC fall time. The output stages switch a 1/2 the oscillator frequency, with specified duty cycle of < 50% for both outputs.

Figure 7-2. Block Diagram of Oscillator

7.3 Feature Description

7.3.1 Pin Descriptions

7.3.1.1 COMP

The COMP pin is the output of the error amplifier and the input of the PWM comparator. The error amplifier in the UCC2808A-xEP is a true low-output impedance, 2MHz operational amplifier. As such, the COMP pin both sources and sinks current. However, the error amplifier is internally current limited, so the zero duty cycle is externally forced by pulling COMP to GND.

The UCC2808A-xEP family features built-in full cycle soft start. Soft start is implemented as a clamp on the maximum COMP voltage.

7.3.1.2 CS

The input to the PWM, peak current, and overcurrent comparators. The overcurrent comparator is only intended for fault sensing. Exceeding the overcurrent threshold causes a soft-start cycle.

7.3.1.3 FB

The inverting input to the error amplifier. For best stability, keep FB lead length as short as possible and FB stray capacitance as small as possible.

7.3.1.4 GND

Reference ground and power ground for all functions. Because of high currents, and high-frequency operation of the UCC2808A-xEP, a low-impedance printed-circuit board ground plane is highly recommended.

7.3.1.5 OUTA and OUTB

Alternating high current output stages. Both stages are capable of driving the gate of a power MOSFET. Each stage is capable of 500mA peak source current, and 1A peak sink current.

The output stages switch at half the oscillator frequency, in a push-pull configuration. When the voltage on the RC pin is rising, one of the two outputs is high, but during fall time, both outputs are off. This dead time between the two outputs, along with a slower output rise time than fall time, insures that the two outputs can not be on at the same time. This dead time is typically 60ns to 200ns, and depends upon the values of the timing capacitor and resistor.

The high-current output drivers consist of MOSFET output devices, which switch from VDD to GND. Each output stage also provides a very low impedance to overshoot and undershoot. This provision means that in many cases, external Schottky clamp diodes are not required.

7.3.1.6 RC

The oscillator programming pin. The oscillator of the UCC2808A-xEP tracks VDD and GND internally, so that variations in power supply rails minimally affect frequency stability. Section 7.2 shows the oscillator block diagram.

Only two components are required to program the oscillator: a resistor (tied to the VDD and RC), and a capacitor (tied to the RC and GND). Equation 1 determines the approximate oscillator frequency.

$$f_{OSCILLATOR} = \frac{1.41}{RC} \quad (1)$$

where

- frequency is in Hz
- resistance in Ω
- capacitance in Farads

The recommended range of the timing resistors is from 10kΩ to 200kΩ, and range of the timing capacitors is from 100pF to 1000pF. Avoid timing resistors smaller than 10kΩ.

For best performance, keep the timing capacitor lead to GND as short as possible, the timing resistor lead from VDD as short as possible, and the leads between timing components and RC as short as possible. Separate ground and VDD traces to the external timing network are encouraged.

7.3.1.7 VDD

The VDD pin is the power input connection for this device. Although quiescent VDD current is very low, total supply current is higher, depending on OUTA and OUTB current, and the programmed oscillator frequency. Total VDD current is the sum of quiescent VDD current and the average OUT current. Using the operating frequency and the MOSFET gate charge (Q_g), Equation 2 calculates the average OUT current.

$$I_{OUT} = Q_g \times f \quad (2)$$

where

- f is frequency

To prevent noise problems, bypass VDD to GND with a ceramic capacitor as close to the chip as possible along with an electrolytic capacitor. TI recommends a 1µF decoupling capacitor.

7.4 Device Functional Modes

7.4.1 VCC

When VCC rises above 12.5V (for the UCC2808A-1EP) or above 4.3V (for the UCC2808A-2EP) the device is enabled. When any fault conditions are cleared, a soft-start condition is initiated and the gate driver outputs begin switching.

When VCC drops below 8.3V (for the UCC2808A-1EP) or 4.1V (for the UCC2808A-2EP) the device enters the UVLO protection mode and both gate drivers are actively pulled low.

7.4.2 Push-Pull or Half-Bridge Function

Because the UCC2808A-xEP provide alternate 180° out-of-phase gate drive signals (OUTA and OUTB), these devices are excellent for use as a controller for push-pull or half-bridge topologies. For half-bridge topology, the UCC2808A-xEP device requires an external high side gate driver or pulse transformer on one or both of the OUTA and OUTB signals.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

Figure 8-1 shows a 200kHz push-pull application circuit with a full-wave rectifier. The output, V_O, provides 5V at 50W maximum and is electrically isolated from the input. Because the UCC2808A-xEP is a peak-current-mode controller, the 2N2907 emitter following amplifier (buffers the CT waveform) provides slope compensation that is necessary for duty ratios greater than 50%. Capacitor decoupling is very important with a single-ground IC controller. TI recommends using a 1µF capacitor that is placed as close to the IC as possible. The controller supply is a series RC for start-up, paralleled with a bias winding on the output inductor used in steady-state operation.

Isolation is provided by an optocoupler with regulation done on the secondary side using the TL431 adjustable precision shunt regulator. Small-signal compensation with tight voltage regulation is achieved using this part on the secondary side. Many choices exist for the output inductor depending on cost, volume, and mechanical strength. Several design options are iron powder, molypermalloy (MPP), or a ferrite core with an air gap as shown here. The main power transformer has a Magnetics Inc. ER28-size core made of P material for efficient operation at this frequency and temperature. The input voltage ranges from 36Vdc to 72Vdc.

8.2 Typical Application

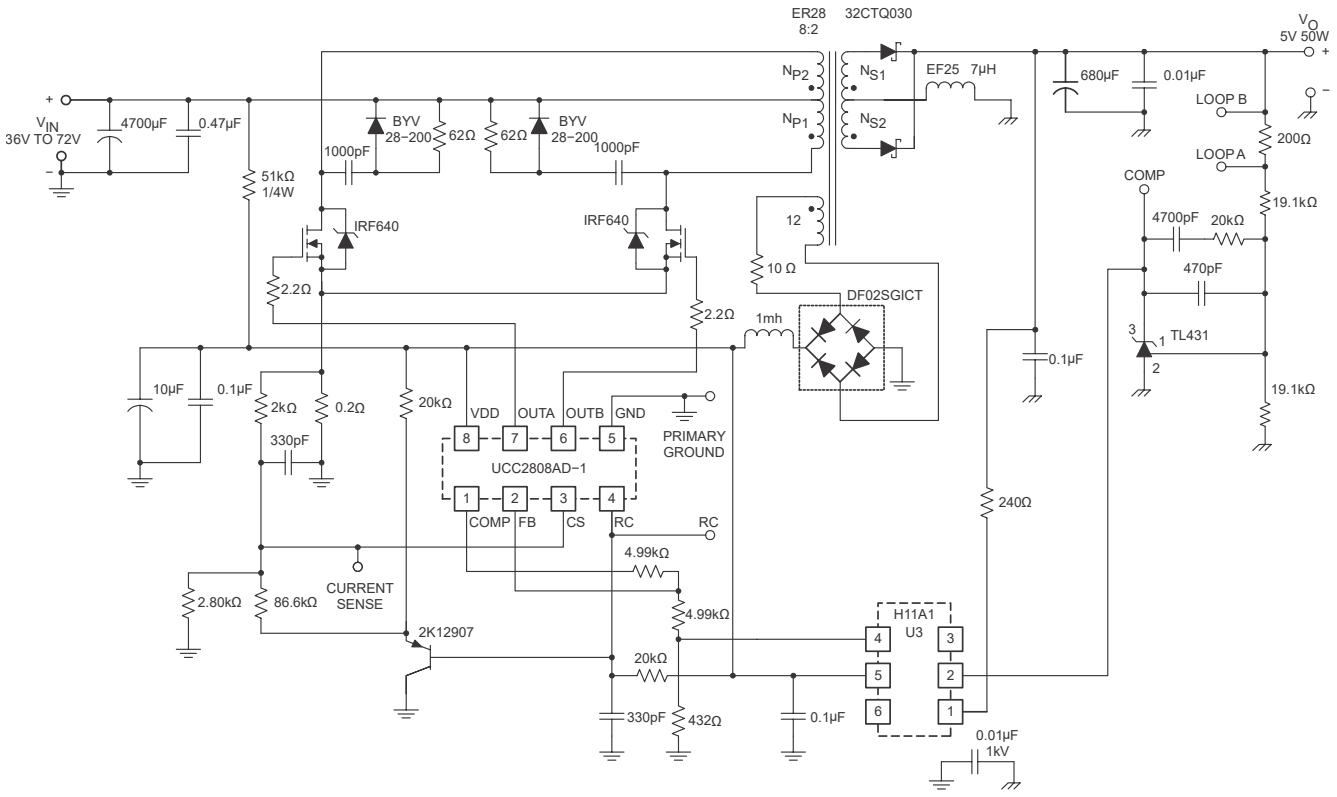


Figure 8-1. Typical Application Diagram: 48Vin, 5V, 50W Output

8.2.1 Design Requirements

Table 8-1 lists the design parameters for the UCC2808A-xEP.

Table 8-1. Design Parameters

PARAMETER	VALUE
Output voltage	5V
Rated output power	50W
Input DC voltage range	36V to 72V
Switching frequency	210kHz

8.2.2 Detailed Design Procedure

The output, V_O, provides 5V at 50W maximum and is electrically isolated from the input. Because the UCC2808A-xEP is a peak current mode controller, the 2N2907 emitter follower amplifier buffers the oscillator waveform (RC pin) and provides slope compensation to the current sense (CS) input. This configuration is necessary for duty cycle ratios greater than 50%.

Capacitor decoupling is provided on the VDD pin. TI recommends using a minimum decoupling capacitance of 10µF electrolytic and 0.1µF ceramic. Place the ceramic capacitor as close to the VDD pin as possible. The UCC2808A-xEP is initially powered up from the 36V to 72V input supply. After the power supply has started, the bias supply is provided by an auxiliary winding on the main power transformer.

Isolation is provided by an optocoupler with regulation done on the secondary side using the TL431 precision programmable reference. The internal error amplifier of the UCC2808A-xEP is set up as a unity gain amplifier and the compensation network is provided on the secondary side.

Many choices exist for the output inductor depending on cost and size constraints. Design options are powdered iron, molypermalloy, or the ferrite core option used in this design. The power transformer is a low profile design, EFD25 size, using the Magnetics Inc. P material. This material is a good choice for low power loss at high switching frequency.

The switching frequency is set at 210kHz with the RC network on the RC pin.

8.2.3 Application Curves

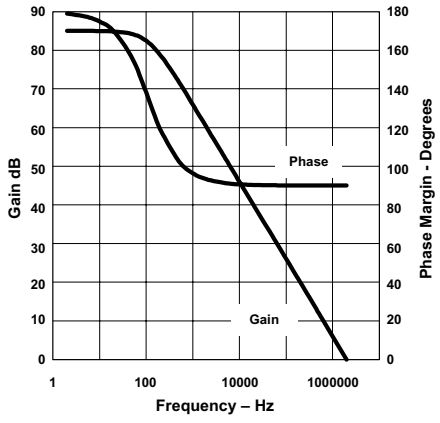


Figure 8-2. Error Amplifier Gain and Phase Response vs Frequency

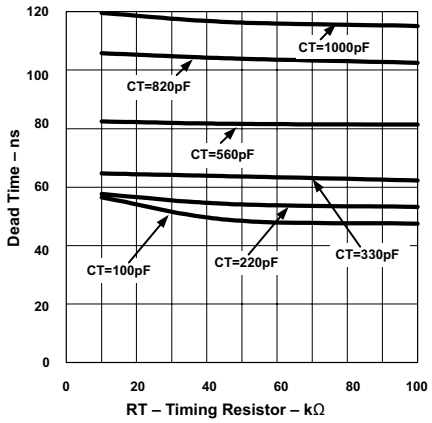


Figure 8-3. Dead Time vs Timing Resistor

8.3 Power Supply Recommendations

The VDD power terminal for these devices requires the placement of electrolytic capacitor as energy storage capacitor because of the 1A drive capability of the UCC2808A-xEP controller. A low-ESR noise decoupling capacitor is also required; place this capacitor as close as possible to the VDD and GND pins. Ceramic

capacitors with stable dielectric characteristics over temperature are recommended. X7R is a good dielectric material for use here.

TI recommends a 10µF, 25V electrolytic capacitor.

8.4 Layout

8.4.1 Layout Guidelines

1. Place the VDD capacitor as close as possible between the VDD pin and GND of the UCC2808A-xEP, tracked directly to both pins.
2. A small, external filter capacitor is recommended on the CS pin. Track the filter capacitor as directly as possible from the CS to GND pins.
3. The tracking and layout of the FB pin and connecting components is critical to minimizing noise pickup and interference. Reduce the total surface area of traces on the FB net to a minimum.
4. The OUTA and OUTB pins have a high-current source and sink capability. An external gate resistor is recommended to damp oscillations. A value of approximately a few ohms (Ω) is recommended. A pulldown resistor on the gate to source is recommended to prevent the MOSFET gate from floating on if there is an open-circuit fault in the gate drive path.

8.4.2 Layout Example

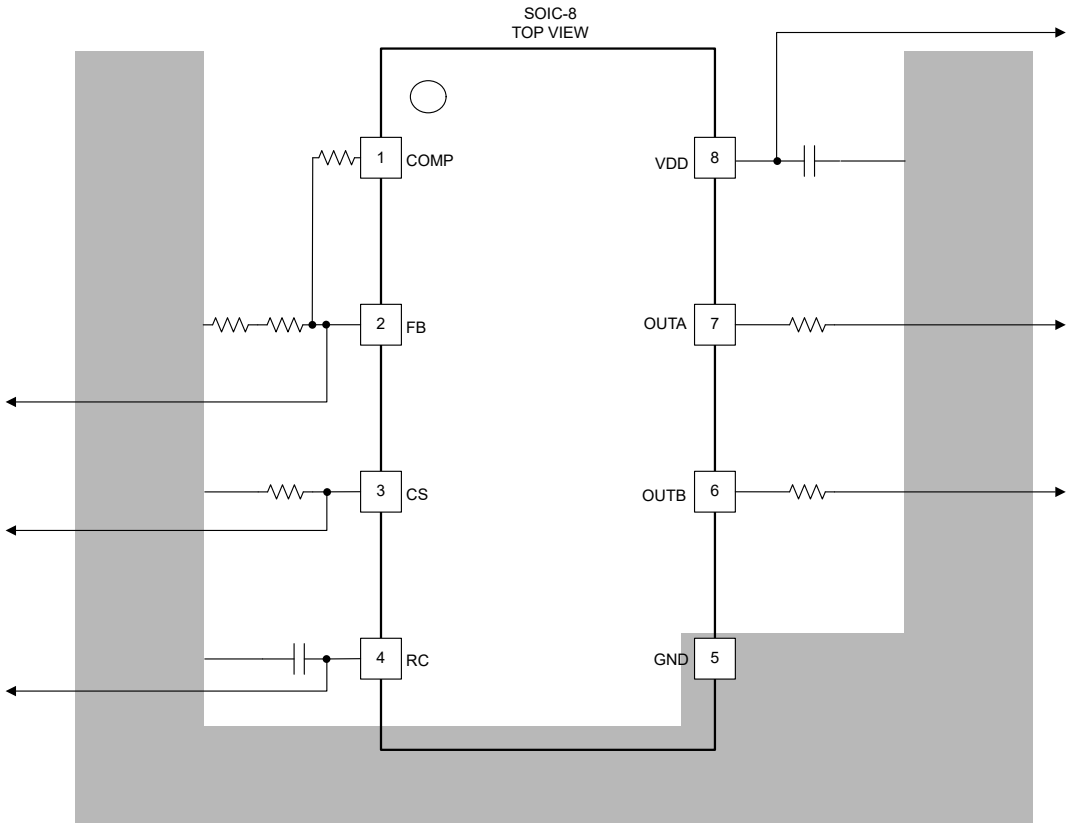


Figure 8-4. Recommended Layout

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Power Supply Control Products* data book
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application note

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (April 2013) to Revision C (August 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated the *Features* section	1
• Added the *Applications* section	1
• Deleted *Ordering Information* from the *Description*	1
• Updated *Simplified Typical Application* diagram	1
• Changed from: *Ordering Information Table* to: *Device Comparison Table*	3
• Added the *Pin Configuration and Functions* section	4
• Added the *Absolute Maximum Ratings* table	6
• Added the *ESD Ratings* section	6
• Added the *Recommended Operating Conditions* section	6
• Added the *Thermal Information* section	6
• Updated the *Electrical Characteristics* table	7

- Added the *Detailed Description* section
- Added the *Overview* section
- Deleted *UDG-00097* text from *Functional Block Diagram*
- Moved *Functional Block Diagram* to *Detailed Description* section
- Moved *Block Diagram of Oscillator* to *Detailed Description* section
- Deleted *UDG-00095* text from *Block Diagram of Oscillator*
- Added the *Device Functional Modes* section
- Updated *Application Information* section
- Moved the *Application Information* to the *Application and Implementation* section
- Added the *Typical Application* section
- Deleted the *UDG-00096* text from the *Typical Application Diagram*
- Added the *Design Requirements* section
- Added the *Detailed Design Procedure* section
- Added the *Application Curves* section
- Added the *Power Supply Recommendations* section
- Added the *Layout* section

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC2808AQDR-1EP	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	Call TI | Nipdau	Level-1-260C-UNLIM	-40 to 125	UCC2808 A-1EP
UCC2808AQDR-1EP.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UCC2808 A-1EP
UCC2808AQDR-2EP	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	Call TI | Nipdau	Level-1-260C-UNLIM	-40 to 125	UCC2808 A-2EP
UCC2808AQDR-2EP.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UCC2808 A-2EP
V62/04642-01XE	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UCC2808 A-1EP
V62/04642-02XE	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UCC2808 A-2EP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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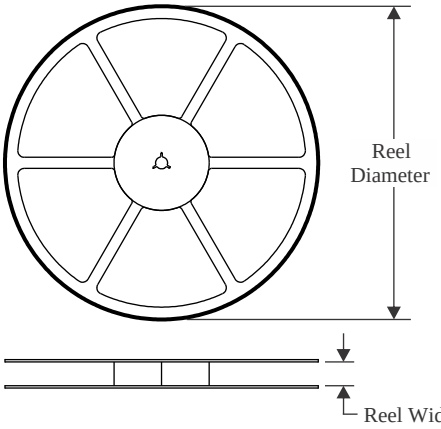
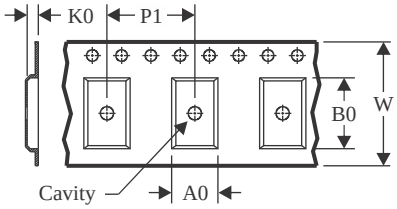
TAPE AND REEL INFORMATION

REEL DIMENSIONS

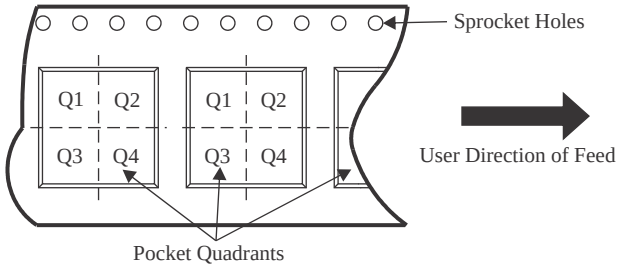


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

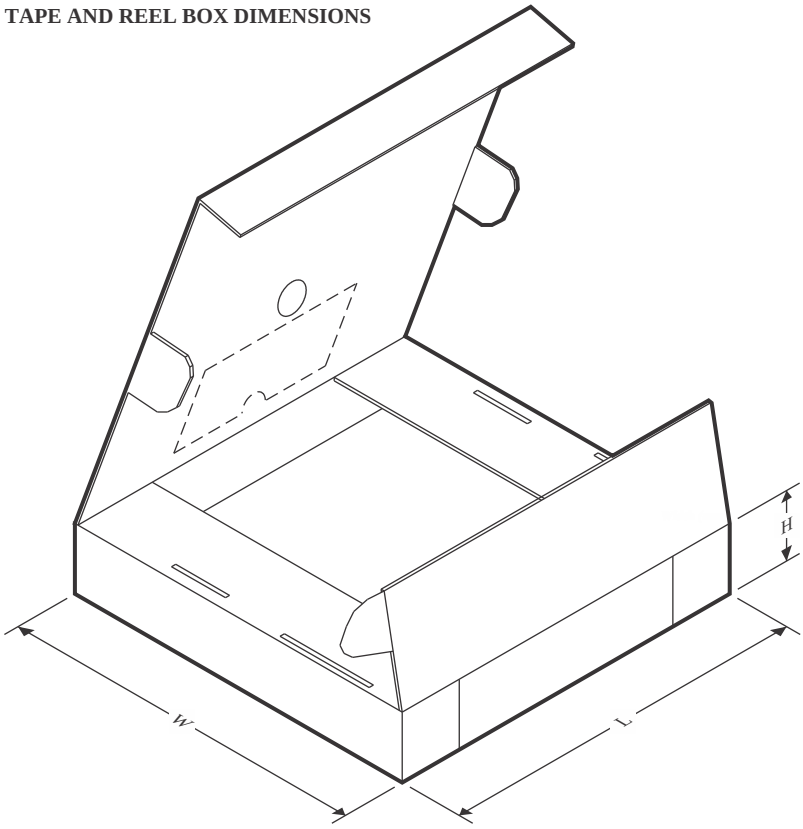
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC2808AQDR-1EP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC2808AQDR-2EP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC2808AQDR-1EP	SOIC	D	8	2500	353.0	353.0	32.0
UCC2808AQDR-2EP	SOIC	D	8	2500	353.0	353.0	32.0

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Last updated 10/2025