UCCx8C4x BiCMOS Low-Power Current-Mode PWM Controller

1 Features

- Enhanced replacement for UCx84x and UCx84xA family with pin-to-pin compatibility
- Operating frequency: 1MHz Maximum
- 50µA Startup Current, 100µA Maximum
- Low operating current: 2.3mA (at f_{OSC} = 52kHz)
- Fast, cycle-by-cycle overcurrent limiting: 35ns
- Peak driving current: ±1A. Rail-to-rail output:
  - 25ns rise time
  - 20ns fall time
- ±1% accurate 2.5V error amplifier reference
- Trimmed oscillator discharge current
- Undervoltage lockout protections
- VSSOP-8 package minimizes board space

2 Applications

- Switch-mode power supplies
- General purpose single-ended DC-DC or off-line isolated power converters
- Board mount power modules

3 Description

The UCCx8C4x family are high-performance, current-mode PWM controllers. The UCCx8C4x is an enhanced BiCMOS version with pin-for-pin compatibility to the industry standard UCx84xA family and UCx84x family of PWM controllers. The BiCMOS technology offers lower power consumption to improve efficiency as well as faster current sense and oscillator frequency.

In addition, lower startup voltage versions of 7V are offered as UCCx8C40 and UCCx8C41 for use in battery systems. The UCC28C4x series is specified for operation from –40°C to 125°C, and the UCC38C4x series is specified for operation from 0°C to 85°C.

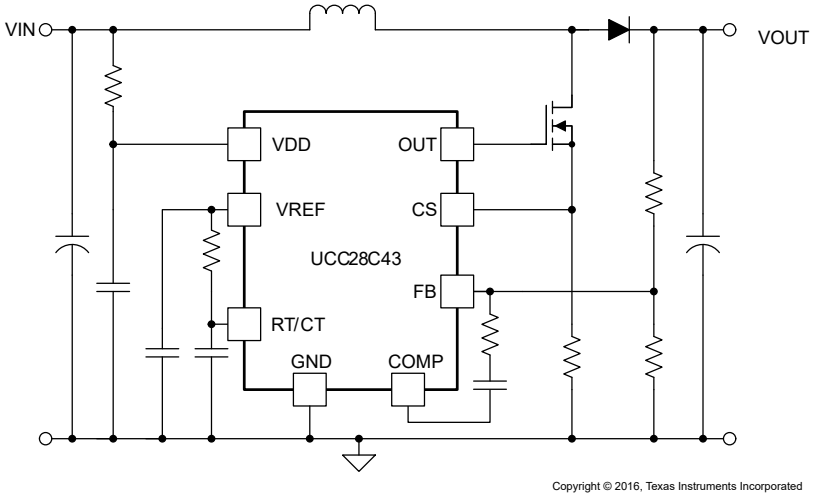
Providing necessary features to control fixed frequency, peak current-mode power supplies, this family offers the following performance advantages. The device offers high-frequency operation up to 1MHz, suitable for high speed applications. The trimmed discharge current enables more precise programming of the maximum duty cycle and dead-time limit when compared to the UCCx8C4x family. Reduced start-up and operating currents minimizes start-up loss and low operating power consumption for improved efficiency. The device also features a fast current-sense-to-output delay time of 35ns for superior overload protection at the power switch, and a ±1A peak output current capability with improved rise and fall times for driving large external MOSFETs directly.

The UCCx8C4x family is offered in 8-pin VSSOP (DGK) and 8-pin SOIC (D) packages.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
UCC28C4x UCC38C4x	SOIC (8)	3.91mm × 4.90mm
	VSSOP (8)	3.00mm × 3.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



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Simplified Application

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4 Device Comparison Table

UVLO			Junction Temperature (T_J) (°C)	Maximum duty cycle
Turn on at 14.5V Turn off at 9V for off-line applications	Turn on at 8.4V Turn off at 7.6V for dc/dc applications	Turn on at 7V Turn off at 6.6V for battery applications		
UCC28C42	UCC28C43	UCC28C40	–40 to 125	100%
UCC38C42	UCC38C43	UCC38C40	0 to 85	
UCC28C44	UCC28C45	UCC28C41	–40 to 125	50%
UCC38C44	UCC38C45	UCC38C41	0 to 85	

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5 Pin Configuration and Functions

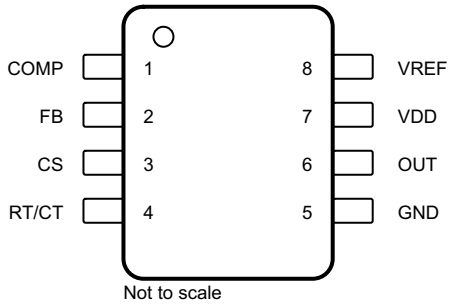


Figure 5-1. D Package 8-Pin SOIC (Top View)

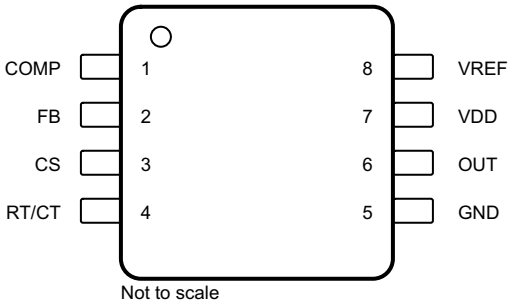


Figure 5-2. DGK Package, 8-Pin VSSOP (Top View)

Table 5-1. Pin Functions

PIN		TYPE (1)	DESCRIPTION
NAME	NO.		
COMP	1	O	This pin provides the output of the error amplifier for compensation. In addition, the COMP pin is frequently used as a control port, by utilizing a secondary-side error amplifier to send an error signal across the secondary-primary isolation boundary through an opto-isolator. The error amplifier is internally current limited so the user can command zero duty cycle by externally forcing COMP to GND.
CS	3	I	Primary-side current sense pin. The current sense pin is the noninverting input to the PWM comparator. Connect to current sensing resistor. This signal is compared to a signal proportional to the error amplifier output voltage. The PWM uses this to terminate the OUT switch conduction. A voltage ramp can be applied to this pin to run the device with a voltage mode control configuration.
FB	2	I	This pin is the inverting input to the error amplifier. FB is used to control the power converter voltage-feedback loop for stability. The noninverting input to the error amplifier is internally trimmed to 2.5V ± 1%.
GND	5	—	Ground return pin for the output driver stage and the logic level controller section.
OUT	6	O	The output of the on-chip drive stage. OUT is intended to directly drive a MOSFET. The OUT pin in the UCCx8C40, UCCx8C42, and UCCx8C43 is the same frequency as the oscillator, and can operate near 100% duty cycle. In the UCCx8C41, UCCx8C44, and UCCx8C45, the frequency of OUT is one-half that of the oscillator due to an internal T flipflop. This limits the maximum duty cycle to < 50%. Peak currents of up to 1A are sourced and sunk by this pin. OUT is actively held low when VDD is below the turn-on threshold.
RT/CT	4	I/O	Fixed frequency oscillator set point. Connect timing resistor (R_{RT}) to VREF and timing capacitor (C_{CT}) to GND from this pin to set the switching frequency. For best performance, keep the timing capacitor lead to the device GND as short and direct as possible. If possible, use separate ground traces for the timing capacitor and all other functions. The switching frequency (f_{SW}) of the UCCx8C40, UCCx8C42, and UCCx8C43 gate drive is equal to f_{OSC}; the switching frequency of the UCCx8C41, UCCx8C44, and UCCx8C45 is equal to half of the f_{OSC}.
VDD	7	I	Analog controller bias input that provides power to the device. Total VDD current is the sum of the quiescent VDD current and the average OUT current. A bypass capacitor, typically 0.1µF, connected directly to GND with minimal trace length, is required on this pin. Additional capacitance at least 10 times greater than the gate capacitance of the main switching FET used in the design is also required on VDD.
VREF	8	O	5V reference voltage. VREF is used to provide charging current to the oscillator timing capacitor through the timing resistor. It is important for reference stability that VREF is bypassed to GND with a ceramic capacitor connected as close to the pin as possible. A minimum value of 0.1µF ceramic is required. Additional VREF bypassing is required for external loads on VREF.

(1) I = input, O = output, G = ground

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1) (2)

		MIN	MAX	UNIT
Input voltage	VDD		20	V
Input current	IVDD		30	mA
Output drive current (peak)			±1	A
Output energy (capacitive load), E_{OUT}			5	µJ
Analog input voltage	COMP, CS, FB, RT/CT	–0.3	6.3	V
Output driver voltage	OUT	–0.3	20	
Reference voltage	VREF		7	
Error amplifier output sink current	COMP		10	mA
Total power dissipation at T_A = 25°C	D package		72.3	°C/W
	DGK package		98.1	
Lead temperature (soldering, 10 s), T_{LEAD}			300	°C
Operating junction temperature, T_J		–55	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Section 6.3*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND pin. Currents are positive into and negative out of the specified terminals.

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6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{VDD}	Input voltage			18	V
V_{OUT}	Output driver voltage			18	V
V_{REF}	Maximum continuous voltage from external circuitry			5.5	V
I_{OUT}	Average output driver current (source and sink) [1]			200	mA
$I_{OUT(VREF)}$	Reference output current (source) [1]			20	mA
T_J	Operating junction temperature[1]	UCC28C4x	–40	125	°C
		UCC38C4x	0	85	

(1) TI recommends against operating the device under conditions beyond those specified in this table for extended periods of time.

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6.4 Thermal Information

THERMAL METRIC[1]		UCC28C4x, UCC38C4x		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	128.9	176.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	71.7	67.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	72.3	98.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	23.4	11.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	71.5	91.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

V_{VDD} = 15V [1], R_{RT} = 10kΩ, C_{CT} = 3.3nF, C_{VDD} = 0.1µF and no load on the outputs, T_J = –40°C to 125°C for the UCC28C4x and T_J = 0°C to 85°C for the UCC38C4x (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE						
V_{VREF}	VREF voltage, initial accuracy	T_J = 25°C, I_{OUT} = 1mA	4.9	5	5.1	V
	Line regulation	V_{VDD} = 12V to 18V		0.2	20	mV
	Load regulation	1mA to 20mA		3	25	mV
	Temperature stability	See [2]		0.2	0.4	mV/°C
	Total output variation	See [2]	4.82		5.18	V
	VREF noise voltage	10Hz to 10kHz, T_J = 25°C, see [2]		50		µV
	Long term stability	1000 hours, T_J = 125°C, see [2]		5	25	mV
I_{VREF}	Output short circuit (source current)		30	45	55	mA
OSCILLATOR						
f_{OSC}	Initial accuracy	T_J = 25°C, see [3]	50.5	53	55	kHz
	Voltage stability	12V ≤ V_{VDD} ≤18V		0.2%	1%	
	Temperature stability	$T_{J(MIN)}$ to $T_{J(MAX)}$, see [2]		1%	2.5%	
	Amplitude	RT/CT pin peak-to-peak voltage		1.9		V
	Discharge current	T_J = 25°C, $V_{RT/CT}$ = 2V, see [4]	7.7	8.4	9	mA
		$V_{RT/CT}$ = 2V, see [4]	7.2	8.4	9.5	
ERROR AMPLIFIER						
V_{FB}	Feedback input voltage, initial accuracy	V_{COMP} = 2.5V, T_J = 25°C	2.475	2.5	2.525	V
	Feedback input voltage, total variation	V_{COMP} = 2.5V	2.45	2.5	2.55	V
I_{FB}	Input bias current (source current)	V_{FB} = 5V		0.1	2	µA
A_{VOL}	Open-loop voltage gain	2V ≤ V_{OUT} ≤ 4V	65	90		dB
	Unity gain bandwidth	See [2]	1	1.5		MHz
PSRR	Power supply rejection ratio	12V ≤ V_{VDD} ≤ 18V	60			dB
	Output sink current	V_{FB} = 2.7V, V_{COMP} = 1.1V	2	14		mA
	Output source current	V_{FB} = 2.3V, V_{COMP} = 5V	0.5	1		mA
	Output source current[2]	V_{FB} ≤ 2.3V, V_{COMP} = 0V			5.5	mA
VOH	High-level COMP voltage	V_{FB} = 2.3V, R_{COMP} = 15kΩ COMP to GND	V_{REF} - 0.2			V
VOL	Low-level COMP voltage	V_{FB} = 2.7V, R_{COMP} = 15kΩ COMP to VREF		0.1	1.1	V

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V_{VDD} = 15V (1), R_{RT} = 10kΩ, C_{CT} = 3.3nF, C_{VDD} = 0.1µF and no load on the outputs, T_J = –40°C to 125°C for the UCC28C4x and T_J = 0°C to 85°C for the UCC38C4x (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT SENSE						
A_{CS}	Gain	See (5) (6)	2.85	3	3.15	V/V
V_{CS}	Maximum input signal	V_{FB} < 2.4V	0.9	1	1.1	V
PSRR	Power supply rejection ratio	V_{VDD} = 12V to 18V(2) (5)		70		dB
I_{CS}	Input bias current (source current)			0.1	2	µA
t_D	CS to output delay			35	70	ns
	COMP to CS offset	V_{CS} = 0V		1.15		V
OUTPUT						
$V_{OUT(low)}$	$R_{DS(on)}$ pulldown	I_{SINK} = 200mA		5.5	15	Ω
$V_{OUT(high)}$	$R_{DS(on)}$ pullup	I_{SOURCE} = 200mA		10	25	Ω
t_{RISE}	Rise tIme	T_J = 25°C, C_{OUT} = 1nF		25	50	ns
t_{FALL}	Fall tIme	T_J = 25°C, C_{OUT} = 1nF		20	40	ns
UNDERVOLTAGE LOCKOUT						
VDD_{ON}	Start threshold	UCCx8C42, UCCx8C44	13.5	14.5	15.5	V
		UCCx8C43, UCCx8C45	7.8	8.4	9	
		UCCx8C40, UCCx8C41	6.5	7	7.5	
VDD_{OFF}	Minimum operating voltage	UCCx8C42, UCCx8C44	8	9	10	V
		UCCx8C43, UCCx8C45	7	7.6	8.2	
		UCCx8C40, UCCx8C41	6.1	6.6	7.1	
PWM						
D_{MAX}	Maximum duty cycle	UCCx8C42, UCCx8C43, UCCx8C40, V_{FB} < 2.4 V	94%	96%		
		UCCx8C44, UCCx8C45, UCCx8C41, V_{FB} < 2.4 V	47%	48%		
D_{MIN}	Minimum duty cycle	V_{FB} > 2.6V			0%	
CURRENT SUPPLY						
$I_{START-UP}$	Start-up current	V_{VDD} = VDD_{ON} – 0.5V		50	100	µA
I_{VDD}	Operating supply current	V_{FB} = V_{CS} = 0V		2.3	3	mA

(1) Adjust V_{VDD} above the start threshold before setting at and 15.5V.
(2) Specified by design. Not production tested.
(3) Output frequencies of the UCCx8C41, UCCx8C44, and the UCCx8C45 are half the oscillator frequency.
(4) Oscillator discharge current is measured with R_{RT} = 10kΩ to VREF.
(5) Parameter measured at trip point of latch with V_{FB} = 0V.
(6) Gain is defined as $A_{CS} = \Delta V_{COMP} / \Delta V_{CS}$, 0V ≤ V_{CS} ≤ 900mV

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6.6 Typical Characteristics

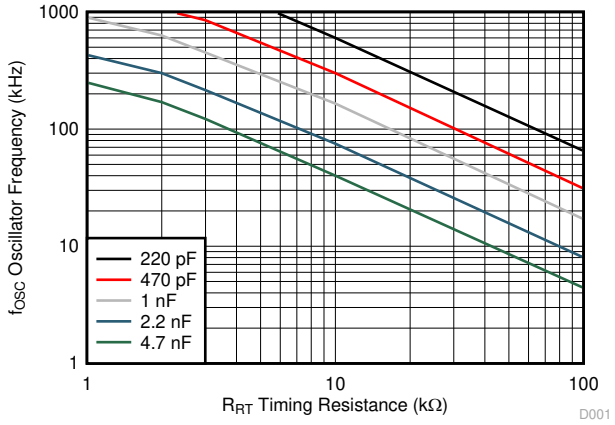


Figure 6-1. Oscillator Frequency vs Timing Resistance and Capacitance

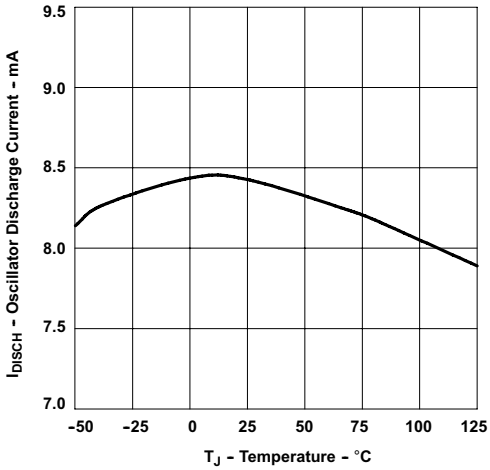


Figure 6-2. Oscillator Discharge Current vs Temperature

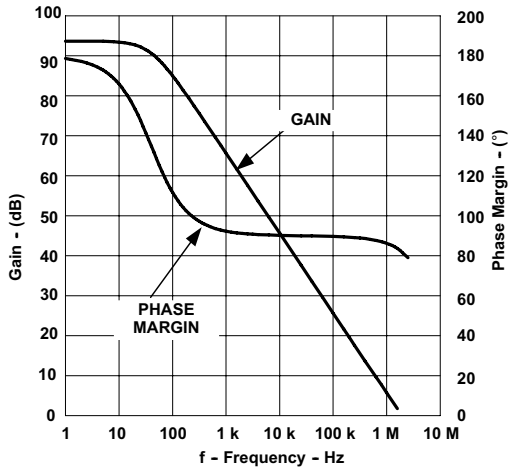
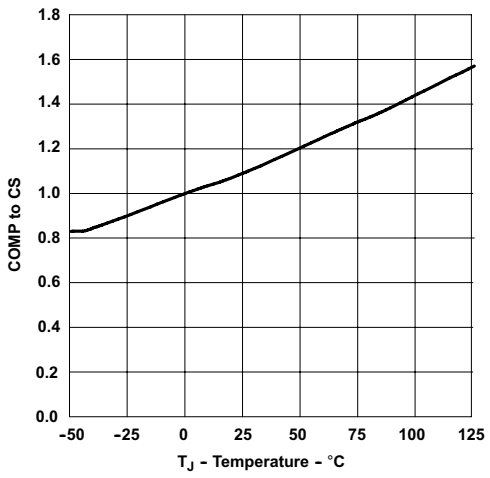


Figure 6-3. Error Amplifier Frequency Response



V_{CS} = 0V

Figure 6-4. COMP to CS Offset Voltage vs Temperature

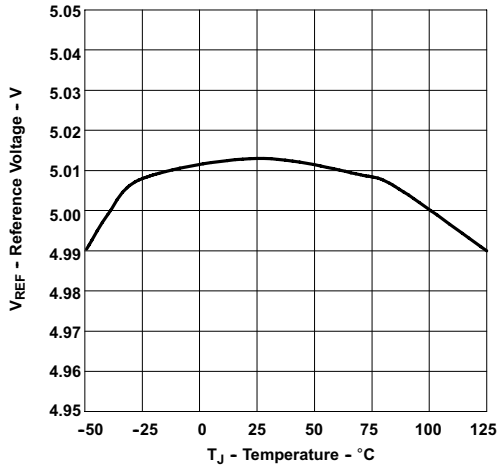


Figure 6-5. Reference Voltage vs Temperature

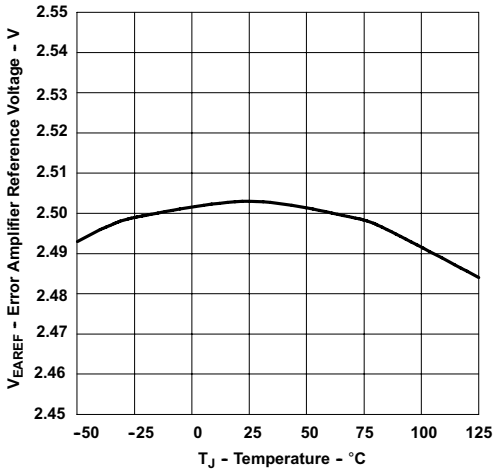


Figure 6-6. Error Amplifier Reference Voltage vs Temperature

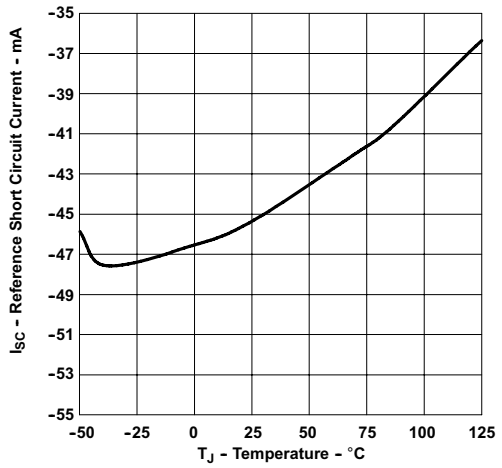


Figure 6-7. Reference Short-Circuit Current vs Temperature

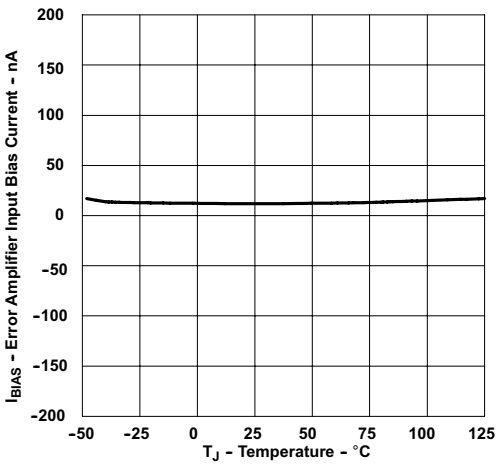
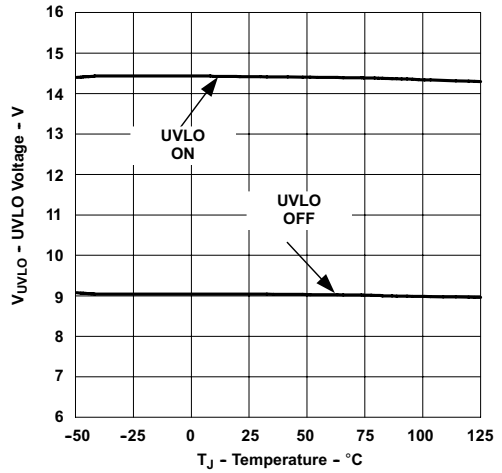
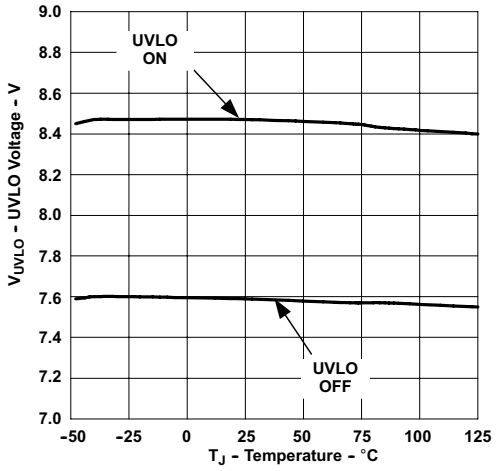


Figure 6-8. Error Amplifier Input Bias Current vs Temperature



UCCx8C42 and UCCx8C44

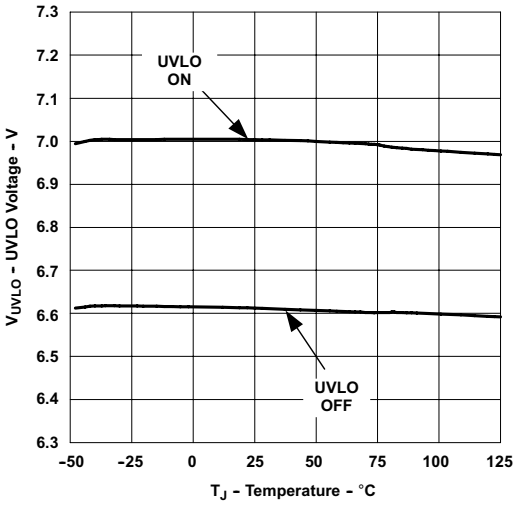
Figure 6-9. Undervoltage Lockout vs Temperature



UCCx8C43 and UCCx8C45

Figure 6-10. Undervoltage Lockout vs Temperature

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UCCx8C40 and UCCx8C41

Figure 6-11. Undervoltage Lockout vs Temperature

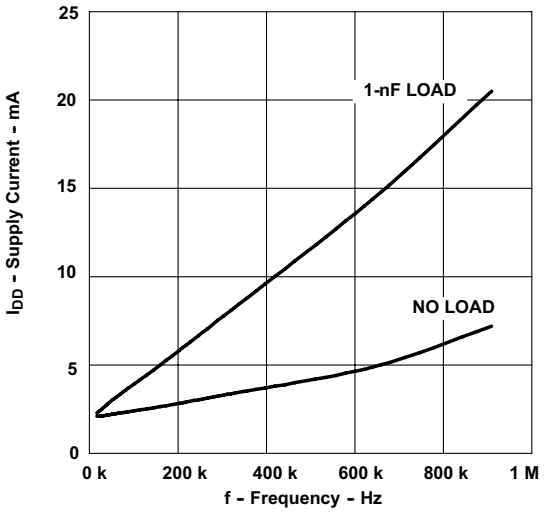


Figure 6-12. Supply Current vs Oscillator Frequency

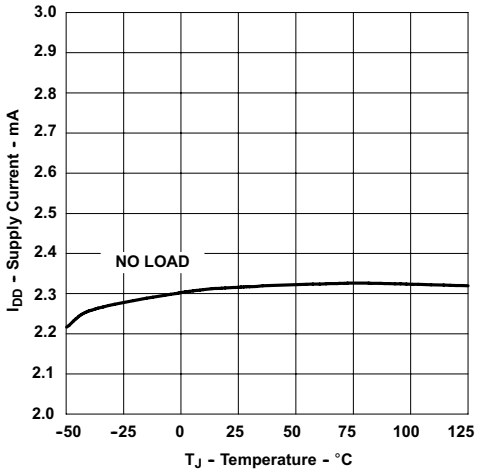


Figure 6-13. Supply Current vs Temperature

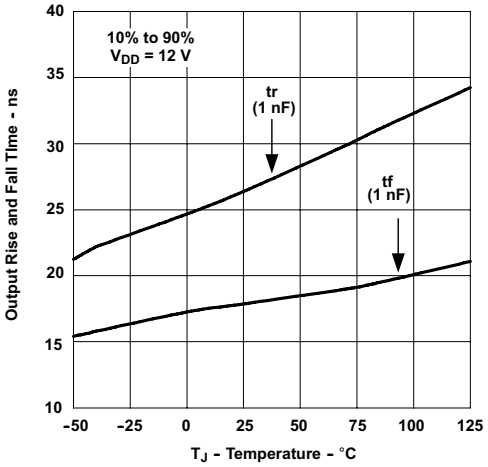


Figure 6-14. Output Rise Time and Fall Time vs Temperature

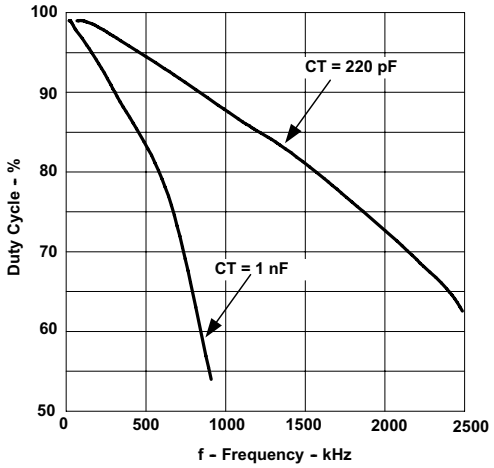


Figure 6-15. Maximum Duty Cycle vs Oscillator Frequency

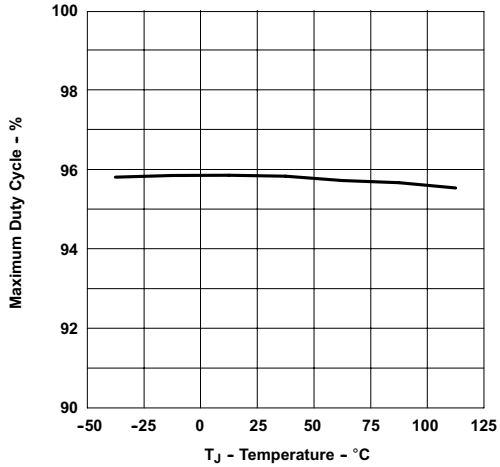


Figure 6-16. Maximum Duty Cycle vs Temperature (for part numbers with maximum 100% duty cycle)

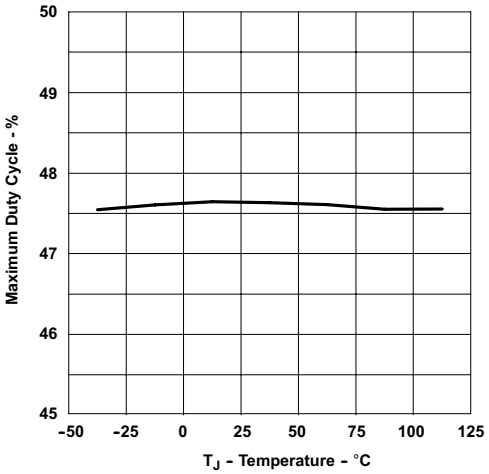


Figure 6-17. Maximum Duty Cycle vs Temperature (for part numbers with maximum 50% duty cycles)

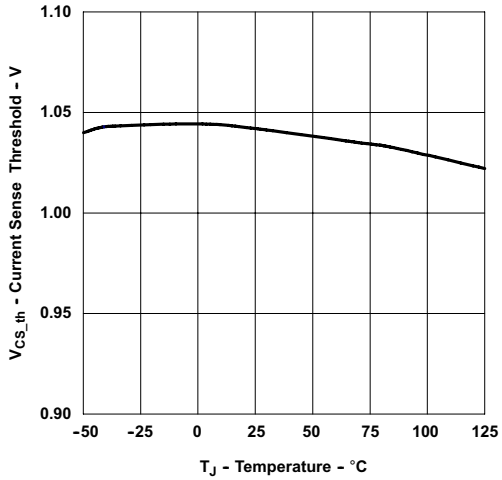


Figure 6-18. Current Sense Threshold Voltage vs Temperature

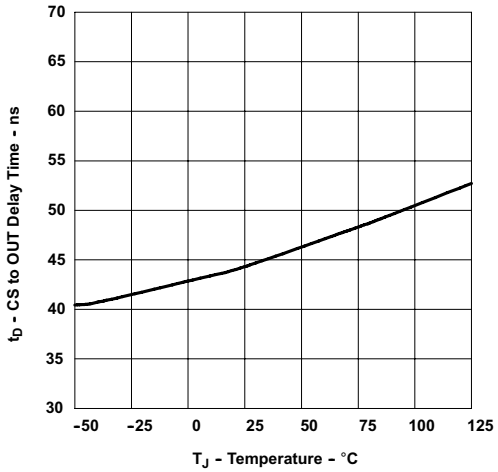


Figure 6-19. Current Sense to Output Delay Time vs Temperature

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7 Detailed Description

7.1 Overview

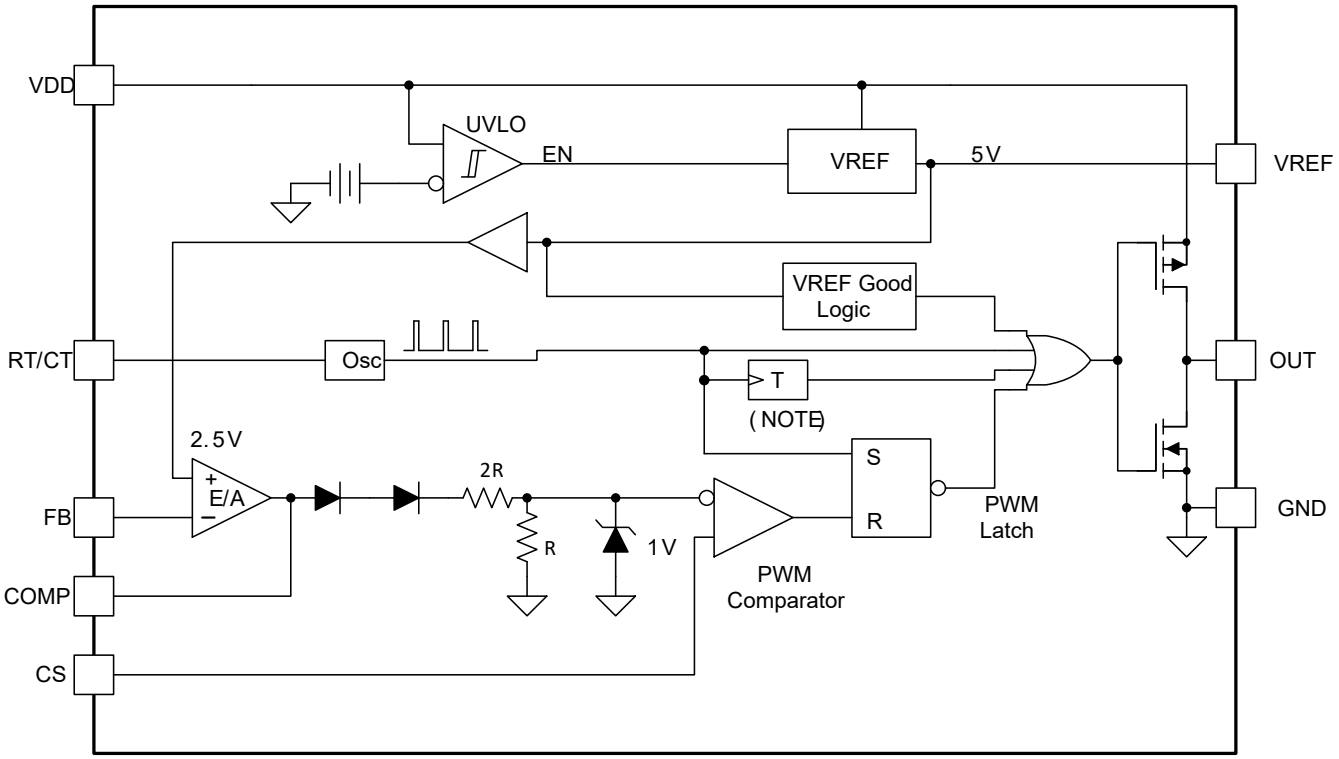
The UCCx8C4x series of control integrated circuits provide the features necessary to implement AC-DC or DC-to-DC fixed-frequency current-mode control schemes with a minimum number of external components. Protection circuitry includes undervoltage lockout (UVLO) and current limiting. Internally implemented circuits include a start-up current of less than 100µA, a precision reference trimmed for accuracy at the error amplifier input, logic to ensure latched operation, a pulse-width modulation (PWM) comparator that also provides currentlimit control, and an output stage designed to source or sink high-peak current. The output stage, suitable for driving N-channel MOSFETs, is low when it is in the OFF state. The oscillator contains a trimmed discharge current that enables accurate programming of the maximum duty cycle and dead time limit, making this device suitable for high-speed applications.

Major differences between members of this series are the UVLO thresholds, acceptable ambient temperature range, and maximum duty cycle. Typical UVLO thresholds of 14.5V (ON) and 9V (OFF) on the UCCx8C42 and UCCx8C44 devices make them ideally suited to off-line AC-DC applications. The corresponding typical thresholds for the UCCx8C43 and UCCx8C45 devices are 8.4V (ON) and 7.6V (OFF), making them ideal for use with regulated input voltages used in DC-DC applications. The UCCx8C40 and UCCx8C41 feature a start-up threshold of 7V and a turnoff threshold of 6.6V (OFF), which makes them suitable for battery-powered applications. The UCCx8C40, UCCx8C42, and UCCx8C43 devices operate to duty cycles approaching 100%. The UCCx8C41, UCCx8C44, and UCCx8C45 obtain a duty cycle from 0% to 50% by the addition of an internal toggle flip-flop, which blanks the output off every other clock cycle. The UCC28C4x series is specified for operation from –40°C to 125°C, and the UCC38C4x series is specified for operation from 0°C to 85°C.

The UCC28C4x and UCC38C4x series are an enhanced replacement with pin-to-pin compatibility to the bipolar UC284x, UC384x, UC284xA, and UC384xA families. The new series offers improved performance when compared to older bipolar devices and other competitive BiCMOS devices with similar functionality. These improvements generally consist of tighter specification limits that are a subset of the older product ratings, maintaining drop-in capability. In new designs, these improvements can reduce the component count or enhance circuit performance when compared to the previously available devices.

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7.2 Functional Block Diagram



Toggle flip-flop used only in UCCx8C41, UCCx8C44, and UCCx8C45

7.3 Feature Description

The BiCMOS design allows operation at high frequencies that were not feasible in the predecessor bipolar devices. First, the output stage has been redesigned to drive the external power switch in approximately half the time of the earlier devices. Second, the internal oscillator is more robust, with less variation as frequency increases. This faster oscillator makes this device suitable for high speed applications and the trimmed discharge current enables precise programming of the maximum duty cycle and dead-time limit. In addition, the current sense to output delay is kept the same 45ns (typical) . Such a delay time in the current sense results in superior overload protection at the power switch. The reduced start-up current of this device minimizes steady state power dissipation in the startup resistor, and the low operating current maximizes efficiency while running, increasing the total circuit efficiency, whether operating off-line, DC input, or battery operated circuits. These features combine to provide a device capable of reliable, high-frequency operation.

Table 7-1. Improved Key Parameters

PARAMETER	UCCx8C4x	UCx84x
Supply current at 50 kHz	2.3mA	11mA
Start-up current	50µA	1mA
Overcurrent propagation delay	50ns	150ns
Reference voltage accuracy	± 1%	± 2%
Error amplifier reference voltage accuracy	± 25mV	± 80mV
Maximum oscillator frequency	> 1MHz	500kHz
Output rise/fall times	25ns	50ns
UVLO turn-on accuracy	± 1V	± 1.5V
Smallest package option	VSSOP-8 (MSOP-8)	SOIC-8

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7.3.1 Detailed Pin Description

7.3.1.1 COMP

The error amplifier in the UCCx8C4x family has a unity-gain bandwidth of 1.5MHz. The COMP terminal can both source and sink current. The error amplifier is internally current-limited, so that one can command zero duty cycle by externally forcing COMP to GND.

7.3.1.2 FB

FB is the inverting input of the error amplifier. The noninverting input to the error amplifier is internally trimmed to 2.5V ± 1%. FB is used to control the power converter voltage-feedback loop for stability. For best stability, keep FB lead length as short as possible and FB stray capacitance as small as possible.

7.3.1.3 CS

The UCCx8C4x current sense input connects directly to the PWM comparator. Connect CS to the MOSFET source current sense resistor. The PWM uses this signal to terminate the OUT switch conduction. A voltage ramp can be applied to this pin to run the device with a voltage mode control configuration or to add slope compensation. To prevent false triggering due to leading edge noises, an RC current sense filter may be required. The gain of the current sense amplifier is typically 3 V/V.

7.3.1.4 RT/CT

The internal oscillator uses a timing capacitor (C_{CT}) and a timing resistor (R_{RT}) to program the oscillator frequency and maximum duty cycle. The operating frequency can be programmed based the curves in Oscillator Frequency vs Timing Resistance and Capacitance, where the timing resistor can be found once the timing capacitor is selected. It is best for the timing capacitor to have a flat temperature coefficient, typical of most COG or NPO type capacitors. For this converter, 15.4kΩ and 1000pF were selected for R_{RT} and C_{CT} to operate at 110kHz switching.

7.3.1.5 GND

GND is the signal and power returning ground. TI recommends separating the signal return path and the high current gate driver path so that the signal is not affected by the switching current.

7.3.1.6 OUT

The high-current output stage of the UCCx8C4x has been redesigned to drive the external power switch in approximately half the time of the earlier devices. To drive a power MOSFET directly, the totem-pole OUT driver sinks or source up to 1A peak of current. The OUT of the UCCx8C40, UCCx8C42, and UCCx8C43 devices switch at the same frequency as the oscillator and can operate near 100% duty cycle. In the UCCx8C41, UCCx8C44, and UCCx8C45, the switching frequency of OUT is one-half that of the oscillator due to an internal T flip-flop. This limits the maximum duty cycle in the UCCx8C41, UCCx8C44, and UCCx8C45 to < 50%.

The UCCx8C4x family houses unique totem pole drivers exhibiting a 10Ω impedance to the upper rail and a 5.5Ω impedance to ground, typically. This reduced impedance on the low-side switch helps minimize turnoff losses at the power MOSFET, whereas the higher turnon impedance of the high-side switch is intended to better match the reverse recovery characteristics of many high-speed output rectifiers. Transition times, rising and falling edges, are typically 25 nanoseconds and 20 nanoseconds, respectively, for a 10% to 90% change in voltage.

A low impedance MOS structure in parallel with a bipolar transistor, or BiCMOS construction, comprises the totem-pole output structure. This more efficient utilization of silicon delivers the high peak current required along with sharp transitions and full rail-to-rail voltage swings. Furthermore, the output stage is self-biasing, active low during undervoltage lockout type. With no VDD supply voltage present, the output actively pulls low if an attempt is made to pull the output high. This condition frequently occurs at initial power-up with a power MOSFET as the driver load.

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7.3.1.7 VDD

VDD is the power input connection for this device. In normal operation, power VDD through a current limiting resistor. The absolute maximum supply voltage is 20V, including any transients that may be present. If this voltage is exceeded, device damage is likely. This is in contrast to the predecessor bipolar devices, which could survive up to 30V on the input bias pin. Also, because no internal clamp is included in the device, the VDD pin must be protected from external sources which could exceed the 20V level. If containing the start-up and bootstrap supply voltage from the auxiliary winding NA below 20V under all line and load conditions can not be achieved, use a zener protection diode from VDD to GND. Depending on the impedance and arrangement of the bootstrap supply, this may require adding a resistor, R_{VDD}, in series with the auxiliary winding to limit the current into the zener as shown in Figure 7-1. Ensure that over all tolerances and temperatures, the minimum zener voltage is higher than the highest UVLO upper turnon threshold. To prevent noise related problems, filter VDD with a ceramic bypass capacitor to GND. The VDD pin must be decoupled as close to the GND pin as possible.

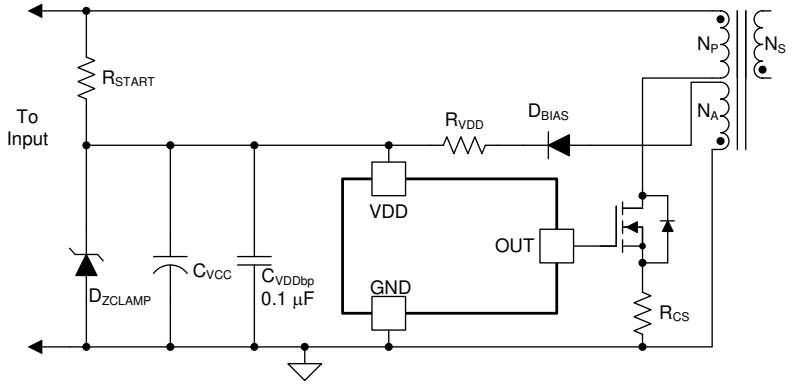


Figure 7-1. VDD Protection

Although nominal VDD operating current is only 2.3mA, the total supply current is higher, depending on the OUT current. Total VDD current is the sum of quiescent VDD current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Q_g), average OUT current can be calculated from Equation 1.

$$I_{OUT} = Q_g \times f_{SW} \quad (1)$$

7.3.1.8 VREF

VREF is the voltage reference for the error amplifier and also for many other internal circuits in the IC. The 5V reference tolerance is ±1% for the UCCx8C4x family. The high-speed switching logic uses VREF as the logic power supply. The reference voltage is divided down internally to 2.5V ±1% and connected to the error amplifier's noninverting input for accurate output voltage regulation. The reference voltage sets the internal bias currents and thresholds for functions such as the oscillator upper and lower thresholds along with the overcurrent limiting threshold. The output short-circuit current is 55mA (maximum). To avoid device over-heating and damage, do not pull VREF to ground as a means to terminate switching. For reference stability and to prevent noise problems with high-speed switching transients, bypass VREF to GND with a ceramic capacitor close to the IC package. A ceramic capacitor with a minimum value of 0.1µF is required. Additional VREF bypassing is required for external loads on the reference. An electrolytic capacitor may also be used in addition to the ceramic capacitor.

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7.3.2 Undervoltage Lockout

Six sets of UVLO thresholds are available with turn-on and turnoff thresholds of: (14.5V and 9V), (8.4V and 7.6V), (7V and 6.6V) respectively. The first set is primarily intended for off-line and 48V distributed power applications, where the wider hysteresis allows for lower frequency operation and longer soft-starting time of the converter. The second group of UVLO options is ideal for high frequency DC-DC converters typically running from a 12VDC input. The third, and newest, set has been added to address battery powered and portable applications. Table 7-2 shows the maximum duty cycle and UVLO thresholds by device.

Table 7-2. UVLO Options

MAXIMUM DUTY CYCLE (%)	UVLO ON (V)	UVLO OFF (V)	DEVICE NUMBER
100	14.5	9	UCCx8C42
100	8.4	7.6	UCCx8C43
100	7	6.6	UCCx8C40
50	14.5	9	UCCx8C44
50	8.4	7.6	UCCx8C45
50	7	6.6	UCCx8C41

During UVLO the IC draws less than 100µA of supply current. After crossing the turnon threshold, the device supply current increases to a maximum of 3mA, typically 2.3mA. This low start-up current allows the power supply designer to optimize the selection of the startup resistor value to provide a more efficient design. In applications where low component cost overrides maximum efficiency, the low run current of 2.3mA (typical) allows the control device to run directly through the single resistor to (+) rail, rather than requiring a bootstrap winding on the power transformer, along with a rectifier. The start and run resistor for this case must also pass enough current to allow driving the primary switching MOSFET, which may be a few milliamps in small devices.

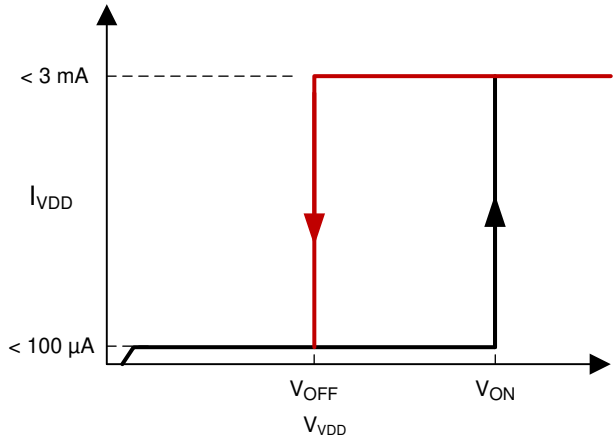


Figure 7-2. UVLO ON and OFF Profile

7.3.3 ±1% Internal Reference Voltage

The BiCMOS internal reference of 2.5V has an enhanced design, and uses production trim to allow initial accuracy of ±1% at room temperature and ±2% over the full temperature range. This reference voltage can be used to eliminate an external reference in applications that do not require the extreme accuracy afforded by the additional device. This reference voltage is useful for non-isolated DC-DC applications, where the control device is referenced to the same common as the output. It is also applicable in off-line designs that regulate on the primary side of the isolation boundary by looking at a primary bias winding, or from a winding on the output inductor of a buck-derived circuit.

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7.3.4 Current Sense and Overcurrent Limit

An external series resistor (R_{CS}) senses the current and converts this current into a voltage that becomes the input to the CS pin. The CS pin is the noninverting input to the PWM comparator. The device compares the CS input with a signal proportional to the error amplifier output voltage. The gain of the current sense amplifier is typically 3V/V. The peak I_{SENSE} current is determined using Equation 2

$$I_{SENSE} = \frac{V_{CS}}{R_{CS}} \tag{2}$$

The typical value for V_{CS} is 1V. A small RC filter (R_{CSF} and C_{CSF}) may be required to suppress switch transients caused by the reverse recovery of a secondary side diode or equivalent capacitive loading in addition to parasitic circuit impedances. The time constant of this filter should be considerably less than the switching period of the converter.

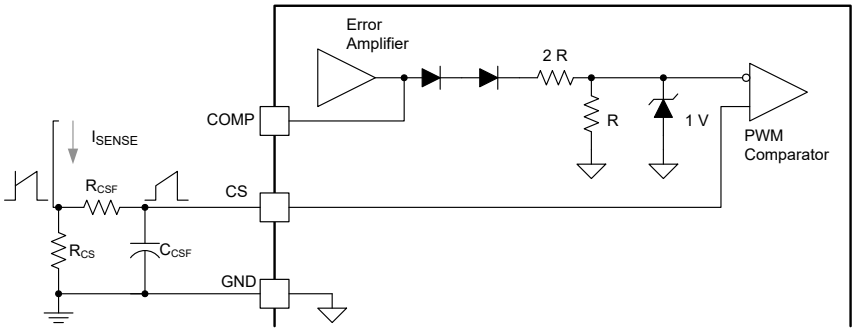


Figure 7-3. Current-Sense Circuit Schematic

Cycle-by-cycle pulse width modulation performed at the PWM comparator essentially compares the error amplifier output to the current sense input. This is not a direct volt-to-volt comparison, as the error amplifier output network incorporates two diodes in series with a resistive divider network before connecting to the PWM comparator. The two-diode drop adds an offset voltage that enables zero duty cycle to be achieved with a low amplifier output. The 2R/R resistive divider facilitates the use of a wider error amplifier output swing that can be more symmetrically centered on the 2.5V noninverting input voltage.

The 1V Zener diode associated with the PWM comparator input from the error amplifier is not an actual diode in the device design, but an indication that the maximum current sense input amplitude is 1V (typical). When this threshold is reached, regardless of the error amplifier output voltage, cycle-by-cycle current limiting occurs, and the output pulse width is terminated within 35ns (typical). The minimum value for this current limit threshold is 0.9V with a 1.1V maximum. In addition to the tolerance of this parameter, the accuracy of the current sense resistor, or current sense circuitry, must be taken into account. It is advised to factor in the worst case of primary and secondary currents when sizing the ratings and worst-case conditions in all power semiconductors and magnetic components.

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7.3.5 Reduced-Discharge Current Variation

The oscillator design for the UCCx8C4x controllers incorporates a trimmed discharge current to accurately program maximum duty cycle and operating frequency. In its basic operation, a timing capacitor (C_{CT}) is charged by a current source, formed by the timing resistor (R_{RT}) connected to the device reference voltage (VREF). The oscillator design incorporates comparators to monitor the amplitude of the timing capacitor voltage. The exponentially shaped waveform charges up to a specific amplitude representing the oscillator upper threshold of 3V. After the controller reaches this level, an internal current sink to ground turns on and the capacitor begins to discharge. This discharge continues until the oscillator lower threshold has reached 0.7 V at which point the current sink is turned off. Next, the timing capacitor starts charging again and a new switching cycle begins.

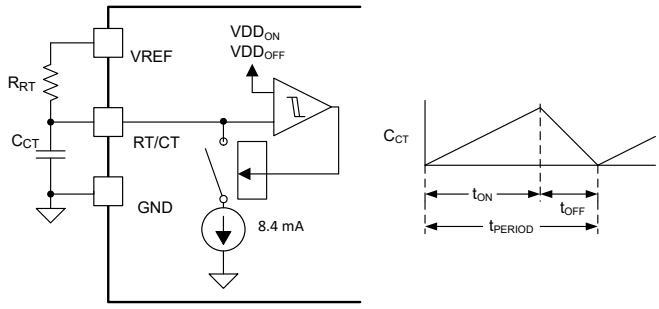
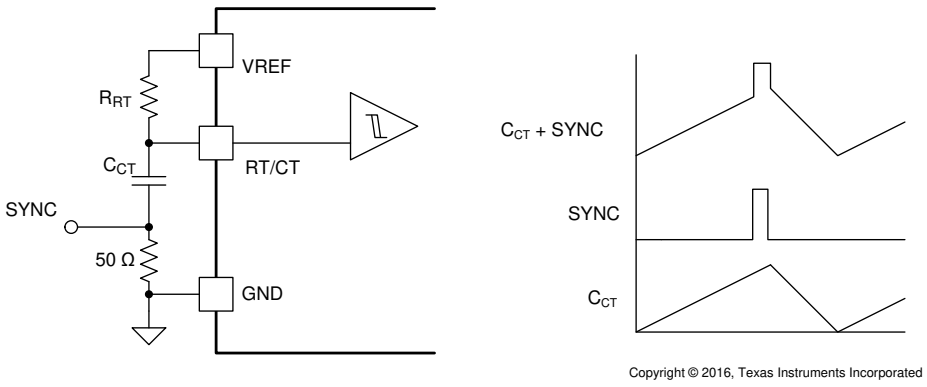


Figure 7-4. Oscillator Circuit

While the device discharges the timing capacitor, resistor R_{RT} continues attempting to charge C_{CT}. It is the exact ratio of these two currents, the discharging versus the charging current, which specifies the maximum duty cycle. During the discharge time of C_{CT}, the device output is always off. This represents an ensured minimum off time of the switch, commonly referred to as dead-time. To program an accurate maximum duty cycle, use the information provided in Maximum Duty Cycle vs Oscillator Frequency for maximum duty cycle versus oscillator frequency. Any number of maximum duty cycles can be programmed for a given frequency by adjusting the values of R_{RT} and C_{CT}. After selecting the value of R_{RT}, find the oscillator timing capacitance using the curves in Oscillator Frequency vs Timing Resistance and Capacitance. However, because resistors are available in more precise increments, typically 1%, and capacitors are only available in 5% accuracy, it might be more practical to select the closest capacitor value first and then calculate the timing resistor value.

7.3.6 Oscillator Synchronization

Synchronization is best achieved by forcing the timing capacitor voltage above the oscillator internal upper threshold. A small resistor is placed in series with C_{CT} to GND. This resistor serves as the input for the sync pulse which raises the C_{CT} voltage above the oscillator internal upper threshold. The PWM is allowed to run at the frequency set by R_{RT} and C_{CT} until the sync pulse appears. This scheme offers several advantages including having the local ramp available for slope compensation. The UCCx8C4x oscillator must be set to a lower frequency than the sync pulse stream, typically 20 percent with a 0.5V pulse applied across the resistor.



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Figure 7-5. Oscillator Synchronization Circuit

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7.3.7 Soft-Start Timing

The soft-start timing is the technique to gradually power up the converter in a well-controlled fashion by slowly increasing the effective duty cycle starting at zero and gradually rising. Following start-up of the PWM, the error amplifier inverting input is low, commanding the error amplifier's output to go high. The output stage of the amplifier can source 1mA typically, which is enough to drive most high impedance compensation networks, but not enough for driving large loads quickly. Soft-start timing is achieved by charging a fairly large value, >1µF, capacitor (C_{SS}) connected to the error amplifier output through a PNP transistor as shown in Figure 7-6

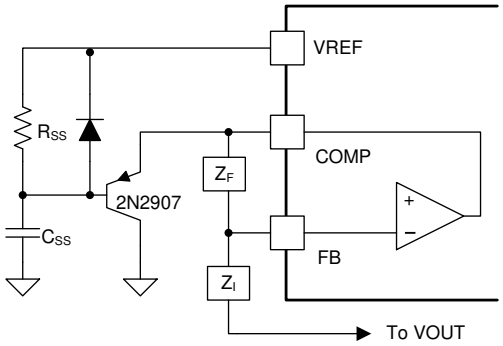


Figure 7-6. Soft-Start Implementation

The limited charging current of the amplifier into the capacitor translates into a dv/dt limitation on the error amplifier output. This directly corresponds to some maximum rate of change of primary current in a current mode controlled system as one of the PWM comparator inputs gradually rises. The values of R_{SS} and C_{SS} must be selected to bring the COMP pin up at a controlled rate, limiting the peak current supplied by the power stage. After the soft-start interval is complete, the capacitor continues to charge to VREF, effectively removing the PNP transistor from the circuit consideration. Soft-start timing offers a different, frequently preferred function in current mode controlled systems than it does in voltage mode control. In current mode, soft start controls the rising of the peak switch current. In voltage mode control, soft start gradually widens the duty cycle, regardless of the primary current or rate of ramp-up.

The purpose of resistor R_{SS} and the diode is to remove the soft-start capacitor from the error amplifier path during normal operation, after the soft-start period completes and the capacitor charges fully. The optional diode in parallel with the resistor forces a soft-start period each time the PWM goes through UVLO condition that forces VREF to go low. Without the diode, the capacitor remains charged during a brief loss of supply or brown-out, and the device does not emable a soft-start function upon re-application of VDD.

7.3.8 Enable and Disable

There are several ways to enable or disable the UCCx8C4x devices, depending on which type of restart is required. The two basic techniques use external transistors to either pull the error amplifier output low (< $2V_{BE}$) or pull the current sense input high (> 1.1V). Application of the disable signal causes the output of the PWM comparator to be high. The PWM latch is reset dominant so that the output remains low until the next clock cycle after the shutdown condition at the COMP or CS pin is removed. Another choice for restart without a soft-start period is to pull the current sense input above the cycle-by-cycle current limiting threshold. A logic level P-channel FET from the reference voltage to the current sense input can be used.

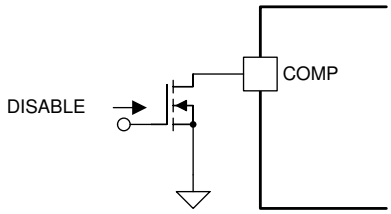


Figure 7-7. Disable Circuit

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7.3.9 Slope Compensation

With current mode control, slope compensation is required to stabilize the overall loop with duty cycles exceeding 50%. Although not required, slope compensation also improves stability in applications using below a 50% maximum duty cycle. Slope compensation is introduced by injecting a portion of the oscillator waveform to the actual sensed primary current. The two signals are summed together at the current sense input (CS) connection at the filter capacitor. To minimize loading on the oscillator, it is best to buffer the timing capacitor waveform with a small transistor whose collector is connected to the reference voltage.

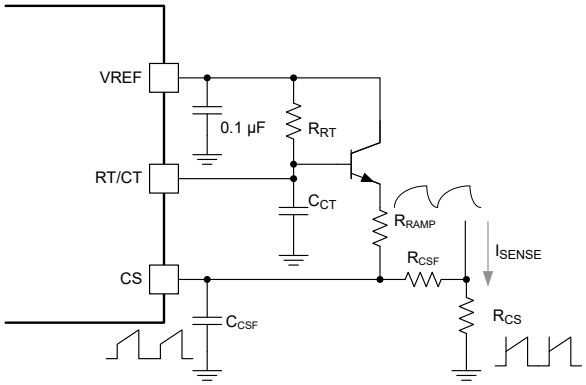


Figure 7-8. Slope Compensation Circuit

7.3.10 Voltage Mode

In certain applications, voltage mode control may be a preferred control strategy for a variety of reasons. Voltage mode control is easily executable with any current mode controller, especially the UCCx8C4x family members. Implementation requires generating a 0V to 0.9V sawtooth shaped signal to input to the current sense pin (CS) which is also one input to the PWM comparator. This is compared to the divided down error amplifier output voltage at the other input of the PWM comparator. As the error amplifier output is varied, it intersects the sawtooth waveform at different points in time, thereby generating different pulse widths. This is a straightforward method of linearly generating a pulse whose width is proportional to the error voltage.

Implementation of voltage mode control is possible by using a fraction of the oscillator timing capacitor (C_{CT}) waveform. This value can be divided down and fed to the current sense pin as shown in Figure 7-9. The oscillator timing components must be selected to approximate as close to a linear sawtooth waveform as possible. Although exponentially charged, large values of timing resistance and small values of timing capacitance help approximate a more linear shaped waveform. A small transistor is used to buffer the oscillator timing components from the loading of the resistive divider network. Due to the offset of the oscillator's lower timing threshold, a DC blocking capacitor is added.

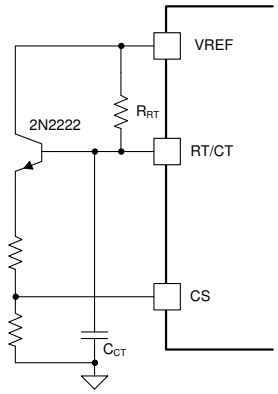


Figure 7-9. Current Mode PWM Used as a Voltage Mode PWM

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7.4 Device Functional Modes

7.4.1 Normal Operation

During normal operating mode, the controller can be used in peak current mode or voltage mode control. When the converter is operating in peak current mode, the controller regulates the converter's peak current and duty cycle. When used in voltage mode control, the controller regulates the power converter's duty cycle. The regulation of the system's peak current and duty cycle can be achieved with the use of the integrated error amplifier and external feedback circuitry.

7.4.2 UVLO Mode

During the system start-up, VDD voltage starts to rise from 0 V. Before the VDD voltage reaches its corresponding turn-on threshold, the IC is operating in UVLO mode. During UVLO mode operation, the VREF pin voltage is not generated. When VDD is above 1V and below the turn-on threshold, the VREF pin is actively pulled low. This behavior allows VREF to be used as a logic signal to indicate UVLO mode. If the bias voltage to VDD drops below the UVLO-OFF threshold, the PWM switching stops and VREF returns to 0V. The device can be restarted by applying a voltage greater than the UVLO-ON threshold to the VDD pin.

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The UCCx8C4x controllers are peak current mode pulse width modulators. These controllers have an onboard amplifier and can be used in isolated and nonisolated power supply designs. The onboard totem pole gate driver is capable of delivering 1A of peak current. This high-speed PWM is capable of operating at switching frequencies up to 1MHz. . Figure 8-1 shows a typical off-line application using UCC38C44.

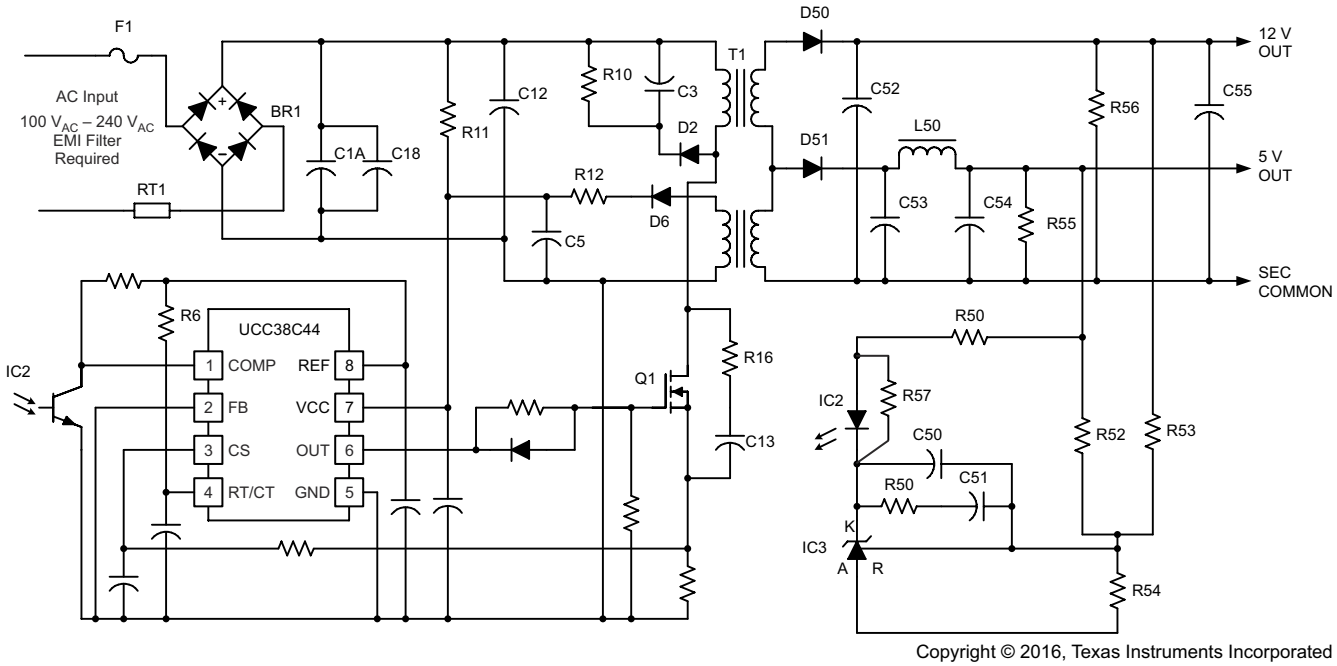


Figure 8-1. Typical Off-Line Application

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Figure 8-2 shows a forward converter with synchronous rectification. This application provides 48V to 3.3V at 10A with over 85% efficiency, and uses the UCC38C42 as the secondary-side controller and UCC3961 as the primary-side startup control device.

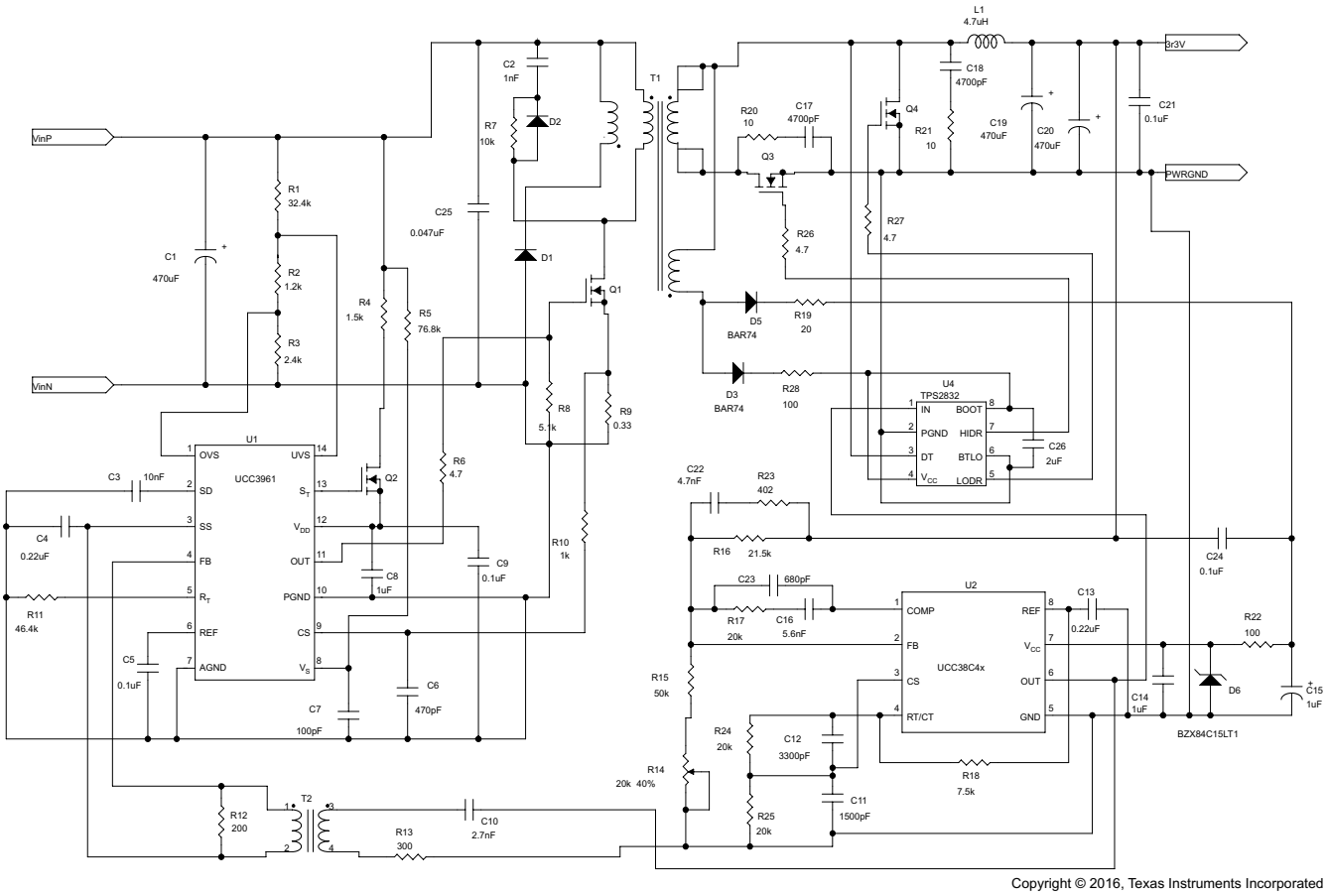
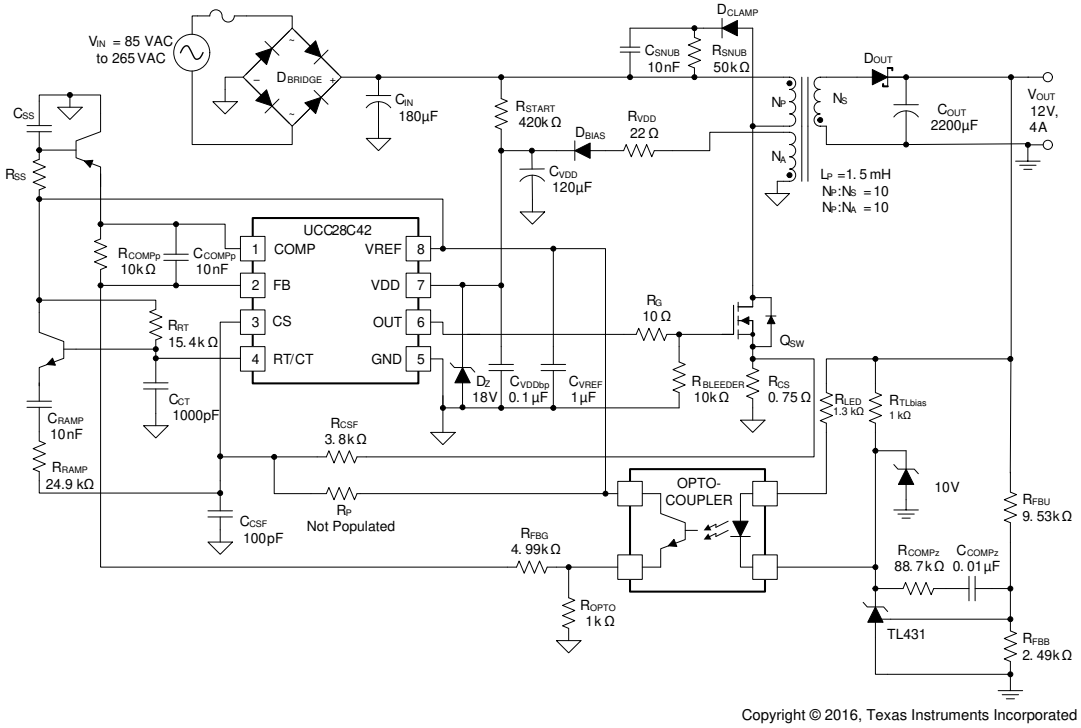


Figure 8-2. Forward Converter with Synchronous Rectification Using the UCC38C42 as the Secondary-Side Controller

8.2 Typical Application

A typical application for the UCC28C42 controller in an off-line flyback converter is shown in Figure 8-3. The controller uses an inner current control loop that contains a small current sense resistor which senses the primary inductor current ramp. This current sense resistor transforms the inductor current waveform to a voltage signal that is input directly into the primary side PWM comparator. This inner loop determines the response to input voltage changes. An outer voltage control loop involves comparing a portion of the output voltage to a reference voltage at the input of an error amplifier. When used in an off-line isolated application, the voltage feedback of the isolated output is accomplished using a secondary-side error amplifier and adjustable voltage reference, such as the TL431. The error signal crosses the primary to secondary isolation boundary using an opto-isolator whose collector is connected to the VREF pin and the emitter is connected to FB. The outer voltage control loop determines the response to load changes.



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Figure 8-3. Typical Application Design Schematic

8.2.1 Design Requirements

Table 8-1 shows a typical set of performance requirements for an off-line flyback converter capable of providing 48W at 12V output voltage from a universal AC input. The design uses peak primary current control in a continuous current mode PWM converter.

Table 8-1. Design Parameters

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{IN}	Input Voltage		85	115/230	265	V_{RMS}
f_{LINE}	Line Frequency		47	50/60	63	Hz
V_{OUT}	Output Voltage	$I_{VOUT(min)} \le I_{VOUT} \le I_{VOUT(max)}$	11.75	12	12.25	V
V_{RIPPLE}	Output Ripple Voltage	$I_{VOUT(min)} \le I_{VOUT} \le I_{VOUT(max)}$			100	mVpp
I_{VOUT}	Output Current		0	4		A
f_{SW}	Switching Frequency			110		kHz
η	Efficiency			85%		

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8.2.2 Detailed Design Procedure

This procedure outlines the steps to design an off-line universal input continuous current mode (CCM) flyback converter. See Figure 8-3 for component names referred to in the design procedure.

8.2.2.1 Input Bulk Capacitor and Minimum Bulk Voltage

Bulk capacitance may consist of one or more capacitors connected in parallel, often with some inductance between them to suppress differential-mode conducted noise. The value of the input capacitor sets the minimum bulk voltage;. Setting the bulk voltage lower by using minimal input capacitance results in higher peak primary currents leading to more stress on the MOSFET switch, the transformer, and the output capacitors. Setting the bulk voltage higher by using a larger input capacitor results in higher peak current from the input source and the capacitor itself is physically larger. Compromising between size and component stresses determines the acceptable minimum input voltage. The total required value for the primary-side bulk capacitance (C_{IN}) is selected based upon the power level of the converter (P_{OUT}), the efficiency target (η), the minimum input voltage ($V_{IN(min)}$), and is chosen to maintain an acceptable minimum bulk voltage level ($V_{BULK(min)}$), using Equation 3.

$$C_{IN} = \frac{2 \times P_{IN} \times \left(0.25 + \frac{1}{\pi} \times \arcsin\left(\frac{V_{BULK\,(min)}}{\sqrt{2} \times V_{IN\,(min)}}\right)\right)}{\left(2 \times V_{IN\,(min)}^2 - V_{BULK\,(min)}^2\right) \times f_{LINE\,(min)}} \quad (3)$$

where

- $V_{IN(min)}$ is the RMS value of the minimum AC input voltage (85VRMS) whose minimum line frequency is denoted as $f_{LINE(min)}$, equal to 47Hz

Based on Equation 3, to achieve a minimum bulk voltage of 75V, assuming 85% converter efficiency, the bulk capacitor must be larger than 126µF. this design uses a value of 180µF, with consideration for component tolerances and efficiency estimation.

8.2.2.2 Transformer Turns Ratio and Maximum Duty Cycle

The transformer design begins with selecting a suitable switching frequency for the given application. The UCC28C42 is capable of switching up to 1MHz but considerations such as overall converter size, switching losses, core loss, system compatibility, and interference with communication frequency bands generally determine an optimum frequency that should be used. For this off-line converter, the switching frequency (f_{SW}) is selected to be 110kHz as a compromise to minimize the transformer size and the EMI filter size, and still have acceptable losses.

The transformer primary to secondary turns ratio (N_{PS}) can be selected based on the desired MOSFET voltage rating and the secondary diode voltage rating. Because the maximum input voltage is 265VRMS, the peak bulk input voltage can be calculated as shown in Equation 4.

$$V_{BULK\,(max)} = \sqrt{2} \times V_{IN\,(max)} \approx 375\ V \quad (4)$$

To minimize the cost of the system, a readily available 650V MOSFET is selected. Derating the maximum voltage stress on the drain to 80% of its rated value and allowing for a leakage inductance voltage spike of up to 30% of the maximum bulk input voltage, the reflected output voltage must be less than 130V as shown in Equation 5.

$$V_{REFLECTED} = 0.8 \times \left(V_{DS(rated)} - 1.3 \times V_{BULK(max)}\right) = 130.2\ V \quad (5)$$

The maximum primary to secondary transformer turns ratio (N_{PS}) for a 12V output can be selected as

$$N_{PS} = \frac{V_{REFLECTED}}{V_{OUT}} = 10.85 \quad (6)$$

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A turns ratio of N_{PS} = 10 is used in the design example.

The auxiliary winding is used to supply bias voltage to the controller. Maintaining the bias voltage above the VDD minimum operating voltage after turnon is required for stable operation. The minimum VDD operating voltage for the controller selected for this design is 10V. The auxiliary winding is selected to support a 12V bias voltage so that it is above the minimum operating level but maintains a low level of losses in the IC. The primary to auxiliary turns ratio (N_{PA}) can be calculated from Equation 7:

$$N_{PA} = N_{PS} \times \frac{V_{OUT}}{V_{BIAS}} = 10 \tag{7}$$

The output diode experiences a voltage stress that is equal to the output voltage plus the reflected input voltage:

$$V_{DIODE} = \frac{V_{BULK\,(max)}}{N_{PS}} + V_{OUT} = 49.5\ V \tag{8}$$

TI recommends a Schottky diode with a rated blocking voltage greater than 60V to allow for voltage spikes due to ringing. The forward voltage drop (V_F) of this diode is estimated to be equal to 0.6V

To avoid high peak currents, the flyback converter in this design operates in continuous conduction mode. Once N_{PS} is determined, the maximum duty cycle (D_{MAX}) can be calculated using the transfer function for a CCM flyback converter:

$$\frac{V_{OUT} + V_F}{V_{BULK\,(min)}} = \left(\frac{1}{N_{PS}}\right) \times \left(\frac{D_{MAX}}{1 - D_{MAX}}\right) \tag{9}$$

$$D_{MAX} = \frac{N_{PS} \times (V_{OUT} + V_F)}{V_{BULK(min)} + N_{PS} \times (V_{OUT} + V_F)} = 0.627 \tag{10}$$

Because the maximum duty cycle exceeds 50%, and the design is an off-line (AC-input) application, the UCC28C42 is best suited for this application.

8.2.2.3 Transformer Inductance and Peak Currents

For this design example, the transformer magnetizing inductance is selected based upon the CCM condition. An inductance value that allows the converter to stay in CCM over a wider operating range before transitioning into discontinuous current mode is used to minimize losses due to otherwise high currents and also to decrease the output ripple. The design of the transformer in this example sizes the inductance so the converter enters CCM operation at approximately 10% load and minimum bulk voltage to minimize output ripple.

The inductor (L_P) for a CCM flyback can be calculated using Equation 11.

$$L_P = \frac{1}{2} \times \frac{\left(V_{BULK\,(min)}\right)^2 \times \left(\frac{N_{PS} \times V_{OUT}}{V_{BULK\,(min)} + N_{PS} \times V_{OUT}}\right)^2}{0.1 \times P_{IN} \times f_{SW}} \tag{11}$$

where

- P_{IN} is estimated by dividing the maximum output power (P_{OUT}) by the target efficiency (η)
- f_{SW} is the switching frequency of the converter

For the UCC28C42 the switching frequency is equal to the oscillator frequency and is set to 110kHz. Selecting f_{SW} to be 110kHz provides a good compromise between size of magnetics, switching losses, and places the first harmonic below the 150kHz lower limit of EN55022. Therefore, the transformer inductance must be approximately 1.8mH. A 1.5mH inductance is chosen as the magnetizing inductance, L_P, value for this design.

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Based on calculated inductor value and the switching frequency, the current stress of the MOSFET and output diode can be calculated.

The peak current in the primary-side MOSFET of a CCM flyback can be calculated as shown in Equation 12.

$$I_{PK_{MOSFET}} = \frac{P_{IN}}{V_{BULK\,(min)} \times \frac{N_{PS} \times V_{OUT}}{V_{BULK\,(min)} + (N_{PS} \times V_{OUT})}} + \left(\frac{V_{BULK\,(min)}}{2 \times L_m} \times \frac{\frac{N_{PS} \times V_{OUT}}{V_{BULK\,(min)} + (N_{PS} \times V_{OUT})}}{f_{SW}} \right) \quad (12)$$

The MOSFET peak current is 1.36A. The RMS current of the MOSFET is calculated to be 0.97A as shown in Equation 13. Therefore, IRFB9N65A is selected to be used as the primary-side switch.

$$I_{RMS_{MOSFET}} = \sqrt{\frac{{D_{MAX}}^3}{3} \times \left(\frac{V_{BULK\,(min)}}{L_P \times f_{SW}} \right)^2 - \left(\frac{{D_{MAX}}^2 \times I_{PK_{MOSFET}} \times V_{BULK\,(min)}}{L_P \times f_{SW}} \right) + \left(D_{MAX} \times {I_{PK_{MOSFET}}}^2 \right)} \quad (13)$$

The output diode peak current is equal to the MOSFET peak current reflected to the secondary side.

$$I_{PK_{DIODE}} = N_{PS} \times I_{PK_{MOSFET}} = 13.634\ A \quad (14)$$

The diode average current is equal to the total output current (4A) combined with a required 60V rating and 13.6A peak current requirement, a 48CTQ060-1 is selected for the output diode.

8.2.2.4 Output Capacitor

The total output capacitance is selected based upon the output voltage ripple requirement. In this design, 0.1% voltage ripple is assumed. Based on the 0.1% ripple requirement, the capacitor value can be selected using Equation 15.

$$C_{OUT} \geq \frac{I_{OUT} \times \frac{N_{PS} \times V_{OUT}}{V_{BULK\,(min)} + N_{PS} \times V_{OUT}}}{0.001 \times V_{OUT} \times f_{SW}} = 1865\ \mu F \quad (15)$$

To design for device tolerances, a 2200-µF capacitor was selected.

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8.2.2.5 Current Sensing Network

The current sensing network consists of the primary-side current sensing resistor (R_{CS}), filtering components R_{CSF} and C_{CSF}, and optional R_P. Typically, the direct current sense signal contains a large amplitude leading edge spike associated with the turnon of the main power MOSFET, reverse recovery of the output rectifier, and other factors including charging and discharging of parasitic capacitances. Therefore, C_{CSF} and R_{CSF} form a low-pass filter that provides immunity to suppress the leading edge spike. For this converter, C_{CSF} is chosen to be 100pF.

Without R_P, R_{CS} sets the maximum peak current in the transformer primary based on the maximum amplitude of the CS pin, which is specified to be 1V. To achieve 1.36A primary side peak current, a 0.75Ω resistor is chosen for R_{CS}.

The high current sense threshold of CS helps to provide better noise immunity to the system but also results in higher losses in the current sense resistor. These current sense losses can be minimized by injecting an offset voltage into the current sense signal using R_P. R_P and R_{CSF} form a resistor divider network from the current sense signal to the reference voltage of the controller (V_{VREF}) which adds an offset to the current sense voltage. This technique still achieves current mode control with cycle-by-cycle over-current protection. To calculate required offset value (V_{OFFSET}), use Equation 16.

$$V_{OFFSET} = \frac{R_{CSF}}{R_{CSF} + R_P} \times V_{REF} \tag{16}$$

After adding the R_P resistance, adjust the R_{CS} value accordingly.

8.2.2.6 Gate Drive Resistor

R_G is the gate driver resistor for the power switch (Q_{SW}). The selection of this resistor value must be done in conjunction with EMI compliance testing and efficiency testing. Using a larger resistor value for R_G slows down the turnon and turnoff of the MOSFET. A slower switching speed reduces EMI but also increases the switching loss. A tradeoff between switching loss and EMI performance must be carefully performed. For this design, a 10Ω resistor was chosen for the gate drive resistor.

8.2.2.7 VREF Capacitor

A precision 5V reference voltage performs several important functions. The reference voltage is divided down internally to 2.5V and connected to the error amplifier's noninverting input for accurate output voltage regulation. Other duties of the reference voltage are to set internal bias currents and thresholds for functions such as the oscillator upper and lower thresholds. Therefore, the reference voltage must be bypassed with a ceramic capacitor. A 1µF, 16V ceramic capacitor was selected for this converter. Placement of this capacitor on the physical printed-circuit board layout must be as close as possible to the respective VREF and GND pins.

8.2.2.8 RT/CT

The internal oscillator uses a timing capacitor (C_{CT}) and a timing resistor (R_{RT}) to program the oscillator frequency and maximum duty cycle. The operating frequency can be programmed based the curves in Oscillator Frequency vs Timing Resistance and Capacitance, where the timing resistor can be found once the timing capacitor is selected. It is best for the timing capacitor to have a flat temperature coefficient, typical of most COG or NPO type capacitors. For this converter, 15.4kΩ and 1000pF were selected for R_{RT} and C_{CT} to operate at 110kHz switching.

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8.2.2.9 Start-Up Circuit

At start-up, the IC gets its power directly from the high-voltage bulk, through a high-voltage resistor (R_{START}). The selection of the start-up resistor is the tradeoff between power loss and start-up time. The current flowing through R_{START} at the minimum input voltage must be higher than the VDD current under UVLO conditions (100µA at its maximum value). A resistance of 420kΩ was chosen for R_{START}, providing 250µA of start-up current at low-line conditions. The start-up resistor is physically comprised of two 210kΩ resistors in series to meet the high voltage requirements and power rating at high-line.

After VDD is charged up above the UVLO-ON threshold, the UCC28C42 starts to consume full operating current. The VDD capacitor is required to provide enough energy to prevent its voltage from dropping below the UVLO-OFF threshold during start-up, before the output is able to reach its regulated level. A large bulk capacitance would hold more energy but would result in slower start-up time. In this design, a 120µF capacitor is chosen to provide enough energy and maintain a start-up time of approximately 7 seconds. For faster start-up, the bulk capacitor value may be decreased or the R_{START} resistor modified to a lower value.

8.2.2.10 Voltage Feedback Compensation

Feedback compensation, also called closed-loop control, can reduce or eliminate steady state error, reduce the sensitivity of the system to parametric changes, change the gain or phase of a system over some desired frequency range, reduce the effects of small signal load disturbances and noise on system performance, and create a stable system from an unstable system. A system is stable if its response to a perturbation is that the perturbation eventually dies out. A peak current mode flyback uses an outer voltage feedback loop to stabilize the converter. To adequately compensate the voltage loop, the open-loop parameters of the power stage must be determined.

8.2.2.10.1 Power Stage Poles and Zeroes

The first step in compensating a fixed frequency flyback is to verify if the converter is continuous conduction mode (CCM) or discontinuous conduction mode (DCM). If the primary inductance (L_P) is greater than the inductance for DCM or CCM boundary mode operation, called the critical inductance (L_{Pcrit}), then the converter operates in CCM:

$$L_P > L_{Pcrit}\text{, then CCM} \tag{17}$$

$$L_{Pcrit} = \frac{R_{OUT} \times (N_{PS})^2}{2 \times f_{SW}} \times \left(\frac{V_{IN}}{V_{IN} + V_{OUT} \times N_{PS}}\right)^2 \tag{18}$$

For the entire input voltage range, the selected inductor has a value larger than the critical inductor. Therefore, the converter operates in CCM and the compensation loop requires design based on CCM flyback equations.

The current-to-voltage conversion is done externally with the ground-referenced R_{CS} and the internal 2R/R resistor divider which sets up the internal current sense gain, A_{CS} = 3. The exact value of these internal resistors is not critical but the IC provides tight control of the resistor divider ratio, so regardless of the actual resistor value variations their relative value to each other is maintained.

The DC open-loop gain (G_O) of the fixed-frequency voltage control loop of a peak current mode control CCM flyback converter shown in Equation 19 is approximated by first using the output load (R_{OUT}), the primary to secondary turns ratio (N_{PS}), and the maximum duty cycle (D) as calculated in Equation 20.

$$G_O = \frac{R_{OUT} \times N_{PS}}{R_{CS} \times A_{CS}} \times \frac{1}{\frac{(1-D)^2}{\tau_L} + (2 \times M) + 1} \tag{19}$$

In Equation 19, D is calculated with Equation 20, τ_L is calculated with Equation 21, and M is calculated with Equation 22.

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$$D = \frac{N_{PS} \times V_{OUT}}{V_{BULKmin} + (N_{PS} \times V_{OUT})} \quad (20)$$

$$\tau_L = \frac{2 \times L_P \times f_{SW}}{R_{OUT} \times (N_{PS})^2} \quad (21)$$

$$M = \frac{V_{OUT} \times N_{PS}}{V_{BULKmin}} \quad (22)$$

For this design, a converter with an output voltage (V_{OUT}) of 12V, and 48W relates to an output load (R_{OUT}) equal to 3Ω at full load. With a maximum duty cycle of 0.627, a current sense resistance of 0.75Ω, and a primary to secondary turns-ratio of 10, the open-loop gain calculates to 3.082 or 9.776dB.

A CCM flyback has two zeroes that are of interest. The ESR and the output capacitance contribute a left-half plane zero (ω_{ESRz}) to the power stage, and the frequency of this zero (f_{ESRz}), are calculated with Equation 23 and Equation 24.

$$\omega_{ESRz} = \frac{1}{R_{ESR} \times C_{OUT}} \quad (23)$$

$$f_{ESRz} = \frac{1}{2 \times \pi \times R_{ESR} \times C_{OUT}} \quad (24)$$

The f_{ESRz} zero for an output capacitance of 2200µF and a total ESR of 43mΩ is located at 1.682 kHz.

CCM flyback converters have a zero in the right-half plane (RHP) in their transfer function. A RHP zero has the same 20dB per decade rising gain magnitude with increasing frequency just like a left-half plane zero, but it adds a 90° phase lag instead of lead. This phase lag tends to limit the overall loop bandwidth. The frequency location (f_{RHPz}) of the RHP zero (ω_{RHPz}) is a function of the output load, the duty cycle, the primary inductance (L_P), and the primary to secondary side turns ratio (N_{PS}).

$$\omega_{RHPz} = \frac{R_{OUT} \times (1-D)^2 \times (N_{PS})^2}{L_P \times D} \quad (25)$$

$$f_{RHPz} = \frac{R_{OUT} \times (1-D)^2 \times (N_{PS})^2}{2 \times \pi \times L_P \times D} \quad (26)$$

The right-half plane zero frequency increases with higher input voltage and lighter load. Generally, the design requires consideration of the worst case of the lowest right-half plane zero frequency and the converter must be compensated at the minimum input and maximum load condition. With a primary inductance of 1.5mH, at 75V DC input, the RHP zero frequency (f_{RHPz}) is equal to 7.07kHz at maximum duty cycle, full load.

The power stage has one dominate pole (ω_{P1}) which is in the region of interest, located at a lower frequency (f_{P1}); which is related to the duty cycle, the output load, and the output capacitance, and calculated with Equation 28. There is also a double pole placed at half the switching frequency of the converter (f_{P2}) calculated with Equation 30. For this example, pole f_{P1} is located at 40.37Hz and f_{P2} is at 55kHz.

$$\omega_{P1} = \frac{\frac{(1-D)^3}{\tau_L} + 1 + D}{R_{OUT} \times C_{OUT}} \quad (27)$$

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$$f_{P1} = \frac{\frac{(1-D)^3}{\tau_L} + 1 + D}{2 \times \pi \times R_{OUT} \times C_{OUT}} \quad (28)$$

$$\omega_{P2} = \pi \times f_{SW} \quad (29)$$

$$f_{P2} = \frac{f_{SW}}{2} \quad (30)$$

8.2.2.10.2 Slope Compensation

Slope compensation is the large signal subharmonic instability that can occur with duty cycles that may extend beyond 50% where the rising primary side inductor current slope may not match the falling secondary side current slope. The subharmonic oscillation would result in an increase in the output voltage ripple and may even limit the power handling capability of the converter.

The target of slope compensation is to achieve an ideal quality coefficient (Q_P), equal to 1 at half of the switching frequency. The Q_P is calculated with Equation 31.

$$Q_P = \frac{1}{\pi \times [M_C \times (1-D) - 0.5]} \quad (31)$$

where

- D is the primary side switch duty cycle
- M_C is the slope compensation factor, which is defined with Equation 32

$$M_C = \frac{S_e}{S_n} + 1 \quad (32)$$

where

- S_e is the compensation ramp slope
- S_n is the inductor rising slope

The optimal goal of the slope compensation is to achieve Q_P = 1; upon rearranging Equation 32 the ideal value of slope compensation factor is determined:

$$M_{ideal} = \frac{\frac{1}{\pi} + 0.5}{1-D} \quad (33)$$

For this design to have adequate slope compensation, M_C must be 2.193 when D reaches it maximum value of 0.627.

The inductor rising slope (S_n) at the CS pin is calculated with Equation 34.

$$S_n = \frac{V_{INmin} \times R_{CS}}{L_P} = 0.038 \ \frac{V}{\mu s} \quad (34)$$

The compensation slope (S_e) is calculated with Equation 35.

$$S_e = (M_C - 1) \times S_n = 44.74 \ \frac{mV}{\mu s} \quad (35)$$

The compensation slope is added into the system through R_{RAMP} and R_{CSF}. The C_{RAMP} is an AC-coupling capacitor that allows the voltage ramp of the oscillator to be used without adding an offset to the current sense; select a value to approximate a high-frequency short circuit, such as 10nF, as a starting point and make adjustments if required. The R_{RAMP} and R_{CSF} resistors form a voltage divider from the oscillator charge slope and this proportional ramp is injected into the CS pin to add slope compensation. Choose the value of R_{RAMP} to be much larger than the R_{RT} resistor so that it does not load down the internal oscillator and result in a frequency shift. The oscillator charge slope is calculated using the peak-to-peak voltage of the RT/CT sawtooth waveform (V_{OSCpp}) equal to 1.9V, and the minimum ON time, as shown in Equation 37.

$$t_{ONmin} = \frac{D}{f_{SW}} \tag{36}$$

$$S_{OSC} = \frac{V_{OSCpp}}{t_{ONmin}} = \frac{1.9\ V}{5.7\ \mu s} = 333\ \frac{mV}{\mu s} \tag{37}$$

To achieve a 44.74-mV/µs compensation slope, R_{CSF} is calculated with Equation 38. In this design, R_{RAMP} is selected as 24.9kΩ, a 3.8kΩ resistor was selected for R_{CSF}.

$$R_{CSF} = \frac{R_{RAMP}}{\frac{S_{OSC}}{S_e} - 1} \tag{38}$$

8.2.2.10.3 Open-Loop Gain

Once the power stage poles and zeros are calculated and the slope compensation is determined, the power stage open-loop gain and phase of the CCM flyback converter can be plotted as a function of frequency. The power stage transfer function can be characterized with Equation 39.

$$H_{OPEN}(s) = G_0 \times \frac{\left(1 + \frac{s(f)}{\omega_{ESRz}}\right) \times \left(1 - \frac{s(f)}{\omega_{RHPz}}\right)}{1 + \frac{s(f)}{\omega_{P1}}} \times \frac{1}{1 + \frac{s(f)}{\omega_{P2} \times Q_P} + \frac{s(f)^2}{(\omega_{P2})^2}} \tag{39}$$

The bode for the open-loop gain and phase can be plotted by using Equation 40.

$$Gain_{OPEN}(s) = 20 \times \log(|H_{OPEN}(s)|) \tag{40}$$

See Figure 8-4 and Figure 8-5.

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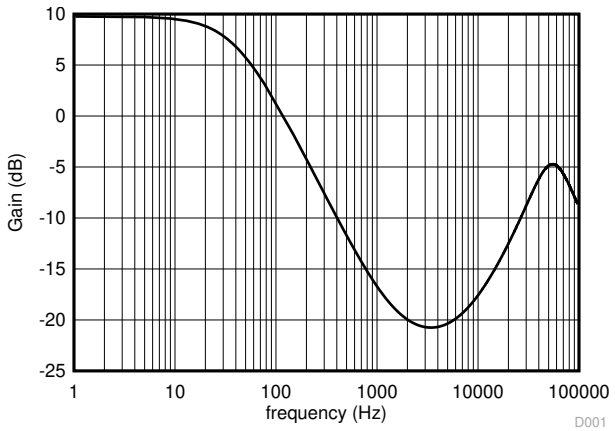


Figure 8-4. Converter Open-Loop Bode Plot - Gain

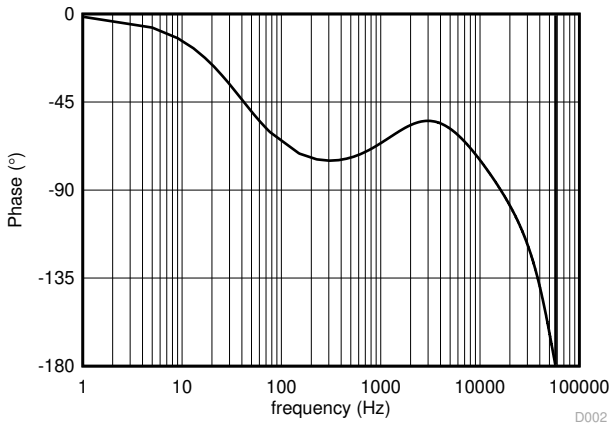


Figure 8-5. Converter Open-Loop Bode Plot - Phase

8.2.2.10.4 Compensation Loop

The design of the compensation loop involves selecting the appropriate components so that the required gain, poles, and zeros can be designed to result in a stable system over the entire operating range. There are three distinct portions of the loop: the TL431, the opto-coupler, and the error amplifier. Each of these stages combines with the power stage to result in a stable robust system.

For good transient response, the bandwidth of the finalized design must be as large as possible. The bandwidth of a CCM flyback, f_{BW}, is limited to ¼ of the RHP zero frequency, or approximately 1.77kHz using Equation 41.

$$f_{BW} = \frac{f_{RHPz}}{4} \tag{41}$$

The gain of the open-loop power stage at f_{BW} can be calculated using Equation 40 or can be observed on the Bode plot (Figure 8-4) and is equal to –19.55dB and the phase at f_{BW} is equal to –58°.

The secondary side portion of the compensation loop begins with establishing the regulated steady state output voltage. To set the regulated output voltage, a TL431 adjustable precision shunt regulator is ideally suited for use on the secondary side of isolated converters due to its accurate voltage reference and internal op-amp. The resistors used in the divider from the output terminals of the converter to the TL431 REF pin are selected based upon the desired power consumption. Because the REF input current for the TL431 is only 2µA, selecting the resistors for a divider current (I_{FB_REF}) of 1mA results in minimal error. The top divider resistor (R_{FBU}) is calculated:

$$R_{FBU} = \frac{V_{OUT} - REF_{TL431}}{I_{FB_REF}} \tag{42}$$

The TL431 reference voltage (REF_{TL431}) has a typical value of 2.495V. A 9.53kΩ resistor is chosen for R_{FBU}. To set the output voltage to 12V, 2.49kΩ is used for R_{FBB}.

$$R_{FBB} = \frac{REF_{TL431}}{V_{OUT} - REF_{TL431}} \times R_{FBU} \tag{43}$$

For good phase margin, a compensator zero (f_{COMPz}) is required and should be placed at 1/10th the desired bandwidth:

$$f_{COMPz} = \frac{f_{BW}}{10} \tag{44}$$

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$$\omega_{COMPz} = 2 \times \pi \times f_{COMPz} \quad (45)$$

With this converter, f_{COMPz} should be set at approximately 177Hz. A series resistor (R_{COMPz}) and capacitor (C_{COMPz}) placed across the TL431 cathode to REF sets the compensator zero location. Setting C_{COMPz} to 0.01µF, R_{COMPz} is calculated:

$$R_{COMPz} = \frac{1}{\omega_{COMPz} \times C_{COMPz}} \quad (46)$$

Using a standard value of 88.7kΩ for R_Z and a 0.01µF for C_Z results in a zero placed at 179Hz.

In Figure 8-3, R_{TLbias} provides cathode current to the TL431 from the regulated voltage provided from the Zener diode (D_{REG}). For robust performance, 10mA is provided to bias the TL431 by way of the 10V Zener and a 1kΩ resistor is used for R_{TLbias}.

The gain of the TL431 portion of the compensation loop is calculated with Equation 47.

$$G_{TL431}(s) = \left(R_{COMPz} + \frac{1}{s(f) \times C_{ZCOMPz}}\right) \times \frac{1}{R_{FBU}} \quad (47)$$

A compensation pole is required at the frequency of right half plane zero or the ESR zero, whichever is lowest. Based previous the analysis, the right half plane zero (f_{RHPz}) is located at 7.07 kHz and the ESR zero (f_{ESRz}) is at 1.68 kHz; therefore, for this design, the compensation pole must be put at 1.68 kHz. The opto-coupler contains a parasitic pole that is difficult to characterize over frequency so the opto-coupler is set up with a pull-down resistor (R_{OPTO}) equal to 1kΩ, which moves the parasitic opto-coupler pole further out and beyond the range of interest for this design.

The required compensation pole can be added to the primary side error amplifier using R_{COMPp} and C_{COMPp}. Choosing R_{COMPp} as 10kΩ, the required value of C_{COMPp} is determined using Equation 48.

$$C_{COMPp} = \frac{1}{2 \times \pi \times f_{ESRz} \times R_{COMPp}} = 9.46\ nF \quad (48)$$

A 10-nF capacitor is used for C_{COMPp} setting the compensation pole at 1.59 kHz.

Adding a DC gain to the primary-side error amplifier may be required to obtain the required bandwidth and helps to adjust the loop gain as needed. Using 4.99 kΩ for R_{FBG} sets the DC gain on the error amplifier to 2. At this point the gain transfer function of the error amplifier stage ($G_{EA}(s)$) of the compensation loop can be characterized using Equation 49.

$$G_{EA}(s) = \left(\frac{R_{COMPp}}{R_{FBG}}\right) \times \left(\frac{1}{1 + s(f) \times C_{COMPp} \times R_{COMPp}}\right) \quad (49)$$

Using an opto-coupler whose current transfer ratio (CTR) is typically at 100% in the frequency range of interest so that CTR = 1, the transfer function of the opto-coupler stage ($G_{OPTO}(s)$) is found using Equation 50.

$$G_{OPTO}(s) = \frac{CTR \times R_{OPTO}}{R_{LED}} \quad (50)$$

The bias resistor (R_{LED}) to the internal diode of the opto-coupler and the pull-down resistor on the opto emitter (R_{OPTO}) sets the gain across the isolation boundary. R_{OPTO} has already been set to 1kΩ but the value of R_{LED} has not yet been determined.

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The total closed loop gain ($G_{TOTAL}(s)$) is the combination of the open-loop power stage ($H_o(s)$), the opto gain ($G_{OPTO}(s)$), the error amplifier gain ($G_{EA}(s)$), and the gain of the TL431 stage ($G_{TL431}(s)$), as shown in Equation 51.

$$G_{TOTAL}(s) = |H_{OPEN}(s)| \times |G_{OPTO}(s)| \times |G_{EA}(s)| \times |G_{TL431}(s)| \quad (51)$$

The required value for R_{LED} can be selected to achieve the desired crossover frequency (f_{BW}). By setting the total loop gain equal to 1 at the desired crossover frequency and rearranging Equation 51, the optimal value for R_{LED} can be determined, as shown in Equation 52.

$$R_{LED} \leq |H_{OPEN}(s)| \times |CTR \times C_{OPTO}| \times |G_{EA}(s)| \times |G_{TL431}(s)| \quad (52)$$

A 1.3kΩ resistor suits the requirement for R_{LED}.

Based on the compensation loop structure, the entire compensation loop transfer function is written as Equation 53.

$$G_{CLOSED}(s) = H_{OPEN}(s) \times \left(\frac{CTR \times R_{OPTO}}{R_{LED}}\right) \times \left(\frac{R_{COMPp}}{R_{FBG}}\right) \times \left(\frac{1}{1 + \left(s \times C_{COMPp} \times R_{COMPp}\right)}\right) \times \left(\frac{R_{COMPz} + \left(\frac{1}{s \times C_{COMPz}}\right)}{R_{FBU}}\right) \quad (53)$$

The final closed-loop bode plots are show in Figure 8-6 and Figure 8-7. The converter achieves a crossover frequency of approximately 1.8kHz and has a phase margin of approximately 67°.

TI recommends checking the loop stability across all the corner cases including component tolerances to ensure system stability.

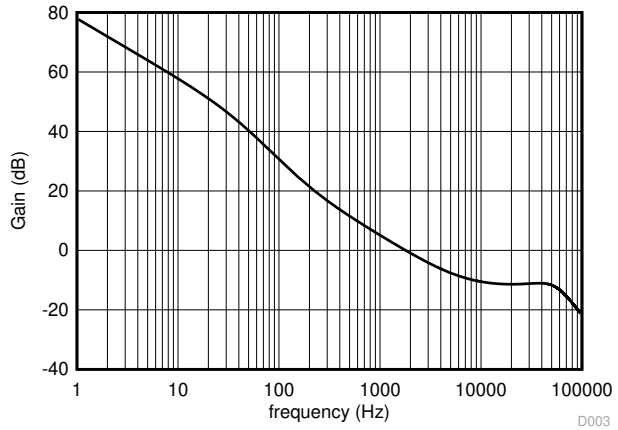


Figure 8-6. Converter Closed-Loop Bode Plot – Gain

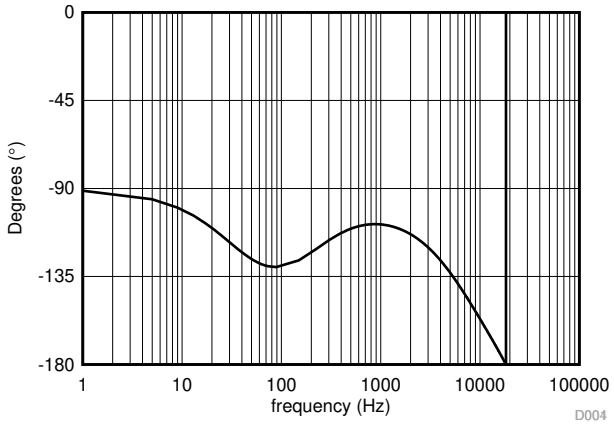


Figure 8-7. Converter Closed-Loop Bode Plot – Phase

8.2.3 Application Curves

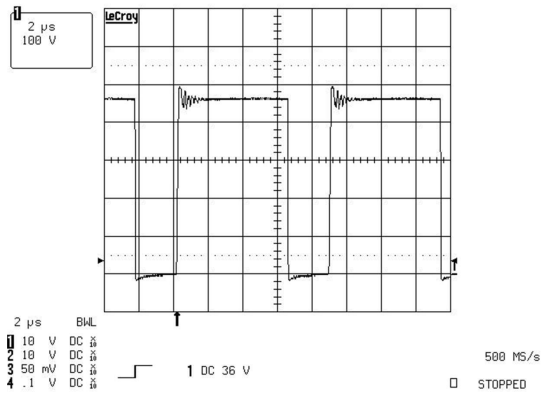


Figure 8-8. Primary Side MOSFET Drain to Source Voltage at 240V AC Input (100V/div)

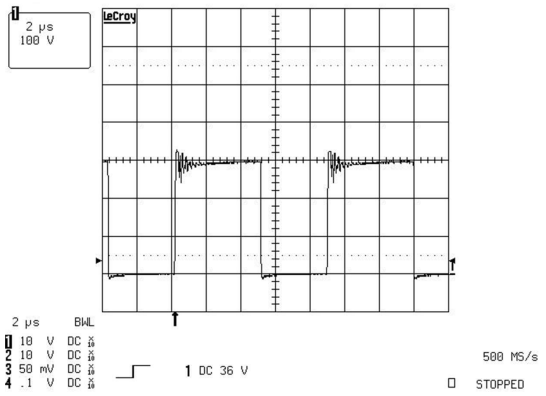
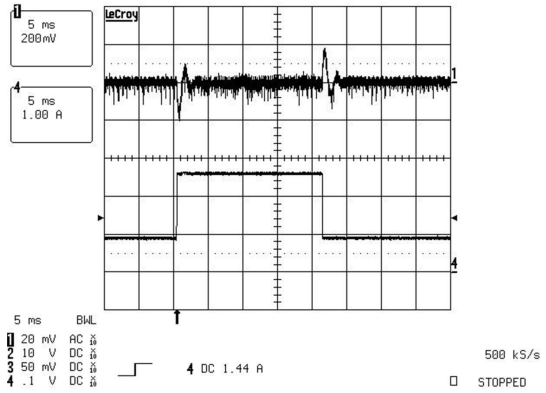


Figure 8-9. Primary Side MOSFET Drain to Source Voltage at 120V AC Input (100 V/div)



CH1: Output Voltage AC Coupled, 200mV/div
CH4: Output Current, 1A/div

Figure 8-10. Output Voltage During 0.9A to 2.7A Load Transient

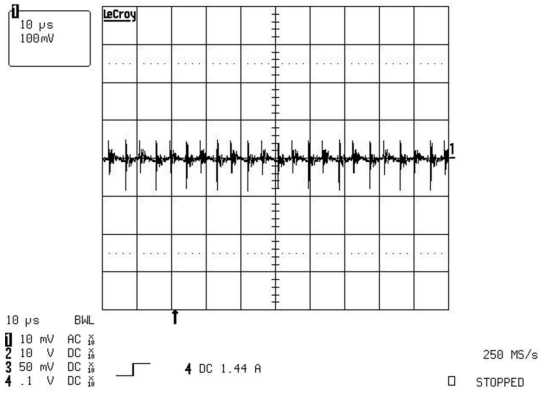


Figure 8-11. Output Voltage Ripple at Full Load (100mV/div)

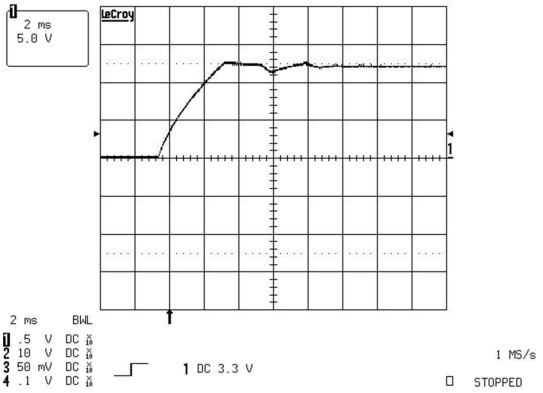


Figure 8-12. Output Voltage Behavior at Full Load Start-up (5V/div)

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8.3 Power Supply Recommendations

The absolute maximum supply voltage is 20V of UCC28C42, including any transients that may be present. If this voltage is exceeded, device damage is likely. This damage risk is in contrast to the predecessor bipolar devices, which could survive up to 30V. Thus, the supply pin must be decoupled as close to the GND pin as possible.

Because no clamp is included in the device, the supply pin must be protected from external sources which could exceed the 20V level.

To prevent false triggering due to leading edge noises, an RC current sense filter may be required on CS. Keep the time constant of the RC filter well below the minimum on-time pulse width.

To prevent noise problems with high-speed switching transients, bypass VREF to ground with a ceramic capacitor close to the IC package. A minimum of 0.1µF ceramic capacitor is required. Additional VREF bypassing is required for external loads on the reference. An electrolytic capacitor may also be used in addition to the ceramic capacitor.

8.4 Layout

8.4.1 Layout Guidelines

8.4.1.1 Precautions

Careful layout of the printed board is a necessity for high-frequency power supplies. As the device-switching speeds and operating frequencies increase, the layout of the converter becomes increasingly important.

This 8-pin device has only a single ground for the logic and power connections. This forces the gate-drive current pulses to flow through the same ground that the control circuit uses for reference. Thus, the interconnect inductance must be minimized as much as possible. One implication is to place the device (gate driver) circuitry close to the MOSFET it is driving. This can conflict with the need for the error amplifier and the feedback path to be away from the noise generating components.

The single most critical item in a PWM controlled printed-circuit board layout is the placement of the timing capacitor. While both the supply and reference bypass capacitor locations are important, the timing capacitor placement is far more critical. Any noise spikes on the C_{CT} waveform due to lengthy printed circuit trace inductance or pick-up noise from being in proximity to high power switching noise causes a variety of operational problems. Dilemmas vary from incorrect operating frequency caused by pre-triggering the oscillator due to noise spikes to frequency jumping with varying duty cycles, also caused by noise spikes. The placement of the timing capacitor must be treated as the most important layout consideration. Keep PC traces as short as possible to minimize added series inductance.

8.4.1.2 Feedback Traces

Try to run the feedback trace as far from the inductor and noisy power traces as possible. You would also like the feedback trace to be as direct as possible and somewhat thick. These two sometimes involve a trade-off, but keeping it away from EMI and other noise sources is the more critical of the two. If possible, run the feedback trace on the side of the PCB opposite of the inductor with a ground plane separating the two.

8.4.1.3 Bypass Capacitors

When using a low value ceramic bypass capacitor, it must be placed as close to the VDD pin of the device as possible. This eliminates as much trace inductance effects as possible and give the internal device rail a cleaner voltage supply. Using surface mount capacitors also reduces lead length and lessens the chance of noise coupling into the effective antenna created by through-hole components.

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8.4.1.4 Compensation Components

For best stability, external compensation components must be placed close to the IC. Keep FB lead length as short as possible and FB stray capacitance as small as possible. TI recommends surface mount components here as well for the same reasons discussed for the filter capacitors. These must not be placed very close to traces with high switching noise.

8.4.1.5 Traces and Ground Planes

Make all of the power (high current) traces as short, direct, and thick as possible. It is good practice on a standard PCB board to make the traces an absolute minimum of 15 mils (0.381 mm) per ampere. The inductor, output capacitors, and output diode must be as close to each other possible. This helps reduce the EMI radiated by the power traces due to the high switching currents through them. This also reduces lead inductance and resistance as well, which in turn reduces noise spikes, ringing, and resistive losses that produce voltage errors.

The grounds of the IC, input capacitors, output capacitors, and output diode, if applicable, must be connected close together directly to a ground plane. It would also be a good idea to have a ground plane on both sides of the PCB. This reduces noise as well by reducing ground loop errors as well as by absorbing more of the EMI radiated by the inductor. For multi-layer boards with more than two layers, a ground plane can be used to separate the power plane, where the power traces and components are, and the signal plane, where the feedback and compensation and components are, for improved performance. On multi-layer boards the use of vias is required to connect traces and different planes. It is good practice to use one standard via per 200 mA of current if the trace conducts a significant amount of current from one plane to the other.

Arrange the components so that the switching current loops curl in the same direction. Due to the way switching regulators operate, there are two power states. One state when the switch is ON and one when the switch is OFF. During each state there is a current loop made by the power components that are currently conducting. Place the power components so that during each of the two states the current loop is conducting in the same direction. This prevents magnetic field reversal caused by the traces between the two half-cycles and reduces radiated EMI.

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8.4.2 Layout Example

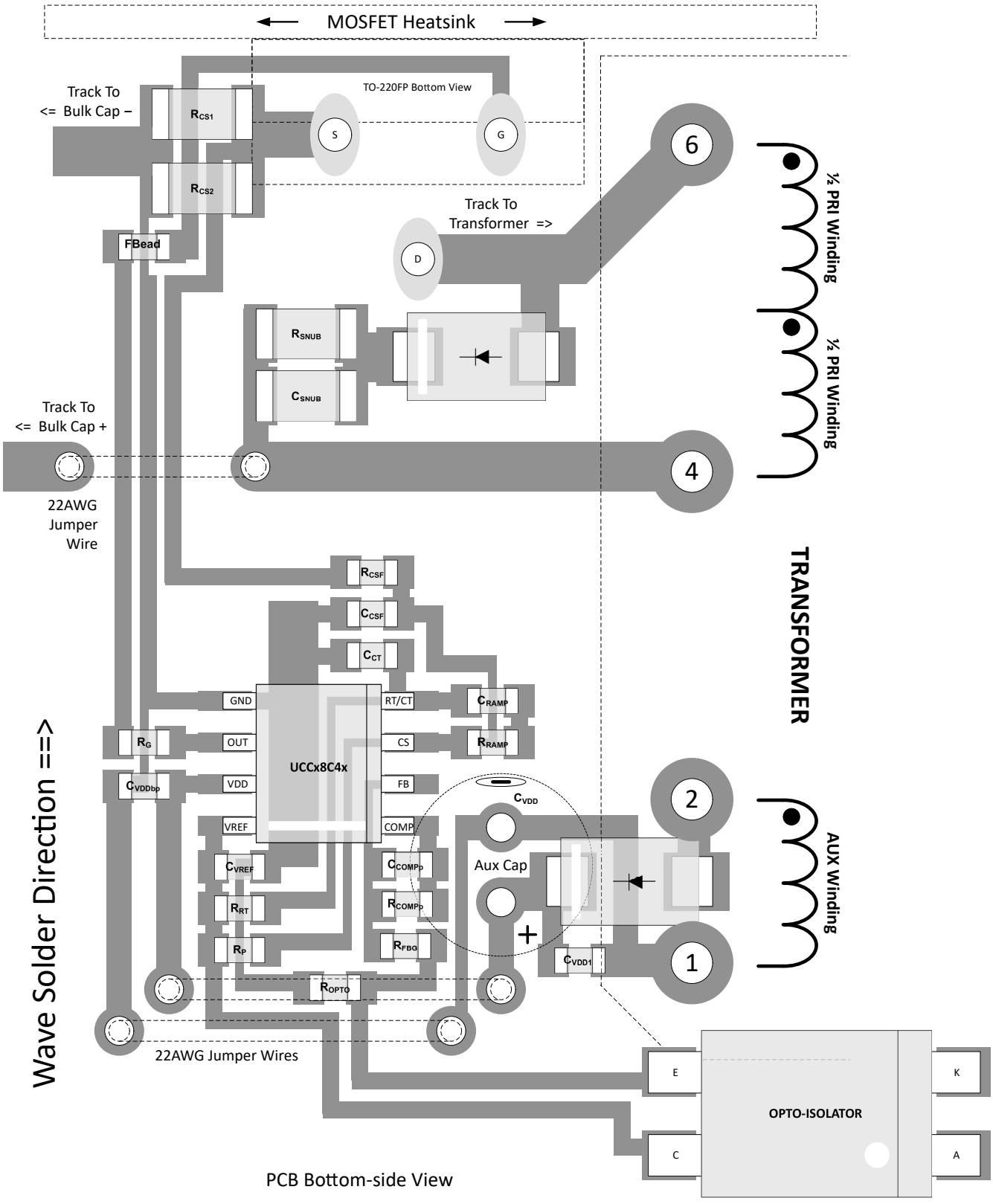


Figure 8-13. UCCx8C4x Layout Example

9 Device and Documentation Support

9.1 Device Support

9.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

UC384x Provides Low-Cost Current-Mode Control (SLUA143)

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.5 Trademarks

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9.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (September 2022) to Revision I (June 2024)	Page
• Added COMP pin short circuit current into Electrical Characteristics section	7

Changes from Revision G (January 2017) to Revision H (September 2022)	Page
• Changed -40°C to 105°C to -40°C to 125°C, and 0°C to 70°C to 0°C to 85°C	1
• Removed *PDIP* package from Device Information	1
• Updated T_J *range* in Device Comparison Table	3
• Removed *PDIP* package from Pin Configuration	4
• Removed *PDIP* package from Absolute Maximum Table	5
• Updated *Total Power Dissipation* values in Absolute Maximum Table	5
• Added V_{REF} *maximum continuous voltage* from external circuitry in Recommended Operating Conditions	6
• Updated T_J *max values* in Recommended Operating Conditions Table	6
• Updated all *Thermal Resistance Numbers* in Thermal Information	7
• Updated Electrical Characteristics section	7

Changes from Revision F (August 2016) to Revision G (January 2017)	Page
• Changed $V_{REFLECTED}$ equation.	27
• Changed D_{MAX} equation.	27

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC28C40D	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	28C40
UCC28C40DGK	Obsolete	Production	VSSOP (DGK) | 8	-	-	Call TI	Call TI	-40 to 125	28C40
UCC28C40DGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(28C40, 2C40)
UCC28C40DGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(28C40, 2C40)
UCC28C40DGKRG4	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2C40
UCC28C40DGKRG4.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2C40
UCC28C40DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28C40
UCC28C40DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28C40
UCC28C41D	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	28C41
UCC28C41DGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	-	Call TI	Level-2-260C-1 YEAR	-40 to 125	(28C41, 2C41)
UCC28C41DGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	-	Call TI	Level-2-260C-1 YEAR	-40 to 125	(28C41, 2C41)
UCC28C41DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28C41
UCC28C41DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28C41
UCC28C42DGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	-	Call TI	Level-2-260C-1 YEAR	-40 to 125	(28C42, 2C42)
UCC28C42DGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	-	Call TI	Level-2-260C-1 YEAR	-40 to 125	(28C42, 2C42)
UCC28C42DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28C42
UCC28C42DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28C42
UCC28C42DRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28C42
UCC28C43DGK	Obsolete	Production	VSSOP (DGK) | 8	-	-	Call TI	Call TI	-40 to 125	28C43
UCC28C43DGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	-	Call TI	Level-2-260C-1 YEAR	-40 to 125	(28C43, 2C43)
UCC28C43DGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	-	Call TI	Level-2-260C-1 YEAR	-40 to 125	(28C43, 2C43)
UCC28C43DGKRG4	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	-	Call TI	Level-2-260C-1 YEAR	-40 to 125	(28C43, 2C43)
UCC28C43DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28C43
UCC28C43DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28C43
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UCC28C44DGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(28C44, 2C44)
UCC28C44DGKRG4	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2C44

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
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UCC28C44DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28C44
UCC28C44DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28C44
UCC28C44DRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28C44
UCC28C45DGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(28C45, 2C45)
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UCC28C45DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28C45
UCC28C45DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28C45
UCC28C45DRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28C45
UCC38C40DGK	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	0 to 85	38C40
UCC38C40DGK.A	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	0 to 85	38C40
UCC38C40DGKR	NRND	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	Call TI | Nipdauag	Level-2-260C-1 YEAR	0 to 85	38C40
UCC38C40DGKR.A	NRND	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	0 to 85	38C40
UCC38C40DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 85	38C40
UCC38C40DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 85	38C40
UCC38C41DGK	Active	Production	VSSOP (DGK) | 8	100 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	0 to 85	38C41
UCC38C41DGK.A	Active	Production	VSSOP (DGK) | 8	100 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	0 to 85	38C41
UCC38C41DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 85	38C41
UCC38C41DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 85	38C41
UCC38C41DRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 85	38C41
UCC38C42D	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 85	38C42
UCC38C42DGK	Active	Production	VSSOP (DGK) | 8	100 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	0 to 85	38C42
UCC38C42DGK.A	Active	Production	VSSOP (DGK) | 8	100 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	0 to 85	38C42
UCC38C42DGKR	NRND	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	Call TI | Nipdauag	Level-2-260C-1 YEAR	0 to 85	38C42
UCC38C42DGKR.A	NRND	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	0 to 85	38C42
UCC38C42DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 85	38C42
UCC38C42DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 85	38C42
UCC38C42DRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 85	38C42
UCC38C43D	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 85	38C43
UCC38C43DGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	-	Call TI	Level-2-260C-1 YEAR	0 to 85	(38C43, 3C43)
UCC38C43DGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	-	Call TI	Level-2-260C-1 YEAR	0 to 85	(38C43, 3C43)

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC38C43DGKRG4	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	-	Call TI	Level-2-260C-1 YEAR	0 to 85	(38C43, 3C43)
UCC38C43DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 85	38C43
UCC38C43DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 85	38C43
UCC38C43P	Obsolete	Production	PDIP (P) | 8	-	-	Call TI	Call TI	0 to 85	UCC38C43P
UCC38C44D	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 85	38C44
UCC38C44DGK	NRND	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	0 to 85	38C44
UCC38C44DGK.A	NRND	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	0 to 85	38C44
UCC38C44DGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	Call TI | Nipdauag	Level-2-260C-1 YEAR	0 to 85	38C44
UCC38C44DGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	0 to 85	38C44
UCC38C44DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 85	38C44
UCC38C44DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 85	38C44
UCC38C45DGK	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	0 to 85	38C45
UCC38C45DGK.A	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	0 to 85	38C45
UCC38C45DGKR	NRND	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	Call TI | Nipdauag	Level-2-260C-1 YEAR	0 to 85	38C45
UCC38C45DGKR.A	NRND	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	0 to 85	38C45
UCC38C45DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 85	38C45
UCC38C45DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 85	38C45

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF UCC28C40, UCC28C41, UCC28C42, UCC28C43, UCC28C44, UCC28C45 :

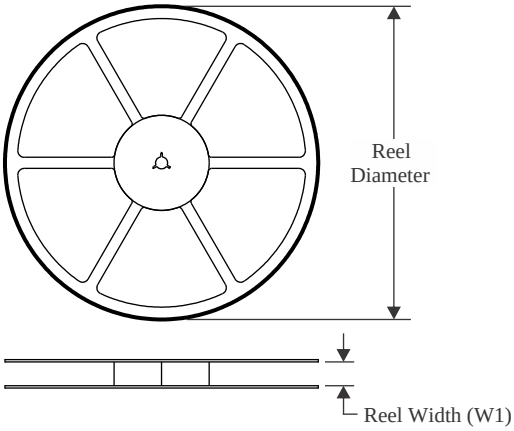
- Automotive : UCC28C40-Q1, UCC28C41-Q1, UCC28C42-Q1, UCC28C43-Q1, UCC28C44-Q1, UCC28C45-Q1
- Enhanced Product : UCC28C43-EP, UCC28C45-EP

NOTE: Qualified Version Definitions:

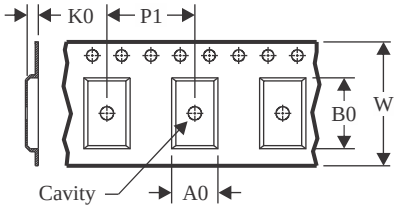
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

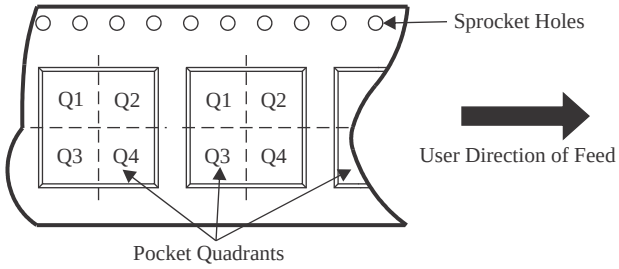


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

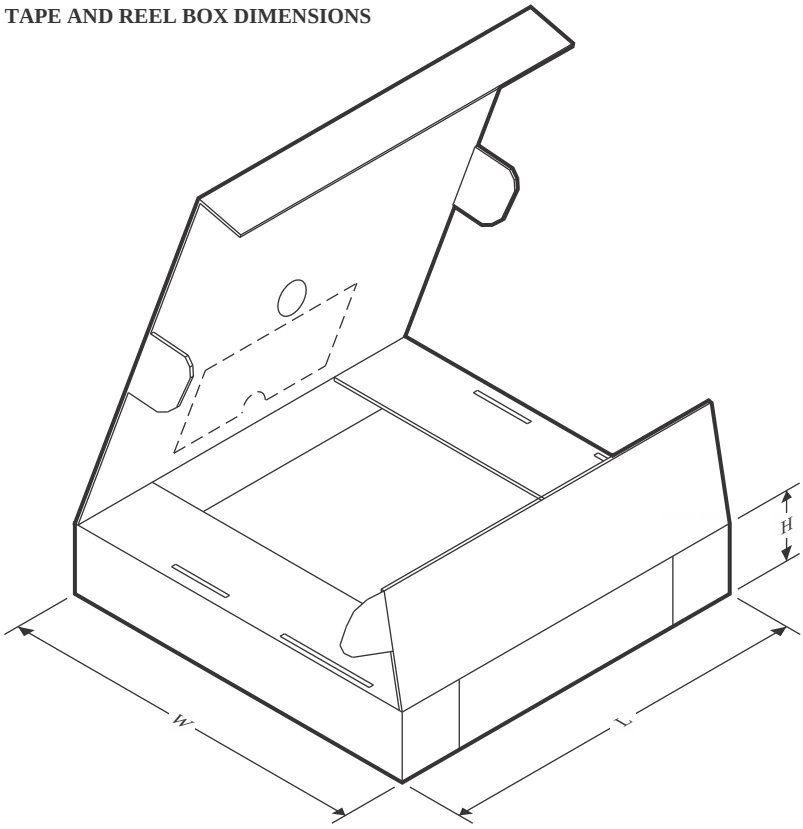


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC28C40DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC28C40DGKRG4	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC28C40DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC28C41DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC28C41DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC28C42DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC28C42DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC28C43DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC28C43DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC28C44DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC28C44DGKRG4	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC28C44DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC28C45DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC28C45DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC38C40DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC38C41DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC38C42DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC38C43DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC38C43DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC38C44DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC38C45DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

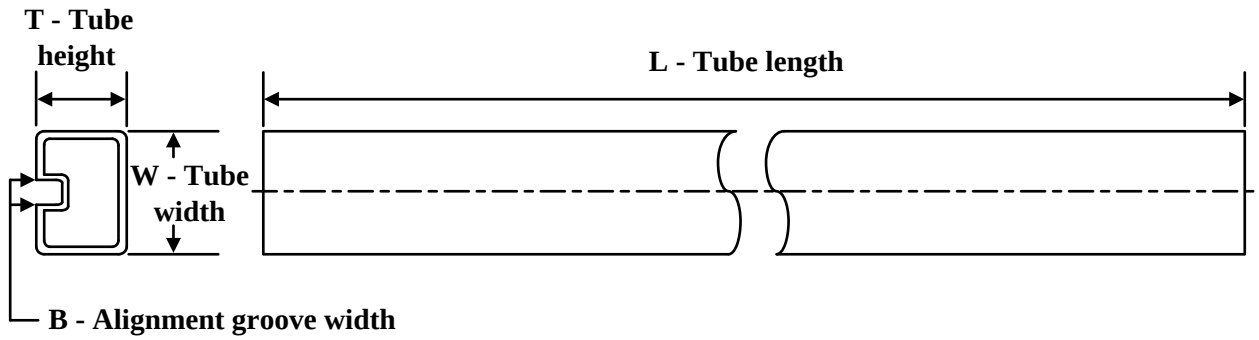


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC28C40DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
UCC28C40DGKRG4	VSSOP	DGK	8	2500	353.0	353.0	32.0
UCC28C40DR	SOIC	D	8	2500	353.0	353.0	32.0
UCC28C41DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
UCC28C41DR	SOIC	D	8	2500	353.0	353.0	32.0
UCC28C42DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
UCC28C42DR	SOIC	D	8	2500	353.0	353.0	32.0
UCC28C43DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
UCC28C43DR	SOIC	D	8	2500	353.0	353.0	32.0
UCC28C44DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
UCC28C44DGKRG4	VSSOP	DGK	8	2500	353.0	353.0	32.0
UCC28C44DR	SOIC	D	8	2500	353.0	353.0	32.0
UCC28C45DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
UCC28C45DR	SOIC	D	8	2500	353.0	353.0	32.0
UCC38C40DR	SOIC	D	8	2500	353.0	353.0	32.0
UCC38C41DR	SOIC	D	8	2500	353.0	353.0	32.0
UCC38C42DR	SOIC	D	8	2500	353.0	353.0	32.0
UCC38C43DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC38C43DR	SOIC	D	8	2500	353.0	353.0	32.0
UCC38C44DR	SOIC	D	8	2500	353.0	353.0	32.0
UCC38C45DR	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

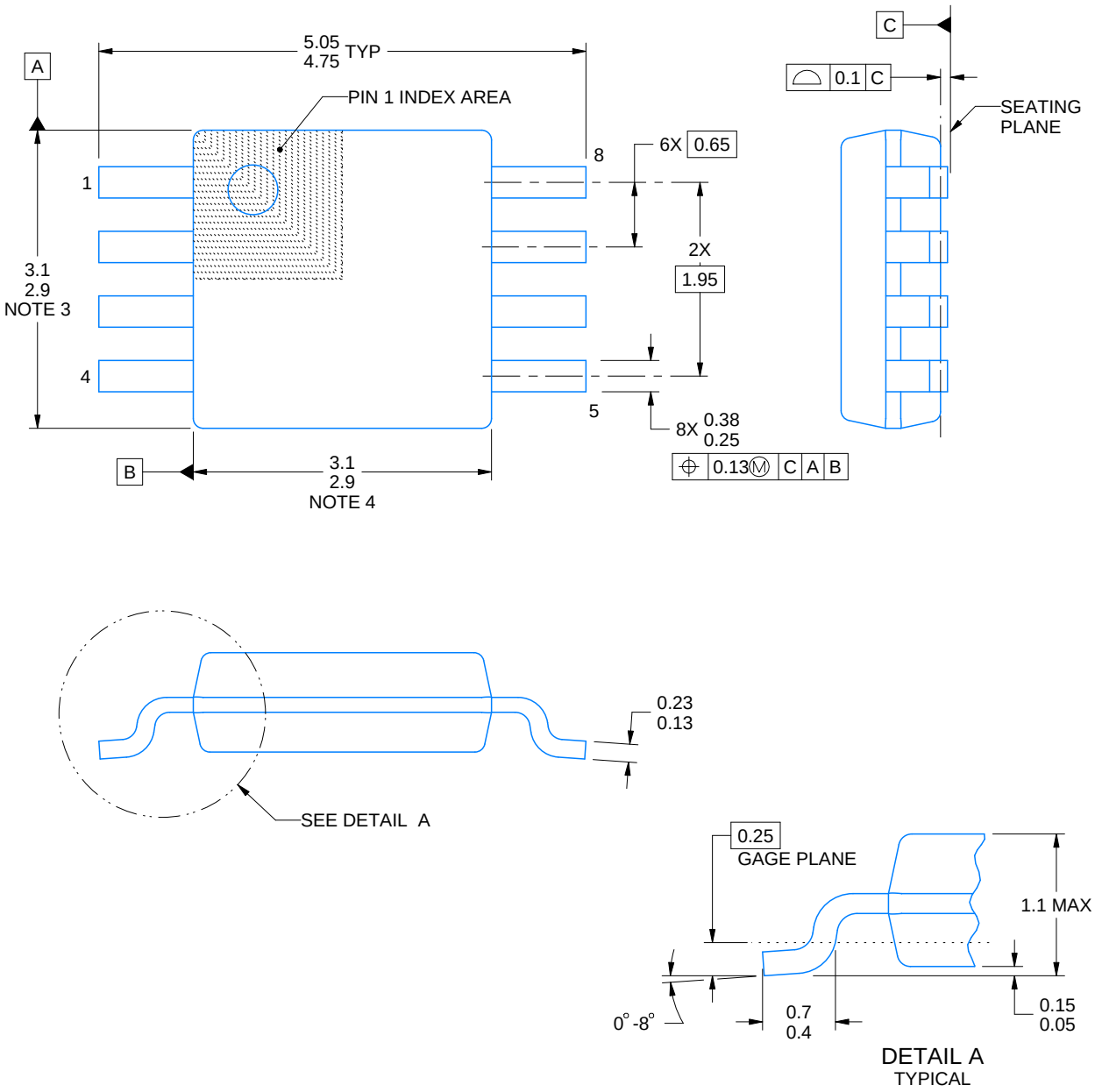
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UCC38C40DGK	DGK	VSSOP	8	80	330.2	6.6	3005	1.88
UCC38C40DGK.A	DGK	VSSOP	8	80	330.2	6.6	3005	1.88
UCC38C41DGK	DGK	VSSOP	8	100	330.2	6.6	3005	1.88
UCC38C41DGK.A	DGK	VSSOP	8	100	330.2	6.6	3005	1.88
UCC38C42DGK	DGK	VSSOP	8	100	330.2	6.6	3005	1.88
UCC38C42DGK.A	DGK	VSSOP	8	100	330.2	6.6	3005	1.88
UCC38C44DGK	DGK	VSSOP	8	80	330.2	6.6	3005	1.88
UCC38C44DGK.A	DGK	VSSOP	8	80	330.2	6.6	3005	1.88
UCC38C45DGK	DGK	VSSOP	8	80	330.2	6.6	3005	1.88
UCC38C45DGK	DGK	VSSOP	8	80	274	6.55	500	2.88
UCC38C45DGK.A	DGK	VSSOP	8	80	330.2	6.6	3005	1.88
UCC38C45DGK.A	DGK	VSSOP	8	80	274	6.55	500	2.88

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

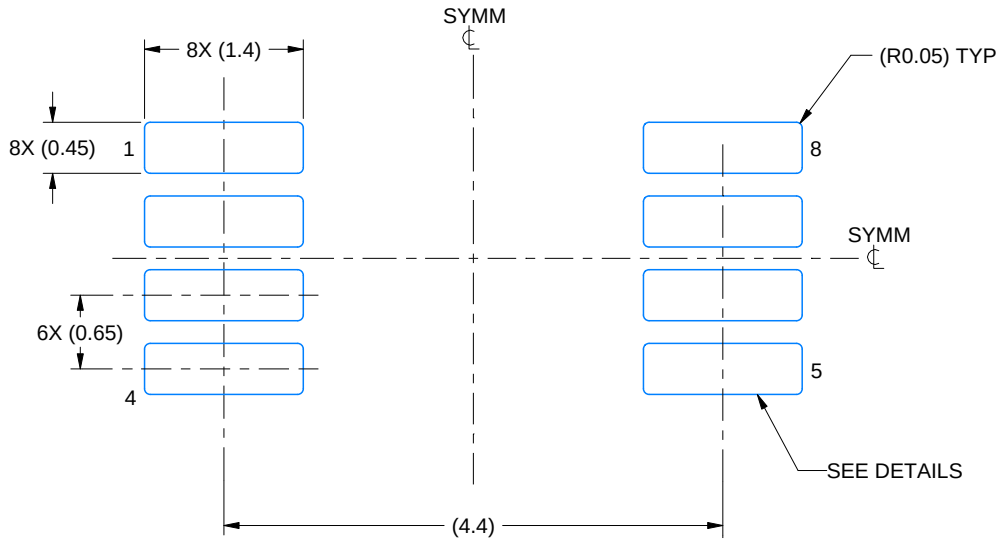
SMALL OUTLINE PACKAGE



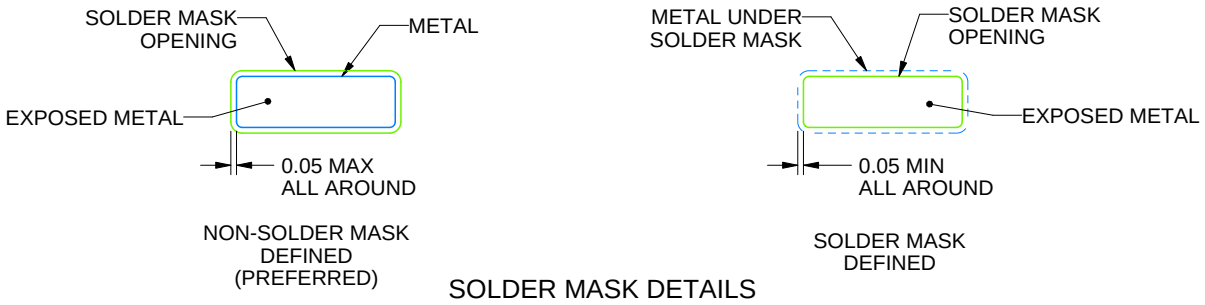
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

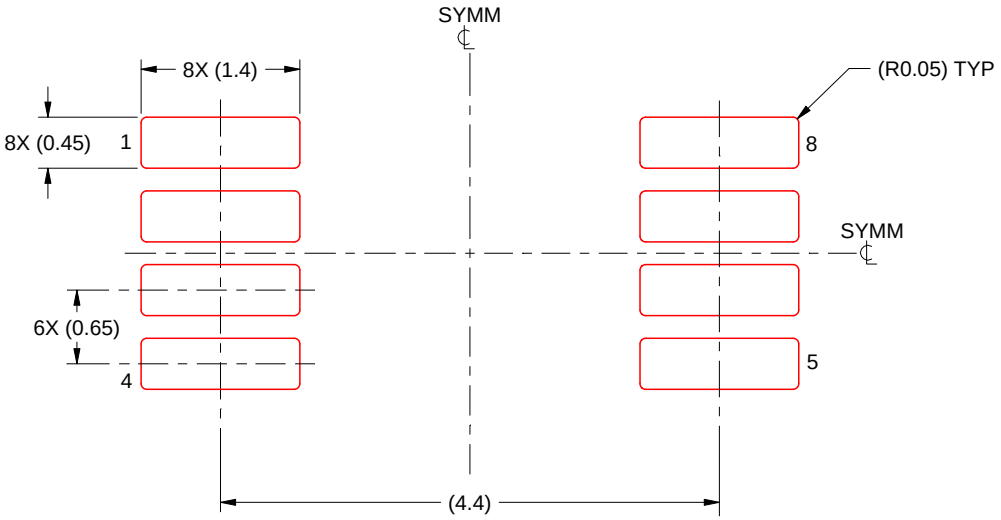


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

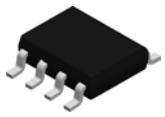


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

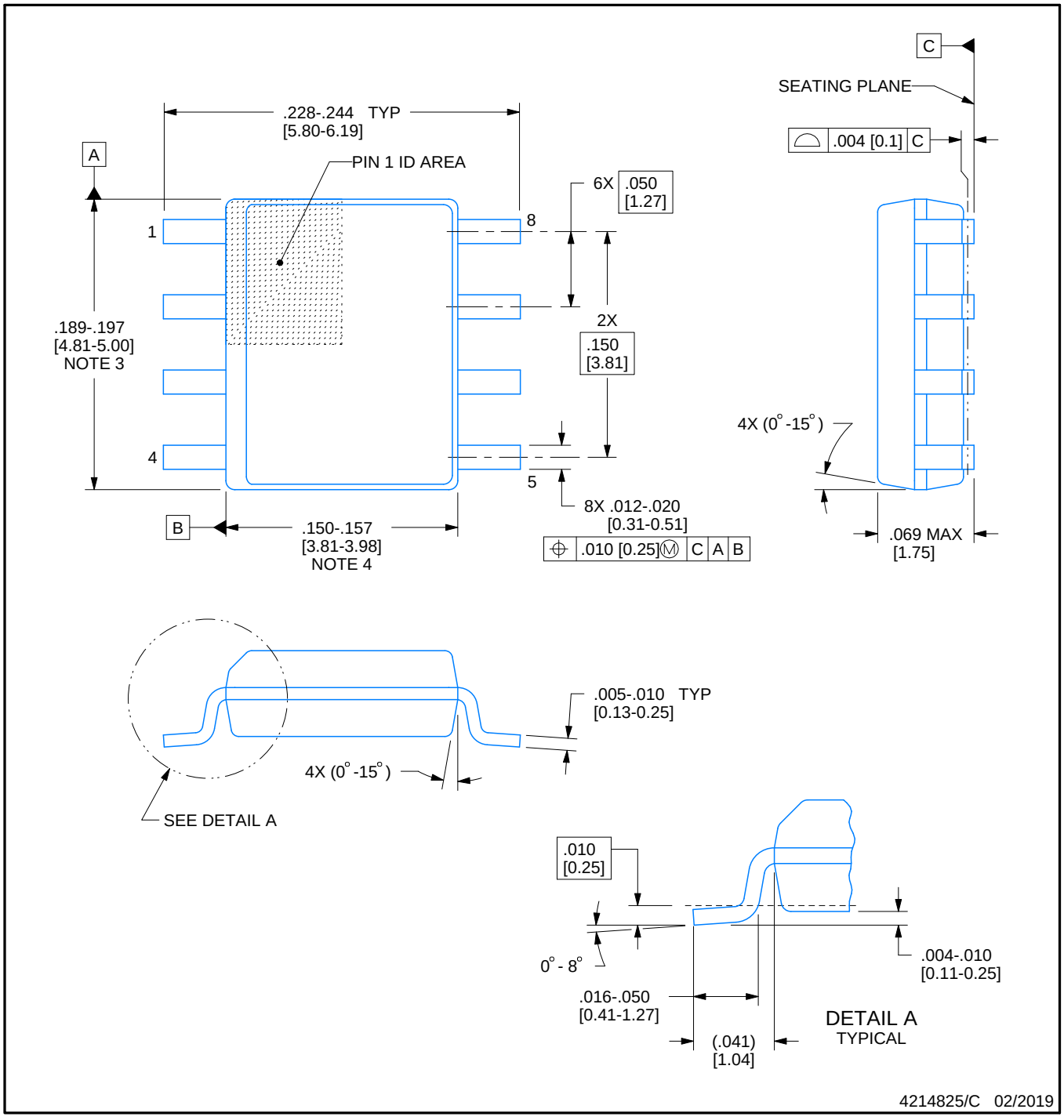


PACKAGE OUTLINE

D0008A

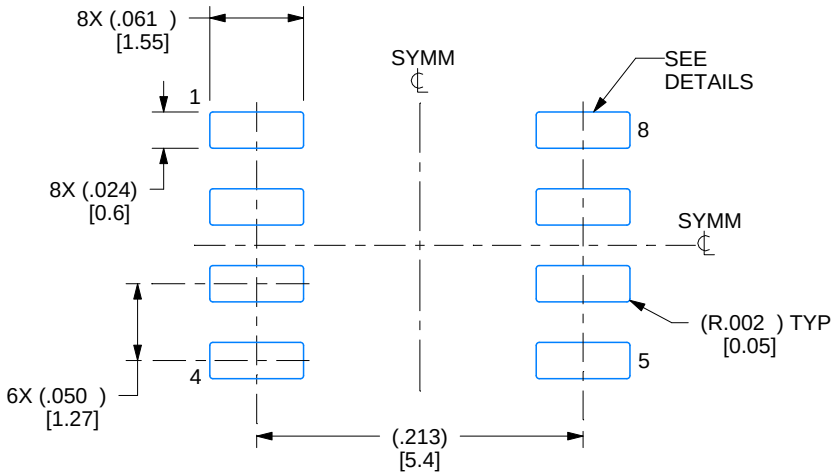
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

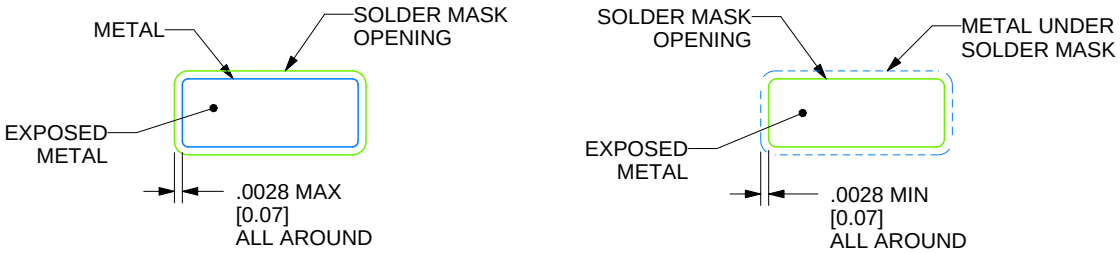


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

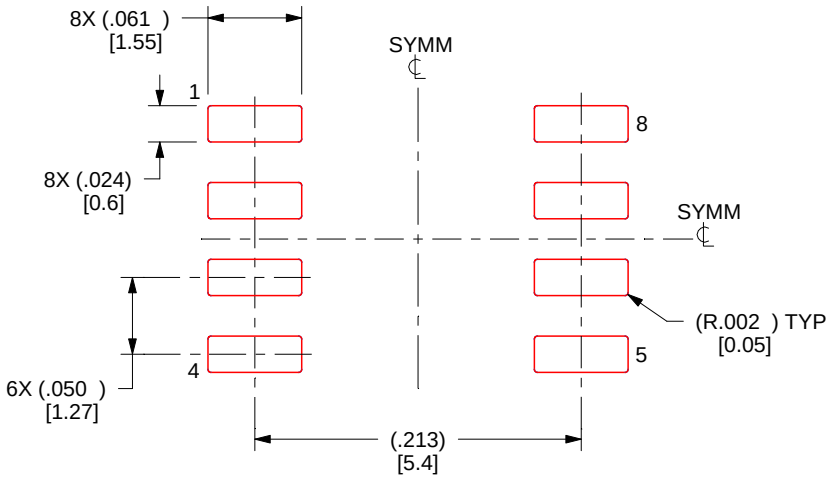
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



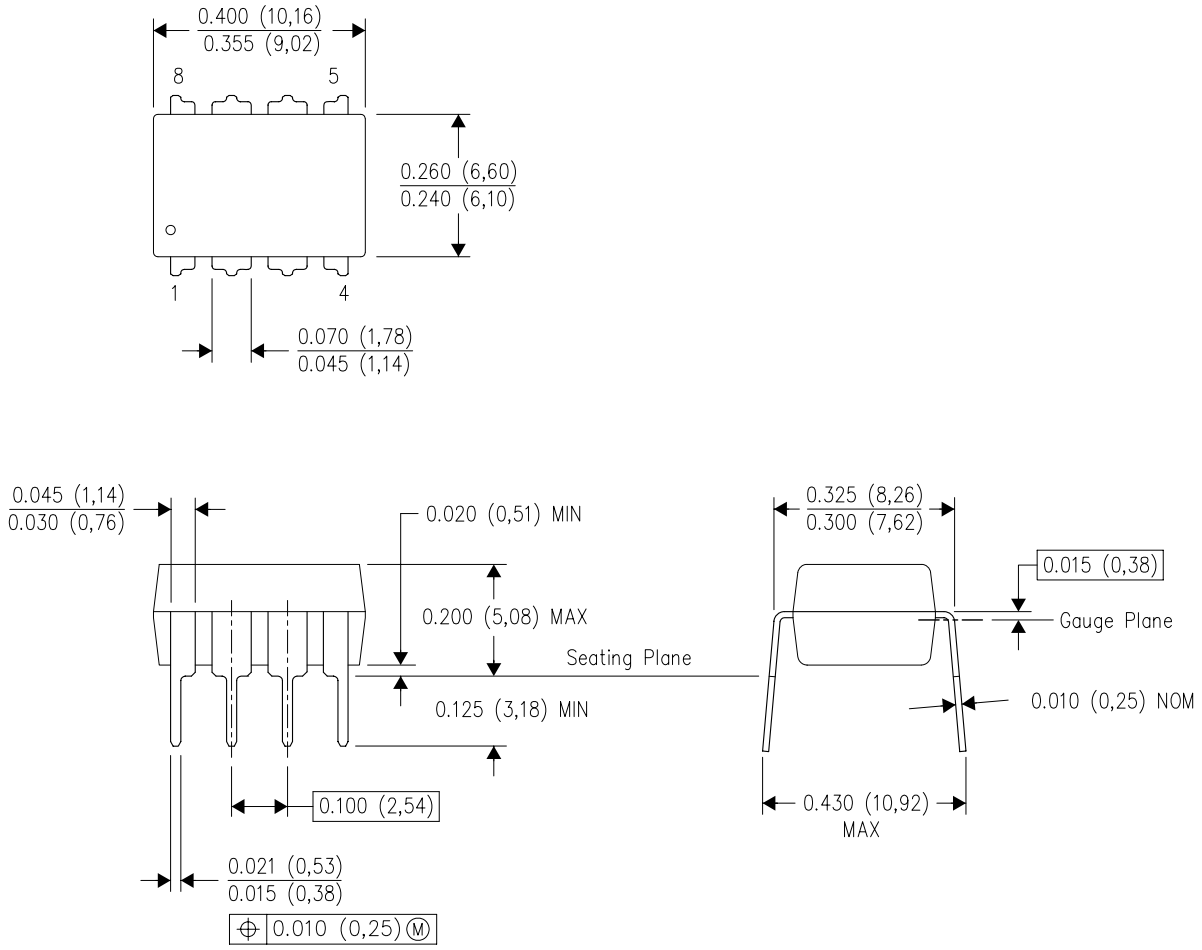
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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