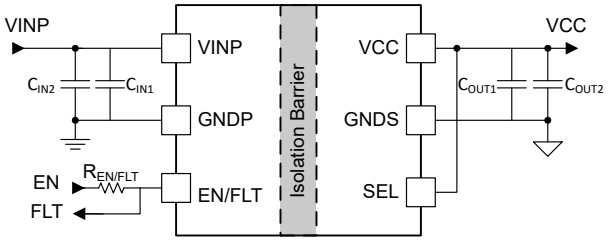
UCC33411-Q1 Ultra-Small, 1.0W, 3.3V, 5kV$_{RMS}$ Isolation, Automotive DC/DC Module

1 Features

- Maximum output power; 1.0W
- Input voltage operation range: 4.5V to 5.5V
- Regulated selectable output voltage: 3.3V, 3.7V
  - Available load current: 3.3V: 300mA
- Typical load regulation: 0.5%
- Typical line regulation: 4mV/V
- Robust isolation barrier:
  - Isolation rating: 5kV$_{RMS}$
  - Surge capability: 10.4kV$_{PK}$
  - Working voltage: 1700V$_{PK}$
  - ± 8KV IEC 61000-4-2 contact discharge protection across isolation barrier
  - 250V/ns common mode transient immunity
- Power dense isolated DC/DC module with integrated transformer technology
- Adaptive spread spectrum modulation (SSM)
- Meets CISPR-32 Class B emission
- Meets CISPR-25 Class 5 emission
- Strong magnetic field immunity
- Overload and short circuit protection
- Thermal shutdown
- Low inrush current soft-start
- Enable pin with fault reporting mechanism
- AEC-Q100 qualified with the following results:
  - Device temperature Grade 1: –40°C to 125°C ambient operating temperature
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- SSOP-16 (5.85mm × 7.50mm) package
- >8.2mm clearance and creepage

2 Applications

- HEV/EV Onboard charger
- HEV/EV Traction inverter
- HEV/EV Charging inlet control
- Bias power for isolated measurements
- Bias power for isolated signal chain
- Bias power for RS-485, RS-422, and CAN interfaces



Simplified Application

3 Description

The UCC33411-Q1 is an automotive qualified DC/DC power module with integrated transformer technology designed to provide 1.0W of isolated output power. It can support an input voltage operation range from 4.5V to 5.5V and regulate 3.3V output voltage with a selectable headroom of 3.7V.

The UCC33411-Q1 features a proprietary transformer architecture that achieves a 5kV$_{RMS}$ isolation withstand voltage, while simultaneously supporting low electro-magnetic interference (EMI) and excellent load regulation.

The UCC33411-Q1 integrates protection features for increased system robustness such as enable pin with fault reporting mechanism, short circuit protection and thermal shutdown.

The UCC33411-Q1 comes in a miniaturized, low-profile SSOP (5.85mm × 7.50mm) package with 2.65mm height and > 8.2mm clearance and creepage.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
UCC33411-Q1	DHA SSOP 16	5.85mm × 7.50mm

(1) For all available packages, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Device Comparison

Table 4-1. Device Comparison Table

DEVICE NAME	V_{VIN} RANGE	OUTPUT (VCC)	TYPICAL POWER	ISOLATION RATING
UCC33420-Q1	4.5V to 5.5V	5.0V / 5.5V	1.5W	Basic
UCC33420	4.5V to 5.5V	5.0V / 5.5V	1.5W	Basic
UCC33020-Q1	3.0V to 5.5V	5.0V / 5.5V	1.0W	Basic
UCC33410-Q1	4.5V to 5.5V	3.3V / 3.7V	1.0W	Basic
UCC33410	4.5V to 5.5V	3.3V / 3.7V	1.0W	Basic
UCC33421-Q1	4.5V to 5.5V	5.0V / 5.5V	1.5W	Reinforced
UCC33411-Q1	4.5V to 5.5V	3.3V / 3.7V	1.0W	Reinforced

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5 Pin Configuration and Functions

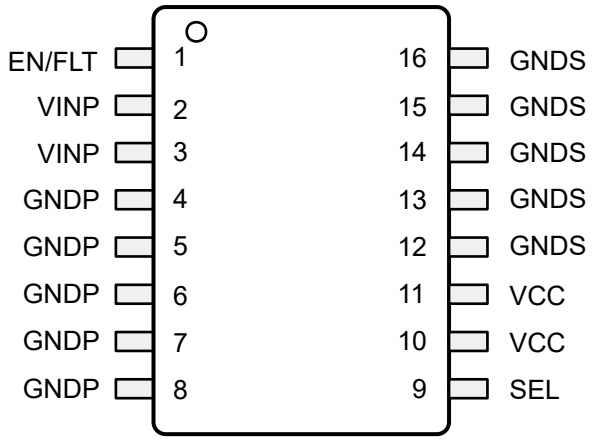

Figure 5-1. DHA SSOP 16-Pin Package (top view)

Table 5-1. Pin Functions

PIN		TYPE (1)	DESCRIPTION
NAME	NO.		
EN/FLT	1	I/O	Multi-function Enable input pin and fault output pin. Connect to microcontroller through an 18kΩ or greater pull-up resistor. Enable input pin: Forcing EN low disables the device. Pull high to enable normal device functionality. Fault output pin: This pin is pulled low for t_{Fault} to alert the system that power converter is shutdown due to fault conditions.
VINP	2	P	Primary side input supply voltage pin. 15nF (C_{IN1}) and 10µF (C_{IN2}) ceramic bypass capacitors placed close to device pins are required between VINP and GNDP pins
	3		
GNDP	4	G	Power ground return connection for VINP.
	5		
	6		
	7		
	8		
SEL	9	I	VCC selection pin. VCC setpoint is 3.3V when SEL is connected to VCC, and 3.7V when SEL is shorted to GNDS
VCC	10	P	Isolated supply output voltage pin. 15nF (C_{OUT1}) and 22µF (C_{OUT2}) ceramic bypass capacitors placed close to device pins are required between VCC and GNDS pins
	11		
GNDS	12	G	Power ground return connection for VCC.
	13		
	14		
	15		
	16		

(1) P = Power, G = Ground, I = Input, O = Output, I/O = bidirectional

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

PIN	MIN	TYP	MAX	UNIT
VINP to GNDP	–0.3		6	V
EN/FLT to GNDP	–0.3		6	V
VCC to GNDS	–0.3		6	V
SEL to GNDS	–0.3		6	V
Total VCC output power at T_A=25°C, VINP = 4.5V, VCC = 3.3V, $P_{OUT_VCC_MAX}$			1.6	W
Total VCC output power at T_A=25°C, VINP = 5.5V, VCC = 3.3V, $P_{OUT_VCC_MAX}$			1.9	W
VCC maximum current sink capability			30	mA
Operating junction temperature range, T_J	–40		150	°C
Storage temperature, T_{stg}	–65		150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011 Section 7.2	±750	V
		Contact discharge per IEC 61000-4-2; Isolation barrier withstand test (2)	±8000	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification
(2) IEC ESD strike is applied across the barrier with all pins on each side tied together creating a two-terminal device

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PIN		MIN	TYP	MAX	UNIT
V_{VINP}	Primary-side input voltage to GNDP	4.5		5.5	V
$V_{EN/FLT}$	EN/FLT pin voltage to GNDP	0		5.5	V
V_{VCC}	Secondary-side Isolated output voltage to GNDS	0		3.9	V
V_{SEL}	SEL pin input voltage to GNDS	0		3.9	V
P_{VCC}	VCC output power at VINP=5.0V±10%, VCC = 3.3V, T_A=25°C - 85°C (1)		1		W
P_{VCC}	VCC output power at VINP=5.0V±10%, VCC = 3.3V, T_A=105°C (1)		0.7		W
P_{VCC}	VCC output power at VINP=5.0V±10%, VCC = 3.3V, T_A=125°C (1)		0.4		W
Static CMTI	Static Common mode transient immunity rating (dV/dt rate across the isolation barrier)			250	V/ns
Dynamic CMTI	Dynamic Common mode transient immunity rating (dV/dt rate across the isolation barrier)			250	V/ns
T_A	Ambient temperature	–40		125	℃

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6.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

PIN		MIN	TYP	MAX	UNIT
T_J	Junction temperature	–40		150	℃

(1) See the VCC Load Recommended Operating Area section for maximum rated values across temperature and VINP conditions for different VCC output voltage settings.

6.4 Thermal Information

THERMAL METRIC(1)		DHA SOIC 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	61.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	5.88	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.2	°C/W
Ψ_{JA}	Junction-to-ambient characterization parameter	59.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	5.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	23.6	°C/W

(1) The thermal resistances (R) are based on JEDEC board, and the characterization parameters (Ψ) are based on the EVM described in the Layout section. For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

6.5 Power Ratings

V_{VINP} = 5.0V, C_{IN1} = C_{OUT1} = 15nF, C_{IN2} = 10µF, C_{OUT2} = 22µF SEL connected to VCC, $V_{EN/FLT}$ = 5.0V, T_A = 25°C.

PARAMETER		TEST CONDITIONS	VALUE	UNIT
P_D	Power dissipation	I_{VCC} = 300 mA	920	mW
P_{DP}	Power dissipation by driver side (primary)	I_{VCC} = 300 mA	360	mW
P_{DS}	Power dissipation by rectifier side (secondary)	I_{VCC} = 300 mA	250	mW
P_{DT}	Power dissipation by transformer	I_{VCC} = 300 mA	310	mW

6.6 Insulation Specifications

Parameter		TEST CONDITIONS	VALUE	UNIT
General				
CLR	External clearance (1)	Shortest terminal-to-terminal distance through air	> 8.2	mm
CPG	External creepage (1)	Shortest terminal-to-terminal distance across the package surface	> 8.2	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	> 70	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category	Rated mains voltage ≤ 300V_{RMS}	I-IV	
	Overvoltage category	Rated mains voltage ≤ 600V_{RMS}	I-IV	
	Overvoltage category	Rated mains voltage ≤ 1000V_{RMS}	I-III	
DIN EN IEC60747-17 (VDE 0884-17) (2)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1700	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage (sine wave) Time dependent dielectric breakdown (TDDB) test	1202	V_{RMS}
		DC voltage	1700	V_{DC}

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6.6 Insulation Specifications (continued)

Parameter		TEST CONDITIONS	VALUE	UNIT
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60s (qualification)	7071	V_{PK}
		$V_{TEST} = 1.2 \times V_{IOTM}$, t = 1s (100%) production	8485	V_{PK}
V_{IMP}	Impulse Voltage (3)	Tested in air, 1.2/50µs waveform per IEC 62368-1	8000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage (4)	Tested in oil (qualification test), 1.2/50µs waveform per IEC 62368-1.	10400	V_{PK}
q_{pd}	Apparent charge (5)	Method a: After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10s	≤ 5	pC
q_{pd}	Apparent charge (5)	Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10s	≤ 5	pC
q_{pd}	Apparent charge (5)	Method b1: At routine test (100% production) and preconditioning (type test), $V_{ini} = V_{IOTM}$, t_{ini} = 1s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1s	≤ 5	pC
C_{IO}	Barrier capacitance, input to output (6)	V_{IO} = 0.4 sin (2πft), f = 1MHz	< 3	pF
R_{IO}	Isolation resistance, input to output (6)	V_{IO} = 500V, T_A = 25°C	> 10^{12}	Ω
R_{IO}	Isolation resistance, input to output (6)	V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	> 10^{11}	Ω
R_{IO}	Isolation resistance, input to output (6)	V_{IO} = 500V at T_S = 150°C	> 10^{9}	Ω
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	Withstand isolation voltage $V_{TEST} = V_{ISO}$, t = 60s (qualification) $V_{TEST} = 1.2 \times V_{ISO}$, t=1s (100% production)	5000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed-circuit board are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air to determine the surge immunity of the package.
(4) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier
(5) Apparent charge is electrical discharge caused by a partial discharge (pd).
(6) All pins on each side of the barrier tied together creating a two-terminal device

6.7 Safety Limiting Values

Safety Limiting (1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to over-heat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MAX	UNIT
P_S	Safety power dissipation (input power - output power)	$R_{θJA}$ = 61.1 °C/W, T_J = 150 °C, T_A = 25 °C	2.05	W
T_S	Safety temperature		150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and PS should not be exceeded. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{θJA}$, in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{qJA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{θJA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.

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$P_S = I_S \times V_{VINP}$, where V_{VINP} is the maximum input voltage.

6.8 Electrical Characteristics

Over operating temperature range (T_J = –40°C to 150°C), VINP = 5.0V, $C_{IN1} = C_{OUT1}$ = 15 nF, C_{IN2} = 10 µF, C_{OUT2} = 22 µF SEL connected to VCC, EN/FLT = 5.0V unless otherwise noted. All typical values at VINP=5.0V, T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY (Primary-side. All voltages with respect to GNDP)						
I_{VINP_Q}	VIN quiescent current,disabled	EN/FLT=Low, VINP=5.0V, no load			180	uA
I_{VINP_NL}	VIN operating current, no load	EN/FLT=High; VINP=4.5V-5.5V; VCC=3.3V no load		5	10	mA
		EN/FLT=High; VINP=4.5V-5.5V; VCC=3.7V no load		5	10	mA
I_{VINP_FL}	VIN operating current, full load	EN/FLT=High; VINP=5.0V; VCC=3.3V, I_{out}=300mA, T_A=25°C	375	395	412	mA
I_{VINP_SC}	DC current from VINP supply under short circuit on VCC	EN/FLT=High; VINP=5.0V; VCC=0V, T_A=25°C (1)		45		mA
UVLOP COMPARATOR (Primary-side. All voltages with respect to GNDP)						
$V_{VINP_UVLO_R}$	VINP under-voltage lockout rising threshold			2.8	2.9	V
$V_{VINP_UVLO_F}$	VINP under-voltage lockout falling threshold		2.6	2.7		V
V_{UVLO_H}	VINP under-voltage lockout hysteresis			0.1		V
OVLO COMPARATOR (Primary-side. All voltages with respect to GNDP)						
$V_{VINP_OVLO_R}$	VINP over-voltage lockout rising threshold			5.77	5.9	V
$V_{VINP_OVLO_F}$	VINP over-voltage lockout falling threshold		5.55	5.72		V
V_{VINP_H}	VINP over-voltage lockout hysteresis			0.05		V
Switching Charactarestics						
f_{Sw}	DC-DC Converter switching frequency			64.5		MHz
PRIMARY SIDE THERMAL SHUTDOWN						
TSD_{P_R}	Primary-side over-temperature shutdown rising threshold		150	165		ºC
TSD_{P_F}	Primary-side over-temperature shutdown falling threshold		130			ºC
TSD_{P_H}	Primary-side over-temperature shutdown hysteresis			20		ºC
$t_{TSHUTP_DEGLITCH_D}$	over-temperature shutdown digital deglitch time.			64		us
EN/FLT PIN						
V_{EN_R}	Enable voltage rising threshold	EN/FLT = 0V to 5.0V			2.1	V
V_{EN_F}	Enable voltage falling threshold	EN/FLT = 5.0V to 0V	0.8			V
I_{EN}	Enable Pin Input Current	EN/FLT = 5.0V			10	uA
I_{FLT}	Fault pin sink current when fault occurs	EN/FLT > 0.5V	0.375			mA
V_{FLT}	EN/FLT pin voltage when faults occur	With a minimum 18kΩ (10% tolerance) resistor connected to EN/FLT pin			0.5	V
t_{Fault}	EN/FLT pull down interval when faults occur	EN/FLT > 0.5V , Fault occur		200		us
PRIMARY-SIDE Soft-Start						
$t_{SOFT_START_TIME_OUT}$	soft-start time-out	Timer is reset and started when (VIN>UVLO_P and EN = High).		16		ms

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6.8 Electrical Characteristics (continued)

Over operating temperature range (T_J = –40°C to 150°C), VINP = 5.0V, C_{IN1} = C_{OUT1} = 15 nF, C_{IN2} = 10 µF, C_{OUT2} = 22 µF SEL connected to VCC, EN/FLT = 5.0V unless otherwise noted. All typical values at VINP=5.0V, T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON-MAX}	Maximum Ton primary side will limit to regardless PSON			13		us
$t_{OFF-MIN}$	Minimum Toff during overpower protection			1.5		us
VCC OUTPUT VOLTAGE (Secondary-side. All voltages with respect to GNDS)						
V_{CC}	Isolated supply regulated output voltage	VINP = 5.0V, SEL = VCC, I_{out} = 0 - 300mA	3.2	3.3	3.4	V
		VINP = 5.0V, SEL = GNDS, I_{out} = 0 - 270mA	3.59	3.7	3.81	V
	Isolated supply regulated output voltage accuracy	VINP = 4.5V - 5.5V; VCC = 3.3V / 3.7V	-4		4	%
V_{CC_Line}	V_{cc} DC line regulation	VINP = 4.5V - 5.5V; VCC = 3.3V, I_{out} = 150mA		2	12	mV/V
		VINP = 4.5V - 5.5V; VCC = 3.7V, I_{out} = 150mA		2	12	mV/V
V_{CC_Load}	V_{cc} DC load regulation	VINP = 5.0V; VCC = 3.3V, I_{out} = 0 - 300mA		0.5		%
		VINP = 5.0V; VCC = 3.7V, I_{out} = 0 - 270mA		0.5		%
V_{CC_Ripple}	Voltage ripple on isolated supply output	20-MHz bandwidth, VINP = 5.0V , VCC = 3.3V, I_{out} = 300mA, T_A=25°C(1)		50	75	mV
EFF	Efficiency P_{VCC} to P_{VINP}	VINP = 5.0V, VCC = 3.3V, I_{out} = 300mA, T_A = 25°C		51		%
V_{CC_Rise}	VCC rise time from 10% - 90%	VINP = 5.0V, VCC = 3.3V, T_A = 25°C, I_{out} = 70mA (1)		450	600	us
		VINP = 5.0V, VCC = 3.7V, T_A = 25°C, I_{out} = 70mA (1)		450	650	us
UVLO_S COMPARATOR (Secondary-side. All voltages with respect to GNDS)						
V_{VCC_UVLO}	VCC under-voltage lockout threshold			2.4		V
VCC UVP UNDER -VOLTAGE PROTECTION (Secondary-side. All voltages with respect to GNDS)						
K_{VCC_UVP}	VCC under-voltage protection threshold ratio	VCC= 3.3V, VUVP = VCC * 90%		90		%
V_{UVP_H}	VCC under-voltage protection hysteresis	VCC =3.3V	52	66	90	mV
V_{UVP_H}	VCC under-voltage protection hysteresis	VCC =3.7V	68	93	112	mV
VCC OVP OVER -VOLTAGE PROTECTION (Secondary-side. All voltages with respect to GNDS)						
$V_{VCC_OVP_R}$	VCC over-voltage protection rising threshold	VCC = 3.3V		3.75	3.8	V
$V_{VCC_OVP_H}$	VCC over-voltage protection hysteresis	VCC = 3.3V		0.1		V
$V_{VCC_OVP_R}$	VCC over-voltage protection rising threshold	VCC = 3.7V		4.2	4.25	V
$V_{VCC_OVP_H}$	VCC over-voltage protection hysteresis	VCC = 3.7V		0.1		V
SECONDARY SIDE THERMAL SHUTDOWN						
TSD_{S_R}	Secondary-side over-temperature shutdown rising threshold		150	165		ºC
TSD_{S_F}	Secondary-side over-temperature shutdown falling threshold		130			ºC
TSD_{S_H}	Secondary-side over-temperature shutdown hysteresis			20		ºC

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6.8 Electrical Characteristics (continued)

Over operating temperature range (T_J = –40°C to 150°C), VINP = 5.0V, C_{IN1} = C_{OUT1} = 15 nF, C_{IN2} = 10 µF, C_{OUT2} = 22 µF SEL connected to VCC, EN/FLT = 5.0V unless otherwise noted. All typical values at VINP=5.0V, T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AUTO_RESTART						
$t_{RESTART}$	Primary-side auto-restart time	After secondary-side faults assert or soft-start time-out expires		155		ms

(1) Specified by design. Not production tested

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6.9 Insulation Characteristics Curves

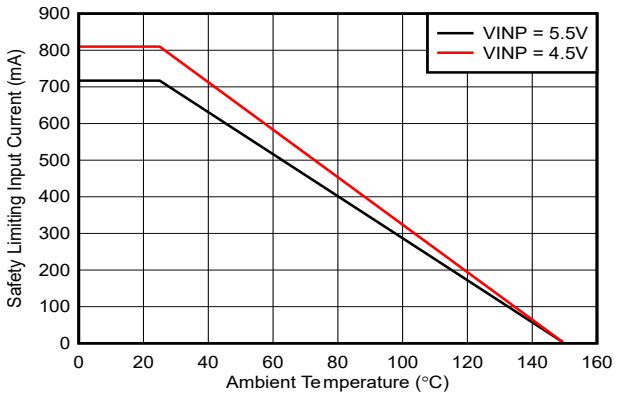

Figure 6-1. Thermal Derating Curve for Safety Related Limiting Current

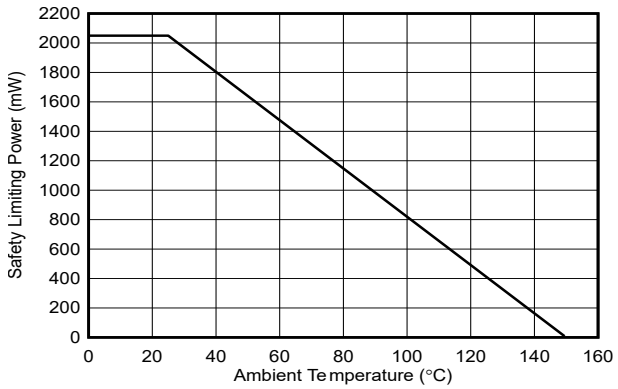

Figure 6-2. Thermal Derating Curve for Safety Related Limiting Power

6.10 Typical Characteristics

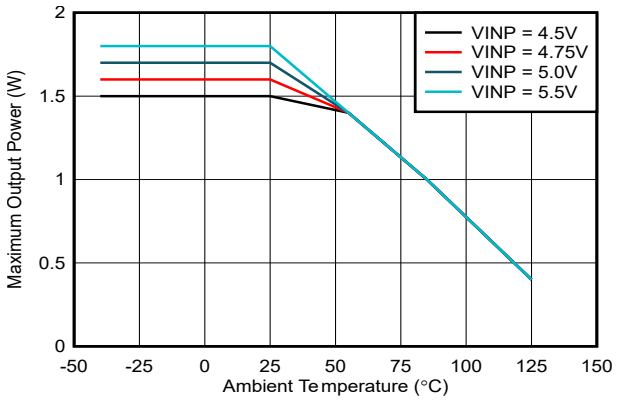

Figure 6-3. Maximum Output Power vs Ambient Temperature : VCC = 3.30V, C_{OUT2} = 22µF

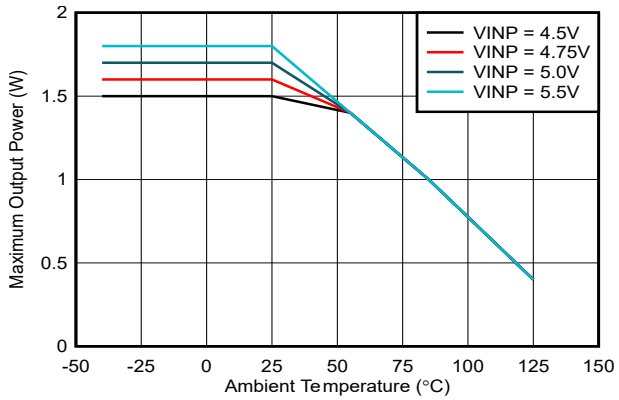

Figure 6-4. Maximum Output Power vs Ambient Temperature : VCC = 3.7V, C_{OUT2} = 22µF

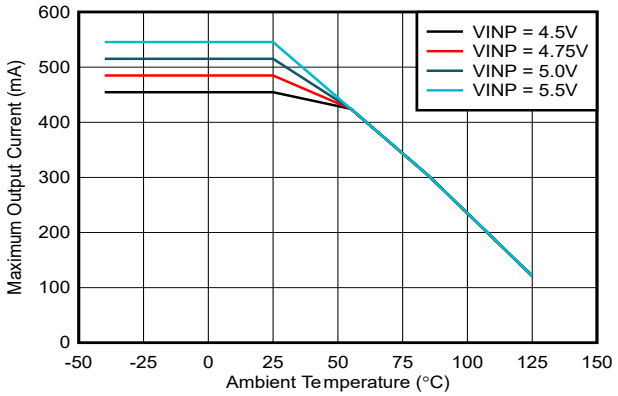

Figure 6-5. Maximum Output Current vs Ambient Temperature : VCC = 3.3V, C_{OUT2} = 22µF

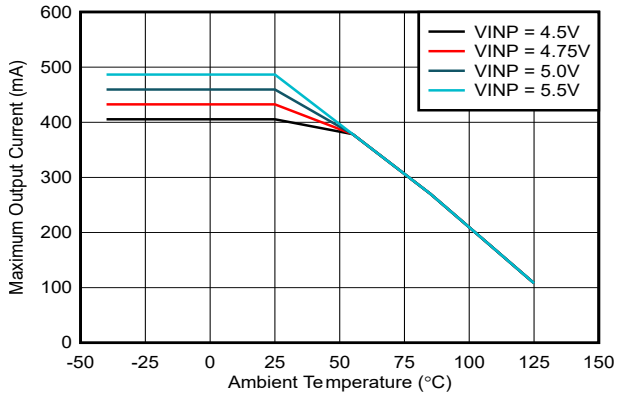

Figure 6-6. Maximum Output Current vs Ambient Temperature : VCC = 3.7V, C_{OUT2} = 22µF

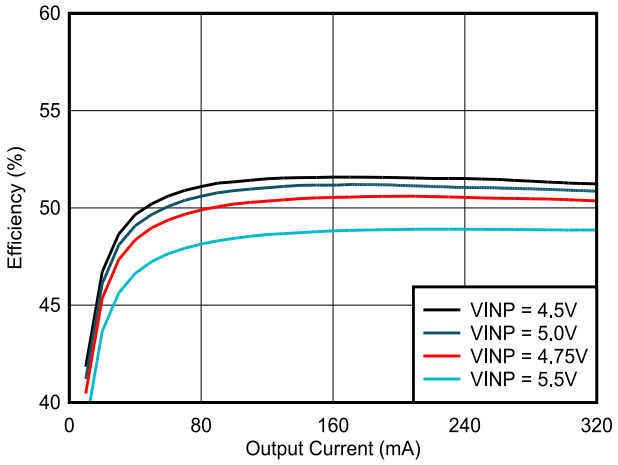

Figure 6-7. Efficiency vs Load Current (I_{VCC}): VCC = 3.3V, T_A = 25°C, C_{OUT2} = 22µF

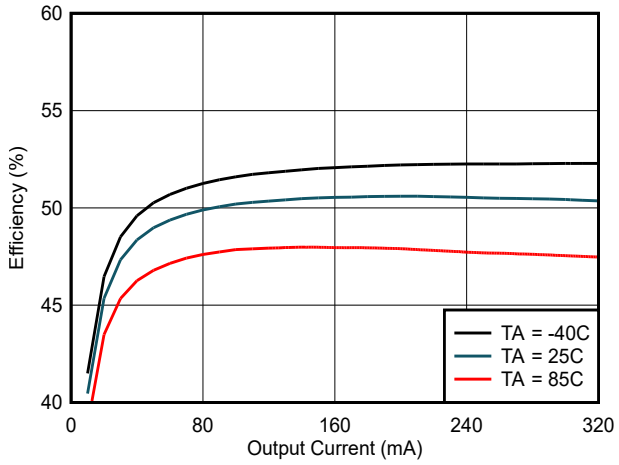

Figure 6-8. Efficiency vs Load Current (I_{VCC}): VCC = 3.3V, VINP = 5.0V, C_{OUT2} = 22µF

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6.10 Typical Characteristics (continued)

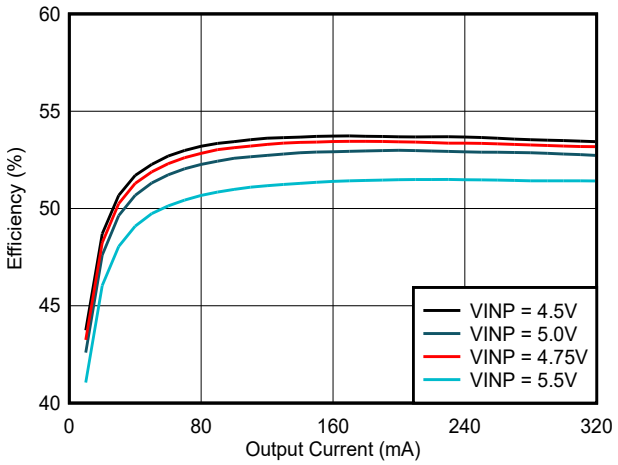

Figure 6-9. Efficiency vs Load Current (I_{VCC}): VCC = 3.7V, T_A = 25°C, C_{OUT2} = 22µF

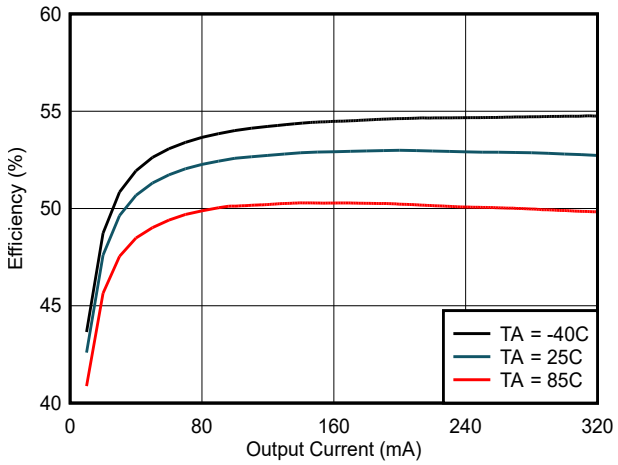

Figure 6-10. Efficiency vs Load Current (I_{VCC}): VCC = 3.7V, VINP = 5.0V, C_{OUT2} = 22µF

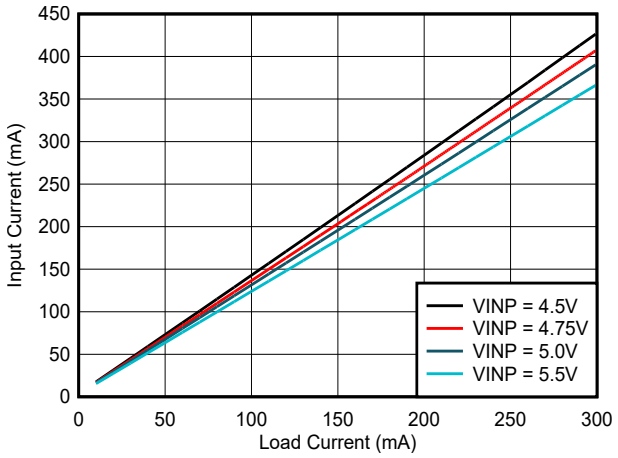

Figure 6-11. Input Current (I_{VINP}) vs Load Current (I_{VCC}): VCC = 3.3V, T_A = 25°C, C_{OUT2} = 22µF

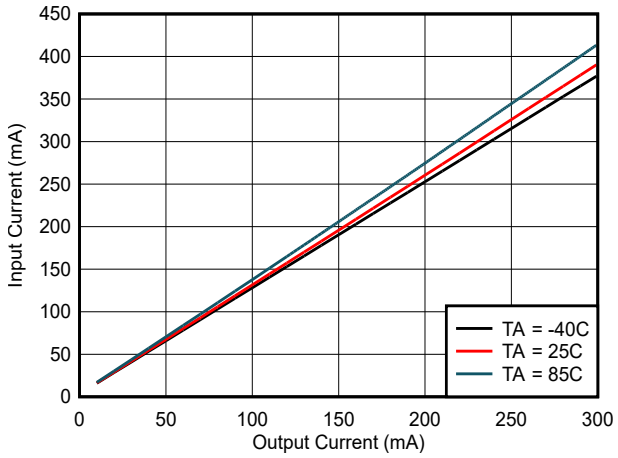

Figure 6-12. Input Current (I_{VINP}) vs Load Current (I_{VCC}): VCC = 3.3V, VINP = 5.0V, C_{OUT2} = 22µF

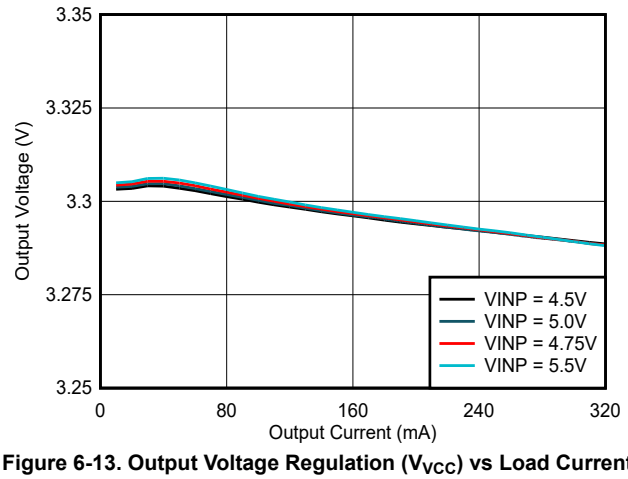

Figure 6-13. Output Voltage Regulation (V_{VCC}) vs Load Current (I_{VCC}): VCC = 3.3V, T_A = 25°C, C_{OUT2} = 22µF

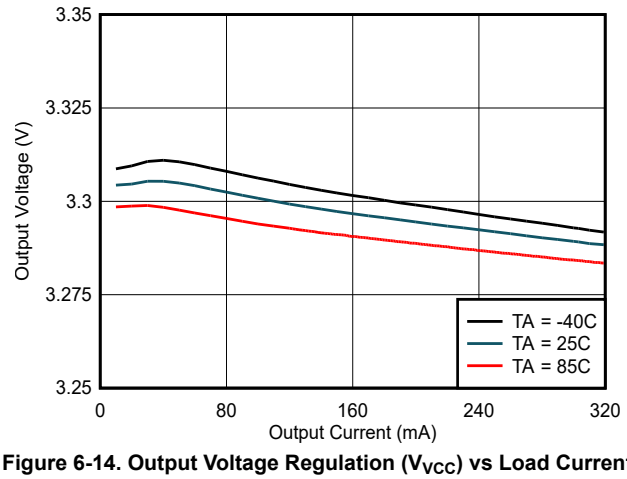

Figure 6-14. Output Voltage Regulation (V_{VCC}) vs Load Current (I_{VCC}): VCC = 3.3V, VINP = 5.0V, C_{OUT2} = 22µF

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7 Detailed Description

7.1 Overview

The UCC33411-Q1 device integrates a high-efficiency, low-emissions isolated DC/DC converter. Requiring minimum passive components to form a completely functional DC/DC power module, the device can deliver a maximum power of 1.0W across a $5kV_{RMS}$ reinforced isolation barrier over a wide range of operating temperatures in a low profile, high power density SSOP-16-pin package.

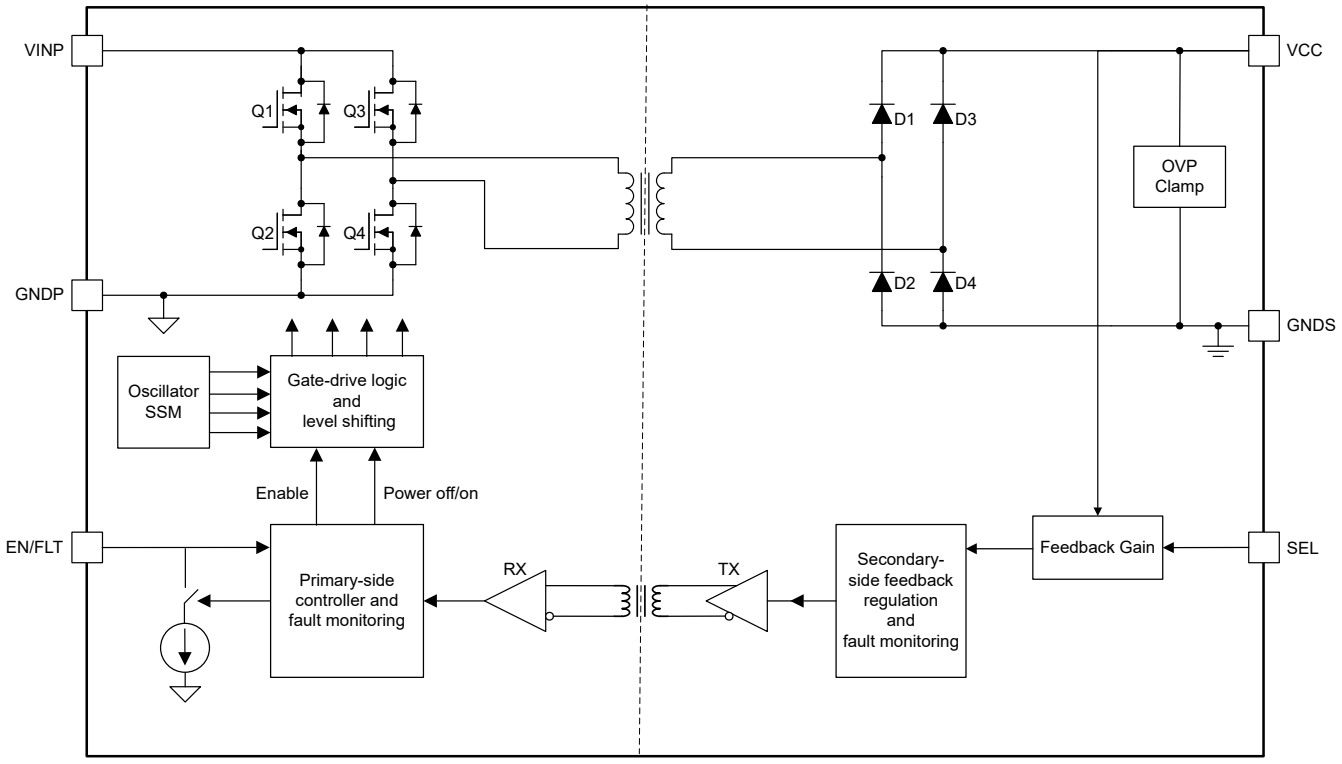
This module is easy-to-use, low profile, and has high power density, making it ideal for size constrained, cost sensitive systems to replace bulky and expensive transformer based designs with minimum design effort.

The integrated DC/DC converter uses switched mode operation and proprietary circuit techniques to reduce power losses and boost efficiency across all loading conditions. Specialized control mechanisms, clocking schemes, and the use of an on-chip transformer provide high efficiency and low electro-magnetic emissions.

The VINP supply is provided to the primary power controller that switches the power stage connected to the integrated transformer. Power is transferred to the secondary side, rectified, and regulated using a fast hysteretic burst mode control scheme that monitors VCC and ensures it is kept within the hysteresis band under normal and transient loading events while maintaining efficient operation across all loading conditions. The VCC is regulated to 3.3V or to 3.7V by SEL pin connection to have enough headroom for a post regulator LDO for tighter regulation or lower output ripple requirement applications.

The device has an enable pin to turn the device on or off depending on the system requirement. Pulling enable pin low reduces the quiescent current significantly if the system wants to operate in a low power consumption mode. The enable pin can also be used as a fault reporting pin, when connected to 18kΩ, the pin pulls low for t_{Fault} for any fault shutdown of the device. The device has a soft-start mechanism for a smooth and fast VCC ramp up with minimum input inrush current to avoid oversizing front-end power supplies powering the device's input.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Enable and Disable

Forcing EN/FLT pin low disables the device, which greatly reduces the VINP power consumption. Pull the EN/FLT pin high to enable normal device functionality. The EN/FLT pin has a weak internal pull-down resistor so it is not recommended to leave this pin floating in noisy systems.

7.3.2 Output Voltage Soft-Start

The UCC33411-Q1 integrates a soft-start mechanism that ensures a smooth and fast soft-start operation with minimum input inrush current. The output voltage Soft-Start diagram is shown in Figure 7-1. After VINP > $V_{VINP_UVLO_R}$ and EN/FLT is pulled high, the soft-start sequence starts with a primary duty cycle open loop control. The power stage operates with a fixed burst frequency with an incremental increasing duty cycle The rate of change of the duty cycle is pre-programmed in the part to reduce the input inrush current while building the output voltage VCC. The primary side limits the maximum duty cycle during this phase till the secondary side VCC voltage passes V_{VCC_UVLO}. This limit prevents excessive input current in case the device starts on a short circuit and the VCC voltage is not increasing.

The soft-start time varies depending on the output capacitors, input voltage and loading conditions. The UCC33411-Q1 has a soft-start timeout feature by which the VCC output voltage state is monitored during soft-start. In certain conditions, the VCC might not reach steady-state regulation threshold due to short circuit on the output voltage as shown in Figure 7-2, heavy loading conditions above recommended operating conditions or higher output capacitor values as shown in Figure 7-3. In these conditions, if the soft-start timeout duration, $t_{SOFT_START_TIMEOUT}$ expires without the VCC reaching steady-state regulation, the part shuts down and EN/FLT pin pulls low for t_{Fault} to report the fault condition. An auto-restart timer starts afterward, the part attempts to restart $t_{RESTART}$. More details regarding fault reporting and auto-restart can be found in Fault Reporting and Auto-Restart. If the same conditions continue to exist the same cycle repeats again as shown in Figure 7-2 and Figure 7-3 below.

The UCC3341x_CALC can help the system designer check if the soft-start timeout condition above would take place based on the system's input voltage, outputvoltage, output capacitor and soft-start loading conditions.

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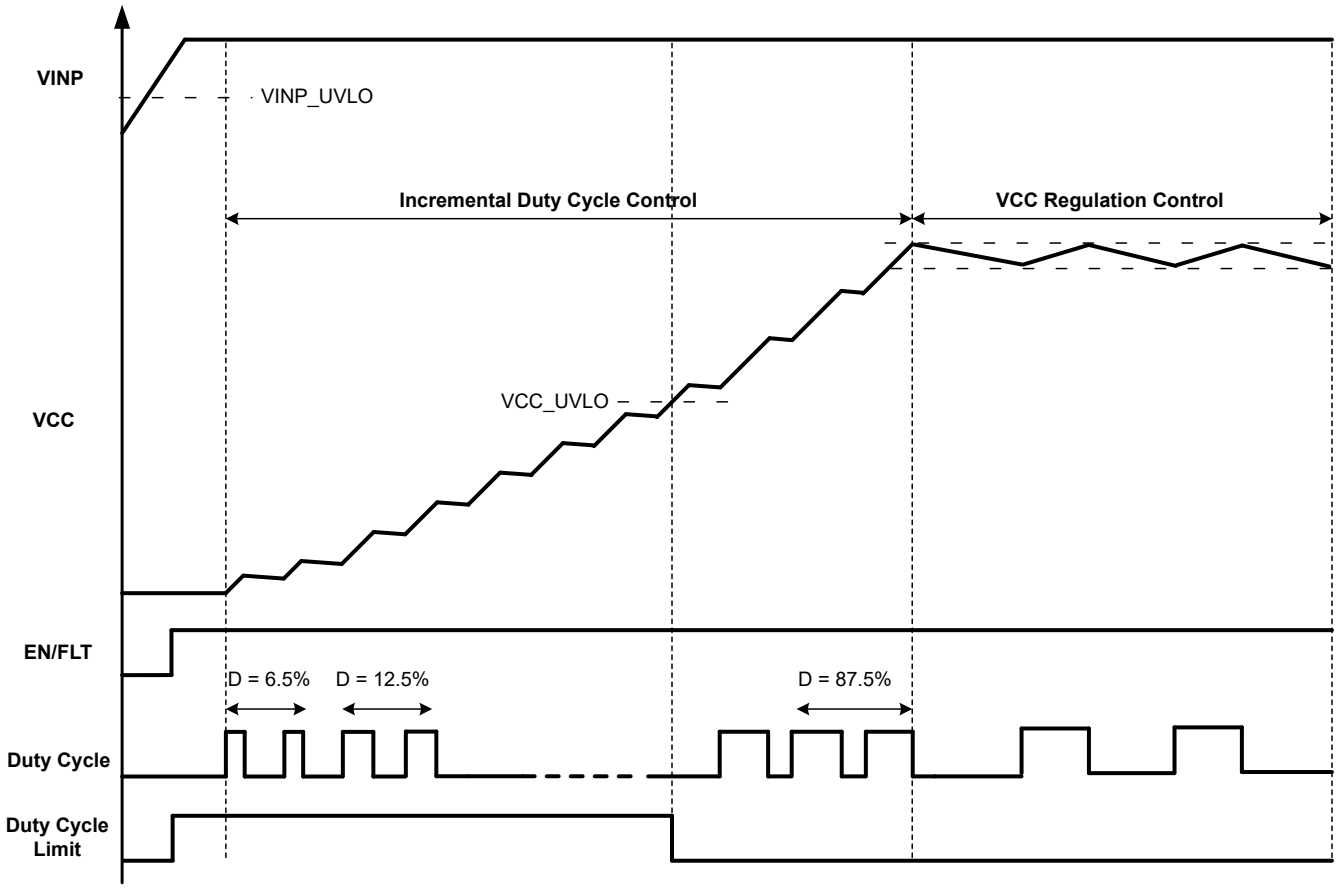

Figure 7-1. Output Voltage Soft-Start Diagram

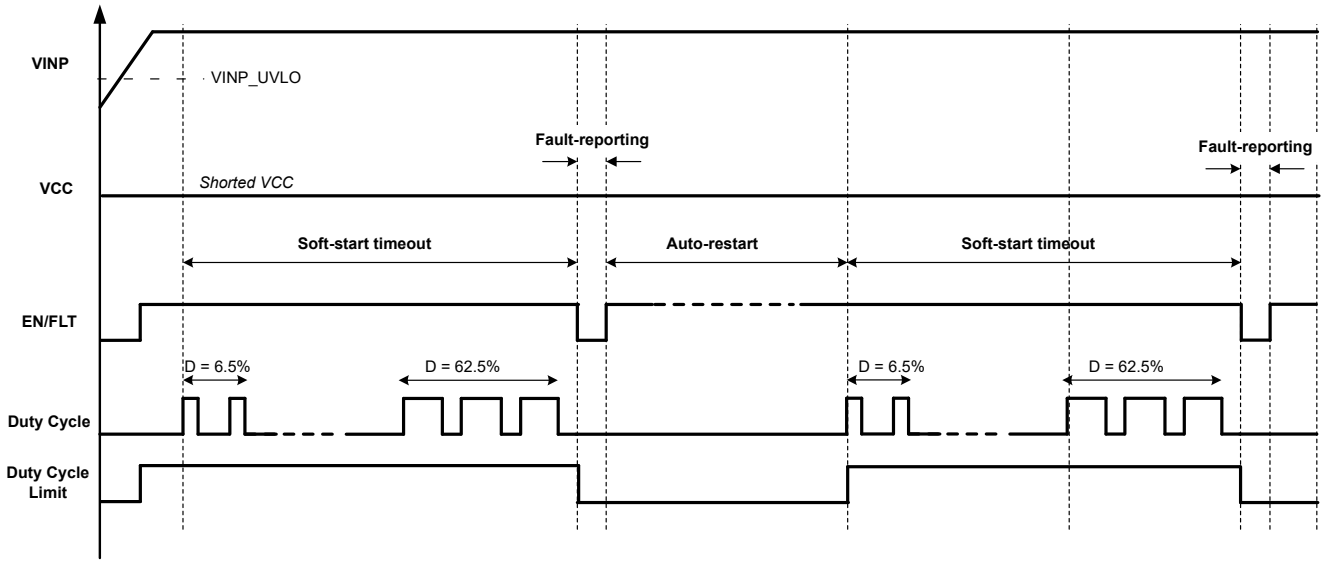

Figure 7-2. Soft-Start Under Short-Circuit Output Diagram

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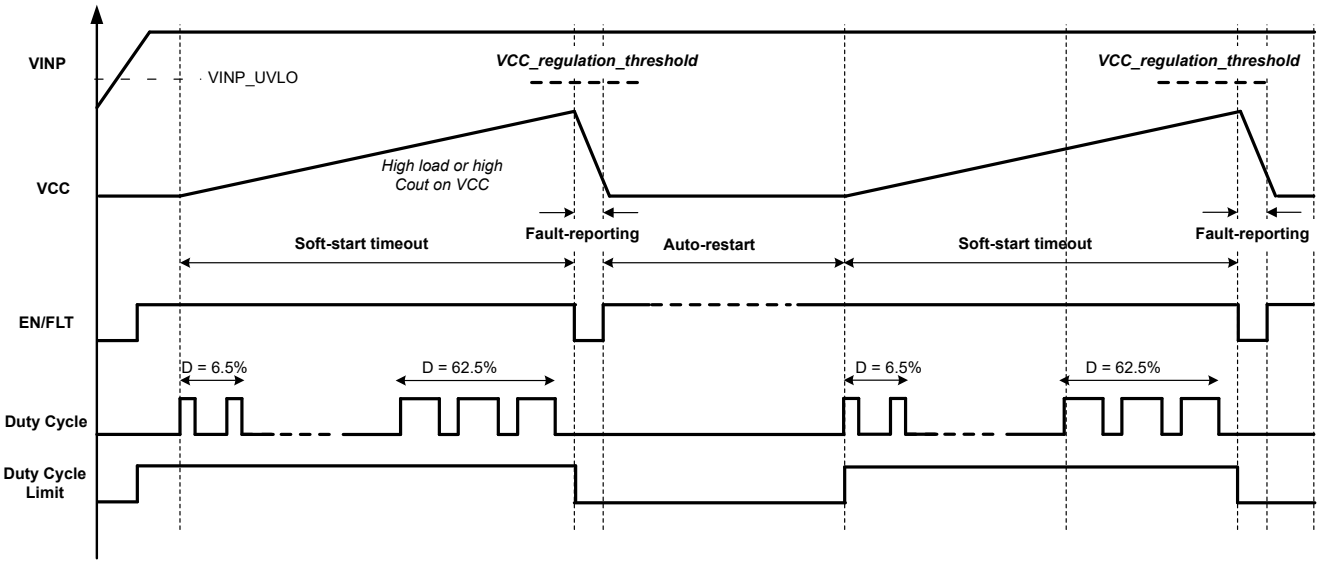

Figure 7-3. Soft-Start Under High Load or High Output Capacitor Conditions Diagram

7.3.3 Output Voltage Steady-State Regulation

The UCC33411-Q1 uses hysteretic control to regulate the output voltage between upper and lower bands as shown in Figure 7-4. The regulation block on the secondary side senses the regulated output voltage and sends a feedback signal to the primary side through the inductive communication channel to turn the primary power stage On or Off to maintain the regulated output within the hysteresis bands. During steady-state regulation, the burst frequency changes according to the output capacitors and loading conditions. The burst frequency is highest at higher loading conditions and lowest at light loading conditions by which light load efficiency improvements can be achieved.

The Burst-On duration (t_{ON}) increases with heavy loading conditions or higher output capacitor. The UCC33411-Q1 enters an overpower protection mode if the Burst-on duration exceeds t_{ON-MAX} as shown in Figure 7-5. In this condition, as the VCC has not reached the upper hysteresis threshold, the device turns-on the power stage again after minimum Burst-off duration of $t_{OFF-MIN}$. This repeats as the heavy load condition remains resulting in higher peak-to-peak VCC steady state ripple or lower VCC regulation voltage. The UCC3341x_CALC can help the system designer appropriately select the output capacitor for the targeted maximum load and input voltage range conditions to avoid triggering this condition.

The UCC33411-Q1 can program the VCC_REG voltage accoring to the SEL pin connection. The SEL pin voltage is monitored during soft-start sequence when VCC < V_{VCC_UVLO} threshold. The output voltage is then programmed to 3.3V with SEL = VCC or to 3.7V with SEL = GNDS. Note that after this initial monitoring, the SEL pin no longer affects the VCC output level. To change the output mode selection, either the EN/FLT pin must be toggled or the VINP power supply must be cycled off and back on.

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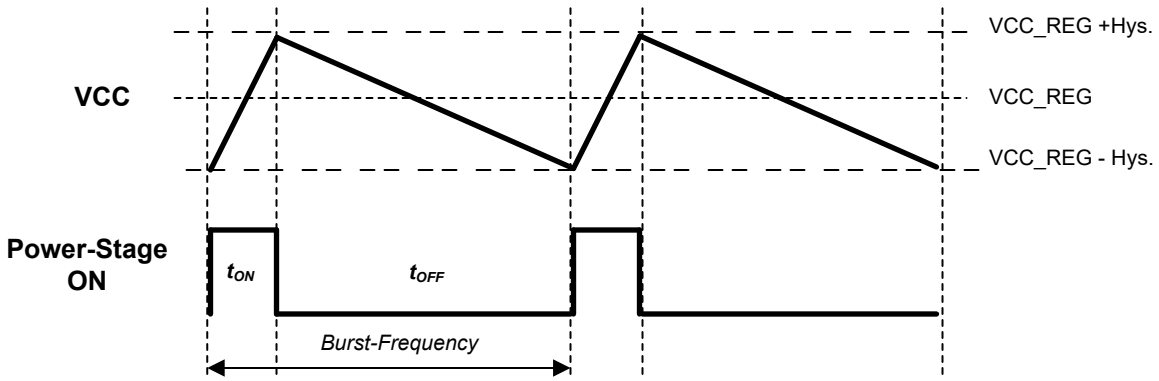

Figure 7-4. Output Voltage Hysteresis Mode Control

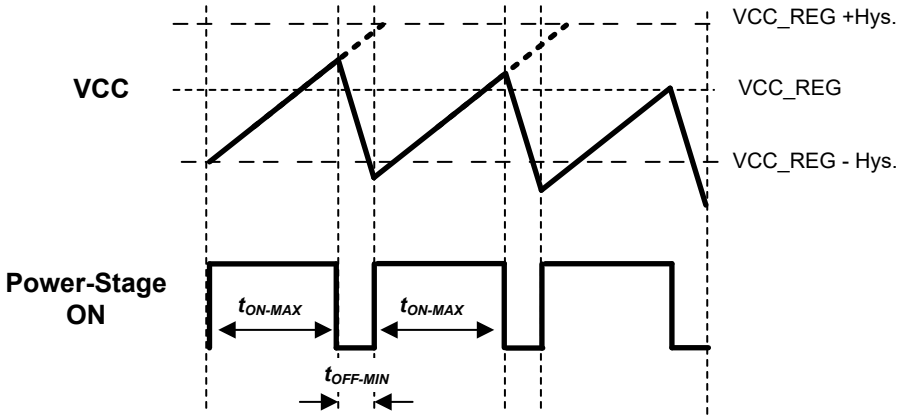

Figure 7-5. Overpower Protection Condition

7.3.4 Protection Features

The UCC33411-Q1 is equipped with a full set of protection functions including input under-voltage lockout, input over-voltage lockout, output under-voltage protection, and over-temperature protection. In addition, the device has a fault reporting mechanism to notify the system of any faults causing a shutdown. Under certain faulty conditions the device shuts down and attempts an auto-restart after $t_{RESTART}$

7.3.4.1 Input Under-Voltage and Over-Voltage Lockout

The UCC33411-Q1 can operate at input voltage range from 4.5V to 5.5V. If the VINP < $V_{VINP_UVLO_F}$ or VINP > $V_{VINP_OVLO_R}$ conditions occurred, the converter stops switching and part shuts down. Once the VINP returns to normal operation range, VINP > $V_{VINP_UVLO_R}$ or VINP < $V_{VINP_OVLO_F}$. The part resumes switching immediately without waiting for the auto-restart timer.

7.3.4.2 Output Under-Voltage Protection

The UCC33411-Q1 has under voltage protection feature to protect the part when overload condition occurs. If an overload or a short circuit occurs at VCC such that VCC < V_{UVP} condition occurs, the converter will go into the duty cycle limit mode as in the soft-start operation then will shutdown after a deglitch time of $t_{VCC_UVP_DEGLITCH}$. The deglitch time is added to accommodate for any instantaneous overloading or short circuit conditions that might be removed quickly and normal operation can resume. Once the part shuts down, the part will attempt an auto-restart after $t_{RESTART}$. If the fault condition remains, the part will shutdown again and attempt another auto-restart.

7.3.4.3 Output Over-Voltage Protection

The UCC33411-Q1 has over voltage protection feature to protect the load against over-voltage conditions during severe transient events causing large overshoots on the output voltage. If the VCC voltage rise above

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$V_{VCC_OVP_R}$ threshold, an OV_CLAMP circuit verifies the output voltage remains within absolute maximum operating conditions. The converter enters duty cycle limit mode as in the soft-start operation then shuts down after a a deglitch time of $t_{VCC_OV_clamp_deglitch}$. Once the part shuts down, the part attempts an auto-restart after $t_{RESTART}$. If the fault condition remains, the part shuts down again and attempts another auto-restart.

7.3.4.4 Over-Temperature Protection

The UCC33411-Q1 integrates the primary-side and secondary-side power stages, as well as the isolation transformer. The power loss caused by the power conversion causes the module temperature to rise above the ambient temperature. To ensure the safe operation of the power module, the device is equipped with over-temperature protection. Both the primary-side power stage, and the secondary-side power stage temperatures are sensed and compared with the over-temperature protection threshold. If the primary-side power stage temperature becomes higher TSD_{P_R}, or the secondary-side power stage temperature becomes higher than TSD_{S_R} , the module enters over-temperature protection mode. The module stops switching after a deglitch time of $t_{TSHUTP_DEGLITCH_D}$, report the fault and attempt an auto-restart after $t_{RESTART}$.

7.3.4.5 Fault Reporting and Auto-Restart

The UCC33411-Q1 has a fault reporting mechanism that can alert a system level MCU or monitoring circuitry of faulty conditions on the device that resulted in a shutdown. If an input over-voltage, over-temperature or output under-voltage protection faults occur. The primary-side controller and fault monitoring system enables a current source that sinks I_{Fault} current for t_{Fault} duration. If a resistor >18kΩ is connected between the MCU and the EN/FLT pin, the EN/FLT pin will pull low to V_{FLT} for the same t_{Fault} duration whenever one of the above mentioned faults occur that resulted in a shutdown of the device as shown in Figure 7-6. If the fault reporting mechanism is not required on the system, the EN/FLT pin can be connected directly to the enable source voltage without the 18kΩ resistor.

The device has an auto-restart feature that occurs after the device is shutdown when output under-voltage or over-temperature faults occur. After the t_{Fault} time expires, a timer starts and after $t_{RESTART}$ the part attempts a new soft-start sequence as shown in Figure 7-7. If the fault has been removed, the VCC soft-starts to regulation successfully. If the fault remains, the part shuts down again and report the fault. The device can continuously operate safely in hiccup mode as long as the fault persists.

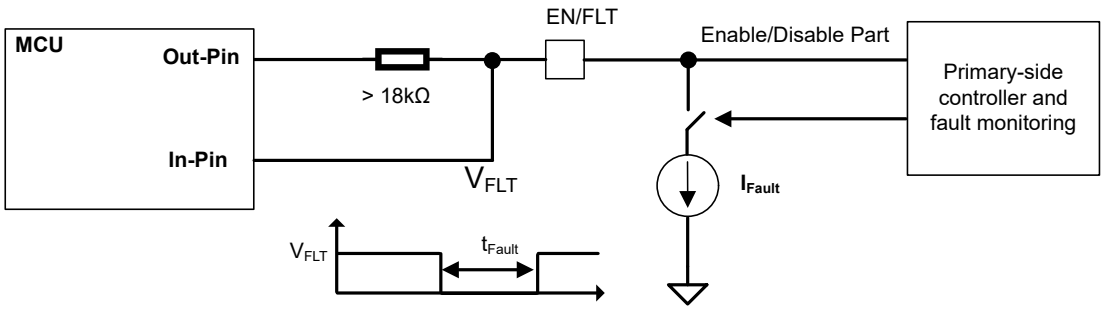

Figure 7-6. Fault Reporting Mechanism

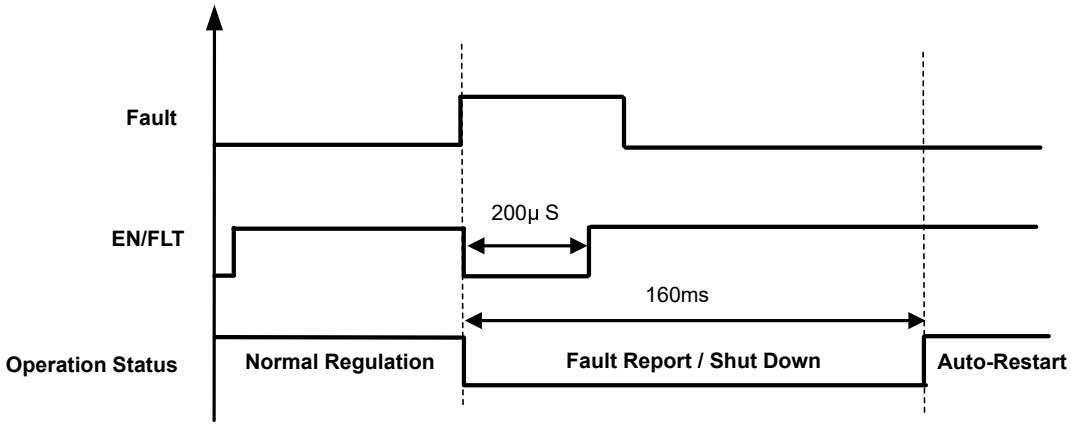

Figure 7-7. Auto-Restart Operation

7.3.5 VCC Load Recommended Operating Area

Figure 7-8 depicts the device VCC regulation behavior across the output load range, including when the output is overloaded. For proper device operation, ensure that the device VCC output load does not exceed the maximum output current I_{OUT_MAX}. If the UCC33411-Q1 is loaded beyond the recommended operating area, the VCC drops and once it goes below the VCC_UVP threshold, the part enters a power limiting mode to avoid stressing the device until power stage stop switching and shutdown.

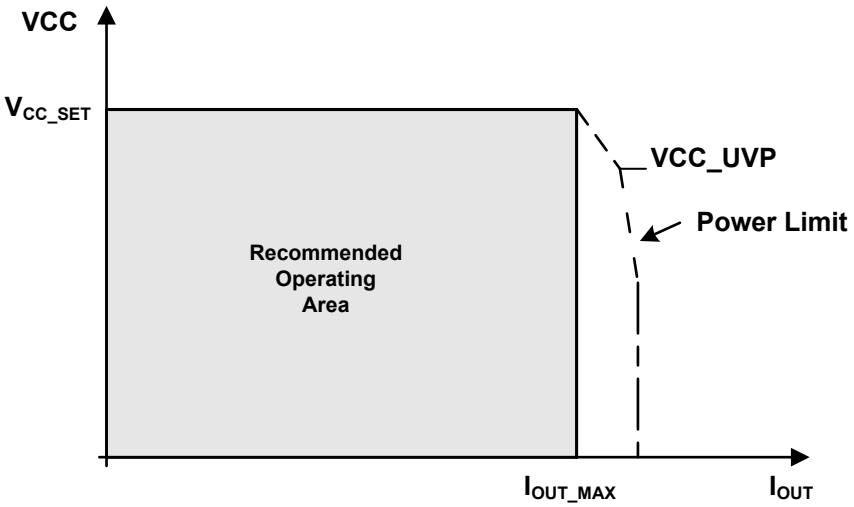

Figure 7-8. VCC Load Recommended Operating Area Description

7.3.6 Electromagnetic Compatibility (EMC) Considerations

UCC33411-Q1 devices use adaptive spread spectrum modulation (SSM) algorithm for the internal oscillator to reduce the noise emissions from the device. The adaptive SSM algorithm ensures a full switching frequency span between two bands during each burst cycle regardless of the loading conditions to ensure similar impact of SSM at different loading conditions. In addition, the UCC33411-Q1 uses advanced internal layout scheme to minimize radiated emissions at the system level.

7.4 Device Functional Modes

Table 7-1 lists the supply functional modes for this device.

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Table 7-1. Device Functional Modes

INPUTS		ISOLATED SUPPLY OUTPUT VOLTAGE (VCC) SETPOINT
EN/FLT	SEL	
HIGH	Shorted to VCC	3.3V
HIGH	Shorted to GNDS	3.7V
Low	x	0V
OPEN(1)	OPEN(1)	UNSUPPORTED

(1) The SEL and EN/FLT pins has an internal weak pull-down resistance to ground, but leaving these pins open is not recommended.

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The UCC33411-Q1 device is suitable for applications that have limited board space and desire more integration. This device is also suitable for very high voltage applications, where power transformers meeting the required isolation specifications are bulky and expensive.

8.2 Typical Application

Figure 8-1 shows the schematic for the UCC33411-Q1 device supplying an isolated load.

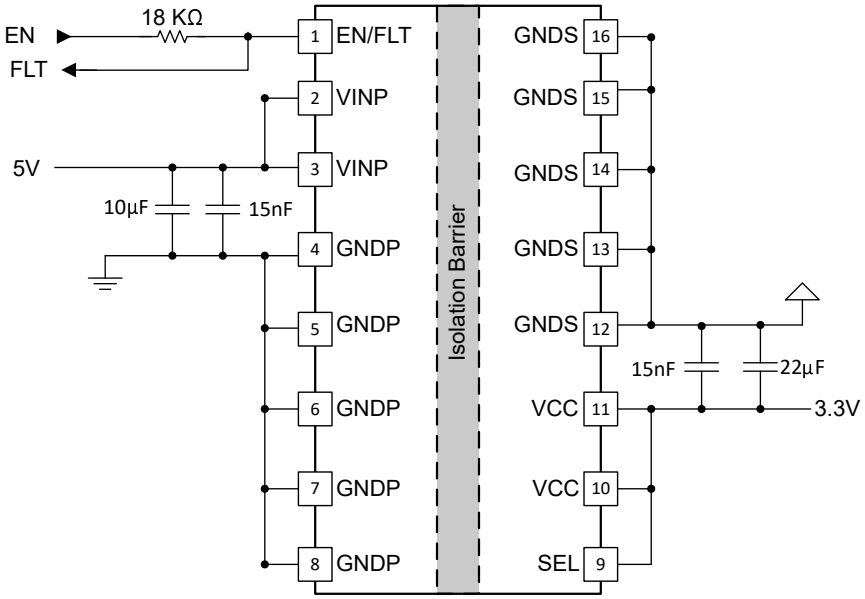

Figure 8-1. Typical Application

8.2.1 Design Requirements

To design using UCC33411-Q1, a few simple design considerations must be evaluated. Table 8-1 shows some recommended values for a typical application. See Section 8.3 and Section 8.4 sections to review other key design considerations for the UCC33411-Q1.

Table 8-1. Design Parameters

PARAMETER	RECOMMENDED VALUE
Input supply voltage, VINP	4.5V to 5.5V
First Decoupling capacitance between VINP and GNDP	15nF, 50V, ± 10%, X7R
Second Decoupling capacitance between VINP and GNDP	10µF, 10V, X7R
First Decoupling capacitance between VCC and GNDS	15nF, 50V, ± 10%, X7R
Second Decoupling capacitance between VCC and GNDS	22µF, 10V, X7R
EN/FLT pin resistor for fault reporting	18kΩ

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8.2.2 Detailed Design Procedure

The UCC33411-Q1 design procedure is very simple, the device requires two decoupling capacitors connected between VINP and GNDP pins for the input supply, and two decoupling capacitors for the isolated output supply placed between VCC and GNDS pins to form a completely functional DC/DC converter.

The SEL should be tied directly to VCC to select a 3.3V output voltage, and to GNDS to select a 3.7V output voltage. The higher voltage setting allows UCC33411-Q1 to output a higher voltage with enough headroom for an external LDO to provide aditional regulation accuracy.

Low ESR, ESL ceramic capacitors are recommended to be connected close to the device pins. Note that the effective burst frequency is impacted by the selected VCC output capacitor.

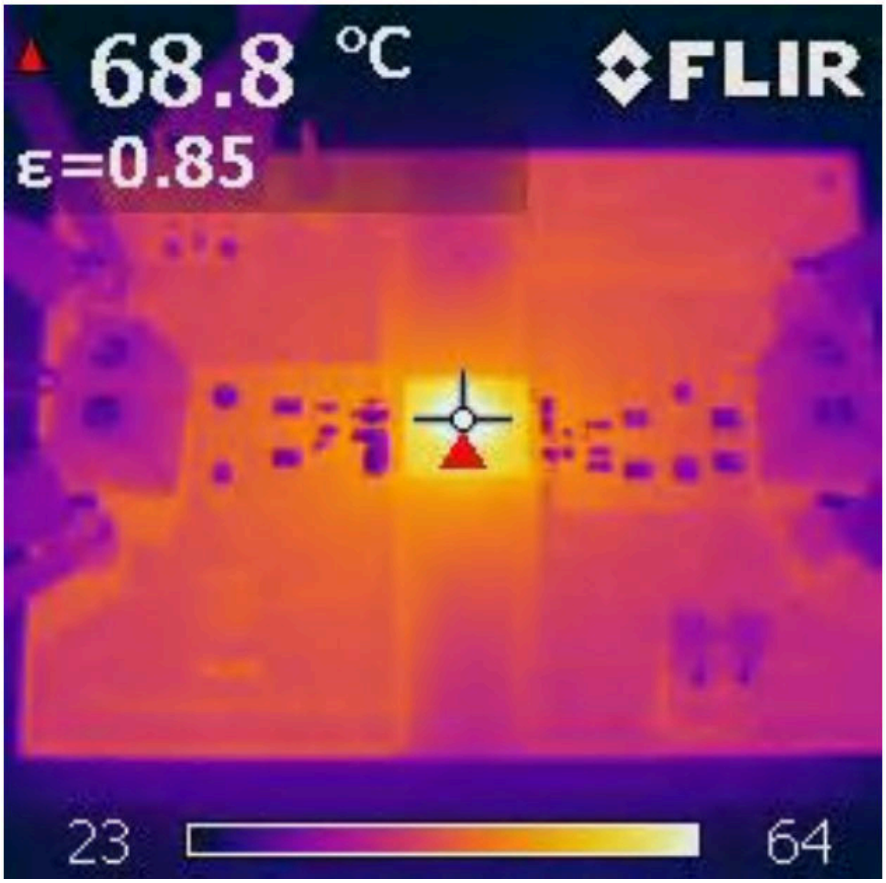

Figure 8-2. UCC33411-Q1 Thermal Image: VINP = 5.0V, VCC = 3.3V, P_{Out}=1.0W

8.3 Power Supply Recommendations

The recommended input supply voltage (VINP) for the UCC33411-Q1 is between 4.5V and 5.5V. To help ensure reliable operation, adequate decoupling capacitors must be located as close to supply pins as possible. Place local bypass capacitors between the VINP and GNDP pins at the input, and between VCC and GNDS at the isolated output supply. The input supply must have an appropriate current rating to support output load required by the end application, as well as sufficient current to charge the output capacitance within before the soft start timeout expires (Typically 150mA during soft start).

8.4 Layout

8.4.1 Layout Guidelines

The UCC33411-Q1 integrated isolated power solution simplifies system design and reduces board area usage. Proper PCB layout is important to achieve optimum performance. Here is a list of recommendations:

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- Place decoupling capacitors as close as possible to the device pins. For the input supply, place 0402 and 0805 ceramic capacitor between pins 2 and 3 (VINP) and pins 4, 5, 6, 7 and 8 (GNDP). For the isolated output supply, place 0402 and 0805 ceramic capacitor between pins 10 and 11 (VCC) and pins 12, 13, 14, 15 and 16 (GNDS). This location is of particular importance to the input decoupling capacitor, because this capacitor supplies the transient current associated with the fast switching waveforms of the power drive circuits.
- Because the device does not have a thermal pad for heat-sinking, the device dissipates heat through the respective GND pins. Ensure that enough copper (preferably a connection to the ground plane) is present on all GNDP and GNDS pins for best heat-sinking. Placing vias close to the device pins and away from the high frequency path between the ceramic capacitors and the device pins is essential for better thermal performance.
- If space and layer count allow, it is also recommended to connect the VINP, GNDP, VCC and GNDS pins to internal ground or power planes through multiple vias of adequate size. Alternatively, make traces for these nets as wide as possible to minimize losses.
- Pay close attention to the spacing between primary ground plane (GNDP), and any signals refrenced to it, and secondary ground plane (GNDS) and it's signals on the PCB outer layers. The effective creepage and or clearance of the system reduces if the two ground planes and their respective signals have a lower spacing than that of the device package.

8.4.2 Layout Example

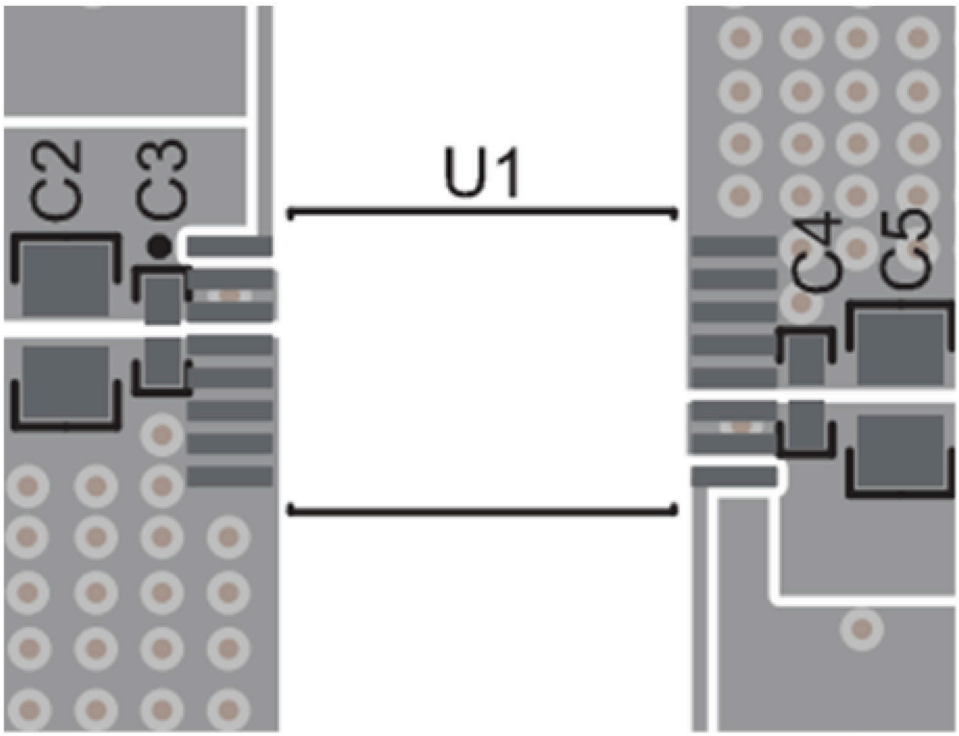

Figure 8-3. Layout Example

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9 Device and Documentation Support

9.1 Device Support

9.1.1 Third-Party Products Disclaimer

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9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *UCC33421EVM-092 Evaluation Module for Automotive and Industrial Applications User's Guide*
- Texas Instruments, UCC33411(-Q1) CISPR-32 Class B Certificate of Compliance
- Texas Instruments, UCC3341x(-Q1) Simplis Model
- Texas Instruments, UCC3341x(-Q1) Soft-start rise time and burst-on duration calculator
- Texas Instruments, Isolation Glossary

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.5 Trademarks

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All trademarks are the property of their respective owners.

9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (November 2024) to Revision A (March 2026)	Page
• Changed the document status from *Advance Information* to *Production Data*	1

11 Mechanical and Packaging Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PUCC33411QDHARQ1	Active	Preproduction	SO-MOD (DHA) | 16	3000 | LARGE T&R	-	Call TI	Call TI	-	
PUCC33411QDHARQ1.A	Active	Preproduction	SO-MOD (DHA) | 16	3000 | LARGE T&R	-	Call TI	Call TI	See PUCC33411QDHARQ1	
UCC33411QDHARQ1	Active	Production	SO-MOD (DHA) | 16	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-	UC33411Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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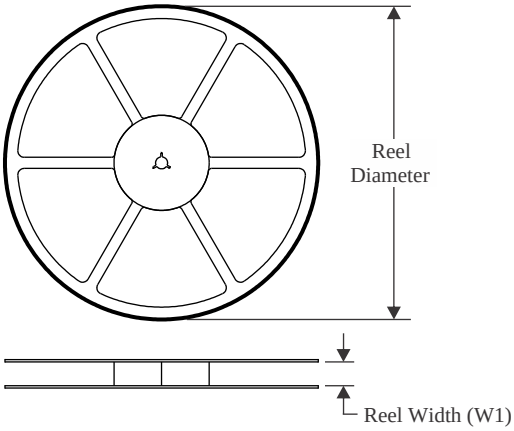
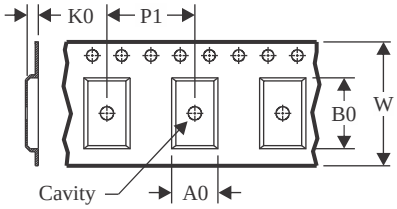
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

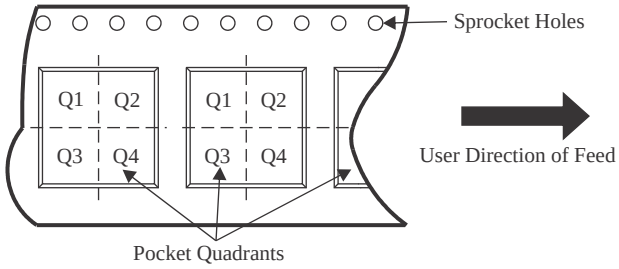


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

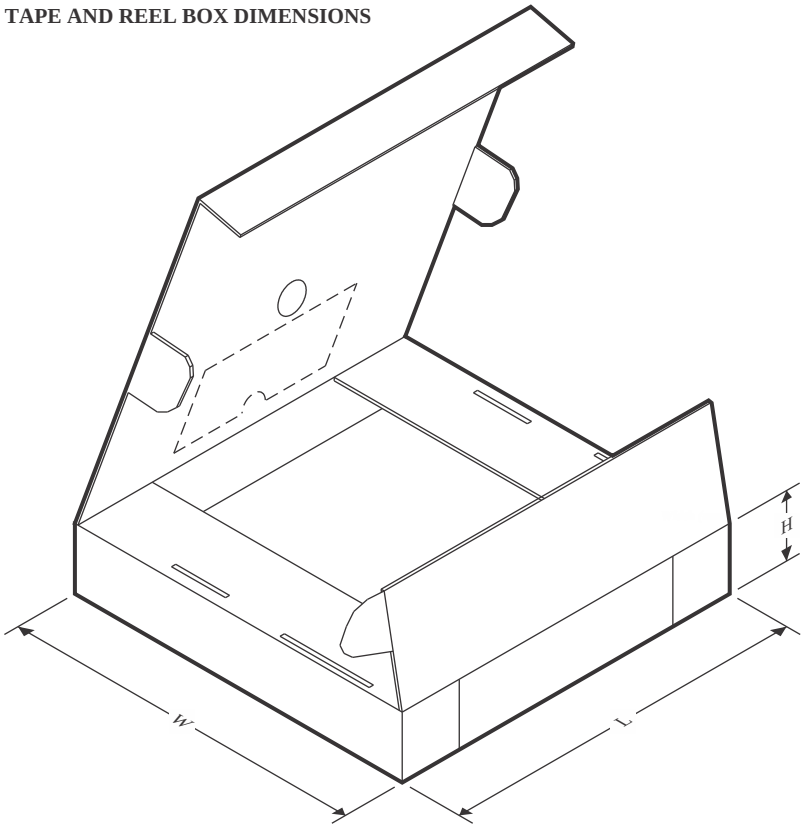
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC33411QDHARQ1	SO-MOD	DHA	16	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

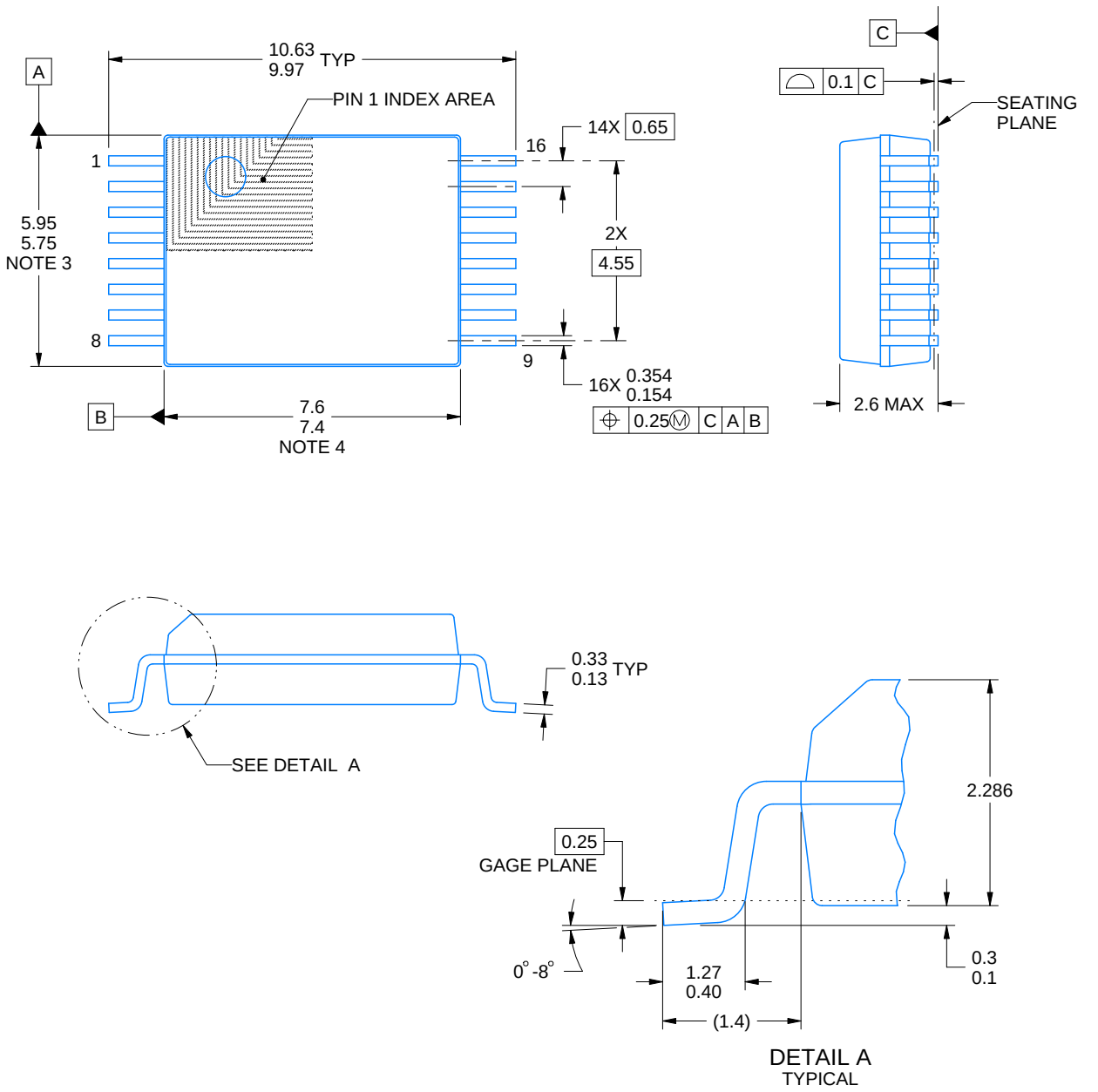
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC33411QDHARQ1	SO-MOD	DHA	16	1000	350.0	350.0	43.0

PACKAGE OUTLINE

DHA0016A

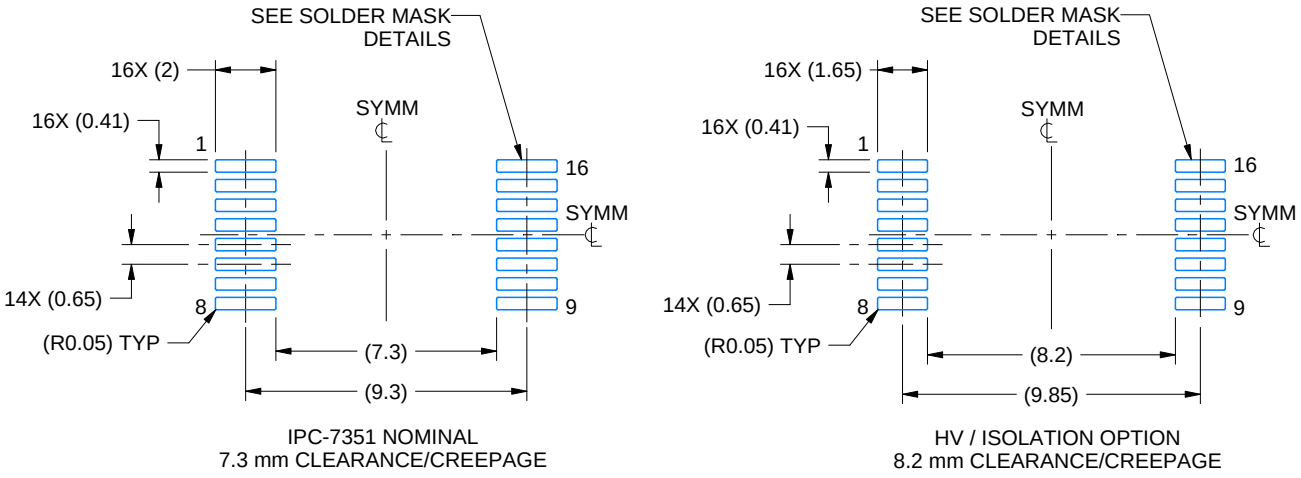
SSOP - 2.6 mm max height

SMALL OUTLINE PACKAGE

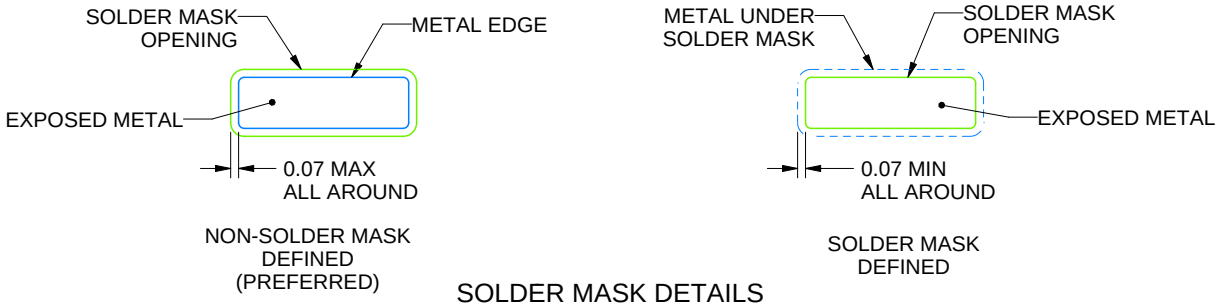


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLES
EXPOSED METAL SHOWN
SCALE: 4X



SOLDER MASK DETAILS

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NOTES: (continued)

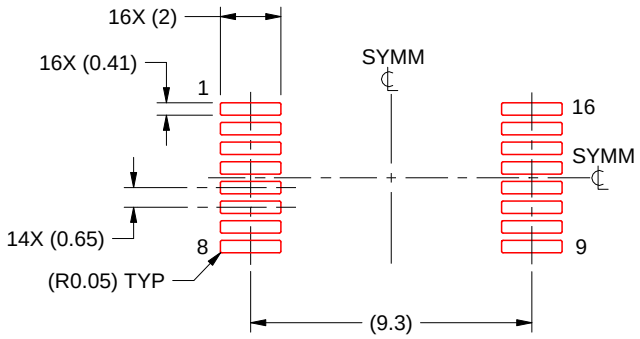
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

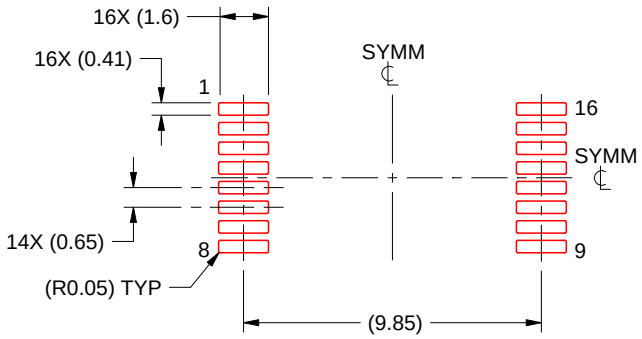
DHA0016A

SSOP - 2.6 mm max height

SMALL OUTLINE PACKAGE



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE



HV / ISOLATION OPTION
8.2 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLES
BASED ON 0.125 mm THICK STENCIL
SCALE: 4X

4230131/A 10/2023

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025