UCC34141 Industrial 1.5W, 12V V_{IN}, 25V V_{OUT}, High Power Density, > 5kV_{RMS}, Isolated DC/DC Module

1 Features

- Fully integrated isolated planar transformer
- Wide input range: 5.5V to 28V (with 22V OVLO)
  - ≥ 1.5W typical output for 11V ≤ V_{VIN} ≤ 13V, 18V ≤ $V_{VDD\text{-}COM}$ ≤ 20V, at T_A ≤ 85°C
- Programmable (VDD – COM) output voltage
  - 15V to 20V, ≤ ±1.5% total regulation accuracy
- Programmable (VEE – COM) output voltage
  - -2V to -8V, ≤ ±5% total regulation accuracy
- Adaptive spread spectrum modulation (SSM)
- Strong magnetic and radiated field immunities
- Reduced inrush current soft-start
- ENA pin for logic enable and programming input UVLO
- Open-drain Power-Good for fault indication
- Integrated protections: UVLO, OVLO, short-circuit, OVP, UVP, and thermal shutdown.
- < 3pF isolation capacitance
- > 8.2mm creepage and clearance
- Static and dynamic CMTI > ±250kV/µs

2 Applications

- Data center
  - Rack power and thermal management
- Energy infrastructure
  - DC fast charging power module
  - DC fast charging station
  - String inverter
- Power delivery
  - Industrial AC-DC

3 Description

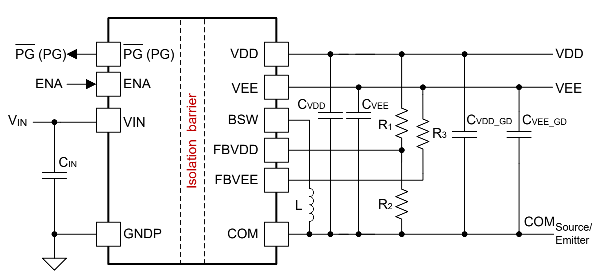
UCC34141 is a reinforced isolation, high working voltage, DC/DC power module designed to provide power to SiC and IGBT isolated gate drivers. TI's proprietary integrated transformer and advanced control architectures achieve high power density, low noise, and a low system bill of materials. This device is capable of delivering 1.5W typical output power at 85°C ambient temperature. The highly accurate dual-output voltages, easily set by resistor dividers, enables low on-resistance, fast and reliable switching for SiC/IGBT. The low-latency feedback control reduces the output capacitance for fast load transient and supports dynamic voltage programming. The wide input voltage and adjustable V_{IN} UVLO supports both wide battery voltage of electric vehicles and regulated input rails. The device is operational from 5.5V to 20V V_{IN}, and can withstand V_{IN} overvoltage transients up to 28V.

The integrated protection features, fault-report Power-Good pin, and enables function increase system robustness and save external components. The SOIC package with 8.2mm creepage and clearance distance establishes high isolation capability.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
UCC34141 DDHAR	DHA (SSOP, 16)	5.85mm × 7.50mm

(1) For all available packages, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Application

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4 Device Comparison

Table 4-1. Device Comparison Table

DEVICE NAME	V_{VIN} RANGE	OUTPUT (VDD-COM) ADJUSTABLE RANGE	OUTPUT (VEE-COM) ADJUSTABLE RANGE	TYPICAL POWER	POWER-GOOD ACTIVE POLARITY	FAULT RESPONSE
UCC34141D	8V to 20V	18V to 20V	-2V to -8V	1.5W	HIGH	AUTO-RESTART
		15V to 18V	-2V to -8V	≥1W		
	5.5V to 8V	15V to 20V	-2V to -8V	≥0.3W		

5 Pin Configuration and Functions

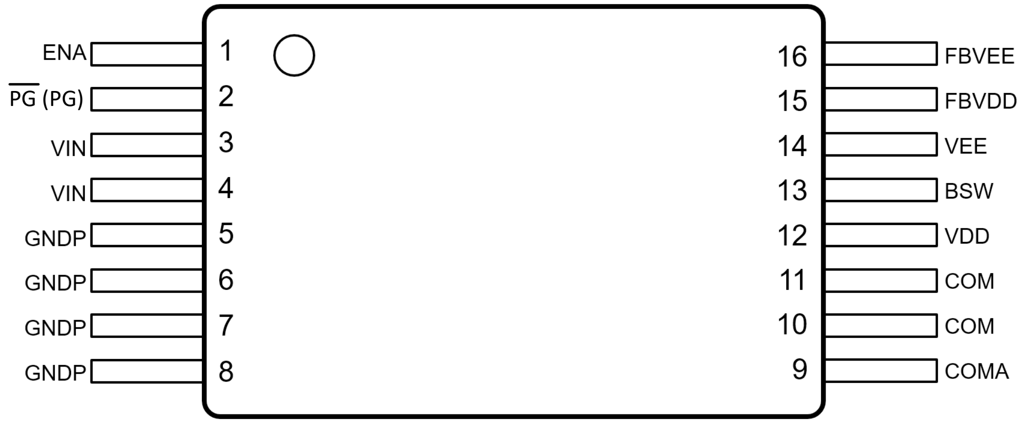


Figure 5-1. DHA Package, 16-Pin SSOP (Top View)

Table 5-1. Pin Functions

PIN		TYPE (1)	DESCRIPTION
NAME	NO.		
BSW	13	P	Internal buck-boost converter switch pin. Connect an inductor from this pin to COM. Recommend a 3.3µH to 10µH chip inductor. If using the device in single output mode leave this pin floating.
COM	10, 11	G	Secondary ground. Connect to Source of power switch.
COMA	9	G	Secondary-side analog sense reference connection for the noise sensitive analog feedback input FBVDD, and FBVEE. Connect the low-side FBVDD feedback resistor and high frequency decoupling filter capacitors close to the COMA pin and respective feedback pin FBVDD. Connect to secondary-side gate drive voltage reference, COM. Use a single point connection and place the high frequency decoupling ceramic capacitor close to the COMA pin.
ENA	1	I	Enable pin. Forcing ENA LOW disables the device. Pull HIGH to enable normal device functionality. Can be used to program input UVLO with a resistor divider from VIN.
FBVDD	15	I	Feedback (VDD – COM) output voltage sense pin and to adjust the output (VDD – COM) voltage. Connect a resistor divider from VDD to COMA so that the midpoint is connected to FBVDD. The equivalent FBVDD voltage is regulated at 2.5V with the internal hysteresis control across isolation. Adding a 470pF ceramic capacitor for high frequency decoupling in parallel with the low-side feedback resistor is needed. The 470pF ceramic capacitor for high frequency bypass must be next to the FBVDD and COMA pins on top layer or back layer connected with vias.
FBVEE	16	I	Feedback (COM – VEE) output voltage sense pin used to adjust the output (COM – VEE) voltage. Connect one feedback resistor to VEE to program the (COM – VEE) voltage from 2V to 8V. Connect a 10pF ceramic capacitor from FBVEE to COMA for bypassing high frequency noise. The 10pF ceramic capacitor must be next to the FBVEE pin on top layer or back layer connected with vias. If using the device in single output mode connect a 180kΩ resistor to VEE.
GNDP	5, 6, 7, 8	G	Primary-side ground connection for VIN. Place several vias to copper pours for thermal relief.
$\overline{PG}$(PG)	2	O	Power-Good open-drain output pin. Remains active when $V_{VIN\_UVLOP} \le V_{VIN} \le V_{VIN\_OVLOP}$; $V_{VDD\_UVP} \le V_{FBVDD} \le V_{VDD\_OVP}$; $V_{VEE\_UVP} \le V_{FBVEE} \le V_{VEE\_OVP}$; $T_{J\_Primary} \le T_{SHUT\_P\_R}$; and $T_{J\_secondary} \le T_{SHUT\_S\_R}$. Pull up to a 3.3V or 5V rail through a 4.99kΩ resistor. Connect a 1uF decoupling capacitor in 0402 body size for by-passing the high frequency noise next to the Power-Good pin on the same side of the PCB as the IC. This pin is active low for UCC34141-Q1 but can active high depending on the part number.
VDD	12	P	Secondary-side isolated output voltage from transformer. Connect a 10µF and a parallel 0.1µF ceramic capacitor from VDD to COM. The 0.1µF ceramic capacitor in 0402 body size is for bypassing high frequency noise and must be next to the VDD and COM pins.
VEE	14	P	Secondary-side isolated output voltage for negative rail. Connect a 2.2µF ceramic capacitor from VEE to COM for bypassing high frequency noise. If using the device in single output mode connect VEE directly to COM.

Table 5-1. Pin Functions (continued)

PIN		TYPE [(1)]	DESCRIPTION
NAME	NO.		
VIN	3, 4	P	Primary input voltage. Connect a 10µF and a parallel 0.1µF ceramic capacitor from VIN to GNDP. The 0.1µF ceramic capacitor in 0402 body size is for by-passing the high frequency noise and must be next to the VIN and GNDP pins on the same side of the PCB as the IC.

(1) P = power, G = ground, I = input, O = output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	TYP	MAX	UNIT
V_{VIN}	VIN to GNDP	–0.3		30	V
V_{ENA}, V_{PG}	ENA, PG to GNDP	–0.3		7	V
$V_{FBVEE\text{-}COM}$	FBVEE to COM	-0.3		7	V
$V_{BSW\text{-}COM}$	BSW to COM	-10		25.5	V
$V_{BSW\text{-}VEE}$	BSW to VEE	-0.7		32	V
$V_{BSW\text{-}VEE\_tran}$	BSW to VEE (0.24ns transient)	-2.1		33.4	V
$V_{COM\text{-}VEE}$	COM to VEE	-0.3		10	V
$V_{VDD\text{-}COM}$, $V_{FBVDD\text{-}COM}$	VDD, FBVDD to COM	–0.3		25.5	V
$V_{VDD\text{-}VEE}$	VDD to VEE	–0.3		32	V
$P_{OUT\_VDD\_MAX}$	Total output power at T_A=25°C			3	W
T_J	Operating junction temperature range	–40		150	°C
T_{stg}	Storage temperature	–65		150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002	±750	V

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{VIN}	Primary-side input voltage to GNDP during continuous operation	5.5[1]	12	20	V
V_{VIN}	Primary-side input voltage to GNDP during overvoltage transient			28	V
V_{ENA}	Enable to GNDP	0		5.5	V
V_{PG}	Power-Good to GNDP	0		5.5	V
$V_{VDD\text{-}COM}$	VDD to COM	15	18	20	V
$V_{VDD\text{-}VEE}$	VDD to VEE	15	22	25	V
$V_{COM\text{-}VEE}$	COM to VEE	2	4	8	V
T_A	Ambient temperature	–40		125	°C
T_J [2]	Junction temperature	–40		150	°C

(1) See the $V_{VIN\_UVLO\_R}$ and $V_{VIN\_UVLO\_F}$ electrical characteristics for the minimum operational V_{VIN}.
(2) See the Typical Characteristics section and COM_VEE Output Capability section for maximum rated load values across temperature and V_{VIN} conditions for different (VDD-COM) and (COM-VEE) output voltage settings.

6.4 Thermal Information

THERMAL METRIC[1]		DHA (SOIC) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	63.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	32.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	20.1	°C/W
Ψ_{JA}	Junction-to-ambient characterization parameter	47.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	20.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	3	°C/W

(1) The thermal resistances (R) are based on JEDEC board, and the characterization parameters (Ψ) are based on the EVM described in the Layout section. For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

6.5 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
General				
CLR	External clearance [1]	Shortest terminal-to-terminal distance through air	> 8.2	mm
CPG	External creepage [1]	Shortest terminal-to-terminal distance across the package surface	> 8.2	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance – transformer power isolation)	> 70	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category	Rated mains voltage ≤ $300V_{RMS}$	I-IV	
		Rated mains voltage ≤ $600V_{RMS}$	I-IV	
		Rated mains voltage ≤ $1000V_{RMS}$	I-III	
DIN EN IEC 60747-17 (VDE 0884-17) (Planned Certification Targets) [2]				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1700	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage (sine wave) Time dependent dielectric breakdown (TDDB) test	1202	V_{RMS}
		DC voltage	1700	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1s (100% production)	7071	V_{PK}
V_{IMP}	Maximum impulse voltage [3]	Tested in air, 1.2/50µs waveform per IEC 62368-1	8000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage [3]	$V_{IOSM} \geq 1.3 \times V_{IMP}$; Tested in oil (qualification test), 1.2/50µs waveform per IEC 62368-1	10400	V_{PK}
q_{pd}	Apparent charge [4]	Method a: After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10s	≤ 5	pC
		Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10s	≤ 5	pC
		Method b1: At routine test (100% production), $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1s	≤ 5	pC
C_{IO}	Barrier capacitance, input to output [5]	$V_{IO} = 0.4 \sin(2\pi ft)$, f = 1MHz	< 3	pF
R_{IO}	Isolation resistance, input to output [5]	V_{IO} = 500V, T_A = 25°C	$> 10^{12}$	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	$> 10^{11}$	Ω
		V_{IO} = 500V at T_S = 150°C	$> 10^{9}$	Ω
	Pollution degree		2	

6.5 Insulation Specifications (continued)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
	Climatic category		40/125/21	
UL 1577 (Planned Certification Target)				
V_{ISO}	Withstand isolation voltage	V_{TEST} = V_{ISO} = 5000V_{RMS}, t = 60s (qualification); V_{TEST} = 1.2 × V_{ISO} = 6000V_{RMS}, t = 1s (100% production)	5000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed-circuit board are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the maximum operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air to determine the surge immunity of the package. Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-terminal device.

6.6 Electrical Characteristics

Over operating temperature range (T_J = –40°C to 150°C), unless otherwise noted. All typical values at T_A = 25°C and V_{VIN} = 12V. External BOM components are listed in the pin description table.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY (Primary-side. All voltages with respect to GNDP)						
V_{VIN}	Input voltage range	Primary-side input voltage to GNDP. (VDD-COM)=18V; (COM-VEE)=4V; $P_{VDD-COM}$ = 0.3W; $P_{COM-VEE}$ = 0; T_A=85ºC.	5.5[(1)]	12	20	V
V_{VIN}	Input voltage range	Primary-side input voltage to GNDP. (VDD-COM)=18V; (COM-VEE)=4V; $P_{VDD-COM}$ = 1.3W; $P_{COM-VEE}$ = 0; T_A=85ºC.	8[(1)]	12	18	V
I_{VINQ}	VIN quiescent current, disabled	V_{ENA} = 0V; V_{VIN} = 5.5V-20V;			600	µA
I_{VINP_NL}	VIN operating current, enabled, No Load	V_{ENA} = 5V; V_{VIN} = 12V; (VDD-COM) = 18V, (COM-VEE)=5V, regulating; $I_{VDD-COM}$ = $I_{COM-VEE}$ = 0mA.			18	mA
I_{VINP_FL}	VIN operating current, enabled, Full Load	V_{ENA} = 5V; V_{VIN} = 12V; (VDD-COM) = 18V, (COM-VEE)=4V, regulating; $I_{VDD-COM}$ = 83mA; $I_{COM-VEE}$ =0		250		mA
UVLOP COMPARATOR (Primary-side. All voltages with respect to GNDP)						
$V_{VIN\_UVLO\_R}$	VIN analog undervoltage lockout rising threshold	Analog Comparator Always Active First	4	4.25	4.5	V
$V_{VIN\_ UVLO\_F}$	VIN analog undervoltage lockout falling threshold	Analog Comparator Always Active First	3.8	4.04	4.28	V
OVLOP COMPARATOR (Primary-side. All voltages with respect to GNDP)						
$V_{VIN\_OVLO\_R}$	VIN overvoltage lockout rising threshold		21.25	22	22.5	V
$V_{VIN\_OVLO\_F}$	VIN overvoltage lockout falling threshold		19.7	20.3	20.6	V
TSHUTP THERMAL SHUTDOWN COMPARATOR (Primary-side. All voltages with respect to GNDP)						
$T_{SHUT\_P\_R}$	Primary-side over-temperature shutdown rising threshold		150	165		°C
$T_{SHUT\_P\_HYST}$	Primary-side over-temperature shutdown hysteresis		10	20		°C
ENA INPUT PIN (Primary-side. All voltages with respect to GNDP)						

6.6 Electrical Characteristics (continued)

Over operating temperature range (T_J = –40°C to 150°C), unless otherwise noted. All typical values at T_A = 25°C and V_{VIN} = 12V. External BOM components are listed in the pin description table.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ENA_R}	Enable pin rising threshold	Rising edge	1.425	1.5	1.575	V
V_{ENA_F}	Enable pin falling threshold	Falling edge	1.282	1.35	1.418	V
I_{ENA}	Enable Pin Input Current	V_{ENA} = 5.0V		5	10	µA
PG OPEN-DRAIN OUTPUT PIN (Primary-side. All voltages with respect to GNDP)						
V_{PG_L}	PG output-low saturation voltage	Sink Current = 5mA			0.5	V
I_{PG_H}	PG Leakage current	V_{PG} = 5.5V			5	µA
PRIMARY-SIDE SOFT START						
t_{PG_Delay}	Deglitch time during soft start between VDD reaches regulation and Power-Good signal (PG) is issued.		8.2	9.5	10.7	ms
Primary-side Control (All voltages with respect to GNDP)						
f_{SW}	Switching frequency	V_{VIN} = 12V; V_{ENA} = 5V; (VDD-COM)=18V, (COM-VEE)=4V		16.5		MHz
t_{SSTO}	Primary-side soft-start time-out	Timer begins when VIN > UVLOP and ENA = High and reset when Power-Good pin indicates Good	30	38	46	ms
(VDD-COM) OUTPUT VOLTAGE (Secondary-side)						
V_{VDD}	(VDD – COM) output voltage range		15	18	20	V
V_{VDD_REG}	(VDD – COM) output voltage DC regulation accuracy	Secondary-side (VDD – COM) output voltage accuracy at FBVDD, over load, line and temperature range, externally adjust with external resistor divider, within SOA range.	-1.45		1.45	%
(VDD-COM) REGULATION HYSTERETIC COMPARATOR (Secondary-side)						
V_{FBVDD_REF}	Feedback regulation reference voltage rising threshold for (VDD – COM)		2.473	2.51	2.547	
V_{FBVDD_HYST}	Hysteresis at the FBVDD pin. The value represents peak-to-peak magnitude.		16	20	24	mV
(COM-VEE) REGULATION HYSTERETIC COMPARATOR (Secondary-side)						
V_{FBVEE_HYST}	Hysteresis at the FBVEE pin. The value represents peak-to-peak magnitude.		20	60	75	mV
(VDD-COM) UVLOs COMPARATOR (Secondary-side)						
$V_{VDD\_UVLOS\_R}$	(VDD – COM) undervoltage lockout rising threshold	Voltage from VDD to COM, rising	3.2	3.45	3.7	V
$V_{VDD\_UVLOS\_F}$	(VDD – COM) undervoltage lockout falling threshold	Voltage from VDD to COM, falling	3	3.25	3.5	V
(VDD-COM) OVLOs COMPARATOR (Secondary-side)						
$V_{VDD\_OVLOS\_R}$	(VDD – COM) over-voltage lockout rising threshold	Voltage from VDD to COM, rising	22.5	23	23.5	V
$V_{VDD\_OVLOS\_F}$	(VDD – COM) over-voltage lockout falling threshold	Voltage from VDD to COM, falling	21.7	22.2	22.7	V
(VDD-COM) UVP, UNDER -VOLTAGE PROTECTION COMPARATOR (Secondary-side)						
$V_{VDD\_UVP\_R}$	(VDD – COM) under-voltage protection rising threshold, V_{UVP} = V_{REF} × 90%	At FBVDD	2.175	2.25	2.35	V

6.6 Electrical Characteristics (continued)

Over operating temperature range (T_J = –40°C to 150°C), unless otherwise noted. All typical values at T_A = 25°C and V_{VIN} = 12V. External BOM components are listed in the pin description table.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{VDD\_UVP\_HYST}$	(VDD – COM) under-voltage protection hysteresis	At FBVDD		22		mV
(VDD-COM) OVP, OVER-VOLTAGE PROTECTION COMPARATOR (Secondary-side)						
$V_{VDD\_OVP\_R}$	(VDD – COM) over-voltage protection rising threshold, V_{OVP} = V_{REF} ×110%	At FBVDD	2.7	2.75	2.825	V
$V_{VDD\_OVP\_HYST}$	(VDD – COM) over-voltage protection hysteresis	At FBVDD		23		mV
(COM-VEE) Buck-Boost Converter (Secondary Side)						
V_{VEE_REG}	(COM-VEE) regulation accuracy	COM-VEE=2V, with 1% feedback resistance accuracy	-9.5		9.5	%
		COM-VEE=3V, 4V, 5V, with 1% feedback resistance accuracy	-4.5		4.5	%
		COM-VEE=6V, 7V, 8V, with 1% feedback resistance accuracy	-6.5		6.5	%
$V_{VEE\_OVLOS\_R}$	(COM-VEE) over-voltage lockout rising threshold	Voltage from COM to VEE, rising	8.8	9	9.2	V
$V_{VEE\_OVLOS\_F}$	(COM-VEE) over-voltage lockout falling threshold	Voltage from COM to VEE, falling	8.4	8.6	8.8	V
f_{SW_VEE}	Switching frequency of VEE converter	VDD-COM=18V, COM-VEE=4V, 3.3uH external inductor		3.2		MHz
I_{LIM}	Buck boost inductor current limit, out of BSW pin	Max current limit across conditions	0.235	0.261	0.287	A
I_{LIM}	Buck boost inductor current limit, out of BSW pin	VDD-COM=6V.	0.199	0.221	0.243	A
I_{LIM}	Buck boost inductor current limit, out of BSW pin	VDD-COM=18V	0.127	0.141	0.155	A
I_{LIM}	Buck boost inductor current limit, out of BSW pin	VDD-COM=25V	0.085	0.094	0.104	A
t_{VEE_SSTO}	Timeout threshold to determine if the VEE soft start is succesful		4.6	6.3	8	ms
(COM-VEE) UVP, UNDER -VOLTAGE PROTECTION COMPARATOR (Secondary-side)						
$V_{VEE\_UVP\_F}$	(COM – VEE) under-voltage protection falling threshold	COM-VEE=2V		83		%
		COM-VEE=5V		90		%
		COM-VEE=8V		92		%
$V_{VEE\_UVP\_HYST}$	(COM – VEE) under-voltage protection hysteresis	COM-VEE=5V		85		mV
(COM-VEE) OVP, OVER-VOLTAGE PROTECTION COMPARATOR (Secondary-side)						
$V_{VEE\_OVP\_R}$	(COM – VEE) over-voltage protection rising threshold	COM-VEE=2V		117		%
		COM-VEE=5V		110		%
		COM-VEE=8V		108		%
$V_{VEE\_OVP\_HYST}$	(COM – VEE) over-voltage protection hysteresis	COM-VEE=5V		84		mV
TSHUTS THERMAL SHUTDOWN COMPARATOR (Secondary-side)						
$T_{SHUT\_S\_R}$	Secondary -side over-temperature shutdown rising threshold		150	165		°C
$T_{SHUT\_S\_HYST}$	Secondary-side over-temperature shutdown hysteresis		10	20		°C
AUTO RESTART						

6.6 Electrical Characteristics (continued)

Over operating temperature range (T_J = –40°C to 150°C), unless otherwise noted. All typical values at T_A = 25°C and V_{VIN} = 12V. External BOM components are listed in the pin description table.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{RESTART}$	Primary-side auto-restart time	After secondary-side faults assert or soft-start time-out expires		160		ms
CMTI (Common Mode Transient Immunity)						
CMTI	Common Mode Transient Immunity	Static CMTI (Rising and falling)	250			V/ns
		Dynamic CMTI (Rising and falling)	250			V/ns
INTEGRATED TRANSFORMER						
N	Transformer effective turns ratio	Secondary side to primary side		2.43		

(1) See the $V_{VIN\_UVLO\_R}$ and $V_{VIN\_ UVLO\_F}$ electrical characteristics for the miminum operational V_{VIN}.

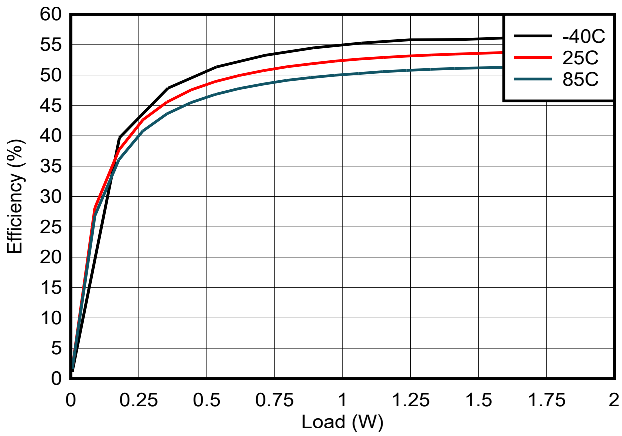
6.7 Safety Limiting Values

PARAMETER		TEST CONDITIONS	MAX	UNIT
I_S	Safety input rms current	$R_{\theta JA}$ = 52.3°C/W, V_{VIN} = 18V, T_J = 150°C, T_A = 25°C, P_{OUT} = 1.5W (1) (2)	220	mA
		$R_{\theta JA}$ = 52.3°C/W, V_{VIN} = 8V, T_J = 150°C, T_A = 25°C, P_{OUT} = 1.2W (1) (2)	450	mA
P_S	Safety power dissipation (input power - output power)	$R_{\theta JA}$ = 52.3°C/W, T_J = 150°C, T_A = 25°C (1) (2)	2.39	W
T_S	Safety temperature	(1) (2)	150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power dissipation respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.
(2) The junction-to-air thermal resistance, $R_{\theta JA}$, in the Thermal Information table is that of a device installed on a high-K JEDEC test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter: $T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device. $T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.

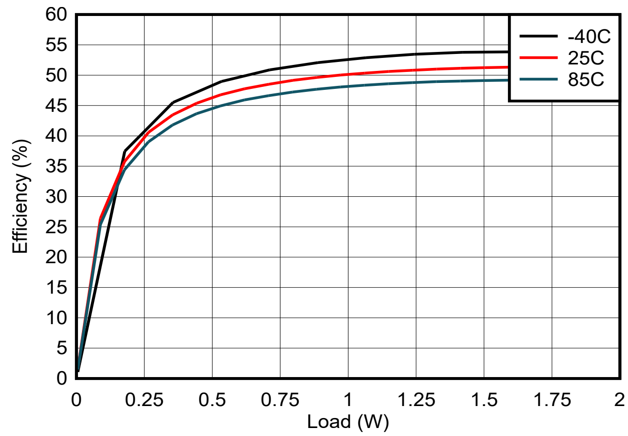
6.8 Typical Characteristics

As shown in Figure 6-4, Figure 6-5, and Figure 6-6, the VDD-COM maximum recommended average power safe operating area (SOA) at each V_{IN} is determined by the lower value of the 3W limit (dotted line) and the corresponding thermal derating curve (solid line) at that input voltage. It is not recommended to operate at an ambient temperatures higher than 125°C. As shown in the Electrical Characteristics table, the typical T_{SHUT} value is 165°C, and minimal T_{SHUT} value is 150°C. The SOA derating curves with T_{SHUT} = 150°C are provided below. The thermal derating power is acquired with the EVM shown in the "Layout" section. The total power requirement in the application can be calculated by the last row of "design requirements" section of the UCC34141 calculator tool , as another design supporting document besides this data sheet.



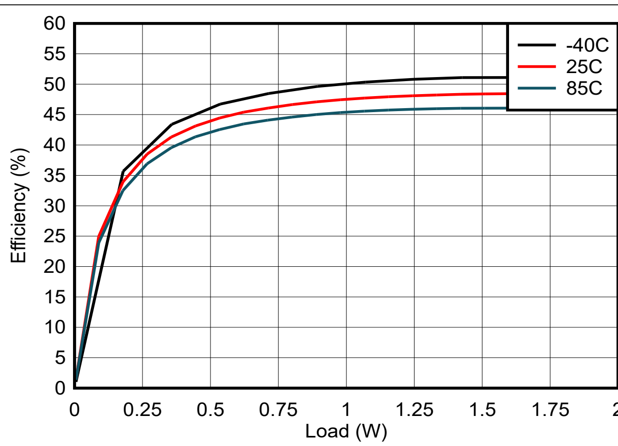
V_{IN} = 12V $V_{VDD-COM}$ = 18V $V_{COM-VEE}$ = 5V
No Load on $V_{COM-VEE}$

Figure 6-1. Efficiency vs. Load on $V_{VDD-COM}$



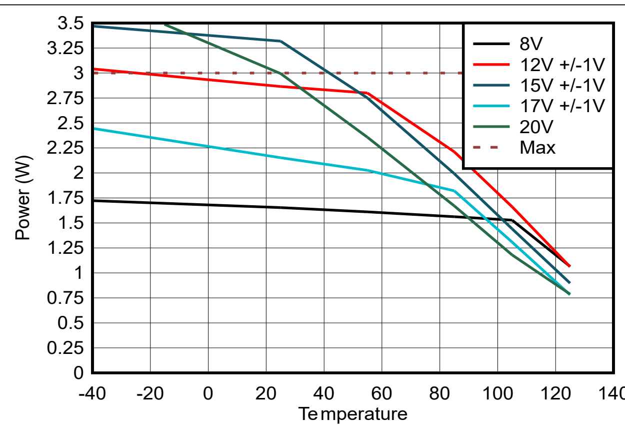
V_{IN} = 15V $V_{VDD-COM}$ = 18V $V_{COM-VEE}$ = 5V
No Load on $V_{COM-VEE}$

Figure 6-2. Efficiency vs. Load on $V_{VDD-COM}$



V_{IN} = 17V $V_{VDD-COM}$ = 18V $V_{COM-VEE}$ = 5V
No Load on $V_{COM-VEE}$

Figure 6-3. Efficiency vs. Load on $V_{VDD-COM}$

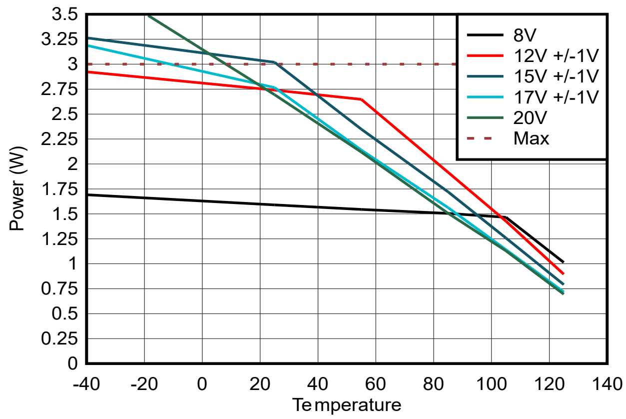


$V_{VDD-COM}$ = 20V $V_{COM-VEE}$ = 5V No Load on $V_{COM-VEE}$

Figure 6-4. SOA Derating Curves for Pre-regulated Input Voltages

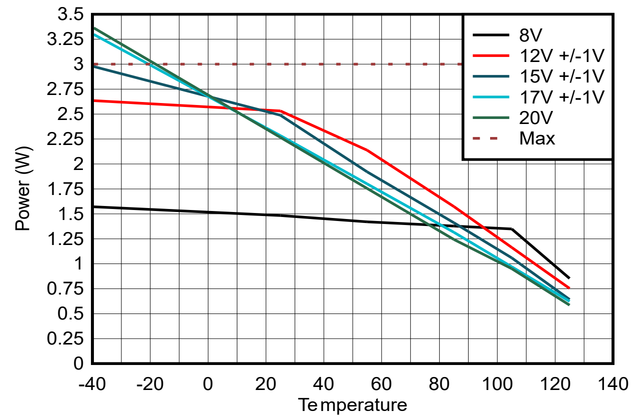
6.8 Typical Characteristics (continued)

As shown in Figure 6-4, Figure 6-5, and Figure 6-6, the VDD-COM maximum recommended average power safe operating area (SOA) at each V_{IN} is determined by the lower value of the 3W limit (dotted line) and the corresponding thermal derating curve (solid line) at that input voltage. It is not recommended to operate at an ambient temperatures higher than 125°C. As shown in the Electrical Characteristics table, the typical T_{SHUT} value is 165°C, and minimal T_{SHUT} value is 150°C. The SOA derating curves with T_{SHUT} = 150°C are provided below. The thermal derating power is acquired with the EVM shown in the "Layout" section. The total power requirement in the application can be calculated by the last row of "design requirements" section of the UCC34141 calculator tool , as another design supporting document besides this data sheet.



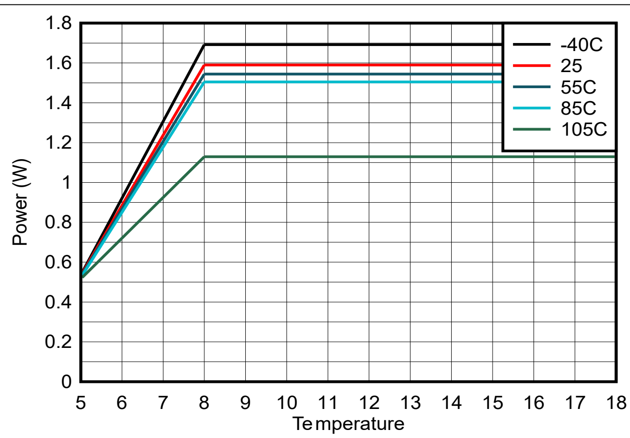
$V_{VDD-COM}$ = 18V $V_{COM-VEE}$ = 5V No Load on $V_{COM-VEE}$

Figure 6-5. SOA Derating Curves for Pre-regulated Input Voltages



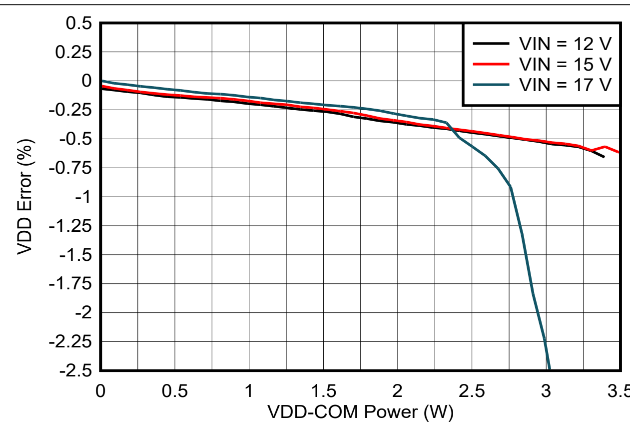
$V_{VDD-COM}$ = 15V $V_{COM-VEE}$ = 7V No Load on $V_{COM-VEE}$

Figure 6-6. SOA Derating Curves for Pre-regulated Input Voltages



$V_{VDD-COM}$ = 18V $V_{COM-VEE}$ = 5V No Load on $V_{COM-VEE}$

Figure 6-7. SOA Derating Curves with Wide Input Voltage for Direct Battery Connection



$V_{VDD-COM}$ = 18V $V_{COM-VEE}$ = 5V No Load on $V_{COM-VEE}$

Figure 6-8. Typical Load Regulation

7 Detailed Description

7.1 Overview

UCC34141 is an isolated power module designed for applications that have limited board space and require more integration. The device is also an excellent choice for very-high voltage applications, where power transformers meeting the required isolation specifications are bulky and expensive. The low-profile, low-center of gravity, and low weight provides a higher vibration tolerance than systems using large bulky transformers. The device is easy-to-use and provides flexibility to adjust both positive and negative output voltages as needed when optimizing the gate voltage for maximum efficiency while also protecting gate oxide from over-stress with its tight voltage regulation accuracy.

The device integrates a high-efficiency, low-emissions, isolated DC/DC converter for powering the gate drive of SiC or IGBT power devices in traction inverter motor drives, on-board-charger (OBC), server telecom rectifiers, industrial motor drives, or other high voltage DC/DC converters. This DC/DC converter can provide greater than 1.5W of power at an ambient temperature of 85C.

The integrated DC/DC converter uses switched mode operation and proprietary circuit techniques to reduce power losses and boost efficiency. Specialized control mechanisms, clocking schemes, and the use of an on-chip transformer provide high efficiency and low radiated emissions.

The integrated transformer provides power delivery throughout a wide temperature range while maintaining a 5000V_{RMS} isolation, and an 1202V_{RMS} continuous working voltage. The low isolation capacitance of the transformer provides high CMTI allowing fast dv/dt switching and higher switching frequencies, while emitting less noise.

The VIN supply is provided to the primary-side power controller that switches the input stage connected to the integrated transformer. Power is transferred to the secondary-side output stage, and regulated to a level set by the resistor divider connected between the VDD pin and the FBVDD pin with respect to the COMA pin. The output voltage is adjustable with external resistor divider allowing a wide (VDD – COM) range.

A fast hysteretic feedback burst control loop monitors (VDD – COM) and verifies the output voltage is kept within the hysteresis with low overshoot and undershoot during load and line transients. The burst control loop enables efficient operation across full load and allows a wide output voltage adjustability throughout the whole V_{VIN} range. The undervoltage lockout (UVLO) protection monitors the input voltage pin, VIN, with hysteresis and input filter ensuring robust system performance under noisy conditions. The overvoltage lockout (OVLO) protection monitors the input voltage pin, VIN, to protect against over-voltage stress by disabling switching and reducing the internal peak voltage. Controlled soft-start timing, provided throughout the full power-up time, limits the peak input inrush current while charging the output capacitor and load.

The UCC34141 can also provide a second output rail, VEE, that is used as a negative bias for the gate drivers allowing quicker turn-off switching for the IGBTs and protecting from unwanted turn-on during the fast switching of SiC devices. VEE has a simple, yet fast and efficient, bias controller to regulate the negative rail during gate driver PWM switching. The COM pin is the reference for the negative VEE rail, and connects to the source of SiC device or emitter of an IGBT device.

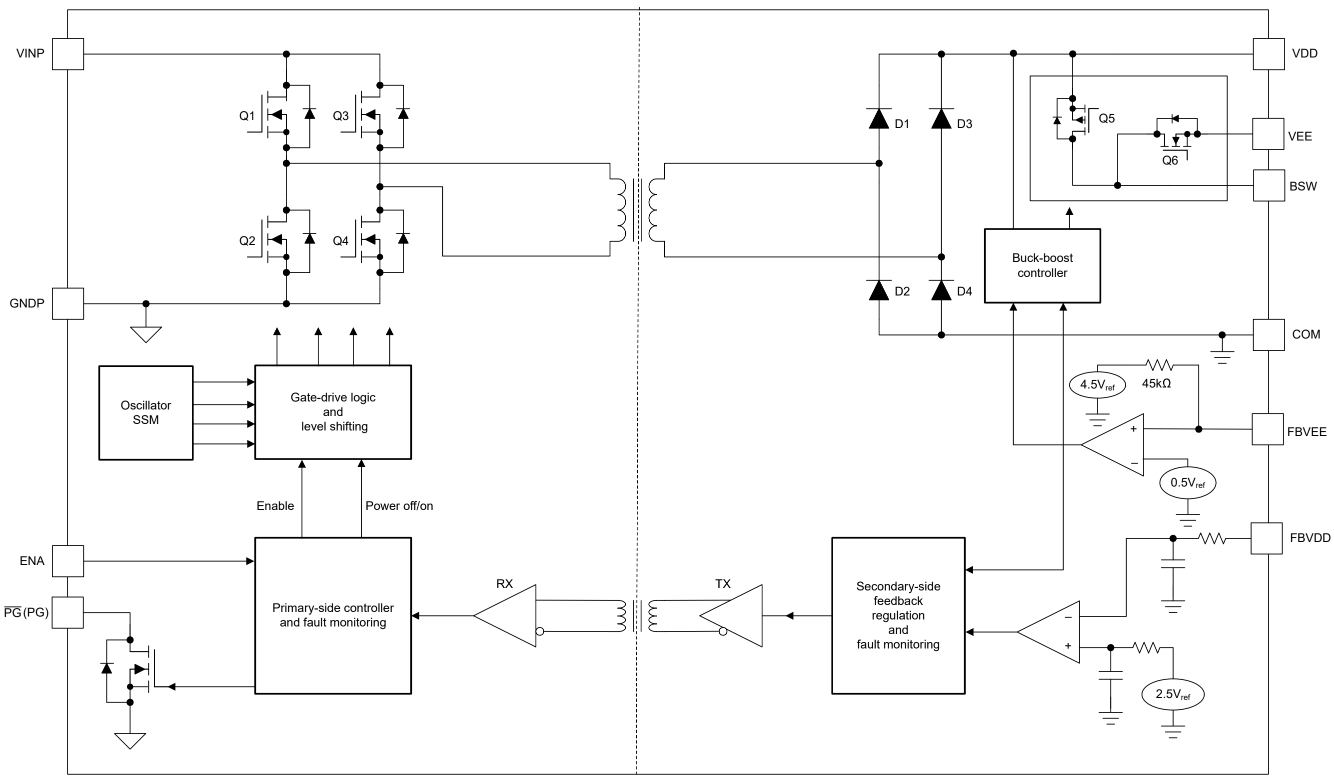
A fault detection and status pin, $\overline{PG}$(PG), provides a mechanism for the host controller to monitor the status of the DC/DC converter and provide proper sequencing of power and PWM control signals to the gate driver. Fault protection includes undervoltage, overvoltage, over-temperature shutdown, and isolated channel communication interface watchdog timer.

The typical soft-start ramp-up time is shorter than t_{SSTO}, and varies based on input voltage, output voltage, output capacitance, and load. If either output is shorted or over-loaded, the device is not able to power-up within the t_{SSTO} soft-start time, so the device shuts down. The fault response of the device varies based on the part number as listed in Table 4-1. For latch-off operation, the device shuts down and latches-off for protection and can be reset by toggling the ENA pin or resetting V_{VIN}. For auto-restart operation a timer is enabled after shutdown, and a new power up sequence starts after $t_{RESTART}$. If the fault has been removed, the part soft-starts to regulation successfully. If the fault condition remains, the part shuts down again and attempts another auto-restart. The device can continuously operate safely in hiccup mode as long as the fault occurs.

The UCC34141 has a Power-Good indicator with active polarity either High or Low based on the he part number as listed in Table 4-1. The output load must be kept low until start-up is complete and Power-Good pin becomes Active. For successful soft-start, do not apply a heavy load to (VDD – COM) or (COM – VEE) outputs until the Power-Good pin has indicated Active status.

The Power-Good status indicator allows the system to wait to apply any additional loading such as gate driver PWM until both (VDD – COM) and (COM – VEE) outputs have reached the regulation.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Power Stage Operation

The UCC34141 module uses a soft-switching full-bridge converter on the primary-side and a passive full-bridge rectifier on the secondary-side. The small integrated transformer operates with a high switching frequency to reduce the size for integrating into the 16-pin SSOP package. The power stage switching frequency is within 16.5MHz to 27MHz. The power stage switching frequency is determined by input voltage with a feed-forward control as illustrated by the figure below. Adaptive spread spectrum modulation (ASSM) is used to reduce emissions. Zero voltage switching (ZVS) operation is maintained to reduce switching power losses.

UCC34141 can be configured either as a single output converter, VDD to COM only, or a dual-output converter, VDD to COM and COM to VEE, where the COM to VEE supply is derived from VDD by an inverting buck-boost.

These two outputs are controlled independently through hysteretic control.

7.3.1.1 VDD-COM Voltage Regulation

The VDD output is the main output of the module. The power stage operation is controlled by a hysteretic comparator that detects when the FBVDD pin voltage is above or below the internal reference voltage V_{FBVDD_REF}. The FBVDD voltage is by the voltage divider between R_{FBVDD_TOP} and R_{FBVDD_BOT}. When FBVDD voltage stays below the turn-off threshold, the power stage operates in burst on state, delivering power to the secondary side and the VDD voltage increases. After FBVDD reaches the turn-off threshold, the power stage turns off. With the power stage off the VDD output capacitors supply the load, and VDD drops. After FBVDD voltage drops below the turn-on threshold, the power stage is turned on again. With the accurate voltage reference and hysteresis control, the VDD output voltage can be regulated with an accuracy of V_{VDD_REG}.

To improve the noise immunity, a small capacitor C_{FBVDD} of 220pF must be added between FBVDD and COMA pins. In an environment with high electro-magnetic noise, higher feedback decoupling capacitance C_{FBVDD}, and lower feedback resistance R_{FBVDD_TOP} and R_{FBVDD_BOT} values can be selected to further improve the noise immunity of the VDD feedback loop.

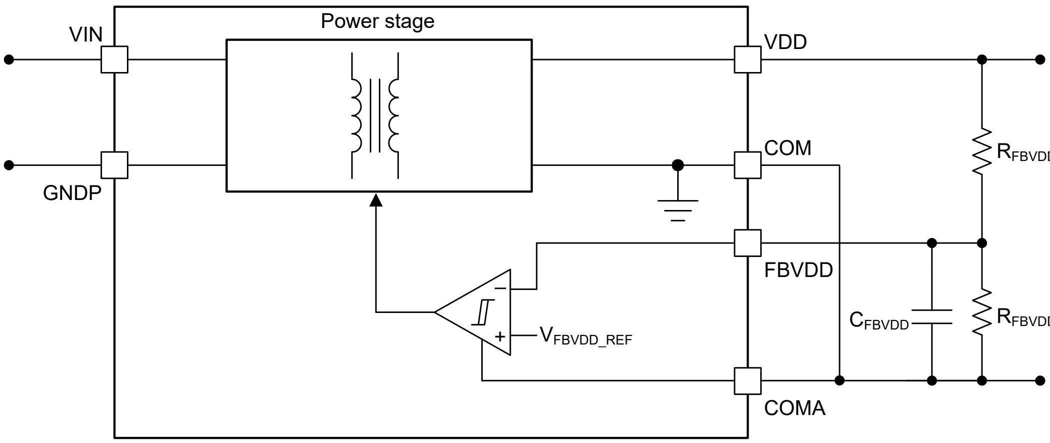


Figure 7-1. VDD-COM Voltage Regulation Functional Block Diagram

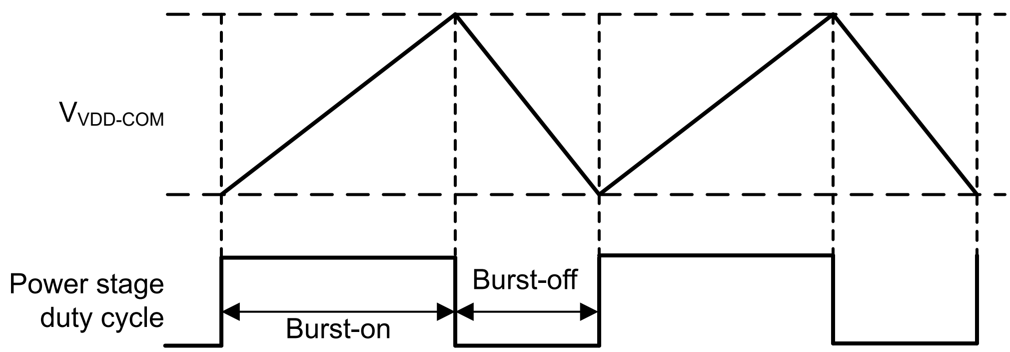


Figure 7-2. Concept of VDD-COM Regulation Scheme

7.3.1.2 COM-VEE Voltage Regulation

An internal buck-boost converter generates the regulated negative VEE voltage. The buck-boost converter operation is determined by the sensed VEE voltage on FBVEE pin as described in theSection 8.2.2.2 section. With an internal 45k resistor and a 4.5V reference voltage, VEE voltage can be programed and regulated from between -2V to -8V.

The buck-boost converter is controlled by an integrated hysteresis voltage feedback loop for COM-to-VEE voltage regulation and an integrated current control loop for cycle-to-cycle current limit. When FBVEE voltage stays below the turn-off threshold, the buck-boost converter operates with peak current mode control. The inductor current increases at the beginning of a switching cycle until it reaches the peak current limit, then returns to zero. In normal operation, the converter operates in boundary conduction mode, but can enter continuous conduction mode during start-up. As the peak current of the buck-boost is limited to less than I_{LIM}, the chosen inductor must have a saturation current above I_{LIM}. The peak current limit, I_{LIM}, is optimized based on VDD voltage, so that considering the overshoot due to the control loop delay at different VDD voltages, the maximum inductor current does not exceed the maximum I_{LIM} at the condition without VDD feedforward. A higher VDD voltage leads to a bigger overshoot, and thus results in a lower I_{LIM} value with VDD feedforward control for compensation. The recommended inductor selection is between 3.0µH and 10.0µH. The typical switching frequency is f_{SW_VEE} under the conditions listed in the Electrical Characteristics table.

After the FBVEE voltage reaches the turn-off threshold, the buck-boost converter turns off. After the FBVEE voltage drops below the turn-on threshold due to the load current, the buck-boost converter is turned on again. With the accurate voltage reference and hysteresis control, the VEE output voltage can be regulated with ≤5% accuracy.

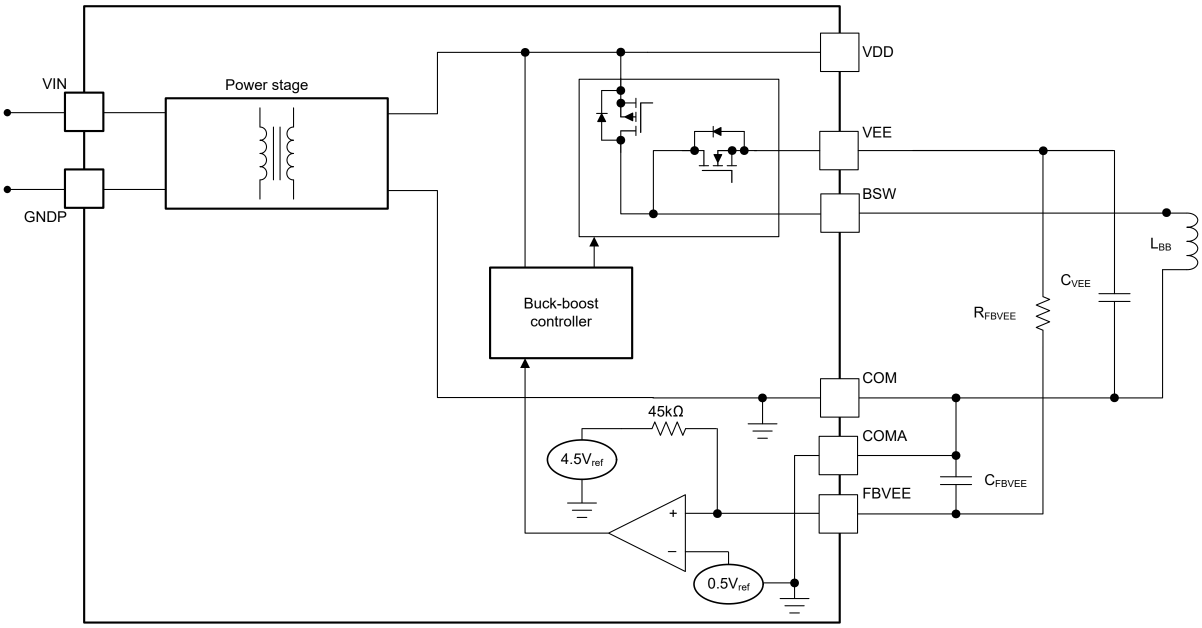


Figure 7-3. COM-VEE Voltage Regulation Functional Block Diagram

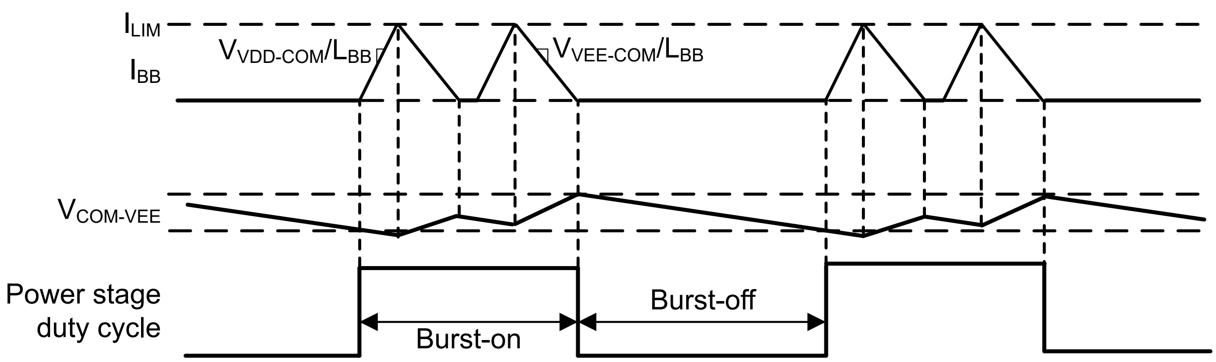


Figure 7-4. Concept of COM-VEE Regulation Scheme

7.3.1.3 COM-VEE Output Capability

The maximum output current and output power capability of the VEE buck-boost converter at different VDD-COM and COM-VEE voltages are shown in Figure 7-5 and Figure 7-6. The power capabilities can also be calculated in the UCC34141 calculator tool , as another design supporting document besides this data sheet. The power module has two independent output power capabilities: one is of VDD-COM output as shown by the SOA curves in the Typical Characteristics section, and the other one is of COM-VEE output as shown in this section. Excessive output power requirement out of either of the two output rails can cause an output undervoltage protection and shutdown of the device.

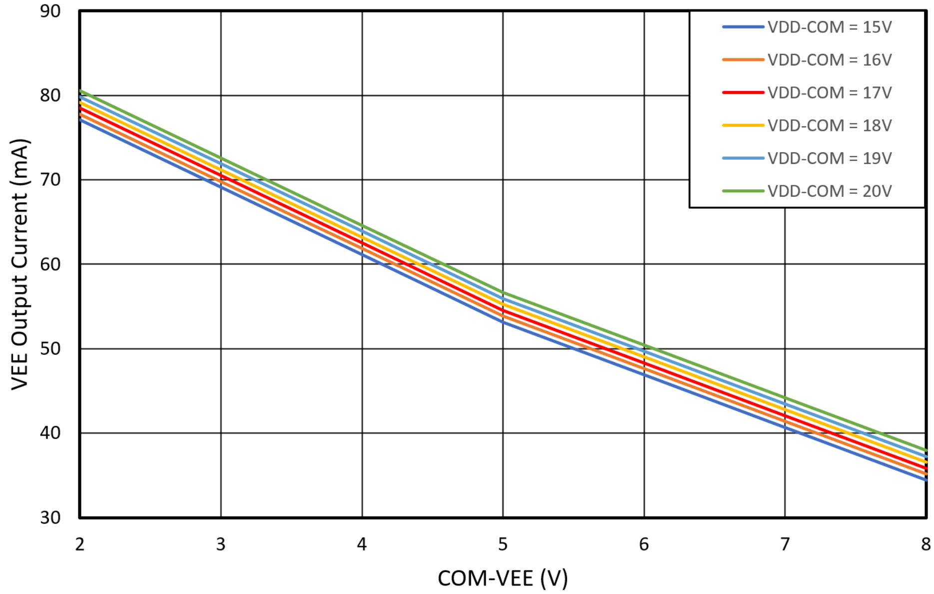


Figure 7-5. Output Current Capability of VEE Buck-Boost Converter at Different VDD-COM and VEE-COM Voltages

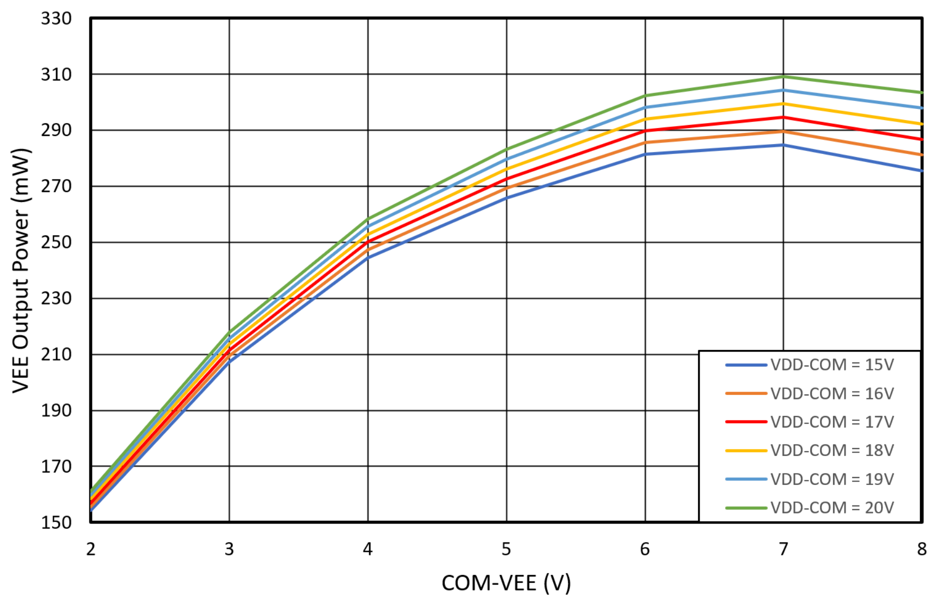


Figure 7-6. Output Power Capability of VEE Buck-Boost Converter at Different VDD-COM and VEE-COM Voltages

7.3.2 Output Voltage Soft Start

UCC34141 has soft-start mechanism that establishes a smooth and fast soft-start operation with minimum input inrush current. The output voltage soft-start diagram is shown in the figure below. After the input voltage is higher than the VIN_UVLO threshold, and the ENA signal is pulled high, the soft-start sequence starts with a primary duty cycle open loop control. The power stage operates with a fixed burst frequency with an incremental increasing duty cycle starting at 6.5%. The rate of change of the duty cycle is pre-programmed in part to reduce the input inrush current while building the output voltage VDD. The primary side limits the maximum duty cycle to 62.5% during this phase until the secondary side VDD voltage passes VDD_UVLO before releasing this duty cycle limit. This limit establishes minimum input current in case the device starts on a short circuit and the VDD does not build up. Once the VDD reaches the regulation range, the duty cycle is no longer determined from the primary side controller but instead VDD hysteretic control is active to tightly regulate the output voltage within the defined hysteresis band.

When VDD passes the UVLO threshold $V_{VDD\_UVLOS\_R}$, a FBVEE status check is performed, and then a single inductor current pulse generates for BSW pin fault detection.

The VEE soft start begins after the VDD rail capacitors are charged and VDD reaches regulation. During soft start the VEE peak current limit is reduced while the VEE voltage is less than 0.5V. When VEE voltage is higher than 0.5V the inductor peak current limit is set to the I_{LIM} value.

To establish that VEE reaches VEE_UVP threshold within t_{VEE_SSTO} period, the sum of the COM-to-VEE output capacitance at gate driver side (C_{VEE_GD}) and at isolated-converter bias side (C_{VEE_BIAS}) must not exceed a maximum allowed value. The maximum allowed value at gate driver side (C_{VEE_GD}) is available in the UCC34141 calculator tool as another design supporting document besides this datasheet. Equation 1 determines the maximum allowed capacitor value is shown as below. In Equation 1, $I_{LOAD\_SS\_VEE}$ represents the quiescent current of output load during VEE soft start.

$$C_{VEE\_GD} \le \frac{t_{VEE\_SSOT\_min}}{\frac{V_{VEE\_SS}}{I_{VEE\_Phase1} - I_{LOAD\_SS\_VEE}} + \frac{V_{VEE} - V_{VEE\_SS}}{I_{VEE\_Phase2} - I_{LOAD\_SS\_VEE}}} - C_{VEE\_BIAS} \tag{1}$$

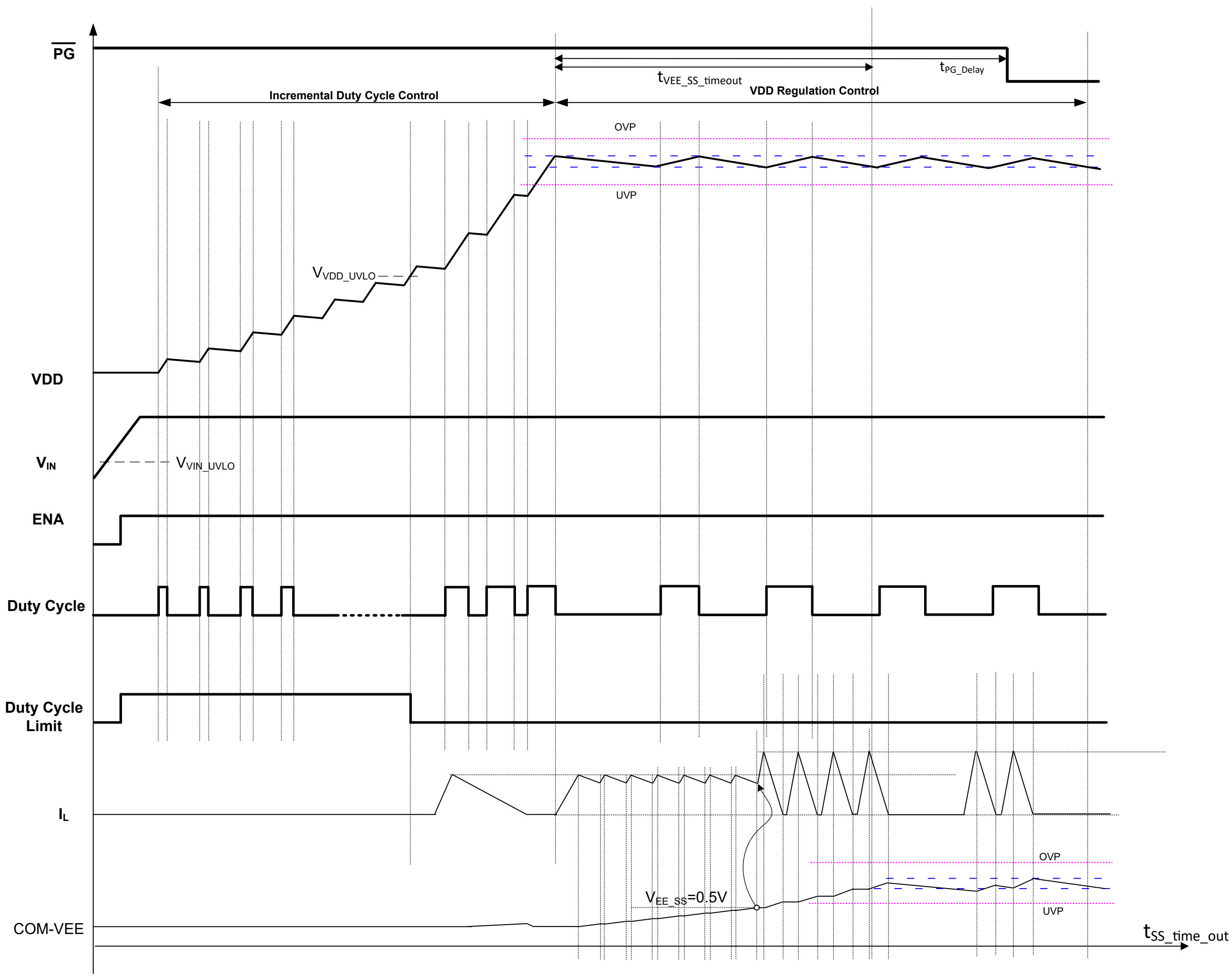


Figure 7-7. Output Voltage Soft-Start Diagram with Power-Good Active LOW

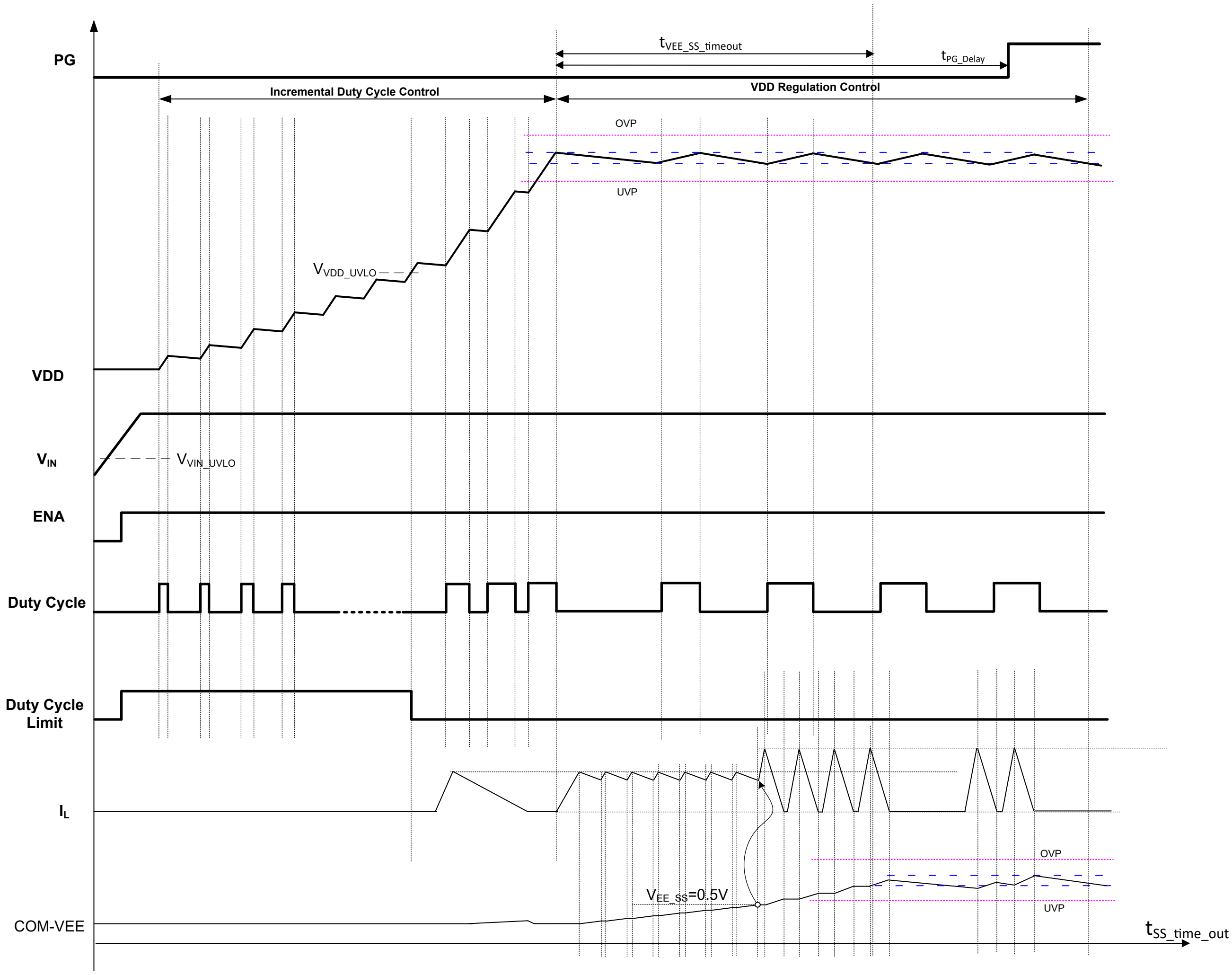


Figure 7-8. Output Voltage Soft-Start Diagram with Power-Good Active HIGH

7.3.3 ENA and Power-Good

The ENA input pin and Power-Good output pin on the primary-side support both TTL and CMOS logic levels in 5V or 3.3V domain. The active-high enable input (ENA) pin is used to turn-on the isolated DC/DC converter. After ENA pin voltage rises above the enable threshold V_{ENA_R}, the power module starts switching, goes through the soft-start process and delivers power to the secondary side. After ENA pin voltage falls below the disable threshold V_{ENA_F}, UCC34141 is disabled, and the internal power stage stops switching.

For Latch-off devices, the ENA pin is also used to reset the device after it enters the protection safe-state mode. After a detected fault, the protection logic latches off and place the device into a safe state. To reset the part, the system must toggle the ENA-pin voltage below V_{ENA_F} for longer than $t_{EN\_LO\_RST}$, then toggle back up above V_{ENA_R} to exit the latch-off mode and begin the soft-start sequence. There is a built in delay after a fault detection before the device reenables, $t_{EN\_LO\_DLY}$. Toggling ENA before $t_{EN\_LO\_DLY}$ after a fault is detected does not reset the fault.

The ENA pin can also be used to implement a programmable input UVLO by using an external resistor divider between VIN and ENA pins. For the device and application with relatively low input UVLO and relatively high V_{IN}, when there is a slow V_{IN} ramp during start-up, the relatively low transformer turns-ratio is not able to generate enough power to charge up the output capacitor and therefore fails the start-up. This issue can be solved by adding a resistor divider between VIN, ENA, and GNDP pins to program the ENA signal time and override the internal input UVLO. The programmable input UVLO feature can also be used to sequentially start-up multiple integrated DC/DC modules, by adding delay capacitors between ENA and GNDP pins to program the delay time between each power module. Specifically, the ENA1 signal can enable one module or one grouped modules, while the delayed ENA2 signal from ENA1 can sequentially enable another module or another grouped modules. For the application where ENA1 and ENA2 are too far away for the R_{ENA2} routing, the RC circuitry for ENA1 can be duplicated at the ENA pin of each module to enable sequential startup. If the sequential power up is not needed, multiple modules can share the same resistor divider to program input UVLO threshold. To facilitate the implementation, the recommended resistor and capacitor values are available in the UCC34141 calculator tool .

If a single fault event on the resistor divider needs to be considered, for example, the single bottom resistor is failed open, the risk of exceeding the 7V absolute maximum of ENA pin must be mitigated at the application level. Two approaches can be applied: one option is adding an external Zener diode on ENA pin; another option is to split the bottom resistance into two resistor components.

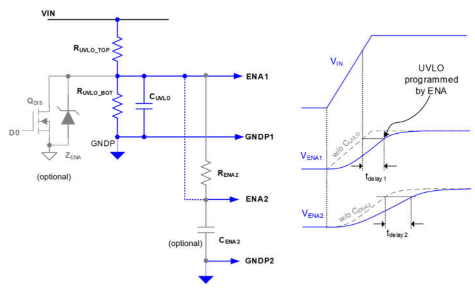


Figure 7-9. Input UVLO Programming Circuit and Operation Principle

The Power-Good is an open-drain output which active state indicates when the module has no fault and the output voltages are within ±10% of the output voltage regulation set points. To account for the maximum current sinking capability of the internal pull-down MOSFET < 5mA, a pull-up resistor (> 1kΩ) from Power-Good pin to either a 5V or 3.3V logic rail is recommended. Higher resistance reduces the quiescent current in normal logic state of Power-Good pin.

During power up, when VDD voltage reaches regulation, two timers of t_{VEE_SSTO} and t_{PG_Delay} are started. If VEE does not pass VEE_UVP threshold within t_{VEE_SSTO} period, a fault is triggered to shut down the part and flag a failed soft start. If no fault is detected within the t_{PG_Delay} period, Power-Good signal changes to active status to indicate a Power-Good state. If VDD voltage does not reach regulation within t_{SSTO} period, a fault is triggered to shut down the part and flag a failed soft start.

Once a fault is triggered to shut down the part, an auto-restart timer of $t_{RESTART}$ starts afterwards, and the part attempts to auto-restart after that timer expires. If the fault condition remains, the part shuts down again and attempt another auto-restart. The device can continuously operate safely in hiccup mode as long as the fault occurs.

For Active-Low Power-Good polarity, there is a voltage drop in the $\overline{PG}$ signal during start up, due to the parasitic capacitance between the adjacent VIN pin and $\overline{PG}$ pin. This capacitive coupling generates a pulling current into the $\overline{PG}$ pin and therefore leads to a voltage drop across the pull-up resistor and thus a voltage drop on $\overline{PG}$ signal during start up. A 4.99kΩ pull-up resistor, and a 1µF decoupling capacitor connecting $\overline{PG}$ pin and ground are recommended to diminish the voltage drop during start up.

For Active-High Power-Good polarity, the PG is grounded during the start up, so a small decoupling capacitor in the range from 0.1µF - 1µF with a 10kΩ pull-up resistor can be selected. The active-high setting allows an easy group fault reporting by direct connection of the PG pin signals from multiple DC/DC modules, because the combined PG signal stays low when a power-bad condition in any one (or more) module(s) turns-on the pull-down FET; during power-good condition conversely, the combined PG signal stays high because the pull-down FETs of all the DC/DC modules stay off

7.3.4 Protection Functions

UCC34141 is equipped with a full feature of protection functions, including input undervoltage lockout, overvoltage lockout, output undervoltage, overvoltage, and over-temperature. The input undervoltage and overvoltage lockout protections have an auto recovery response. All other protections have a fault response based on the part number as listed in Table 4-1. For the latch-off-response, protections are triggered, the converter enters a latch-off state, and stops switching. The latch is reset by either toggling the ENA pin Off then On, or by lowering the V_{VIN} voltage below the $V_{VIN\_UVLO\_F}$ threshold, and then above the $V_{VIN\_UVLO\_R}$ threshold. For auto-restart response, once the part shuts down, a $t_{RESTART}$ timer starts and then the part attempts an auto-restart with a new soft-start sequence as shown in Figure 7-10. If the fault has been removed, the part soft-starts to regulation successfully. If the fault condition remains, the part shuts down again and attempt another auto-restart. The device can continuously operate safely in hiccup mode as long as the fault occurs.

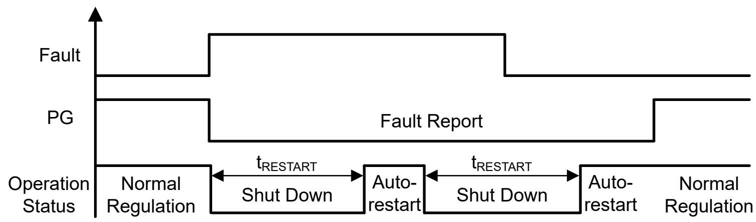


Figure 7-10. Auto-Restart Operation with PG Active High

7.3.4.1 Input Undervoltage Lockout

The UCC34141 enters input undervoltage lockout when V_{VIN} voltage becomes lower than the UVLO threshold $V_{VIN\_UVLO\_F}$. In UVLO mode, the converter stops switching. After VIN pin voltage falls lower than the $V_{VIN\_UVLO\_F}$, UCC34141 resets all the protections. And then, after the V_{VIN} voltage rises above the UVLO threshold $V_{VIN\_UVLO\_R}$, the converter is enabled. Depending on the ENA pin voltage, the converter starts switching, going through the soft-start sequence, or enter disable mode, waiting for ENA pin voltage to go high.

7.3.4.2 Input Overvoltage Lockout

The input overvoltage lockout protection is used to notify the system of an overvoltage event. When the VIN pin voltage becomes higher than the input overvoltage lockout threshold $V_{VIN\_OVLO\_R}$, switching stops and the converter stops sending energy to the secondary side. Once V_{VIN} pin voltage drops below the recovery threshold $V_{VIN\_OVLO\_F}$ following an overvoltage lockout, depending on the ENA pin voltage, the converter starts switching, going through the soft-start sequence, or enter disable mode, waiting for ENA pin voltage to go high.

The input overvoltage lockout does not reset other latch-off protections.

7.3.4.3 Output Undervoltage Protection

There are two output undervoltage protection features. The first monitors the output voltage based on the FBVDD and FBVEE pin voltages. When the FBVDD pin voltage falls below the UVP threshold $V_{VDD\_UVP\_F}$, or the FBVEE pin voltage falls below the UVP threshold $V_{VEE\_UVP\_F}$, the undervoltage protection is activated. UCC34141 stops switching, and the Power-Good pin change to non-active status. The second undervoltage monitor, UVLO, directly monitors the VDD voltage at the VDD pin. When the VDD pin voltage drops below $V_{VDD\_UVLOS\_F}$ UCC34141 stops switching, and the Power-Good pin change to non-active status

During soft start, the output voltages rise from zero volts, thus, both FBVDD and FBVEE pin voltages are below the UVP thresholds. The UVP is disabled during the soft start. If the pin voltage cannot reach the UVP recovery thresholds ($V_{VDD\_UVP\_R}$, $V_{VEE\_UVP\_R}$) after the soft start completes, undervoltage protection is activated, the UCC34141 stops switching, and the Power-Good pin change to non-active status.

7.3.4.4 Output Overvoltage Protection

The UCC34141 senses the output voltage through FBVDD and FBVEE pins to control the output voltage. To prevent the output voltage from getting too high, damaging the load or UCC34141 device, the UCC34141 is equipped with the output overvoltage protection. There are two levels of overvoltage protection based on the feedback pin voltage, and the output voltage.

During the normal operation, because of load transient, the output voltages can exceed the regulation level. Based on the pin voltages on FBVDD and FBVEE, after the voltage exceeds the threshold, $V_{VDD\_OVP\_R}$, or $V_{VEE\_OVP\_R}$, the converter stops switching immediately.

In the case of a system fault involving a short or open of the external feedback resistors, the voltage divider can malfunction resulting in the wrong output voltage information. As a result, the control loop regulates the output voltages at a wrong voltage level. For failures of this type UCC34141 is also equipped with a fail-safe overvoltage protection. After the VDD-COM or COM-VEE voltage exceeds the overvoltage protection threshold $V_{VDD\_OVLOS\_R}$ or $V_{VEE\_OVLOS\_R}$, the converter shuts down immediately. This fail-safe protection level is meant to protect UCC34141 rather than the load.

7.3.4.5 Output Short Circuit Protection

UCC34141 integrates short circuit protection for both the VDD and VEE rails. During power up,short circuit protection is accomplished through the primary side soft start timeout, t_{SSTO}. If VDD and VEE have not reached the regulation targets by the time t_{SSTO} expires the module stops switching and the Power-Good pin change to non-active status. During normal operation, if a short circuit condition occurs the output is protected by the UVLO and UVP features on VDD, and by a short circuit comparator on VEE that limits output current when COM-VEE is less than 0.5V.

7.3.4.6 Over-Temperature Protection

UCC34141 integrates the primary-side and secondary-side power stages, as well as the isolation transformer. The power loss caused by the power conversion causes the module temperature to increase above the ambient temperature. For the safe operation of the power module, the UCC34141 is equipped with over-temperature protection. Both the primary-side power stage, and the secondary-side power stage temperatures are sensed and compared to the over-temperature protection threshold. If the primary-side power stage temperature becomes higher than $T_{SHUT\_P\_R}$, or the secondary-side power stage temperature becomes higher than $T_{SHUT\_S\_R}$, the module enters over-temperature protection mode. The module stops switching and the Power-Good pin change to non-active status.

7.3.4.7 BSW Pin Faults Protection

UCC34141 has protection mechanism against BSW Pin faults during the soft-start period for the COM-VEE buck-boost converter.

In the case of BSW pin-open, when VDD voltage passes $V_{VDD\_UVLOS\_R}$ threshold, the part detects the first inductor current pulse width, which is the current ramp-up period until the peak current limit is hit. If the first inductor current pulse width is higher than the normal pulse width using largest inductance (>2.9μs), the BSW fault protection is triggered to disable the buck-boost switching. Then, the device stops switching after VDD soft start completion.

In the case of BSW pin-short to COM or VEE pin, the part detects the inductor current at the end of leading-edge-blank period. If the current is higher than the inductor peak current limit during soft-start, the BSW fault protection is triggered to disable the buck-boost switching. Then the device stops switching after VDD soft start completion.

7.4 Device Functional Modes

Depending on the input and output conditions, ENA pin voltage, as well as the device temperature, the UCC34141 operates in one of the below operation modes.

- Disable mode: In this mode, the module is off, waiting for ENA pin to go high to begin operation.
- Soft-start mode: In this mode, the module starts to deliver power to the secondary side. The primary-side operation duty cycle is raised gradually to reduce the stress to the module.
- Normal operation mode: In this mode, the module operates normally, delivering power to the secondary side.

- Protection mode, auto-recovery: In this mode the module is off due to the input UVLO or OVLO protection. After the input voltage fault is cleared, depending on the ENA pin voltage condition, it either becomes disabled mode if the ENA pin voltage is low, or it goes through soft-start mode to the normal operation mode.
- Protection mode, latched-off: In this mode the part is off due to other protections. The module remains off even the fault causing the protection is cleared. Recycling V_{VIN} operation must verify that the input voltage goes below the analog UVLO falling threshold ($V_{VIN\_UVLO\_F}$) first to reset the latch-off state, or the ENA pin is toggled Low (OFF) then High (ON).
- Protection mode, auto-restart after defined duration $t_{RESTART}$: In this mode, the part shuts down due to other protections. Once the part shuts down, a $t_{RESTART}$ timer starts and then the part attempts an auto-restart with a new soft-start sequence. If the fault has been removed, the part soft-starts to successfully regulate. If the fault condition remains, the part shuts down again and attempt another auto-restart. The device continuously operates safely in hiccup mode, as long as the fault occurs.

Table 7-1 lists the supply functional modes for this device. The ENA pin has an internal weak pull-down resistance to ground, but TI does not recommend leaving this pin open.

Table 7-1. Device Functional Modes

INPUT			OUTPUTS			OPERATION MODE
V_{VIN}	ENA	FAULT	$V_{(VDD – COM)}$ Isolated Output1	$V_{(COM – VEE)}$ Isolated Output2	Power-Good(1) (2) Open Drain	
$V_{VIN} < V_{VIN\_UVLO\_R}$	X	X	OFF	OFF	Non-Active Status	Protection mode, auto-recovery
$V_{VIN\_UVLO\_R} < V_{VIN} < V_{VIN\_OVLO\_R}$	LOW	X	OFF	OFF	Non-Active Status	Disable mode
$V_{VIN\_UVLO\_R} < V_{VIN} < V_{VIN\_OVLO\_R}$	HIGH	NO FAULT	Regulating at Setpoint	Regulating at Setpoint	Active Status	Normal operation
$V_{VIN\_UVLO\_R} < V_{VIN} < V_{VIN\_OVLO\_R}$	HIGH	YES FAULT	OFF	OFF	Non-Active Status	Protection mode, latched-off or auto-restart after $t_{RESTART}$
$V_{VIN} > V_{VIN\_OVLO\_R}$	X	X	OFF	OFF	Non-Active Status	Protection mode, auto-recovery

(1) For Power-Good active HIGH devices listed in Table 4-1: Active status PG = HIGH , Non-Active status PG = LOW .
(2) For Power-Good active LOW devices listed in Table 4-1: Active status $\overline{PG}$ = LOW , Non-Active status $\overline{PG}$ = HIGH.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

UCC34141 is designed for applications that have limited board space and desire more integration. This device is also an excellent choice for very high voltage applications, where power transformers that meet the required isolation specifications are bulky and expensive.

8.2 Typical Application

The following figures show the typical application schematics for the UCC34141 device configurations supplying an isolated load.

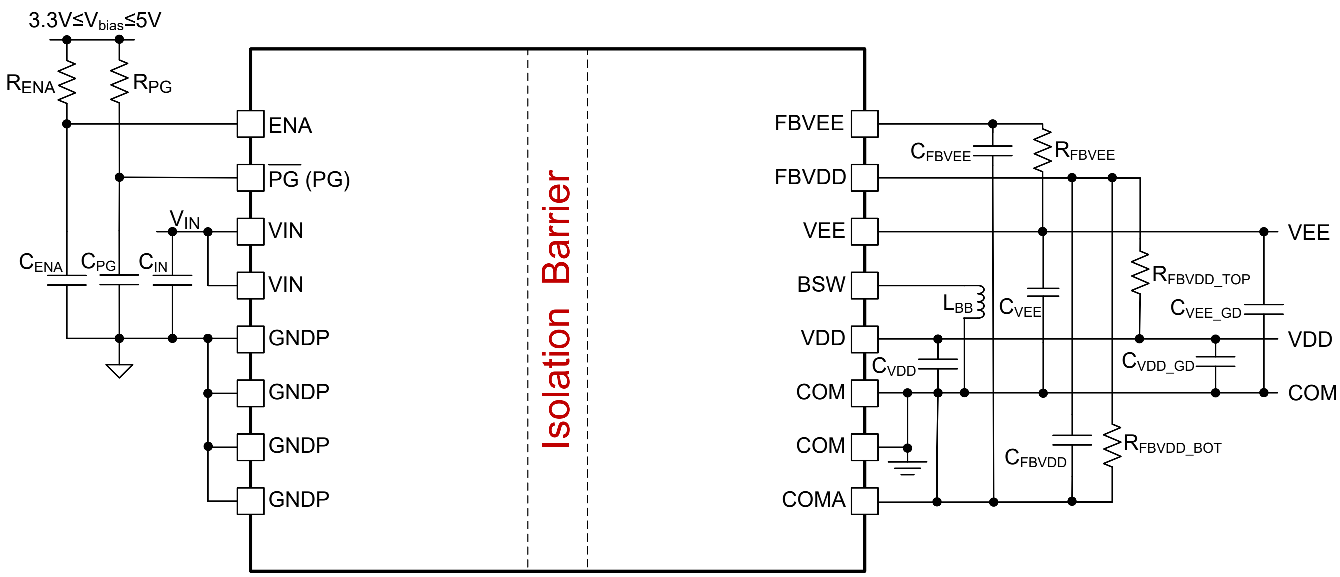


Figure 8-1. Dual Adjustable Output Configuration

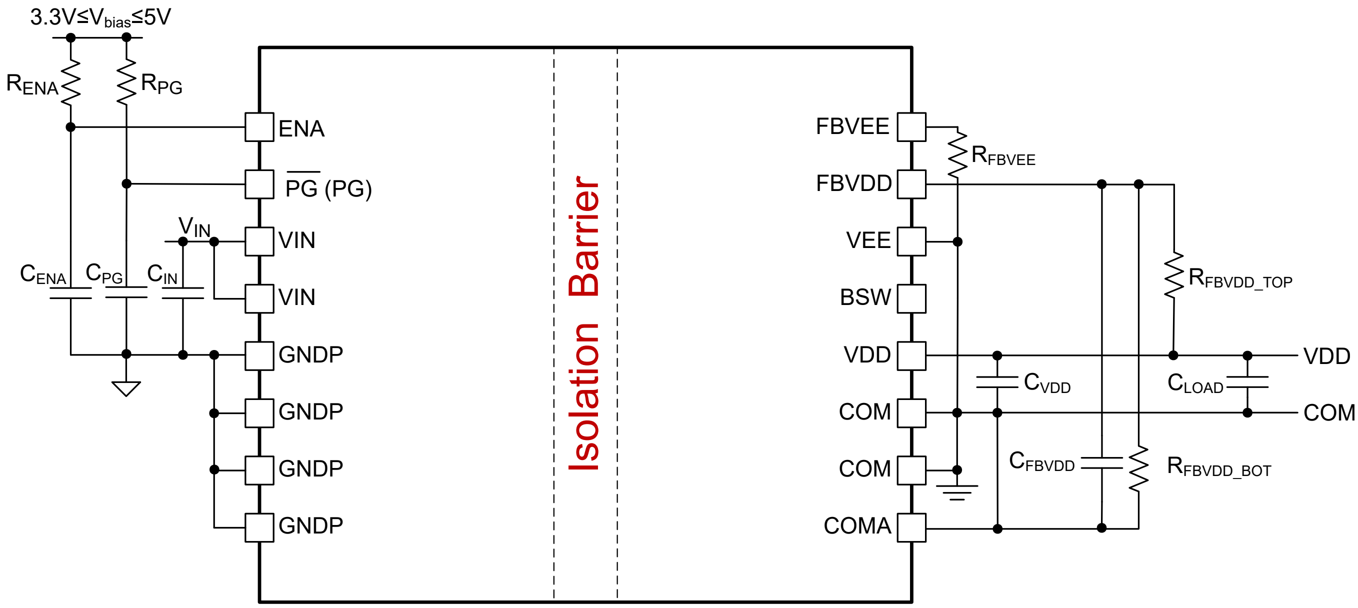


Figure 8-2. Single Adjustable Output Configuration

8.2.1 Design Requirements

Designing with the UCC34141 is simple. First, select single output or dual output. Determine the voltage for each output and then set the regulation through feedback resistors. The gate charge of the power device determines the amount of output decoupling capacitance needed at the gate driver input.

For dual adjustable output configuration an internal inverting buck-boost converter generates a regulated negative rail for the turn-off supply (VEE). The buck-boost converter is controlled by a peak current mode, hysteretic controller. In normal operation, the converter remains in discontinuous-conduction mode, but can enter continuous-conduction mode during start-up. The converter is controlled internally and requires only a single surface-mount inductor (L_{BB}) and output bypass capacitor (C_{VEE}). Typically, the converter is designed to use a 3.3µH inductor and a 2.2µF output capacitor.

A summary table for the recommended values of BOM components shown below and is also available in the UCC34141 calculator tool , as another design supporting document besides this data sheet.

Table 8-1. Recommended Component Values

Component	Description	Recommended Value
R_{ENA}	ENA pin pullup resistor	4.9kΩ to a 3.3V or 5V rail, or driving by control signal
R_{PG}	$\overline{PG}$(PG) pin pullup resistor	4.9kΩ to a 3.3V or 5V rail
C_{ENA}	ENA pin filter capacitor	100nF
C_{PG}	$\overline{PG}$(PG) pin filter capacitor	1uF
C_{IN}	Input voltage decoupling capacitor	10uF in parallel with 1.0uF
R_{FBVEE}	Resistor to set VEE voltage	See Section 8.2.2.2
C_{FBVEE}	Filter capacitor on FBVEE	10pF to COMA
L_{BB}	VEE rail inverting buck boost inductor	3.3uH to 10uH
R_{FBVDD_TOP}	VDD output voltage top selection resistor	See Section 8.2.2.1
R_{FBVDD_BOT}	VDD output voltage bottom selection resistor	See Section 8.2.2.1
C_{FBVDD}		220pF
C_{VDD}	Output bias supply capacitors	10uF in parallel with 1.0uF
C_{VDD_GD}	Gate driver bypass capacitors	Load capacitor depends on gate charge of switching load and must be increased to achieve an acceptable ripple voltage

Table 8-1. Recommended Component Values (continued)

Component	Description	Recommended Value
C_{VEE_GD}	Gate driver bypass capacitors	Load capacitor depends on gate charge of switching load and must be increased to achieve an acceptable ripple voltage

8.2.2 Detailed Design Procedure

Place ceramic decoupling capacitors as close as possible to the device pins. For the input supply, place the capacitors between pins 3 and 4(VIN), and pin 5 (GNDP). For the isolated output supply, (VDD – COM), place the C_{VDD} capacitor between pin 12 (VDD) and pin 11 (COM). For the negative voltage supply, (COM – VEE), place the C_{VEE} capacitor between pin 14 (VEE) and pin 11 (COM). These locations are of particular importance to all the decoupling capacitors because the capacitors supply the transient current associated with the fast switching waveforms of the power drive circuits. Verify that the capacitor dielectric material is compatible with the target application temperature.

8.2.2.1 VDD-COM Voltage Regulation

The UCC34141 creates an isolated output VDD-COM as its main output. The power stage operation is determined by sensing the VDD voltage on FBVDD pin using hysteresis control. The internal reference voltage V_{FBVDD_REF} = 2.5V typ. To determine the values for R_{FBVDD_TOP} with a chosen R_{FBVDD_BOT}, use the equation:

$$R_{FBVDD\_TOP} = \frac{V_{VDD} \times R_{FBVDD\_BOT}}{V_{FBVDD\_REF}} - R_{FBVDD\_BOT} \tag{2}$$

As an example, to set a VDD value of 20V, a 10kΩ resistor can be chosen as R_{FBVDD_BOT}, and the R_{FBVDD_TOP} can be calculated as

$$R_{FBVDD\_TOP} = \frac{20V \times 10k\Omega}{2.5V} - 10k\Omega = 70k\Omega \tag{3}$$

To improve the noise immunity, add a small capacitor C_{FBVDD} of 220pF between the FBVDD and COMA pins.

8.2.2.2 COM-VEE Voltage Regulation and Single Output Configuration

UCC34141 can be configured either as a dual output or a single output converter, using the VEE feedback resistor R_{FBVEE}. The table below summarizes the programmable range with different R_{FBVEE} value. The VDD single output mode can be programmed by a R_{FBVEE} value between 150kΩ and 300kΩ. TI recommends a 180kΩ SMD resistor with ≤±5% tolerance. A R_{FBVEE} lower than 150kΩ can trigger VDD and VEE dual output mode, and a R_{FBVEE} higher than 300kΩ can trigger FBVEE pin-open fault. The typical application schematic of single output configuration is shown in Figure 8-2

Table 8-2. R_{FBVEE} Programming

R_{FBVEE}	0kΩ to 5kΩ	25kΩ to 85kΩ	150kΩ to 300kΩ	>1000kΩ
Operation Mode	Trigger FBVEE pin-short fault, output shuts off.	VEE in regulation, VDD & VEE dual output Recommend a SMD resistor with ≤ ±1% tolerance for best regulation accuracy.	VDD single output Recommend a 180kΩ SMD resistor with ≤±5% tolerance.	Trigger FBVEE pin-open fault, output shuts off.

An internal buck-boost converter generates the regulated negative VEE voltage. The buck-boost converter operation is determined by sensing the VEE voltage on FBVEE pin. With an internal 45k resistor and a 4.5V reference voltage, VEE voltage can be programed and regulated from -2V to -8V. The transfer function between COM-VEE and R_{FBVEE} in dual output mode is

$$R_{FBVEE} = \frac{(0.5V - V_{VEE}) \times 45k\Omega}{4.5V} \tag{4}$$

An example equation to set a VEE regulation value at -5V

$$R_{FBVEE} = \frac{[0.5V - (-5V)] \times 45k\Omega}{4.5V} = 55k\Omega \quad (5)$$

8.3 System Examples

The UCC34141 module integrates seamlessly into the system to provide power to a gate driver for both IGBT and SiC power FET control. Fault and status feedback is provided through the $\overline{PG}$(PG) pin, and power sequencing can be controlled with the ENA pin. The system diagrams for the dual-output configuration and single-output configuration are shown below.

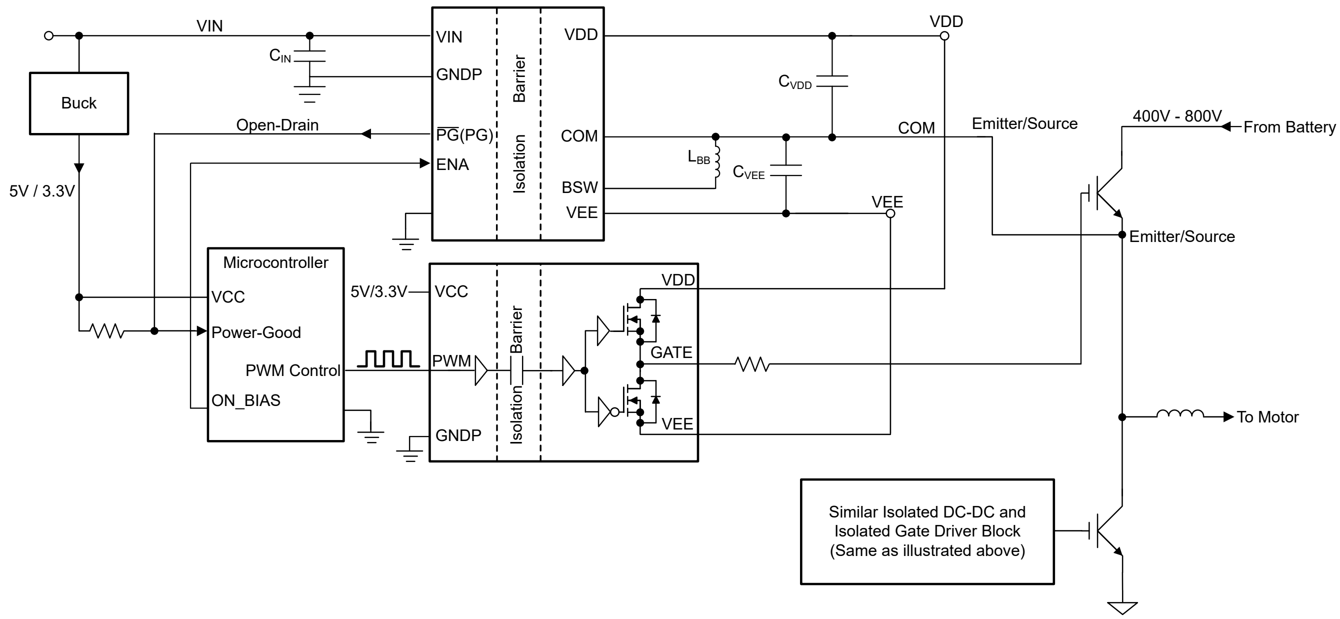


Figure 8-3. Dual Output System Configuration

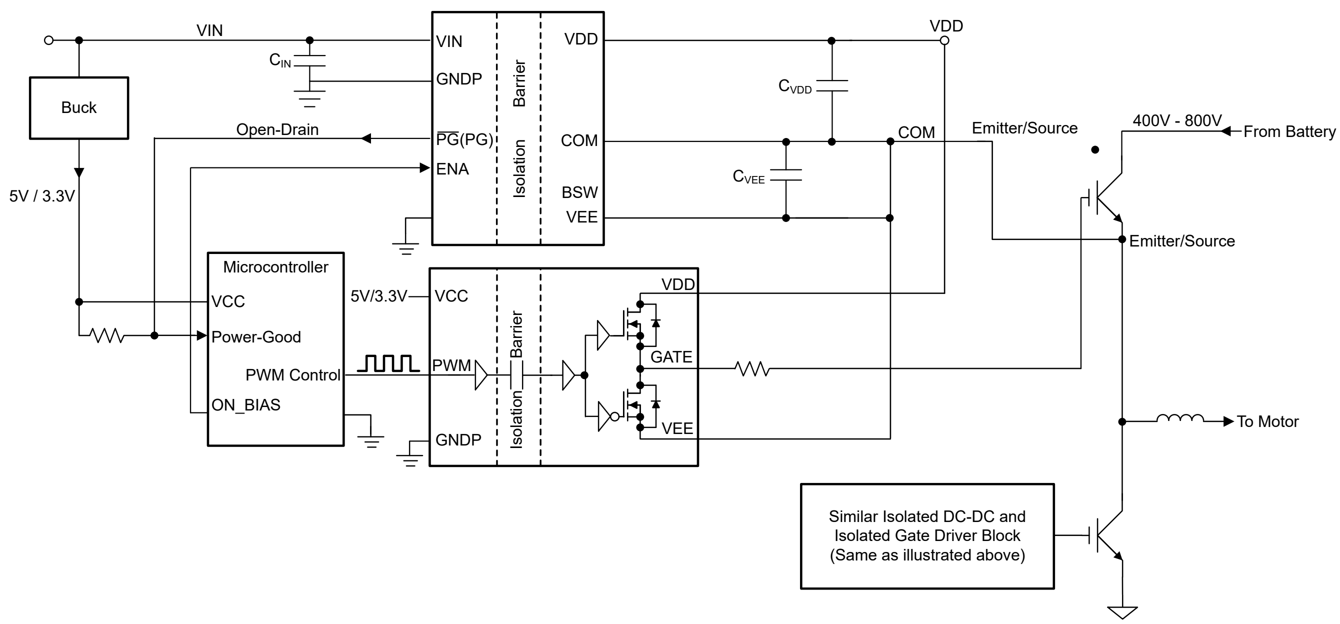


Figure 8-4. Single Output System Configuration

8.4 Power Supply Recommendations

UCC34141 requires a single input power supply, VIN. To help establish reliable operation, locate adequate decoupling capacitors as close to supply pins as possible. Local bypass capacitors must be placed between the VIN and GNDP pins at the input; between VDD and COM, and between COM and VEE at the output. TI recommends low ESR, ceramic surface mount capacitors to provide the recommended capacitance for high frequency decoupling. The input supply must have an appropriate current rating to support output load required by the end application.

8.5 Layout

8.5.1 Layout Guidelines

The UCC34141 integrated isolated power solution simplifies system design and reduces board area usage. Follow these guidelines for proper PCB layout to achieve optimum performance. A minimum of 4-layer PCB layer stack using 2-ounce copper on external layers is recommended to accomplish a good thermal PCB design. It is not recommended to route signal tracks or place components directly beneath the UCC34141.

1. Input capacitors between VIN pin and GNDP pin:
   a. Place the 0.1µF high frequency bypass capacitor (C3) as close as possible to pins 3, 4 (VIN) and pins 5–8 (GNDP) and on the same side of the PCB as the IC. 0402 ceramic SMD or smaller is a desired size for optimal placement. The self-resonant frequency in a range from 10MHz to 30MHz is most ideal to offer low impedance decoupling for the switching frequency noise of the internal isolated convertor. Do not place any vias between the bypass capacitor and the IC pins so as to force the high frequency current through the capacitor.
   b. Place the bulk VIN capacitor(s) (C2) as close as possible and parallel to the 0.1µF high frequency bypass capacitor (C3) and on the same side of the PCB as the IC as shown in Figure 8-5.
2. Output capacitors between VDD pin and COM pin:
   a. Place the 0.1µF high frequency bypass capacitor (C5) as close as possible to pin 12 (VDD) and pins 10, 11 (COM) and on the same side of the PCB as the IC. 0402 ceramic SMD or smaller is a desired size for optimal placement. The self-resonant frequency in a range between 10MHz to 30MHz is most ideal to offer low impedance decoupling for the switching frequency noise of the internal isolated convertor. Do not place any vias between the bypass capacitor and the IC pins so as to force the high frequency current through the capacitor.
   b. Place the bulk VDD-COM capacitor (C8) as close as possible and parallel to the 0.1µF high frequency bypass capacitor (C5) and on the same side of the PCB as the IC as shown in Figure 8-5.
3. Output capacitors between VEE pin and COM pin:
   a. Place the 2.2µF high frequency bypass capacitor (C9) as close as possible to VEE and COM pins. The self-resonant frequency in 3MHz to 4MHz is most ideal to offer low impedance decoupling for the switching frequency noise of the buck-boost converter with the 3.3uH inductor (L1) selection. It is possible to put the capacitor on the different side of PCB and use vias to connect, to reduce the switching loop between the capacitor and the internal low-side MOSFET of the VEE buck-boost converter. In addition, putting the capacitor on different side also simplifies the decoupling capacitor placement of VDD pin and COM pin. An example of bottom side PCB placement of C9 and L1 is shown in Figure 8-9.
4. Feedback:
   a. COMA must be isolated through all PCB layers, from the COM plane. Use one via to make a direct connection to the low-side resistor and filter capacitor from FBVDD pin, same as the low-side filter capacitor from FBVEE pin.
   b. Place the RFBVDD feedback resistors (R6 and R7) and the decoupling ceramic capacitor (C6) close to the IC.
   c. The top-side feedback resistor must be placed next to the low-side resistor with a short, direct connection between both resistors and single connection to FBVDD pin. The top connection to sense the regulated rail (VDD-COM) must be routed and connected at the VDD bias capacitor remote location near the gate driver pins for best accuracy and best transient response.

   d. The VEE feedback resistor (R5) must be placed with the decoupling ceramic capacitor (C4) next to FBVEE (pin 15); while the connection to sense the regulated rail (COM-VEE) must be routed and connected at the COM bias capacitor remote location near the gate driver pins for best accuracy and best transient response.
   e. When using the dual output mode, the buck-boost inductor (L1) and a 2.2uF decoupling ceramic capacitor (C9) must be populated. They can be place on the opposite side of the IC or on the same layer as IC.
   f. A layout example is shown in Figure 8-6, where L2 (yellow) is routed on layer 2 and L3 (green) is routed on layer 3.

5. Thermal vias: The UCC34141 internal transformer makes a direct connection to the lead frame. It is therefore critical to provide adequate space and proper heat-sinking designed into the PCB as outlined in the steps below.
   a. TI recommends to connect the VIN, GNDP, VDD, and COM pins to internal ground or power planes through multiple vias. Alternatively, make the polygons connected to these pins as wide as possible.
   b. Use multiple thermal vias connecting PCB top side GNDP copper to bottom side GNDP copper. If possible, it is recommended to use 2-ounce copper on external top and bottom PCB layers.
   c. Use multiple thermal vias connecting PCB top side VEE copper to bottom side VEE copper. If possible, it is recommended to use 2-ounce copper on external top and bottom PCB layers.
   d. Thermal vias connecting top and bottom copper can also connect to internal copper layers for further improved heat extraction.
   e. Thermal vias must be similar to pattern shown below but apply as many as the copper area allows. TI recommends to use thermal via with 30mil diameter, 12mil hole size.
   f. A layout example is shown in Figure 8-7. For cases where less copper area is available, use as many thermal vias as the design permits, placed close to pins 5-8 (primary) and 9-11 (secondary).

6. Creepage clearance: To maintain the full creepage, clearance and voltage isolation ratings specified in the data sheet, avoid routing signal traces or placing components directly under the UCC34141. Maintain the clearance width highlighted in red, throughout the entire defined isolation barrier. Keep-out clearance for basic isolation can be 50% less than the reinforced isolation requirement (8.2mm). Using 8.2mm provides additional margin. A layout example is shown in Figure 8-8.
7. Gate driver output capacitors: C_{VDD_GD} (C11 and C12) and C_{VEE_GD} (C10) are reference designators referred to in the UCC34141 calculator tool . C11 and C12 are the capacitors between VDD-COM and C10 is the capacitor between COM-VEE. C10-12 are capacitors required by the gate driver IC.
   a. C_{VDD_GD} and C_{VEE_GD} must be placed next to the gate driver IC for best decoupling and gate driver switching performance.
   b. For optimal voltage regulation, the feedback trace from VEE (FBVEE) and VDD (FBVDD) must be as direct as possible so that the voltage feedback is being sensed directly at the VDD and VEE capacitors near the gate driver IC.

8. Power good pins decoupling capacitor: The decoupling capacitor must be placed close to pin 2 (power good pin) and on the same side of the PCB as the UCC34141. Refer to C13 placement shown in Figure 8-5.

8.5.2 Layout Example

The PCB layout example, highlighted in the following figures, is based on the schematic shown in Figure 8-1.

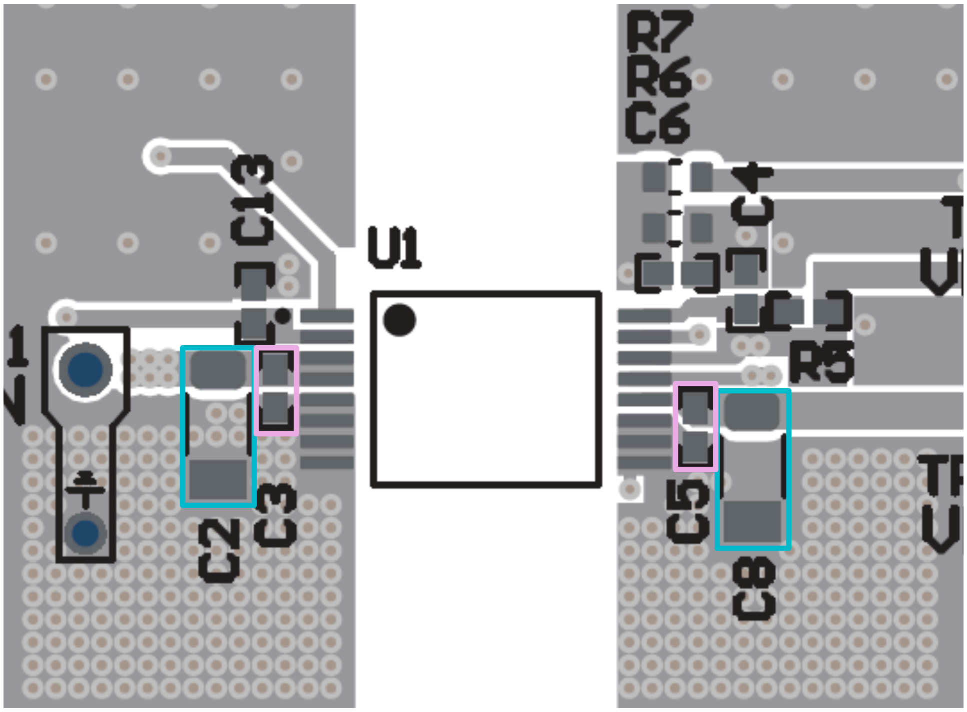


Figure 8-5. VIN (C2, C3) and VDD (C5, C8) Capacitors

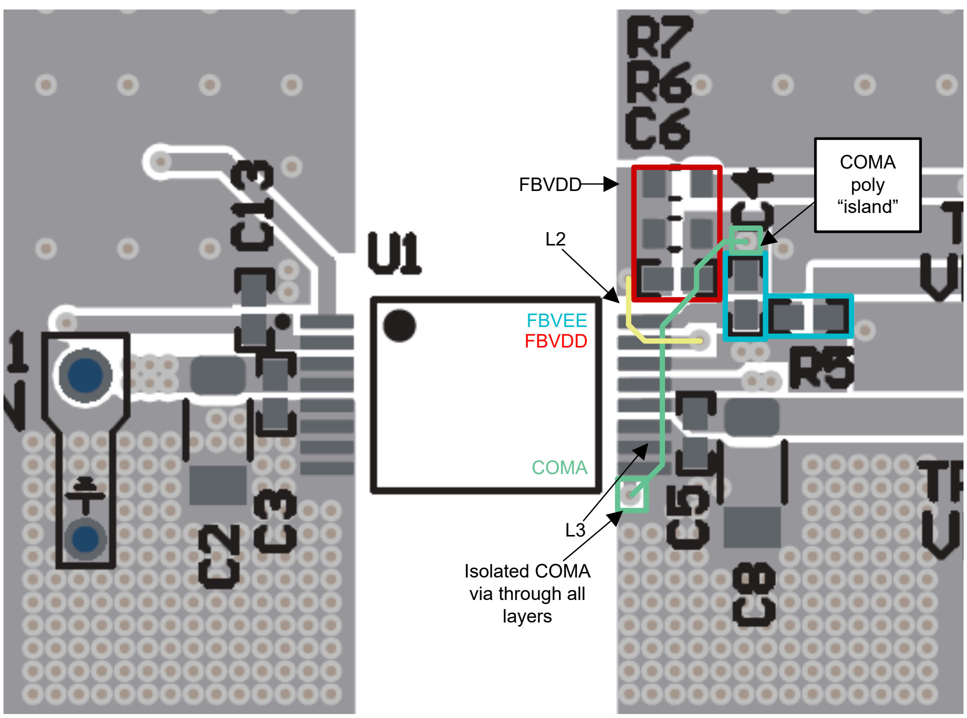


Figure 8-6. FBVDD (R6-7, C6), FBVEE (R5, C4), COMA Routing

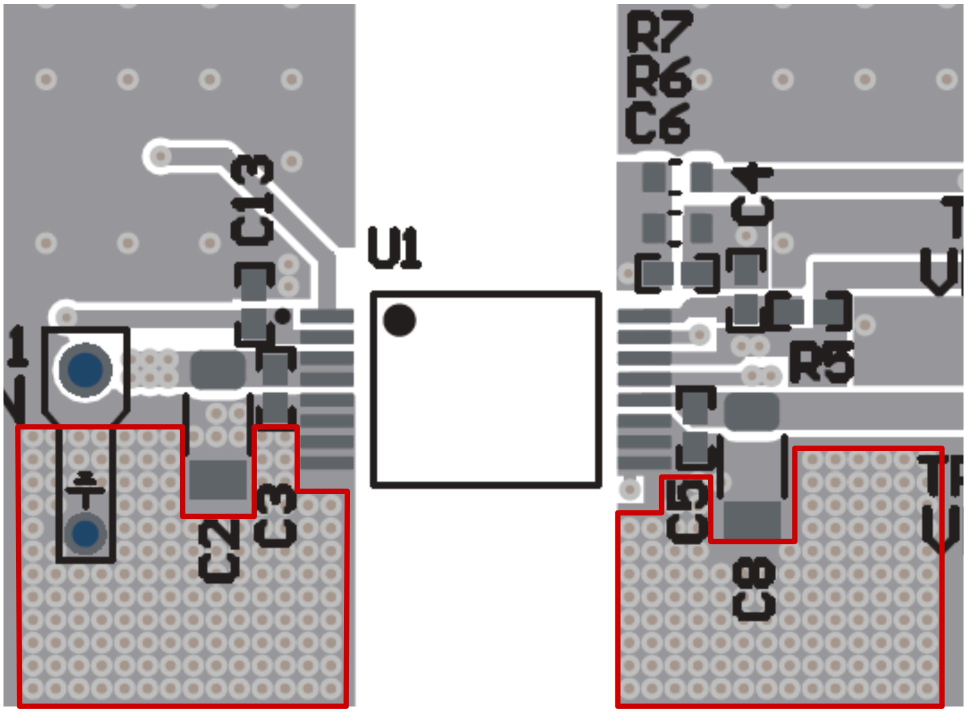


Figure 8-7. Thermal Vias

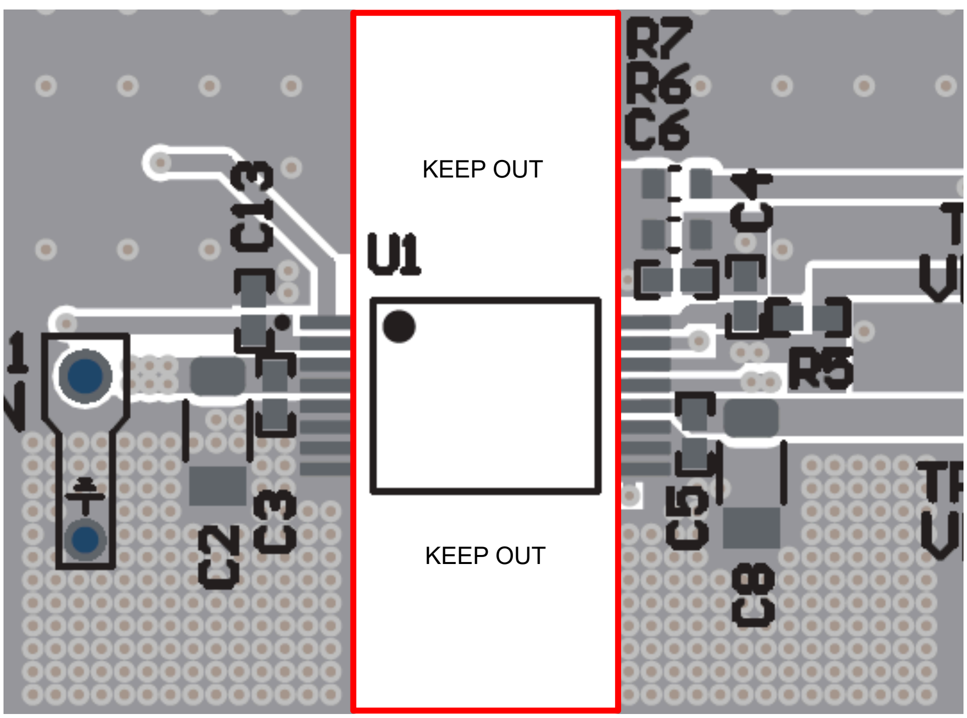


Figure 8-8. Isolation Keep Out Region

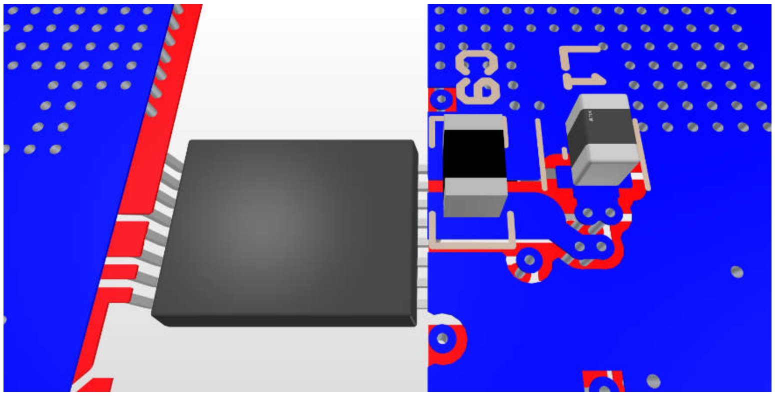


Figure 8-9. Bottom Side, Buck Boost, VEE LC Placement and Routing

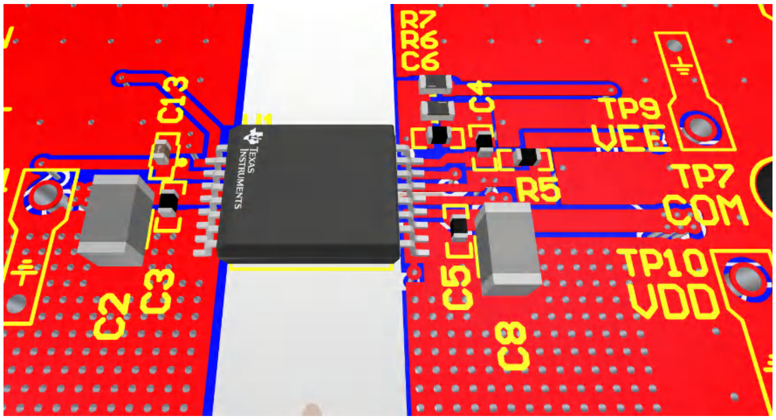


Figure 8-10. Top Side, Component Placement and Routing

9 Device and Documentation Support

9.1 Third-Party Products Disclaimer

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9.2 Documentation Support

9.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Isolation Glossary*

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (March 2026) to Revision A (April 2026) **Page**

- Updated I_{VINP_NL} maximum from: 16mA to: 18mA.. 8

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

TI recommends to install the device with JEDEC standard J-STD-020 reflow process. The peak solder temperature should not exceed 260ºC. If manual installation is needed during the testing process, TI recommends to limit the peak temperature not exceeding 260°C.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC34141DDHAR	Active	Production	SO-MOD (DHA) | 16	1000 | LARGE T&R	In-Work	NIPDAU	Level-3-260C-168 HR	-40 to 125	UCC34141

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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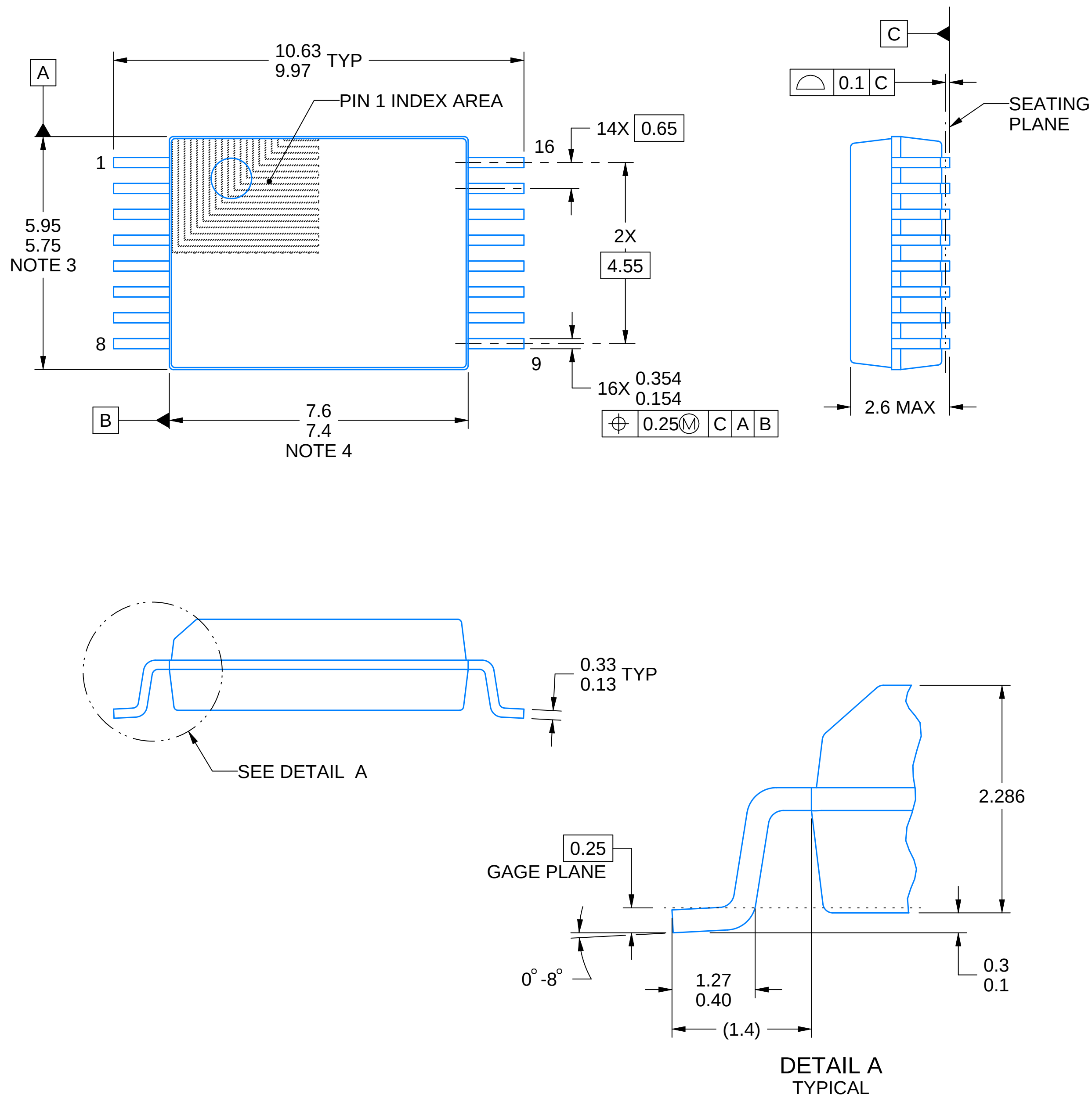
OTHER QUALIFIED VERSIONS OF UCC34141 :

- Automotive : UCC34141-Q1

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects



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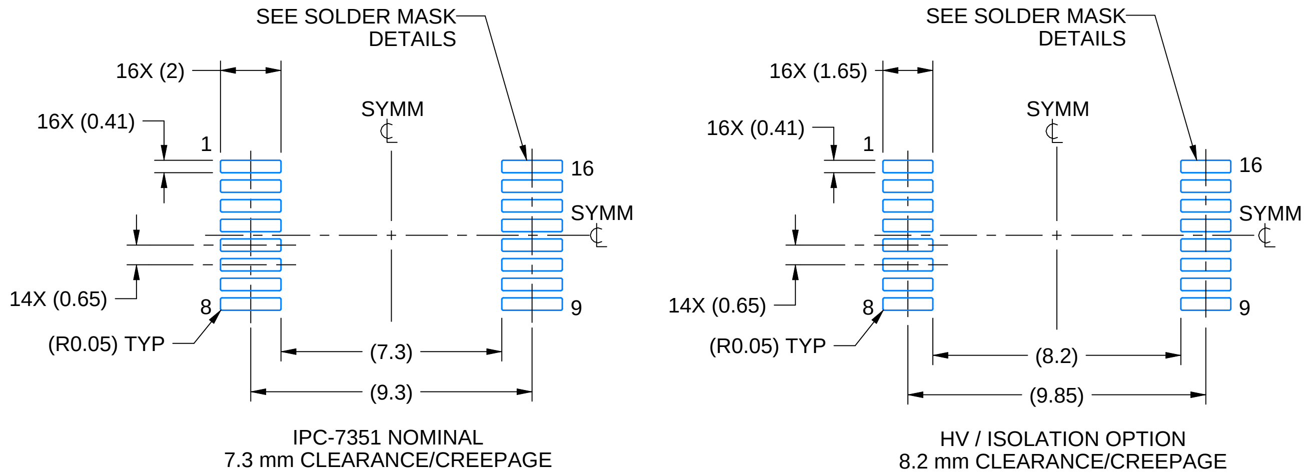
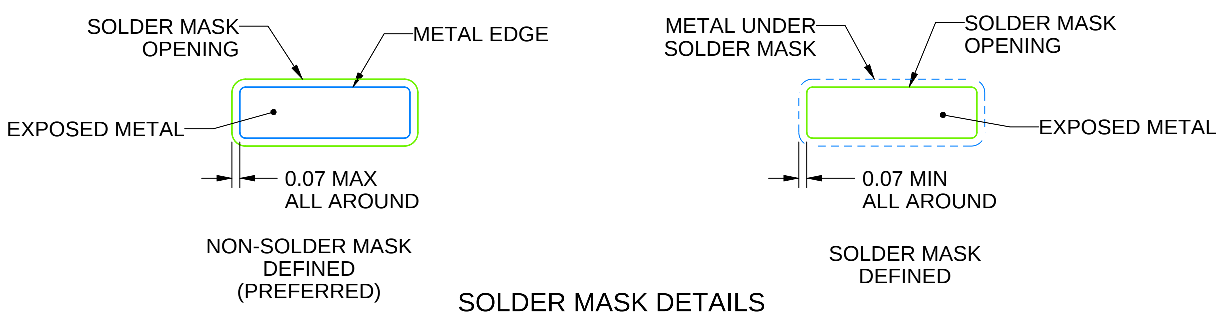
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLES
EXPOSED METAL SHOWN
SCALE: 4X



SOLDER MASK DETAILS

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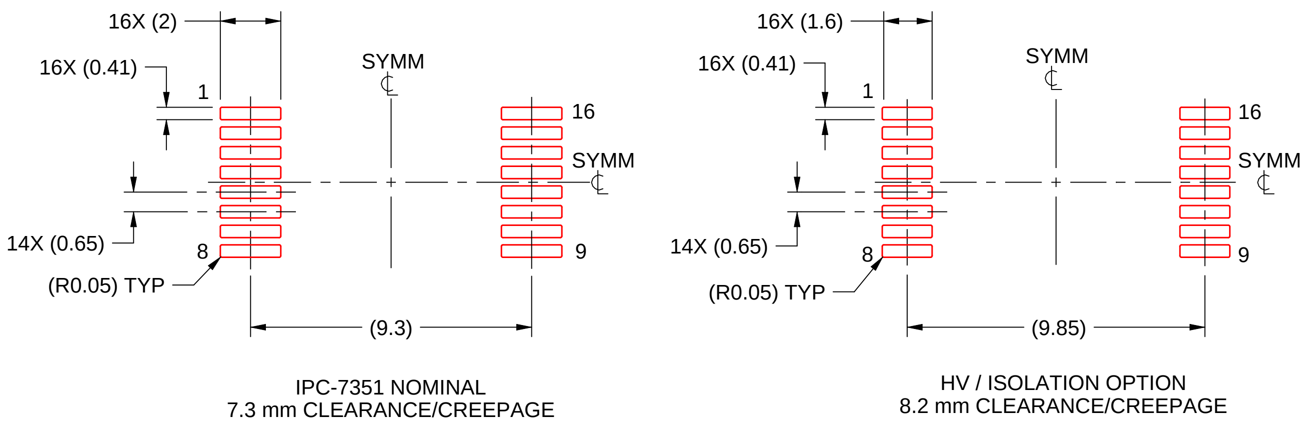
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLES
BASED ON 0.125 mm THICK STENCIL
SCALE: 4X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.