UCC5520-Q1 Single-Channel Isolated Gate Driver for SiC/IGBT and Automotive Applications

1 Features

- 5kV$_{RMS}$ single-channel isolated gate driver
- AEC-Q100 Qualified
- SiC MOSFETs and IGBTs up to 1500V$_{pk}$
- Input supply voltage (V$_{CC}$-GND): 3V to 18V
- Maximum output drive voltage (V$_{DD}$-V$_{EE}$): 36V
- Drive strength and split output: ±10A
- Minimum CMTI: 500V/ns
- Internal active Miller clamp: 5A
- V$_{DD}$ UVLO options: 8V and 12V
- 8 pin DWV and 12 pin DFP wide body package with creepage and clearance distance > 8mm
- CMOS inputs
- Operating junction temperature –40°C to 150°C

2 Applications

- On-board battery chargers
- DC Charging Stations
- Automotive HVAC, body electronics
- Motor drive and inverters
- Energy Storage Systems

3 Description

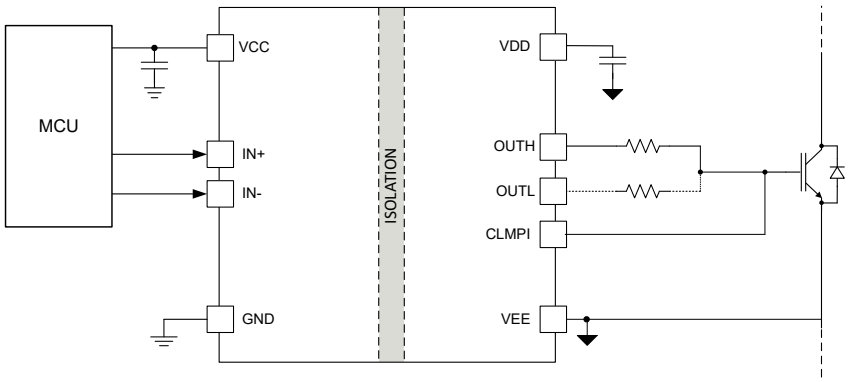
The UCC5520-Q1 is a single-channel, isolated gate driver with 10A source and 10A sink typical peak current designed to drive MOSFETs, IGBTs, and SiC MOSFETs. The UCC5520-Q1 has the option for Miller clamp or split outputs. The CLMPI pin is used to connect the transistor gate to an internal FET beside the output to prevent false turn-on caused by Miller current injection. The split output option allows separate control of the rise and fall times of the gate voltage with OUTH and OUTL pins.

UCC5520-Q1 is available in 7.5mm wide body SOIC-8 (DWV), SOIC-12 (DFP) UCC5520-Q1 support isolation voltage up to 5kV$_{RMS}$(12DFP, 8DWV). The input side is isolated from the output side with high reliability SiO_2 magnetic isolation technology. The UCC5520-Q1 is designed for driving IGBTs or MOSFETs in applications such as high-voltage inverters and onboard chargers. UCC5520-Q1 family offers lower part-to-part skew, higher operating temperature, and CMTI greater than 500V/ns. With all these advanced features, UCC5520-Q1 enables high efficiency, high power density, and robustness in a wide variety of power applications.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
UCC5520MBDWV	DWV (SOIC 8)	7.5mm × 5.85mm
UCC5520MCDWV		
UCC5520PBDFP	DFP (SOIC 12)	7.5mm × 3.65mm
UCC5520PCDFP		

(1) For all available packages, see Section 12.1.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application Schematic - 12DFP

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4 Device Comparison Table

Table 4-1. Device Comparison Table

DEVICE OPTION(1)	PACKAGE	TYPICAL SOURCE CURRENT	TYPICAL SINK CURRENT	PIN CONFIGURATION	UVLO	ISOLATION RATING
UCC5520MB	DWV	10A	10A	Miller clamp	8V	$5kV_{RMS}$
UCC5520MC	DWV	10A	10A	Miller clamp	12V	$5kV_{RMS}$
UCC5520SB	DWV	10A	10A	Split output	8V	$5kV_{RMS}$
UCC5520SC	DWV	10A	10A	Split output	12V	$5kV_{RMS}$
UCC5520PB	DFP	10A	10A	Miller clamp + Split output	8V	$5kV_{RMS}$
UCC5520PC	DFP	10A	10A	Miller clamp + split output	12V	$5kV_{RMS}$

(1) See Section 12 for the full orderable part number.

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5 Pin Configuration and Functions

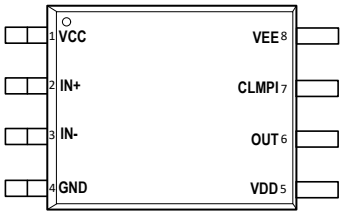


Figure 5-1. UCC5520MxDWV 8 - Pin SOIC Top View

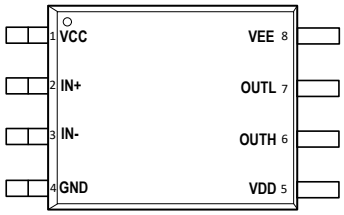


Figure 5-2. UCC5520SxDWV 8 - Pin SOIC Top View

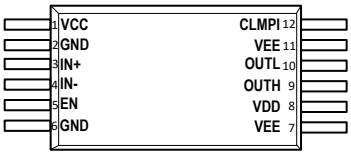


Figure 5-3. UCC5520PxDFP 12- Pin SOIC Top View

Table 5-1. Pin Functions

PIN			TYPE[1]	DESCRIPTION
NAME	(DWV, D-8)	(DFP-12)		
VCC	1	1	P	Primary side input supply voltage. Locally decouple pin to GND. Use a low-ESR or ESL capacitor located as close to the device as possible.
IN+	2	3	I	Non-inverting gate-drive voltage-control input. The IN+ pin has a CMOS input threshold. This pin is pulled low internally if left open.
IN-	3	4	I	Inverting gate-drive voltage control input. The IN– pin has a CMOS input threshold. This pin is pulled high internally if left open
GND	4	2,6	G	Primary side ground. All signals on the input side are referenced to this ground.
VDD	5	8	P	Secondary side positive output supply rail. Locally decouple pin to VEE. Use a low-ESR or ESL capacitor located as close to the device as possible.
OUT	6	-	O	Gate-drive output
OUTH	-	9	O	Gate-drive pull-up output
OUTL	-	10	O	Gate-drive pull-down output
CLMPI	7	12	O	Active Miller-clamp input used to prevent false turn-on of the power switches found on the 'M' and 'P' version. Connect to gate directly with low inductance.
VEE	8	7,11	G	Secondary side ground pin. Connect to FET source or IGBT emitter.

(1) P = Power, G = Ground, I = Input, O = Output

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
VCC	VCC - GND	–0.3	20	V
VDD	VDD - VEE	–0.3	36	V
IN+, IN-	DC	GND–0.3	VCC+0.3	V
OUT	DC	VEE-0.3	VDD	
OUTH, OUTL	DC	VEE-0.3	VDD	V
OUT	Transient, less than 100ns(2)	TBD	TBD	
OUTH, OUTL	Transient, less than 100ns(2)	TBD	TBD	V
CLMPI	Voltage on CLMPI, reference to VEE	–0.3	VDD	V
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Values are verified by characterization on bench.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged device model (CDM), per AEC Q100-011	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
VCC	VCC-GND	3	18	V
VDD	VDD-VEE	UVLO_ON (max)	30	V
T_A	Ambient temperature	–40	125	°C
T_J	Junction temperature	–40	150	°C

6.4 Thermal Information

THERMAL METRIC(1)		UCC552x		UNIT
		DWV	DFP	
		8 Pins	12 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	TBD	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	TBD	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	TBD	TBD	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	TBD	TBD	°C/W

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THERMAL METRIC(1)		UCC552x		UNIT
		DWV	DFP	
		8 Pins	12 Pins	
Ψ_{JB}	Junction-to-board characterization parameter	TBD	TBD	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation (both sides)	VCC-GND = 5V, VDD-VEE = 25V, IN+/- = 5V, 140kHz, 50% Duty Cycle for 10nF load, Ta = 25℃		TBD		mW
P_{D1}	Maximum power dissipation by transmitter side	VCC-GND = 5V, VDD-VEE = 25V, IN+/- = 5V, 140kHz, 50% Duty Cycle for 10nF load, Ta = 25℃		TBD		mW
P_{D2}	Maximum power dissipation by receiver side	VCC-GND = 5V, VDD-VEE = 25V, IN+/- = 5V, 140kHz, 50% Duty Cycle for 10nF load, Ta = 25℃		TBD		mW

6.6 Insulation Specifications Reinforced Isolation

PARAMETER		TEST CONDITIONS	SPECIFICATION	UNIT
GENERAL				
CLR	External clearance(1)	Shortest terminal-to-terminal distance through air	> 8	mm
CPG	External Creepage(1)	Shortest terminal-to-terminal distance across the package surface	> 8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	> 17	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
	Material Group	According to IEC 60664–1	I	
	Overvoltage Category per IEC 60664–1	Rated mains voltage ≤ 300V_{RMS}	I-IV	
		Rated mains voltage ≤ 600V_{RMS}	I-III	
		Rated mains voltage ≤ 1000V_{RMS}	I-II	
DIN V VDE 0884-10 (VDE V 0884-10): 2016-12				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1500	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave); time-dependent dielectric breakdown (TDDB) test; see Figure 1	1063	V_{RMS}
		DC voltage	1500	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60s (qualification test) $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1s (100% production test)	7071	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(2)	Test method per IEC 60065, 1.2/50µs waveform, $V_{TEST} = 1.6 \times V_{IOSM} = 11300V_{PK}$ (qualification)	10000	V_{PK}
q_{pd}	Apparent charge(3)	After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, tini = 60s; Vpd(m) = 1.2 × $V_{IORM} = 2545V_{PK}$, tm = 10s	≤ 5	pC
		After environmental tests subgroup 1,$V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.6 \times V_{IORM} = 3394V_{PK}$, tm = 10s	≤ 5	
		At routine test (100% production) and preconditioning (type test), $V_{ini} = V_{IOTM}$, t_{ini} = 1s; $V_{pd(m)} = 1.875 \times V_{IORM} = x\ V_{PK}$, t_m = 1s	≤ 5	
C_{IO}	Barrier capacitance, input to output(4)	$V_{IO} = 0.5 \times \sin(2\pi ft)$, f = 1MHz	~ 1.2	pF

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PARAMETER		TEST CONDITIONS	SPECIFICATION	UNIT
R_{IO}	Insulation resistance, input to output(4)	V_{IO} = 500V, T_A = 25°C	≥ 10^{12}	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	≥ 10^{11}	
		V_{IO} = 500V at T_S = 150°C	≥ 10^{9}	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	V_{TEST} = V_{ISO} = 5000V_{RMS}, t = 60s (qualification), V_{TEST} = 1.2 × V_{ISO} = 6000V_{RMS}, t = 1s (100% production)	5000	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves and ribs on the PCB are used to help increase these specifications.
(2) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(3) Apparent charge is electrical discharge caused by a partial discharge (pd).
(4) All pins on each side of the barrier tied together creating a two-pin device.

6.7 Insulation Specifications Basic Isolation

PARAMETER		TEST CONDITIONS	SPECIFICATION	UNIT
General				
CLR	External clearance(1)	Shortest terminal-to-terminal distance through air	>4	mm
CPG	External creepage DW and DWK package(1)	Shortest terminal-to-terminal distance across the package surface	>4	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>9	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
	Material Group	According to IEC 60664-1	I	
	Overvoltage category	Rated mains voltage ≤ 150V_{RMS}	I-IV	
	Overvoltage category	Rated mains voltage ≤ 300V_{RMS}	I-III	
	Overvoltage category	Rated mains voltage ≤ 600V_{RMS}	TBD	
		Rated mains voltage ≤ 1000V_{RMS}	TBD	
DIN EN IEC 60747-17 (VDE 0884-17)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	707	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave); time-dependent dielectric breakdown (TDDB) test; see Figure 6-1	500	V_{RMS}
		DC voltage	707	V_{DC}
V_{IMP}	Maximum inpulse voltage	Tested in air, 1.2/50µs waveform per IEC 62368-1	4000	V_{PK}
V_{IOTM}	Maximum transient isolation voltage	V_{TEST} = V_{IOTM}, t = 60s (qualification) V_{TEST} = 1.2 × V_{IOTM}, t = 1s (100% production)	4243	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(2)	V_{IOSM} ≥ 1.3x V_{IMP}; Tested in oil (qualification test), 1.2/50-µs waveform per IEC 62368-1	5200	V_{PK}
q_{pd}	Apparent charge(3)	After I/O safety test subgroup 2/3, V_{ini} = V_{IOTM}, t_{ini} = 60s; $V_{pd(m)}$ = 1.2 × V_{IORM} , t_m = 10s	≤5	pC
		After environmental tests subgroup 1, V_{ini} = V_{IOTM}, t_{ini} = 60s; $V_{pd(m)}$ = 1.6 × V_{IORM}, t_m = 10s	≤5	
		At routine test (100% production) and preconditioning (type test), V_{ini} = 1.2 × V_{IOTM}, t_{ini} = 1s; $V_{pd(m)}$ = 1.875 × V_{IORM} , t_m = 1s	≤5	
C_{IO}	Barrier capacitance, input to output(4)	V_{IO} = 0.4 × sin (2πft), f = 1MHz	~1.1	pF

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PARAMETER		TEST CONDITIONS	SPECIFICATION	UNIT
R_{IO}	Insulation resistance, input to output(4)	V_{IO} = 500V, T_A = 25°C	>10^{12}	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	>10^{11}	
		V_{IO} = 500V at T_S = 150°C	>10^{9}	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	V_{TEST} = V_{ISO} = 3000V_{RMS}, t = 60s (qualification), V_{TEST} = 1.2 × V_{ISO}, t = 1s (100% production)	3000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed-circuit board are used to help increase these specifications.
(2) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(3) Apparent charge is electrical discharge caused by a partial discharge (pd).
(4) All pins on each side of the barrier tied together creating a two-pin device.

6.8 Electrical Characteristics

VCC = 3.3V or 5V or 18V, 1-µF capacitor from VCC to GND, VDD - VEE = 20V, 18V or 15V, C_L = 100pF, -40°C < T_J < 150°C (unless otherwise noted)(1)(2).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY QUIESCENT CURRENT						
I_{VCCQ}	VCC quiescent current	OUT = Low, f_s = 0Hz		0.467	1	mA
		OUT = High, f_s = 0Hz		2.9	3.5	mA
I_{VDDQ}	VDD quiescent current	OUT = High, f_s = 0Hz		1.2	2.0	mA
		OUT = Low, f_s = 0Hz		0.66	1.5	mA
POWER SUPPLY PROTECTION						
V_{VCC_ON}	VCC UVLO rising threshold			2.6	2.8	V
V_{VCC_OFF}	VCC UVLO falling threshold		2.3	2.45		V
V_{VCC_HYST}	VCC UVLO hysteresis			185		mV
t_{VCCFIL}	VCC UVLO deglitch time			4.5		µs
$V_{VDD_UVLO_ON}$	VDD UVLO rising threshold	UCC5520xB		8		V
$V_{VDD_UVLO_OFF}$	VDD UVLO falling threshold	UCC5520xB		7.5		V
V_{VDD_HYST}	VDD UVLO hysteresis for 8V UVLO			0.5		V
$V_{VDD_UVLO_ON}$	VDD UVLO rising threshold	UCC5520xC		12	13	V
$V_{VDD_UVLO_OFF}$	VDD UVLO falling threshold	UCC5520xC	10.3	11		V
V_{VDD_HYST}	VDD UVLO hysteresis			1		V
t_{VDDFIL}	VDD UVLO deglitch time			6		µs
$t_{VDD+ \text{ to OUT}}$	VDD UVLO on delay to output high	IN+ = VCC, IN- = GND VDD+ to OUTH 10% VDD- to OUTL 90%	2	6	8	µs
$t_{VDD- \text{ to OUT}}$	VDD UVLO off delay to output low			6	8.5	µs
PRIMARY SIDE LOGIC INPUTS (IN+, IN-)						
V_{INH}	Input High Threshold			2	2.3	V
V_{INL}	Input low threshold		0.8	1		V
V_{INHYS}	Input threshold hysteresis			1		V
I_{IH}	Input high level input leakage current	V_{IN} = 5V, VCC=5V		50		uA
I_{IL}	Input low level input leakage current	V_{IN} = 0V, VCC = 5V		-45		uA
t_{in}	Miniumum pulse width for Input	30 Deglitch Variant		30		ns

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VCC = 3.3V or 5V or 18V, 1-µF capacitor from VCC to GND, VDD - VEE = 20V, 18V or 15V, C_L = 100pF, -40°C < T_J < 150°C (unless otherwise noted)(1)(2).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GATE DRIVER STAGE						
I_{OUT}	Peak source current	C_L = 0.22µF, f_S = 1kHz		10		A
I_{OUT}	Peak sink current	C_L = 0.22µF, f_S = 1kHz		10		A
R_{OUTH}	Output pull-up resistance	IOH = 1A, C_L=1.8nF		0.5		Ω
R_{OUTL}	Output pull-down resistance	IOL = -1A, C_L=1.8nF		0.3		Ω
ACTIVE PULLDOWN						
V_{OUTPD}	Output active pull down on OUT	I_{OUT} = 1A, VDD=OPEN, VEE=COM	1.4	2.0	2.6	V
INTERNAL MILLER CLAMP						
V_{CLMPTH}	Miller clamp threshold voltage	Reference to VEE	1.5	2.1	2.5	V
V_{CLMPI}	Output low clamp voltage	I_{CLMPI} = 20mA		7.6		mV
I_{CLMPI}	Output low clamp current	V_{CLMPI} = 0V, VEE = –2.5V		5		A
R_{CLMPI}	Miller clamp pull down resistance	I_{CLMPI} = 0.2A		0.37		Ω
SHORT CIRCUIT CLAMPING						
$V_{CLP-OUTH}$	V_{OUTH} - VDD	OUT = Low, I_{OUTH} = 500mA, t_{CLP}=10us		0.9		V
$V_{CLP-OUTL}$	V_{OUTL} - VDD	OUT = High, I_{OUTL} = 500mA, t_{CLP}=10us		1.1		V
THERMAL PROTECTION						
TSD	Thermal Shutdown			165		°C
TSD_hyst	Thermal Shutdown hysteresis			30		°C
COMMON MODE TRANSIENT IMMUNITY						
CMTI	CMTI noise immunity	V_{CM} = 1200V	500			V/ns

(1) Currents are positive into and negative out of the specified terminal.
(2) All voltages are referenced to COM unless otherwise noted

6.9 Switching Characteristics

VCC = 5.0V, 1-µF capacitor from VCC to GND, VDD - VEE = 20V, 18V or 15V, C_L = 100pF, -40°C<T_J<150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Driver output rise time (20% to 80% of output)	C_L = 1.8nF, R_G=0Ω		11.7		ns
t_f	Driver output fall time (20% to 80% of output)	C_L = 1.8nF, R_G=0Ω		5.5		ns
t_{PDLH}	Propagation delay time low-to-high	C_L = 1.8nF, R_G=0Ω, from VIH to 10% Vout		60		ns
t_{PDHL}	Propagation delay time high-to-low	C_L = 1.8nF, R_G=0Ω, from VIL to 90% Vout	TBD	60	TBD	ns
$t_{UVLOVCC_REC}$	UVLO recovery delay of VCC			8.2		µs
$t_{UVLOVDD_REC}$	UVLO recovery delay of VDD			4.5		µs
PWD	Pulse width distortion (t_{PDHL}-t_{PDLH})				3.5	ns
t_{sk-pp}	Part to part skew	Rising or falling propagation delay			10	ns
f_{MAX}	Maximum switching frequency				1000	kHz

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7 Parameter Measurement Information

7.1 Propagation Delay, Inverting, and Noninverting Configuration

Figure 7-1 shows the propagation delay for noninverting configurations. Figure 7-2 shows the propagation delay with the inverting configuration. These figures also demonstrate the method used to measure the rise (t_r) and fall (t_f) times.

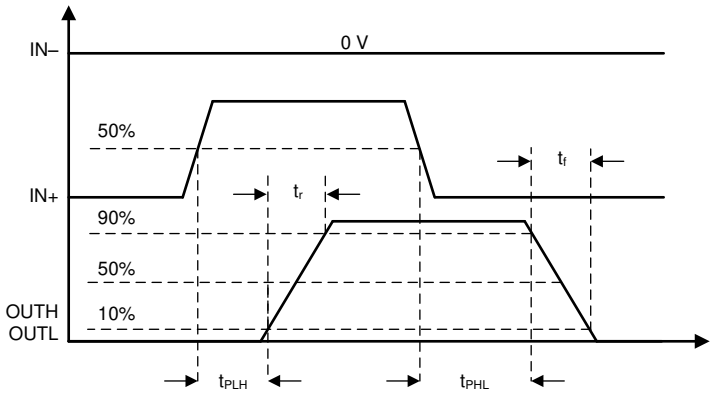


Figure 7-1. OUTH and OUTL Propagation Delay, Noninverting Configuration

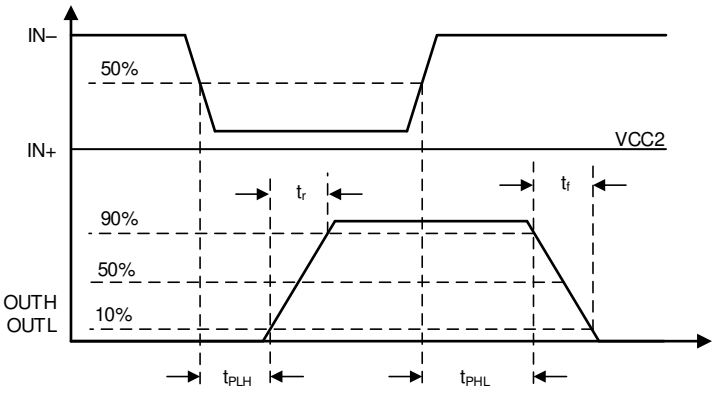
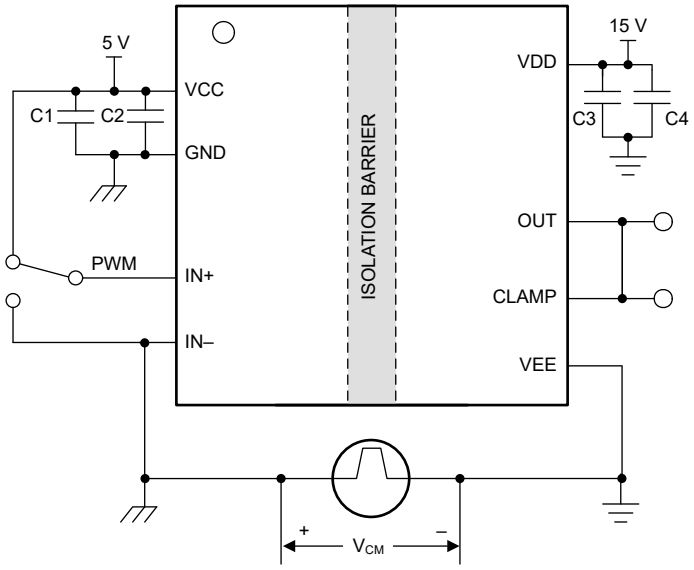


Figure 7-2. OUTH and OUTL Propagation Delay, Inverting Configuration

7.2 CMTI Testing

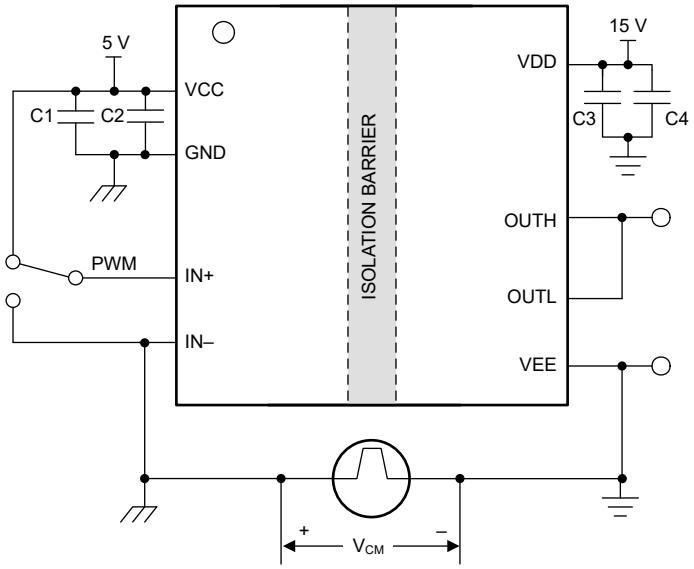
Figure 7-3 and Figure 7-4 are simplified diagrams of the CMTI testing configuration for UCC552xMx and UCC552xSx.

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Figure 7-3. Simplified CMTI Test Circuit for UCC5520Mx



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Figure 7-4. Simplified CMTI Test Circuit for UCC5520Sx

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8 Detailed Description

8.1 Overview

The UCC5520x isolated gate driver family offers three distinct variations to meet diverse design requiremetns: Miller clamp, split output, and a dual-feature version integrating both Miller clamp and split output (see Table 4-1). The isolation inside the UCC5520x family of devices is implemented with high-voltage SiO_2- based isolation transformer that provides reinforced and basic isolation, while providing superior common mode transient immunity. The signal across the isolation has an on-off keying (OOK) modulation scheme to transmit digital data across isolation barrier (see Figure 8-3). The transmitter sends a high-frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. The UCC5520x devices also incorporates advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions from the high-frequency carrier and IO buffer switching.

8.2 Functional Block Diagram

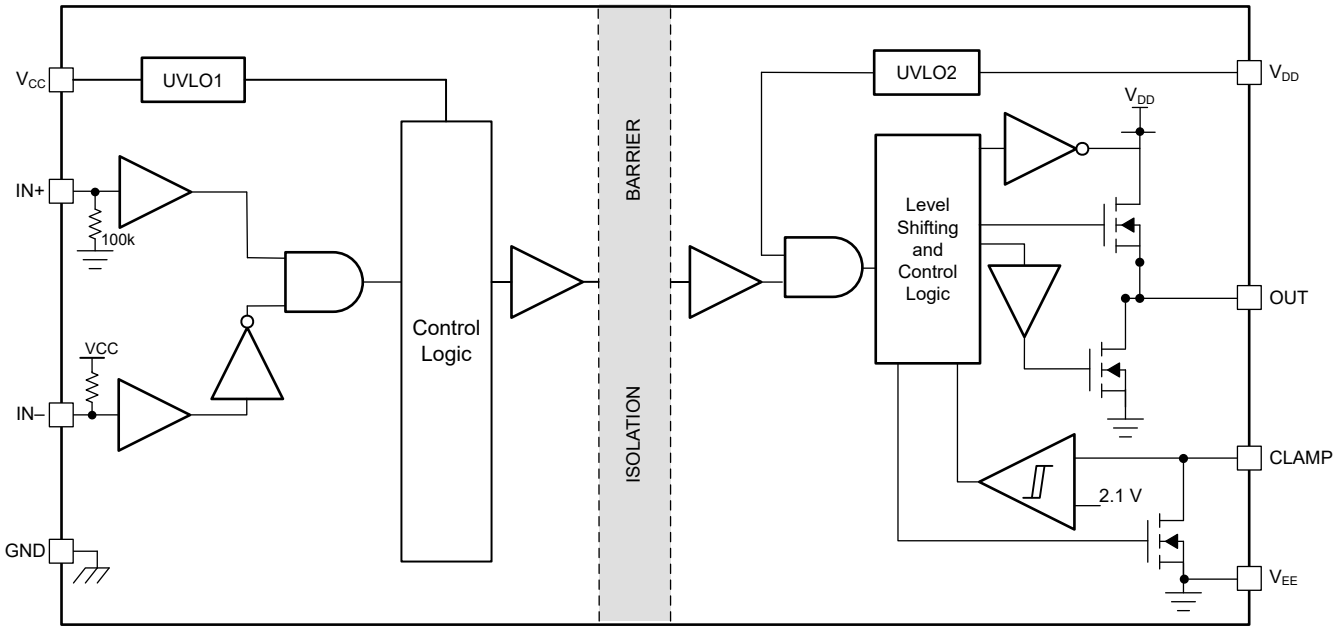


Figure 8-1. Functional Block Diagram — Miller Clamp

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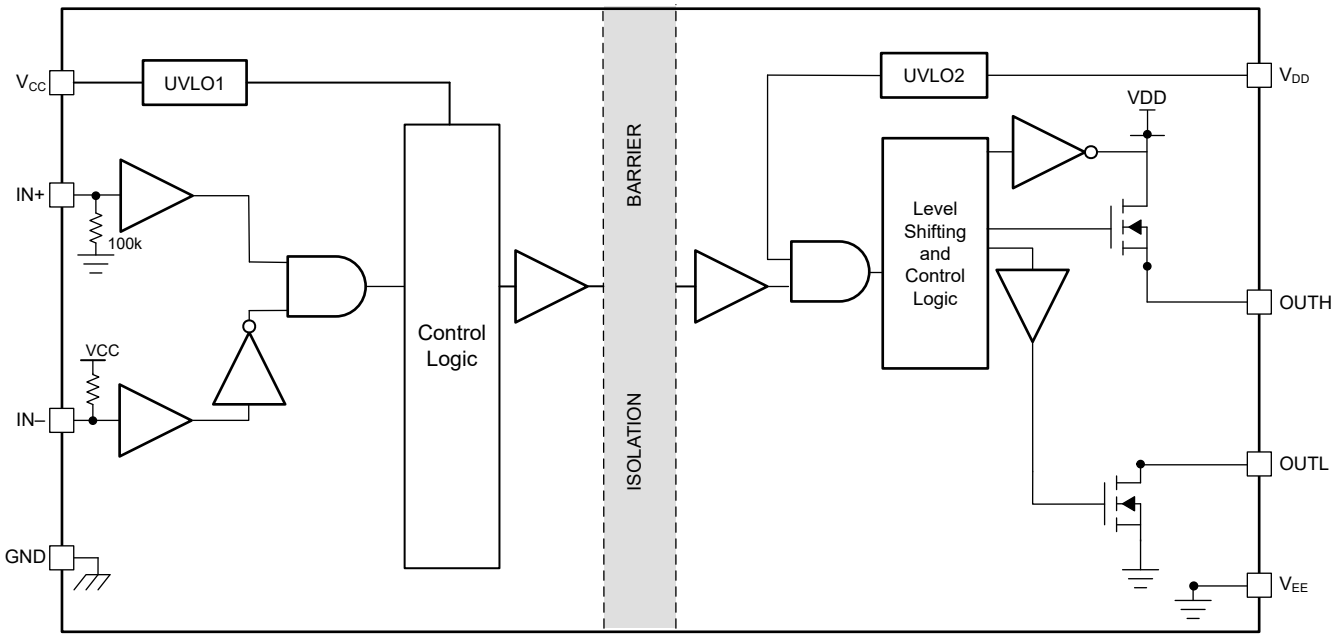


Figure 8-2. Functional Block Diagram — Split Output

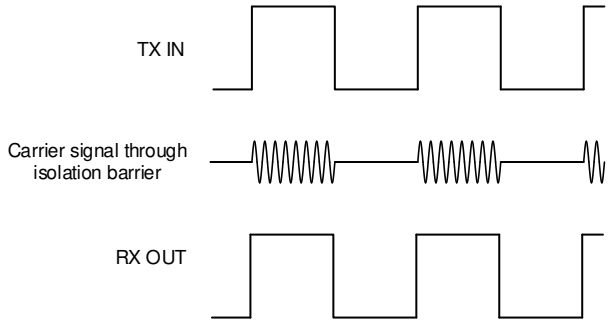


Figure 8-3. On-Off Keying (OOK) Based Modulation Scheme

8.3 Feature Description

8.3.1 Power Supply

The VCC input power supply supports a wide voltage range from 3V to 15V, and the VDD output supply supports a voltage range from 9.5V to 30V.

8.3.2 Input Stage

The input pins (IN+ and IN–) of UCC5520-Q1 are based on CMOS-compatible input-threshold logic that is completely isolated from the VCC supply voltage. The input pins can be driven with logic-level control signals (such as from 3.3V microcontrollers), because the UCC5520-Q1 has a typical high threshold V_{INH} and a typical low threshold V_{INL}. Wide hysteresis makes for good noise immunity and stable operation. If either of the inputs are left open, 100kΩ of internal pull-down resistance forces the IN+ pin low and 100kΩ of internal resistance pulls IN– high. However, TI still recommends grounding an input or tying to VCC if it is not being used for improved noise immunity.

UCC5520-Q1 provides isolation between inputs and outputs. This allows the input signal to be either larger or smaller than VDD, provided it stays within the recommended limits. This flexibility enables easier integration with various control signal sources and allows users to optimize VDD for specific gate drive requirements. Note: The voltage of any signal applied to IN+ and IN- must never exceed VCC.

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8.3.3 Output Stage

The output stage of the UCC5520-Q1 features a pull-up structure that delivers the highest peak-source current when it is most needed which is during the Miller plateau region of the power-switch turn-on transition (when the power-switch drain or collector voltage experiences dV/dt). The output stage pull-up structure features an N-channel MOSFET. Table 8-1 lists the typical internal resistance values of the pull-up and pull-down structure.

Table 8-1. UCC5520-Q1 On-Resistance

DEVICE OPTION	R_{OH}	R_{OL}	UNIT
UCC5520-Q1	0.5	0.3	Ω

R_{OH} and R_{OL} parameters represent the DC on-resistance of the pull-up and pull-down N-channel device, respectively.

The output stage of the UCC5520-Q1 also features a pull-down structure composed of an N-channel MOSFET. The output of the UCC5520-Q1 is capable of sinking, 10A peak current pulses. The output voltage swing between VDD and VEE provides rail-to-rail operation because of the MOS-out stage, which delivers very low dropout voltage.

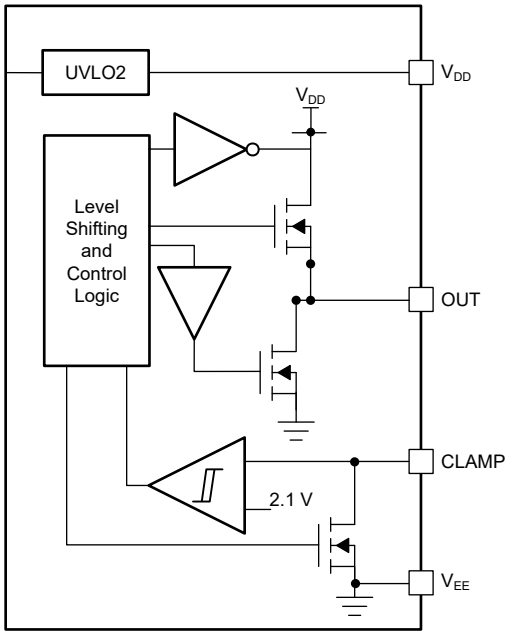


Figure 8-4. Output Stage — Miller Clamp

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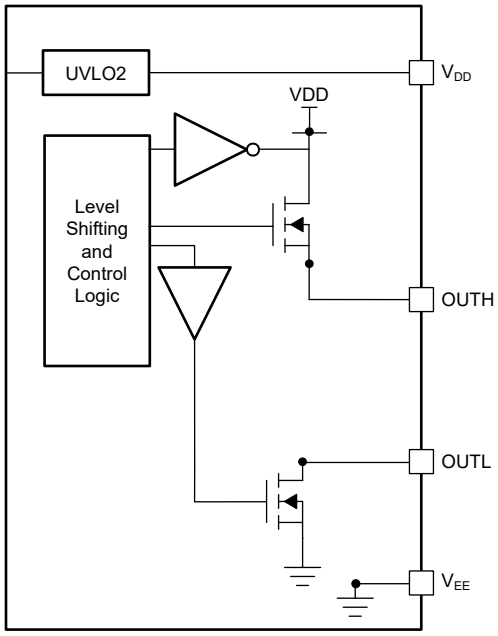


Figure 8-5. Output Stage — Split output

8.3.4 Protection Features

8.3.4.1 Undervoltage Lockout (UVLO)

UVLO functions are implemented for both the VCC-GND and VDD-VEE supplies to prevent an underdriven condition on IGBTs and MOSFETs. When VCC is lower than V_{VCC_ON} at device start-up or lower than V_{VCC_OFF} after start-up, the voltage-supply UVLO feature holds the effected output low, regardless of the input pins (IN+ and IN–) as shown in Table 8-2. The VCC UVLO and VDD UVLO protection has a hysteresis feature (V_{VCC_HYST} and V_{VDD_HYST}). This hysteresis prevents chatter when the power supply produces ground noise; this allows the device to permit small drops in bias voltage, which occurs when the device starts switching and operating current consumption increases suddenly. Table 8-2 and Table 8-3shows the UVLO functions.

Table 8-2. VCC UVLO Logic

CONDITION	INPUTS		OUTPUTS	
	IN+	IN–	OUTH	OUTL
VCC – GND < V_{VCC_ON} during device start-up	H	L	Hi-Z	L
	L	H	Hi-Z	L
	H	H	Hi-Z	L
	L	L	Hi-Z	L
VCC – GND < V_{VCC_OFF} after device start-up	H	L	Hi-Z	L
	L	H	Hi-Z	L
	H	H	Hi-Z	L
	L	L	Hi-Z	L

Table 8-3. VDD UVLO Logic

CONDITION	INPUTS		OUTPUTS	
	IN+	IN–	OUTH	OUTL
VDD – VEE < $V_{VDD_UVLO_ON}$ during device start-up	H	L	Hi-Z	L
	L	H	Hi-Z	L
	H	H	Hi-Z	L
	L	L	Hi-Z	L

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Table 8-3. VDD UVLO Logic (continued)

CONDITION	INPUTS		OUTPUTS	
	IN+	IN–	OUTH	OUTL
VDD – VEE < $V_{VDD_UVLO_OFF}$ after device start-up	H	L	Hi-Z	L
	L	H	Hi-Z	L
	H	H	Hi-Z	L
	L	L	Hi-Z	L

When VCC or VDD drops below the UVLO1 or UVLO2 threshold, a delay, $t_{UVLOVCC_REC}$ or $t_{UVLOVDD_REC}$, occurs on the output when the supply voltage rises above V_{VCC_ON} or $V_{VDD_UVLO_ON}$ again. Figure 8-6 shows this delay.

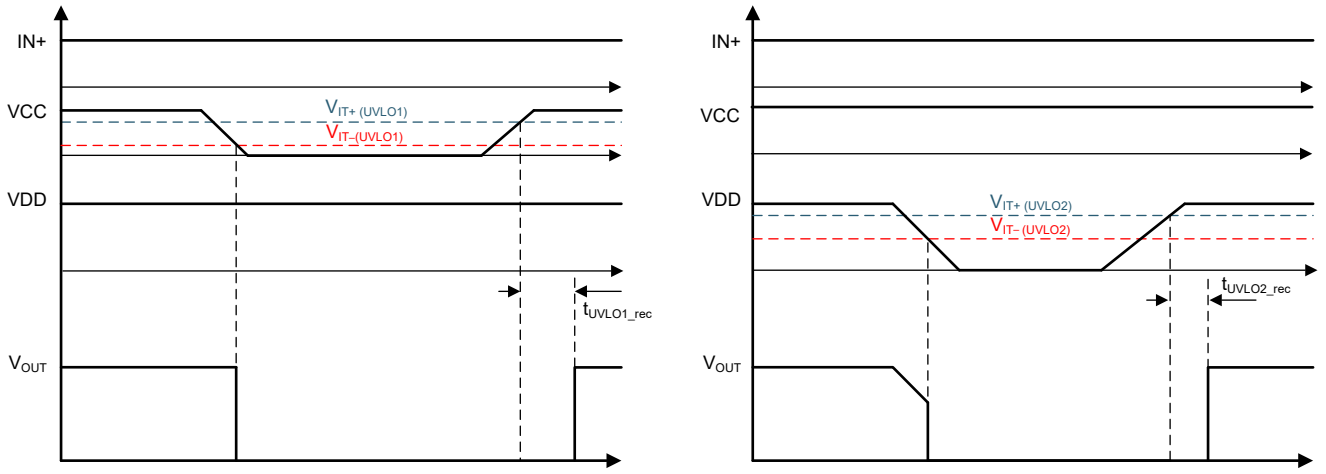


Figure 8-6. UVLO Functions

8.3.4.2 Active Miller Clamp

The active Miller-clamp function helps to prevent a false turn-on of the power switches caused by Miller current in applications where a unipolar power supply is used. The active Miller-clamp function is implemented by adding a low impedance path between the power-switch gate terminal and ground (VEE) to sink the Miller current. With the Miller-clamp function, the power-switch gate voltage is clamped to less than 2V during the off state.

8.3.4.3 Short-Circuit Clamping

The short-circuit clamping function is used to clamp voltages at the driver output slightly higher than the VDD voltage during short-circuit conditions. The short-circuit clamping function helps protect the IGBT or MOSFET gate from overvoltage breakdown or degradation. The short-circuit clamping function is implemented by adding a diode connection between the dedicated pins and the VDD pin inside the driver. The internal diodes can conduct up to 500mA current for a duration of 10µs and a continuous current of 20mA. Use external Schottky diodes to improve current conduction capability as needed.

8.3.5 Diode Structure in the UCC5520-Q1

Figure 8-7 and Figure 8-8 shows the multiple diodes involved in the ESD protection components of the UCC5520-Q1. This provides a pictorial representation of the absolute maximum rating for the device.

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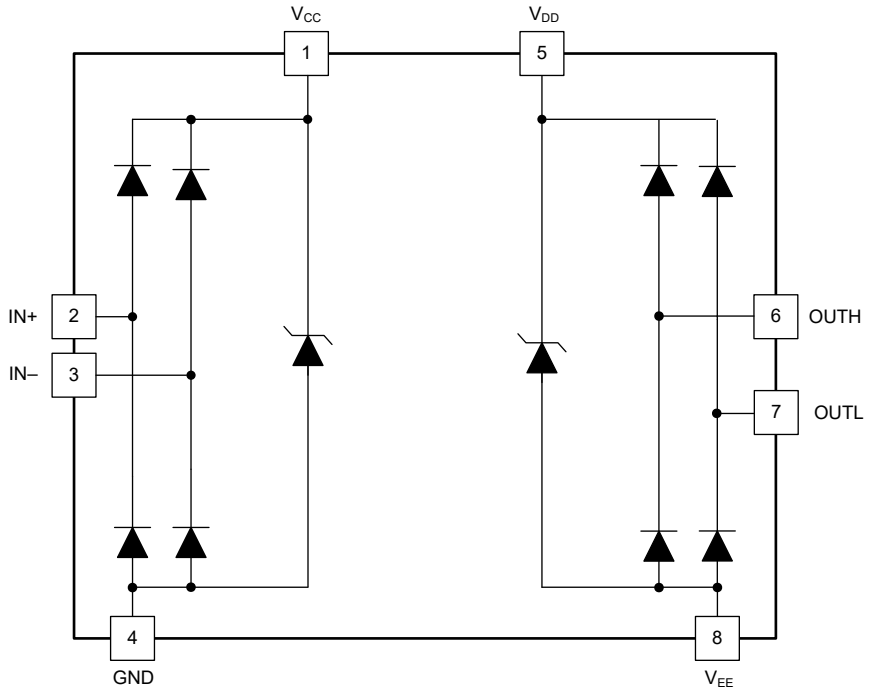


Figure 8-7. ESD Structure — Split Output

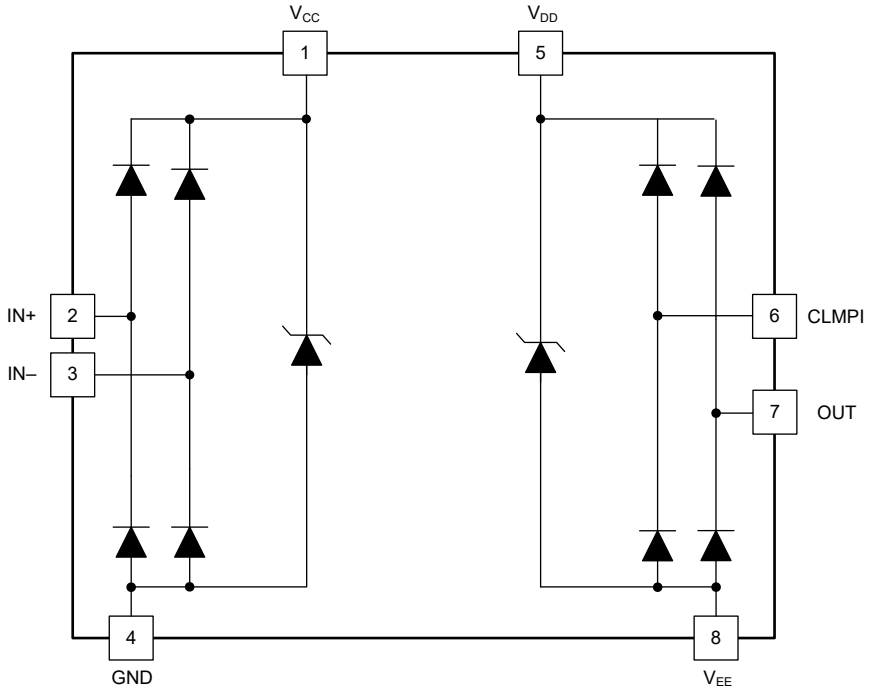


Figure 8-8. ESD Structure — Miller Clamp

8.4 Device Functional Modes

Table 8-4 lists the functional modes for the UCC5520-Q1 assuming VCC and VDD are in the recommended range.

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Table 8-4. Function Table for UCC5520Sx-Q1

IN+	IN–	OUTH	OUTL
Low	X	Hi-Z	Low
X	High	Hi-Z	Low
High	Low	High	High-Z

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

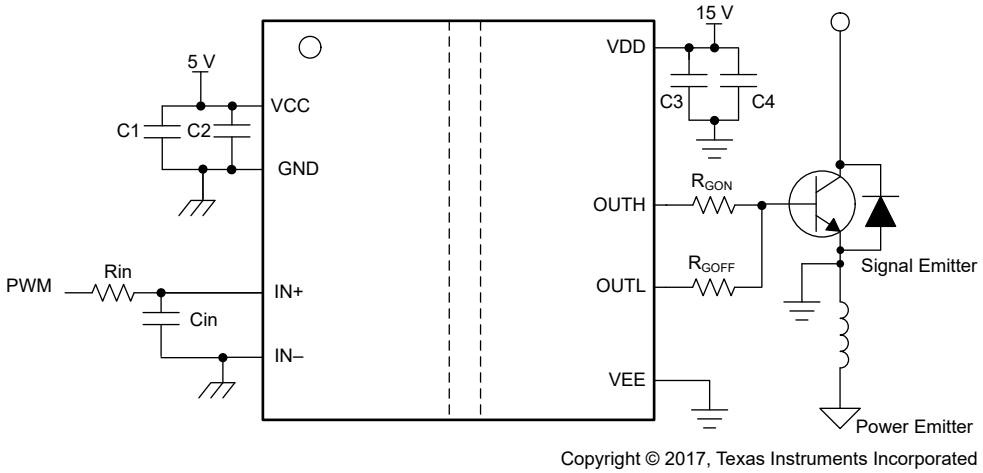
9.1 Application Information

UCC5520-Q1 is a simple, isolated gate driver for power semiconductor devices, such as MOSFETs, IGBTs, or SiC MOSFETs. The family of devices is intended for use in applications such as On board chargers, solar inverters, switched-mode power supplies, and industrial inverters.

The UCC5520-Q1 family of devices has three pinout configurations, featuring split outputs, Miller clamp, and a combination variant offering split output and Miller clamp. The UCC5520Sx-Q1 variant, has a split output, OUTH and OUTL. The two pins can be used to separately decouple the power transistor turnon and turnoff commutations. The UCC5520Mx-Q1 features active Miller clamping, which can be used to prevent false turn-on of the power transistors induced by the Miller current. The UCC5520Px-Q1 variant offers Miller clamp and split outputs while being in a smaller package which enables higher power density for board design.

9.2 Typical Application

The circuit in Figure 9-1 shows a typical application for driving IGBTs.



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Figure 9-1. Typical Application Circuit for UCC5520Sx-Q1

9.3 Power Supply Recommendations

The recommended input supply voltage (VCC) for the UCC5520-Q1 device is from 3V to 18V. The lower limit of the range of output bias-supply voltage (VDD) is determined by the internal UVLO protection feature of the device. The VCC and VDD voltages must not fall below the respective UVLO thresholds for normal operation, or else the gate-driver outputs can become clamped low by the UVLO protection feature. For more information on UVLO, see Section 8.3.4.1. The higher limit of the VDD range depends on the maximum gate voltage of the power device that is driven by the UCC5520-Q1 device, and must not exceed the recommended maximum V_{CC2} of 30V. A local bypass capacitor must be placed between the VDD and VEE pins, with a value from 220nF to 10µF for device biasing. TI recommends placing an additional 100nF capacitor in parallel with the device biasing capacitor for high-frequency filtering. Both capacitors must be positioned as close to the device as possible. Low-ESR, ceramic surface-mount capacitors are recommended. Similarly, a bypass capacitor must also be placed between the VCC and GND pins. Given the small amount of current drawn by the logic circuitry

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within the input side of the UCC5520-Q1 device, this bypass capacitor has a minimum recommended value of 100nF.

9.4 Layout

9.4.1 Layout Guidelines

Pay close attention to PCB layout to achieve peak performance for the UCC5520-Q1. Below are some key points.

9.4.1.1 Component Placement

- Low-ESR and low-ESL capacitors must be connected close to the device between the VCC and GND pins and between the VDD and VEE pins to bypass noise and to support high peak currents when turning on the external power transistor.
- To avoid large negative transients on VEE pins connected to the switch node, the parasitic inductances between the source of the top transistor and the source of the bottom transistor must be minimized by placing as close as possible.

9.4.1.2 Grounding Considerations

- The gate driver must be placed as close as possible to the transistors. Limiting the high peak currents that charge and discharge the transistor gates to a minimal physical area is essential. This limitation decreases the loop inductance and minimize noise on the gate terminals of the transistors.

9.4.1.3 High-Voltage Considerations

- To confirm isolation performance between the primary and secondary side, one must avoid placing any PCB traces or copper below the driver device.
- A PCB cutout is recommended to prevent contamination that can compromise the isolation performance of the UCC5520-Q1.

9.4.1.4 Thermal Considerations

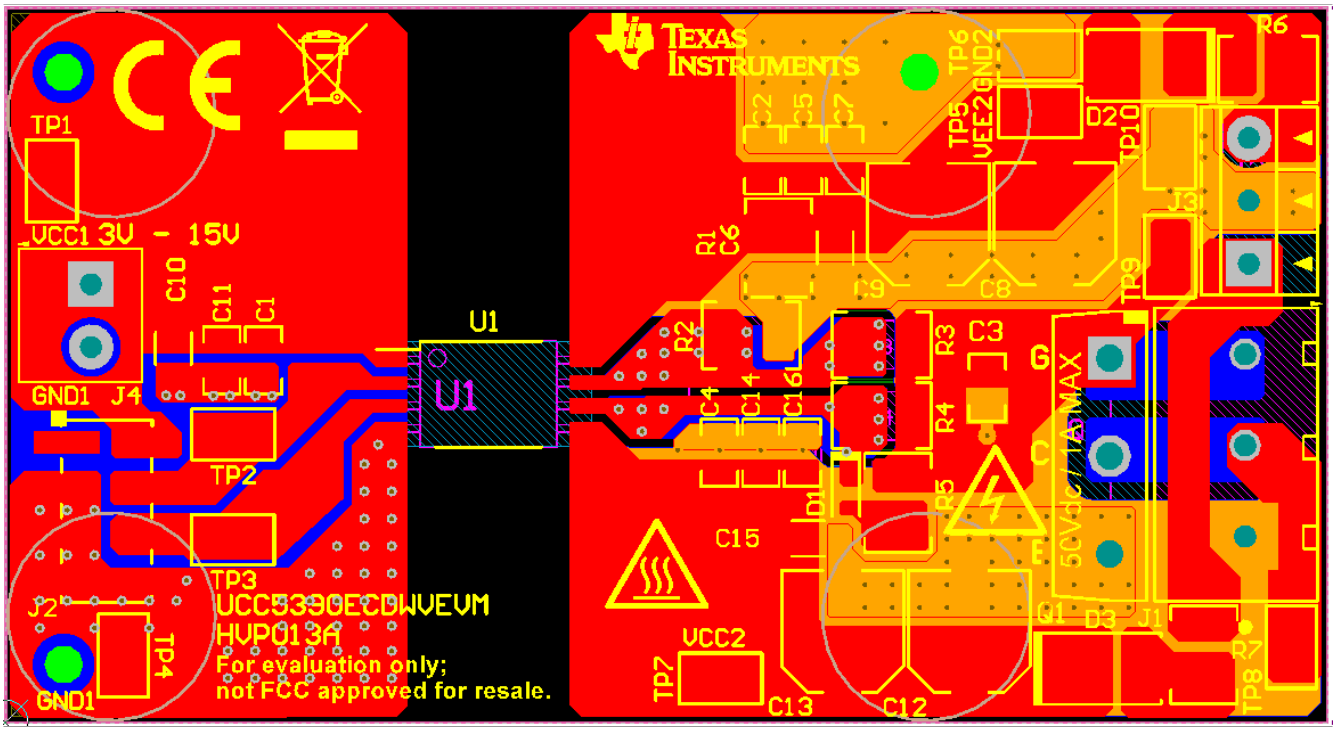
- A large amount of power can be dissipated by the UCC5520-Q1 if the driving voltage is high, the load is heavy, or the switching frequency is high. Proper PCB layout can help dissipate heat from the device to the PCB and minimize junction to board thermal impedance (θ_{JB}).
- Increasing the PCB copper connecting to VDD, VEE pins is recommended, with priority on maximizing the connection to VEE. However, the high voltage PCB considerations mentioned above must be maintained.
- If there are multiple layers in the system, TI also recommends to connecting the VDD and VEE pins to internal ground or power planes through multiple vias of adequate size. However, there must not be any traces/coppers from different high voltage planes overlapping.

9.4.2 Layout Example

The figure below shows a PCB layout example with the signals and key components labeled. The UCC5390ECDWV evaluation module (EVM) is given as an example, available in the same DWV package as the UCC5520-Q1. The UCC5390EC has a split emitter versus Miller clamp so although the layout is not exactly the same, general guidelines and practices still apply. The evaluation board is configurable for the Miller clamp version as well as described in the *UCC5390ECDWV Isolated Gate Driver Evaluation Module User's Guide*.

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A. No PCB traces or copper are located between the primary and secondary side, which confirms isolation performance.

Figure 9-2. Layout Example

The figures below show the top and bottom layer traces and copper.

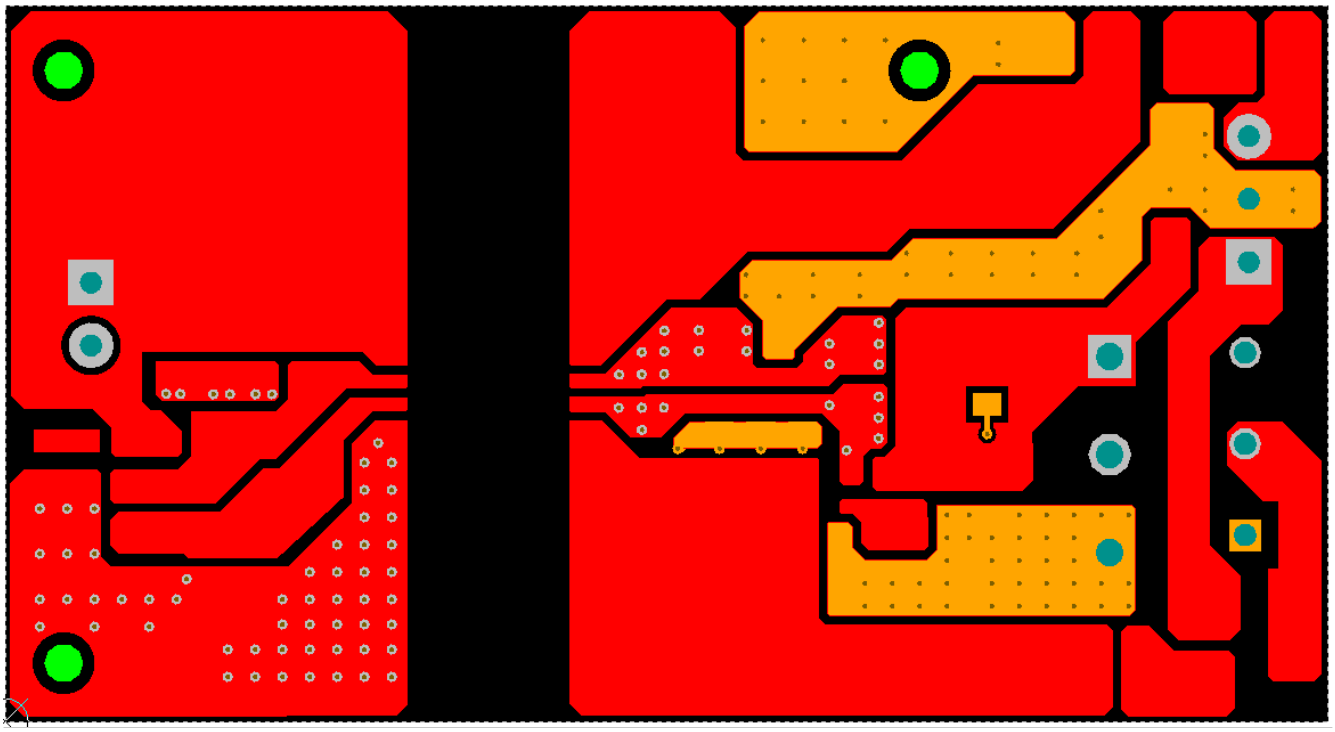


Figure 9-3. Top-Layer Traces and Copper

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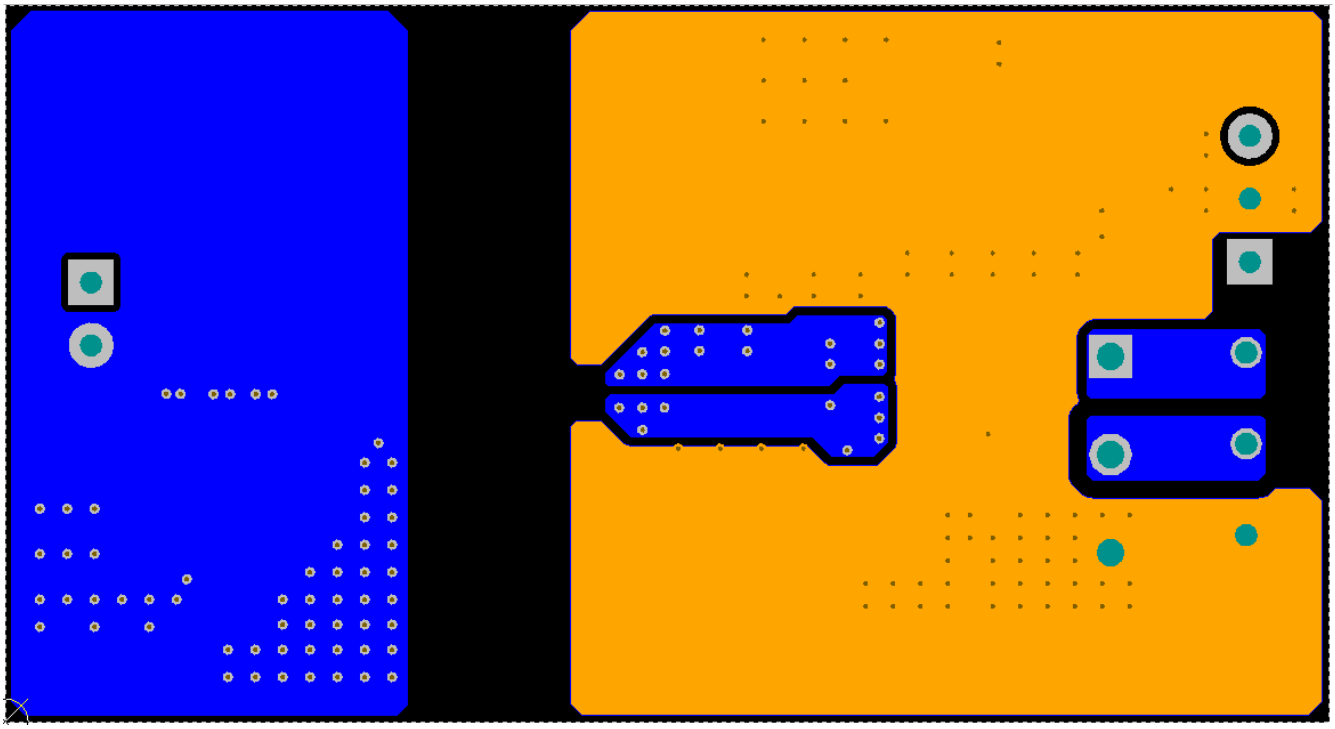


Figure 9-4. Bottom-Layer Traces and Copper (Flipped)

The figure below shows the 3D layout of the top view of the PCB.

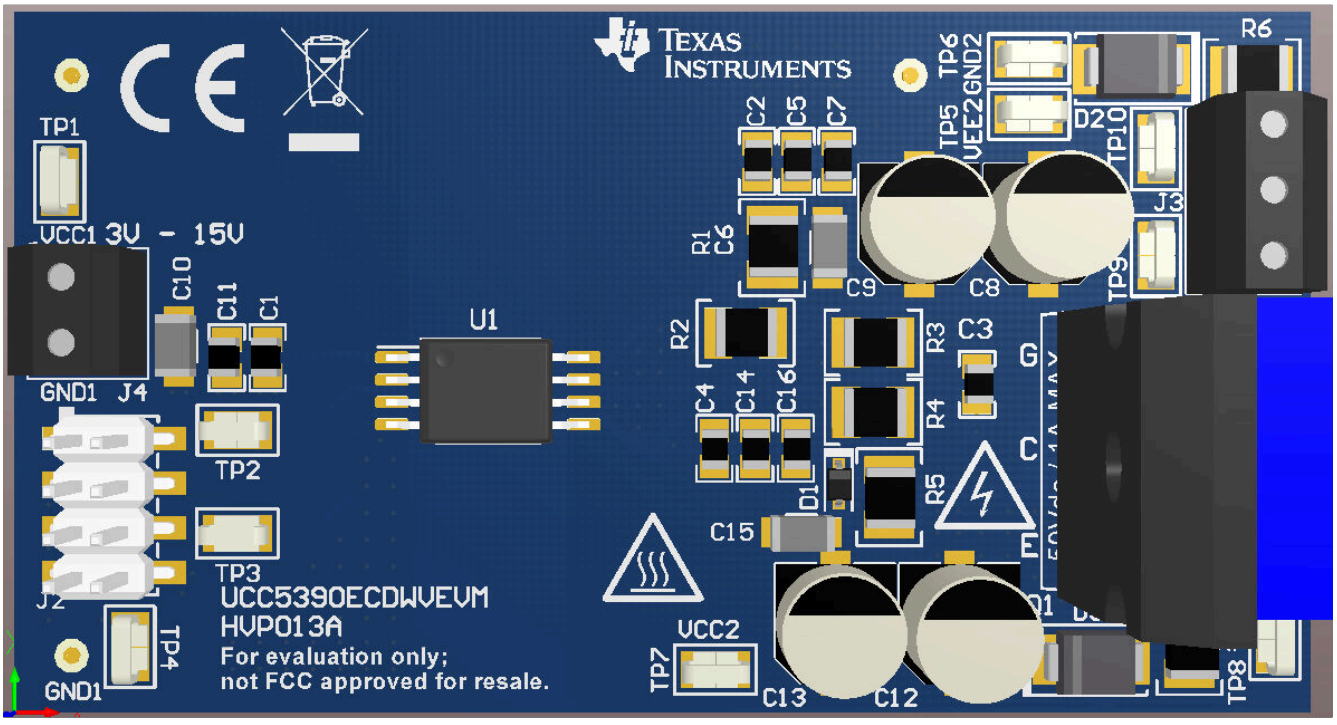


Figure 9-5. 3D PCB View

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10 Device and Documentation Support

10.1 Device Support

10.1.1 Third-Party Products Disclaimer

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10.2 Documentation Support

10.2.1 Related Documentation

For related documentation see the following:

- *Semiconductor and IC Package Thermal Metrics Application Report*
- Isolation Glossary

10.3 Certifications

UL Online Certifications Directory, *"FPPT2.E181974 Nonoptical Isolating Devices - Component"* Certificate Number: 20160516E181974,

VDE Pruf- und Zertifizierungsinstitut Certification, Certificate of Conformity with Factory Surveillance

CQC Online Certifications Directory, "GB4943.1-2011, Digital Isolator Certificate" Certificate Number:CQC16001155011

CSA Online Certifications Directory, "CSA Certificate of Compliance" Certificate Number:70097761, Master Contract Number:220991

10.4 Receiving Notification of Documentation Updates

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ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.8 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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DATE	REVISION	NOTES
November 2026	*	Initial Release

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Mechanical Data

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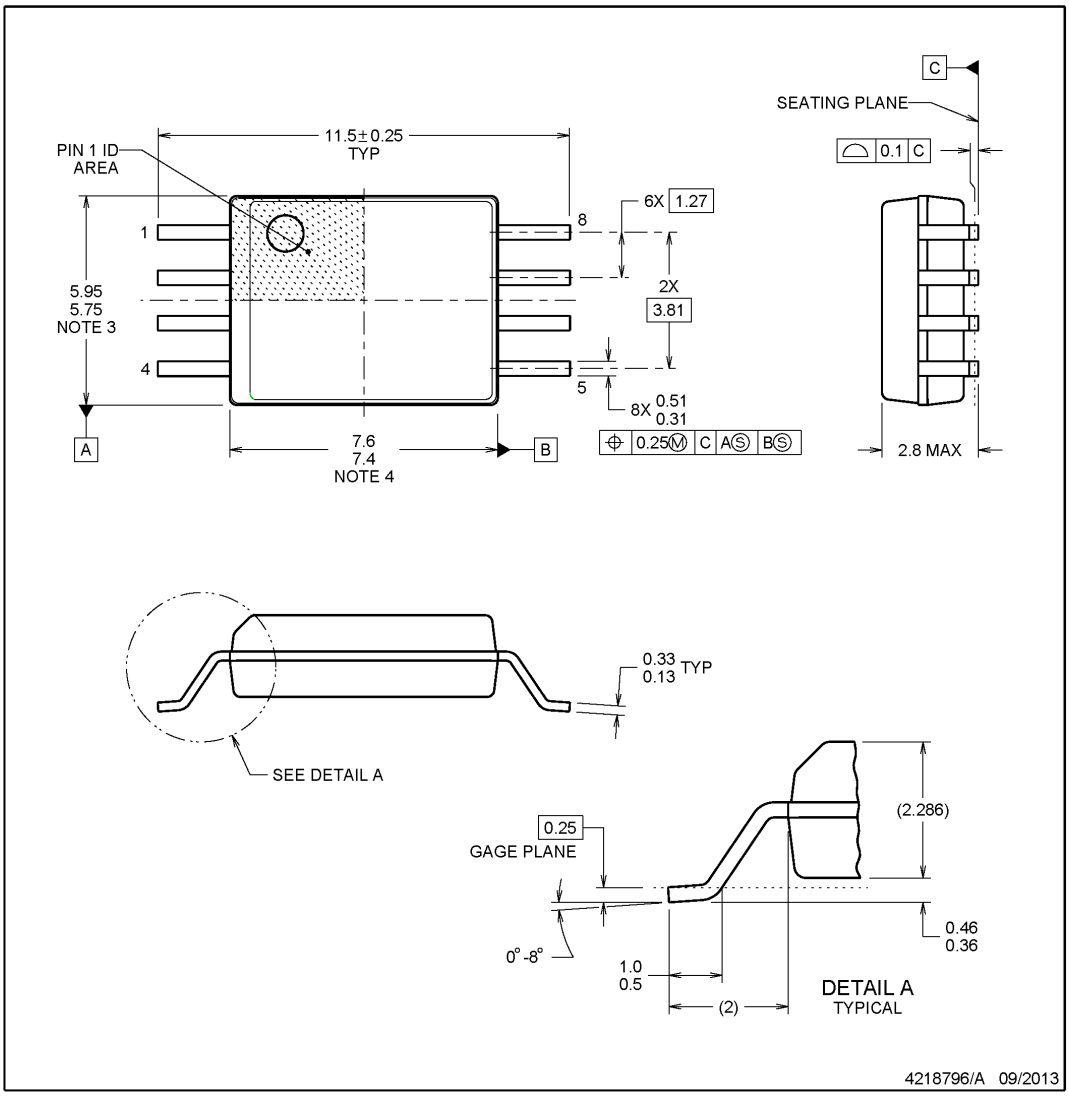
PACKAGE OUTLINE



DWV0008A

SOIC - 2.8 mm max height

SOIC



NOTES:

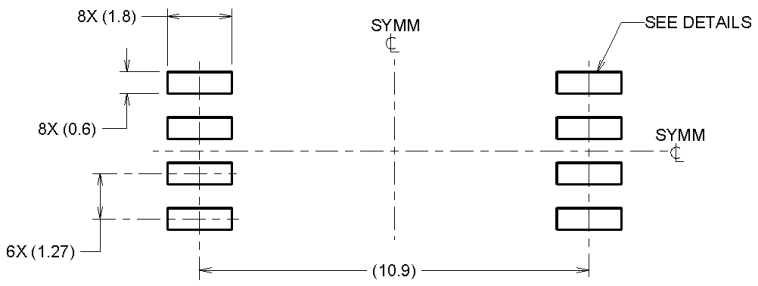
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

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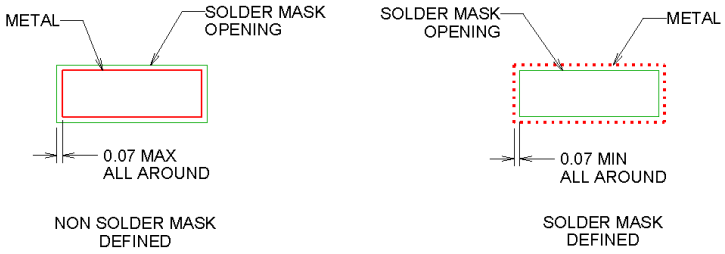
EXAMPLE BOARD LAYOUT

DWV0008A — SOIC - 2.8 mm max height

SOIC



LAND PATTERN EXAMPLE
9.1 mm NOMINAL CLEARANCE/CREEPAGE
SCALE:6X



SOLDER MASK DETAILS

4218796/A 09/2013

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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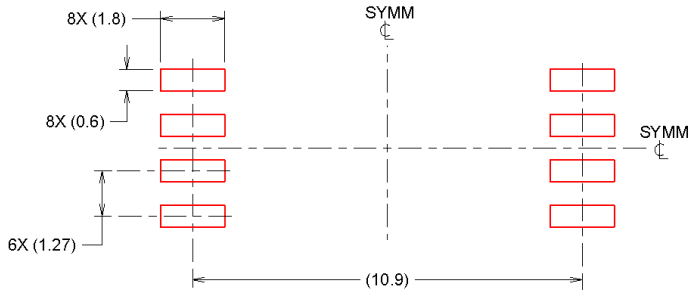
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EXAMPLE STENCIL DESIGN

DWV0008A — SOIC - 2.8 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4218796/A 09/2013

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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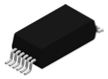
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Logic	logic.ti.com	Security	www.ti.com/security
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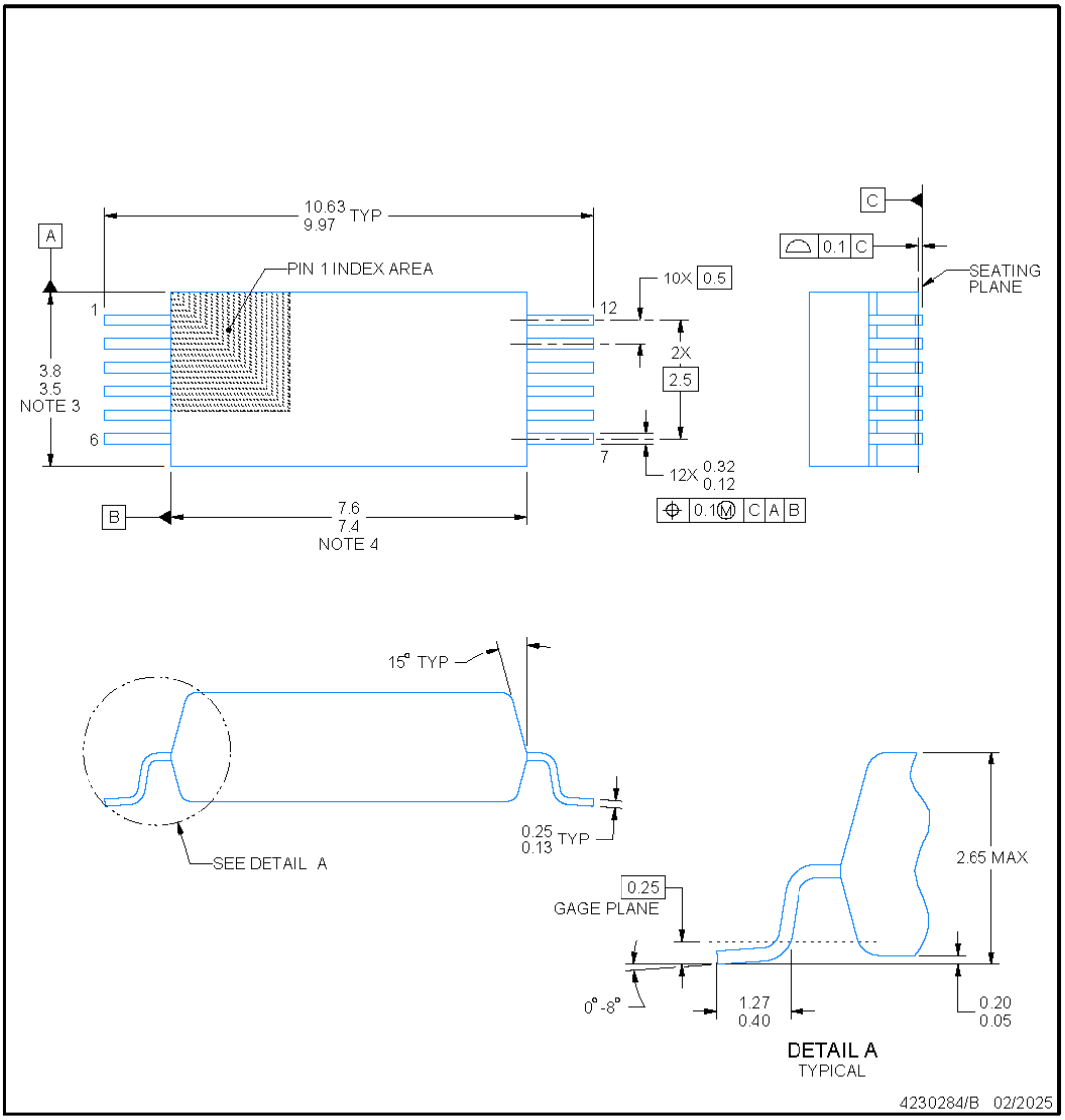
PACKAGE OUTLINE

DFP0012A



SSOP - 2.65 mm max height

SMALL OUTLINE PACKAGE



NOTES:

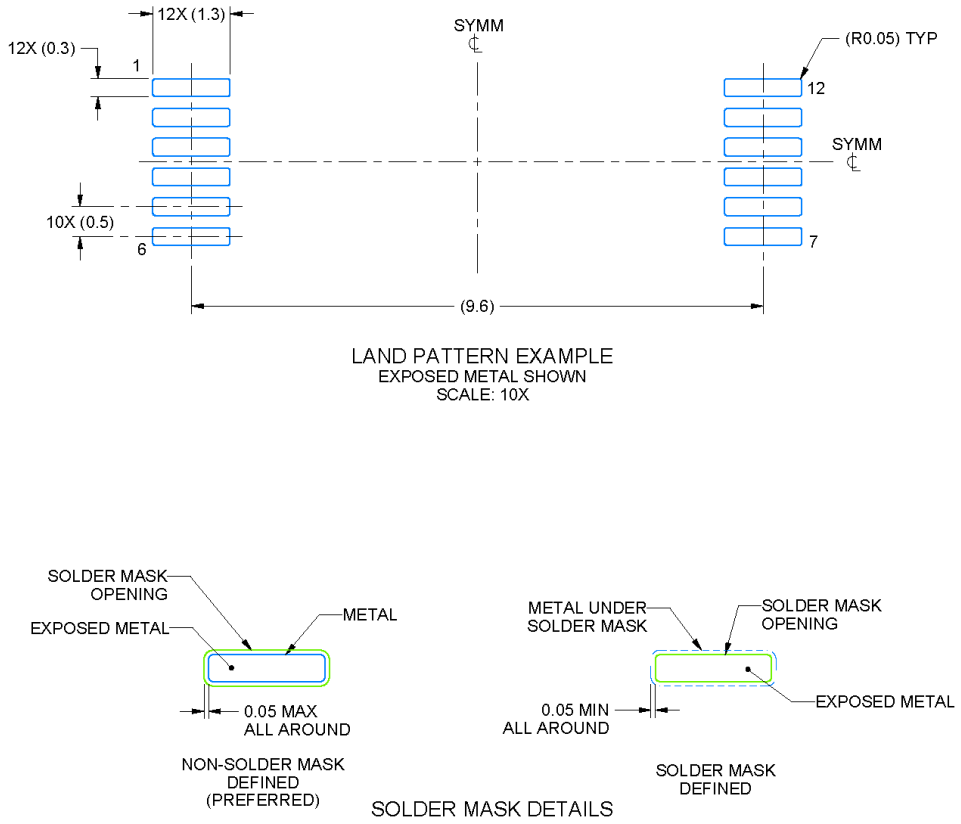
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.

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EXAMPLE BOARD LAYOUT

DFP0012A — **SSOP - 2.65 mm max height**

SMALL OUTLINE PACKAGE



NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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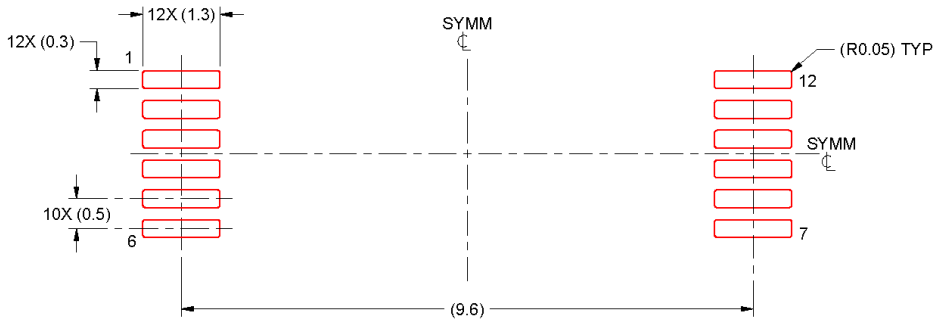
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ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

DFP0012A — **SSOP - 2.65 mm max height**

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4230284/B 02/2025

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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Figure 12-1.

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