XTR117 4-20mA Current-Loop Transmitter

1 Features

- Low quiescent current: 130µA
- 5V regulator for external circuits
- Low span error: 0.05%
- Low nonlinearity error: 0.003%
- Wide-loop supply range: 7.5V to 36V
- Temperature range: –40°C to +125°C
- Packages: VSON-8 and VSSOP-8

2 Applications

- Field transmitter & sensor
- Flow transmitter
- Temperature transmitter
- PLC, DCS, & PAC
- Two-wire, 4-20mA current loop transmitter
- Voltage-to-current amplifier

3 Description

The XTR117 is a precision current output converter designed to transmit analog 4mA to 20mA signals over an industry-standard current loop. The device provides accurate current scaling and output current limit functions.

The on-chip voltage regulator (5V) can be used to power external circuitry. A current return pin (I_{RET}) senses any current used in external circuitry to provide an accurate control of the output current.

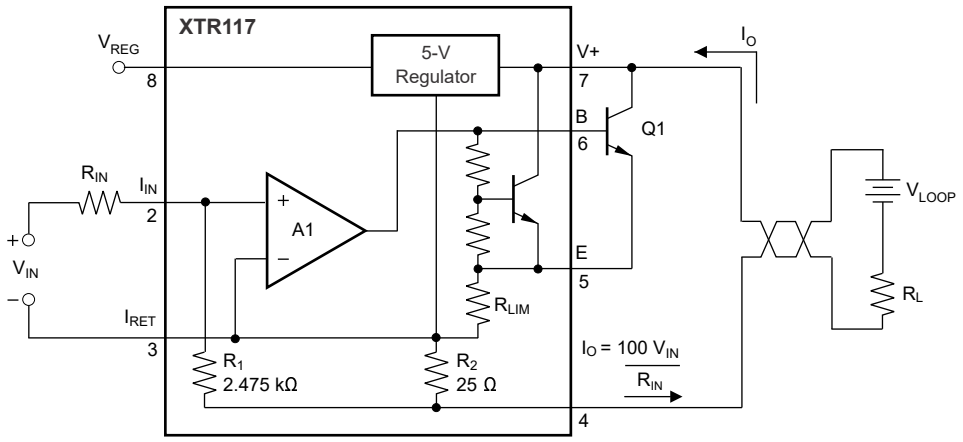
The XTR117 is a fundamental building block of smart sensors using 4mA to 20mA current transmission.

The XTR117 is specified for operation over the extended industrial temperature range, –40°C to +125°C.

Package Information

PRODUCT	PACKAGE(1)	PACKAGE SIZE(2)
XTR117	DGK (VSSOP, 8)	3mm × 4.9mm
	DRB (VSON, 8)	3mm × 3mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Device Comparison Table

Related 4-20mA devices

DEVICE	DESCRIPTION(1)
XTR115	5V regulator output and 2.5V reference output
XTR116	5V regulator output and 4.096V reference output
XTR117	5V regulator output

(1) For complete 4-20mA bridge and RTO conditioner options, see the XTR product family at www.ti.com.

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5 Pin Configuration and Functions

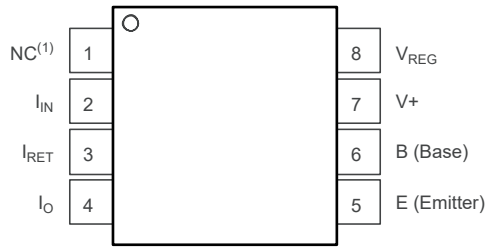


Figure 5-1. DGK Package, 8-Pin VSSOP (Top View)

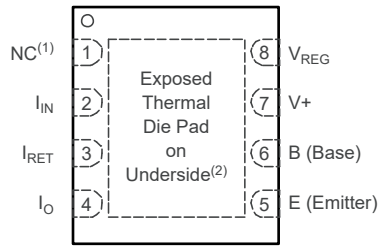


Figure 5-2. DRB Package, 8-Pin VSON (Top View)

(1) NC = No connection.

(2) Connect thermal die pad to I_{RET} or leave unconnected on PCB.

Table 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
I_{IN}	2	I	Current input pin
I_{RET}	3	I	Local ground return pin for V_{REG}
I_O	4	O	Regulated 4mA to 20mA current-loop output
E (Emitter)	5	I	Emitter connection for external transistor
B (Base)	6	O	Base connection for external transistor
V+	7	P	Loop power supply
V_{REG}	8	O	5V regulator voltage output
NC	1	—	Not connected.
Thermal Pad	Pad	—	Thermal Pad. Connect to IRET or leave floating.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

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6 Specifications

Note

TI has qualified multiple fabrication flows for this device. Differences in performance are labeled by chip site origin (CSO). For system robustness, designing for all flows is highly recommended. For more information, please see Section 9.1.

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V+	Power supply (referenced to I_O pin)		40	V
	Input voltage (referenced to I_{RET} pin)	0	V+	V
	Output current limit	Continuous		
	V_{REG} short-circuit	Continuous		
T_A	Operating temperature	–40	125	°C
T_{stg}	Storage temperature	–55	150	°C
T_J	Junction temperature		165	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V+	Power supply voltage	7.5	24	40	V
T_A	Specified temperature	-40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		XTR117		UNIT
		8 PINS		
		DGK (VSSOP)	DRB (VSON)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	173.9	60.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	95.2	33.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.1	4.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	93.7	33.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	66.3	70.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	17.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application note.

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6.5 Electrical Characteristics

at T_A = 25°C, V+ = 24V, R_{IN} = 20kΩ and TIP29C external transistor, all chip site origins (CSO), unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
I_O	Output current equation				$I_O = I_{IN} * 100$		
	Output current, linear range			0.20		25	mA
I_{LIM}	Over-scale limit				32		mA
I_{MIN}	Under-scale limit	I_{REG} = 0			0.13	0.20	mA
SPAN							
S	Span (current gain)				100		A/A
	Error (1)	I_{OUT} = 200µA to 25mA			±0.05	±0.4	%
			T_A = –40°C to +125°C		±3	±20	ppm/°C
	Nonlinearity	I_{OUT} = 200µA to 25mA			±0.003	±0.02	%
INPUT							
V_{OS}	Offset voltage (op amp)	I_{IN} = 40µA			±100	±500	µV
			T_A = –40°C to +125°C		±0.7	±6	µV/°C
			V+ = 7.5V to 36V		±0.1	±2	µV/V
I_B	Bias current	CSO: SHE			–35		nA
		CSO: TID			–50		
	Bias current vs temperature	T_A = –40°C to +125°C	CSO: SHE		150		pA/°C
			CSO: TID		300		
e_n	Noise	0.1Hz to 10Hz			0.6		µVpp
DYNAMIC RESPONSE							
	Small signal bandwidth	C_{LOOP} = 0, R_L = 0			380		kHz
	Slew rate	CSO: SHE			3.2		mA/µs
		CSO: TID			5		
VOLTAGE REGULATOR (V_{REG})							
V_{REG}	Regulator voltage (2)				5		V
	Voltage accuracy	I_{REG} = 0	CSO: SHE		±0.05	±0.1	V
			CSO: TID		±0.003	±0.1	
	Voltage accuracy vs temperature	I_{REG} = 0	T_A = –40°C to +125°C		±0.1		mV/°C
	Voltage accuracy vs power supply, V+	V+ = 7.5V to 36V, I_{REG} = 0	CSO: SHE		1		mV/V
			CSO: TID		0.5		
	Voltage accuracy vs V_{REG} current				See Section 6.6		
	Short circuit current				12		mA
POWER SUPPLY							
I_Q	Quiescent current	CSO: SHE			130	200	µA
		CSO: TID			105	200	
		T_A = –40°C to 125°C				250	

(1) Does not include initial error or TCR of R_{IN}.
(2) Voltage measured with respect to I_{RET} pin.

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6.6 Typical Characteristics

At T_A = +25°C, V+ = 24V, R_{IN} = 20kΩ, TIP29C external transistor, and all chip site origins (CSO) (unless otherwise noted)

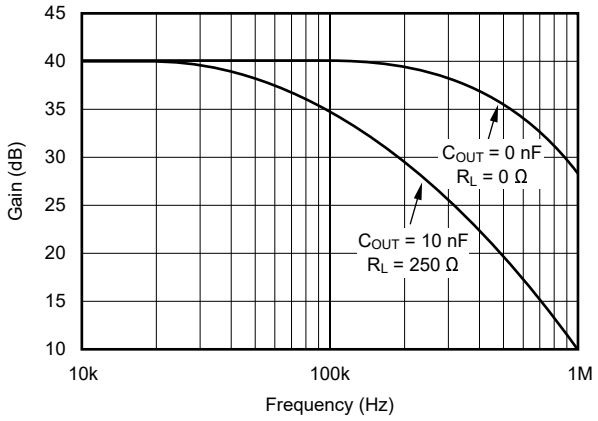


Figure 6-1. Current Gain vs Frequency

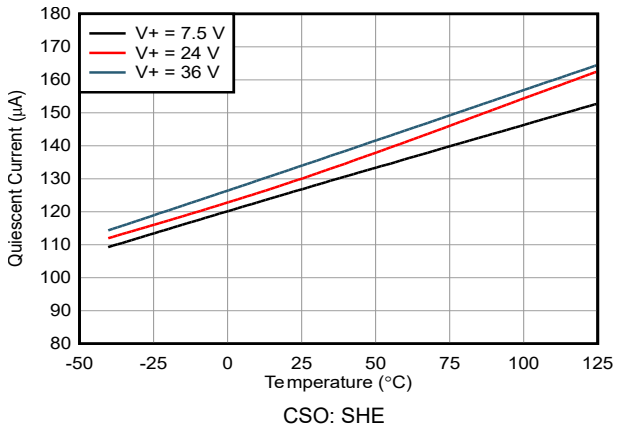


Figure 6-2. Quiescent Current vs Temperature

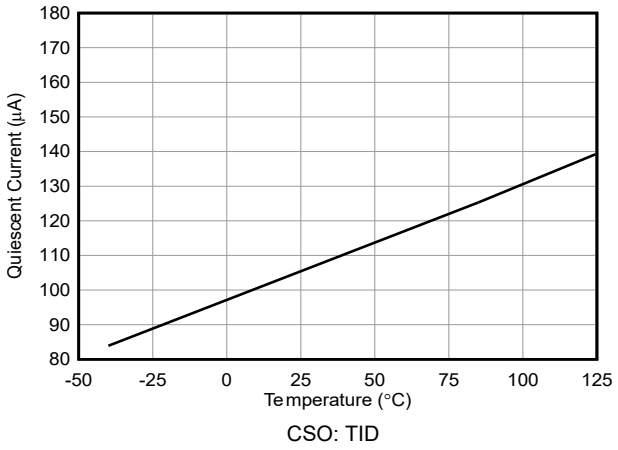


Figure 6-3. Quiescent Current vs Temperature

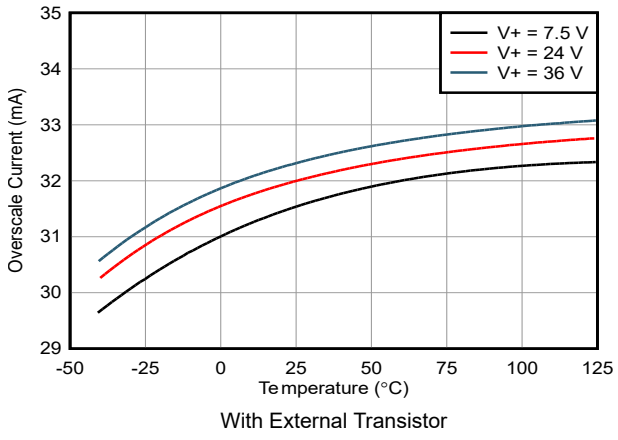


Figure 6-4. Overscale Current vs Temperature

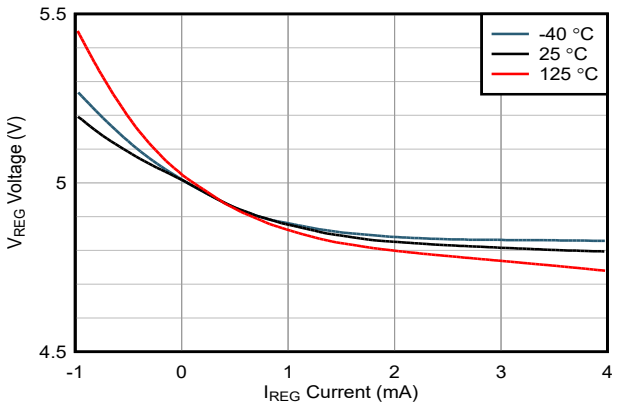


Figure 6-5. V_{REG} Voltage vs V_{REG}Current

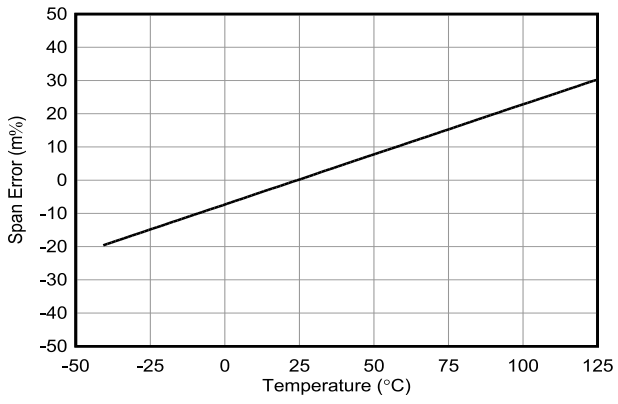


Figure 6-6. Span Error vs Temperature

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6.6 Typical Characteristics (continued)

At T_A = +25°C, V+ = 24V, R_{IN} = 20kΩ, TIP29C external transistor, and all chip site origins (CSO) (unless otherwise noted)

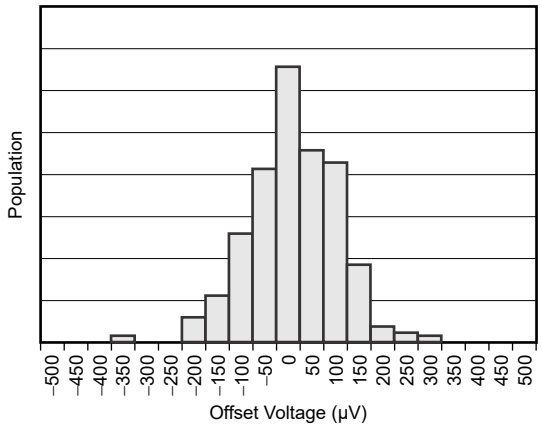


Figure 6-7. Offset Voltage Distribution

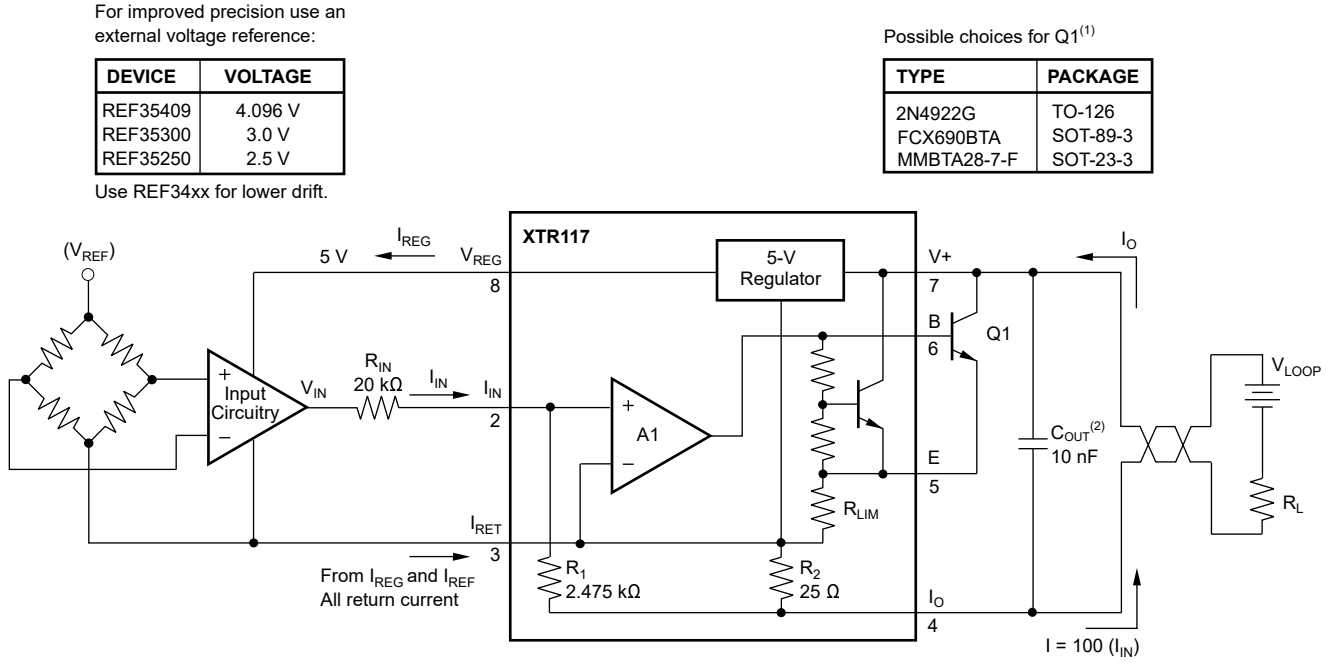
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7 Detailed Description

7.1 Overview

The XTR117 is a precision current output converter designed to transmit analog 4mA to 20mA signals over an industry-standard current loop. Figure 7-1 shows basic circuit connections with representative simplified input circuitry. The XTR117 is a two-wire current transmitter. The input current (pin 2) controls the output current. A portion of the output current flows into the V+ power supply, pin 7. The remaining current flows in Q_1. External input circuitry connected to the XTR117 can be powered from V_{REG}. Current drawn from these terminals must be returned to I_{RET}, pin 3. The I_{RET} pin is a *local ground* for input circuitry driving the XTR117.

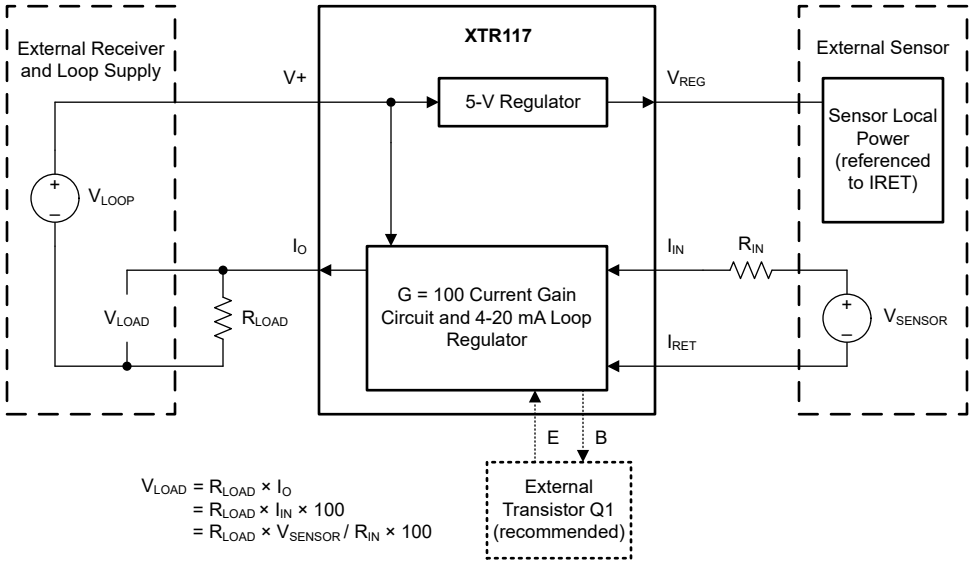
The XTR117 is a current-input device with a gain of 100. A current flowing into pin 2 produces I_O = 100x I_{IN}. The input voltage at the I_{IN} pin is zero (referred to the I_{RET} pin). A voltage input is converted to an input current with an external input resistor, R_{IN}, as shown in Figure 7-1. Typical full-scale input voltages range from 1V and upward. Full-scale inputs greater than 0.5V are recommend to minimize the effects of offset voltage and drift of A1.



(1) See Section 8.1.1.
(2) See Section 8.1.6.

Figure 7-1. Basic Circuit Connections

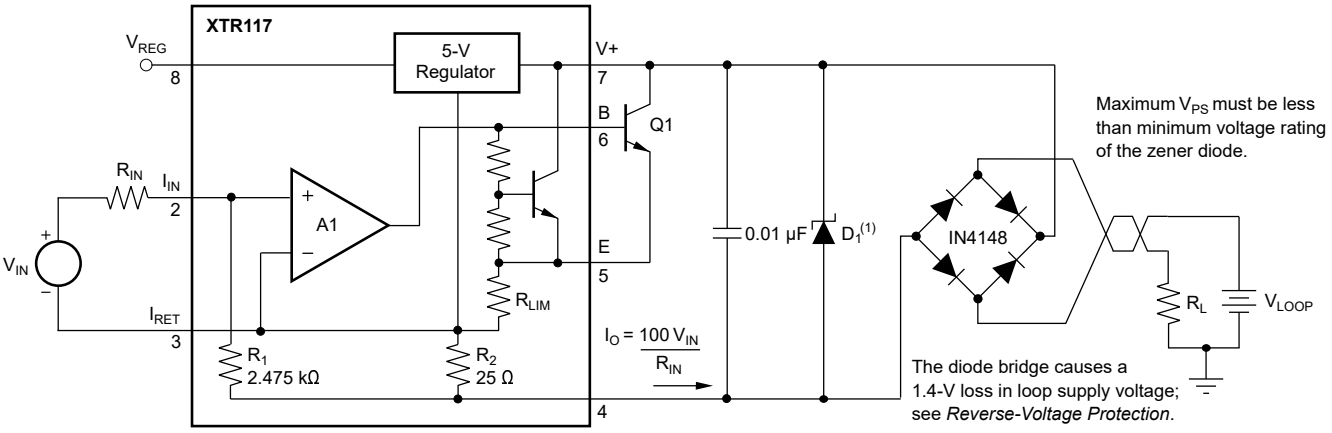
7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Reverse-Voltage Protection

The XTR117 low compliance voltage rating (minimum operating voltage) of 7.5V permits the use of various voltage protection methods without compromising operating range. Figure 7-2 shows a diode bridge circuit that allows normal operation even when the voltage connection lines are reversed. The bridge causes a two-diode drop (approximately 1.4V) loss in loop supply voltage. This voltage drop results in a compliance voltage of approximately 9V, satisfactory for most applications. A diode can be inserted in series with the loop supply voltage and the V+ pin to protect against reverse output connection lines with only a 0.7V loss in loop supply voltage.



(1) 36V Zener diode, such as 1N4753A or P6KE39A. Use lower-voltage Zener diodes with loop power-supply voltages < 30V for increased protection; see Section 7.3.2.

Figure 7-2. Reverse Voltage Operation and Over-Voltage Surge Protection

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7.3.2 Overvoltage Surge Protection

Remote connections to current transmitters can sometimes be subjected to voltage surges. Best practice is to limit the maximum surge voltage applied to the XTR117 to as low as practical. Various Zener diode and surge clamping diodes are specially designed for this purpose. Select a clamp diode with as low a voltage rating as possible for best protection. The absolute maximum power-supply rating on the XTR117 is specified at 40V. Keep overvoltages and transients less than 40V to maintain reliable operation when the supply returns to normal (7.5V to 36V).

Most surge protection Zener diodes have a diode characteristic in the forward direction that conducts excessive current, possibly damaging receiving-side circuitry if the loop connections are reversed. If a surge-protection diode is used, use a series diode or diode bridge for protection against reversed connections.

7.3.3 VSON Package

The XTR117 is offered in a VSON-8 package (also known as SON or DFN). The VSON is a QFN package with lead contacts on only two sides of the bottom of the package. This leadless package maximizes board space and enhances thermal and electrical characteristics through an exposed pad.

VSON packages are physically small, have a smaller routing area, improved thermal performance, and improved electrical parasitics. Additionally, the absence of external leads eliminates bent-lead issues.

The VSON package can be easily mounted using standard printed circuit board (PCB) assembly techniques. See the *QFN/SON PCB Attachment* and *Quad Flatpack No-Lead Logic Packages* application notes, both available for download at www.ti.com.

Connect the exposed leadframe die pad on the bottom of the package to I_{RET} or leave unconnected.

7.4 Device Functional Modes

The device has one mode of operation that applies when operated within the *Recommended Operating Conditions*.

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 External Transistor

The external transistor, Q_1, conducts the majority of the full-scale output current. Power dissipation in this transistor can approach 0.8W with high loop voltage (40V) and 20mA output current. The XTR117 is designed to use an external transistor to avoid on-chip, thermal-induced errors. Heat produced by Q_1 still causes ambient temperature changes that can influence the XTR117 performance. To minimize these effects, locate Q_1 away from sensitive analog circuitry, including the XTR117. Mount Q_1 so that heat is conducted to the outside of the transducer housing.

The XTR117 is designed to use virtually any NPN transistor with sufficient voltage, current, and power rating. Case style and thermal mounting considerations often influence the choice for any given application. Several possible choices are listed in Figure 7-1. A MOSFET transistor does not improve the accuracy of the XTR117 and is not recommended. Although the XTR117 can be used without an additional external transistor, this configuration is not always practical at higher loop voltages and currents because of self-heating concerns.

8.1.2 Minimum Output Current

The quiescent current of the XTR117 (typically 130µA) is the lower limit of the output current. Zero input current (I_{IN} = 0) produces an I_O equal to the quiescent current. Output current does not begin to increase until I_{IN} > I_Q/100. Current drawn from V_{REG} is added to this minimum output current. Up to 3.8mA is available to power external circuitry while still allowing the output current to go to less than 4mA.

8.1.3 Offsetting the Input

A low-scale output of 4mA is produced by creating a 40µA input current. Figure 8-1 shows how this input current is created with the proper value resistor from an external reference voltage (V_{REF}). V_{REG} is used as shown in Figure 8-1, but does not have the temperature stability of a high-quality reference, such as the REF3425.

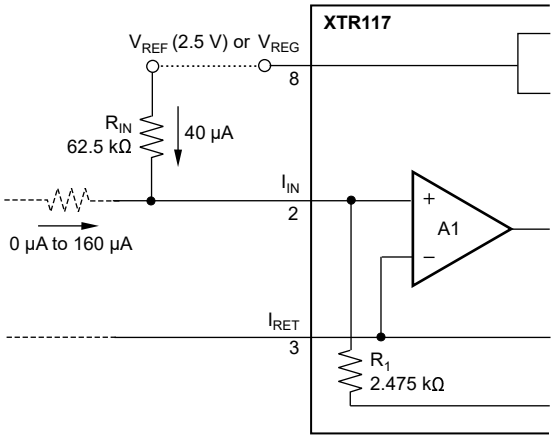


Figure 8-1. Creating Low-Scale Offset

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8.1.4 Radio Frequency Interference

The long wire lengths of current loops invite radio-frequency (RF) interference. RF interference can be rectified by the input circuitry of the XTR117 or preceding circuitry. This effect generally appears as an unstable output current that varies with the position of loop supply or input wiring. Interference cab also enter at the input terminals. For integrated transmitter assemblies with short connections to the sensor, the interference more likely comes from the current-loop connections.

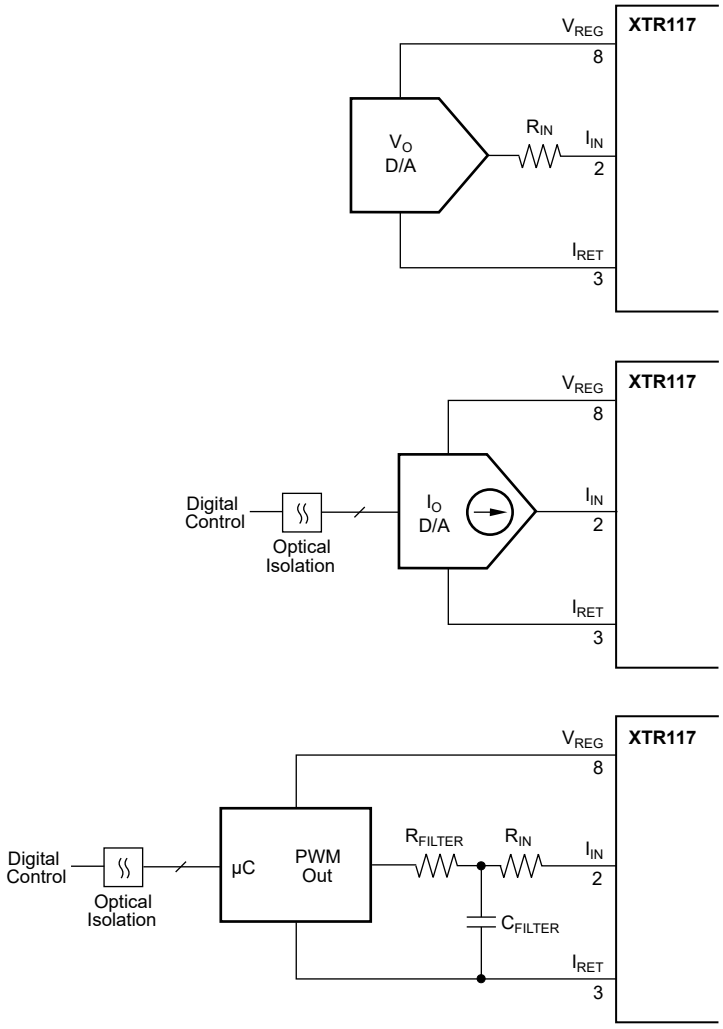


Figure 8-2. Digital Control Methods

8.1.5 Maximum Output Current

The XTR117 provides accurate, linear output up to 25mA. Internal circuitry limits the output current to approximately 32mA to protect the transmitter and loop power or measurement circuitry.

Extending the output current range of the XTR117 is possible by connecting an external resistor from pin 3 to pin 5 to change the current limit value.

CAUTION

All output current must flow through internal resistors; therefore, damage is possible with excessive current. Output currents greater than 45mA can cause permanent damage.

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8.1.6 Circuit Stability

The 4-20mA control-loop stability must be evaluated for any XTR117 design. A 10nF decoupling capacitor between V+ and I_O is recommended for most applications. As this capacitance appears in parallel with the load resistance R_{LOAD} from a stability perspective, the capacitor and resistor form a filter corner that can limit the bandwidth of the system. Therefore, for HART applications, use a bypass capacitance of 2nF to 3nF instead.

For applications with EMI and EMC concerns, use a bypass capacitor with sufficiently low ESR to decouple any ripple voltage from the V_{LOOP} supply. Otherwise, the ripple voltage couples onto the 4mA to 20mA current source, and appears as noise across R_{LOAD} after the current-to-voltage conversion.

8.2 Typical Application

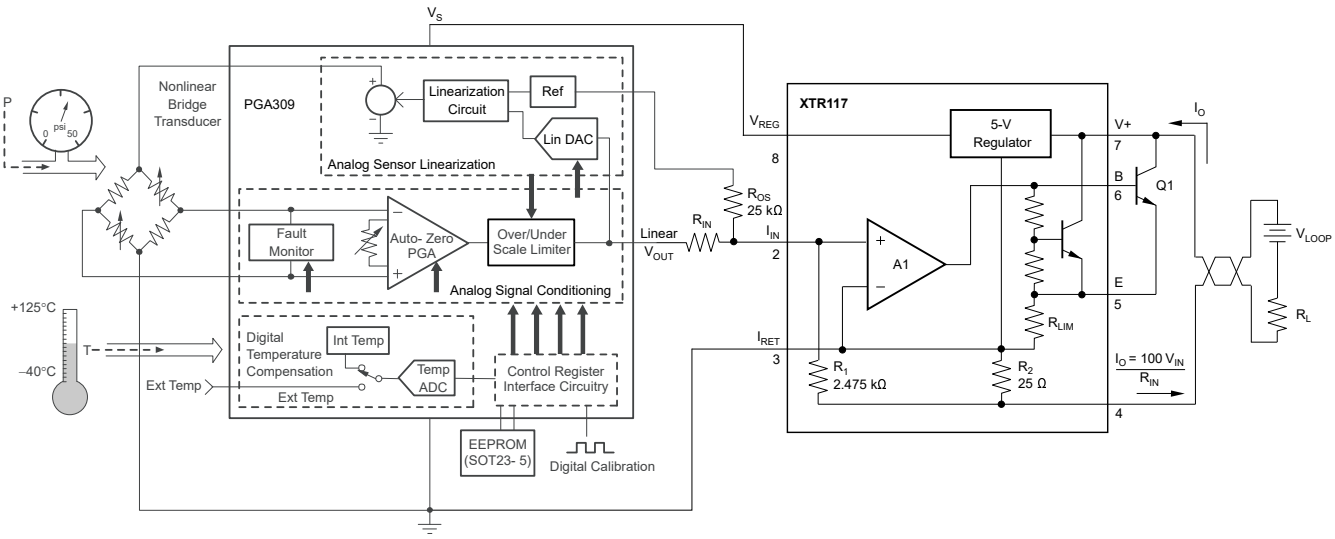


Figure 8-3. Complete 4mA-20mA Pressure Transducer Solution With PGA309 and XTR117

8.3 Layout

8.3.1 Layout Guidelines

The exposed leadframe die pad on the VSON packages can be soldered to a thermal pad on the PCB. A mechanical drawing showing an example layout is attached at the end of this data sheet. Refinements to this layout can be required based on assembly process requirements. Mechanical drawings located at the end of this data sheet list the physical dimensions for the package and pad. The five holes in the landing pattern are optional, and are intended for use with thermal vias that connect the leadframe die pad to the heat-sink area on the PCB.

Soldering the exposed pad significantly improves board-level reliability during temperature cycling, key push, package shear, and similar board-level tests. Even with applications that have low power dissipation, solder the exposed pad to the PCB to provide structural integrity and long-term stability.

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9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Device Support

9.1.1 Device Nomenclature

Table 9-1. Device Nomenclature

Part Number	Definition
XTR117AIDGKR XTR117AIDRBR	The die is manufactured in CSO: SHE or CSO: TID.
XTR117AIDGKT XTR117AIDRBT	The die is manufactured in CSO: SHE.

9.2 Related Documentation

For related documentation see the following:

- Texas Instruments, *Special Function Amplifiers* Precision Labs video series on Current Loop Transmitters
- Texas Instruments, *TIPD126* Bridge Sensor Signal Conditioner with Current Loop Output and EMC Protection Reference Design with XTR117

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

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10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (November 2023) to Revision E (January 2026) **Page**

- Updated Applications sub-bullets to TI.com web links 1
- Added description of device flow information in *Specifications* 5
- Added all chip site origin (CSO) to typical test conditions in *Electrical Characteristics* 5
- Added additional fabrication process specification for Bias Current and Bias Current vs Temperature in *Electrical Characteristics* table 6
- Added additional fabrication process specification for Slew Rate in *Electrical Characteristics* table 6
- Added additional fabrication process specification for V_{REG} Voltage Accuracy and Voltage Accuracy vs Power Supply in *Electrical Characteristics* table 6
- Added additional fabrication process specification for Quiescent Current in *Electrical Characteristics* table 6
- Updated Quiescent Current vs Temperature, Overscale Current vs Temperature, VREG Voltage vs VREG Current, and Span Error vs Temperature to align with absolute maximum temperature rating in *Typical Characteristics* 7
- Added all chip site origin (CSO) to typical test conditions in *Typical Characteristics* 7
- Added additional fabrication process curve for Quiescent Current vs Temperature in the *Typical Characteristics* 7
- Added part number fabrication process information table in *Device Support* 15

Changes from Revision C (May 2012) to Revision D (November 2023) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document 1
- Changed maximum recommended loop supply voltage range from 40V to 36V in *Features*, *Specifications*, and throughout the document 1
- Changed package name MSOP to VSSOP and DFN to VSON throughout the document 1
- Changed Device Information table title to Package Information and updated contents 1
- Added *Pin Configurations and Functions*, *ESD Ratings*, *Recommended Operating Conditions*, *Thermal Information*, *Detailed Description*, *Overview*, *Functional Block Diagram*, *Feature Description*, *Application and Implementation Typical Application*, *Device and Documentation Support*, *Related Documentation*, and *Mechanical, Packaging, and Orderable Information* sections 4
- Updated *Typical Characteristics* title to remove typo 7
- Changed Figure 7-1, *Basic Circuit Connections* 9
- Changed suggested Zener diode part numbers in Figure 7-2, *Reverse Voltage Operation and Overvoltage Surge Protection* 10
- Changed *External Transistor* applications information section to incorporate additional guidance regarding transistor power dissipation and thermal concerns 12
- Added *Circuit Stability* section 14

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
XTR117AIDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	-	Call TI	Level-3-260C-168 HR	-40 to 125	BOZ
XTR117AIDGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	-	Call TI	Level-3-260C-168 HR	-40 to 125	BOZ
XTR117AIDGKT	Obsolete	Production	VSSOP (DGK) | 8	-	-	Call TI	Call TI	-40 to 125	BOZ
XTR117AIDRBR	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BOY
XTR117AIDRBR.B	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BOY

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

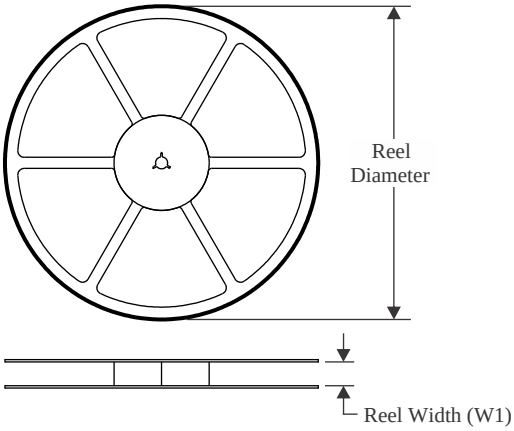
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

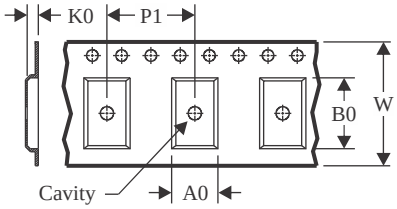
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

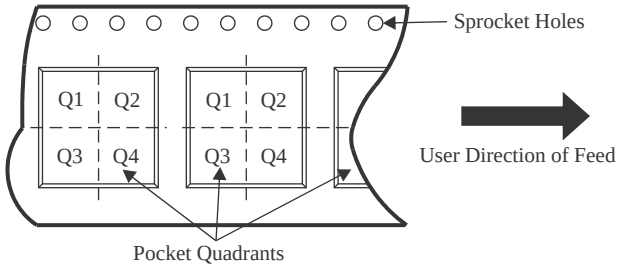


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

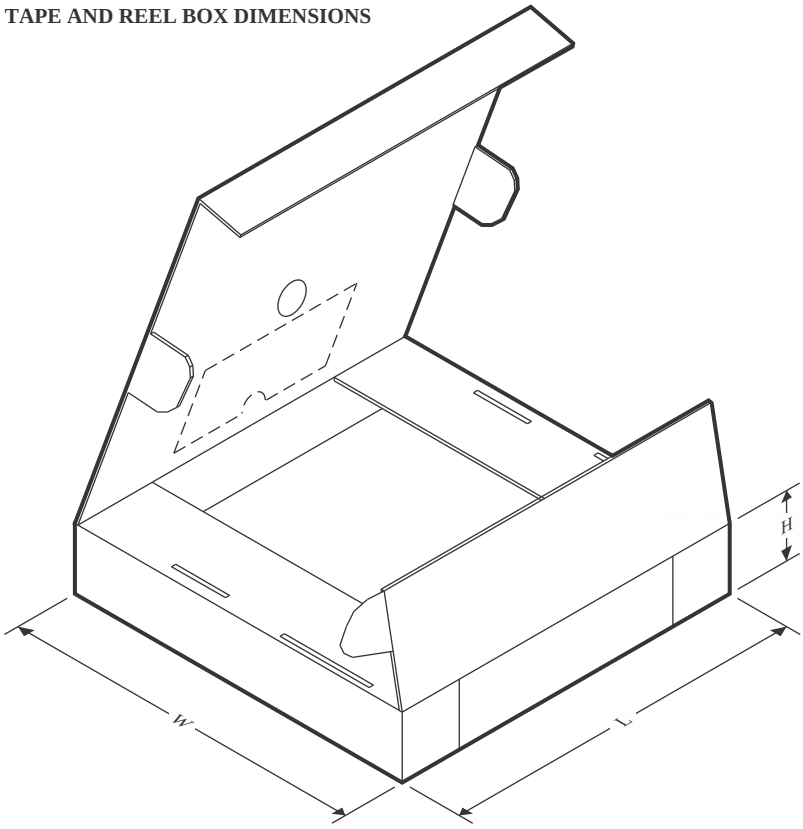
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
XTR117AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
XTR117AIDRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

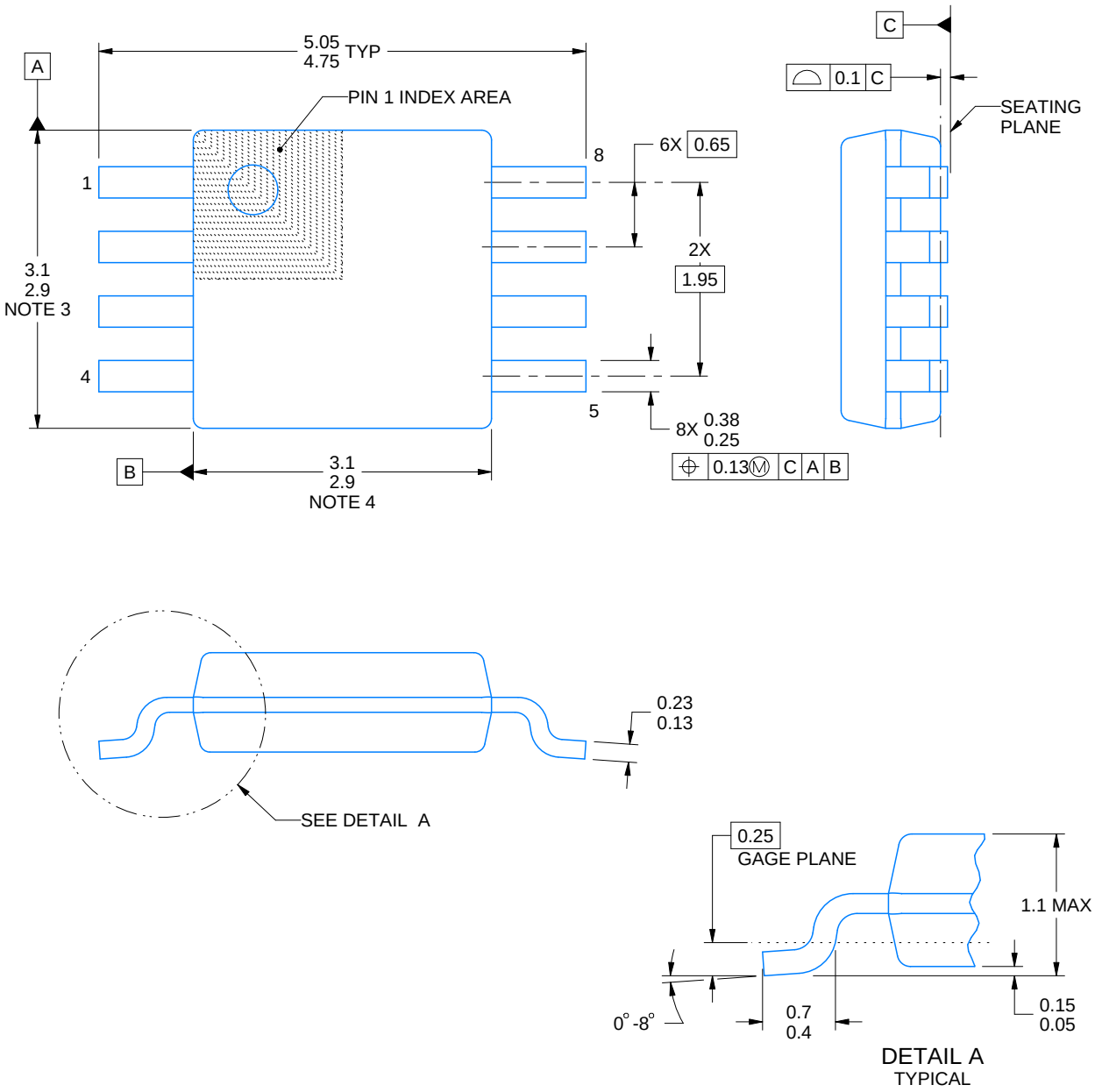
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
XTR117AIDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
XTR117AIDRBR	SON	DRB	8	3000	367.0	367.0	35.0

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

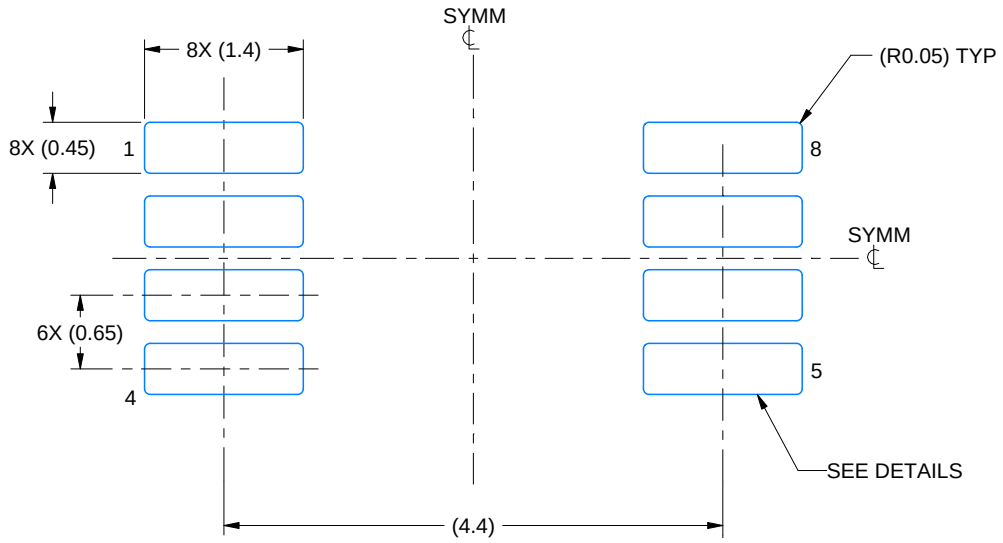
SMALL OUTLINE PACKAGE



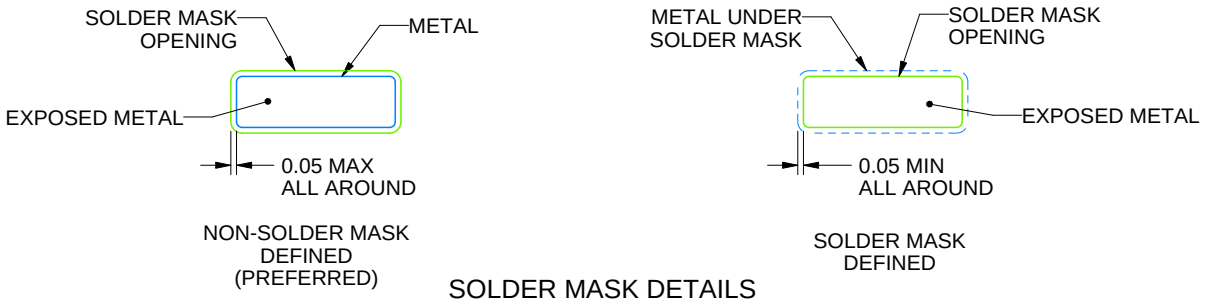
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

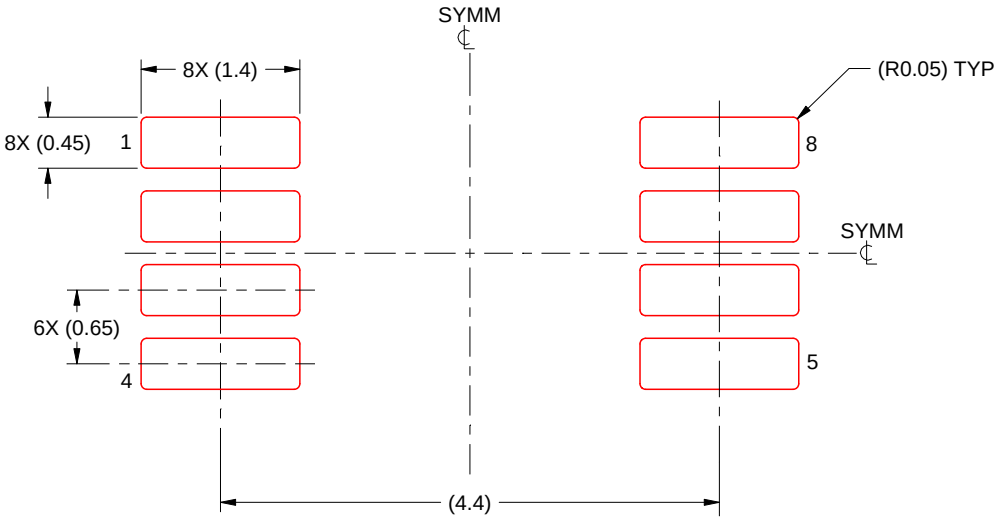


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DRB 8

VSON - 1 mm max height

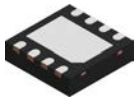
PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203482/L

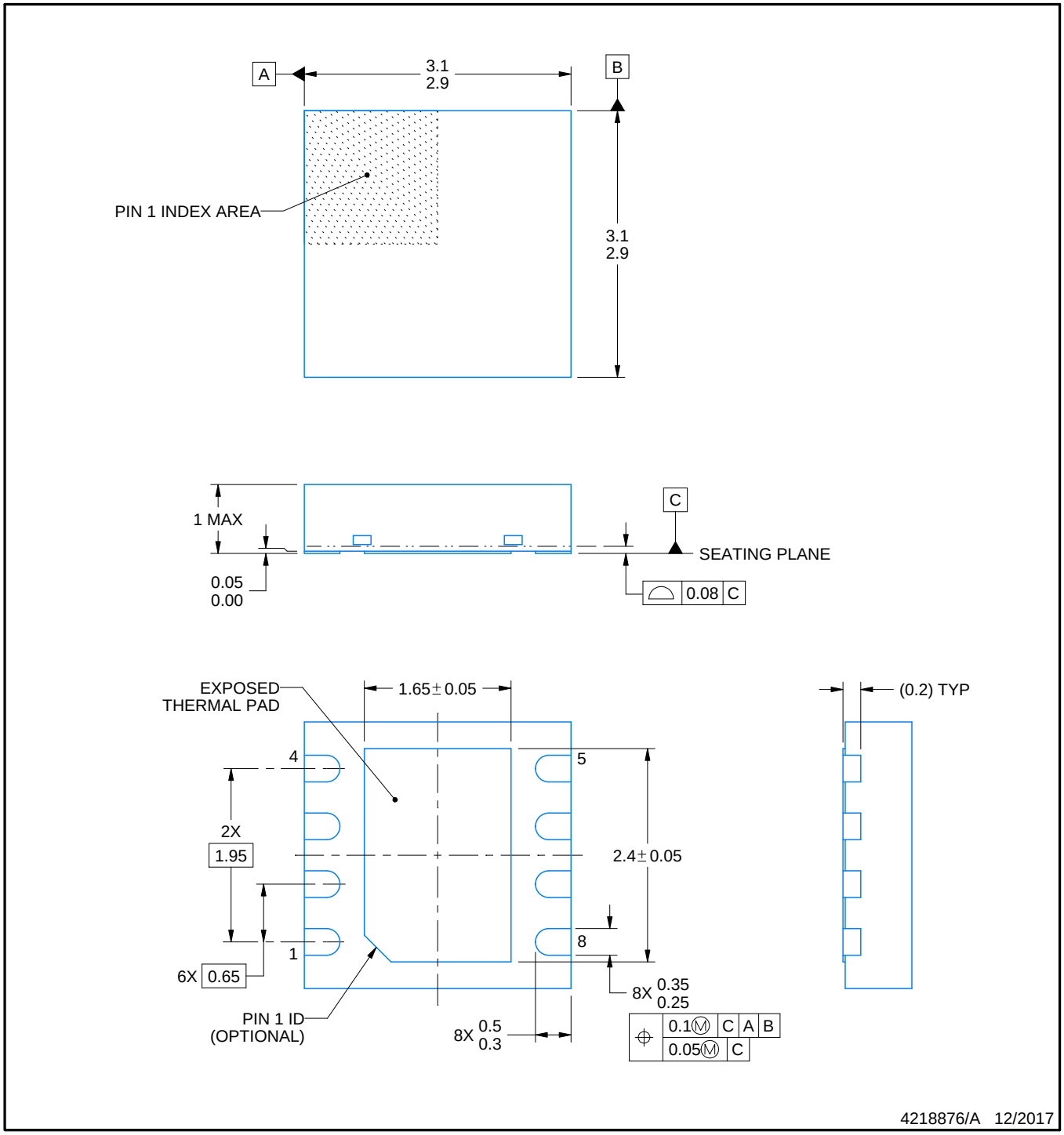
DRB0008B



PACKAGE OUTLINE

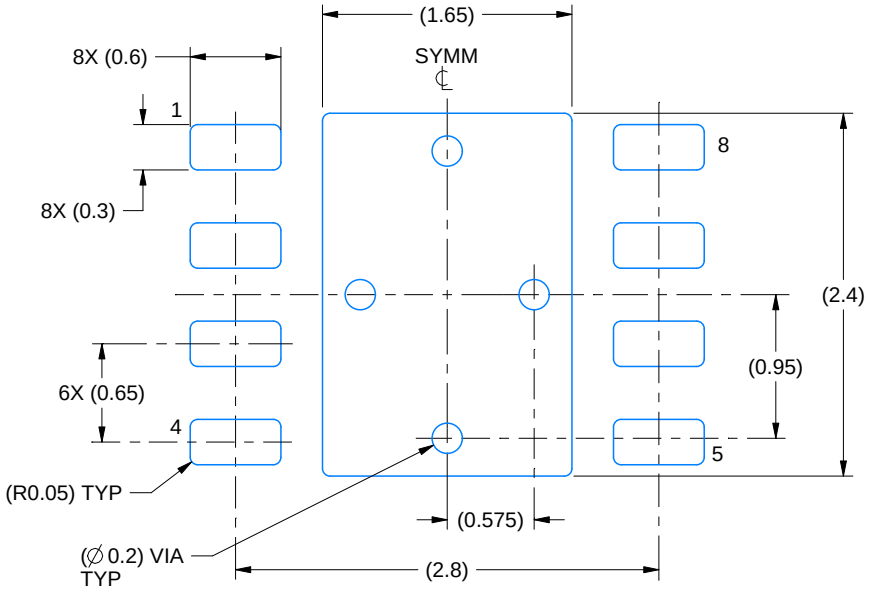
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

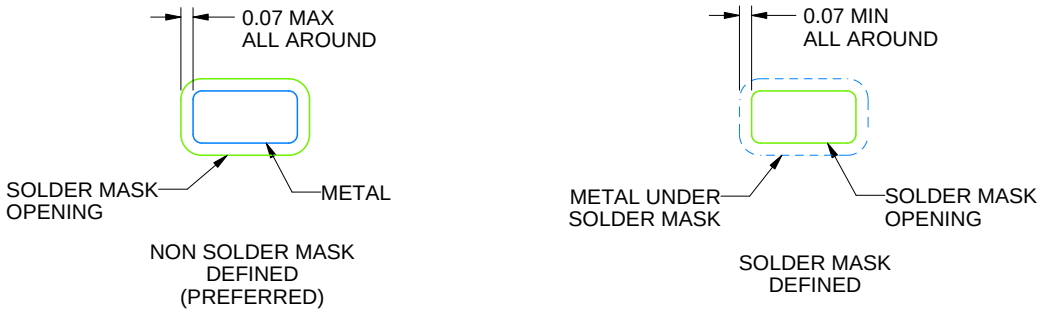


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

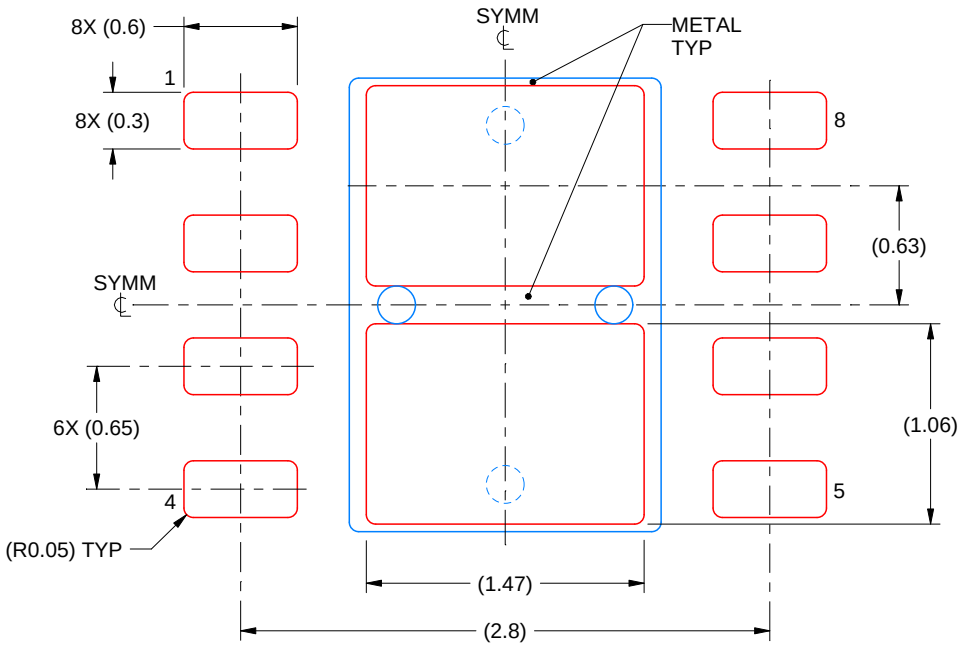


SOLDER MASK DETAILS

4218876/A 12/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218876/A 12/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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