12-Bit, Single or Dual, 3200/1600/800 MSPS RF Sampling ADC

FEATURES

- **Total Ionizing Dose (TID) to 300 krad(Si)**
- **Single Event Latch-up (SEL) > 120 MeV-cm^2/mg**
- **Wide Temperature Range -55°C to +125°C**
- **Low Power Consumption**
- **R/W SPI for Extended Control Mode or Simple Pin Control Mode**
- **Interleaved Timing Automatic with Manual Skew Adjust**
- **Auto-Sync Function for Multi-Chip Systems**
- **Time Stamp Feature to Capture External Trigger**
- **Test Patterns at Output for System Debug**
- **1:1 Non-Demuxed or 1:2 or 1:4 Parallel Demuxed LVDS Outputs**
- **Single 1.9V Power Supply**
- **376 CPGA Hermetic Package**

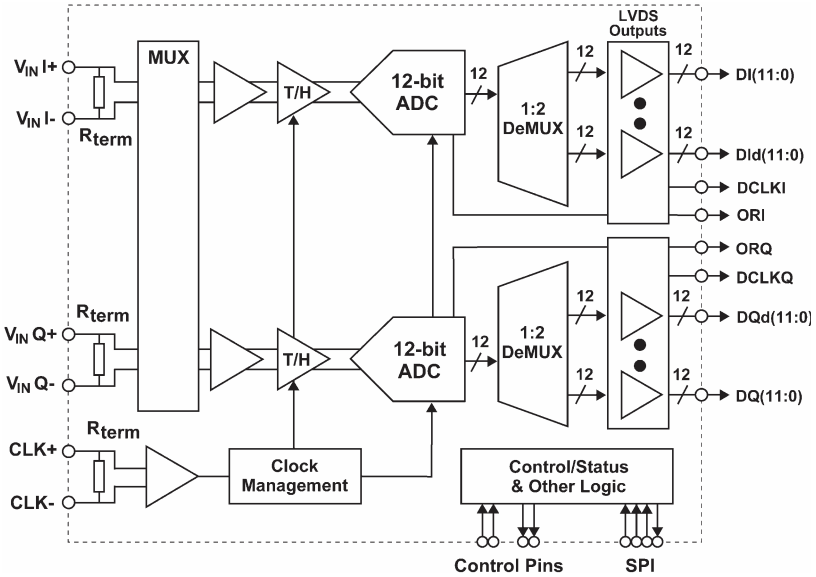
APPLICATIONS

- **Direct RF Down Conversion**
- **Wideband Communications**
- **Data Acquisition Systems**
- **Military Communications**
- **SIGINT**
- **RADAR / LIDAR**

DESCRIPTION

The ADC12D1600QML is a low power, high performance CMOS analog-to-digital converter that digitizes signals at a 12-bit resolution at sampling rates up to 3.2 GSPS in an interleaved mode. It can also be used as a dual channel ADC for sampling rates up to 1.6 GSPS. For sampling rates below 800 MHz, there is a Low Sampling Power Saving Mode (LSPSM) that reduces power consumption to less than 1.4 W per channel (typical). The ADC can support conversion rates as low as 200 MSPS.

The ADC1600QML provides a flexible parallel LVDS interface which has multiple SPI programmable options to facilitate board design and ASIC/FPGA data capture. The LVDS outputs are compatible with IEEE 1596.3-1996 and support programmable common mode voltage. The output of each channel is configurable in either 1:1 non-demuxed or 1:2 demuxed modes. If used as a single channel ADC, there is an option for 1:4 demuxing of the output. The product comes in a hermetic 376 CPGA package for harsh environments.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

Table 1. Key Specifications

	VALUE	UNIT
Resolution	12	Bits
DNL	±0.5	LSB (typ)
IMD_3 (f_{IN} = 2.7 GHz @ -13 dBFS)	-72	dBFS (typ)
IMD_3 (f_{IN} = 2.7 GHz @ -16 dBFS)	-77	dBFS (typ)
Dual 800 MSPS ADC, f_{IN} = 248 MHz		
ENOB	9.3	Bits (typ)
SNR	58.2	dBFS (typ)
SFDR	67.3	dBFS (typ)
Power consumption per channel	1.4	W (typ)
Dual 1600 MSPS ADC, f_{IN} = 248 MHz		
ENOB	8.9	Bits (typ)
SNR	56.6	dBFS (typ)
SFDR	61.5	dBc (typ)
Power consumption per channel	1.9	W (typ)

Connection Diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	GND	V_A	SDO	TPM	NDM	V_A	GND	V_E	GND_E	DId0+	V_DR	DId3+	GND_DR	DId6+	V_DR	DId9+	GND_DR	DId11+	DId11-	GND_DR	A
B	Vbg	GND	ECEb	SDI	CalRun	V_A	GND	GND_E	V_E	DId0-	DId2+	DId3-	DId5+	DId6-	DId8+	DId9-	DId10+	DI0+	DI1+	DI1-	B
C	Rtrim+	GND	Rext+	SCSb	SCLK	GND	V_A	V_E	GND_E	DId1+	DId2-	DId4+	DId5-	DId7+	DId8-	DId10-	DI0-	V_DR	DI2+	DI2-	C
D	V_A	Rtrim-	Rext-	GND	GND	CAL	VbiasI	V_A	V_A	DId1-	V_DR	DId4-	GND_DR	DId7-	V_DR	GND_DR	V_DR	DI3+	DI4+	DI4-	D
E	V_A	Tdiode+	VbiasI	GND													GND_DR	DI3-	DI5+	DI5-	E
F	V_A	GND_TC	Tdiode-	VbiasQ	AA		GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND_DR	DI6+	DI6-	GND_DR	F
G	V_TC	GND_TC	V_TC	V_TC	AB	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	DI7+	DI7-	DI8+	DI8-	G
H	VinI+	V_TC	GND_TC	V_A	AC	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	DI9+	DI9-	DI10+	DI10-	H
J	VinI-	GND_TC	V_TC	VbiasI	AD	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_DR	DI11+	DI11-	V_DR	J
K	GND	VbiasI	V_TC	GND_TC	AE	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	ORI+	ORI-	DCLKI+	DCLKI-	K
L	GND	VbiasQ	V_TC	GND_TC	AF	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	ORQ+	ORQ-	DCLKQ+	DCLKQ-	L
M	VinQ-	GND_TC	V_TC	VbiasQ	AG	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND_DR	DQ11+	DQ11-	GND_DR	M
N	VinQ+	V_TC	GND_TC	V_A	AH	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	DQ9+	DQ9-	DQ10+	DQ10-	N
P	V_TC	GND_TC	V_TC	V_TC	AJ	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	DQ7+	DQ7-	DQ8+	DQ8-	P
R	V_A	GND_TC	V_TC	V_TC	AK	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_DR	DQ6+	DQ6-	V_DR	R
T	V_A	GND_C	GND_C	GND	AL	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_DR	DQ3-	DQ5+	DQ5-	T
U	GND_C	CLK+	PDI	GND	GND	RCOut1-	VbiasQ	V_A	V_A	DQd1-	V_DR	DQd4-	GND_DR	DQd7-	V_DR	V_DR	GND_DR	DQ3+	DQ4+	DQ4-	U
V	CLK-	DCLK_RST+	PDQ	LSPSM	DES	RCOut2+	RCOut2-	V_E	GND_E	DQd1+	DQd2-	DQd4+	DQd5-	DQd7+	DQd8-	DQd10-	DQ0-	GND_DR	DQ2+	DQ2-	V
W	DCLK_RST-	GND	RSV	DDRPh	RCLK-	V_A	GND	GND_E	V_E	DQd0-	DQd2+	DQd3-	DQd5+	DQd6-	DQd8+	DQd9-	DQd10+	DQ0+	DQ1+	DQ1-	W
Y	GND	V_A	FSR	RCLK+	RCOut1+	V_A	GND	V_E	GND_E	DQd0+	V_DR	DQd3+	GND_DR	DQd6+	V_DR	DQd9+	GND_DR	DQd11+	DQd11-	GND_DR	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

Figure 1. ADC12D1600 Connection Diagram

The center ground pins are for thermal dissipation and must be soldered to a ground plane to ensure rated performance. See SUPPLY/GROUNDING, LAYOUT AND THERMAL RECOMMENDATIONS for more information.

Pin Descriptions and Equivalent Circuits

Table 2. Analog Front-End and Clock Pins

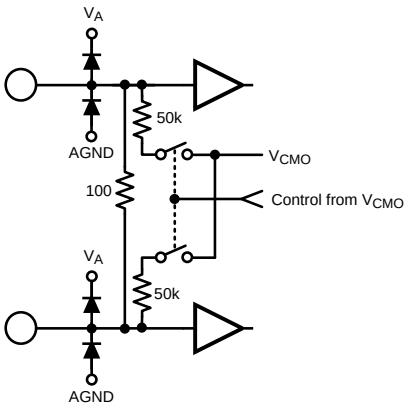
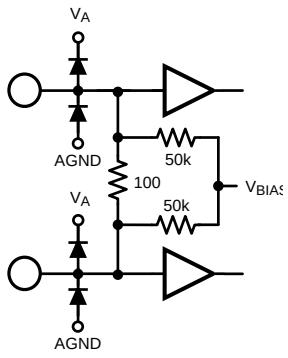
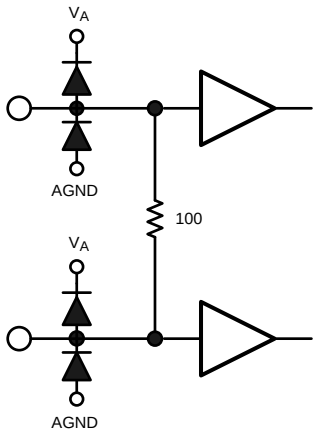
Pin No.	Name	Equivalent Circuit	Description
H1/J1 N1/M1	VinI+/- VinQ+/-		Differential signal I- and Q-inputs. In the Non-Dual Edge Sampling (Non-DES) Mode, each I- and Q-input is sampled and converted by its respective channel with each positive transition of the CLK input. In Non-ECM (Non-Extended Control Mode) and DES Mode, both channels sample the I-input. In Extended Control Mode (ECM), the Q-input may optionally be selected for conversion in DES Mode by the DEQ Bit (Addr: 0**h**, Bit 6). Each I- and Q-channel input has an internal common mode bias that is disabled when DC-coupled Mode is selected. Both inputs must be either AC- or DC-coupled. The coupling mode is selected by the V_{CMO} Pin. In Non-ECM, the full-scale range of these inputs is determined by the FSR Pin; both I- and Q-channels have the same full-scale input range. In ECM, the full-scale input range of the I- and Q-channel inputs may be independently set via the Control Register (Addr: 3**h** and Addr: B**h**). Note that the high and low full-scale input range setting in Non-ECM corresponds to the mid and minimum full-scale input range in ECM. The input offset may also be adjusted in ECM.
U2/V1	CLK+/-		Differential Converter Sampling Clock. In the Non-DES Mode, the analog inputs are sampled on the positive transitions of this clock signal. In the DES Mode, the selected input is sampled on both transitions of this clock. This clock must be AC-coupled.
V2/W1	DCLK_RST+/-		Differential DCLK Reset. A positive pulse on this input is used to reset the DCLKI and DCLKQ outputs of two or more ADC12D1600s in order to synchronize them with other ADC12D1600s in the system. DCLKI and DCLKQ are always in phase with each other, unless one channel is powered down, and do not require a pulse from DCLK_RST to become synchronized. The pulse applied here must meet timing relationships with respect to the CLK input. Although supported, this feature has been superseded by AutoSync.

Table 2. Analog Front-End and Clock Pins (continued)

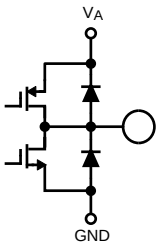
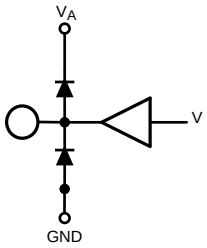
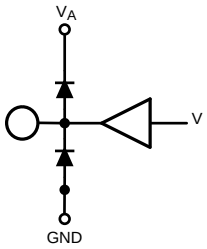
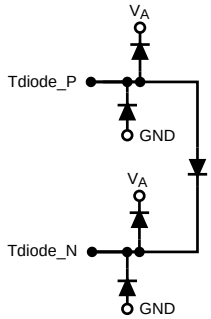
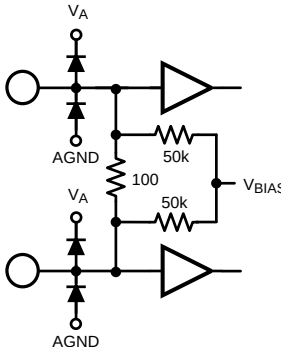
Pin No.	Name	Equivalent Circuit	Description
B1	V_{BG}		Bandgap Voltage Output or LVDS Common-mode Voltage Select. This pin provides a buffered version of the bandgap output voltage and is capable of sourcing/sinking 100 uA and driving a load of up to 80 pF. Alternately, this pin may be used to select the LVDS digital output common-mode voltage. If tied to logic-high, the 1.2V LVDS common-mode voltage is selected; 0.8V is the default.
C3/D3	Rext+/-		External Reference Resistor terminals. A 3.3 kΩ ±0.1% resistor should be connected between Rext+/-. The Rext resistor is used as a reference to trim internal circuits which affect the linearity of the converter; the value and precision of this resistor should not be compromised.
C1/D2	Rtrim+/-		Input Termination Trim Resistor terminals. A 3.3 kΩ ±0.1% resistor should be connected between Rtrim+/-. The Rtrim resistor is used to establish the calibrated 100Ω input impedance of VinI, VinQ and CLK. These impedances may be fine tuned by varying the value of the resistor by a corresponding percentage; however, the tuning range and performance is not tested for such an alternate value.
E2/F3	Tdiode+/-		Temperature Sensor Diode Positive (Anode) and Negative (Cathode) Terminals. This set of pins is used for die temperature measurements. It has not been fully characterized.
Y4/W5	RCLK+/-		Reference Clock Input. When the AutoSync feature is active, and the ADC12D1600 is in Slave Mode, the internal divided clocks are synchronized with respect to this input clock. The delay on this clock may be adjusted when synchronizing multiple ADCs. This feature is available in ECM via Control Register (Addr: E**h**).

Table 2. Analog Front-End and Clock Pins (continued)

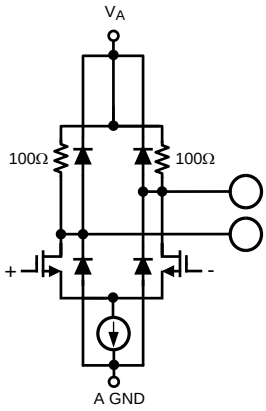
Pin No.	Name	Equivalent Circuit	Description
Y5/U6 V6/V7	RCOut1+/- RCOut2+/-		Reference Clock Output 1 and 2. These signals provide a reference clock at a rate of CLK/4, when enabled, independently of whether the ADC is in Master or Slave Mode. They are used to drive the RCLK of another ADC12D1600, to enable automatic synchronization for multiple ADCs (AutoSync feature). The impedance of each trace from RCOut1 and RCOut2 to the RCLK of another ADC12D1600 should be 100Ω differential. Having two clock outputs allows the auto-synchronization to propagate as a binary tree. Use the DOC Bit (Addr: E**h**, Bit 1) to enable/ disable this feature; default is disabled.

Table 3. Control and Status Pins

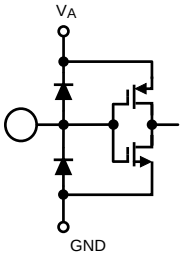
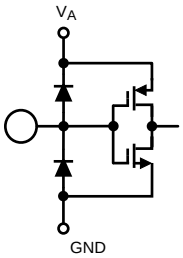
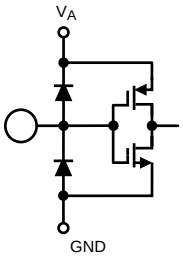
Ball No.	Name	Equivalent Circuit	Description
V5	DES		Dual Edge Sampling (DES) Mode select. In the Non-Extended Control Mode (Non-ECM), when this input is set to logic-high, the DES Mode of operation is selected, meaning that the VinI input is sampled by both channels in a time-interleaved manner. The VinQ input is ignored. When this input is set to logic-low, the device is in Non-DES Mode, i.e. the I- and Q-channels operate independently. In the Extended Control Mode (ECM), this input is ignored and DES Mode selection is controlled through the Control Register by the DES Bit (Addr: 0**h**, Bit 7); default is Non-DES Mode operation.
V4	LSPSM		Low Sampling Power Saving Mode (LSPSM) select. In LSPSM, the power consumption is reduced by approximately 20% and some improvement in performance may be seen. The output will be in SDR in 1:2 Demux mode and DDR in 1:1 non-Demux mode. The maximum sampling rate in LSPSM in non-DES mode is 800 MSPS. When this input is logic-high, the device is in LSPSM and when this input is logic-low, the device is in normal or non-LSPSM.
D6	CAL		Calibration cycle initiate. The user can command the device to execute a self-calibration cycle by holding this input high a minimum of t_{CAL_H} after having held it low a minimum of t_{CAL_L}. This pin is active in both ECM and Non-ECM. In ECM, this pin is logically OR'd with the CAL Bit (Addr: 0**h**, Bit 15) in the Control Register. Therefore, both pin and bit must be set low and then either can be set high to execute an on-command calibration.

Table 3. Control and Status Pins (continued)

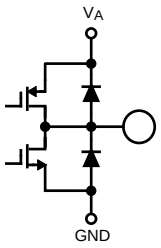
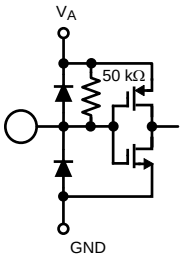
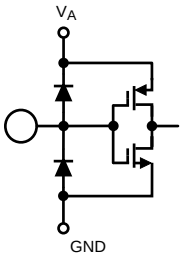
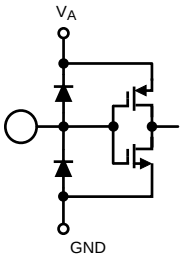
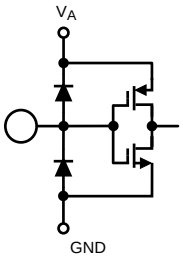
Ball No.	Name	Equivalent Circuit	Description
B5	CalRun		Calibration Running indication. This output is logic-high while the calibration sequence is executing. This output is logic-low otherwise.
U3 V3	PDI PDQ		Power Down I- and Q-channel. Setting either input to logic-high powers down the respective I- or Q-channel. Setting either input to logic-low brings the respective I- or Q-channel to a operational state after a finite time delay. This pin is active in both ECM and Non-ECM. In ECM, each Pin is logically OR'd with its respective Bit. Therefore, either this pin or the PDI and PDQ Bit in the Control Register can be used to power-down the I- and Q-channel (Addr: 0**h**, Bit 11 and Bit 10), respectively.
A4	TPM		Test Pattern Mode select. With this input at logic-high, the device continuously outputs a fixed, repetitive test pattern at the digital outputs. In the ECM, this input is ignored and the Test Pattern Mode can only be activated through the Control Register by the TPM Bit (Addr: 0**h**, Bit 12).
A5	NDM		Non-Demuxed Mode select. Setting this input to logic-high causes the digital output bus to be in the 1:1 Non-Demuxed Mode. Setting this input to logic-low causes the digital output bus to be in the 1:2 Demuxed Mode. This feature is pin-controlled only and remains active during ECM and Non-ECM.
Y3	FSR		Full-Scale input Range select. In Non-ECM, when this input is set to logic-low or logic-high, the full-scale differential input range for both I- and Q-channel inputs is set to the lower or higher FSR value, respectively. In the ECM, this input is ignored and the full-scale range of the I- and Q-channel inputs is independently determined by the setting of Addr: 3**h** and Addr: B**h**, respectively. Note that the high (lower) FSR value in Non-ECM corresponds to the mid (min) available selection in ECM; the FSR range in ECM is greater.

Table 3. Control and Status Pins (continued)

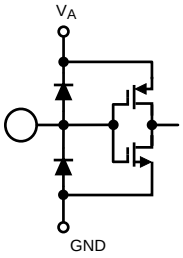
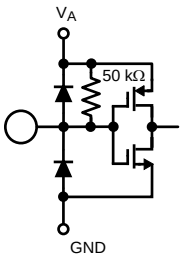
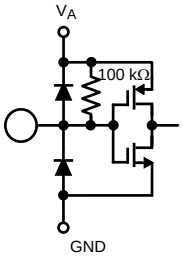
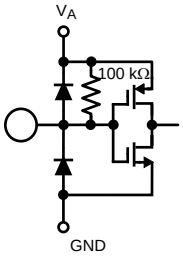
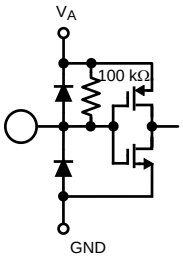
Ball No.	Name	Equivalent Circuit	Description
W4	DDRPh		DDR Phase select. In DDR,this input, when logic-low, selects the 0° Data-to-DCLK phase relationship. When logic-high, it selects the 90° Data-to-DCLK phase relationship, i.e. the DCLK transition indicates the middle of the valid data outputs. In SDR, when this input is logic-low, the output will transition on the rising edge of DCLK. When this input is logic-high output transition will be on the falling edge of DCLK. This pin only has an effect when the chip is in 1:2 Demuxed Mode, i.e. the NDM pin is set to logic-low. In ECM, this input is ignored and the DDR phase is selected through the Control Register by the DPS Bit (Addr: 0**h**, Bit 14); the default is 0° Mode.
B3	$\overline{\text{ECE}}$		Extended Control Enable bar. Extended feature control through the SPI interface is enabled when this signal is asserted (logic-low). In this case, most of the direct control pins have no effect. When this signal is de-asserted (logic-high), the SPI interface is disabled, all SPI registers are reset to their default values, and all available settings are controlled via the control pins.
C4	$\overline{\text{SCS}}$		Serial Chip Select bar. In ECM, when this signal is asserted (logic-low), SCLK is used to clock in serial data which is present on SDI and to source serial data on SDO. When this signal is de-asserted (logic-high), SDI is ignored and SDO is in tri-stated.
C5	SCLK		Serial Clock. In ECM, serial data is shifted into and out of the device synchronously to this clock signal. This clock may be disabled and held logic-low, as long as timing specifications are not violated when the clock is enabled or disabled.
B4	SDI		Serial Data-In. In ECM, serial data is shifted into the device on this pin while $\overline{\text{SCS}}$ signal is asserted (logic-low).

Table 3. Control and Status Pins (continued)

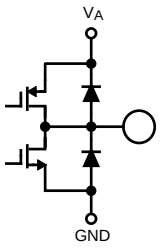
Ball No.	Name	Equivalent Circuit	Description
A3	SDO		Serial Data-Out. In ECM, serial data is shifted out of the device on this pin while $\overline{SCS}$ signal is asserted (logic-low). This output is tri-stated when $\overline{SCS}$ is de-asserted.
W3	RSV	NONE	Reserved. This pin is used for internal purposes and should be connected to GND through a 100 kΩ resistor.
E3	RSV1	NONE	This pin should be decoupled with a 100 nF capacitor vias a low resistance, low inductance path to GND.
F4	RSV2	NONE	This pin should be decoupled with a 100 nF capacitor vias a low resistance, low inductance path to GND.

Table 4. Power and Ground Pins

Ball No.	Name	Equivalent Circuit	Description
A2, A6, B6, C7, D1, D8, D9, E1, F1, H4, N4, R1, T1, U8, U9, W6, Y2, Y6	V_A	NONE	Power Supply for the Analog circuitry. This supply is tied to the ESD ring. Therefore, it must be powered up before or with any other supply.
G1, G3, G4, H2, J3, K3, L3, M3, N2, P1, P3, P4, R3, R4	V_{TC}	NONE	Power Supply for the Track-and-Hold and Clock circuitry.
A11, A15, C18, D11, D15, D17, J17, J20, R17, R20, T17, U11, U15, U16, Y11, Y15	V_{DR}	NONE	Power Supply for the Output Drivers.
A8, B9, C8, V8, W9, Y8	V_E	NONE	Power Supply for the Digital Encoder.
D7, J4, K2	VbiasI	NONE	Bias Voltage I-channel. This is an externally decoupled bias voltage for the I-channel. Each pin should individually be decoupled with a 100 nF capacitor via a low resistance, low inductance path to GND.
L2, M4, U7	VbiasQ	NONE	Bias Voltage Q-channel. This is an externally decoupled bias voltage for the Q-channel. Each pin should individually be decoupled with a 100 nF capacitor via a low resistance, low inductance path to GND.
A1, A7, B2, B7, C2, C6, D4, D5, E4, K1, L1, T4, U4, U5, W2, W7, Y1, Y7, AA2:AA11	GND	NONE	Ground Return for the Analog circuitry.
F2, G2, H3, J2, K4, L4, M2, N3, P2, R2, T2, T3, U1	GND_{TC}	NONE	Ground Return for the Track-and-Hold and Clock circuitry.
A13, A17, A20, D13, D16, E17, F17, F20, M17, M20, U13, U17, V18, Y13, Y17, Y20	GND_{DR}	NONE	Ground Return for the Output Drivers.
A9, B8, C9, V9, W8, Y9	GND_E	NONE	Ground Return for the Digital Encoder.

Table 5. High-Speed Digital Output Pins

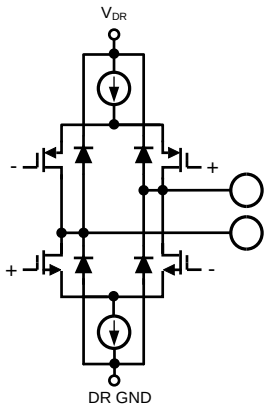
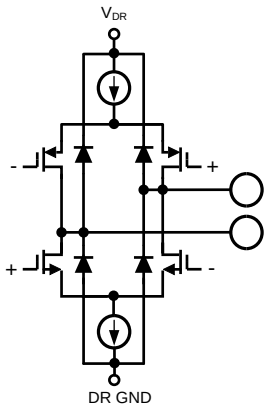
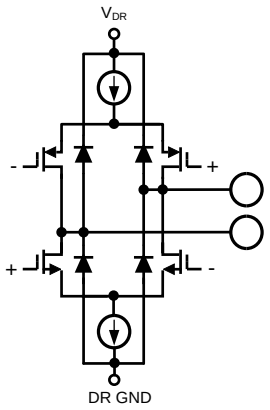
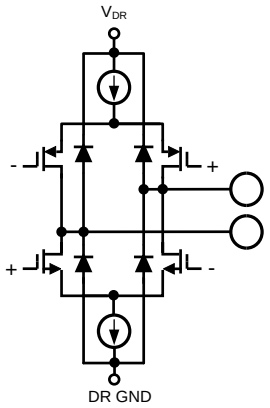
Ball No.	Name	Equivalent Circuit	Description
K19/K20 L19/L20	DCLKI+/- DCLKQ+/-		Data Clock Output for the I- and Q-channel data bus. These differential clock outputs are used to latch the output data and, if used, should always be terminated with a 100Ω differential resistor placed as closely as possible to the differential receiver. Delayed and non-delayed data outputs are supplied synchronously to this signal. In 1:2 Demux Mode or Non-Demux Mode, this signal is at ¼ or ½ the sampling clock rate, respectively. DCLKI and DCLKQ are always in phase with each other, unless one channel is powered down, and do not require a pulse from DCLK_RST to become synchronized.
K17/K18 L17/L18	ORI+/- ORQ+/-		Out-of-Range Output for the I- and Q-channel. This differential output is asserted logic-high while the over- or under-range condition exists, i.e. the differential signal at each respective analog input exceeds the full-scale value. Each OR result refers to the current Data, with which it is clocked out. If used, each of these outputs should always be terminated with a 100Ω differential resistor placed as closely as possible to the differential receiver.
J18/J19 H19/H20 H17/H18 G19/G20 G17/G18 F18/F19 E19/E20 D19/D20 D18/E18 C19/C20 B19/B20 B18/C17 . M18/M19 N19/N20 N17/N18 P19/P20 P17/P18 R18/R19 T19/T20 U19/U20 U18/T18 V19/V20 W19/W20 W18/V17	DI11+/- DI10+/- DI9+/- DI8+/- DI7+/- DI6+/- DI5+/- DI4+/- DI3+/- DI2+/- DI1+/- DI0+/- . DQ11+/- DQ10+/- DQ9+/- DQ8+/- DQ7+/- DQ6+/- DQ5+/- DQ4+/- DQ3+/- DQ2+/- DQ1+/- DQ0+/-		I- and Q-channel Digital Data Outputs. In Non-Demux Mode, this LVDS data is transmitted at the sampling clock rate. In Demux Mode, these outputs provide ½ the data at ½ the sampling clock rate, synchronized with the delayed data, i.e. the other ½ of the data which was sampled one clock cycle earlier. Compared with the DId and DQd outputs, these outputs represent the later time samples. If used, each of these outputs should always be terminated with a 100Ω differential resistor placed as closely as possible to the differential receiver.

Table 5. High-Speed Digital Output Pins (continued)

Ball No.	Name	Equivalent Circuit	Description
A18/A19 B17/C16 A16/B16 B15/C15 C14/D14 A14/B14 B13/C13 C12/D12 A12/B12 B11/C11 C10/D10 A10/B10 . Y18/Y19 W17/V16 Y16/W16 W15/V15 V14/U14 Y14/W14 W13/V13 V12/U12 Y12/W12 W11/V11 V10/U10 Y10/W10	DId11+/- DId10+/- DId9+/- DId8+/- DId7+/- DId6+/- DId5+/- DId4+/- DId3+/- DId2+/- DId1+/- DId0+/- . DQd11+/- DQd10+/- DQd9+/- DQd8+/- DQd7+/- DQd6+/- DQd5+/- DQd4+/- DQd3+/- DQd2+/- DQd1+/- DQd0+/-		Delayed I- and Q-channel Digital Data Outputs. In Non-Demux Mode, these outputs are tri-stated. In Demux Mode, these outputs provide ½ the data at ½ the sampling clock rate, synchronized with the non-delayed data, i.e. the other ½ of the data which was sampled one clock cycle later. Compared with the DI and DQ outputs, these outputs represent the earlier time samples. If used, each of these outputs should always be terminated with a 100Ω differential resistor placed as closely as possible to the differential receiver.

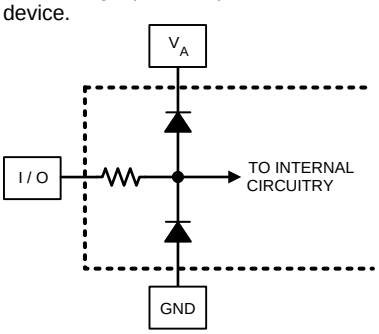
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

Supply Voltage (V_A, V_{TC}, V_{DR}, V_E)	2.2 V
Supply Difference max($V_{A/TC/DR/E}$) -min($V_{A/TC/DR/E}$)	0V to 100 mV
Voltage on Any Input Pin	−0.15 V to (V_A +0.15 V)
Voltage on V_{IN}^+, V_{IN}^-(Maintaining Common Mode)	−0.1 5V to 2.5 V
Ground Difference max($GND_{TC/DR/E}$) -min($GND_{TC/DR/E}$)	0 to 100 mV
Input Current at Any Pin (3)	±50 mA
Power Dissipation at $T_A \le 125°C$ (4)	2.4 W
ESD Susceptibility (5) Human Body Model	2500 V
Storage Temperature	−65°C to +150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. There is no specification of operation at the Absolute Maximum Ratings. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For specifications and test conditions, see the Electrical Characteristics. The specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

(2) The analog inputs are protected as shown below. Input voltage magnitudes beyond the Absolute Maximum Ratings may damage this device.



(3) When the input voltage at any pin exceeds the power supply limit; (i.e. less than GND or greater than V_A), the current at that pin should be limited to 50 mA. In addition, over voltage at a pin must adhere to maximum voltage limits. Simultaneously over voltage at multiple pins require adherence to the maximum package power dissipation limits.

(4) This dissipation limit is calculated using JEDEC JESD51-7 thermal model. Higher dissipation may be possible based on specific application thermal situation and specified thermal resistances.

(5) Human body model is 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is 220 pF discharged through ZERO Ohms.

Operating Ratings (1)(2)

Case Temperature Range	$-55°C \le T_C \le +125°C$
Supply Voltage (V_A, V_{TC}, V_E)	+1.8 V to +2.0 V
Driver Supply Voltage (V_{DR})	+1.8 V to V_A
V_{IN}+, V_{IN}- Voltage Range (3)	-0.4 V to +2.4 V
V_{IN}+, V_{IN}- Current Range (a.c.-coupled)(3)	±50 mA
V_{IN}+, V_{IN}- Power Maintaining common mode voltage (a.c.-coupled) Not maintaining common mode voltage (a.c.-coupled)	 15.3 dBm 17.1 dBm
CLK Pins Voltage Range	0V to V_A
Differential CLK Amplitude	$0.4V_{P-P}$ to $2.0V_{P-P}$

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. There is no specification of operation at the Absolute Maximum Ratings. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For specifications and test conditions, see the Electrical Characteristics. The specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

(2) All voltages are measured with respect to GND = GND_{DR} = GND_E = GND_{TC} = 0V, unless otherwise specified.

(3) Proper common mode voltage must be maintained to ensure proper output code, especially during input overdrive.

Package Thermal Resistance(1)

Package	θ_{JA}	θ_{JB} To Board	θ_{JT} Top (Case)
376 CPGA	10.4°C / W	3.2°C / W	0.5°C / W

(1) **Solder process specifications in BOARD MOUNTING RECOMMENDATION**

Quality Conformance Inspection

MIL-STD-883, Method 5005 - Group A

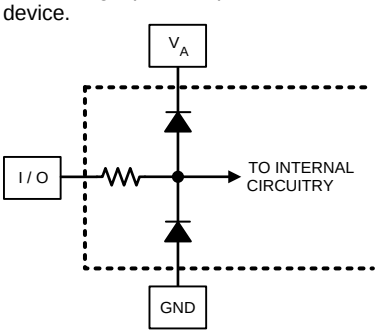
Subgroup	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55
12	Setting time at	+25
13	Setting time at	+125
14	Setting time at	-55

Converter Electrical Characteristics – Static Converter Characteristics

The following specifications apply after calibration for V_A = V_{DR} = V_{TC} = V_E = +1.9V; I- and Q-channels AC coupled, FSR Pin = High; C_L = 10 pF; Differential AC coupled Sine Wave Input Clock, f_{CLK} = 1.6 GHz at 0.5 V_{P-P} with 50% duty cycle; V_{BG} = Floating; Non-extended Control Mode; Rext = Rtrim = 3300 Ω ±0.1%; Analog Signal Source Impedance = 100 Ω Differential; 1:2 Demultiplex Non-DES Mode; I- and Q-channels; Duty Cycle Stabilizer on. (1)(2)(3)

Symbol	Parameter	Conditions	Notes	Typ	Min	Max	Units	Sub-groups
INL	Integral Non-Linearity (Best fit)	D.C. Coupled, 1 MHz Sine Wave Over-ranged		±2.5	-7.5	7.5	LSB	1, 2, 3
DNL	Differential Non-Linearity	D.C. Coupled, 1 MHz Sine Wave Over-ranged		±0.5	-1.35	1.35	LSB	1, 2, 3
	Resolution with No Missing Codes					12	bits	1, 2, 3
V_{OFF}	Offset Error			8			LSB	
V_{OFF_ADJ}	Input Offset Adjustment Range	Extended Control Mode		±45			mV	
PFSE	Positive Full-Scale Error		(4)		-30	30	mV	1, 2, 3
NFSE	Negative Full-Scale Error		(4)		-30	30	mV	1, 2, 3
	Out of Range Output Code	$(V_{IN}+) - (V_{IN}-)$ > + Full Scale				4095		1, 2, 3
		$(V_{IN}+) - (V_{IN}-)$ < − Full Scale			0			1, 2, 3

(1) The analog inputs are protected as shown below. Input voltage magnitudes beyond the Absolute Maximum Ratings may damage this device.



(2) To ensure accuracy, it is required that V_A, V_{TC}, V_E and V_{DR} be well-bypassed. Each supply pin must be decoupled with separate bypass capacitors.

(3) Typical figures are at T_A = 25°C, and represent most likely parametric norms.

(4) Calculation of Full-Scale Error for this device assumes that the actual reference voltage is exactly its nominal value. Full-Scale Error for this device, therefore, is a combination of Full-Scale Error and Reference Voltage Error. See Transfer Characteristic for relationship between Gain Error and Full-Scale Error, see Specification Definitions for Gain Error.

Converter Electrical Characteristics – Dynamic Converter Characteristics

Symbol	Parameter	Conditions	Notes	Typ	Min	Max	Units	Sub-groups
C.E.R.	Code Error Rate			10^{-18}			Error/Sample	
IMD_3	3rd order Intermodulation Distortion	f_{IN} = 2070 MHz ± 2.5 MHz @ -13 dBFS		-76			dBFS	
				-63			dBc	
		f_{IN} = 2070 MHz ± 2.5 MHz @ -16 dBFS		-80			dBFS	
				-64			dBc	
		f_{IN} = 2670 MHz ± 2.5 MHz @ -13 dBFS		-72			dBFS	
				-59			dBc	
		f_{IN} = 2670 MHz ± 2.5 MHz @ -16 dBFS		-77			dBFS	
				-61			dBc	
1:2 Demux, Non-DES Mode, Non-ECM, Non-LSPSM, f_{CLK} = 1.6 GHz, f_{IN} = 248 MHz, V_{IN} = -0.5 dBFS								
ENOB	Effective Number of Bits	T_A = 25°C to T_{Max}		8.9	8.5		bits	4, 5
		$T_A = T_{MIN}$			8.1		bits	6
SINAD	Signal-to-Noise Plus Distortion Ratio	T_A = 25°C to T_{Max}		55.4	53.0		dBFS	4, 5
		$T_A = T_{MIN}$			50.6		dBFS	6
SNR	Signal-to-Noise Ratio	T_A = 25°C to T_{Max}		56.6	54.6		dBFS	4, 5
		$T_A = T_{MIN}$			52.5		dBFS	6
THD	Total Harmonic Distortion	T_A = 25°C to T_{Max}		-61.6		-58.6	dBFS	4, 5
		$T_A = T_{MIN}$				-55.1	dBFS	6
2nd Harm	Second Harmonic Distortion			-68.5			dBFS	
3rd Harm	Third Harmonic Distortion			-61.5			dBFS	
SFDR	Spurious Free Dynamic Range	T_A = 25°C to T_{Max}		61.5	58.0		dBFS	4, 5
		$T_A = T_{MIN}$			55.0		dBFS	6
1:2 Demux, Non-DES Mode, Non-ECM, LSPSM, f_{CLK} = 800 MHz, f_{IN} = 248 MHz, V_{IN} = -0.5 dBFS								
ENOB	Effective Number of Bits	T_A = 25°C to T_{Max}		9.3	8.9		bits	4, 5
		$T_A = T_{MIN}$			8.5		bits	6
SINAD	Signal-to-Noise Plus Distortion Ratio	T_A = 25°C to T_{Max}		57.2	55.4		dBFS	4, 5
		$T_A = T_{MIN}$			53.0		dBFS	6
SNR	Signal-to-Noise Ratio	T_A = 25°C to T_{Max}		58.2	56.4		dBFS	4, 5
		$T_A = T_{MIN}$			55.8		dBFS	6
THD	Total Harmonic Distortion	T_A = 25°C to T_{Max}		-65.9		-62.3	dBFS	4, 5
		$T_A = T_{MIN}$				-57.0	dBFS	6
2nd Harm	Second Harmonic Distortion			-73.2			dBFS	
3rd Harm	Third Harmonic Distortion			-67.5			dBFS	
SFDR	Spurious Free Dynamic Range	T_A = 25°C to T_{Max}		67.3	62.5		dBFS	4, 5
		$T_A = T_{MIN}$			57.5		dBFS	6

Converter Electrical Characteristics – Dynamic Converter Characteristics (continued)

Symbol	Parameter	Conditions	Notes	Typ	Min	Max	Units	Sub-groups
Non-Demux(1), Non-DES Mode, ECM, Non-LSPSM, f_{CLK} = 1.6 GHz, f_{IN} = 248 MHz, V_{IN} = -0.5 dBFS								
ENOB	Effective Number of Bits			9.0			bits	
SINAD	Signal-to-Noise Plus Distortion Ratio			55.9			dBFS	
SNR	Signal-to-Noise Ratio			57.2			dBFS	
THD	Total Harmonic Distortion			-63.2			dBFS	
2nd Harm	Second Harmonic Distortion			-68.5			dBFS	
3rd Harm	Third Harmonic Distortion			-63.3			dBFS	
SFDR	Spurious-Free Dynamic Range			63.3			dBFS	
1:4 Demux, DES Mode, Non-LSPSM, f_{CLK} = 1.6 GHz, f_{IN} = 248 MHz, V_{IN} = -0.5 dBFS								
ENOB	Effective Number of Bits			8.8			bits	
SINAD	Signal-to-Noise Plus Distortion Ratio			54.8			dB	
SNR	Signal-to-Noise Ratio			56.0			dBFS	
THD	Total Harmonic Distortion			-61.8			dBFS	
2nd Harm	Second Harmonic Distortion			-71.1			dBFS	
3rd Harm	Third Harmonic Distortion			-61.8			dBFS	
SFDR	Spurious-Free Dynamic Range			61.7			dBFS	

(1) The maximum clock frequency for Non-Demux Mode is 1 GHz.

Converter Electrical Characteristics – Analog Input/Output and Reference Characteristics

Symbol	Parameter	Conditions	Notes	Typ	Min	Max	Units	Sub-groups
V_{IN_FSR}	Analog Differential Input Full Scale Range	FSR Pin Y3 Low		630			mV_{P-P}	4, 5, 6
		FSR Pin Y3 High		820	750	890	mV_{P-P}	4, 5, 6
		Extended Control Mode						
		FM(14:0) = 0000**h**		600			mV_{P-P}	
		FM(14:0) = 4000**h** (default)		800			mV_{P-P}	
		FM(14:0) = 7FFF**h**		1000			mV_{P-P}	
C_{IN}	Analog Input Capacitance, Non-DES Mode	Differential	(1)	0.02			pF	
		Each input pin to ground		1.6			pF	
	Analog Input Capacitance, DES Mode	Differential	(1)	0.02			pF	
		Each input pin to ground		2.2			pF	
R_{IN}	Differential Input Resistance			103	99	107	Ω	1, 2, 3
V_{BG}	Bandgap Reference Output Voltage	I_{BG} = ±100 µA		1.27	1.15	1.35	V	1, 2, 3
TC_V_{BG}	Bandgap Reference Voltage Temperature Coefficient	I_{BG} = ±100µA		50			ppm/°C	
C_{LOAD} V_{BG}	Maximum Bandgap Reference Load Capacitance			80			pF	

(1) The analog and clock input capacitances are die capacitances only. Additional package capacitances of 0.22 pF differential and 1.06 pF each pin to ground are isolated from the die capacitances by lead and bond wire inductances.

Converter Electrical Characteristics – Channel-to-Channel Characteristics

Symbol	Parameter	Conditions	Notes	Typ	Min	Max	Units	Sub-groups
	Phase Matching (I, Q)	f_{IN} = 1.0 GHz		<1			Degree	
X-TALK Q-channel	Crosstalk from I-channel (Aggressor) to Q-channel (Victim)	Aggressor = 248 MHz		-72			dBFS	
		Aggressor = 498 MHz		-65			dBFS	
X-TALK I-channel	Crosstalk from Q-channel (Aggressor) to I-channel (Victim)	Aggressor = 248 MHz		-74			dBFS	
		Aggressor = 498 MHz		-63			dBFS	

Converter Electrical Characteristics – LVDS CLK Input Characteristics

Symbol	Parameter	Conditions	Notes	Typ	Min	Max	Units	Sub-groups
V_{IN_CLK}	Differential Clock Input Level	Sine Wave Clock	(1)		0.4	2.0	V_{P-P}	1, 2, 3
		Square Wave Clock			.04	2.0	V_{P-P}	1, 2, 3
C_{IN_CLK}	Sampling Clock Input Capacitance	Differential	(2)	0.1			pF	
		Each input to ground		1			pF	
R_{IN_CLK}	Sampling Clock Input Resistance			100			Ω	

(1) This parameter is specified by design and/or characterization and is not tested in production.
(2) The analog and clock input capacitances are die capacitances only. Additional package capacitances of 0.22 pF differential and 1.06 pF each pin to ground are isolated from the die capacitances by lead and bond wire inductances.

Converter Electrical Characteristics – Digital Control and Output Pin Characteristics

Symbol	Parameter	Conditions	Notes	Typ	Min	Max	Units	Sub-groups
Digital Control Pins, (DES, LSPSM, CAL, PDI, PDQ, TPM, NDM, FSR, DDRPh, $\overline{ECE}$, SCLK, SDI, $\overline{SCS}$)								
V_{IH}	Logic High Input Voltage	DES, LSPSM, CAL, PDI, PDQ, TPM, NDM, FSR, DDRPh, $\overline{ECE}$, SCLK, SDI, $\overline{SCS}$			0.7 x V_A		V	1, 2, 3
V_{IL}	Logic Low Input Voltage	DES, LSPSM, CAL, PDI, PDQ, TPM, NDM, FSR, DDRPh, $\overline{ECE}$, SCLK, SDI, $\overline{SCS}$				0.3 x V_A	V	1, 2, 3
I_{IH}	Input Current High $V_{IN} = V_A$	DES, LSPSM, CAL, PDI, PDQ, TPM, NDM, FSR, DDRPh, $\overline{ECE}$, SCLK, SDI, $\overline{SCS}$			-1	1	µA	1, 2, 3
I_{IL}	Ipnut Current Low V_{IN} = GND	DES, LSPSM, CAL, TPM, NDM, FSR, DDRPh,			-1	1	µA	1, 2, 3
		SCLK, SDI, $\overline{SCS}$			-30		µA	1, 2, 3
		PDI, PDQ, $\overline{ECE}$,			-55		µA	1, 2, 3
C_{IN_DIG}	Input Capacitance	Each input to ground	(1)	1.5			pF	
Digital Output Pins (Data, DCLKI, DCLKQ, ORI, ORQ) - See Figure 2 in Specification Definitions								
V_{OD}	LVDS Differential Output Voltage	V_{BG} = Floating, OVS = V_A		600	380	840	mV_{P-P}	1, 2, 3
		V_{BG} = Floating, OVS = GND		440	240	650	mV_{P-P}	1, 2, 3
		V_{BG} = V_A, OVS = V_A		670			mV_{P-P}	1, 2, 3
		V_{BG} = V_A, OVS = GND		500			mV_{P-P}	1, 2, 3
$\Delta V_{O\ DIFF}$	Change in LVDS Output Swing Between Logic Levels			1	-20	20	mV	
V_{OS}	Output Offset Voltage	V_{BG} = Floating		0.8			V	
		V_{BG} = V_A		1.2			V	
ΔV_{OS}	Output Offset Voltage Change Between Logic Levels			±1			mV	
I_{OS}	Output Short Circuit Current	V_{BG} = Floating; D+ and D− connected to 0.8V		±3.8			mA	
Z_O	Differential Output Impedance			100			Ω	
V_{OH}	Logic High Output Level	CalRun, SDO I_{OH} = −400 µA		1.7	1.5		V	1, 2, 3
V_{OL}	Logic Low Output Level	CalRun, SDO I_{OH} = 400 µA		0.14	0.3		V	1, 2, 3
Differential DCLK Reset Pins (DCLK_RST)								
V_{CMI_DRST}	DCLK_RST Common Mode Input Voltage			1.25			V	
V_{ID_DRST}	Differential DCLK_RST Input Voltage			0.6			VP-P	
R_{IN_DRST}	Differential DCLK_RST Input Resistance			100			Ω	

(1) The digital control pin capacitances are die capacitances only. Additional package capacitance of 1.6 pF each pin to ground are isolated from the die capacitances by lead and bond wire inductances.

Converter Electrical Characteristics – Power Supply Characteristics

Symbol	Parameter	Conditions	Notes	Typ	Min	Max	Units	Sub-groups
f_{CLK} = 1.6 GHz,1:2 Demux Mode, Non-LSPSM								
I_A	Analog Supply Current	PDI = PDQ = Low		1160		1290	mA	1, 2, 3
		PDI = Low; PDQ = High		637			mA	
		PDI = High; PDQ = Low		635			mA	
		PDI = PDQ = High		2			mA	
I_{TC}	Track-and-Hold and Clock Supply Current	PDI = PDQ = Low		471		520	mA	1, 2, 3
		PDI = Low; PDQ = High		284			mA	
		PDI = High; PDQ = Low		284			mA	
		PDI = PDQ = High		1			mA	
I_{DR}	Output Driver Supply Current	PDI = PDQ = Low		281		380	mA	1, 2, 3
		PDI = Low; PDQ = High		149			mA	
		PDI = High; PDQ = Low		143			mA	
		PDI = PDQ = High		8			µA	
I_E	Digital Encoder Supply Current	PDI = PDQ = Low		90		163	mA	1, 2, 3
		PDI = Low; PDQ = High		54			mA	
		PDI = High; PDQ = Low		42			mA	
		PDI = PDQ = High		0.04			µA	
I_T	Total Current	PDI = PDQ = Low		90		2280	mA	1, 2, 3
		PDI = Low; PDQ = High		54		1300	mA	1, 2, 3
		PDI = High; PDQ = Low		42		1300	mA	1, 2, 3
		PDI = PDQ = High		0.04			µA	
P_C	Power Consumption	PDI = PDQ = Low		3.8		4.4	W	1, 2, 3
		PDI = Low; PDQ = High		2.1			W	
		PDI = High; PDQ = Low		2.1			W	
		PDI = PDQ = High		5.2			mW	
f_{CLK} = 800 MHz,1:2 Demux Mode, LSPSM								
I_A	Analog Supply Current	PDI = PDQ = Low		754		860	mA	1, 2, 3
		PDI = Low; PDQ = High		423			mA	
		PDI = High; PDQ = Low		423			mA	
		PDI = PDQ = High		2			mA	
I_{TC}	Track-and-Hold and Clock Supply Current	PDI = PDQ = Low		344		380	mA	1, 2, 3
		PDI = Low; PDQ = High		212			mA	
		PDI = High; PDQ = Low		212			mA	
		PDI = PDQ = High		1			mA	
I_{DR}	Output Driver Supply Current	PDI = PDQ = Low		273		350	mA	1, 2, 3
		PDI = Low; PDQ = High		141			mA	
		PDI = High; PDQ = Low		141			mA	
		PDI = PDQ = High		8			µA	
I_E	Digital Encoder Supply Current	PDI = PDQ = Low		46		79	mA	1, 2, 3
		PDI = Low; PDQ = High		24			mA	
		PDI = High; PDQ = Low		22			mA	
		PDI = PDQ = High		0.03			µA	
I_T	Total Current	PDI = PDQ = Low		1417		1620	mA	1, 2, 3
		PDI = Low; PDQ = High		801		940	mA	1, 2, 3
		PDI = High; PDQ = Low		799		940	mA	1, 2, 3
		PDI = PDQ = High		2.7			µA	

Converter Electrical Characteristics – Power Supply Characteristics (continued)

Symbol	Parameter	Conditions	Notes	Typ	Min	Max	Units	Sub-groups
f_{CLK} = 1.6 GHz,1:2 Demux Mode, Non-LSPSM								
P_C	Power Consumption	PDI = PDQ = Low		2.7		3.1	W	1, 2, 3
		PDI = Low; PDQ = High		1.5			W	
		PDI = High; PDQ = Low		1.5			W	
		PDI = PDQ = High		5.2			mW	

Converter Electrical Characteristics – AC Electrical Characteristics

Symbol	Parameter	Conditions	Notes	Typ	Min	Max	Units	Sub-groups
Input Clock (CLK)								
$f_{CLK\ (max)}$	Maximum Input Clock Frequency	Non-LSPSM		1.7	1.6		GHz	9, 10, 11
		Non-LSPSM		1000	800		MHz	
$f_{CLK\ (min)}$	Minimum Input Clock Frequency	Non-DES Mode				200	MHz	9, 10, 11
		DES Mode				250	MHz	9, 10, 11
	Input Clock Duty Cycle	$f_{CLK(min)} \le f_{CLK} \le f_{CLK}$ (max)	(1)	50	20	80	%	
t_{CL}	Input Clock Low Time		(1)	500	200		ps (min)	
t_{CH}	Input Clock High Time		(1)	500	200		ps (min)	
	DCLK Duty Cycle			50			% (min)	
							% (max)	
Data Clock (DCLKI, DCLKQ)								
t_{SR}	Setup Time DCLK_RST±			45			ps	
t_{HR}	Hold Time DCLK_RST±			45			ps	
t_{PWR}	Pulse Width DCLK_RST±			5			Input Clock Cycles (min)	
t_{SYNC_DLY}	DCLK Synchronization Delay	90° Mode		4			Input Clock Cycles	
		0° Mode		5				
t_{LHT}	Differential Low-to-High Transition Time	10% to 90%, C_L = 2.5 pF		200			ps	
t_{HLT}	Differential High-to-Low Transition Time	10% to 90%, C_L = 2.5 pF		200			ps	
t_{SU}	Data-to-DCLK Set-Up Time	DDR Mode, 90° DCLK		500			ps	
t_H	DCLK-to-Data Hold Time	DDR Mode, 90° DCLK		500			ps	
t_{OSK}	DCLK-to-Data Output Skew	50% of DCLK Transition to 50% of Data Transition		±50			ps	

(1) This parameter is specified by design and/or characterization and is not tested in production.

Converter Electrical Characteristics – AC Electrical Characteristics (continued)

Symbol	Parameter	Conditions	Notes	Typ	Min	Max	Units	Sub-groups
Data Input to Output								
t_{AD}	Sampling (Aperture) Delay	Input CLK+ Fall to Acquisition of Data		1.3			ns	
t_{AJ}	Aperture Jitter			0.2			ps (rms)	
t_{OD}	Input Clock-to Data Output Delay (in addition to t_{LAT})	50% of Input Clock transition to 50% of Data transition		3.2			ns	
t_{LAT}	Latency in 1:2 Demux Non-DES Mode	DI, DQ Outputs	(2)			34	Input Clock Cycles	4, 5, 6
		DId, DQd Outputs				35		4, 5, 6
	Latency in 1:4 Demux DES Mode	DI Outputs	(2)			34	Input Clock Cycles	4, 5, 6
		DQ Outputs				34.5		4, 5, 6
		DId Outputs				35		4, 5, 6
		DQd Outputs				35.5		4, 5, 6
	Latency in Non-Demux(3) Non-DES Mode	DI Outputs	(2)			34	Input Clock Cycles	4, 5, 6
		DQ Outputs				34		4, 5, 6
	Latency in Non-Demux(3) DES Mode	DI Outputs	(2)			34	Input Clock Cycles	4, 5, 6
		DQ Outputs				34.5		4, 5, 6
t_{ORR}	Over Range Recovery Time	Differential V_{IN} step from ±1.2V to 0V to get accurate conversion		1			Input Clock Cycle	
t_{WU}	PD Low to Rated Accuracy Conversion (Wake-Up Time)	Non-DES Mode		500			ns	
		DES Mode		1			µs	
Serial Port Interface								
f_{SCLK}	Serial Clock Frequency			15			MHz	
	Serial Clock Low Time				30		ns	9, 10, 11
	Serial Clock High Time				30		ns	9, 10, 11
t_{SSU}	Serial Data to Serial Clock Rising Setup Time						ns (min)	
t_{SH}	Serial Data to Serial Clock Rising Hold Time			2.5			ns (min)	
t_{SCS}	$\overline{SCS}$ to Serial Clock Rising Setup Time			1			ns	
t_{HCS}	$\overline{SCS}$ to Serial Clock Falling Hold Time			2.5			ns	
t_{BSU}	Bus Turn-around Time			10			ns	
Calibration								
t_{CAL}	Calibration Cycle Time	Non-ECM		$4.1x10^7$			Clock Cycles	
		ECM CSS = 0b						
		ECM; CSS = 1b						
t_{CAL_L}	CAL Pin Low Time	See Figure 11	(2)		1280		Clock Cycles	9, 10, 11
t_{CAL_H}	CAL Pin High Time				1280		Clock Cycles	9, 10, 11

(2) This parameter is specified by design and/or characterization and is not tested in production.
(3) The maximum clock frequency for Non-Demux Mode is 1 GHz.

Specification Definitions

APERTURE (SAMPLING) DELAY is the amount of delay, measured from the sampling edge of the CLK input, after which the signal present at the input pin is sampled inside the device.

APERTURE JITTER (t_{AJ}) is the variation in aperture delay from sample-to-sample. Aperture jitter can be effectively considered as noise at the input.

CODE ERROR RATE (CER) is the probability of error and is defined as the probable number of word errors on the ADC output per unit of time divided by the number of words seen in that amount of time. A CER of 10^{-18} corresponds to a statistical error in one word about every 31.7 years for the ADC12D1600QML .

CLOCK DUTY CYCLE is the ratio of the time that the clock waveform is at a logic high to the total time of one clock period.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB. It is measured at the relevant sample rate, f_{CLK}, with f_{IN} = 1MHz sine wave.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion Ratio, or SINAD. ENOB is defined as (SINAD − 1.76) / 6.02 and states that the converter is equivalent to a perfect ADC of this many (ENOB) number of bits.

GAIN ERROR is the deviation from the ideal slope of the transfer function. It can be calculated from Offset and Full-Scale Errors. The Positive Gain Error is the Offset Error minus the Positive Full-Scale Error. The Negative Gain Error is the Negative Full-Scale Error minus the Offset Error. The Gain Error is the Negative Full-Scale Error minus the Positive Full-Scale Error; it is also equal to the Positive Gain Error plus the Negative Gain Error.

GAIN FLATNESS is the measure of the variation in gain over the specified bandwidth. For example, for the ADC12D1600QML , from D.C. to Fs/2 is to 800 MHz for the Non- DES Mode and from D.C. to Fs/2 is 1600 MHz for the DES Mode.

INTEGRAL NON-LINEARITY (INL) is a measure of worst case deviation of the ADC transfer function from an ideal straight line drawn through the ADC transfer function. The deviation of any given code from this straight line is measured from the center of that code value step. The best fit method is used.

INSERTION LOSS is the loss in power of a signal due to the insertion of a device, e.g. the ADC12D1600, expressed in dB.

INTERMODULATION DISTORTION (IMD) is a measure of the near-in 3rd order distortion products ($2f_2 - f_1$, $2f_1 - f_2$) which occur when two tones which are close in frequency (f_1, f_2) are applied to the ADC input. It is measured from the input tone's level to the higher of the two distortion products (dBc) or simply the level of the higher of the two distortion products (dBFS).

LSB (LEAST SIGNIFICANT BIT) is the bit that has the smallest value or weight of all bits. This value is

$$V_{FS} / 2^N \quad (1)$$

where

- V_{FS} is the differential full-scale amplitude V_{IN_FSR} as set by the FSR input
- "N" is the ADC resolution in bits, which is 12 for the ADC12D1600

LOW VOLTAGE DIFFERENTIAL SIGNALING (LVDS) DIFFERENTIAL OUTPUT VOLTAGE (V_{ID} and V_{OD}) is two times the absolute value of the difference between the V_D+ and V_D- signals; each signal measured with respect to Ground. V_{OD} peak is $V_{OD,P}$= (V_D+ - V_D-) and V_{OD} peak-to-peak is $V_{OD,P-P}$= 2*(V_D+ - V_D-); for this product, the V_{OD} is measured peak-to-peak.

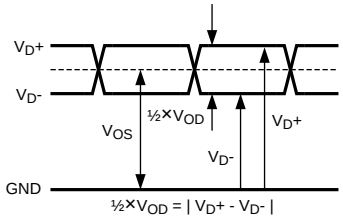


Figure 2. LVDS Output Signal Levels

LVDS OUTPUT OFFSET VOLTAGE (V_{OS}) is the midpoint between the D+ and D- pins output voltage with respect to ground; i.e., [(V_D+) +(V_D-)]/2. See Figure 2.

MISSING CODES are those output codes that are skipped and will never appear at the ADC outputs. These codes cannot be reached with any input value.

MSB (MOST SIGNIFICANT BIT) is the bit that has the largest value or weight. Its value is one half of full scale.

NEGATIVE FULL-SCALE ERROR (NFSE) is a measure of how far the first code transition is from the ideal 1/2 LSB above a differential $-V_{IN}/2$ with the FSR pin low. For the ADC12D1600 the reference voltage is assumed to be ideal, so this error is a combination of full-scale error and reference voltage error.

NOISE FLOOR DENSITY is a measure of the power density of the noise floor, expressed in dBFS/Hz and dBm/Hz. '0 dBFS' is defined as the power of a sinusoid which precisely uses the full-scale range of the ADC.

NOISE POWER RATIO (NPR) is the ratio of the sum of the power inside the notched bins to the sum of the power in an equal number of bins outside the notch, expressed in dB.

OFFSET ERROR (V_{OFF}) is a measure of how far the mid-scale point is from the ideal zero voltage differential input.

Offset Error = Actual Input causing average of 8k samples to result in an average code of 2047.5.

OUTPUT DELAY (t_{OD}) is the time delay (in addition to Latency) after the rising edge of CLK+ before the data update is present at the output pins.

OVER-RANGE RECOVERY TIME is the time required after the differential input voltages goes from ±1.2V to 0V for the converter to recover and make a conversion with its rated accuracy.

PIPELINE DELAY (LATENCY) is the number of input clock cycles between initiation of conversion and when that data is presented to the output driver stage. The data lags the conversion by the Latency plus the t_{OD}.

POSITIVE FULL-SCALE ERROR (PFSE) is a measure of how far the last code transition is from the ideal 1-1/2 LSB below a differential $+V_{IN}/2$. For the ADC12D1600 the reference voltage is assumed to be ideal, so this error is a combination of full-scale error and reference voltage error.

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the fundamental for a single-tone to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or DC.

SIGNAL TO NOISE PLUS DISTORTION (S/(N+D) or SINAD) is the ratio, expressed in dB, of the rms value of the fundamental for a single-tone to the rms value of all of the other spectral components below half the input clock frequency, including harmonics but excluding DC.

SPURIOUS-FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the rms values of the input signal at the output and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input, excluding DC.

θ_{JA} is the thermal resistance between the junction to ambient.

θ_{JB} is the thermal resistance between the junction and the circuit board close to the outer pins.

θ_{JT} is the thermal resistance between the junction and the case, measured at the lid of the package.

TOTAL HARMONIC DISTORTION (THD) is the ratio expressed in dB, of the rms total of the first nine harmonic levels at the output to the level of the fundamental at the output. THD is calculated as

$$THD = 20 \times \log \sqrt{\frac{A_{f2}^2 + \ldots + A_{f10}^2}{A_{f1}^2}}$$

where

- A_{f1} is the RMS power of the fundamental (output) frequency
- A_{f2} through A_{f10} are the RMS power of the first 9 harmonic frequencies in the output spectrum (2)

– Second Harmonic Distortion (2nd Harm) is the difference, expressed in dB, between the RMS power in the input frequency seen at the output and the power in its 2nd harmonic level at the output.

– Third Harmonic Distortion (3rd Harm) is the difference expressed in dB between the RMS power in the input frequency seen at the output and the power in its 3rd harmonic level at the output.

Transfer Characteristic

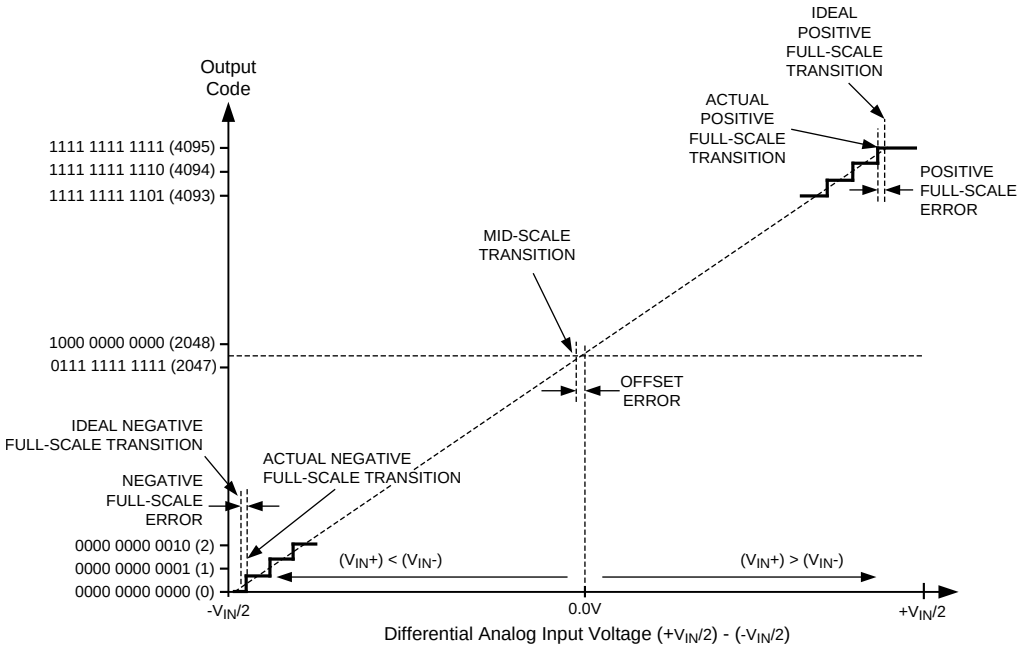


Figure 3. Input / Output Transfer Characteristic

Timing Diagrams

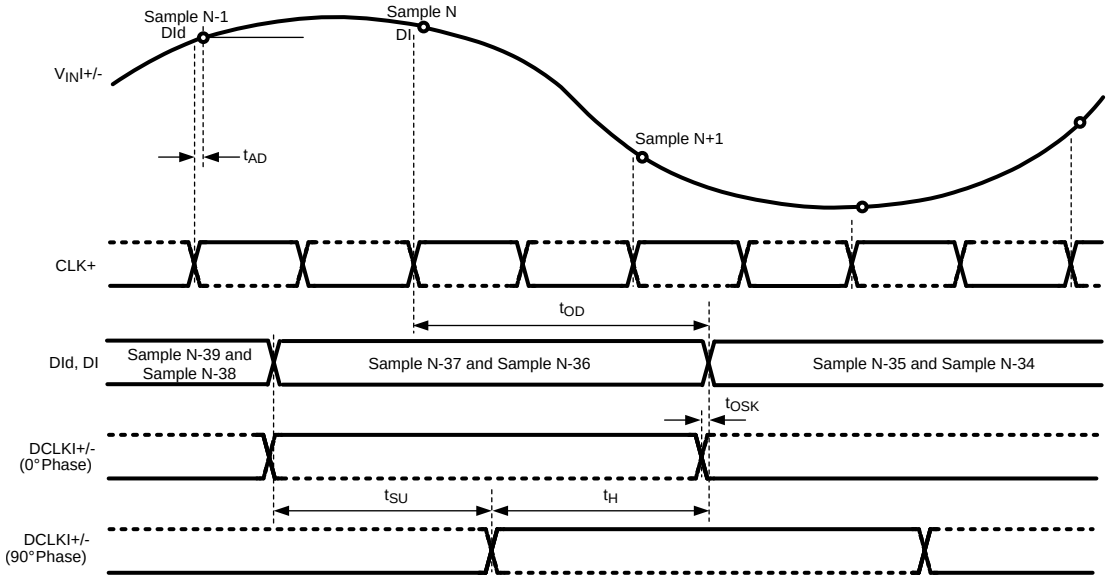


Figure 4. Clocking in Non-LSPSM, 1:2 Demux, Non-DES Mode*

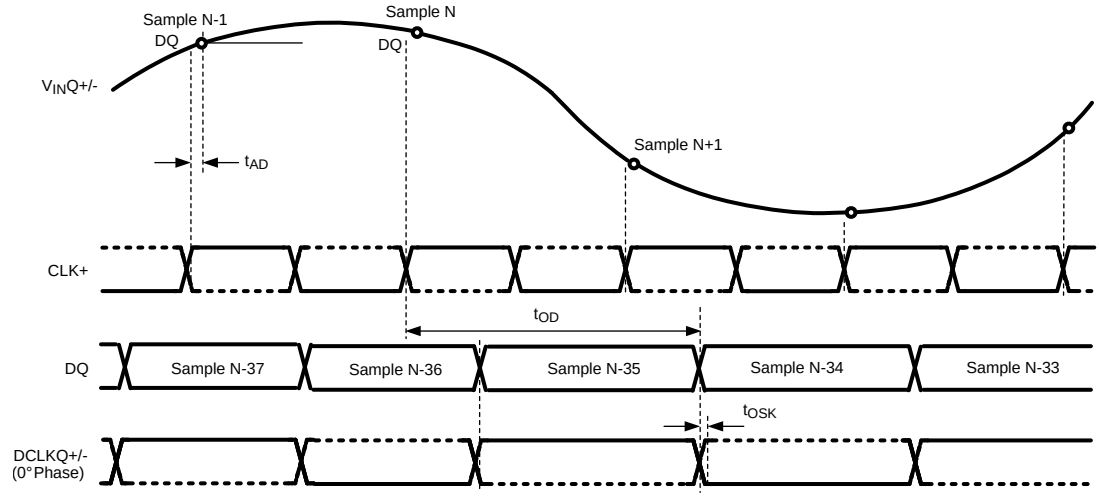


Figure 5. Clocking in Non-LSPSM, Non-Demux, Non-DES Mode*

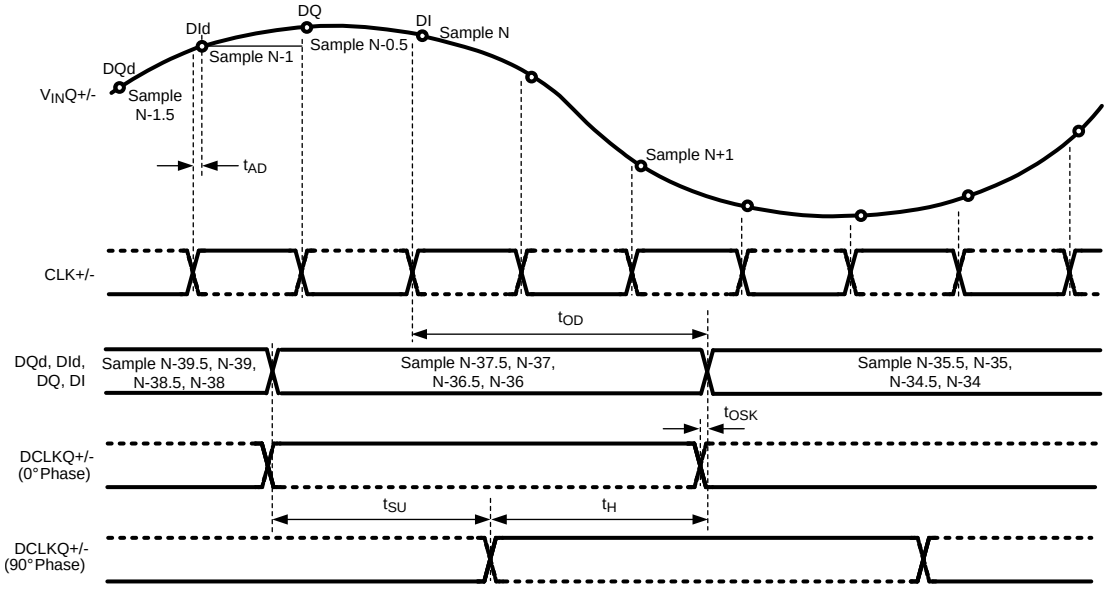


Figure 6. Clocking in Non-LSPSM, 1:4 Demux DES Mode*

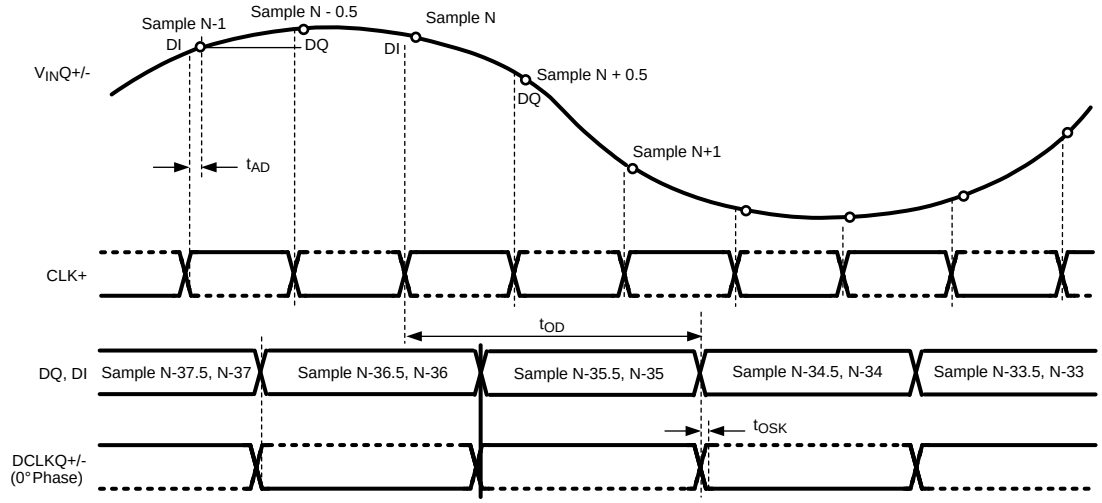


Figure 7. Clocking in Non-LSPSM, Non-Demux Mode DES Mode*

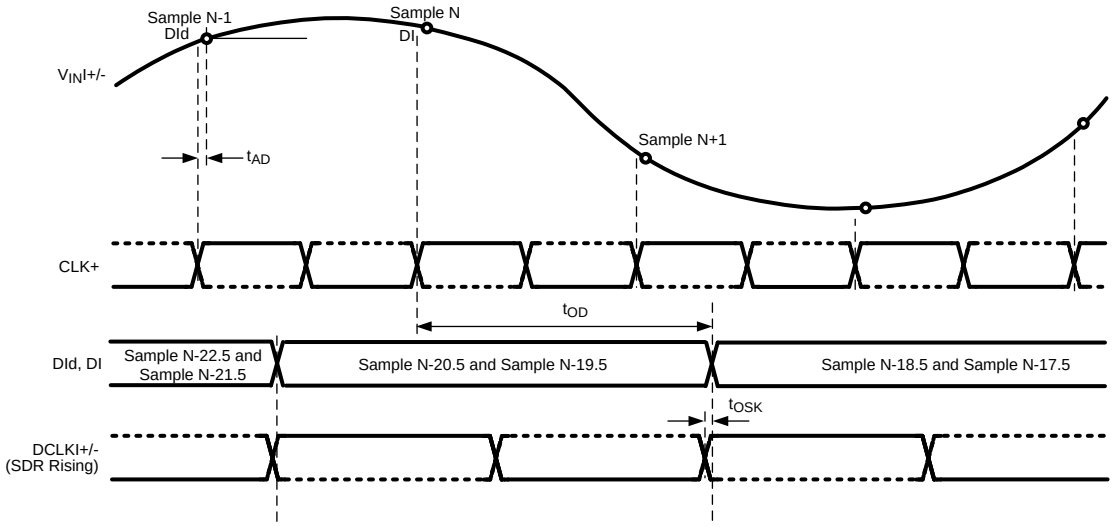


Figure 8. Clocking in LSPSM, 1:2 Demux Mode, Non-DES mode*

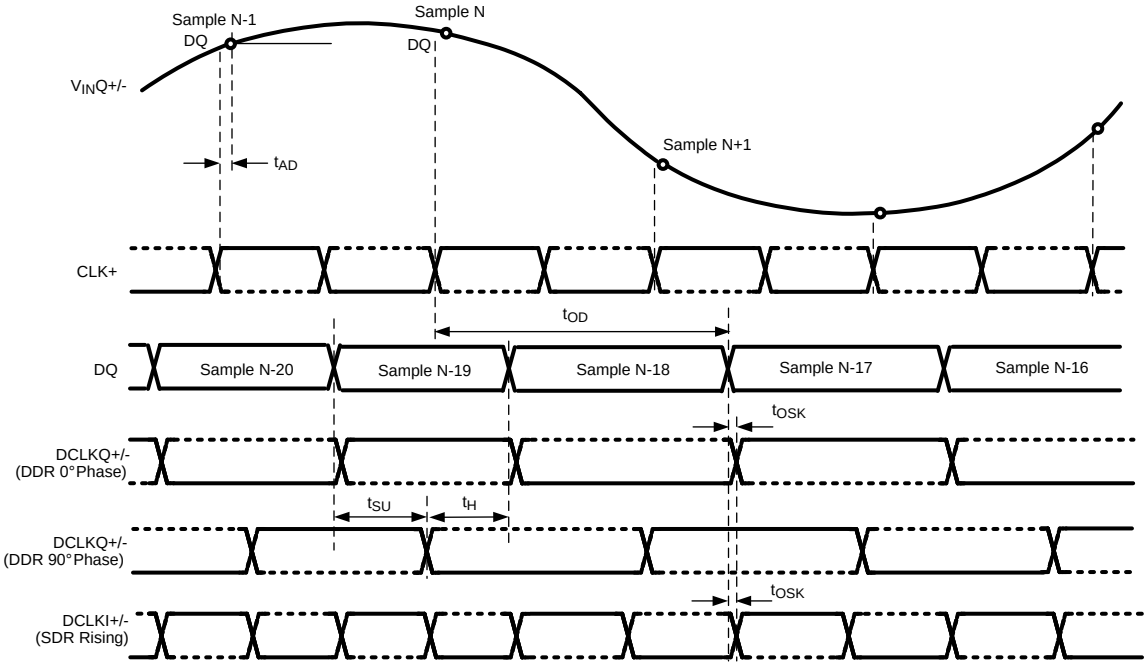


Figure 9. Clocking in LSPSM, Non-Demux Mode, Non-DES Mode*

NOTE

* The timing for Figure 4 through Figure 9 is shown for the one input only (I or Q). However, both I- and Q-inputs may be used. For this case, the I-channel functions precisely the same as the Q-channel, with VinI, DCLKI, DId and DI instead of VinQ, DCLKQ, DQd and DQ. Both I- and Q-channel use the same CLK.

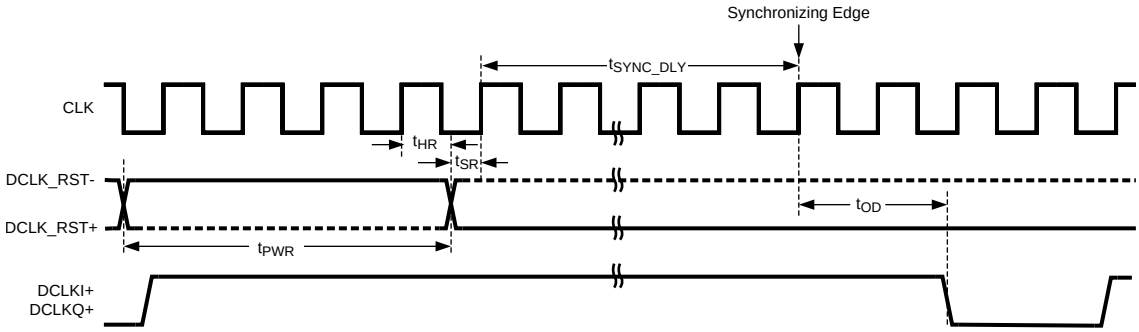


Figure 10. Data Clock Reset Timing (Demux Mode)

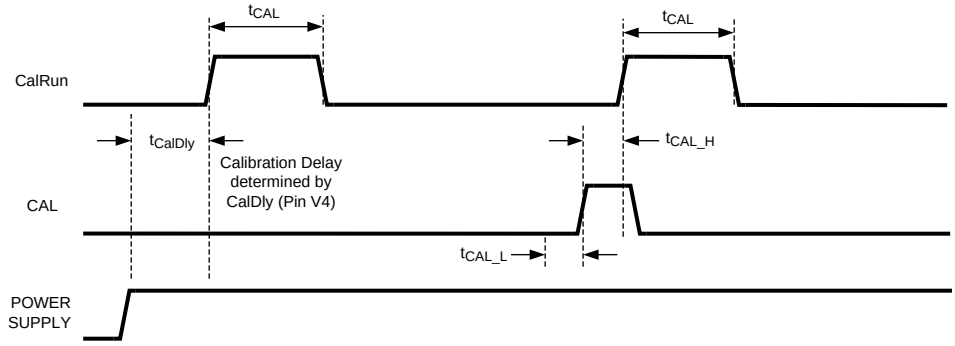


Figure 11. Power-on and On-Command Calibration Timing

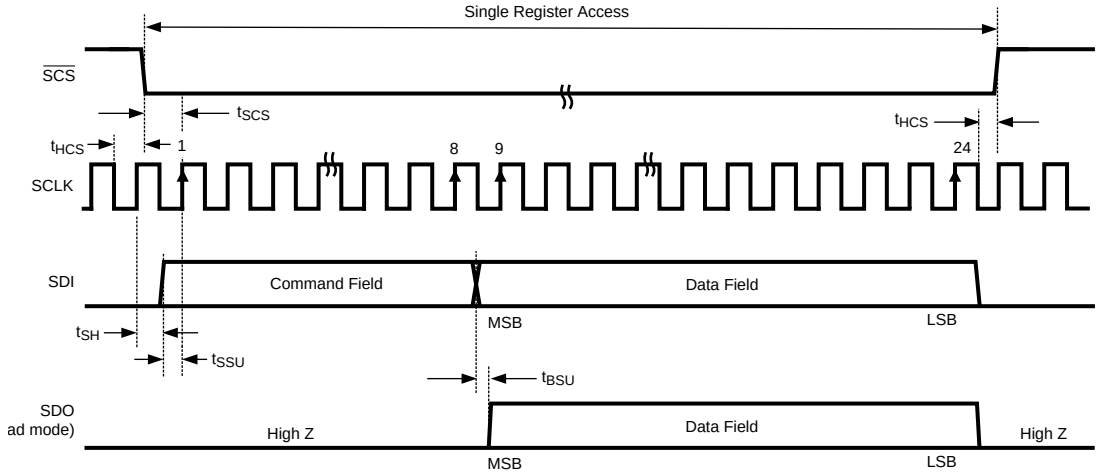


Figure 12. Serial Interface Timing

Typical Performance Plots

V_A = V_{DR} = V_{TC} = V_E = 1.9V, f_{CLK} = 1600 MHz in Non-LSPSM and 800 MHz in LSPSM, f_{IN} = 248 MHz, T_A= 25°C, 1:2 Demux Non-DES Mode, and calibration performed after temperature, supply voltage or sample rate change, unless otherwise stated.

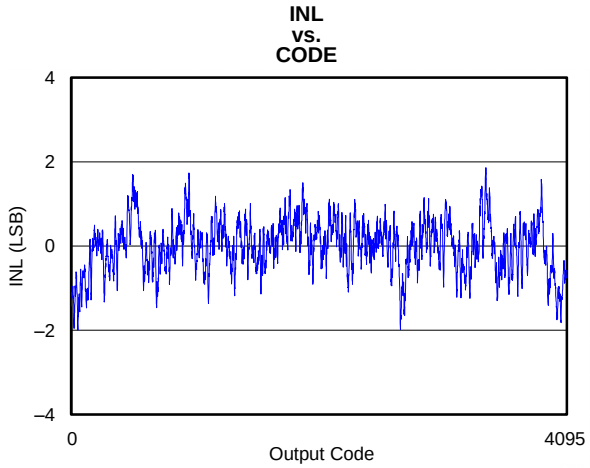


Figure 13.

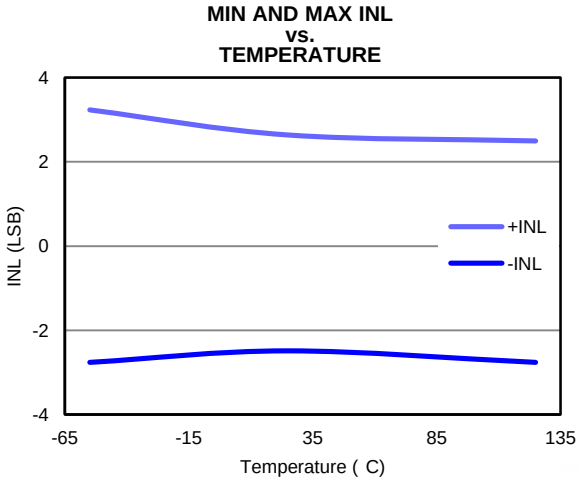


Figure 14.

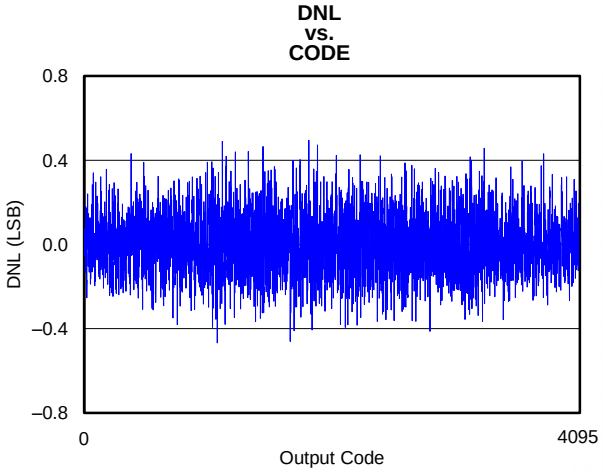


Figure 15.

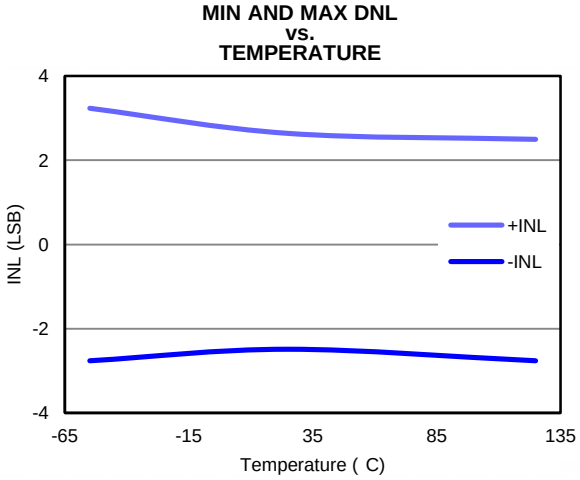


Figure 16.

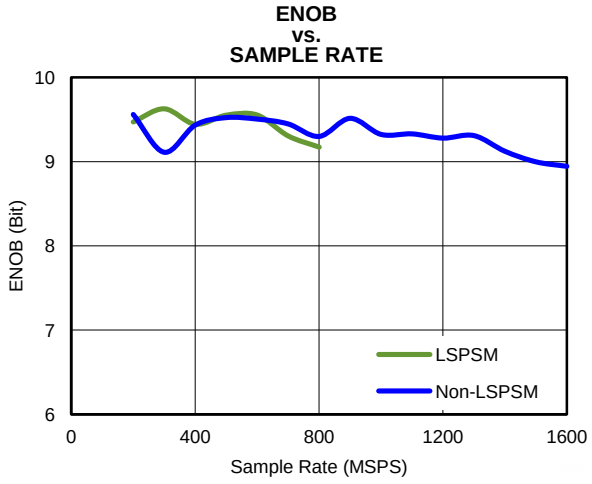


Figure 17.

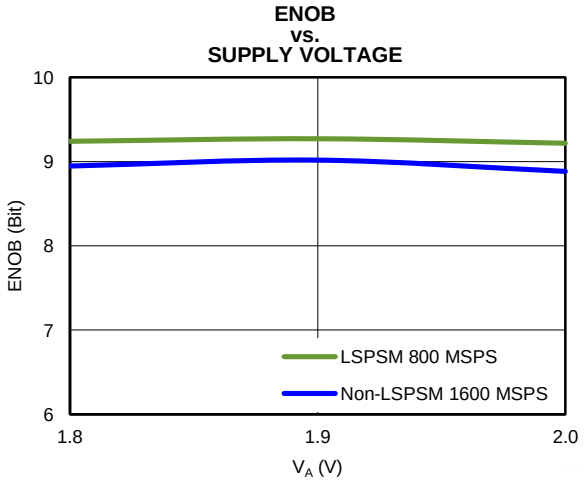


Figure 18.

Typical Performance Plots (continued)

V_A = V_{DR} = V_{TC} = V_E = 1.9V, f_{CLK} = 1600 MHz in Non-LSPSM and 800 MHz in LSPSM, f_{IN} = 248 MHz, T_A= 25°C, 1:2 Demux Non-DES Mode, and calibration performed after temperature, supply voltage or sample rate change, unless otherwise stated.

ENOB vs. TEMPERATURE

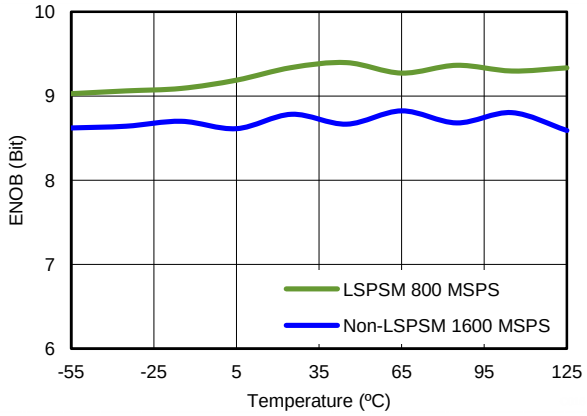


Figure 19.

ENOB vs. INPUT FREQUENCY

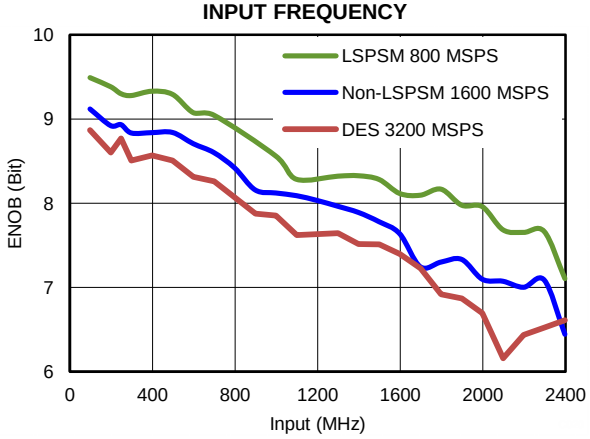


Figure 20.

SNR vs. SAMPLE RATE

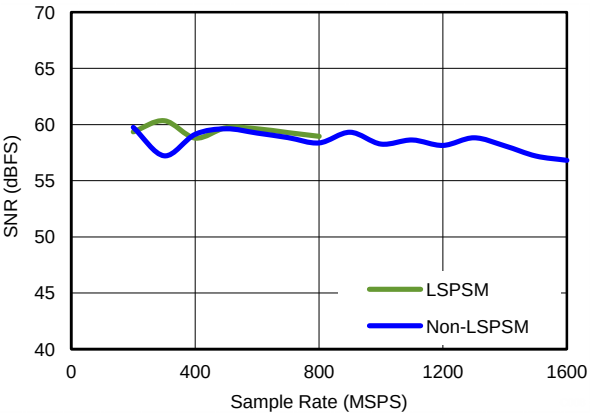


Figure 21.

SNR vs. SUPPLY VOLTAGE

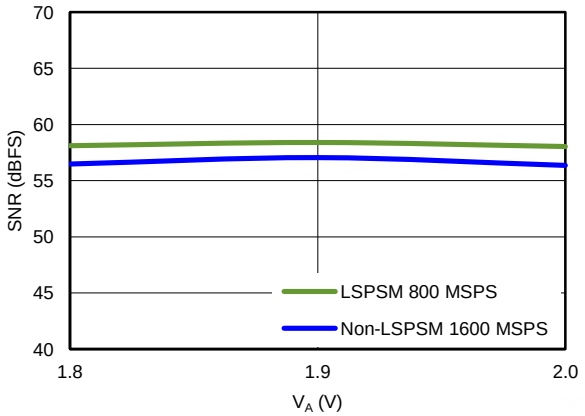


Figure 22.

SNR vs. TEMPERATURE

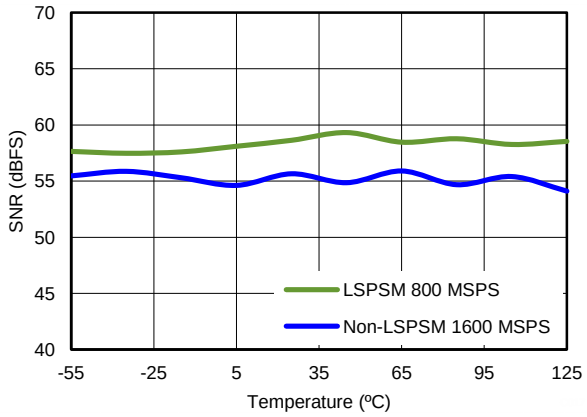


Figure 23.

SNR vs. INPUT FREQUENCY

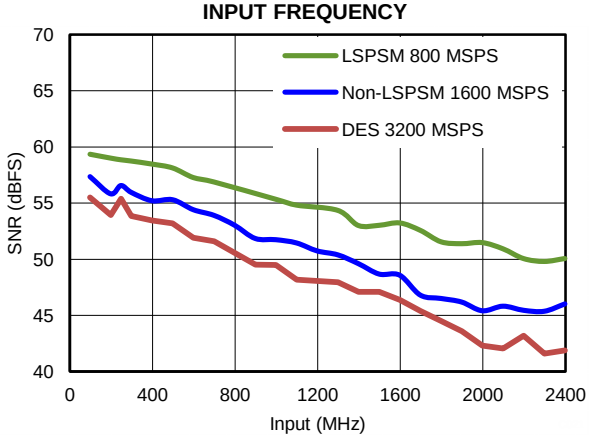


Figure 24.

Typical Performance Plots (continued)

$V_A = V_{DR} = V_{TC} = V_E = 1.9V$, f_{CLK} = 1600 MHz in Non-LSPSM and 800 MHz in LSPSM, f_{IN} = 248 MHz, T_A= 25°C, 1:2 Demux Non-DES Mode, and calibration performed after temperature, supply voltage or sample rate change, unless otherwise stated.

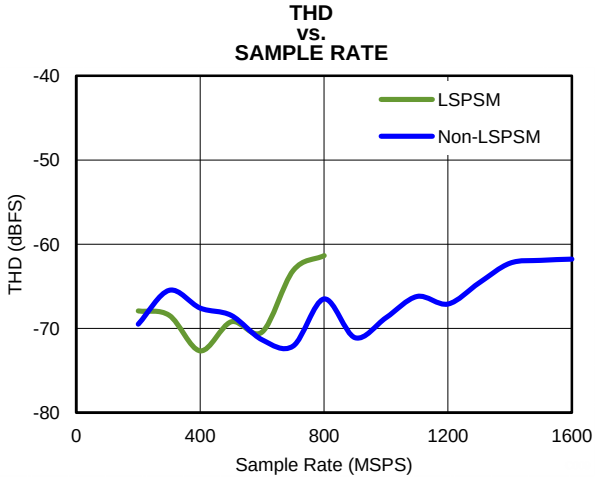


Figure 25.

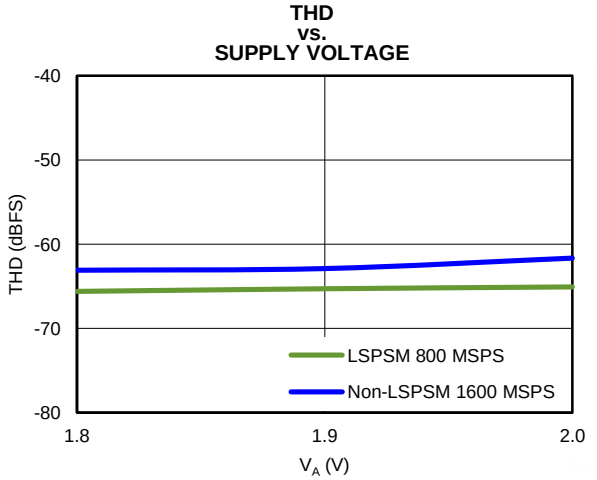


Figure 26.

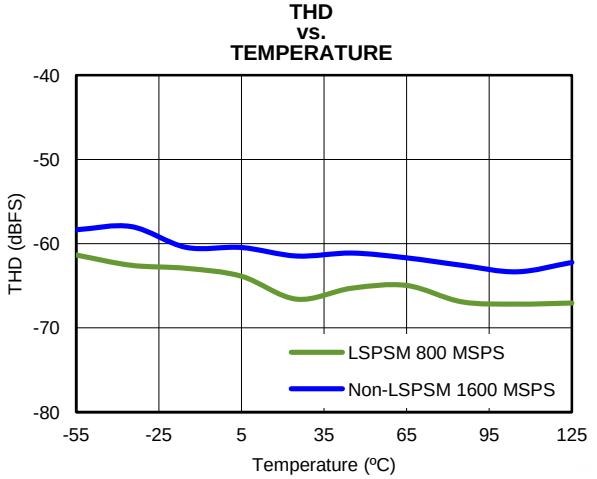


Figure 27.

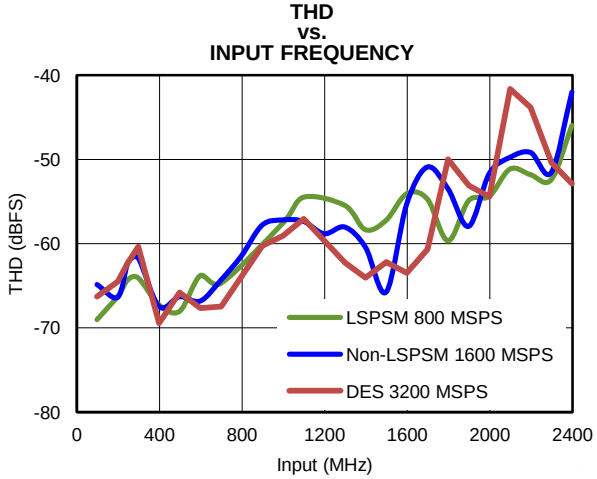


Figure 28.

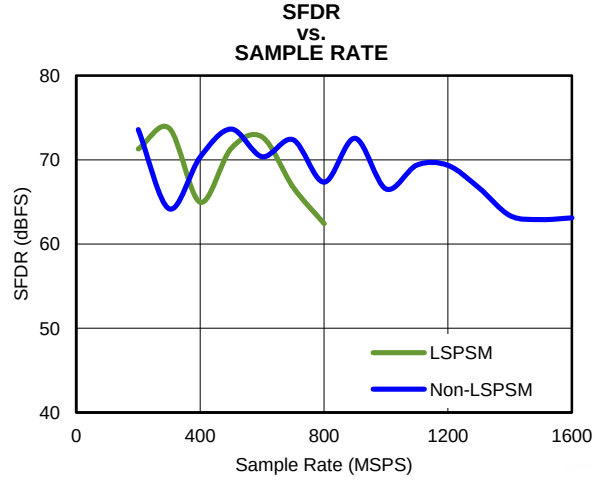


Figure 29.

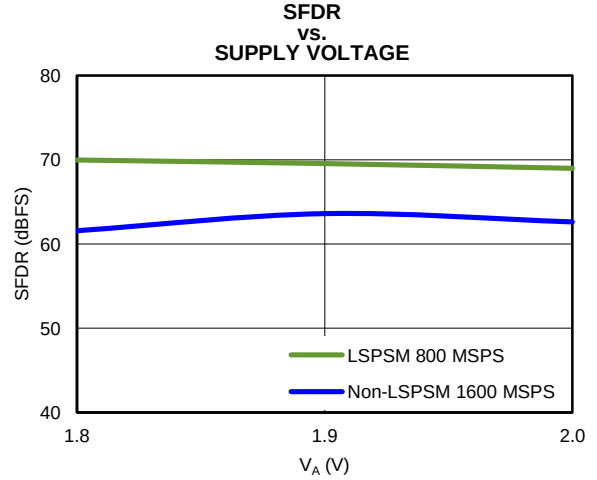


Figure 30.

Typical Performance Plots (continued)

V_A = V_{DR} = V_{TC} = V_E = 1.9V, f_{CLK} = 1600 MHz in Non-LSPSM and 800 MHz in LSPSM, f_{IN} = 248 MHz, T_A= 25°C, 1:2 Demux Non-DES Mode, and calibration performed after temperature, supply voltage or sample rate change, unless otherwise stated.

SFDR vs. TEMPERATURE

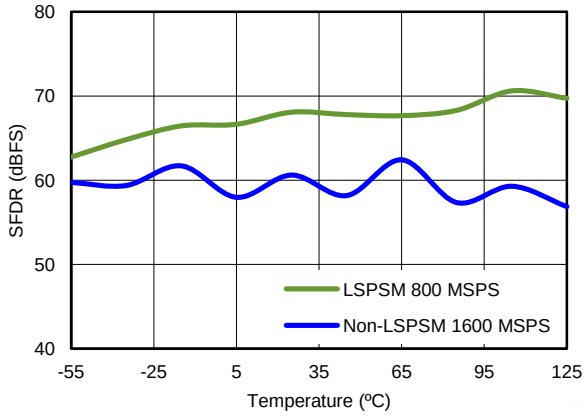


Figure 31.

SFDR vs. INPUT FREQUENCY

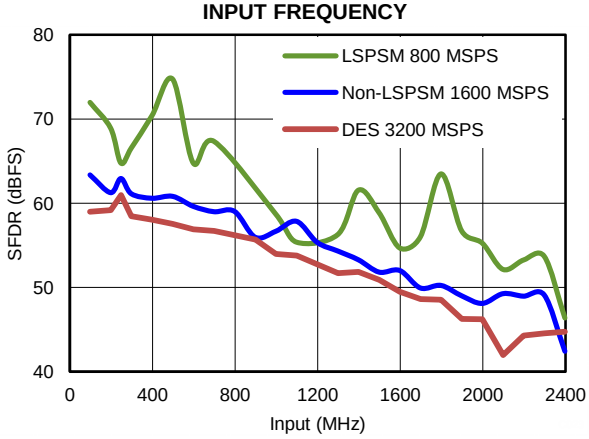


Figure 32.

ENOB vs. TEMPERATURE
Calibration at 50°C only
f_{CLK} = 1.38 GHz; f_{IN} = 770 MHz

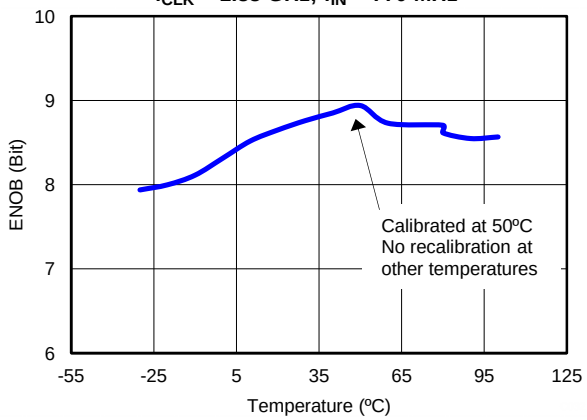


Figure 33.

SNR vs. TEMPERATURE
Calibration at 50°C only
f_{CLK} = 1.38 GHz; f_{IN} = 770 MHz

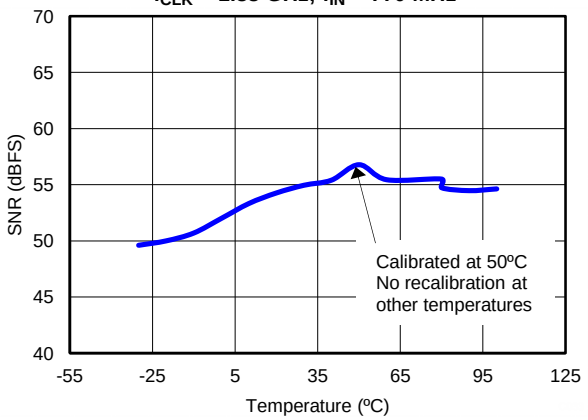


Figure 34.

THD vs. TEMPERATURE
Calibration at 50°C only
f_{CLK} = 1.38 GHz; f_{IN} = 770 MHz

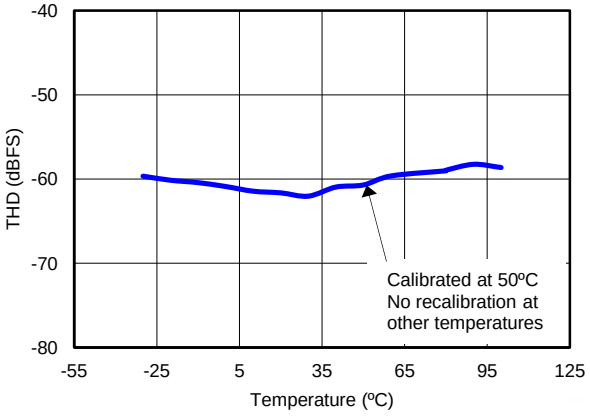


Figure 35.

SFDR vs. TEMPERATURE
Calibration at 50°C only
f_{CLK} = 1.38 GHz; f_{IN} = 770 MHz

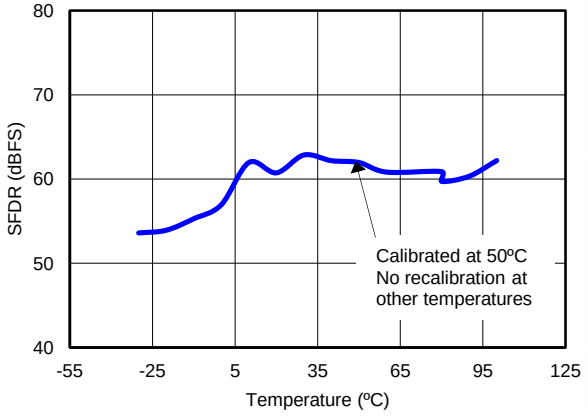


Figure 36.

Typical Performance Plots (continued)

$V_A = V_{DR} = V_{TC} = V_E = 1.9V$, f_{CLK} = 1600 MHz in Non-LSPSM and 800 MHz in LSPSM, f_{IN} = 248 MHz, T_A= 25°C, 1:2 Demux Non-DES Mode, and calibration performed after temperature, supply voltage or sample rate change, unless otherwise stated.

3rd ORDER INTERMODULATION DISTORTION vs. INPUT FREQUENCY

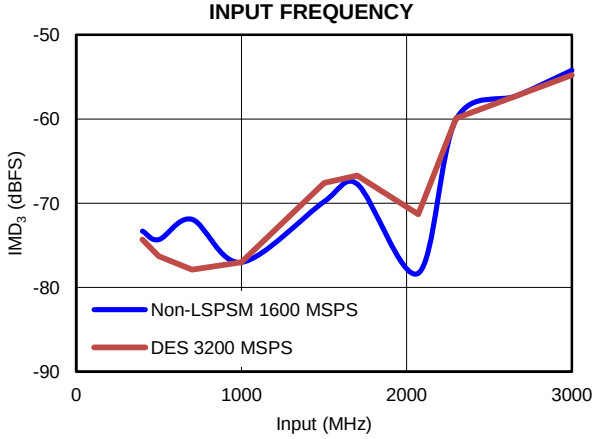


Figure 37.

3rd ORDER INTERMODULATION DISTORTION vs. INPUT FREQUENCY (DES MODE 3200 MSPS)

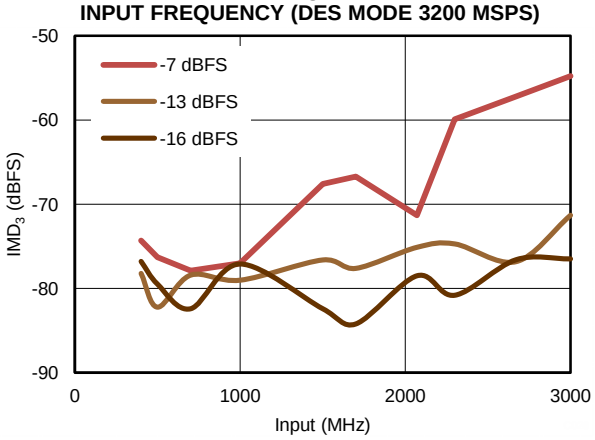


Figure 38.

CROSS TALK vs. INPUT FREQUENCY

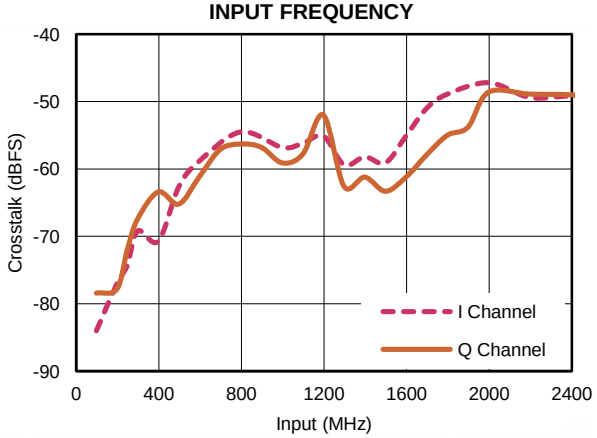


Figure 39.

INSERTION LOSS vs. INPUT FREQUENCY

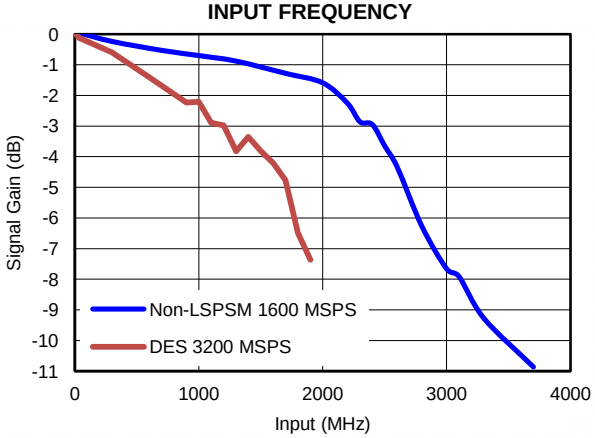


Figure 40.

POWER CONSUMPTION vs. SAMPLE RATE

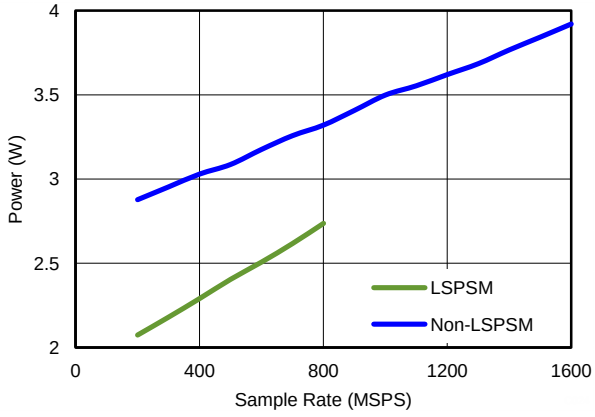


Figure 41.

Functional Description

The ADC12D1600 is a versatile A/D converter with an innovative architecture which permits very high speed operation. The controls available ease the application of the device to circuit solutions. Optimum performance requires adherence to the provisions discussed here and in the Applications Information. This section covers an overview, a description of control modes (Extended Control Mode and Non-Extended Control Mode), and features.

OVERVIEW

The ADC12D1600 uses a calibrated folding and interpolating architecture that achieves a high Effective Number of Bits (ENOB). The use of folding amplifiers greatly reduces the number of comparators and power consumption. Interpolation reduces the number of front-end amplifiers required, minimizing the load on the input signal and further reducing power requirements. In addition to correcting other non-idealities, on-chip calibration reduces the INL bow often seen with folding architectures. The result is an extremely fast, high performance, low power converter.

Operation Summary

A differential analog input is digitized into 12 bits. Differential input signals below the negative full-scale range will cause the output word to be all zeroes, while that about the positive full-scale range will result in the output word being all ones. If either case happens, the Out-of-Range output for the respective channel will have a logic-high signal.

There are 3 major sampling modes:

Dual channel ADC with a sample range of 200 to 1600 MSPS on each channel.

Dual channel ADC in Low Sampling Power Saving Mode (LSPSM) with a sampling range of 200 to 800 MSPS.

Single channel, interleaved ADC in Dual Edge Sampling with a sampling range of 250 to 3200 MSPS.

The part has many operating options. Some of these options can be controlled through pin configurations in Non-Extended Control Mode (Non-ECM or sometimes known as pin control mode). An expanded feature set is available in Extended Control Mode via the Serial Interface.

Each channel has a selectable output demultiplexer which feeds two LVDS buses. Depending upon the sampling mode, and the demux option chosen, the output data rate can be the same, one half or one quarter the sample rate.

CONTROL MODES

The ADC12D1600 may be operated in one of two control modes: Non-extended Control Mode (Non-ECM) or Extended Control Mode (ECM). In the simpler Non-ECM (also sometimes referred to as Pin Control Mode), the user affects available configuration and control of the device through the control pins. The ECM provides additional configuration and control options through a serial interface and a set of 16 registers, most of which are available to the user.

Non-Extended Control Mode

In Non-extended Control Mode (Non-ECM), the Serial Interface is not active and all available functions are controlled via various pin settings. Non-ECM is selected by setting the $\overline{ECE}$ Pin to logic-high. Note that, for the control pins, "logic-high" and "logic-low" refer to V_A and GND, respectively. Nine dedicated control pins provide a wide range of control for the ADC12D1600 and facilitate its operation. These control pins provide DES Mode selection, Demux Mode selection, DDR Phase selection, execute Calibration, Calibration Delay setting, Power Down I-channel, Power Down Q-channel, Test Pattern Mode selection, and Full-Scale Input Range selection. In addition to this, two dual-purpose control pins provide for AC/DC-coupled Mode selection and LVDS output common-mode voltage selection. See Table 6 for a summary.

Table 6. Non-ECM Pin Summary

Pin Name		Logic-Low	Logic-High	Floating
Dedicated Control Pins				
DES		Non-DES Mode	DES Mode	Not valid
NDM		Demux Mode	Non-Demux Mode	Not valid
DDRPh	DDR	0° Mode	90° Mode	Not valid
	SDR	Rising Edge	Falling Edge	
CAL		See Calibration Pin (CAL)		Not valid
LPSSM		Non-LSPSM	LSPSM	Not valid
PDI		I-channel active	Power Down I-channel	Power Down I-channel
PDQ		Q-channel active	Power Down Q-channel	Power Down Q-channel
TPM		Non-Test Pattern Mode	Test Pattern Mode	Not valid
FSR		Lower FS input Range	Higher FS input Range	Not valid
V_{BG}		Not allowed	Higher LVDS common-mode voltage	Lower LVDS common-mode voltage

Dual Edge Sampling Pin (DES)

The Dual Edge Sampling (DES) Pin selects whether the ADC12D1600 is in DES Mode (logic-high) or Non-DES Mode (logic-low). DES Mode means that a single analog input is sampled by both I- and Q-channels in a time-interleaved manner. One of the ADCs samples the input signal on the rising sampling clock edge (duty cycle corrected); the other ADC samples the input signal on the falling sampling clock edge (duty cycle corrected). In Non-ECM, only the I-input may be used for DES Mode, a.k.a. DESI Mode. In ECM, the Q-input may be selected via the DEQ Bit (Addr: 0**h**, Bit: 6), a.k.a. DESQ Mode. In ECM, both the I- and Q-inputs may be selected, a.k.a. DESIQ or DESCLKIQ Mode.

To use this feature in ECM, use the DES bit in the Configuration Register (Addr: 0**h**; Bit: 7). See DES/Non-DES Mode for more information.

Non-Demultiplexed Mode Pin (NDM)

The Non-Demultiplexed Mode (NDM) Pin selects whether the ADC12D1600 is in Demux Mode (logic-low) or Non-Demux Mode (logic-high). In Non-Demux Mode, the data from the input is produced at the sampled rate at a single 12-bit output bus. In Demux Mode, the data from the input is produced at half the sampled rate at twice the number of output buses. For Non-DES Mode, each I- or Q-channel will produce its data on one or two buses for Non-Demux or Demux Mode, respectively. For DES Mode, the selected channel will produce its data on two or four buses for Non-Demux or Demux Mode, respectively.

This feature is pin-controlled only and remains active during both Non-ECM and ECM. See Demux/Non-demux Mode for more information.

Dual Data Rate Phase Pin (DDRPh)

The Dual Data Rate Phase (DDRPh) Pin selects whether the ADC12D1600 is in 0° Mode (logic-low) or 90° Mode (logic-high) for DDR Mode. For DDR Mode, the Data may transition either with the DCLK transition (0° Mode) or halfway between DCLK transitions (90° Mode). The pin is only effective in the NDM pin is set to logic-low. If the device is in SDR Mode, then the DDRPh Pin selects whether the data transitions on the rising edge of DCLK (logic-low) or the falling edge of DCLK (logic-high). The DDRPh Pin selects the mode for both the I-channel: DI- and DId-to-DCLKI phase relationship and for the Q-channel: DQ- and DQd-to-DCLKQ phase relationship.

To use this feature in ECM, use the DPS bit in the Configuration Register (Addr: 0**h**; Bit: 14). See SDR / DDR Clock for more information.

Calibration Pin (CAL)

The Calibration (CAL) Pin may be used to execute an on-command calibration. The effect of calibration is to maximize the dynamic performance. To initiate an on-command calibration via the CAL pin, bring the CAL pin high for a minimum of t_{CAL_H} input clock cycles after it has been low for a minimum of t_{CAL_L} input clock cycles (See for Converter Electrical Characteristics – AC Electrical Characteristics clock cycle specification). ECM, this pin remains active and is logically OR'd with the CAL bit.

To use this feature in ECM, use the CAL bit in the Configuration Register (Addr: 0**h**; Bit: 15). See Calibration Feature for more information.

Low Sampling Power Saving Mode Pin (LSPSM)

The Low Sampling Power Saving Mode (LSPSM) Pin selects whether the part is in Non-LSPSM (logic-low) or Low Sampling Power Saving Mode (logic-high). IIn LSPSM, the input clock is limited to 800 MHz and the sample rate in Non-DES Mode is limited to 800 MSPS.

This pin remains active in ECM. See section Low Sampling Power Saving Mode (LSPSM) for more details.

Power Down I-channel Pin (PDI)

The Power Down I-channel (PDI) Pin selects whether the I-channel is powered down (logic-high) or active (logic-low). The digital data output pins, DI and DId, (both positive and negative) are put into a high impedance state when the I-channel is powered down. Upon return to the active state, the pipeline will contain meaningless information and must be flushed. The supply currents (typicals and limits) are available for the I-channel powered down or active and may be found in Converter Electrical Characteristics – Power Supply Characteristics . The device should be recalibrated following a power-cycle of PDI (or PDQ).

This pin remains active in ECM. In ECM, either this pin or the PDI bit (Addr: 0**h**; Bit: 11) in the Control Register may be used to power-down the I-channel. See Power Down for more information.

Power Down Q-channel Pin (PDQ)

The Power Down Q-channel (PDQ) Pin selects whether the Q-channel is powered down (logic-high) or active (logic-low). This pin functions similarly to the PDI pin, except that it applies to the Q-channel. The PDI and PDQ pins function independently of each other to control whether each I- or Q-channel is powered down or active.

This pin remains active in ECM. In ECM, either this pin or the PDQ bit (Addr: 0**h**; Bit: 10) in the Control Register may be used to power-down the Q-channel. See Power Down for more information.

Test Pattern Mode Pin (TPM)

The Test Pattern Mode (TPM) Pin selects whether the output of the ADC12D1600 is a test pattern (logic-high) or the converted analog input (logic-low). The ADC12D1600 can provide a test pattern at the four output buses independently of the input signal to aid in system debug. In TPM, the ADC is disengaged and a test pattern generator is connected to the outputs, including ORI and ORQ. See Test Pattern Mode for more information.

Full-Scale Input Range Pin (FSR)

The Full-Scale Input Range (FSR) Pin selects whether the full-scale input range for both the I- and Q-channel is higher (logic-high) or lower (logic-low). The input full-scale range is specified as V_{IN_FSR} in Converter Electrical Characteristics – Digital Control and Output Pin Characteristics. In Non-ECM, the full-scale input range for each I- and Q-channel may not be set independently, but it is possible to do so in ECM. The device must be calibrated following a change in FSR to obtain optimal performance.

To use this feature in ECM, use the Configuration Registers (Addr: 3**h** and B**h**). See Input Control and Adjust for more information.

LVDS Output Common-mode Pin (V_{BG})

The V_{BG} Pin serves a dual purpose. When functioning as an output, it provides the bandgap reference. When functioning as an input, it selects whether the LVDS output common-mode voltage is higher (logic-high) or lower (floating). The LVDS output common-mode voltage is specified as V_{OS} and may be found in Converter Electrical Characteristics – Digital Control and Output Pin Characteristics. This pin is always active, in both ECM and Non-ECM.

Extended Control Mode

In Extended Control Mode (ECM), most functions are controlled via the Serial Interface. In addition to this, several of the control pins remain active. See Table 9 for details. ECM is selected by setting the $\overline{ECE}$ Pin to logic-low. If the $\overline{ECE}$ Pin is set to logic-high (Non-ECM), then the registers are reset to their default values. So, a simple way to reset the registers is by toggling the $\overline{ECE}$ pin. Four pins on the ADC12D1600 control the Serial Interface: $\overline{SCS}$, SCLK, SDI and SDO. This section covers the Serial Interface. The Register Definitions are located at the end of the datasheet so that they are easy to find, see Register Definitions.

The Serial Interface

The ADC12D1600 offers a Serial Interface that allows access to the sixteen control registers within the device. The Serial Interface is a generic 4-wire (optionally 3-wire) synchronous interface that is compatible with SPI type interfaces that are used on many micro-controllers and DSP controllers. Each serial interface access cycle is exactly 24 bits long. A register-read or register-write can be accomplished in one cycle. The signals are defined in such a way that the user can opt to simply join SDI and SDO signals in his system to accomplish a single, bidirectional SDI/O signal. A summary of the pins for this interface may be found in Table 7. See Figure 12 for the timing diagram and Converter Electrical Characteristics – AC Electrical Characteristics for timing specification details. Control register contents are retained when the device is put into power-down mode. If this feature is unused, the SCLK, SDI, and $\overline{SCS}$ pins may be left floating because they each have an internal pull-up.

Table 7. Serial Interface Pins

Pin	Name
C4	$\overline{SCS}$ (Serial Chip Select bar)
C5	SCLK (Serial Clock)
B4	SDI (Serial Data In)
A3	SDO (Serial Data Out)

$\overline{SCS}$: Each assertion (logic-low) of this signal starts a new register access, i.e. the SDI command field must be ready on the following SCLK rising edge. The user is required to de-assert this signal after the 24th clock. If the $\overline{SCS}$ is de-asserted before the 24th clock, no data read/write will occur. For a read operation, if the $\overline{SCS}$ is asserted longer than 24 clocks, the SDO output will hold the D0 bit until $\overline{SCS}$ is de-asserted. For a write operation, if the $\overline{SCS}$ is asserted longer than 24 clocks, data write will occur normally through the SDI input upon the 24th clock. Setup and hold times, t_{SCS} and t_{HCS}, with respect to the SCLK must be observed. $\overline{SCS}$ must be toggled in between register access cycles.

SCLK: This signal is used to register the input data (SDI) on the rising edge; and to source the output data (SDO) on the falling edge. The user may disable the clock and hold it at logic-low. There is no minimum frequency requirement for SCLK; see f_{SCLK} in Converter Electrical Characteristics – AC Electrical Characteristics for more details.

SDI: Each register access requires a specific 24-bit pattern at this input, consisting of a command field and a data field. If the SDI and SDO wires are shared (3-wire mode), then during read operations, it is necessary to tri-state the master which is driving SDI while the data field is being output by the ADC on SDO. The master must be tri-stated before the falling edge of the 8^{th} clock. If SDI and SDO are not shared (4-wire mode), then this is not necessary. Setup and hold times, t_{SH} and t_{SSU}, with respect to the SCLK must be observed.

SDO: This output is normally tri-stated and is driven only when $\overline{SCS}$ is asserted, the first 8 bits of command data have been received and it is a READ operation. The data is shifted out, MSB first, starting with the 8th clock's falling edge. At the end of the access, when $\overline{SCS}$ is de-asserted, this output is tri-stated once again. If an invalid address is accessed, the data sourced will consist of all zeroes. If it is a read operation, there will be a bus turnaround time, t_{BSU}, from when the last bit of the command field was read in until the first bit of the data field is written out.

Table 8 shows the Serial Interface bit definitions.

Table 8. Command and Data Field Definitions

Bit No.	Name	Comments
1	Read/Write (R/W)	1**b** indicates a read operation 0**b** indicates a write operation
2-3	Reserved	Bits must be set to 10**b**
4-7	A<3:0>	16 registers may be addressed. The order is MSB first
8	X	This is a "don't care" bit
9-24	D<15:0>	Data written to or read from addressed register

The serial data protocol is shown for a read and write operation in Figure 42 and Figure 43, respectively.

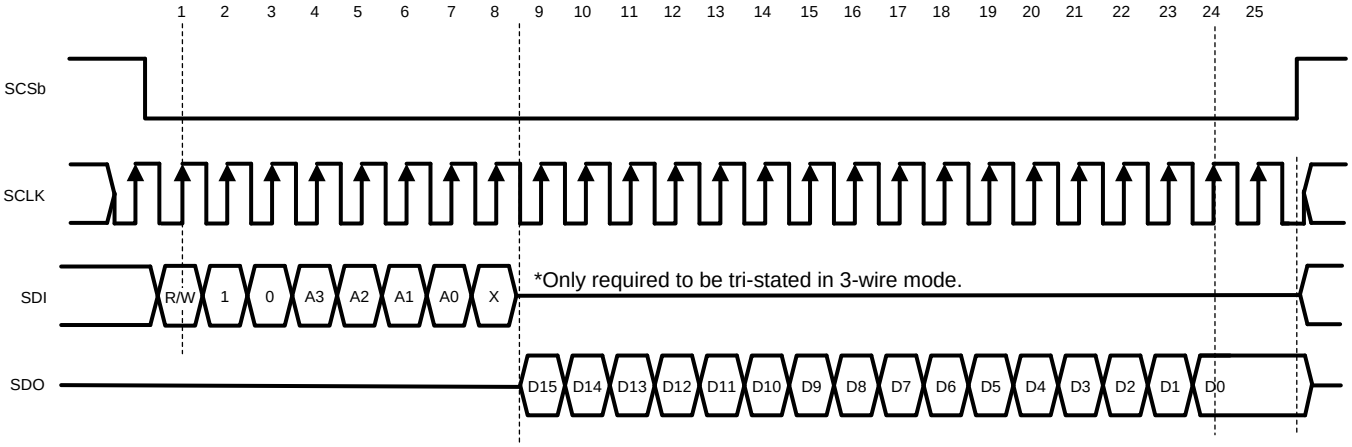


Figure 42. Serial Data Protocol - Read Operation

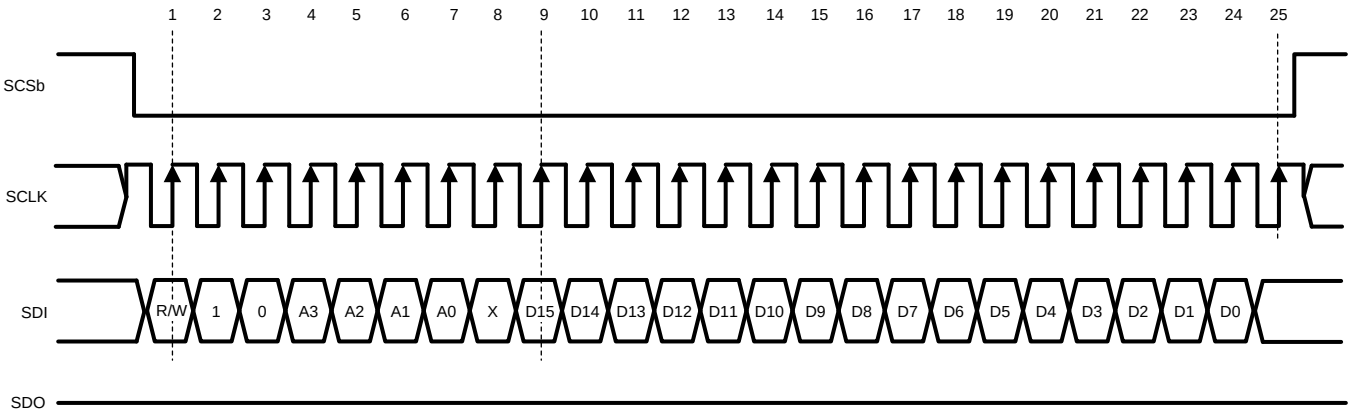


Figure 43. Serial Data Protocol - Write Operation

FEATURES

The ADC12D1600 offers many features to make the device convenient to use in a wide variety of applications. Table 9 is a summary of the features available, as well as details for the control mode chosen. "N/A" means "Not Applicable."

Table 9. Features and Modes

Feature	Non-ECM	Control Pin Active in ECM	ECM	Default ECM State
Input Control and Adjust				
Input Full-scale Range Adjust	Selected via FSR (Pin Y3)	No	Selected via the Config Reg (Addr: 3**h** and B**h**)	Mid FSR value
Input Offset Adjust Setting	Not available	N/A	Selected via the Config Reg (Addr: 2**h** and A**h**)	Offset = 0 mV
Low Sampling Power Saving Mode	Selected via LSPSM (Pin V4)	Yes	Not Available	N/A
DES / Non-DES Mode Selection	Selected via DES (Pin V5)	No	Selected via the DES Bit (Addr: 0**h**; Bit: 7)	Non-DES Mode
DES Mode Input Selection	Not available	N/A	Selected via the DEQ, DIQ Bits (Addr: 0**h**; Bits: 6:5)	N/A
DESCLKIQ Mode	Not available	N/A	Selected via the DCK Bit (Addr: E**h**; Bit: 6)	N/A
DES Timing Adjust	Not available	N/A	Selected via the DES Timing Adjust Reg (Addr: 7**h**)	Mid skew offset
Sampling Clock Phase Adjust	Not available	N/A	Selected via the Config Reg (Addr: C**h** and D**h**)	t_{AD} adjust disabled
Output Control and Adjust				
DDR Clock Phase Selection	Selected via DDRPh (Pin W4)	No	Selected via the DPS Bit (Addr: 0**h**; Bit: 14)	0° Mode
DDR / SDR DCLK Selection	Not available	N/A	Selected via the SDR Bit (Addr: 0**h**; Bit: 2)	DDR Mode
SDR Rising / Falling DCLK Selection	Not available	N/A	Selected via the DPS Bit (Addr: 0**h**; Bit: 14)	N/A
LVDS Differential Voltage Amplitude Selection	Higher amplitude only	N/A	Selected via the OVS Bit (Addr: 0**h**; Bit: 13)	Higher amplitude
LVDS Common-Mode Voltage Amplitude Selection	Selected via V_{BG} (Pin B1)	Yes	Not available	N/A
Output Formatting Selection	Offset Binary only	N/A	Selected via the 2SC Bit (Addr: 0**h**; Bit: 4)	Offset Binary
Test Pattern Mode at Output	Selected via TPM (Pin A4)	No	Selected via the TPM Bit (Addr: 0**h**; Bit: 12)	TPM disabled
Demux/Non-Demux Mode Selection	Selected via NDM (Pin A5)	Yes	Not available	N/A
AutoSync	Not available	N/A	Selected via the Config Reg (Addr: E**h**)	Master Mode, RCOut1/2 disabled
DCLK Reset	Not available	N/A	Selected via the Config Reg (Addr: E**h**; Bit: 0)	DCLK Reset disabled
Time Stamp	Not available	N/A	Selected via the TSE Bit (Addr: 0**h**; Bit: 3)	Time Stamp disabled
Calibration				
On-command Calibration	Selected via CAL (Pin D6)	Yes	Selected via the CAL Bit (Addr: 0**h**; Bit: 15)	N/A (CAL = 0)
Calibration Adjust	Not available	N/A	Selected via the Config Reg (Addr: 4**h**)	t_{CAL}
Read/Write Calibration Settings	Not available	N/A	Selected via the SSC Bit (Addr: 4**h**; Bit: 7)	R/W calibration values disabled
Power-Down				
Power down I-channel	Selected via PDI (Pin U3)	Yes	Selected via the PDI Bit (Addr: 0**h**; Bit: 11)	I-channel operational
Power down Q-channel	Selected via PDQ (Pin V3)	Yes	Selected via the PDQ Bit (Addr: 0**h**; Bit: 10)	Q-channel operational

Input Control and Adjust

There are several features and configurations for the input of the ADC12D1600 so that it may be used in many different applications. This section covers AC/DC-coupled Mode, input full-scale range adjust, input offset adjust, DES/Non-DES Mode, and sampling clock phase adjust.

Input Full-Scale Range Adjust

The input full-scale range for the ADC12D1600 may be adjusted via Non-ECM or ECM. In Non-ECM, a control pin selects a higher or lower value; see Full-Scale Input Range Pin (FSR). In ECM, the input full-scale range may be adjusted with 15-bits of precision. See V_{IN_FSR} in Converter Electrical Characteristics – Analog Input/Output and Reference Characteristics for electrical specification details. Note that the higher and lower full-scale input range settings in Non-ECM correspond to the mid and min full-scale input range settings in ECM. It is necessary to execute an on-command calibration following a change of the input full-scale range. See Register Definitions for information about the registers.

Input Offset Adjust

The input offset adjust for the ADC12D1600 may be adjusted with 12-bits of precision plus sign via ECM. See Register Definitions for information about the registers.

Low Sampling Power Saving Mode

For applications with input clock speeds 200 to 800 MHz, the ADC12D1600 can be switched to the Low Sampling Power Saving Mode for a reduction in power consumption of approximately 20%. SeeLow Sampling Power Saving Mode Pin (LSPSM) for information on how to select the desired mode and Low Sampling Power Saving Mode (LSPSM) for details on operation in this mode.

DES/Non-DES Mode

The ADC12D1600 can operate in Dual-Edge Sampling (DES) or Non-DES Mode. The DES Mode allows for a single analog input to be sampled by both I- and Q-channels. One channel samples the input on the rising edge of the sampling clock and the other samples the same input signal on the falling edge of the sampling clock. A single input is thus sampled twice per clock cycle, resulting in an overall sample rate of twice the sampling clock frequency, e.g. 3.2/2.0 GSPS with a 1600/1000 MHz sampling clock. Since DES Mode uses both I- and Q-channels to process the input signal, both channels must be powered up for the DES Mode to function properly.

In Non-ECM, only the I-input may be used for the DES Mode input. See Dual Edge Sampling Pin (DES) for information on how to select the DES Mode. In ECM, either the I- or Q-input may be selected by first using the DES bit (Addr: 0**h**, Bit 7) to select the DES Mode. The DEQ Bit (Addr: 0**h**, Bit: 6) is used to select the Q-input, but the I-input is used by default. Also, both I- and Q-inputs may be driven externally, i.e. DESIQ Mode, by using the DIQ bit (Addr: 0**h**, Bit 5). See THE ANALOG INPUTS for more information about how to drive the ADC in DES Mode.

In DESCLKIQ Mode, the I- and Q-channels sample their inputs 180° out-of-phase with respect to one another, similar to the other DES Modes. DESCLKIQ Mode is similar to the DESIQ Mode, except that the I- and Q-channels remain electrically separate internal to the ADC12D1600. For this reason, both I- and Q-inputs must be externally driven for the DESCLKIQ Mode. The DCK Bit (Addr: E**h**, Bit: 6) is used to select the 180° sampling clock mode.

The DESCLKIQ Mode results in the best bandwidth for the interleaved modes. In general, the bandwidth decreases from Non-DES Mode to DES Mode (specifically, DESI or DESQ) because both channels are sampling off the same input signal and non-ideal effects introduced by interleaving the two channels lower the bandwidth. Driving both I- and Q-channels externally (DESIQ Mode and DESCLKIQ Mode) results in better bandwidth because each channel is being driven, which reduces routing losses. The DESCLKIQ Mode has better bandwidth than the DESIQ Mode because the routing internal to the ADC12D1600/1000 is simpler, which results in less insertion loss.

In the DES Mode, the outputs must be carefully interleaved in order to reconstruct the sampled signal. If the device is programmed into the 1:4 Demux DES Mode, the data is effectively demultiplexed by 1:4. If the sampling clock is 1600/1000 MHz, the effective sampling rate is doubled to 3.2/2.0 GSPS and each of the 4 output buses has an output rate of 800/500 MSPS. All data is available in parallel. To properly reconstruct the sampled waveform, the four bytes of parallel data that are output with each DCLK must be correctly interleaved. The sampling order is as follows, from the earliest to the latest: DQd, DId, DQ, DI. See Figure 6. If the device is programmed into the Non-Demux DES Mode, two bytes of parallel data are output with each edge of the DCLK in the following sampling order, from the earliest to the latest: DQ, DI. See Figure 7.

DES Timing Adjust

The performance of the ADC12D1600 in DES Mode depends on how well the two channels are interleaved, i.e. that the clock samples either channel with precisely a 50% duty-cycle, each channel has the same offset (nominally code 2047/2048), and each channel has the same full-scale range. The ADC12D1600 includes an automatic clock phase background adjustment in DES Mode to automatically and continuously adjust the clock phase of the I- and Q-channels. In addition to this, the residual fixed timing skew offset may be further manually adjusted, and further reduce timing spurs for specific applications. See the DES Timing Adjust (Addr: 7**h**). As the DES Timing Adjust is programmed from 0**d** to 127**d**, the magnitude of the Fs/2-Fin timing interleaving spur will decrease to a local minimum and then increase again. The default, nominal setting of 64**d** may or may not coincide with this local minimum. The user may manually skew the global timing to achieve the lowest possible timing interleaving spur.

Sampling Clock Phase Adjust

The sampling clock (CLK) phase may be delayed internally to the ADC up to 825 ps in ECM. This feature is intended to help the system designer remove small imbalances in clock distribution traces at the board level when multiple ADCs are used, or to simplify complex system functions such as beam steering for phase array antennas.

Additional delay in the clock path also creates additional jitter when using the sampling clock phase adjust. Because the sampling clock phase adjust delays all clocks, including the DCLKs and output data, the user is strongly advised to use the minimal amount of adjustment and verify the net benefit of this feature in his system before relying on it.

Output Control and Adjust

There are several features and configurations for the output of the ADC12D1600 so that it may be used in many different applications. This section covers DDR clock phase, LVDS output differential and common-mode voltage, output formatting, Demux/Non-demux Mode, Test Pattern Mode, and Time Stamp.

SDR / DDR Clock

The ADC12D1600 output data can be delivered in Double Data Rate (DDR) or Single Data Rate (SDR). For DDR, the DCLK frequency is half the data rate and data is sent to the outputs on both edges of DCLK; see Figure 44. The DCLK-to-Data phase relationship may be either 0° or 90°. For 0° Mode, the Data transitions on each edge of the DCLK. Any offset from this timing is t_{OSK}; (see Converter Electrical Characteristics – AC Electrical Characteristics for details). For 90° Mode, the DCLK transitions in the middle of each Data cell. Setup and hold times for this transition, t_{SU} and t_H, may also be found in Converter Electrical Characteristics – AC Electrical Characteristics. The DCLK-to-Data phase relationship may be selected via the DDRPh Pin in Non-ECM (see Dual Data Rate Phase Pin (DDRPh)) or the DPS bit in the Configuration Register (Addr: 0**h**; Bit: 14) in ECM. Note that for DDR Mode, the 1:2 Demux Mode is not available.

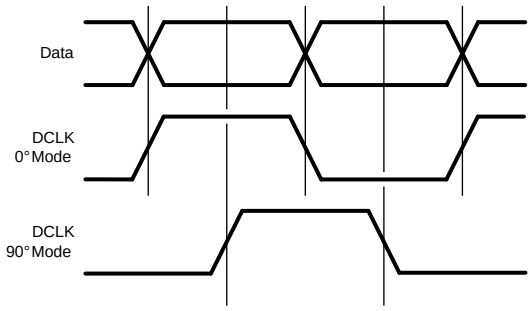


Figure 44. DDR DCLK-to-Data Phase Relationship

For SDR, the DCLK frequency is the same as the data rate and data is sent to the outputs on a single edge of DCLK; see Figure 45. The Data may transition on either the rising or falling edge of DCLK. Any offset from this timing is t_{OSK}; see Converter Electrical Characteristics – AC Electrical Characteristics for details. The DCLK rising / falling edge may be selected via the SDR bit in the Configuration Register (Addr: 0**h**; Bit: 2) in ECM only.

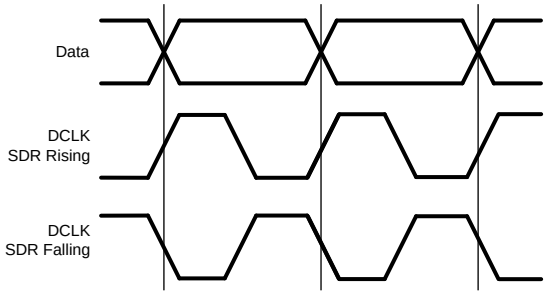


Figure 45. SDR DCLK-to-Data Phase Relationship

LVDS Output Differential Voltage

The ADC12D1600 is available with a selectable higher or lower LVDS output differential voltage. This parameter is V_{OD} and may be found in Converter Electrical Characteristics – Digital Control and Output Pin Characteristics. The desired voltage may be selected via the OVS Bit (Addr: 0**h**, Bit 13). For many applications, in which the LVDS outputs are very close to an FPGA on the same board, for example, the lower setting is sufficient for good performance; this will also reduce the possibility for EMI from the LVDS outputs to other signals on the board. See Register Definitions for more information.

LVDS Output Common-Mode Voltage

The ADC12D1600 is available with a selectable higher or lower LVDS output common-mode voltage. This parameter is V_{OS} and may be found in Converter Electrical Characteristics – Digital Control and Output Pin Characteristics. See LVDS Output Common-mode Pin (V_{BG}) for information on how to select the desired voltage.

Output Formatting

The formatting at the digital data outputs may be either offset binary or two's complement. The default formatting is offset binary, but two's complement may be selected via the 2SC Bit (Addr: 0**h**, Bit 4); see Register Definitions for more information.

Demux/Non-demux Mode

The ADC12D1600 may be in one of two demultiplex modes: Demux Mode or Non-Demux Mode (also sometimes referred to as 1:1 Demux Mode). In Non-Demux Mode, the data from the input is simply output at the sampling rate on one 12-bit bus. In Demux Mode, the data from the input is output at half the sampling rate, on twice the number of buses. Demux/Non-Demux Mode may only be selected by the NDM pin. In Non-DES Mode, the output data from each channel may be demultiplexed by a factor of 1:2 (1:2 Demux Non-DES Mode) or not demultiplexed (Non-Demux Non-DES Mode). In DES Mode, the output data from both channels interleaved may be demultiplexed (1:4 Demux DES Mode) or not demultiplexed (Non-Demux DES Mode).

See Table 10 for a selection of available modes.

Table 10. Supported Demux, Data Rate Modes

	Non-Demux Mode	1:2 Demux Mode
DDR	0° Mode only	0° Mode / 90° Mode
SDR	Not available	Rising / Falling Mode

Test Pattern Mode

The ADC12D1600 can provide a test pattern at the four output buses independently of the input signal to aid in system debug. In Test Pattern Mode, the ADC is disengaged and a test pattern generator is connected to the outputs, including ORI and ORQ. The test pattern output is the same in DES Mode or Non-DES Mode. Each port is given a unique 12-bit word, alternating between 1's and 0's. When the part is programmed into the Demux Mode, the test pattern's order is described in Table 11. If the I- or Q-channel is powered down, the test pattern will not be output for that channel.

Table 11. Test Pattern by Output Port in Non-LSPSM Demux Mode

Time	Qd	Id	Q	I	ORQ	ORI	Comments
T0	000**h**	004**h**	008**h**	010**h**	0**b**	0**b**	Pattern Sequence **n**
T1	FFF**h**	FFB**h**	FF7**h**	FEF**h**	1**b**	1**b**	
T2	000**h**	004**h**	008**h**	010**h**	0**b**	0**b**	
T3	FFF**h**	FFB**h**	FF7**h**	FEF**h**	1**b**	1**b**	
T4	000**h**	004**h**	008**h**	010**h**	0**b**	0**b**	
T5	000**h**	004**h**	008**h**	010**h**	0**b**	0**b**	Pattern Sequence **n+1**
T6	FFF**h**	FFB**h**	FF7**h**	FEF**h**	1**b**	1**b**	
T7	000**h**	004**h**	008**h**	010**h**	0**b**	0**b**	
T8	FFF**h**	FFB**h**	FF7**h**	FEF**h**	1**b**	1**b**	
T9	000**h**	004**h**	008**h**	010**h**	0**b**	0**b**	
T10	000**h**	004**h**	008**h**	010**h**	0**b**	0**b**	Pattern Sequence **n+2**
T11	FFF**h**	FFB**h**	FF7**h**	FEF**h**	1**b**	1**b**	
T12	000**h**	004**h**	008**h**	010**h**	0**b**	0**b**	
T13	...	...	...	...	...	...	

When the part is programmed into the Non-Demux Mode, the test pattern's order is described in Table 12.

Table 12. Test Pattern by Output Port in Non-LSPMS Non-Demux Mode

Time	Q	I	ORQ	ORI	Comments
T0	000**h**	004**h**	0**b**	0**b**	Pattern Sequence **n**
T1	000**h**	004**h**	0**b**	0**b**	
T2	FFF**h**	FFB**h**	1**b**	1**b**	
T3	FFF**h**	FFB**h**	1**b**	1**b**	
T4	000**h**	004**h**	0**b**	0**b**	
T5	FFF**h**	FFB**h**	1**b**	1**b**	
T6	000**h**	004**h**	0**b**	0**b**	
T7	FFF**h**	FFB**h**	1**b**	1**b**	
T8	FFF**h**	FFB**h**	1**b**	1**b**	
T9	FFF**h**	FFB**h**	1**b**	1**b**	
T10	000**h**	004**h**	0**b**	0**b**	Pattern Sequence **n+1**
T11	000**h**	004**h**	0**b**	0**b**	
T12	FFF**h**	FFB**h**	1**b**	1**b**	
T13	FFF**h**	FFB**h**	1**b**	1**b**	
T14	...	...	...	...	

Table 13. Test Pattern by Output Port in LSPSM Demux Mode

Time	Qd	Id	Q	I	ORQ	ORI	Comments
T0	FF7**h**	FEF**h**	008**h**	010**h**	1**b**	1**b**	Pattern Sequence **n**
T1	FF7**h**	FEF**h**	008**h**	010**h**	1**b**	1**b**	
T2	008**h**	010**h**	FF7**h**	FEF**h**	1**b**	1**b**	
T3	008**h**	010**h**	FF7**h**	FEF**h**	1**b**	1**b**	
T4	008**h**	010**h**	008**h**	010**h**	0**b**	0**b**	
T5	FF7**h**	FEF**h**	008**h**	010**h**	1**b**	1**b**	Pattern Sequence **n+1**
T6	FF7**h**	FEF**h**	008**h**	010**h**	1**b**	1**b**	
T7	008**h**	010**h**	FF7**h**	FEF**h**	1**b**	1**b**	
T8	008**h**	010**h**	FF7**h**	FEF**h**	1**b**	1**b**	
T9	008**h**	010**h**	008**h**	010**h**	0**b**	0**b**	
T10	FF7**h**	FEF**h**	008**h**	010**h**	1**b**	1**b**	Pattern Sequence **n+2**
T11	FF7**h**	FEF**h**	008**h**	010**h**	1**b**	1**b**	
T12	008**h**	010**h**	FF7**h**	FEF**h**	1**b**	1**b**	
T13	...	...	...	...	...	...	

Table 14. Test Pattern by Output Port in LSPSM Non-Demux Mode

Time	Q	I	ORQ	ORI	Comments
T0	008**h**	010**h**	0**b**	0**b**	Pattern Sequence **n**
T1	FF7**h**	FEF**h**	1**b**	1**b**	
T2	008**h**	010**h**	0**b**	0**b**	
T3	FF7**h**	FEF**h**	1**b**	1**b**	
T4	008**h**	010**h**	0**b**	0**b**	
T5	008**h**	010**h**	0**b**	0**b**	Pattern Sequence **n+1**
T6	FF7**h**	FEF**h**	1**b**	1**b**	
T7	008**h**	010**h**	0**b**	0**b**	
T8	FF7**h**	FEF**h**	1**b**	1**b**	
T9	008**h**	010**h**	0**b**	0**b**	
T10	008**h**	010**h**	0**b**	0**b**	Pattern Sequence **n+2**
T11	FF7**h**	FEF**h**	1**b**	1**b**	
T12	008**h**	010**h**	0**b**	0**b**	
T13	FF7**h**	FEF**h**	1**b**	1**b**	
T14	...	...	...	...	

Time Stamp

The Time Stamp feature enables the user to capture the timing of an external trigger event, relative to the sampled signal. When enabled via the TSE Bit (Addr: 0**h**; Bit: 3), the LSB of the digital outputs (DQd, DQ, DId, DI) captures the trigger information. In effect, the 12-bit converter becomes an 11-bit converter and the LSB acts as a 1-bit converter with the same latency as the 11-bit converter. The trigger should be applied to the DCLK_RST input. It may be asynchronous to the ADC sampling clock.

Calibration Feature

The ADC12D1600 calibration must be run to achieve specified performance. The calibration procedure is exactly the same regardless of how it was initiated or when it is run. Calibration trims the analog input differential termination resistors, the CLK input resistor, and sets internal bias currents which affect the linearity of the converter. This minimizes full-scale error, offset error, DNL and INL, which results in the maximum dynamic performance, as measured by: SNR, THD, SINAD (SNDR) and ENOB.

Calibration Control Pins and Bits

Table 15 is a summary of the pins and bits used for calibration. See Pin Descriptions and Equivalent Circuits for complete pin information and Figure 11 for the timing diagram.

Table 15. Calibration Pins

Pin (Bit)	Name	Function
D6 (Addr: 0**h**; Bit 15)	CAL (Calibration)	Initiate calibration
(Addr: 4**h**)	Calibration Adjust	Adjust calibration sequence
B5	CalRun (Calibration Running)	Indicates while calibration is running
C1/D2	Rtrim+/- (Input termination trim resistor)	External resistor used to calibrate analog and CLK inputs
C3/D3	Rext+/- (External Reference resistor)	External resistor used to calibrate internal linearity

How to Execute a Calibration

Calibration may be initiated by holding the CAL pin low for at least t_{CAL_L} clock cycles, and then holding it high for at least another t_{CAL_H} clock cycles, as defined in Converter Electrical Characteristics – AC Electrical Characteristics. The minimum t_{CAL_L} and t_{CAL_H} input clock cycle sequences are required to ensure that random noise does not cause a calibration to begin when it is not desired. The time taken by the calibration procedure is specified as t_{CAL}. The CAL Pin is active in both ECM and Non-ECM. However, in ECM, the CAL Pin is logically OR'd with the CAL Bit, so both the pin and bit are required to be set low before executing another calibration via either pin or bit.

On-command Calibration

In addition to executing a calibration after power-on and part stabilization, it is recommended to execute an on-command calibration whenever the settings or conditions to the device are altered significantly, in order to obtain optimal parametric performance. Some examples include: changing the FSR via either ECM or Non-ECM, power-cycling either channel, and switching into or out of DES Mode. For best performance, it is also recommended that an on-command calibration be run 20 seconds or more after application of power and whenever the operating temperature changes significantly, relative to the specific system performance requirements. See Typical Performance Plots for the impact temperature change can have on the performance of the part without recalibration.

Due to the nature of the calibration feature, it is recommended to avoid unnecessary activities on the device while the calibration is taking place. For example, do not read or write to the Serial Interface or use the DCLK Reset feature while calibrating the ADC. Doing so will impair the performance of the device until it is re-calibrated correctly. Also, it is recommended to not apply a strong narrow-band signal to the analog inputs during calibration because this may impair the accuracy of the calibration; broad spectrum noise is acceptable.

Calibration Adjust

The sequence of the calibration event itself may be adjusted. This feature can be used if a shorter calibration time than the default is required; see t_{CAL} in Converter Electrical Characteristics – AC Electrical Characteristics. However, the performance of the device, may be compromised when using this feature.

The calibration sequence may be adjusted via CSS (Addr: 4**h**, Bit 14). The default setting of CSS = 1**b** executes both R_{IN} and R_{IN_CLK} Calibration (using Rtrim) and internal linearity Calibration (using Rext). Executing a calibration with CSS = 0**b** executes only the internal linearity Calibration. The first time that Calibration is executed, it must be with CSS = 1**b** to trim R_{IN} and R_{IN_CLK}. However, once the device is at its operating temperature and R_{IN} has been trimmed at least one time, it will not drift significantly. To save time in subsequent calibrations, trimming R_{IN} and R_{IN_CLK} may be skipped, i.e. by setting CSS = 0**b**.

Read/Write Calibration Settings

When the ADC performs a calibration, the calibration constants are stored in an array which is accessible via the Calibration Values register (Addr: 5**h**). To save the time which it takes to execute a calibration, t_{CAL}, or to allow re-use of a previous calibration result, these values can be read from and written to the register at a later time. For example, if an application requires the same input impedance, R_{IN}, this feature can be used to load a previously determined set of values. For the calibration values to be valid, the ADC must be operating under the same conditions, including temperature, at which the calibration values were originally determined by the ADC.

To read calibration values from the SPI, do the following:

1. Set ADC to desired operating conditions.
2. Set SSC (Addr: 4**h**, Bit 7) to 1.
3. Read exactly 240 times the Calibration Values register (Addr: 5**h**). The register values are R0, R1, R2... R239 where R0 is a dummy value. The contents of R<239:1> should be stored.
4. Set SSC (Addr: 4**h**, Bit 7) to 0.
5. Continue with normal operation.

To write calibration values to the SPI, do the following:

1. Set ADC to operating conditions at which Calibration Values were previously read.
2. Set SSC (Addr: 4**h**, Bit 7) to 1.
3. Write exactly 239 times the Calibration Values register (Addr: 5**h**). The registers should be written with stored register values R1, R2... R239.
4. Make two additional dummy writes of 0000**h**.
5. Set SSC (Addr: 4**h**, Bit 7) to 0.
6. Continue with normal operation.

Calibration and Power-Down

If PDI and PDQ are simultaneously asserted during a calibration cycle, the ADC12D1600 will immediately power down. The calibration cycle will continue when either or both channels are powered back up, but the calibration will be compromised due to the incomplete settling of bias currents directly after power up. Therefore, a new calibration should be executed upon powering the ADC12D1600 back up. In general, the ADC12D1600 should be recalibrated when either or both channels are powered back up, or after one channel is powered down. For best results, this should be done after the device has stabilized to its operating temperature.

Calibration and the Digital Outputs

During calibration, the digital outputs (including DI, DId, DQ, DQd and OR) are set logic-low, to reduce noise. The DCLK runs continuously during calibration. After the calibration is completed and the CalRun signal is logic-low, it takes an additional 60 Sampling Clock cycles before the output of the ADC12D1600 is valid converted data from the analog inputs. This is the time it takes for the pipeline to flush, as well as for other internal processes.

Power Down

On the ADC12D1600, the I- and Q-channels may be powered down individually. This may be accomplished via the control pins, PDI and PDQ, or via ECM. In ECM, the PDI and PDQ pins are logically OR'd with the Control Register setting. See Power Down I-channel Pin (PDI) andPower Down Q-channel Pin (PDQ) for more information.

Low Sampling Power Saving Mode (LSPSM)

For applications with input clock speeds of 200 to 800 MHz (sample rates of 200 to 800 MSPS in Non-DES mode), the ADC may be put in Low Sampling Power Saving Mode (LSPSM) using the LSPSM (V4) pin (see Low Sampling Power Saving Mode Pin (LSPSM)). LSPSM powers down certain areas of the part, reduces the power consumption by approximately 20% and may improve the spectral purity of the output. In 1:2 Demux mode, the output will be in SDR and DLCK frequency will be Fs/2. In Non-Demux mode, the output is switchable between DDR and SDR.

APPLICATIONS INFORMATION

SYSTEM POWER-ON CONSIDERATIONS

Control Pins

Upon power-on, the Control Pins need to be set to the proper configuration per Table 6, ensuring the abs max values in Absolute Maximum Ratings are not violated. This can be done through either pull-up and pull-down ressitors to V_A and V_{GND} or through an FPGA or ASIC. If using and FPGA or ASIC, it is not recommended to write to the Control Pins or SPI before power is applied to the ADC12D1600.

Power-On in Non-ECM

If the part is in Non-ECM at power-on, the control registers will be configured in the default mode shown in Table 9 and Register Definitions. The part may be run in Non-ECM or switched to ECM and have the registered changed through the SPI per Extended Control Mode. After the part has been configured and has stabilized, a calibration should be run per Calibration Feature.

Power-On in ECM

If the part is in ECM at power-on, the control registers will come up in an unknown, random state. It is necessary to configure the registers through the SPI per Extended Control Mode or the registers can be set to the default settings in Table 9 by toggling the $\overline{ECE}$ pin logic-high and then logic-low. After the part has been configured and has stabilized, a calibration should be run per Calibration Feature.

Power-on and Data Clock (DCLK)

Many applications use the DCLK output for a system clock. For the ADC12D1600, each I- and Q-channel has its own DCLKI and DCLKQ, respectively. The DCLK output is always active, unless that channel is powered-down or the DCLK Reset feature is used while the device is in Demux Mode. As the supply to the ADC12D1600 ramps, the DCLK also comes up, see this example from the ADC12D1600QML RB: Figure 46. While the supply is too low, there is no output at DCLK. As the supply continues to ramp, DCLK functions intermittently with irregular frequency, but the amplitude continues to track with the supply. Much below the low end of operating supply range of the ADC12D1600, the DCLK is already fully operational.

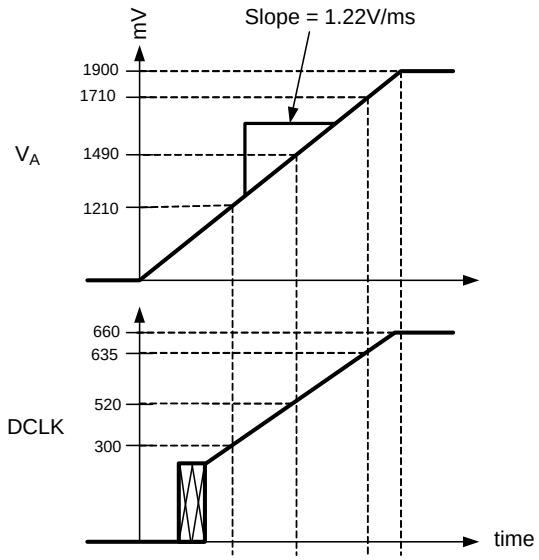


Figure 46. Supply and DCLK Ramping

THE ANALOG INPUTS

The ADC12D1600 will continuously convert any signal which is present at the analog inputs, as long as a CLK signal is also provided to the device. This section covers important aspects related to the analog inputs including: acquiring the input, driving the ADC in DES Mode, the reference voltage and FSR, out-of-range indication, AC/DC-coupled signals, and single-ended input signals.

Acquiring the Input

The Aperture Delay, t_{AD}, is the amount of delay, measured from the sampling edge of the clock input, after which signal present at the input pin is sampled inside the device. Data is acquired at the rising edge of CLK+ in Non-DES Mode and both the falling and rising edges of CLK+ in DES Mode. In Non-DES Mode, the I- and Q-channels always sample data on the rising edge of CLK+. In DES Mode, i.e. DESI, DESQ, DESIQ, and DESCLKIQ, the I-channel samples data on the rising edge of CLK+ and the Q-channel samples data on the falling edge of CLK+. The digital equivalent of that data is available at the digital outputs a constant number of sampling clock cycles later for the DI, DQ, DId and DQd output buses, a.k.a. Latency, depending on the demultiplex mode which is selected. In addition to the Latency, there is a constant output delay, t_{OD}, before the data is available at the outputs. See t_{OD} in the Timing Diagrams. See t_{LAT}, t_{AD}, and t_{OD}in Converter Electrical Characteristics – AC Electrical Characteristics.

Driving the ADC in DES Mode

The ADC12D1600 can be configured as either a 2-channel, 1600/1000 GSPS device (Non-DES Mode) or a 1-channel 3.2/2.0 GSPS device (DES Mode). When the device is configured in DES Mode, there is a choice for with which input to drive the single-channel ADC. These are the 3 options:

DES – externally driving the I-channel input only. This is the default selection when the ADC is configured in DES Mode. It may also be referred to as “DESI” for added clarity.

DESQ – externally driving the Q-channel input only.

DESIQ, DESCLKIQ – externally driving both the I- and Q-channel inputs. VinI+ and VinQ+ should be driven with the exact same signal. VinI- and VinQ- should be driven with the exact same signal, which is the differential compliment to the one driving VinI+ and VinQ+.

The input impedance for each I- and Q-input is 100Ω differential (or 50Ω single-ended), so the trace to each VinI+, VinI-, VinQ+, and VinQ- should always be 50Ω single-ended. If a single I- or Q-input is being driven, then that input will present a 100Ω differential load. For example, if a 50Ω single-ended source is driving the ADC, then a 1:2 balun will transform the impedance to 100Ω differential. However, if the ADC is being driven in DESIQ Mode, then the 100Ω differential impedance from the I-input will appear in parallel with the Q-input for a composite load of 50Ω differential and a 1:1 balun would be appropriate. See Figure 47 for an example circuit driving the ADC in DESIQ Mode. A recommended part selection is using the Mini-Circuits TC1-1-13MA+ balun with Ccouple = 0.22µF.

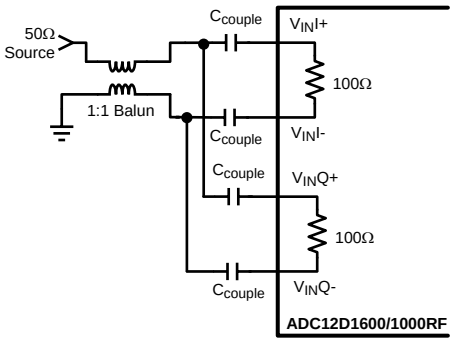


Figure 47. Driving DESIQ Mode

In the case that only one channel is used in Non-DES Mode or that the ADC is driven in DESI or DESQ Mode, the unused analog input should be terminated to reduce any noise coupling into the ADC. See Table 16 for details.

Table 16. Unused Analog Input Recommended Termination

Mode	Unused Channel	Recommended Termination
Non-DES	Powered Down	Tie Unused+ and Unused- to Vbg
DES/Non-DES	Not Powered Down	Tie Unused+ to Unused-

FSR and the Reference Voltage

The full-scale analog differential input range (V_{IN_FSR}) of the ADC12D1600 is derived from an internal bandgap reference. In Non-ECM, this full-scale range has two settings controlled by the FSR Pin; see Full-Scale Input Range Pin (FSR). The FSR Pin operates on both I- and Q-channels. In ECM, the full-scale range may be independently set for each channel via Addr:3**h** and B**h** with 15 bits of precision; see Register Definitions. The best SNR is obtained with a higher full-scale input range, but better distortion and SFDR are obtained with a lower full-scale input range. It is not possible to use an external analog reference voltage to modify the full-scale range, and this adjustment should only be done digitally, as described.

A buffered version of the internal bandgap reference voltage is made available at the V_{BG} Pin for the user. The V_{BG} pin can drive a load of up to 80 pF and source or sink up to 100 µA. It should be buffered if more current than this is required. This pin remains as a constant reference voltage regardless of what full-scale range is selected and may be used for a system reference. V_{BG} is a dual-purpose pin and it may also be used to select a higher LVDS output common-mode voltage; see LVDS Output Common-mode Pin (V_{BG}).

Out-Of-Range Indication

Differential input signals are digitized to 12 bits, based on the full-scale range. Signal excursions beyond the full-scale range, i.e. greater than $+V_{IN\_FSR}/2$ or less than $-V_{IN\_FSR}/2$, will be clipped at the output. An input signal which is above the FSR will result in all 1's at the output and an input signal which is below the FSR will result in all 0's at the output. When the conversion result is clipped for the I-channel input, the Out-of-Range I-channel (ORI) output is activated such that ORI+ goes high and ORI- goes low while the signal is out of range. This output is active as long as accurate data on either or both of the buses would be outside the range of 000**h** to FFF**h**. The Q-channel has a separate ORQ which functions similarly.

Maximum Input Range

The recommended operating and absolute maximum input range may be found in Absolute Maximum Ratings and Operating Ratings, respectively. Under the stated allowed operating conditions, each Vin+ and Vin- input pin may be operated in the range from 0V to 2.15V if the input is a continuous 100% duty cycle signal and from 0V to 2.5V if the input is a 10% duty cycle signal. The absolute maximum input range for Vin+ and Vin- is from -0.15V to 2.5V. These limits apply only for input signals for which the input common mode voltage is properly maintained.

AC-coupled Input Signals

The ADC12D1600 analog inputs require a precise common-mode voltage. This voltage is generated on-chip when AC-coupling Mode is selected. The analog inputs must be AC-coupled. For an ADC12D1600 used in a typical application, this may be accomplished by on-board capacitors, as shown in Figure 48.

Unused channels should be terminated as shown in Table 16. Do not connect an unused analog input directly to ground.

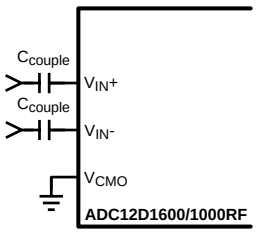


Figure 48. AC-coupled Differential Input

The analog inputs for the ADC12D1600 are internally buffered, which simplifies the task of driving these inputs and the RC pole which is generally used at sampling ADC inputs is not required. If the user desires to place an amplifier circuit before the ADC, care should be taken to choose an amplifier with adequate noise and distortion performance, and adequate gain at the frequencies used for the application.

Single-Ended Input Signals

The analog inputs of the ADC12D1600 are not designed to accept single-ended signals. The best way to handle single-ended signals is to first convert them to differential signals before presenting them to the ADC. The easiest way to accomplish single-ended to differential signal conversion is with an appropriate balun-transformer, as shown in Figure 49.

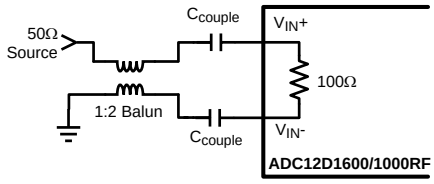


Figure 49. Single-Ended to Differential Conversion Using a Balun

When selecting a balun, it is important to understand the input architecture of the ADC. The impedance of the analog source should be matched to the ADC12D1600's on-chip 100Ω differential input termination resistor. The range of this termination resistor is specified as R_{IN} in Converter Electrical Characteristics – Analog Input/Output and Reference Characteristics.

THE CLOCK INPUTS

The ADC12D1600 has a differential clock input, CLK+ and CLK-, which must be driven with an AC-coupled, differential clock signal. This provides the level shifting necessary to allow for the clock to be driven with LVDS, PECL, LVPECL, or CML levels. The clock inputs are internally terminated to 100Ω differential and self-biased. This section covers coupling, frequency range, level, duty-cycle, jitter, and layout considerations.

CLK Coupling

The clock inputs of the ADC12D1600 must be capacitively coupled to the clock pins as indicated in Figure 50.

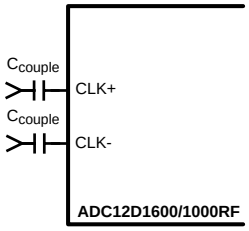


Figure 50. Differential Input Clock Connection

The choice of capacitor value will depend on the clock frequency, capacitor component characteristics and other system economic factors. For example, on the ADC12D1600QML RB, the capacitors have the value C_{couple} = 4.7 nF which yields a highpass cutoff frequency, f_c = 677.2 kHz.

CLK Frequency

Although the ADC12D1600 is tested and its performance is specified with a differential 1.6 GHz sampling clock, it will typically function well over the input clock frequency range; see f_{CLK}(min) and f_{CLK}(max) in Converter Electrical Characteristics – AC Electrical Characteristics. Operation up to f_{CLK}(max) is possible if the maximum ambient temperatures indicated are not exceeded. Operating at sample rates above f_{CLK}(max) for the maximum ambient temperature may result in reduced device reliability and product lifetime. This is due to the fact that higher sample rates results in higher power consumption and die temperatures. If in Non-LSPSM and f_{CLK} < 300 MHz, enable LFS in the Control Register (Addr: 0**h**, Bit 8). In LSPSM, this register bit is already enabled.

CLK Level

The input clock amplitude is specified as V_{IN_CLK} in Converter Electrical Characteristics – AC Electrical Characteristics. Input clock amplitudes above the max V_{IN_CLK} may result in increased input offset voltage. This would cause the converter to produce an output code other than the expected 2047/2048 when both input pins are at the same potential. Insufficient input clock levels will result in poor dynamic performance. Both of these results may be avoided by keeping the clock input amplitude within the specified limits of V_{IN_CLK}.

CLK Duty Cycle

The duty cycle of the input clock signal can affect the performance of any A/D converter. The ADC12D1600 features a duty cycle clock correction circuit which can maintain performance over the 20%-to-80% specified clock duty-cycle range. This feature is enabled by default and provides improved ADC clocking, especially in the Dual-Edge Sampling (DES) Mode.

CLK Jitter

High speed, high performance ADCs such as the ADC12D1600 require a very stable input clock signal with minimum phase noise or jitter. ADC jitter requirements are defined by the ADC resolution (number of bits), maximum ADC input frequency and the input signal amplitude relative to the ADC input full scale range. The maximum jitter (the sum of the jitter from all sources) allowed to prevent a jitter-induced reduction in SNR is found to be

$$t_{J(MAX)} = (V_{IN(P-P)}/ V_{FSR}) \times (1/(2^{(N+1)} \times \pi \times f_{IN})) \quad (3)$$

where

- $t_{J(MAX)}$ is the rms total of all jitter sources in seconds
- $V_{IN(P-P)}$ is the peak-to-peak analog input signal
- V_{FSR} is the full-scale range of the ADC
- "N" is the ADC resolution in bits
- f_{IN} is the maximum input frequency, in Hertz, at the ADC analog input

$t_{J(MAX)}$ is the square root of the sum of the squares (RSS) of the jitter from all sources, including: the ADC input clock, system, input signals and the ADC itself. Since the effective jitter added by the ADC is beyond user control, it is recommended to keep the sum of all other externally added jitter to a minimum.

CLK Layout

The ADC12D1600 clock input is internally terminated with a trimmed 100Ω resistor. The differential input clock line pair should have a characteristic impedance of 100Ω and (when using a balun), be terminated at the clock source in that (100Ω) characteristic impedance.

It is good practice to keep the ADC input clock line as short as possible, tightly coupled, keep it well away from any other signals, and treat it as a transmission line. Otherwise, other signals can introduce jitter into the input clock signal. Also, the clock signal can introduce noise into the analog path if it is not properly isolated.

THE LVDS OUTPUTS

The Data, ORI, ORQ, DCLKI and DCLKQ outputs are LVDS. The electrical specifications of the LVDS outputs are compatible with typical LVDS receivers available on ASIC and FPGA chips; but they are not IEEE or ANSI communications standards compliant due to the low +1.9V supply used on this chip. These outputs should be terminated with a 100Ω differential resistor placed as closely to the receiver as possible. If the 100Ω differential resistance is built in to the receiver, then an externally placed resistor is not necessary. This section covers common-mode and differential voltage, and data rate.

Common-mode and Differential Voltage

The LVDS outputs have selectable common-mode and differential voltage, V_{OS} and V_{OD}; see Converter Electrical Characteristics – Digital Control and Output Pin Characteristics. See Output Control and Adjust for more information.

Selecting the higher V_{OS} will also increase V_{OD} slightly. The differential voltage, V_{OD}, may be selected for the higher or lower value. For short LVDS lines and low noise systems, satisfactory performance may be realized with the lower V_{OD}. This will also result in lower power consumption. If the LVDS lines are long and/or the system in which the ADC12D1600 is used is noisy, it may be necessary to select the higher V_{OD}.

Output Data Rate

The data is produced at the output at the same rate it is sampled at the input. The minimum recommended input clock rate for this device is $f_{CLK(MIN)}$; see Converter Electrical Characteristics – AC Electrical Characteristics. However, it is possible to operate the device in 1:2 Demux Mode and capture data from just one 12-bit bus, e.g. just DI (or DId) although both DI and DId are fully operational. This will decimate the data by two and effectively halve the data rate.

Terminating Unused LVDS Output Pins

If the ADC is used in Non-Demux Mode, then only the DI and DQ data outputs will have valid data present on them. The DId and DQd data outputs may be left not connected; if unused, they are internally tri-stated.

Similarly, if the Q-channel is powered-down (i.e. PDQ is logic-high), the DQ data output pins, DCLKQ and ORQ may be left not connected.

SYNCHRONIZING MULTIPLE ADC12D1600S IN A SYSTEM

The ADC12D1600 has two features to assist the user with synchronizing multiple ADCs in a system; AutoSync and DCLK Reset. The AutoSync feature is new and designates one ADC12D1600 as the Master ADC and other ADC12D1600s in the system as Slave ADCs. The DCLK Reset feature performs the same function as the AutoSync feature, but is the first generation solution to synchronizing multiple ADCs in a system; it is disabled by default. For the application in which there are multiple Master and Slave ADC12D1600s in a system, AutoSync may be used to synchronize the Slave ADC12D1600(s) to each respective Master ADC12D1600 and the DCLK Reset may be used to synchronize the Master ADC12D1600s to each other.

If the AutoSync or DCLK Reset feature is not used, see Table 17 for recommendations about terminating unused pins.

Table 17. Unused AutoSync and DCLK Reset Pin Recommendation

Pin(s)	Unused termination
RCLK+/-	Do not connect.
RCOUT1+/-	Do not connect.
RCOUT2+/-	Do not connect.
DCLK_RST+	Connect to GND via 1kΩ resistor.
DCLK_RST-	Connect to V_A via 1kΩ resistor.

AutoSync Feature

AutoSync is a new feature which continuously synchronizes the outputs of multiple ADC12D1600s in a system. It may be used to synchronize the DCLK and data outputs of one or more Slave ADC12D1600s to one Master ADC12D1600. Several advantages of this feature include: no special synchronization pulse required, any upset in synchronization is recovered upon the next DCLK cycle, and the Master/Slave ADC12D1600s may be arranged as a binary tree so that any upset will quickly propagate out of the system.

An example system is shown below in Figure 51 which consists of one Master ADC and two Slave ADCs. For simplicity, only one DCLK is shown; in reality, there is DCLKI and DCLKQ, but they are always in phase with one another.

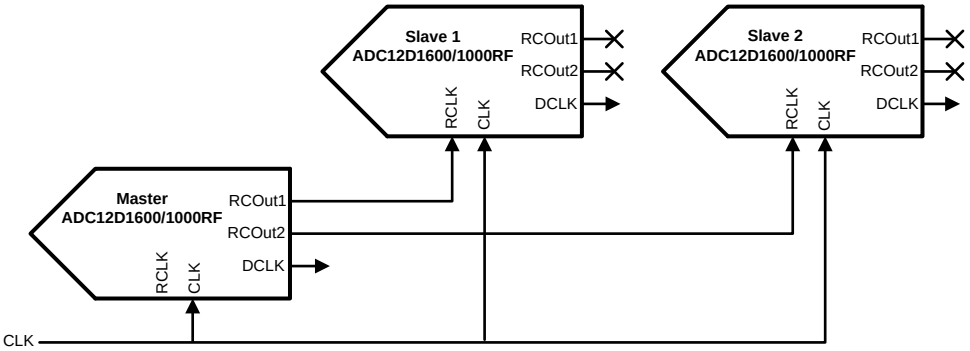


Figure 51. AutoSync Example

In order to synchronize the DCLK (and Data) outputs of multiple ADCs, the DCLKs must transition at the same time, as well as be in phase with one another. The DCLK at each ADC is generated from the CLK after some latency, plus t_{OD} minus t_{AD}. Therefore, in order for the DCLKs to transition at the same time, the CLK signal must reach each ADC at the same time. To tune out any differences in the CLK path to each ADC, the t_{AD} adjust feature may be used. However, using the t_{AD} adjust feature will also affect when the DCLK is produced at the output. If the device is in Demux Mode, then there are four possible phases which each DCLK may be generated on because the typical CLK = 1GHz and DCLK = 250 MHz for this case. The RCLK signal controls the phase of the DCLK, so that each Slave DCLK is on the same phase as the Master DCLK.

The AutoSync feature may only be used via the Control Registers. For more information, see AN-2132 (literature number SNAA073).

DCLK Reset Feature

The DCLK reset feature is available via ECM, but it is disabled by default. DCLKI and DCLKQ are always synchronized, by design, and do not require a pulse from DCLK_RST to become synchronized.

The DCLK_RST signal must observe certain timing requirements, which are shown in Figure 10 of the Timing Diagrams. The DCLK_RST pulse must be of a minimum width and its deassertion edge must observe setup and hold times with respect to the CLK input rising edge. These timing specifications are listed as t_{PWR}, t_{SR} and t_{HR} and may be found in Converter Electrical Characteristics – AC Electrical Characteristics.

The DCLK_RST signal can be asserted asynchronously to the input clock. If DCLK_RST is asserted, the DCLK output is held in a designated state (logic-high) in Demux Mode; in Non-Demux Mode, the DCLK continues to function normally. Depending upon when the DCLK_RST signal is asserted, there may be a narrow pulse on the DCLK line during this reset event. When the DCLK_RST signal is de-asserted, there are t_{SYNC_DLY} CLK cycles of systematic delay and the next CLK rising edge synchronizes the DCLK output with those of other ADC12D1600s in the system. For 90° Mode (DDRPh = logic-high), the synchronizing edge occurs on the rising edge of CLK, 4 cycles after the first rising edge of CLK after DCLK_RST is released. For 0° Mode (DDRPh = logic-low), this is 5 cycles instead. The DCLK output is enabled again after a constant delay of t_{OD}.

For both Demux and Non-Demux Modes, there is some uncertainty about how DCLK comes out of the reset state for the first DCLK_RST pulse. For the second (and subsequent) DCLK_RST pulses, the DCLK will come out of the reset state in a known way. Therefore, if using the DCLK Reset feature, it is recommended to apply one "dummy" DCLK_RST pulse before using the second DCLK_RST pulse to synchronize the outputs. This recommendation applies each time the device or channel is powered-on.

When using DCLK_RST to synchronize multiple ADC12D1600s, it is required that the Select Phase bits in the Control Register (Addr: E**h**, Bits 3,4) be the same for each Master ADC12D1600.

Temperature Sensor

The ADC12D1600 has an on-die temperature diode connected to pins Tdiode+/- which may be used to monitor the die temperature. In the following typical application, the LM95213 is used to monitor the temperature of an ADC12D1600 as well as an FPGA, see Figure 52. If this feature is unused, the Tdiode+/- pins may be left floating.

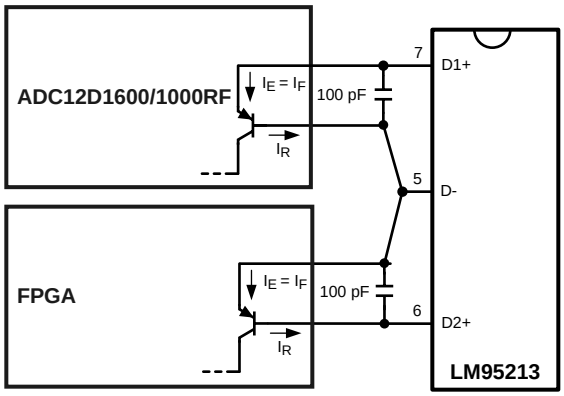


Figure 52. Typical Temperature Sensor Application

SUPPLY/GROUNDING, LAYOUT AND THERMAL RECOMMENDATIONS

Power Planes

All supply buses for the ADC should be sourced from a common linear voltage regulator. This ensures that all power buses to the ADC are turned on and off simultaneously. This single source will be split into individual sections of the power plane, with individual decoupling and connection to the different power supply buses of the ADC. Due to the low voltage but relatively high supply current requirement, the optimal solution may be to use a switching regulator to provide an intermediate low voltage, which is then regulated down to the final ADC supply voltage by a linear regulator. Please refer to the documentation provided for the ADC12D1600QML RB for additional details on specific regulators that are recommended for this configuration.

Power for the ADC should be provided through a broad plane which is located on one layer adjacent to the ground plane(s). Placing the power and ground planes on adjacent layers will provide low impedance decoupling of the ADC supplies, especially at higher frequencies. The output of a linear regulator should feed into the power plane through a low impedance multi-via connection. The power plane should be split into individual power peninsulas near the ADC. Each peninsula should feed a particular power bus on the ADC, with decoupling for that power bus connecting the peninsula to the ground plane near each power/ground pin pair. Using this technique can be difficult on many printed circuit CAD tools. To work around this, zero ohm resistors can be used to connect the power source net to the individual nets for the different ADC power buses. As a final step, the zero ohm resistors can be removed and the plane and peninsulas can be connected manually after all other error checking is completed.

Bypass Capacitors

The general recommendation is to have one 100nF capacitor for each power/ground pin pair. The capacitors should be surface mount multi-layer ceramic chip capacitors similar to Panasonic part number ECJ-0EB1A104K.

Ground Planes

Grounding should be done using continuous full ground planes to minimize the impedance for all ground return paths, and provide the shortest possible image/return path for all signal traces.

Power System Example

The ADC12D1600QML RB uses continuous ground planes (except where clear areas are needed to provide appropriate impedance management for specific signals), see Figure 53. Power is provided on one plane, with the 1.9V ADC supply being split into multiple zones or peninsulas for the specific power buses of the ADC. Decoupling capacitors are connected between these power bus peninsulas and the adjacent ground planes using vias. The capacitors are located as close to the individual power/ground pin pairs of the ADC as possible. In most cases, this means the capacitors are located on the opposite side of the PCB to the ADC.

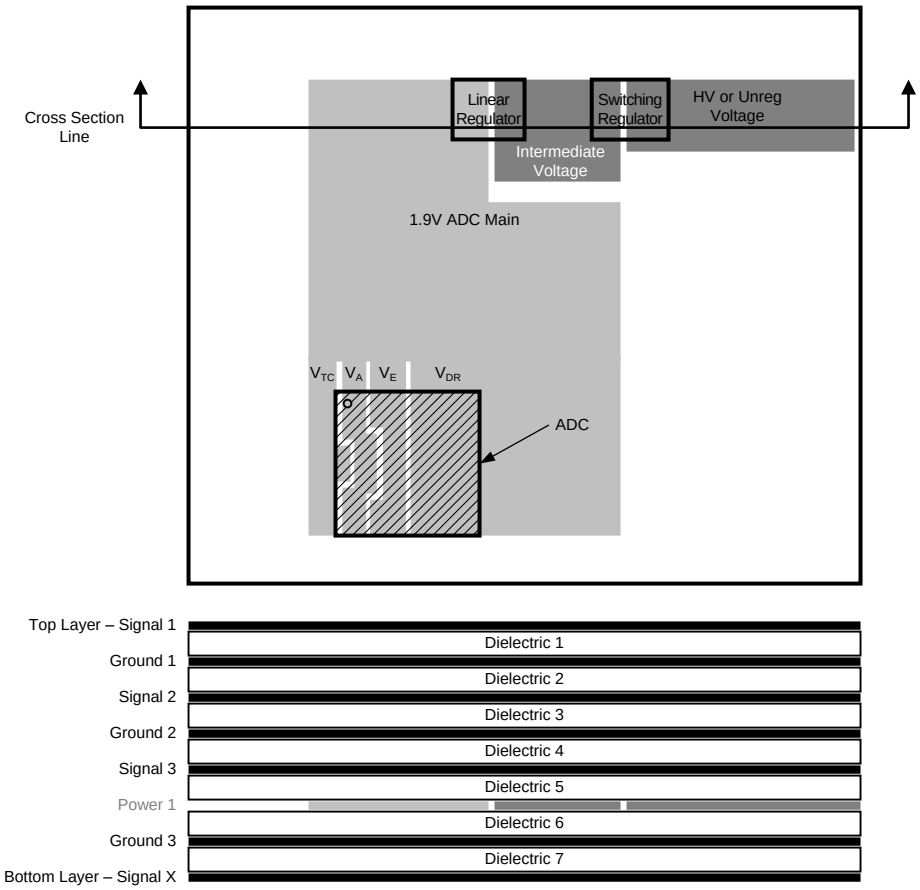


Figure 53. Power and Grounding Example

Thermal Management

The CPGA package is a modified Ceramic Land Grid Array with an added heat sink. The signal pins on the outer edge are 1.27mm pitch, while the pins in the center attached to the heat sink are 1mm. The smaller pitch for the center pins is to improve the thermal resistance. The center pins of the package are attached to the back of the die through a heat sink. Connecting these pins to the PCB ground planes with a low thermal resistance path is the best way to remove heat from the ADC. These pins should also be connected to the ground planes through low impedance path for electrical purposes.

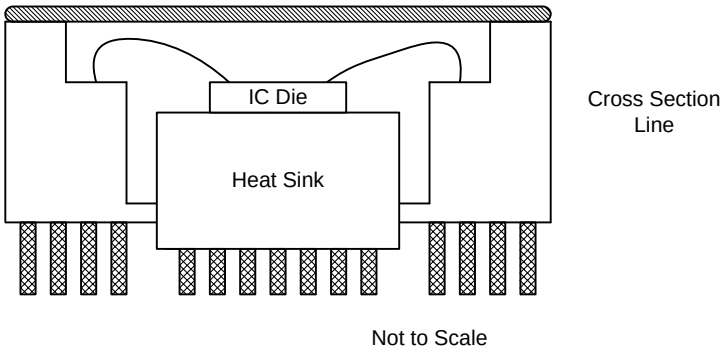


Figure 54. CPGA Conceptual Drawing

BOARD MOUNTING RECOMMENDATION

Proper thermal profile is required to establish re-flow under the package and ensure all joints meet profile specifications.

Table 18. Solder Profile Specification

Range Up °C/sec	≤ 4°C/sec
Peak Temp (Tpk) °C	210°C ≤Tpk ≤ 215°C
Max Peak Temp °C	≤ 220°C
Ramp down °C/sec	≤ 5°C/sec

The 220°C peak temperature is driven by the requirement to limit the dissolution of lead from the high-melt pin to the eutectic solder. To much lead increases the effective melting point of the board side joint and makes it much more difficult to remove the part if module rework is required.

Cool down rates and methods affect CPGA assemble yield and reliability. Picking up boards or opening the oven while solder joints are in molten state can disturb the solder joint. Boards should not be picked up until the solder joints have fully solidified. Board warping may potentially cause CPGA lifting off pads during cooling and this condition can also cause pin cracking when severe. This warping is a result of a high differential cooling rate between the top and bottom of the board. Both conditions can be prevented by using even top and bottom cooling.

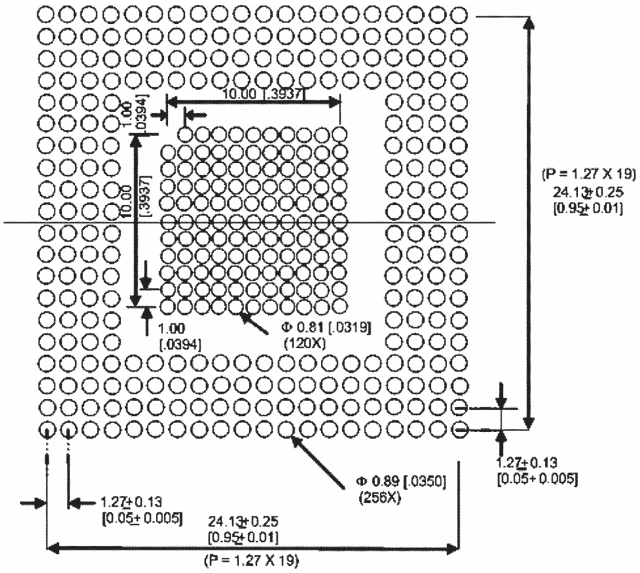


Figure 55. Landing Pattern Recommendation

RADIATION ENVIRONMENTS

Careful consideration should be given to environmental conditions when using a product in a radiation environment.

Total Ionizing Dose

Radiation hardness assured (RHA) products are those part numbers with a total ionizing dose (TID) level specified in the Ordering Information. Testing and qualification of these products is done on a wafer level according to MIL-STD-883, Test Method 1019. Wafer level TID data are available with lot shipments.

Single Event Latch-Up and Functional Interrupt

One time single event latch-up (SEL) and single event functional interrupt (SEFI) testing was preformed according to EIA/JEDEC Standard, EIA/JEDEC57. The linear energy transfer threshold (LETth) shown in the Key Specifications table is the maximum LET tested. A test report is available upon request.

Single Event Upset

A report on single event upset (SEU) is available upon request.

Register Definitions

Eleven read/write registers provide several control and configuration options in the Extended Control Mode. When the device is in Non-extended Control Mode (Non-ECM), the registers have the settings shown in the "**Default**" rows and cannot be changed. See Table 19 for a summary.

Table 19. Register Addresses

A3	A2	A1	A0	Hex	Register Addressed
0	0	0	0	0**h**	Configuration Register 1
0	0	0	1	1**h**	Reserved
0	0	1	0	2**h**	I-channel Offset Adjust
0	0	1	1	3**h**	I-channel Full-Scale Range Adjust
0	1	0	0	4**h**	Calibration Adjust
0	1	0	1	5**h**	Calibration Values
0	1	1	0	6**h**	Reserved
0	1	1	1	7**h**	DES Timing Adjust
1	0	0	0	8**h**	Reserved
1	0	0	1	9**h**	Reserved
1	0	1	0	A**h**	Q-channel Offset Adjust
1	0	1	1	B**h**	Q-channel Full-Scale Range Adjust
1	1	0	0	C**h**	Aperture Delay Coarse Adjust
1	1	0	1	D**h**	Aperture Delay Fine Adjust
1	1	1	0	E**h**	AutoSync
1	1	1	1	F**h**	Reserved

Table 20. Configuration Register 1

Addr: 0**h** (0000**b**)									POR state: 2000**h**							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CAL	DPS	OVS	TPM	PDI	PDQ	Res	LFS	DES	DEQ	DIQ	2SC	TSE	SDR	Res	
Default	0	0	1	0	0	0	0	0/1	0	0	0	0	0	0	0	0

Bit 15	CAL: Calibration Enable. When this bit is set to 1**b**, an on-command calibration is initiated. This bit is not reset automatically upon completion of the calibration. Therefore, the user must reset this bit to 0**b** and then set it to 1**b** again to execute another calibration. This bit is logically OR'd with the CAL Pin; both bit and pin must be set to 0**b** before either is used to execute a calibration.
Bit 14	DPS: DCLK Phase Select. In DDR, set this bit to 0**b** to select the 0° Mode DDR Data-to-DCLK phase relationship and to 1**b** to select the 90° Mode. In SDR, set this bit to 0**b** to transition the data on the Rising edge of DCLK; set this bit to 1**b** to transition the data on the Falling edge of DCLK. (1)
Bit 13	OVS: Output Voltage Select. This bit sets the differential voltage level for the LVDS outputs including Data, OR, and DCLK. 0**b** selects the lower level and 1**b** selects the higher level. See V_{OD} in Converter Electrical Characteristics – Digital Control and Output Pin Characteristics for details.
Bit 12	TPM: Test Pattern Mode. When this bit is set to 1**b**, the device will continually output a fixed digital pattern at the digital Data and OR outputs. When set to 0**b**, the device will continually output the converted signal, which was present at the analog inputs. See Test Pattern Mode for details about the TPM pattern.
Bit 11	PDI: Power-down I-channel. When this bit is set to 0**b**, the I-channel is fully operational; when it is set to 1**b**, the I-channel is powered-down. The I-channel may be powered-down via this bit or the PDI Pin, which is active, even in ECM.
Bit 10	PDQ: Power-down Q-channel. When this bit is set to 0**b**, the Q-channel is fully operational; when it is set to 1**b**, the Q-channel is powered-down. The Q-channel may be powered-down via this bit or the PDQ Pin, which is active, even in ECM.
Bit 9	Reserved. Must be set as shown.

(1) This functionality is not tested in the production program; performance is tested in the default/specified mode only.

Bit 8	LFS: Low-Frequency Select. If the sampling clock (CLK) is at or below 300 MHz in Non-LSPSM, set this bit to 1**b** for improved performance. In LSPSM, the part is automatically in LFS and this bit is inactive.		
Bit 7	DES: Dual-Edge Sampling Mode select. When this bit is set to 0**b**, the device will operate in the Non-DES Mode; when it is set to 1**b**, the device will operate in the DES Mode. See DES/Non-DES Mode for more information.		
Bit 6	DEQ: DES Q-input select, a.k.a. DESQ Mode. When the device is in DES Mode, this bit selects the input that the device will operate on. The default setting of 0**b** selects the I-input and 1**b** selects the Q-input.		
Bit 5	DIQ: DES I- and Q-input, a.k.a. DESIQ Mode. When in DES Mode, setting this bit to 1**b** shorts the I- and Q-inputs internally to the device. If the bit is left at its default 0**b**, the I- and Q-inputs remain electrically separate. In this mode, both the I- and Q-inputs must be externally driven; see DES/Non-DES Mode for more information. The allowed DES Modes settings are shown below. For DESCLKIQ Mode, see Addr E**h**.		
	Mode	Addr 0**h**, Bit<7:5>	Addr E**h**, Bit<6>
	Non-DES Mode	000**b**	0**b**
	DESI Mode	100**b**	0**b**
	DESQ Mode	110**b**	0**b**
	DESIQ Mode	101**b**	0**b**
	DESCLKIQ Mode	000**b**	1**b**
Bit 4	2SC: Two's Complement output. For the default setting of 0**b**, the data is output in Offset Binary format; when set to 1**b**, the data is output in Two's Complement format.		
Bit 3	TSE: Time Stamp Enable. For the default setting of 0**b**, the Time Stamp feature is not enabled; when set to 1**b**, the feature is enabled. See Output Control and Adjust for more information about this feature.		
Bit 2	SDR: Single Data Rate. For the default setting of 0**b**, the data is clocked in Dual Data Rate; when set to 1**b**, the data is clocked in Single Data Rate. See Output Control and Adjust for more information about this feature. Note that for DDR Mode, the 1:2 Demux Mode is not available. See Table 10 for a selection of available modes.		
Bits 1:0	Reserved. Must be set as shown.		

Table 21. Reserved

Addr: 1**h** (0001**b**)									POR state: 2907**h**							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res															
Default	0	0	1	0	1	0	0	1	0	0	0	0	0	1	1	1

Bits 15:0	Reserved. Must be set as shown.

Table 22. I-channel Offset Adjust

Addr: 2**h** (0010**b**)									POR state: 0000**h**							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res			OS	OM(11:0)											
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 15:13	Reserved. Must be set to 0**b**.	
Bit 12	OS: Offset Sign. The default setting of 0**b** incurs a positive offset of a magnitude set by Bits 11:0 to the ADC output. Setting this bet to 1**b** incurs a negative offset of the set magnitude.	
Bits 11:0	OM(11:0): Offset Magnitude. These bits determine the magnitude of the offset set at the ADC output (straight binary coding). The range is from 0 mV for OM(11:0) = 0**d** to 45 mV for OM(11:0) = 4095**d** in steps of ~11 µV. Monotonicity is specified by design only for the 9 MSBs.	
	Code	**Offset [mV]**
	0000 0000 0000 (default)	0
	1000 0000 0000	22.5
	1111 1111 1111	45

Table 23. I-channel Full Scale Range Adjust

Addr: 3**h** (0011**b**)																POR state: 4000**h**
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res	FM(14:0)														
Default	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit 15	Reserved. Must be set to 0**b**.	
Bits 14:0	FM(14:0): FSR Magnitude. These bits increase the ADC full-scale range magnitude (straight binary coding.) The range is from 600 mV (0**d**) to 1000 mV (32767**d**) with the default setting at 800 mV (16384**d**). Monotonicity is specified by design only for the 9 MSBs. The mid-range (low) setting in ECM corresponds to the nominal (low) setting in Non-ECM. A greater range of FSR values is available in ECM, i.e. FSR values above 800 mV. See V_{IN_FSR} in Converter Electrical Characteristics – Analog Input/Output and Reference Characteristics for characterization details.	
	Code	**FSR [mV]**
	000 0000 0000 0000	600
	100 0000 0000 0000 (default)	800
	111 1111 1111 1111	1000

Table 24. Calibration Adjust(1)

Addr: 4**h** (0100**b**)																POR state: DB4B**h**
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res	CSS	Res						SSC	Res						
Default	1	1	0	1	1	0	1	1	0	1	0	0	1	0	1	1

(1) This functionality is not tested in the production program; performance is tested in the default/specified mode only.

Bit 15	Reserved. Must be set as shown.
Bit 14	CSS: Calibration Sequence Select. The default 1**b** selects the following calibration sequence: reset all previously calibrated elements to nominal values, do R_{IN} Calibration, do internal linearity Calibration. Setting CSS = 0**b** selects the following calibration sequence: do not reset R_{IN} to its nominal value, skip R_{IN} calibration, do internal linearity Calibration. The calibration must be completed at least one time with CSS = 1**b** to calibrate R_{IN}. Subsequent calibrations may be run with CSS = 0**b** (skip R_{IN} calibration) or 1**b** (full R_{IN} and internal linearity Calibration).
Bits 13:8	Reserved. Must be set as shown.
Bit 7	SSC: SPI Scan Control. Setting this control bit to 1**b** allows the calibration values, stored in Addr: 5**h**, to be read/written. When not reading/writing the calibration values, this control bit should left at its default 0**b** setting. See Calibration Feature for more information.
Bits 6:0	Reserved. Must be set as shown.

Table 25. Calibration Values(1)

Addr: 5**h** (0101**b**)																POR state: XXXX**h**
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SS(15:0)															
Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

(1) This functionality is not tested in the production program; performance is tested in the default/specified mode only.

Bits 15:0	SS(15:0): SPI Scan. When the ADC performs a self-calibration, the values for the calibration are stored in this register and may be read from/ written to it. Set SSC (Addr: 4**h**, Bit 7) to read/write. See Calibration Feature for more information.

Table 26. Reserved

Addr: 6**h** (0110**b**)																POR state: 1C2E**h**
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res															
Default	0	0	0	1	1	1	0	0	0	0	1	0	1	1	1	0

Bits 15:0	Reserved. Must be set as shown.

Table 27. DES Timing Adjust(1)

Addr: 7**h** (0111**b**)																POR state: 8142**h**
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DTA(6:0)							Res								
Default	1	0	0	0	0	0	0	1	0	1	0	0	0	0	1	0

(1) This functionality is not tested in the production program; performance is tested in the default/specified mode only.

Bits 15:9	DTA(6:0): DES Mode Timing Adjust. In the DES Mode, the time at which the falling edge sampling clock samples relative to the rising edge of the sampling clock may be adjusted; the automatic duty cycle correction continues to function. See Input Control and Adjust for more information. The nominal step size is 30fs.
Bits 8:0	Reserved. Must be set as shown.

Table 28. Reserved

Addr: 8**h** (1000**b**)																POR state: 0F0F**h**
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res															
Default	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1

Bits 15:0	Reserved. Must be set as shown.

Table 29. Reserved

Addr: 9**h** (1001**b**)																POR state: 0000**h**
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 15:0	Reserved. Must be set as shown.

Table 30. Q-channel Offset Adjust

Addr: A**h** (1010**b**)																POR state: 0000**h**
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res			OS	OM(11:0)											
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 15:13	Reserved. Must be set to 0**b**.	
Bit 12	OS: Offset Sign. The default setting of 0**b** incurs a positive offset of a magnitude set by Bits 11:0 to the ADC output. Setting this bet to 1**b** incurs a negative offset of the set magnitude.	
Bits 11:0	OM(11:0): Offset Magnitude. These bits determine the magnitude of the offset set at the ADC output (straight binary coding). The range is from 0 mV for OM(11:0) = 0**d** to 45 mV for OM(11:0) = 4095**d** in steps of ~11 µV. Monotonicity is specified by design only for the 9 MSBs.	
	Code	**Offset [mV]**
	0000 0000 0000 (default)	0
	1000 0000 0000	22.5
	1111 1111 1111	45

Table 31. Q-channel Full-Scale Range Adjust

Addr: B**h** (1011**b**)																POR state: 4000**h**
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res	FM(14:0)														
Default	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit 15	Reserved. Must be set to 0**b**.	
Bits 14:0	FM(14:0): FSR Magnitude. These bits increase the ADC full-scale range magnitude (straight binary coding.) The range is from 600 mV (0**d**) to 1000 mV (32767**d**) with the default setting at 800 mV (16384**d**). Monotonicity is specified by design only for the 9 MSBs. The mid-range (low) setting in ECM corresponds to the nominal (low) setting in Non-ECM. A greater range of FSR values is available in ECM, i.e. FSR values above 800 mV. See V_{IN_FSR} in Converter Electrical Characteristics – Analog Input/Output and Reference Characteristics for characterization details.	
	Code	**FSR [mV]**
	000 0000 0000 0000	600
	100 0000 0000 0000 (default)	800
	111 1111 1111 1111	1000

Table 32. Aperture Delay Coarse Adjust

Addr: C**h** (1100**b**)																POR state: 0004**h**
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CAM(11:0)												STA	DCC	Res	
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits 15:4	CAM(11:0): Coarse Adjust Magnitude. This 12-bit value determines the amount of delay that will be applied to the input CLK signal. The range is 0 ps delay for CAM(11:0) = 0**d** to a maximum delay of 825 ps for CAM(11:0) = 2431**d** (±95 ps due to PVT variation) in steps of ~340 fs. For code CAM(11:0) = 2432**d** and above, the delay saturates and the maximum delay applies. Additional, finer delay steps are available in register D**h**. The STA (Bit 3) must be selected to enable this function.
Bit 3	STA: Select t_{AD} Adjust. Set this bit to 1**b** to enable the t_{AD} adjust feature, which will make both coarse and fine adjustment settings, i.e. CAM(11:0) and FAM(5:0), available.
Bit 2	DCC: Duty Cycle Correct. This bit can be set to 0**b** to disable the automatic duty-cycle stabilizer feature of the chip. This feature is enabled by default.
Bits 1:0	Reserved. Must be set to 0**b**.

Table 33. Aperture Delay Fine Adjust

Addr: D**h** (1101**b**)									POR state: 0000**h**							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FAM(5:0)						Res		Res							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 15:10	FAM(5:0): Fine Aperture Adjust Magnitude. This 6-bit value determines the amount of additional delay that will be applied to the input CLK when the Clock Phase Adjust feature is enabled via STA (Addr: C**h**, Bit 3). The range is straight binary from 0 ps delay for FAM(5:0) = 0**d** to 2.3 ps delay for FAM(5:0) = 63**d** (±300 fs due to PVT variation) in steps of ~36 fs.
Bits 9:0	Reserved. Must be set as shown.

Table 34. AutoSync(1)

Addr: E**h** (1110**b**)									POR state: 0003**h**							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DRC(8:0)								DCK	Res	SP(1:0)			ES	DOC	DR
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

(1) This functionality is not tested in the production program; performance is tested in the default/specified mode only.

Bits 15:7	DRC(8:0): Delay Reference Clock (8:0). These bits may be used to increase the delay on the input reference clock when synchronizing multiple ADCs. The delay may be set from a minimum of 0s (0**d**) to a maximum of 1200 ps (319**d**). The delay remains the maximum of 1200 ps for any codes above or equal to 319**d**. See SYNCHRONIZING MULTIPLE ADC12D1600S IN A SYSTEM for more information.
Bit 6	DCK: DESCLKIQ Mode. Set this bit to 1**b** to enable Dual-Edge Sampling, in which the Sampling Clock samples the I- and Q-channels 180º out of phase with respect to one another, i.e. the DESCLKIQ Mode. To select the DESCLKIQ Mode, Addr: 0**h**, Bits <7:5> must also be set to 000**b**. See Input Control and Adjust for more information.
Bit 5	Reserved. Must be set as shown.
Bits 4:3	SP(1:0): Select Phase. These bits select the phase of the reference clock which is latched. The codes correspond to the following phase shift: 00 = 0° 01 = 90° 10 = 180° 11 = 270°
Bit 2	ES: Enable Slave. Set this bit to 1**b** to enable the Slave Mode of operation. In this mode, the internal divided clocks are synchronized with the reference clock coming from the master ADC. The master clock is applied on the input pins RCLK. If this bit is set to 0**b**, then the device is in Master Mode.
Bit 1	DOC: Disable Output reference Clocks. Setting this bit to 0**b** sends a CLK/4 signal on RCOut1 and RCOut2. The default setting of 1**b** disables these output drivers. This bit functions as described, regardless of whether the device is operating in Master or Slave Mode, as determined by ES (Bit 2).
Bit 0	DR: Disable Reset. The default setting of 1**b** leaves the DCLK_RST functionality disabled. Set this bit to 0**b** to enable DCLK_RST functionality.

Table 35. Reserved

Addr: F**h** (1111**b**)									POR state: 001D**h**							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res															
Default	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1

Bits 15:0	Reserved. This address is read only.

Engineering Samples

Engineering samples are available for order and are identified by the "MPR" in the orderable device name (see Packaging Information in the Addendum). Engineering (MPR) samples meet the performance specifications of the datasheet at room temperature only and have not received the full space production flow or testing. Engineering samples may be QCI rejects that failed tests that would not impact the performance at room temperature, such as radiation or reliability testing.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADC12D1600CCMLS	Active	Production	CCGA (NAA) | 376	1 | EIAJ TRAY (10+1)	No	Call TI	Call TI	-55 to 125	ADC12D1600CC MLS
ADC12D1600CCMPR	Active	Production	CCGA (NAA) | 376	36 | EIAJ TRAY (10+1)	No	Call TI	Call TI	25 to 25	ADC12D1600CC MPR E.S.
ADC12D1600CCMPR.A	Active	Production	CCGA (NAA) | 376	36 | EIAJ TRAY (10+1)	No	Call TI	Call TI	25 to 25	ADC12D1600CC MPR E.S.

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

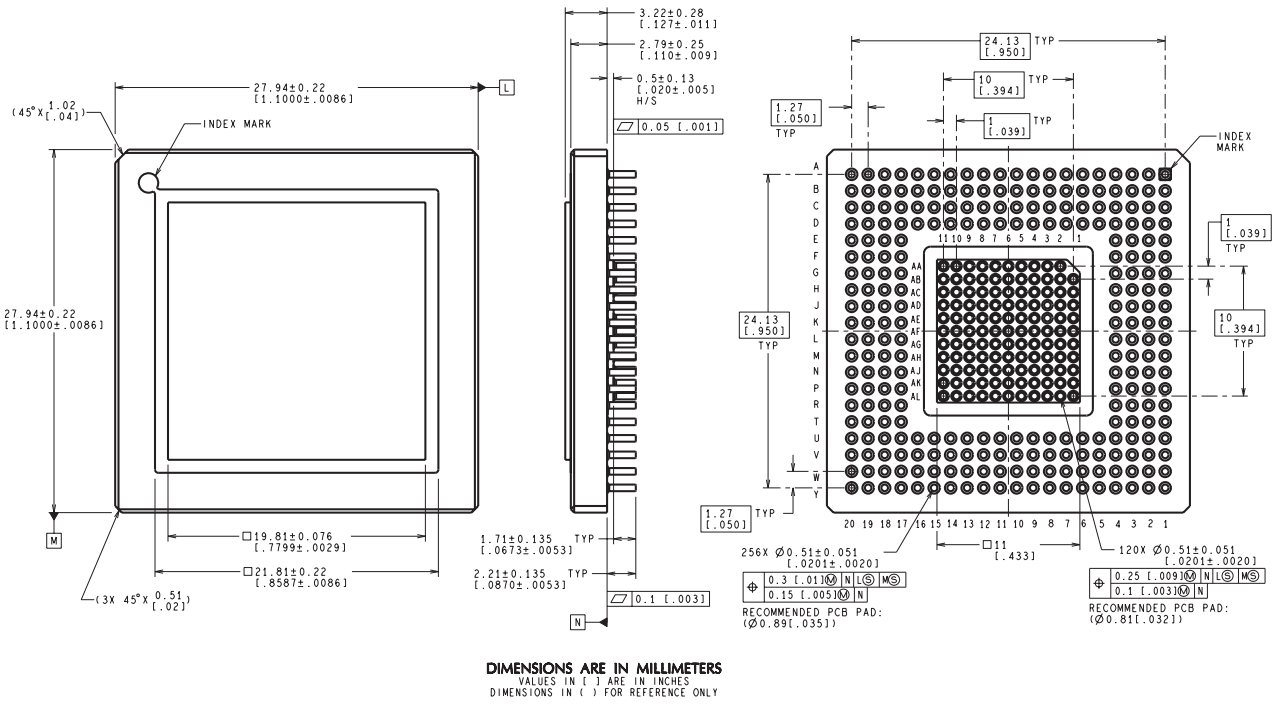
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

NAA0376A



DIMENSIONS ARE IN MILLIMETERS
VALUES IN [ ] ARE IN INCHES
DIMENSIONS IN ( ) FOR REFERENCE ONLY

CCC376A (Rev D)

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025