ADS1x2S14 Low-power, 16- and 24-Bit, 8-Channel, 64kSPS, Delta-Sigma ADC with PGA, Voltage Reference, and SPI

1 Features

- Low power consumption (as low a 57µA)
- Wide supply voltage range:
  - Analog: 1.74V to 3.6V
  - Digital: 1.65V to 3.6V
- Programmable gain: 0.5 to 256
- Programmable data rate (up to 64kSPS) and speed mode to trade power consumption and noise performance
- Simultaneous 50Hz and 60Hz rejection at 20 or 25SPS with single-cycle settling digital filter
- Analog multiplexer with 8 independently selectable inputs
- Dual-matched programmable current sources
- Internal programmable voltage reference: 1.25V or 2.5V with 25ppm/°C (max) drift
- Internal 1% (max) accurate oscillator
- Internal temperature sensor
- Four general-purpose I/Os (push-pull or open-drain output)
- SPI-compatible interface with optional CRC and daisy-chain capability

2 Applications

- Field transmitters:
  Temperature, pressure, strain, flow
- PLC and DCS analog input modules
- Temperature controllers
- Patient monitoring systems:
  Body temperature, blood pressure

3 Description

The ADS1x2S14 are precision, low-power, 16- and 24-bit, analog-to-digital converters (ADCs) that offer many integrated features to reduce system cost and component count in the most common sensor measurement applications. The devices feature eight analog inputs through a flexible input multiplexer (MUX), a low-noise, programmable gain amplifier (PGA), a programmable low-drift voltage reference, two programmable excitation current sources, an oscillator, and a temperature sensor.

Four speed modes, with programmable output data rates from 20SPS up to 64kSPS, allow to optimize power consumption and noise performance for each application. At output data rates of 20SPS and 25SPS, the integrated digital filter offers simultaneous 50Hz and 60Hz line-cycle rejection with single-cycle settling.

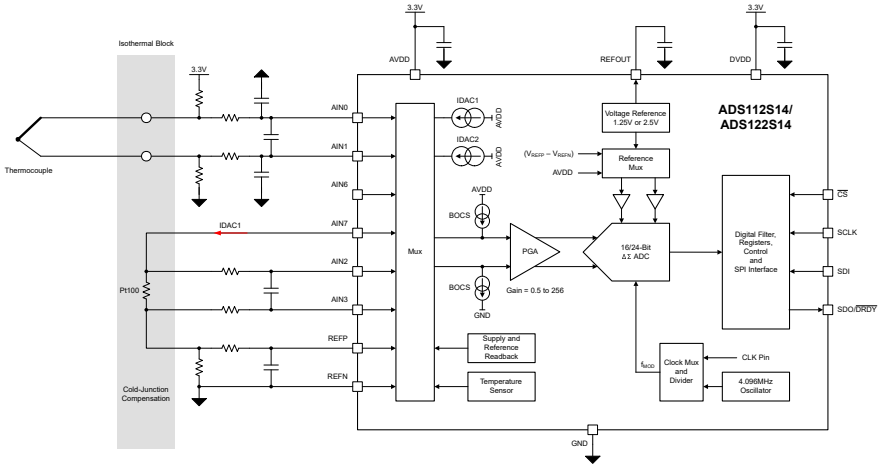
Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
ADS1x2S14	RTE (WQFN, 16)	3.00mm × 3.00mm
	YBH (DSBGA, 16)	1.87mm × 1.97mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value.

Table 3-1. Device Information

PART NUMBER	RESOLUTION	ANALOG INPUTS
ADS112S14	16 Bit	8
ADS122S14	24 Bit	8



K-Type Thermocouple Measurement With Cold-Junction Compensation Using a 2-wire Pt100 RTD

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4 Pin Configuration and Functions

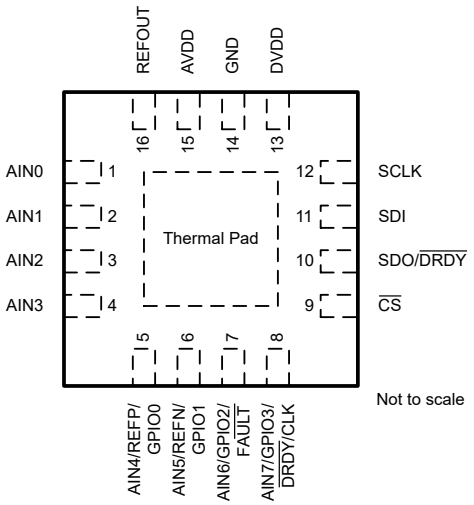


Figure 4-1. ADS1x2S14, RTE Package, 16-pin WQFN, Top View

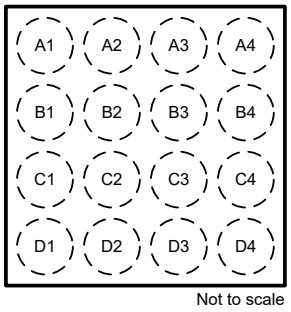


Figure 4-2. ADS1x2S14, YBH Package, 16-pin DSBGA, Top View

Table 4-1. ADS1x2S14 Pin Functions

PIN			TYPE	DESCRIPTION[1]
NAME	RTE	YBH		
AIN0	1	A4	Analog Input	Analog input 0
AIN1	2	B4	Analog Input	Analog input 1
AIN2	3	C4	Analog Input	Analog input 2
AIN3	4	D4	Analog Input	Analog input 3
AIN4/REFP/ GPIO0	5	B3	Analog Input/ Digital IO	Analog input 4. Positive external reference input. General purpose digital input/output 0.[2] [4]
AIN5/REFN/ GPIO1	6	C3	Analog Input/ Digital IO	Analog input 5. Negative external reference input. General purpose digital input/output 1.[2] [4]
AIN6/ GPIO2/$\overline{\text{FAULT}}$	7	D3	Analog Input/ Digital IO	Analog input 6. General purpose digital input/output 2.[2] [4] Pin can be configured as dedicated $\overline{\text{FAULT}}$ output.
AIN7/ GPIO3/$\overline{\text{DRDY}}$/CLK	8	D2	Analog Input/ Digital IO	Analog input 7. General purpose digital input/output 3.[2] [4] Pin can be configured as dedicated $\overline{\text{DRDY}}$ output or external clock input.
AVDD	15	A2	Analog Supply	Positive analog supply. Connect a 100nF capacitor to GND.
$\overline{\text{CS}}$	9	C2	Digital Input	Chip select input. Active low.[5]
DVDD	13	A1	Digital Supply	Digital supply. Connect a 100nF capacitor to GND.
GND	14	B2	Ground	Ground
REFOUT	16	A3	Analog Output	Internal voltage reference output. Connect a 100nF capacitor to GND.
SCLK	12	B1	Digital Input	Serial data clock input[5]
SDI	11	C1	Digital Input	Serial data input[5]
SDO/$\overline{\text{DRDY}}$	10	D1	Digital Output	Serial data output and data ready indication[3] [5]
Thermal Pad	-	N/A	-	Thermal power pad. Connect to GND.

(1) See the Unused Inputs and Outputs section for details on how to connect unused pins.
(2) Configurable as push-pull or open-drain output.
(3) Push-pull output.
(4) Logic levels referenced to AVDD.
(5) Logic levels referenced to DVDD.

5 Specifications

5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Power supply voltage	AVDD to GND	–0.3	5	V
	DVDD to GND	–0.3	5.5	V
Analog input voltage	AINx, REFP, REFN	GND – 0.3	AVDD + 0.3	V
Digital input voltage	GPIO0, GPIO1, GPIO2/$\overline{\text{FAULT}}$, GPIO3/$\overline{\text{DRDY}}$/CLK	GND – 0.3	AVDD + 0.3	V
Digital input voltage	$\overline{\text{CS}}$, SCLK, SDI, SDO/$\overline{\text{DRDY}}$	GND – 0.3	DVDD + 0.3	V
Input current	Continuous, any pin except power-supply pins	–10	10	mA
Temperature	Junction, T_J		140	°C
	Storage, T_{stg}	–60	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	±750	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
	Analog power supply	AVDD to GND, I_{IDAC} ≤ 500µA	1.74		3.6	V
		AVDD to GND, I_{IDAC} > 500µA or internal V_{REF} = 2.5V	2.7		3.6	
	Digital power supply	DVDD to GND	1.65		3.6	V
ANALOG INPUTS(1)						
V_{AINx}	Absolute input voltage	Gain = 0.5 to 10	GND		AVDD – 0.35	V
		Gain = 16 to 256	GND + 0.35		AVDD – 0.4	
V_{IN}	Differential input voltage(2)	Unipolar straight binary coding	0		V_{REF} / Gain	V
		Binary two's complement coding	$-V_{REF}$ / Gain		V_{REF} / Gain	
VOLTAGE REFERENCE INPUTS						
V_{REF}	Differential reference input voltage	$V_{REF} = (V_{REFP} - V_{REFN})$	0.5		AVDD	V
V_{REFN}	Absolute negative reference voltage	Negative reference buffer disabled	GND – 0.05			V
		Negative reference buffer enabled	GND + 0.1			V
V_{REFP}	Absolute positive reference voltage	Positive reference buffer disabled			AVDD + 0.05	V
		Positive reference buffer enabled			AVDD – 0.1	V
EXTERNAL CLOCK SOURCE(3)						
f_{CLK}	External clock frequency		3	4.096	4.15	MHz
	Duty Cycle		40%	50%	60%	
GENERAL-PURPOSE INPUTS (GPIOs)						
	Input voltage		GND		AVDD	V
DIGITAL INPUTS (other than GPIOs)						
	Input voltage		GND		DVDD	V
TEMPERATURE RANGE						
	Specified ambient temperature		–40		125	°C
T_A	Operating ambient temperature		–50		125	°C

(1) AIN_P and AIN_N denote the positive and negative inputs of the PGA. Any of the available analog inputs (AINx) can be selected as either AIN_P or AIN_N by the input multiplexer.
(2) $V_{IN} = (V_{AINP} - V_{AINN})$. Excluding the effects of offset and gain error.
(3) An external clock is not required when the internal oscillator is used.

5.4 Thermal Information

THERMAL METRIC(1)		WQFN (RTE) 16 PINS	DSBGA (YBH) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	59.3	86.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	40.2	0.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	31.6	22.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.8	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	31.5	22.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	27.2	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

minimum and maximum specifications apply from T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; all specifications are at AVDD = 1.74V to 3.6V, DVDD = 1.65V to 3.6V, internal reference, internal oscillator, all speed modes, all data rates, all gain settings, and global chop disabled (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
	Absolute input current[1]	All gains, f_{DATA} = 20SPS or 25SPS, global chop enabled or disabled, $V_{AINx(MIN)} \le V_{AINx} \le V_{AINx(MAX)}$, V_{IN} = 0V	–2	±0.3	2	nA
	Absolute input current drift[1]	All gains, f_{DATA} = 20SPS or 25SPS, global chop enabled or disabled, $V_{AINx(MIN)} \le V_{AINx} \le V_{AINx(MAX)}$, V_{IN} = 0V		2		pA/°C
	Differential input current[1]	All gains, f_{DATA} = 20SPS or 25SPS, global chop enabled or disabled, V_{CM} = AVDD/2, $-V_{REF}/Gain \le V_{IN} \le V_{REF}/Gain$	–2	±0.1	2	nA
	Differential input current drift[1]	All gains, f_{DATA} = 20SPS or 25SPS, global chop enabled or disabled, V_{CM} = AVDD/2, $-V_{REF}/Gain \le V_{IN} \le V_{REF}/Gain$		2		pA/°C
PGA						
	Gain settings			0.5, 1, 2, 4, 5, 8, 10, 16, 20, 32, 50, 64, 100, 128, 200, 256		
SYSTEM PERFORMANCE						
	Resolution (no missing codes)	ADS112S14	16			Bits
		ADS122S14	24			
f_{DATA}	Output data rate	Speed mode 0 (f_{MOD} = 32kHz)	20		2k	SPS
		Speed mode 1 (f_{MOD} = 256kHz)	20		16k	
		Speed mode 2 (f_{MOD} = 512kHz)	20		32k	
		Speed mode 3 (f_{MOD} = 1024kHz)	20		64k	
INL	Integral nonlinearity	V_{CM} = AVDD/2, best fit		5	15	ppm_{FSR}
V_{IO}	Input offset voltage	T_A = 25°C, gain = 0.5, global chop disabled	–250	±50	250	µV
		T_A = 25°C, gains = 1 to 10, global chop disabled	–150	±20	150	
		T_A = 25°C, gain ≥ 16, global chop disabled	–50	±10	50	
		T_A = 25°C, gain = 0.5, global chop enabled	–5	±0.5	5	
		T_A = 25°C, gain ≥ 1, global chop enabled	–2	±0.2	2	
	Offset drift	Gains ≤ 10, global chop disabled		60	300	nV/°C
		Gains ≥ 16, global chop disabled		20	125	
		All gains, global chop enabled		10	50	
	Gain error	T_A = 25°C, all gains, external reference	–0.3	±0.08	0.3	%
	Gain drift	All gains, external reference		0.5	2.5	ppm/°C
	Noise (input-referred)		See the *Noise Performance* section			
NMRR	Normal-mode rejection ratio	f_{IN} = 50Hz or 60Hz (±1Hz), f_{DATA} = 20SPS	82	95		dB
		f_{IN} = 50Hz or 60Hz (±1Hz), f_{DATA} = 20SPS, external f_{CLK} = 4.096MHz	95			
		f_{IN} = 50Hz or 60Hz (±1Hz), f_{DATA} = 25SPS	57	62		
		f_{IN} = 50Hz or 60Hz (±1Hz), f_{DATA} = 25SPS, external f_{CLK} = 4.096MHz	62			
CMRR	Common-mode rejection ratio	At dc		120		dB
		f_{CM} = 50Hz or 60Hz (±1Hz), f_{DATA} = 20SPS or 25SPS		130		
		f_{CM} = 50Hz or 60Hz (±1Hz), f_{DATA} > 25SPS		120		
PSRR	Power-supply rejection ratio	AVDD at dc		110		dB
		DVDD at dc		115		

minimum and maximum specifications apply from T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; all specifications are at AVDD = 1.74V to 3.6V, DVDD = 1.65V to 3.6V, internal reference, internal oscillator, all speed modes, all data rates, all gain settings, and global chop disabled (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOLTAGE REFERENCE INPUTS						
	Absolute input current	REF buffer disabled, speed mode 0[2]	–1.5	±1	1.5	μA/V
		REF buffer disabled, speed mode 1[2]	–7	±6	7	
		REF buffer disabled, speed mode 2[2]	–8	±7	8	
		REF buffer disabled, speed mode 3[2]	–9	±8	9	
		REF buffer enabled, speed mode 0	–2	±0.2	2	nA
		REF buffer enabled, speed mode 1		3	7	
		REF buffer enabled, speed mode 2		10	12	
		REF buffer enabled, speed mode 3		17	23	
INTERNAL VOLTAGE REFERENCE						
V_{REF}	Output voltage	AVDD < 2.7V		1.25		V
		AVDD ≥ 2.7V		1.25, 2.5		
	Accuracy	T_A = 25°C	–0.15	±0.05	0.15	%
	Temperature drift			10	25	ppm/°C
	Output current	V_{REF} = 1.25V, sink or source	–5		5	mA
		V_{REF} = 2.5V, AVDD ≥ 2.75V, sink or source	–10		5	
	Short-circuit current limit	Sink or source		±25		mA
PSRR	Power-supply rejection ratio	AVDD at dc		90		dB
	Load regulation	Load current = –5mA to 0mA (source)		100		μV/mA
	Capacitive load stability		50	100	1300	nF
	Reference noise	f = 0.1Hz to 10Hz, 100nF capacitor on REFOUT		4		ppm_{PP}
	Start-up time	From power-down mode, 100nF capacitor on REFOUT, 0.01% settling			10	ms
INTERNAL OSCILLATOR						
f_{OSC}	Frequency			4.096		MHz
	Accuracy		–1		1	%
EXCITATION CURRENT SOURCES (IDACS)						
	Current settings	IDAC unit current = 1μA		1 to 100		μA
		IDAC unit current = 10μA, AVDD < 2.7V		10 to 500		
		IDAC unit current = 10μA, AVDD ≥ 2.7V		10 to 1000		
	Compliance voltage	I_{IDAC} <100μA, current changes by less than 1% from (AVDD – 1V)	GND		AVDD – 0.3	V
		I_{IDAC} = 100μA to 700μA, current changes by less than 1% from (AVDD – 1V)	GND		AVDD – 0.4	
		I_{IDAC} current ≥ 800μA, current changes by less than 1% from (AVDD – 1V)	GND		AVDD – 0.45	
	Accuracy	I_{IDAC} = 1μA, T_A = 25°C	–6	±0.4	6	%
		I_{IDAC} = 10μA to 1mA, T_A = 25°C	–3	±0.4	3	
	Current mismatch between IDACs	I_{IDAC} ≤ 10μA, IDAC1 and IDAC2 set to same value, T_A = 25°C		0.5	2	%
		I_{IDAC} ≥ 20μA, IDAC1 and IDAC2 set to same value, T_A = 25°C		0.05	0.5	
	Temperature drift	I_{IDAC} = 1μA		50	300	ppm/°C
		I_{IDAC} ≥ 10μA		25	110	
	Temperature drift matching	I_{IDAC} ≤ 10μA, IDAC1 and IDAC2 set to same value		12	70	ppm/°C
		I_{IDAC} ≥ 20μA, IDAC1 and IDAC2 set to same value		1	10	

minimum and maximum specifications apply from T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; all specifications are at AVDD = 1.74V to 3.6V, DVDD = 1.65V to 3.6V, internal reference, internal oscillator, all speed modes, all data rates, all gain settings, and global chop disabled (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BURNOUT CURRENT SOURCES (BOCS)						
	Current settings			0.2, 1, 10		µA
	Accuracy	Sink and source		±2		%
TEMPERATURE SENSOR						
TS_{Offset}	Output voltage	T_A = 25°C		119.5		mV
TS_{TC}	Temperature coefficient			405		µV/°C
MONITORS						
TH_{DVDD_POR}	DVDD POR threshold			1.55		V
TH_{AVDD_UV}	AVDD undervoltage threshold(3)		1.2		1.5	V
TH_{REF_UV}	Reference undervoltage threshold(3)		0.5		0.6	V
	System monitor voltage readback accuracy	(V_{REFP} – V_{REFN}) / 8		±0.5		%
		AVDD / 8		±1		
		DVDD / 8		±1		
GENERAL-PURPOSE INPUTS/OUTPUTS (GPIOs)						
V_{IL}	Logic input level, low		GND		0.3 AVDD	V
V_{IH}	Logic input level, high		0.7 AVDD		AVDD	V
V_{OL}	Logic output level, low	I_{OL} = 100µA, open-drain or push-pull output	GND		0.2 AVDD	V
V_{OH}	Logic output level, high	I_{OH} = –100µA, push-pull output	0.8 AVDD		AVDD	V
	Input hysteresis			10		mV
DIGITAL INPUTS/OUTPUTS						
V_{IL}	Logic input level, low		GND		0.3 DVDD	V
V_{IH}	Logic input level, high		0.7 DVDD		DVDD	V
V_{OL}	Logic output level, low	I_{OL} = 1mA	GND		0.2 DVDD	V
V_{OH}	Logic output level, high	I_{OH} = –1mA	0.8 DVDD		DVDD	V
	Input hysteresis			180		mV
	Input current	GND ≤ $V_{Digital\ Input}$ ≤ DVDD	–1		1	µA

minimum and maximum specifications apply from T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; all specifications are at AVDD = 1.74V to 3.6V, DVDD = 1.65V to 3.6V, internal reference, internal oscillator, all speed modes, all data rates, all gain settings, and global chop disabled (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG SUPPLY CURRENTS (AVDD = 3.3V, External Reference, Reference Buffers Disabled, IDACs Disabled, All Data Rates, V_{IN} = 0V)						
I_{AVDD}	Analog supply current	Power-down mode		0.2	2	µA
		Standby mode		10	16	
		Conversion mode, speed mode 0, gain = 0.5 to 2		52	59	
		Conversion mode, speed mode 0, gain = 4 and 5		55	63	
		Conversion mode, speed mode 0, gain = 8 to 50		61	68	
		Conversion mode, speed mode 0, gain = 64 to 256		57	64	
		Conversion mode, speed mode 1, gain = 0.5 to 2		135	145	
		Conversion mode, speed mode 1, gain = 4 and 5		155	170	
		Conversion mode, speed mode 1, gain = 8 to 50		205	220	
		Conversion mode, speed mode 1, gain = 64 to 256		255	275	
		Conversion mode, speed mode 2, gain = 0.5 to 2		315	335	
		Conversion mode, speed mode 2, gain = 4 and 5		360	380	
		Conversion mode, speed mode 2, gain = 8 to 50		450	480	
		Conversion mode, speed mode 2, gain = 64 to 256		670	705	
		Conversion mode, speed mode 3, gain = 0.5 to 2		540	570	
		Conversion mode, speed mode 3, gain = 4 and 5		640	680	
		Conversion mode, speed mode 3, gain = 8 to 50		870	920	
		Conversion mode, speed mode 3, gain = 64 to 256		1090	1140	
ADDITIONAL ANALOG SUPPLY CURRENTS PER FUNCTION (AVDD = 3.3V, V_{REF} = 2.5V)						
I_{AVDD}	Analog supply current	Internal voltage reference, speed mode 0		4.5	6	µA
		Internal voltage reference, speed mode 1		25	28	
		Internal voltage reference, speed mode 2		35	40	
		Internal voltage reference, speed mode 3		65	75	
		Either REFP or REFN buffer enabled, speed mode 0		4.5	6	
		Either REFP or REFN buffer enabled, speed mode 1		25	28	
		Either REFP or REFN buffer enabled, speed mode 2		35	40	
		Either REFP or REFN buffer enabled, speed mode 3		65	75	
		Both REFP and REFN buffers enabled, speed mode 0		6.5	9	
		Both REFP and REFN buffers enabled, speed mode 1		33	39	
		Both REFP and REFN buffers enabled, speed mode 2		51	60	
		Both REFP and REFN buffers enabled, speed mode 3		106	124	
		IDAC overhead, IDAC unit current = 1µA		4	6	
		IDAC overhead, IDAC unit current = 10µA		16	28	
DIGITAL SUPPLY CURRENTS (DVDD = 3.3V, All Data Rates, SPI Not Active)						
I_{DVDD}	Digital supply current	Power-down mode		1.6	6.5	µA
		Standby mode, speed mode 0		8	13	
		Standby mode, speed mode 1		20	26	
		Standby mode, speed mode 2		26	33	
		Standby mode, speed mode 3		40	47	
		Conversion mode, speed mode 0		9	16	
		Conversion mode, speed mode 1		30	38	
		Conversion mode, speed mode 2		48	56	
		Conversion mode, speed mode 3		82	92	

minimum and maximum specifications apply from T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; all specifications are at AVDD = 1.74V to 3.6V, DVDD = 1.65V to 3.6V, internal reference, internal oscillator, all speed modes, all data rates, all gain settings, and global chop disabled (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG SUPPLY CURRENTS (AVDD = 1.8V, External Reference, Reference Buffers Disabled, IDACs Disabled, All Data Rates, V_{IN} = 0V)						
I_{AVDD}	Analog supply current	Power-down mode		0.2	2	µA
		Standby mode		8	14	
		Conversion mode, speed mode 0, gain = 0.5 to 2		48	55	
		Conversion mode, speed mode 0, gain = 4 and 5		51	58	
		Conversion mode, speed mode 0, gain = 8 to 50		57	64	
		Conversion mode, speed mode 0, gain = 64 to 256		53	60	
		Conversion mode, speed mode 1, gain = 0.5 to 2		120	130	
		Conversion mode, speed mode 1, gain = 4 and 5		140	155	
		Conversion mode, speed mode 1, gain = 8 to 50		190	205	
		Conversion mode, speed mode 1, gain = 64 to 256		240	260	
		Conversion mode, speed mode 2, gain = 0.5 to 2		285	305	
		Conversion mode, speed mode 2, gain = 4 and 5		325	345	
		Conversion mode, speed mode 2, gain = 8 to 50		420	445	
		Conversion mode, speed mode 2, gain = 64 to 256		635	670	
		Conversion mode, speed mode 3, gain = 0.5 to 2		485	515	
		Conversion mode, speed mode 3, gain = 4 and 5		580	620	
		Conversion mode, speed mode 3, gain = 8 to 50		810	860	
		Conversion mode, speed mode 3, gain = 64 to 256		1020	1080	
ADDITIONAL ANALOG SUPPLY CURRENTS PER FUNCTION (AVDD = 1.8V, V_{REF} = 1.25V)						
I_{AVDD}	Analog supply current	Internal voltage reference, speed mode 0		3.5	5	µA
		Internal voltage reference, speed mode 1		16	20	
		Internal voltage reference, speed mode 2		26	31	
		Internal voltage reference, speed mode 3		56	66	
		Either REFP or REFN buffer enabled, speed mode 0		3.5	5	
		Either REFP or REFN buffer enabled, speed mode 1		16	20	
		Either REFP or REFN buffer enabled, speed mode 2		26	31	
		Either REFP or REFN buffer enabled, speed mode 3		56	66	
		Both REFP and REFN buffers enabled, speed mode 0		5.5	8	
		Both REFP and REFN buffers enabled, speed mode 1		25	30	
		Both REFP and REFN buffers enabled, speed mode 2		43	53	
		Both REFP and REFN buffers enabled, speed mode 3		100	120	
		IDAC overhead, IDAC unit current = 1µA		4	6	
		IDAC overhead, IDAC unit current = 10µA		16	28	
DIGITAL SUPPLY CURRENTS (DVDD = 1.8V, All Data Rates, SPI Not Active)						
I_{DVDD}	Digital supply current	Power-down mode		1.6	6.5	µA
		Standby mode, speed mode 0		7	13	
		Standby mode, speed mode 1		19	26	
		Standby mode, speed mode 2		25	33	
		Standby mode, speed mode 3		39	47	
		Conversion mode, speed mode 0		9	16	
		Conversion mode, speed mode 1		30	38	
		Conversion mode, speed mode 2		48	56	
		Conversion mode, speed mode 3		82	92	

(1) Input currents scale with speed mode, data rate, gain, and global-chop mode settings.
(2) Current is flowing into REFP and out of REFN.
(3) Undervoltage monitor does always trip below the specified MIN value and does never trip above the specified MAX value.

5.6 Timing Requirements

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$t_{c(SC)}$	SCLK period	60	1/(4 f_{DATA})	ns
$t_{w(SCL)}$	Pulse duration, SCLK low	20		ns
$t_{w(SCH)}$	Pulse duration, SCLK high	30		ns
$t_{d(CSSC)}$	Delay time, first SCLK rising edge after $\overline{CS}$ falling edge	10		ns
$t_{d(SCCS)}$	Delay time, $\overline{CS}$ rising edge after final SCLK falling edge	10		ns
$t_{w(CSH)}$	Pulse duration, $\overline{CS}$ high	30		ns
$t_{su(DI)}$	Setup time, SDI valid before SCLK falling edge	8		ns
$t_{h(DI)}$	Hold time, SDI valid after SCLK falling edge	8		ns
$t_{d(fr2fr)}$	Delay time, between frames in 3-wire SPI mode	0		ns
$t_{h(DIIR)}$	Hold time, SDI high to force interface resynchronization (3-wire SPI mode only). Interface resynchronization happens on first SCLK falling edge where SDI is low again.	63		t_{SCLK}
$t_{d(RST)}$	Delay time, SPI communication start after software reset using SPI reset pattern or RESET[5:0] bit field	500		µs
$t_{d(POR)}$	Delay time, first SCLK rising edge after DVDD exceeds minimum DVDD voltage	5		ms

5.7 Switching Characteristics

over operating ambient temperature range, C_{LOAD} = 20pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{p(CSDO)}$	Propagation delay time, $\overline{CS}$ falling edge to SDO/$\overline{DRDY}$ driven				25	ns
$t_{p(CSDOZ)}$	Propagation delay time, $\overline{CS}$ rising edge to SDO/$\overline{DRDY}$ high impedance state				25	ns
$t_{p(SCDO)}$	Propagation delay time, SCLK rising edge to valid SDO/$\overline{DRDY}$				28	ns
$t_{w(DRH)}$	Pulse duration, $\overline{DRDY}$ high		2			t_{MOD}
$t_{p(SCDR)}$	Propagation delay time, 8th SCLK falling edge of conversion result MSB readout to $\overline{DRDY}$ return high				5	t_{MOD}
$t_{p(DODR)}$	Propagation delay time, last SCLK falling edge of read operation for SDO/$\overline{DRDY}$ transition from SDO to $\overline{DRDY}$ mode	SDO_DRDY = 1b			50	ns
$t_{p(GPIO)}$	Propagation delay time, $\overline{CS}$ rising edge of register write command to GPIOx output valid				100	ns

5.8 Timing Diagrams

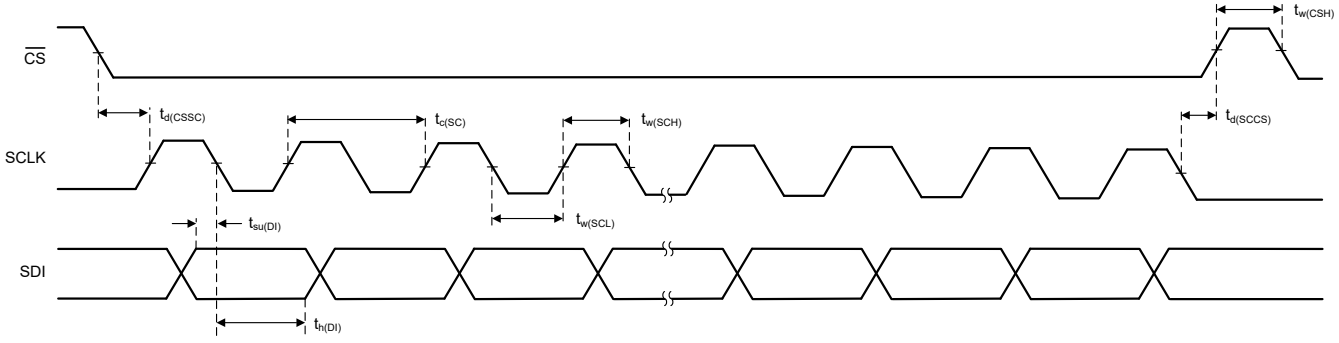


Figure 5-1. Serial Interface Timing Requirements

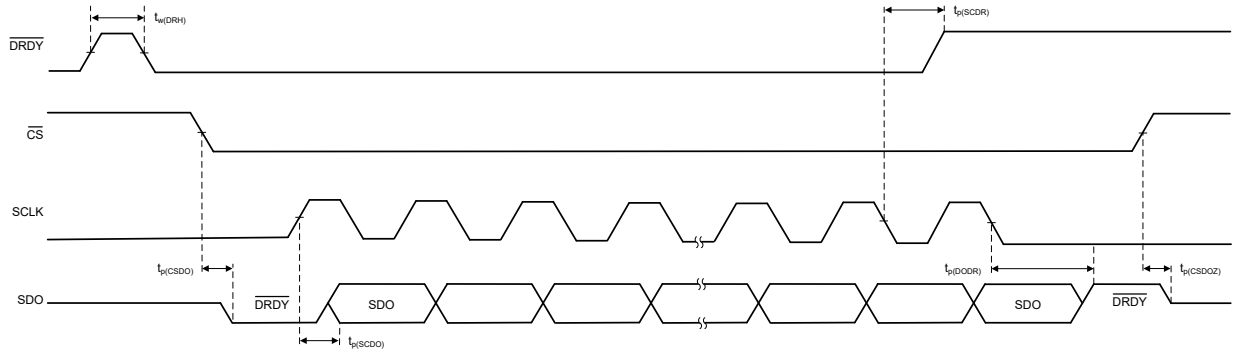


Figure 5-2. Serial Interface Switching Characteristics

5.9 Typical Characteristics

at T_A = 25°C (unless otherwise noted)

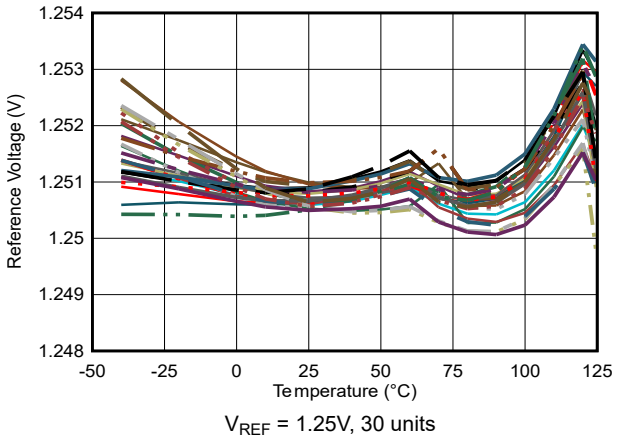


Figure 5-3. Internal Reference Voltage vs Temperature

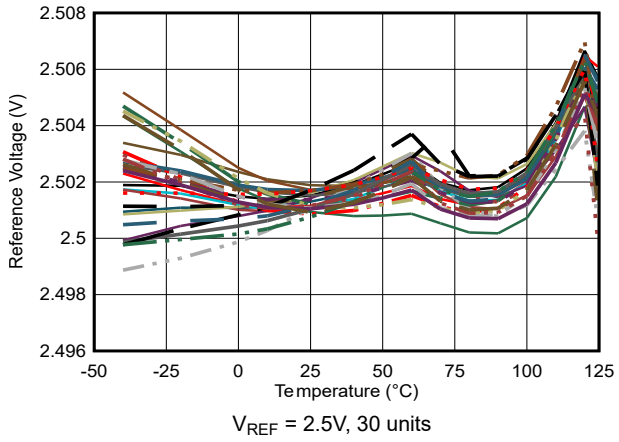


Figure 5-4. Internal Reference Voltage vs Temperature

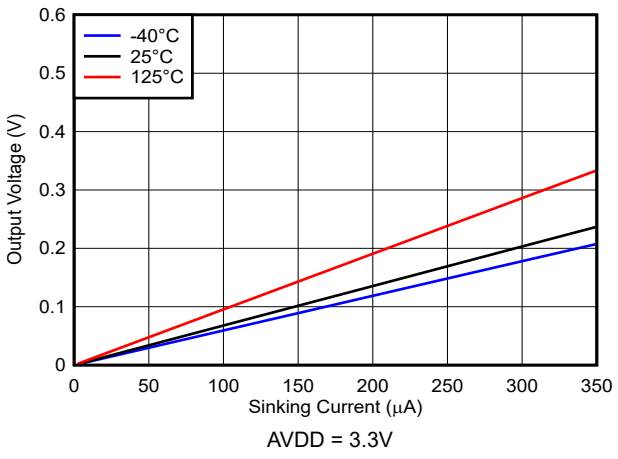


Figure 5-5. GPIO Pin Output Voltage vs Sinking Current

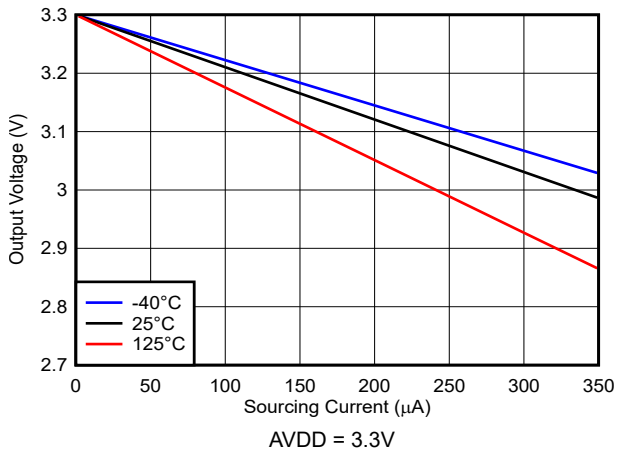


Figure 5-6. GPIO Pin Output Voltage vs Sourcing Current

6 Parameter Measurement Information

6.1 Noise Performance

Delta-sigma (ΔΣ) analog-to-digital converters (ADCs) are based on the principle of oversampling. The input signal of a ΔΣ ADC is sampled at a high frequency (modulator frequency) and subsequently filtered and decimated in the digital domain to yield a conversion result at the respective output data rate. The ratio between modulator frequency and output data rate is called the oversampling ratio (OSR). By increasing the OSR, and thus reducing the output data rate, the noise performance of the ADC can be optimized. In other words, the input-referred noise drops when reducing the output data rate because more samples of the internal modulator are averaged to yield one conversion result. Increasing the gain also reduces the input-referred noise, which is particularly useful when measuring low-level signals.

Table 6-1 to Table 6-3 summarize the typical device noise performance at T_A = 25°C using f_{CLK} = 4.096MHz. The data shown are typical input-referred noise results (e_n) in units of μV_{RMS} with the analog inputs shorted together. A minimum of 1,000 consecutive conversions or 10 seconds of consecutive conversions (whichever occurs first) are used to measure RMS noise. Because of the statistical nature of noise, repeated noise measurements can yield higher or lower noise results.

Use Equation 1 or Equation 2 to calculate effective resolution from the provided μV_{RMS} numbers, depending on the selected coding scheme.

$$\text{Binary two's complement coding: Effective Resolution} = \ln[(2 \times V_{REF} / \text{Gain}) / e_{n(RMS)}] / \ln(2) \quad (1)$$

$$\text{Unipolar straight binary coding: Effective Resolution} = \ln[(V_{REF} / \text{Gain}) / e_{n(RMS)}] / \ln(2) \quad (2)$$

Input-referred noise (e_n) in units of μV_{PP} can be estimated as $e_{n(PP)} = 6.6 \times e_{n(RMS)}$. Use Equation 3 or Equation 4 to calculate noise-free resolution from the estimated μV_{PP} numbers, depending on the selected coding scheme.

$$\text{Binary two's complement coding: Noise-free Resolution} = \ln[(2 \times V_{REF} / \text{Gain}) / e_{n(PP)}] / \ln(2) \quad (3)$$

$$\text{Unipolar straight binary coding: Noise-free Resolution} = \ln[(V_{REF} / \text{Gain}) / e_{n(PP)}] / \ln(2) \quad (4)$$

Input-referred noise performance using shorted inputs does only change insignificantly with the reference voltage. That is, Table 6-1 to Table 6-3 also apply to other reference voltage values.

In global-chop mode, the device averages two measurement of the ADC with the inputs swapped. Global-chop mode significantly reduces the input offset of the device, and reduces noise by a factor of $\sqrt{2}$.

Noise data is measured using the 24-bit version of the device. For the 16-bit device, clip the noise data at the LSB size.

Table 6-1. Input-referred Noise in μV_{RMS}, at AVDD = 3.3V, Global-Chop Mode Disabled, Internal 2.5V Reference, Gain = 0.5 to 8

OSR	DATA RATE (SPS)(1)	GAIN					
		0.5	1	2	4	5	8
SPEED MODE 0 (f_{MOD} = 32kHz)							
1600	20	8.06	3.91	2.20	1.44	1.37	0.99
1280	25	8.44	4.36	2.46	1.51	1.50	1.10
1024	31.25	8.27	4.22	3.32	1.46	1.44	1.07
512	62.5	11.5	5.82	3.27	2.09	2.00	1.47
256	125	16.1	8.18	4.44	2.91	2.91	2.08
128	250	21.6	10.9	6.20	3.80	3.80	2.75
32	1000	33.1	16.5	9.24	5.80	5.80	4.13
16	2000	51.7	26.0	14.1	8.37	8.37	5.81
SPEED MODE 1 (f_{MOD} = 256kHz)							
12800	20	2.46	1.32	0.80	0.57	0.57	0.49
10240	25	2.64	1.41	0.82	0.61	0.59	0.54
1024	250	7.34	3.87	2.33	1.69	1.69	1.53
512	500	10.4	5.41	3.23	2.37	2.37	2.15
256	1000	14.4	7.44	4.51	3.31	3.31	2.98
128	2000	19.5	10.2	6.08	4.39	4.39	3.93
32	8000	29.4	15.2	9.10	6.56	6.56	5.76
16	16000	49.4	25.3	14.5	9.78	9.77	8.26
SPEED MODE 2 (f_{MOD} = 512kHz)							
25600	20	1.74	0.90	0.51	0.33	0.33	0.28
20480	25	1.85	0.99	0.55	0.35	0.35	0.30
1024	500	7.36	3.75	2.11	1.42	1.40	1.18
512	1000	10.2	5.16	2.93	1.97	1.97	1.65
256	2000	14.3	7.16	4.13	2.73	2.73	2.27
128	4000	19.3	9.82	5.55	3.66	3.65	3.04
32	16000	29.0	14.8	8.34	5.40	5.40	4.45
16	32000	49.4	25.1	13.6	8.31	8.31	6.48
SPEED MODE 3 (f_{MOD} = 1024kHz)							
51200	20	1.27	0.67	0.39	0.28	0.28	0.26
40960	25	1.36	0.70	0.41	0.30	0.30	0.27
1024	1000	7.43	3.86	2.27	1.64	1.63	1.55
512	2000	10.4	5.42	3.18	2.29	2.29	2.18
256	4000	14.5	7.47	4.43	3.17	3.17	3.02
128	8000	19.6	10.2	5.93	4.27	4.26	4.03
32	32000	29.5	15.2	8.89	6.31	6.30	5.93
16	64000	50.1	25.6	14.3	9.56	9.56	8.52

(1) Using f_{CLK} = 4.096MHz

Table 6-2. Input-referred Noise in μV_{RMS}, at AVDD = 3.3V, Global-Chop Mode Disabled, Internal 2.5V Reference, Gain = 10 to 64

OSR	DATA RATE (SPS)(1)	GAIN					
		10	16	20	32	50	64
SPEED MODE 0 (f_{MOD} = 32kHz)							
1600	20	1.02	0.57	0.57	0.42	0.41	0.33
1280	25	1.07	0.60	0.60	0.43	0.43	0.35
1024	31.25	1.06	0.61	0.58	0.44	0.44	0.34
512	62.5	1.44	0.84	0.79	0.61	0.61	0.48
256	125	2.08	1.15	1.13	0.80	0.80	0.65
128	250	2.75	1.57	1.54	1.11	1.11	0.91
32	1000	4.13	2.36	2.33	1.66	1.66	1.35
16	2000	5.81	3.25	3.25	2.30	2.30	1.80
SPEED MODE 1 (f_{MOD} = 256kHz)							
12800	20	0.49	0.31	0.31	0.28	0.28	0.16
10240	25	0.53	0.34	0.34	0.30	0.30	0.17
1024	250	1.51	0.97	0.97	0.87	0.87	0.49
512	500	2.12	1.33	1.31	1.25	1.25	0.68
256	1000	2.98	1.90	1.89	1.72	1.72	0.94
128	2000	3.88	2.42	2.41	2.18	2.16	1.19
32	8000	5.76	3.50	3.50	3.10	3.10	1.59
16	16000	8.26	4.97	4.96	4.37	4.36	2.21
SPEED MODE 2 (f_{MOD} = 512kHz)							
25600	20	0.28	0.19	0.19	0.16	0.15	0.10
20480	25	0.30	0.21	0.21	0.17	0.17	0.10
1024	500	1.18	0.82	0.82	0.69	0.69	0.43
512	1000	1.64	1.15	1.15	0.96	0.96	0.59
256	2000	2.27	1.59	1.59	1.37	1.37	0.83
128	4000	3.04	2.10	2.10	1.77	1.74	1.08
32	16000	4.45	3.03	3.03	2.50	2.49	1.55
16	32000	6.48	4.35	4.35	3.53	3.52	2.17
SPEED MODE 3 (f_{MOD} = 1024kHz)							
51200	20	0.26	0.17	0.17	0.16	0.16	0.09
40960	25	0.27	0.19	0.19	0.16	0.16	0.10
1024	1000	1.54	1.09	1.09	0.93	0.93	0.58
512	2000	2.17	1.54	1.54	1.31	1.31	0.80
256	4000	2.99	2.13	2.13	1.81	1.81	1.11
128	8000	4.03	2.83	2.83	2.41	2.37	1.48
32	32000	5.92	4.16	4.16	3.47	3.47	2.14
16	64000	8.50	5.92	5.91	4.91	4.91	3.02

(1) Using f_{CLK} = 4.096MHz

Table 6-3. Input-referred Noise in μV_{RMS}, at AVDD = 3.3V, Global-Chop Mode Disabled, Internal 2.5V Reference, Gain = 100 to 256

OSR	DATA RATE (SPS)(1)	GAIN			
		100	128	200	256
SPEED MODE 0 (f_{MOD} = 32kHz)					
1600	20	0.327	0.299	0.299	0.268
1280	25	0.347	0.310	0.308	0.305
1024	31.25	0.333	0.301	0.301	0.278
512	62.5	0.474	0.435	0.421	0.387
256	125	0.654	0.589	0.572	0.552
128	250	0.914	0.776	0.776	0.773
32	1000	1.349	1.190	1.187	1.117
16	2000	1.812	1.587	1.574	1.510
SPEED MODE 1 (f_{MOD} = 256kHz)					
12800	20	0.146	0.143	0.141	0.134
10240	25	0.164	0.152	0.152	0.141
1024	250	0.482	0.438	0.438	0.426
512	500	0.661	0.635	0.617	0.593
256	1000	0.944	0.900	0.857	0.822
128	2000	1.186	1.086	1.086	1.036
32	8000	1.593	1.441	1.441	1.350
16	16000	2.211	1.987	1.980	1.859
SPEED MODE 2 (f_{MOD} = 512kHz)					
25600	20	0.099	0.083	0.083	0.073
20480	25	0.102	0.086	0.084	0.079
1024	500	0.425	0.353	0.353	0.316
512	1000	0.589	0.507	0.505	0.440
256	2000	0.832	0.690	0.690	0.609
128	4000	1.080	0.902	0.896	0.782
32	16000	1.541	1.260	1.251	1.078
16	32000	2.167	1.747	1.746	1.489
SPEED MODE 3 (f_{MOD} = 1024kHz)					
51200	20	0.093	0.080	0.079	0.068
40960	25	0.101	0.085	0.083	0.074
1024	1000	0.576	0.484	0.474	0.414
512	2000	0.801	0.666	0.666	0.589
256	4000	1.114	0.929	0.929	0.804
128	8000	1.477	1.221	1.208	1.045
32	32000	2.140	1.742	1.742	1.490
16	64000	3.007	2.436	2.434	2.067

(1) Using f_{CLK} = 4.096MHz

7 Detailed Description

7.1 Overview

The ADS1x2S14 are small, low-power, 16- and 24-bit, ΔΣ ADCs that offer many integrated features to reduce system cost and component count in the most common sensor measurement applications. The devices are available in a 3mm × 3mm WQFN-16, as well as in a 1.87mm × 1.97mm DSBGA-16 package for extremely space-constrained applications.

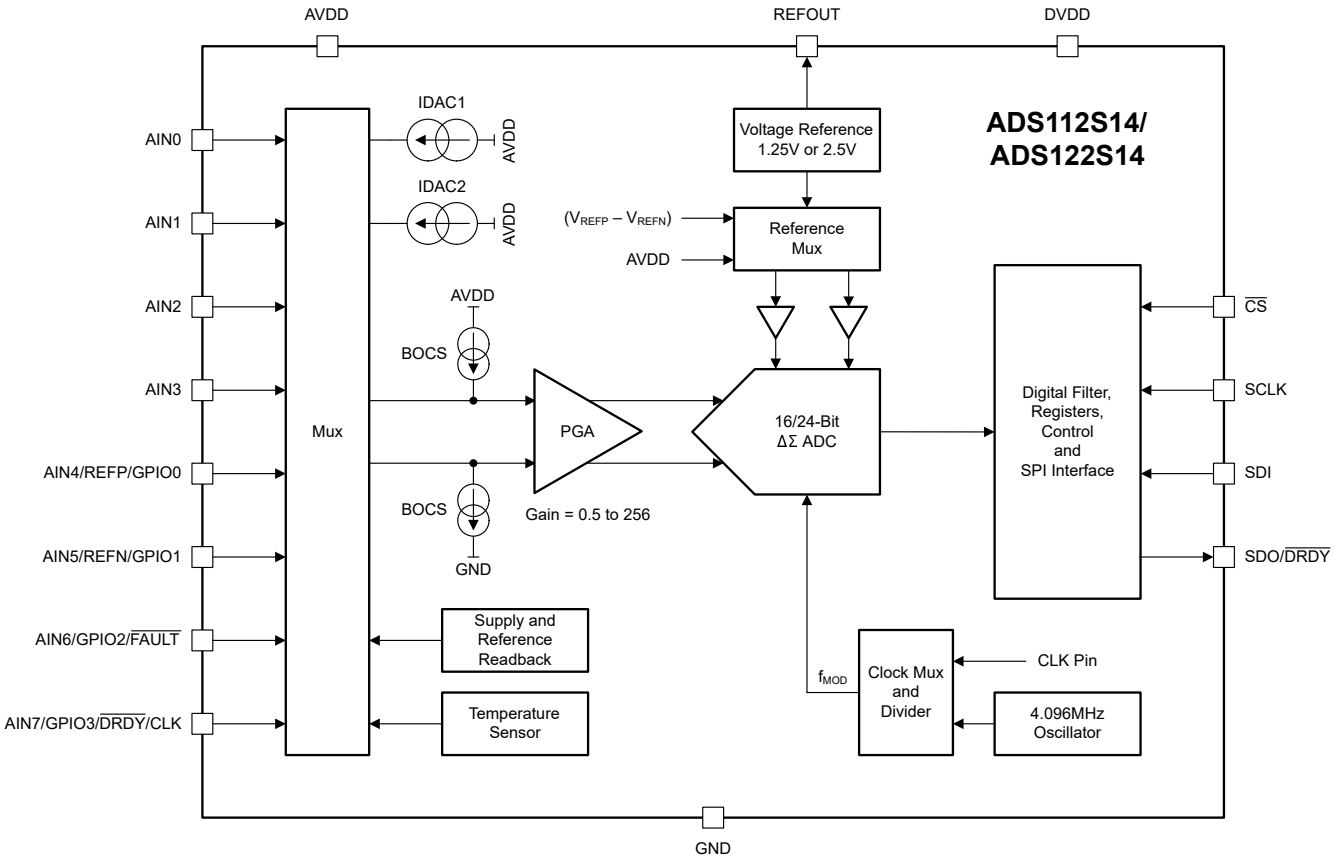
Key integrated analog features include:

- A flexible input multiplexer which allows to select any of the eight analog inputs or GND as positive or negative input.
- A low-noise, high input-impedance PGA with programmable gain from 0.5 to 256.
  - Gain of 0.5 allows to measure signals which are larger than the selected reference voltage.
  - Single-ended measurements, where the negative input is connected to GND, are possible for gain settings between 0.5 and 10.
- A low-drift voltage reference programmable to 1.25V or 2.5V. A buffered version of the internal voltage reference is available on the REFOUT pin which can be used to bias external circuitry.
- One external, differential reference input with optional reference buffers that can be individually enabled and disabled.
- Two matched, sensor-excitation current sources (IDACs) which can be routed to any of the eight analog inputs to bias resistive sensors, such as thermistors, resistance temperature detectors (RTDs), or bridge sensors. Excitation currents between 1μA and 1mA can be programmed with fine granularity.
- A set of programmable burn-out current sources that are used for sensor fault detection.
- A low-drift 4.096MHz oscillator which establishes the device main clock. Alternatively an external clock can be provided.
- A linear temperature sensor.
- Analog supply and reference undervoltage monitors. Depending on the circuit implementation, the reference undervoltage monitor is especially helpful to detect open sensor conditions.
- Four general-purpose input/output pins (GPIOs) which are shared with analog inputs. Push-pull or open-drain output configurations can be individually selected for each general-purpose output. The GPIOs use logic levels based on the analog supply.

The devices also include a variety of digital features to accommodate a wide range of applications:

- Four speed modes allow to optimize the power consumption and noise performance for each application.
- Depending on the selected speed mode, output data rates from 20SPS up to 64kSPS can be achieved by adjusting the oversampling ratio (OSR) of the integrated digital filter. At output data rates of 20SPS and 25SPS, the digital filter offers simultaneous 50Hz and 60Hz line-cycle rejection with single-cycle settling.
- A global-chop mode which reduces offset and offset drift to a minimum.
- Selection between single-shot and continuous-conversion modes.
- An SPI-compatible serial interface to read conversion and register data, as well as to configure and control the device. 3-wire SPI operation is possible when the $\overline{CS}$ pin is tied low permanently to reduce the number of required digital communication signals. The interface allows communication with multiple devices on one SPI bus in a daisy chain.
- Data integrity features, such as SPI CRC, register map CRC, and internal memory CRC to detect communication faults and unintended bit flips.
- Selection between two output data coding schemes: binary two's complement and unipolar straight binary format. The unipolar straight binary format is beneficial for applications where the differential input signal is always positive.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Analog Inputs and Multiplexer

The ADS1x2S14 contain a flexible input multiplexer; see Figure 7-1. Select any of the eight analog inputs as the positive or negative input for the PGA using the AINP[3:0] and AINN[3:0] bits. In addition, an internal GND connection can be selected as the positive or negative PGA input.

The multiplexer also routes the two integrated excitation current sources to any of the eight analog input pins to bias resistive sensors (bridges, RTDs, and thermistors).

In addition, the ADS1x2S14 contain the following system monitor functions which can be selected for measurement through the multiplexer using the SYS_MON[2:0] bits:

- The inputs of the PGA can be shorted together to mid-supply, (AVDD / 2), to measure and calibrate the input offset of the internal signal chain.
- An integrated temperature sensor that provides an output signal proportional to the device temperature.
- The attenuated external reference voltage, (V_{REFP} – V_{REFN}) / 8.
- The attenuated analog and digital supplies, (AVDD / 8) and (DVDD / 8), respectively.

Electrostatic discharge (ESD) diodes to AVDD and GND protect the inputs. To prevent the ESD diodes from turning on, the absolute voltage on any input must stay within the range provided by Equation 5:

$$GND - 0.3V < V_{AINx} < AVDD + 0.3V \quad (5)$$

External Schottky clamp diodes or series resistors can be required to limit the input current to safe values (see the *Absolute Maximum Ratings* table). Overdriving an unselected input on the device can affect conversions taking place on other input pins.

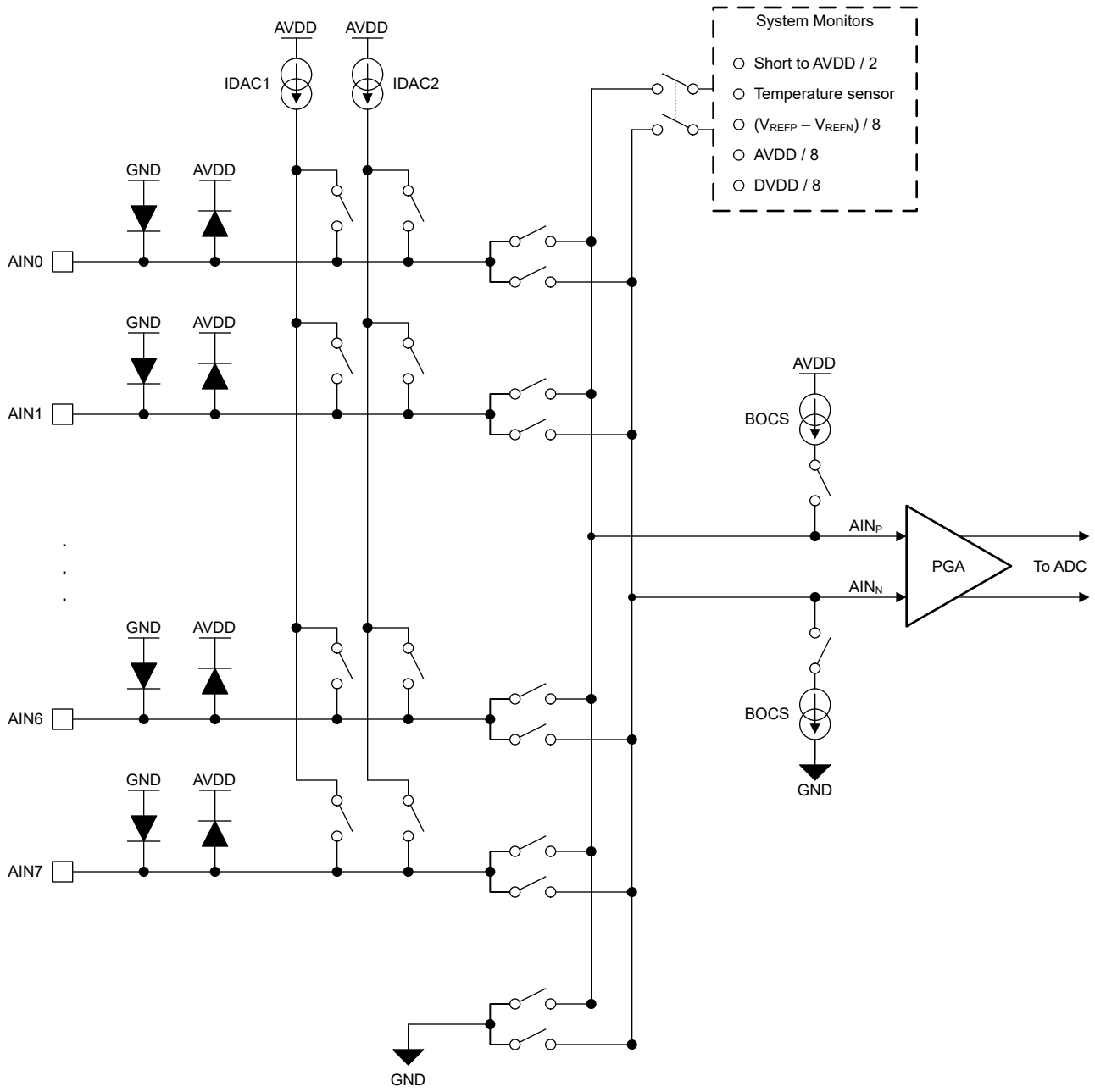


Figure 7-1. Input Multiplexer

7.3.2 Programmable Gain Amplifier (PGA)

The ADS1x2S14 integrate a low-drift, low-noise, high input impedance programmable gain amplifier (PGA). Use the GAIN[3:0] bits to configure the PGA for gains of 0.5, 1, 2, 4, 5, 8, 10, 16, 20, 32, 50, 64, 100, 128, 200, or 256. The full-scale input voltage range (FSR) of the PGA is defined by the gain setting, the reference voltage, and the conversion data coding setting, as shown in Equation 6 and Equation 7:

$$\text{Binary two's complement coding: FSR} = \pm V_{REF} / \text{Gain} \quad (6)$$

$$\text{Unipolar straight binary coding: FSR} = 0\text{V to} + V_{REF} / \text{Gain} \quad (7)$$

Table 7-1 shows the corresponding nominal full-scale ranges using binary two's complement coding for a 1.25V and a 2.5V reference voltage, respectively.

Table 7-1. PGA Full-Scale Range (Binary Two's Complement Coding)

GAIN SETTING	V_{REF} = 1.25V	V_{REF} = 2.5V
0.5	±2.5V	±5V
1	±1.25V	±2.5V
2	±0.625V	±1.25V
4	±0.313V	±0.625V
5	±0.25V	±0.5V
8	±0.156V	±0.313V
10	±0.125V	±0.25V
16	±78.125mV	±0.156V
20	±62.5mV	±0.125V
32	±39.063mV	±78.125mV
50	±25mV	±50mV
64	±19.531mV	±30.063mV
100	±12.5mV	±25mV
128	±9.766mV	±19.531mV
200	±6.25mV	±12.5mV
256	±4.883mV	±9.766mV

Depending on the gain setting, the PGA has certain voltage headroom requirements to stay within the linear operating range that must be met for the selected positive and negative analog inputs as specified by the *absolute input voltage* parameter in the *Recommended Operating Conditions*. Both the positive and negative PGA inputs need to stay within those voltage limits, even for FSR settings which in principle extend beyond those limits. For example, assume AVDD = 3.3V, gain = 0.5, V_{REF} = 2.5V, unipolar coding scheme, and AINN connected to GND. In this case AINP needs to stay between 0V and (3.3V – 0.35V) = 2.95V. Therefore only a portion of the full code range (FSR = 0V to 5V) is utilized.

For gain settings 0.5 to 10, the devices allow single-ended measurements with the negative analog input held at GND. The negative analog input can be connected to GND externally using one of the analog inputs or the internal GND connection of the multiplexer in this case. The devices offer a unipolar, straight binary conversion data coding scheme that can be selected using the CODING bit. This coding scheme is beneficial for single-ended measurements, because the full code range is mapped to the 0V to $+V_{REF}$ / Gain voltage range.

For gain settings 16 to 256 the PGA requires some voltage headroom from GND and AVDD on both the positive and negative analog inputs.

The PGA remains active in idle mode, but turns off in standby and power-down mode.

7.3.3 Voltage Reference

The ADC requires a reference voltage for operation. The magnitude of the reference voltage together with the PGA gain setting establishes the ADC full-scale range. Use the REF_SEL[1:0] bits to select from one of the following reference sources:

- Internal voltage reference
- External reference connected between the REFP and REFN pins ($V_{REF} = V_{REFP} – V_{REFN}$)
- Analog supply (V_{REF} = AVDD)

7.3.3.1 Internal Reference

The devices integrate a precision, low-drift voltage reference. Select between a 1.25V and 2.5V reference voltage option using the REF_VAL bit. When changing the REF_VAL bit setting, allow at least 250µs for the device to switch the reference value before starting any conversions. The internal voltage reference requires a certain voltage headroom from the AVDD supply for operation as specified in the *Electrical Characteristics* table. Keep this headroom in mind when selecting the 2.5V reference value.

The internal reference is always enabled even when the external reference or the analog supply is selected as the reference source. The internal voltage reference only powers down in power-down mode.

The REFOUT pin provides a buffered version of the internal reference voltage. The REFOUT pin can both source and sink current to bias external circuitry. Connect a 100nF capacitor between REFOUT and GND. Larger capacitor values up to 1.3µF can be used to help filter more noise at the expense of a longer reference start-up time. The capacitor is required for the internal voltage reference stability, even when the REFOUT pin is not used to bias any external circuitry, and even when the external reference or the analog supply is selected as the reference source. Keep the reference settling time in mind after device power-up or when coming out of power-down mode before starting any conversions.

7.3.3.2 External Reference

An external reference can be applied between the REFP and REFN pins ($V_{REF} = V_{REFP} – V_{REFN}$). The differential reference input allows freedom in the reference common-mode voltage. However, the polarity of the reference voltage must be positive. Follow the requirements in the *Recommended Operating Conditions* for the absolute and differential reference input voltages.

The REFP and REFN inputs are combined with the AIN4 and AIN5 pins. AIN4 and AIN5 can still be used as analog inputs, even when the inputs are configured as external reference inputs.

7.3.3.3 Reference Buffers

The devices provide two individually selectable reference input buffers to lower the reference input current. Use the REFP_BUF_EN and REFN_BUF_EN bits to enable or disable the positive and negative reference buffers respectively.

Disable the negative reference buffer when the external negative reference input (REFN) is at GND. Disable the positive reference buffer when the external positive reference input (REFP) is at AVDD. Disable both reference buffers when either the internal voltage reference or the analog supply is selected as the reference source.

The reference buffers remain active in idle mode, but turn off in standby and power-down mode.

7.3.4 Clock Source

The ADS1x2S14 require a main clock for operation. The main clock is provided in one of two ways:

- The internal low-drift 4.096MHz oscillator or
- An external clock on the CLK input pin

Use the CLK_SEL bit to select the clock source. At device power-up or after device reset, the internal oscillator is selected as the clock source by default.

The external CLK input is combined with the AIN7/GPIO3 pin. To change from the internal oscillator to the external clock, first set GPIO3_CFG = 01b to configure the GPIO3 pin as external clock input, then set CLK_SEL = 1b.

The modulator clock for the delta-sigma ADC is derived from the main clock. A clock divider divides the main clock frequency (f_{CLK}) by a division factor based on the selected speed mode to create the modulator frequency (f_{MOD} = f_{CLK} / DIV). Table 7-2 shows the respective clock divider settings per speed mode together with the nominal modulator frequencies.

Table 7-2. Clock Divider Settings

SPEED MODE	CLOCK DIVIDER (DIV)	MODULATOR FREQUENCY (f_{MOD})(1)
0	128	32kHz
1	16	256kHz
2	8	512kHz
3	4	1.024MHz

(1) Using a nominal clock frequency of f_{CLK} = 4.096MHz.

7.3.5 Delta-Sigma Modulator

The ADS1x2S14 use an inherently stable, third-order, delta-sigma modulator. The modulator samples the analog input voltage at the modulator frequency (f_{MOD} = 1 / t_{MOD}) and converts the analog input to a ones-density bitstream representing the ratio between the input signal and the reference voltage. The modulator shapes the noise of the converter to high frequency, where the noise is removed by the digital filter.

7.3.6 Digital Filter

The delta-sigma modulator bitstream feeds into a digital filter. The digital filter low-pass filters and decimates the low-resolution, high-speed modulator output to produce high-resolution ADC data at an output data rate of f_{DATA}. The decimation factor, defined as per Equation 8, is called the oversampling ratio (OSR).

$$OSR = f_{MOD} / f_{DATA} \quad (8)$$

The OSR determines the amount of averaging that is applied to the modulator output in the digital filter and, therefore, the filter bandwidth and conversion noise. Higher OSRs lead to lower filter bandwidth and better noise performance.

Use the FLTR_OSR[2:0] bits to select the OSR and to select between the following digital filter types:

- Sinc4 filter for OSRs 16 and 32
- Sinc4 filter followed by a Sinc1 filter for OSRs 128 to 1024
- Finite impulse response (FIR) filter with speed-mode independent data rate options of 20SPS and 25SPS, which offers simultaneous 50Hz and 60Hz line-cycle rejection

Figure 7-2 shows the digital filter architecture.

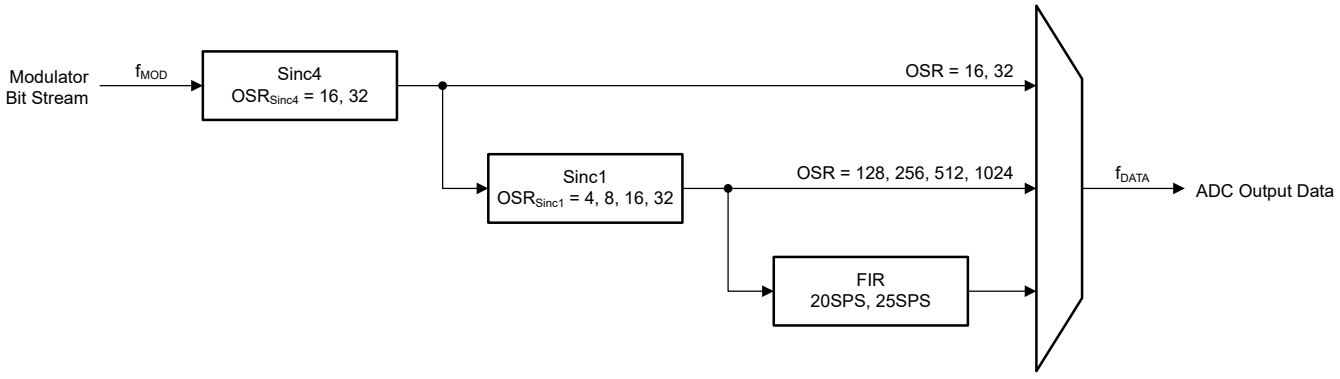


Figure 7-2. Digital Filter Architecture

7.3.6.1 Sinc4 and Sinc4 + Sinc1 Filter

The Sinc filter path is made up of one or two stages based on the FLTR_OSR[2:0] setting as shown in Figure 7-2. For OSR settings 16 and 32, a pure Sinc4 filter is used. For OSR settings 128 to 1024, the Sinc4 filter operates at an OSR = 32, and is followed by a Sinc1 filter stage with OSRs selectable between 4, 8, 16, and 32. Table 7-3 provides an overview of the Sinc filter configurations based on the FLTR_OSR[2:0] setting.

Table 7-3. Sinc Filter OSR Settings

FLTR_OSR[2:0]	SINC4 OSR	SINC1 OSR	OVERALL OSR
000b	16	–	16
001b	32	–	32
010b	32	4	128
011b	32	8	256
100b	32	16	512
101b	32	32	1024

Table 7-4 provides an overview of the resulting output data rates for the various speed modes based on the OSR setting. The data rates scale with f_{CLK}.

Table 7-4. Sinc Filter Output Data Rates

OSR	–3dB Frequency	OUTPUT DATA RATE (f_{DATA})(1)			
		SPEED MODE 0 (f_{MOD} = 32kHz)	SPEED MODE 1 (f_{MOD} = 256kHz)	SPEED MODE 2 (f_{MOD} = 512kHz)	SPEED MODE 3 (f_{MOD} = 1.024MHz)
16	0.228× f_{DATA}	2kSPS	16kSPS	32kSPS	64kSPS
32	0.228× f_{DATA}	1kSPS	8kSPS	16kSPS	32kSPS
128	0.410× f_{DATA}	250SPS	2kSPS	4kSPS	8kSPS
256	0.434× f_{DATA}	125SPS	1kSPS	2kSPS	4kSPS
512	0.440× f_{DATA}	62.5SPS	500SPS	1kSPS	2kSPS
1024	0.442× f_{DATA}	31.25SPS	250SPS	500SPS	1kSPS

(1) Based on a nominal clock frequency of f_{CLK} = 4.096MHz

The frequency response of the combined Sinc4 + Sinc1 filter is given by Equation 9. For the pure Sinc4 filter frequency response ignore the second term in the equation.

$$\left|H_{(f)}\right| = \left|\frac{\sin\left[\frac{A\pi f}{f_{MOD}}\right]}{A\sin\left[\frac{\pi f}{f_{MOD}}\right]}\right|^{4} \cdot \left|\frac{\sin\left[\frac{AB\pi f}{f_{MOD}}\right]}{B\sin\left[\frac{A\pi f}{f_{MOD}}\right]}\right| \quad (9)$$

where:

- f = Signal frequency
- f_{MOD} = Modulator frequency
- A = Sinc4 filter OSR
- B = Sinc1 filter OSR

Figure 7-3 to Figure 7-6 show the filter frequency responses of the Sinc filters normalized to the output data rate. A Sinc filter has infinite attenuation at integer multiples of the output data rate except for integer multiples of f_{MOD}, as shown in Figure 7-4. As with all digital filters, the digital filter response repeats at integer multiples of the modulator frequency, f_{MOD}. The data rate and filter notch frequencies scale with f_{MOD}.

The –3dB frequencies for the various Sinc filter configurations are given in Table 7-4.

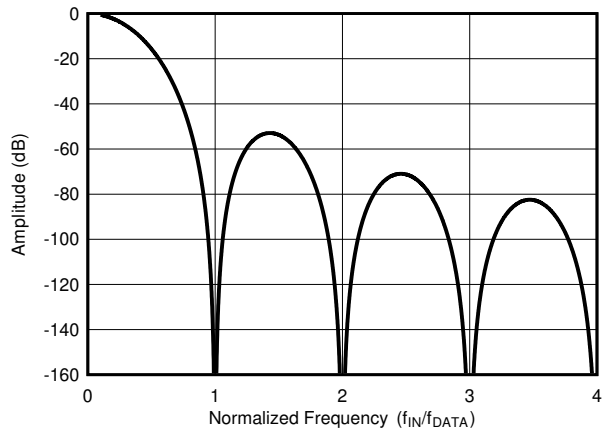


Figure 7-3. Sinc4 Frequency Response

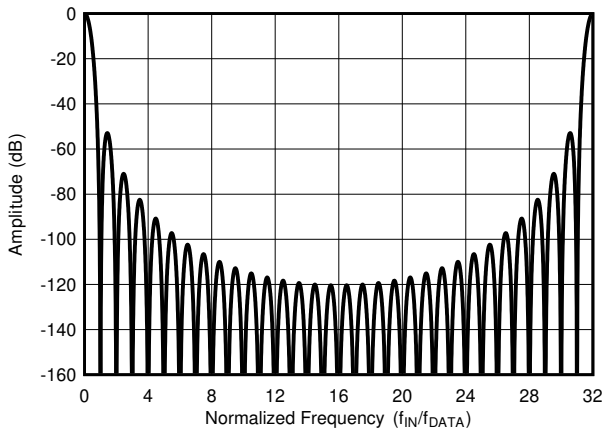


Figure 7-4. Sinc4 Frequency Response to f_{MOD} (OSR = 32)

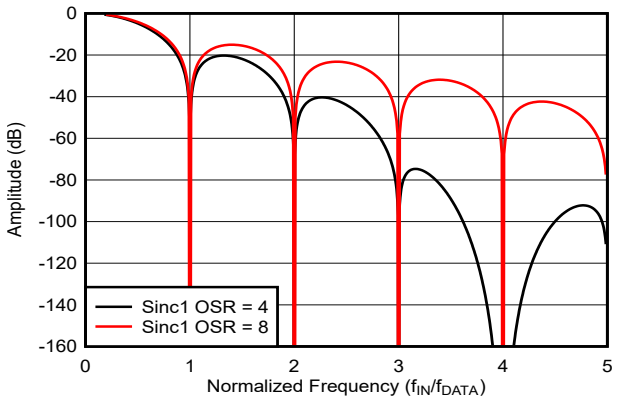


Figure 7-5. Sinc4 + Sinc1 Frequency Response (Sinc4 OSR = 32)

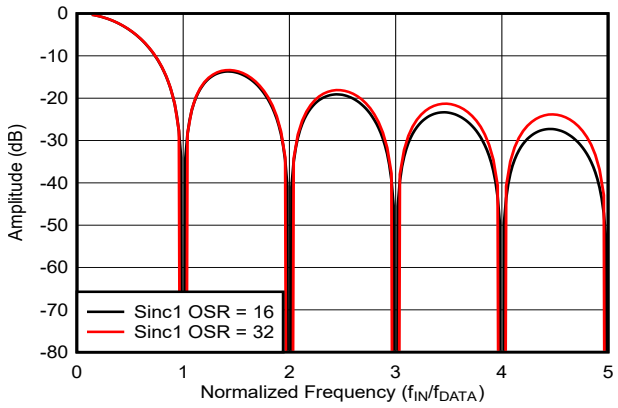


Figure 7-6. Sinc4 + Sinc1 Frequency Response (Sinc4 OSR = 32)

7.3.6.2 FIR Filter

In addition to the Sinc filters, the devices also provide two FIR filter options which offer simultaneous 50Hz and 60Hz line-cycle rejection. Select between a 20SPS and 25SPS data rate option using the FLTR_OSR[2:0] bits. The FIR filter adjusts the OSR based on the selected speed mode to provide data rates of 20SPS and 25SPS in all four speed modes as shown in Table 7-5.

Table 7-5. FIR Filter OSR Settings

OUTPUT DATA RATE(1)	–3dB Frequency	OSR			
		SPEED MODE 0 (f_{MOD} = 32kHz)	SPEED MODE 1 (f_{MOD} = 256kHz)	SPEED MODE 2 (f_{MOD} = 512kHz)	SPEED MODE 3 (f_{MOD} = 1.024MHz)
20SPS	13.2Hz	1600	12800	25600	51200
25SPS	15.1Hz	1280	10240	20480	40960

(1) Based on a nominal clock frequency of f_{CLK} = 4.096MHz

Figure 7-7 to Figure 7-10 show the filter frequency responses for the two FIR filter configurations. The –3dB frequencies for the two FIR filters are given in Table 7-5.

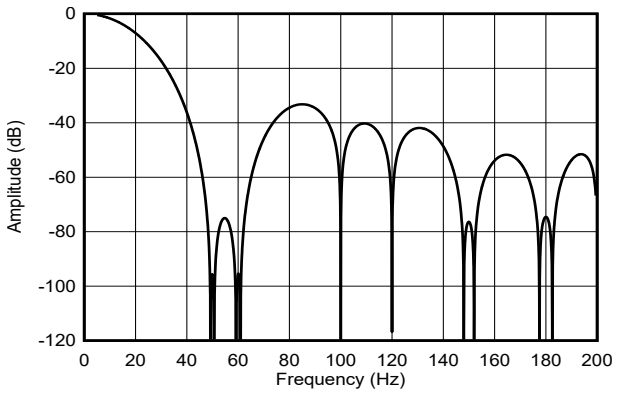


Figure 7-7. 20SPS Frequency Response

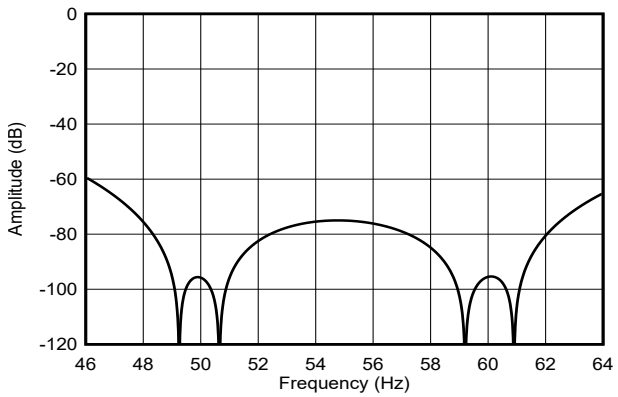


Figure 7-8. 20SPS Frequency Response (Zoomed)

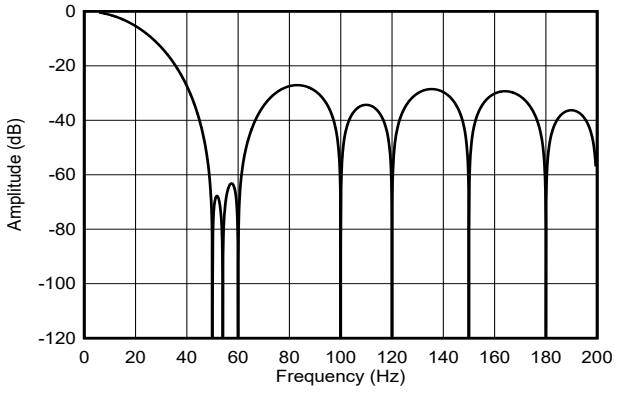


Figure 7-9. 25SPS Frequency Response

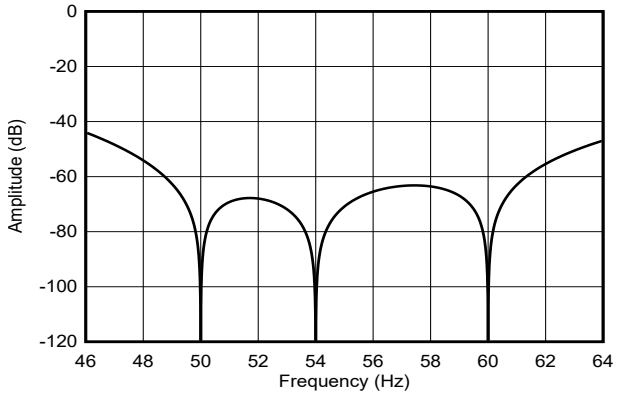


Figure 7-10. 25SPS Frequency Response (Zoomed)

7.3.6.3 Digital Filter Latency

When starting or restarting conversions, the digital filter resets and requires a certain amount of time to provide settled output data. This time is called the latency time, $t_{LATENCY}$. The ADS1x2S14 hide the unsettled data internally and only indicate when settled conversion data are available, by means of a falling $\overline{DRDY}$ edge or the DRDY bit. Table 7-6 and Table 7-7 summarize the latency times for the various speed modes and digital filter settings. The latency times are measured from the rising $\overline{CS}$ edge of the register write frame where the START bit is set to 1b in idle mode, to the first falling $\overline{DRDY}$ edge. Because the $\overline{CS}$ signal in the SPI clock domain is latched by the digital filter logic running on the modulator clock domain, the latency times provided have an uncertainty of ±1 t_{MOD}. The conversion period for the second and all subsequent conversions equals t_{DATA} = 1 / f_{DATA} = OSR / f_{MOD} as shown in Figure 7-11.

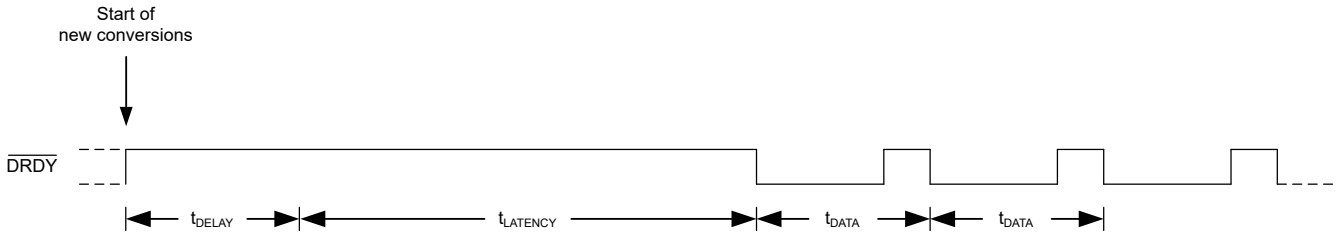


Figure 7-11. Latency Time and Conversion Period

The latency time increases in certain situations:

- when starting conversions from standby mode: adds 5 t_{MOD} (Speed Mode 0), 27 t_{MOD} (Speed Modes 1 and 2), 35 t_{MOD} (Speed Mode 3)
- when restarting ongoing conversions by writing to a register which restarts conversions: adds 6 t_{MOD}

In addition, a programmable delay time can be added to delay the start of the conversion cycle after the START bit is set. This delay time allows for settling of external components, such as the voltage reference after exiting standby mode, or for additional settling time when switching the signal through the multiplexer. The delay time is only added to the first conversion after a conversion start as shown in Figure 7-11. Subsequent conversions are not delayed. Use the DELAY[3:0] bits to configure the delay time.

Table 7-6. Sinc Filter Latency

OSR	LATENCY IN t_{MOD} (1) (ABSOLUTE TIME(2))			
	SPEED MODE 0 (f_{MOD} = 32kHz)	SPEED MODE 1 (f_{MOD} = 256kHz)	SPEED MODE 2 (f_{MOD} = 512kHz)	SPEED MODE 3 (f_{MOD} = 1.024MHz)
16	80 (2.5ms)	88 (344µs)	88 (172µs)	104 (102µs)
32	144 (4.5ms)	152 (594µs)	152 (297µs)	168 (164µs)
128	240 (7.5ms)	248 (969µs)	248 (484µs)	264 (258µs)
256	368 (11.5ms)	376 (1.47ms)	376 (734µs)	392 (383µs)
512	624 (19.5ms)	632 (2.47ms)	632 (1.23ms)	648 (633µs)
1024	1136 (35.5ms)	1144 (4.47ms)	1144 (2.23ms)	1160 (1.13ms)

(1) t_{MOD} = 1 / f_{MOD}. Latency time is measured when starting conversions from idle mode.
(2) Based on a nominal clock frequency of f_{CLK} = 4.096MHz.

Table 7-7. FIR Filter Latency

OUTPUT DATA RATE	LATENCY IN t_{MOD} (1) (ABSOLUTE TIME(2))			
	SPEED MODE 0 (f_{MOD} = 32kHz)	SPEED MODE 1 (f_{MOD} = 256kHz)	SPEED MODE 2 (f_{MOD} = 512kHz)	SPEED MODE 3 (f_{MOD} = 1.024MHz)
20SPS	1736 (54.25ms)	12944 (50.56ms)	25744 (50.28ms)	51360 (50.16ms)
25SPS	1416 (44.25ms)	10384 (40.56ms)	20624 (40.28ms)	41120 (40.16ms)

(1) t_{MOD} = 1 / f_{MOD}. Latency time is measured when starting conversions from idle mode.
(2) Based on a nominal clock frequency of f_{CLK} = 4.096MHz.

7.3.6.4 Global-Chop Mode

The signal chain of the ADS1x2S14 uses a very low-drift, chopper-stabilized PGA and delta-sigma modulator to provide very low offset error and offset drift. However, a small amount of offset drift remains in normal measurement. For that reason, the devices incorporate an optional global-chop mode to reduce offset error and offset drift over both temperature and time to exceptionally low levels. When the global-chop mode is enabled by setting the GC_EN bit, the device performs two consecutive conversions with alternate input signal polarity to cancel offset error. The first conversion is taken with normal input polarity. The global-chop control logic inverts the input polarity and resets the digital filter for the second conversion. The average of the two conversions yields the final offset-corrected result. Figure 7-12 illustrates a block diagram of the global-chop implementation. V_{OFS} models the combined PGA and ADC internal offset voltage. Only this device-inherent offset voltage is reduced by the global-chop mode. Any offset in the external circuitry connected to the analog inputs is not affected by global-chop mode.

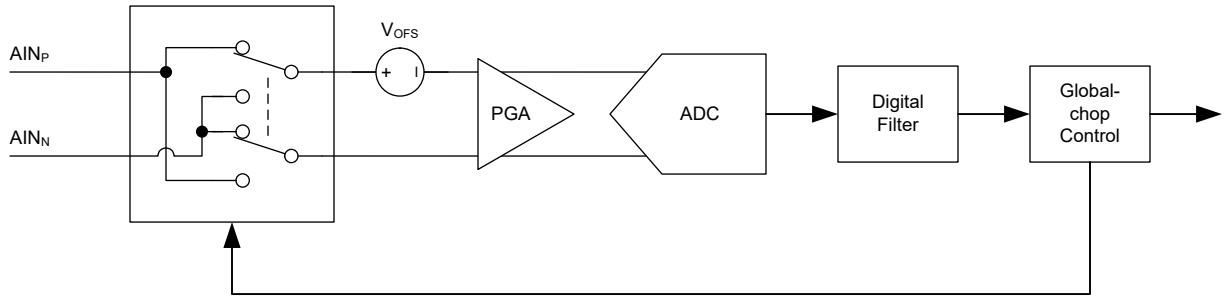


Figure 7-12. Global-Chop Mode Control Diagram

The operational sequence of global-chop mode is as follows:

- Conversion C1: $V_{AINP} – V_{AINN} – V_{OFS}$ → First conversion withheld after conversion start
- Conversion C2: $V_{AINN} – V_{AINP} – V_{OFS}$ → Output 1 = $(V_{C1} – V_{C2}) / 2 = V_{AINP} – V_{AINN}$
- Conversion C3: $V_{AINP} – V_{AINN} – V_{OFS}$ → Output 2 = $(V_{C3} – V_{C2}) / 2 = V_{AINP} – V_{AINN}$
- ...

The first conversion result (Output 1) after a conversion start is available after the device performed two settled conversions. Equation 10 calculates the time required to output the first conversion result after a conversion start.

In continuous-conversion mode with global-chop mode enabled, subsequent conversions complete in t_{GC_DATA}, as calculated by Equation 11.

$$t_{GC\_LATENCY} = 2 \times (t_{DELAY} + t_{LATENCY}) – 12\ t_{MOD} \quad (10)$$

$$t_{GC\_DATA} = t_{DELAY} + t_{LATENCY} – 12\ t_{MOD} \quad (11)$$

Where:

- $t_{LATENCY}$ is the latency time given in Table 7-6 and Table 7-7
- t_{DELAY} is the delay time programmable through the DELAY[3:0] bits

The device waits the programmable delay time after inverting the input polarity before starting the next conversion, to allow for the internal circuitry to settle. In some cases, the programmable delay time must be increased to allow for settling of external components.

Global-chop mode reduces the ADC noise by a factor of $\sqrt{2}$ because two conversions are averaged. Divide the input-referred noise values in Table 6-1 to Table 6-3 by $\sqrt{2}$ to derive the noise performance when global-chop mode is enabled.

The digital filter notches do not change in global-chop mode. However, additional filter notches appear at multiples of $f_{GC\_DATA} / 2$.

7.3.7 Excitation Current Sources (IDACs)

The devices incorporate two programmable, matched current sources (IDAC1 and IDAC2). The current sources provide excitation current to resistive temperature devices (RTDs), thermistors, diodes, and other resistive sensors that require constant current biasing. Each current source is independently programmable to output values between 1µA to 1mA.

Use the I1MAG[3:0] and I2MAG[3:0] bits in combination with the IUNIT bit to set the desired output current for each IDAC. The IUNIT bit sets the base current for both IDAC1 and IDAC2 to either 1µA or 10µA. The I1MAG[3:0] and I2MAG[3:0] bits act as multipliers of that base current to configure the individual IDAC1 and IDAC2 output currents.

Best matching between current sources is achieved when both IDACs are set to the same current value. In three-wire RTD applications, the matched current sources can be used to cancel errors caused by sensor lead resistance (see the *Software-Configurable RTD Measurement Input* section for more details).

Each current source can be routed to any of the analog inputs AINx using the I1MUX[2:0] and I2MUX[2:0] bits. Both current sources can also be combined onto the same pin by setting I1MUX[2:0] and I2MUX[2:0] to the same bit values, if excitation current values up to 2mA are required. Analog inputs AIN3 to AIN7 can be configured as analog inputs, reference inputs, or GPIOs irrespective of the IDAC routing. A pin that is selected as a current source output can still be used as an analog or reference input at the same time. However, note that the IDAC current causes a voltage drop along the internal signal trace of the analog or reference input path which leads to an offset that needs to be taken into consideration. Figure 7-1 shows the IDAC connections through the input multiplexer.

The current sources require voltage headroom to the AVDD supply to operate. This voltage headroom is also called the compliance voltage. When driving resistive loads, take care not to exceed the compliance voltage of

the IDACs, otherwise the specified accuracy of the IDAC current is not always met. For the IDAC compliance voltage specifications, see the *Electrical Characteristics* table.

The IDACs remain active in idle mode, but turn off in standby and power-down mode.

7.3.8 Burn-Out Current Sources (BOCS)

To help detect potential sensor faults, the ADS1x2S14 provide a pair of programmable burn-out current sources (BOCS). Use the BOCS[1:0] bits to enable the current sources and to set the values to 0.2µA, 1µA, or 10µA.

The BOCS connect to the PGA inputs after the internal multiplexer. When enabled, one BOCS sources current from AVDD to the selected positive analog input (AINP) and the other BOCS sinks current from the selected negative analog input (AINN) to GND.

In case of an open-circuit in the external sensor or a sensor wire disconnection, these BOCS pull the positive input toward AVDD and the negative input toward GND, resulting in a full-scale reading. A full-scale reading can also indicate that the sensor is overloaded or that the reference voltage is absent. A near-zero reading can indicate a shorted sensor. Distinguishing a shorted sensor condition from a normal reading can be difficult, especially if an RC filter is used at the inputs. The voltage drop across the external filter resistance and the residual resistance of the internal multiplexer created by the current sources can cause the ADC output to read a value larger than zero.

The ADC readings of a functional sensor can be corrupted when the burn-out current sources are enabled. Therefore, disable the burn-out current sources when performing precision measurements, and only enable the BOCS to test for sensor fault conditions during a dedicated diagnostic measurement.

Disable the BOCS when using global-chop mode (GC_EN = 1b). The burn-out current source function is not compatible with global-chop mode.

The burn-out current sources remain active in idle mode, but turn off in standby and power-down mode.

7.3.9 General Purpose IOs (GPIOs)

The ADS1x2S14 provide four analog inputs (AIN4 to AIN7) that can be configured as general purpose inputs and outputs (GPIOs). The logic levels of those GPIOs are referenced to the AVDD supply. Use the GPIOx_CFG[1:0] (x = 0 to 3) bits to configure the pins as either analog inputs, digital inputs or digital outputs with either push-pull or open-drain characteristic.

Set the digital output levels of the GPIOs using the GPIOx_DAT_OUT bits. The GPIOx_DAT_OUT bit setting has no effect when GPIOx is configured as an analog or digital input.

The GPIOx_DAT_IN bits indicate the readback values at the GPIOx pins irrespective if the pins are configured as digital inputs or outputs. The GPIOx_DAT_IN bits read back 0b when GPIOx is configured as an analog input.

In addition, the following special functions are available:

- GPIO2 can be configured as a $\overline{\text{FAULT}}$ indication output.
- GPIO3 can be configured as a dedicated $\overline{\text{DRDY}}$ output.
- GPIO3 can be configured as an external clock input. See the Clock Source section for details.

7.3.9.1 $\overline{\text{FAULT}}$ Output

Configure GPIO2 as a $\overline{\text{FAULT}}$ output by setting GPIO2_CFG = 10b or 11b and GPIO2_SRC = 1b. The $\overline{\text{FAULT}}$ pin is low when any of the AVDD_UVn, REF_UVn, REG_MAP_CRC_FAULTn, or MEM_FAULTn status bits are 0b to indicate a fault. Connect a pulldown resistor from GPIO2 to GND to also detect potential device resets because the pin reverts back to a high-Z analog input during and after reset.

Use the FAULT_PIN_BEHAVIOR bit to select from the following $\overline{\text{FAULT}}$ output behaviors:

- Static output. The $\overline{\text{FAULT}}$ output is low when a fault occurred, otherwise the output is high.
- Heart beat output. The $\overline{\text{FAULT}}$ output is low when a fault occurred, otherwise the output is a 50% duty-cycle signal with a frequency of f_{MOD} / 256. The heart beat signal frequency can be monitored by the host to detect potential device clock faults.

7.3.9.2 $\overline{\text{DRDY}}$ Output

Configure GPIO3 as a dedicated $\overline{\text{DRDY}}$ output by setting GPIO3_CFG = 10b or 11b and GPIO3_SRC = 1b. A falling edge on the $\overline{\text{DRDY}}$ pin indicates the completion of new conversion data. The $\overline{\text{DRDY}}$ output is always driven even when $\overline{\text{CS}}$ is high. See the $\overline{\text{DRDY}}$ Pin Behavior section for more details.

7.3.10 System Monitors

The devices offer a set of system monitoring functions which can be routed to the PGA inputs internally for measurement through the input multiplexer. Use the SYS_MON[2:0] bits to select from one of the following system monitors:

- The inputs of the PGA can be shorted together to mid-supply, (AVDD / 2), to measure and calibrate the input offset of the internal signal chain.
- An integrated temperature sensor that provides an output signal proportional to the device temperature.
- The attenuated external reference voltage, $(V_{REFP} – V_{REFN}) / 8$.
- The attenuated analog and digital supplies, (AVDD / 8) and (DVDD / 8), respectively.

The AINP[3:0] and AINN[3:0] bits have no effect and the analog inputs are disconnected from the PGA when one of the system monitors is selected. The internal reference with the value set by the REF_VAL bit is automatically selected for SYS_MON[2:0] settings 010b to 101b irrespective of the REF_SEL[1:0] bit setting. Select an appropriate PGA gain setting for the respective measurement.

7.3.10.1 Internal Short (Offset Calibration)

The system monitor offers the option to short both PGA inputs (AINP and AINN) to mid-supply (AVDD / 2). This option can be used to measure and calibrate the device offset by storing the result of the shorted input voltage reading in a microcontroller and consequently subtracting the result from each following reading. Take multiple readings with the inputs shorted and average the result to reduce the effect of noise.

7.3.10.2 Internal Temperature Sensor

The ADS1x2S14 provide an integrated temperature sensors (TS) to measure the die temperature. The temperature sensor outputs a voltage that is proportional to the die temperature. The output voltage characteristic (TS_{Offset}, TS_{TC}) of the temperature sensor is specified in the *Electrical Characteristics* table.

Equation 12 shows how to convert the measured temperature sensor output voltage to die temperature:

$$\text{Die temperature [°C]} = 25°C + (\text{Measured voltage} – TS_{Offset}) / TS_{TC} \quad (12)$$

Select a gain setting for the PGA so that the maximum temperature sensor output voltage that can occur in the application is smaller than V_{REF} / Gain.

7.3.10.3 External Reference Voltage Readback

The system monitor allows to monitor the external voltage reference connected between the REFP and REFN pins. For this purpose, select the attenuated external reference voltage, $(V_{REFP} – V_{REFN}) / 8$ for measurement.

7.3.10.4 Power-Supply Readback

The system monitor allows to monitor both the analog and digital supplies. For this purpose, select either the attenuated analog supply (AVDD / 8) or the attenuated digital supply (DVDD / 8) for measurement.

7.3.11 Monitors and Status Flags

The ADS1x2S14 provide a set of monitors with corresponding status flags to detect and indicate specific device or system faults to the host. Table 7-8 provides an overview of the available monitors. Some monitors need to be enabled using a dedicated monitor enable bit. The monitor fault flags are available in the STATUS_MSB register for readout. If a monitor detects a fault, the according low-active fault flag is set to 0b immediately, even when no conversions are ongoing.

Table 7-8. Monitor Overview

MONITOR NAME	MONITOR ENABLE BIT	MONITOR FAULT FLAG	FAULT FLAG RESET MECHANISM
Reset	N/A	RESETn	Write 1b to clear bit to 1b
AVDD undervoltage	N/A	AVDD_UVn	Write 1b to clear bit to 1b
Reference undervoltage	REV_UV_EN	REF_UVn	Write 1b to clear bit to 1b
SPI CRC	SPI_CRC_EN	SPI_CRC_FAULTn	Updates in every new SPI frame based on the CRC result of the previous SPI frame
Register Map CRC	REG_MAP_CRC_EN	REG_MAP_CRC_FAULTn	Write 1b to clear bit to 1b
Memory Map CRC	N/A	MEM_FAULTn	Reset or power-cycle the device
Register Write Fault	N/A	REG_WRITE_FAULTn	Updates with the next register write command

In addition to the monitors, a data ready indication bit (DRDY) is available in the STATUS_MSB register, and a 4-bit conversion counter in the STATUS_LSB register.

Instead of reading the STATUS_MSB or STATUS_LSB registers on demand using a register read command, the devices can output a STATUS header as the first two bytes of every frame on SDO. Enable the STATUS header transmission using the STATUS_EN bit. The 16-bit STATUS header is a concatenation of the STATUS_MSB[7:0] and STATUS_LSB[7:0] register bits.

7.3.11.1 Reset (RESETn flag)

The RESETn flag indicates if a device reset happened since the last time the bit was cleared to 1b. Write 1b to clear the RESETn bit to 1b.

7.3.11.2 AVDD Undervoltage Monitor (AVDD_UVn flag)

The AVDD undervoltage monitor detects if the analog supply dropped below the AVDD undervoltage threshold (TH_{AVDD_UV}). Write 1b to clear the AVDD_UVn bit to 1b.

The AVDD undervoltage monitor is always active, except in power-down mode. AVDD_UVn sets to 0b when entering power-down mode even when the AVDD supply did not drop below the AVDD undervoltage threshold. The AVDD_UVn bit can set to 0b unintentionally when changing the internal voltage reference value using the REF_VAL bit.

The device does not reset when the analog supply drops below the AVDD threshold as long as the DVDD supply is still present.

7.3.11.3 Reference Undervoltage Monitor (REV_UVn flag)

The reference undervoltage monitor detects if the reference voltage selected by the REF_SEL[1:0] bits dropped below the reference undervoltage threshold (TH_{REF_UV}). Enable the reference undervoltage monitor using the REF_UV_EN bit. However, the reference undervoltage monitor is inactive in standby and power-down mode irrespective of the REF_UV_EN bit setting. The REF_UVn bit can set to 0b unintentionally, when enabling the reference undervoltage monitor, when changing the reference voltage source, or when coming out of power-down or standby mode. Write 1b to clear the REF_UVn bit to 1b.

7.3.11.4 SPI CRC Fault (SPI_CRC_FAULTn flag)

The SPI_CRC_FAULTn flag indicates if a SPI CRC fault occurred on SDI in the previous SPI frame. The execution of the command in the frame where the SPI CRC fault occurred is blocked. Instead, a no operation command is executed. Commands in following frames are not blocked. The SPI_CRC_FAULTn bit updates in every new SPI frame based on the CRC result of the previous SPI frame. Enable the SPI CRC using the

SPI_CRC_EN bit. In addition, enable the transmission of the STATUS header using the STATUS_EN bit to get notified about any SPI CRC faults. See the SPI CRC section for details about the SPI CRC implementation.

7.3.11.5 Register Map CRC Fault (REG_MAP_CRC_FAULTn flag)

The REG_MAP_CRC_FAULTn flag indicates if a register map CRC fault occurred due to an unintended register bit flip. Enable the register map CRC using the REG_MAP_CRC_EN bit. However, the register map CRC stops in standby and power-down mode irrespective of the REG_MAP_CRC_EN bit setting. Write 1b to clear the REG_MAP_CRC_FAULTn bit to 1b. See the Register Map CRC section for details about the register map CRC implementation.

7.3.11.6 Internal Memory Fault (MEM_FAULTn flag)

The MEM_FAULTn flag indicates if a memory map CRC fault occurred. Similar to the register map CRC, the devices use a memory map CRC to check the internal memory for unintended bit changes. Changes to the internal memory bits can cause undetermined device behavior or degraded device performance. The memory map CRC is always enabled, except in standby and power-down mode, and constantly calculates the CRC value across the internal memory map. The devices compare the calculation result against a memory map CRC value that is stored in the memory map in production. If the internal calculation result and the stored memory map CRC value do not match, the MEM_FAULTn flag is set to 0b. No other action is taken by the device in the event of a memory map CRC fault. Perform a power cycle or reset the device when the MEM_FAULTn bit is 0b.

7.3.11.7 Register Write Fault (REG_WRITE_FAULTn flag)

The REG_WRITE_FAULTn flag indicates if a write access to an invalid register address occurred. This flag sets when an invalid register address is written to, and updates at the next register write command. Reading from an invalid register address does not set the flag, but can be detected from the address indication inside the SPI frame of the read command.

7.3.11.8 DRDY Indicator (DRDY bit)

The DRDY bit is the inverse of the $\overline{\text{DRDY}}$ pin. Enable the transmission of the STATUS header using the STATUS_EN bit to leverage the DRDY bit indication. The DRDY bit indicates if the conversion data read within the current SPI frame are new or are repeated data from the last read operation. Polling the DRDY bit using the register read command is not reliable, because the DRDY bit returns to 0b during the first frame of the read register command transmission already.

7.3.11.9 Conversion Counter (CONV_COUNT[3:0])

The conversion counter (CONV_COUNT[3:0]) increments every time a new conversion completes. After reaching a counter value of Fh, the counter rolls over to 0h with the completion of the next conversion. Reset the counter to Fh by putting the device into power-down mode or by resetting the device. At the completion of the first conversion after reset or power down, the counter reads 0h.

When the conversion counter is output as part of the STATUS header (STATUS_EN = 1b), the devices make sure that the conversion counter value always matches to the ADC conversion result that is output in the same SPI frame.

7.4 Device Functional Modes

7.4.1 Power-up and Reset

The ADS1x2S14 is reset in one of three ways:

- Power-on reset (POR)
- Writing to the RESET[5:0] bit field (software reset)
- Sending the SPI reset pattern (software reset)

After a reset occurs, the user registers reset to the respective default settings and the device is in idle mode; no conversions are started. SPI communication with the device is possible after the reset process completes. See the *Timing Requirements* for timing specifications to consider after the various reset events before starting communication with the device.

The RESETn bit indicates if a reset occurred since the last time the RESETn bit was cleared to 1b. Clear the RESETn bit to 1b right after a device reset to get notified of unintended device resets during operation.

7.4.1.1 Power-On Reset (POR)

A power-on reset (POR) circuit holds the device in reset until the DVDD supply exceeds the DVDD POR threshold (TH_{DVDD_POR}). The power-on reset also ensures that the device starts operating in a known good state in case a brown-out event occurred, where the DVDD supply dipped below the DVDD POR threshold. An undervoltage event on AVDD does not cause a device reset, but is indicated by the AVDD_UVn flag.

7.4.1.2 Reset by Register Write

Initiate a software reset by writing 010110b to the RESET[5:0] bit field. Writing any other value to this bit field does not result in reset. In 4-wire SPI mode, reset takes effect at the end of the frame at the time $\overline{CS}$ is taken high. In 3-wire SPI mode, reset takes effect on the last SCLK falling edge of the register write operation. Reset in 3-wire SPI mode requires that the SPI is synchronized to the SPI host. If SPI synchronization is not assured, use the pattern described in the *Reset by SPI Input Pattern* section to reset the device.

7.4.1.3 Reset by SPI Input Pattern

The device is also reset through SPI operation by inputting a special bit pattern on SDI. The input pattern does not follow the regular SPI command format. Two input patterns are available to reset the ADC.

Pattern 1 consists of a *minimum* 1023 consecutive ones followed by one zero. The device resets on the falling edge of SCLK when the final zero is shifted in. This pattern can be used in either 3- or 4-wire SPI mode. Figure 7-13 shows a pattern 1 reset example.

Reset pattern 2 is only for use with 4-wire SPI mode. To reset, input a *minimum* of 1024 consecutive ones (no ending zero value), followed by taking $\overline{CS}$ high at which time the reset occurs. Use pattern 2 when multiple devices are connected in a daisy-chain. Figure 7-14 shows a pattern 2 reset example.

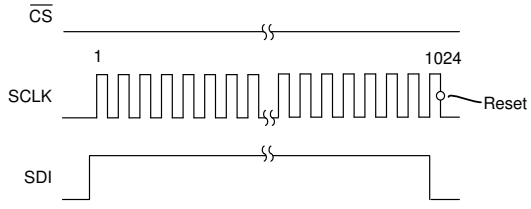


Figure 7-13. Reset Pattern 1 (3-Wire or 4-Wire SPI Mode)

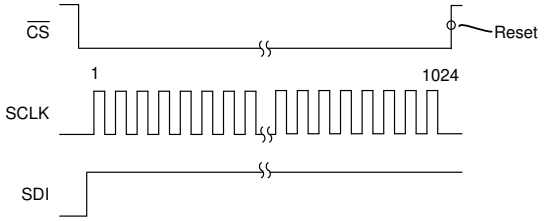


Figure 7-14. Reset Pattern 2 (4-Wire SPI Mode)

7.4.2 Operating Modes

The ADS1x2S14 offer four operating modes: power-scalable conversion mode, standby, idle, and power-down mode. Figure 7-15 shows how the device transitions between the different operating modes.

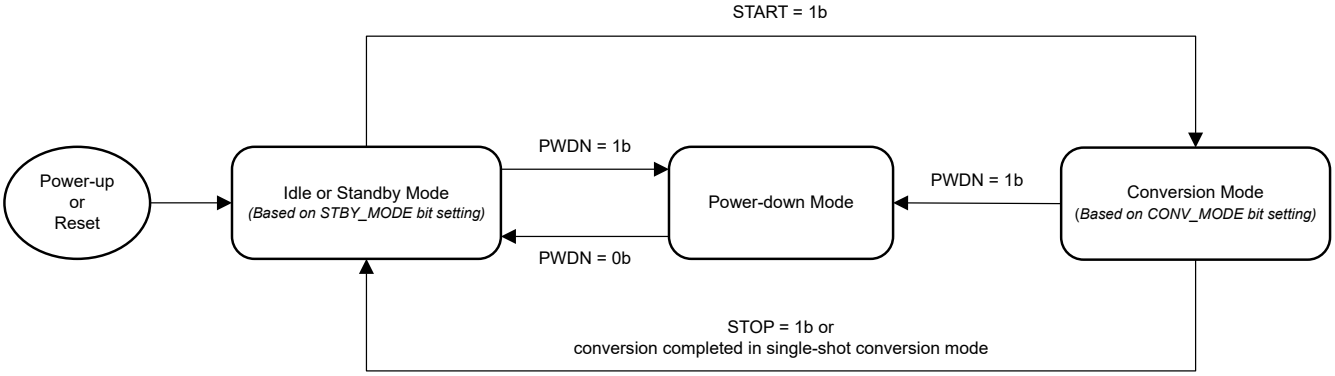


Figure 7-15. Operating Mode State Diagram

7.4.2.1 Idle and Standby Mode

After reset, the device is in idle mode. All analog circuitry is powered up, based on the respective register bit settings, but no conversions are ongoing, and the digital filter is held in reset.

In standby mode, the ADC, PGA, IDACs, BOCS, reference buffers, reference undervoltage monitor, register map CRC, and memory map CRC power down, irrespective of the register bit settings. The internal voltage reference and oscillator stay powered-up in standby mode.

Setting the START bit to 1b, exits idle or standby mode and starts conversions. When conversions stop, the device transitions to either idle or standby mode depending on the STBY_MODE bit setting.

Use standby mode to save power when conversions stop. When starting conversions from standby mode, the latency time for the first conversion is longer compared to the latency time when starting conversions from idle mode as explained in the Digital Filter Latency section.

7.4.2.2 Power-Down Mode

In power-down mode, all analog and digital circuitry are powered off, except for circuitry which is required to retain the user register settings. SPI communication is still possible. Setting the PWDN bit to 1b powers the device down immediately; any ongoing conversions are aborted. In power-down mode, the conversion counter (CONV_COUNT[3:0]) resets to Fh, the conversion data clears, and the START bit is ignored.

Any analog inputs configured as GPIO digital outputs transition into a Hi-Z state in power-down mode. To maintain a certain GPIO logic level during power-down, consider external pullup or pulldown resistors on the respective GPIO pins.

Allow the internal voltage reference to start up and settle when coming out of power-down mode before starting any conversions.

7.4.2.3 Power-Scalable Conversion Modes

The ADS1x2S14 offer two conversion modes: continuous-conversion and single-shot conversion mode. The CONV_MODE bit selects the conversion mode.

In addition, the devices offer four speed modes to trade off power consumption, resolution, and data rate. Each speed mode corresponds to a specific modulator clock frequency and device bias current setting. Speed mode 3 (f_{MOD} = 1.024MHz) offers the highest data rates (up to 64kSPS) and the lowest noise at the 20SPS data rate setting. In contrast, speed mode 0 (f_{MOD} = 32kHz) minimizes power consumption at the expense of noise performance. Select the speed mode using the SPEED_MODE[1:0] bits based on the desired data rate, resolution, and device power consumption requirements.

7.4.2.3.1 Continuous-Conversion Mode

In continuous-conversion mode, the ADC converts indefinitely until stopped by the user. Set the START bit to 1b to start conversions. Setting the START bit to 1b while conversions are ongoing aborts the ongoing conversion and restarts conversions.

Use the STOP bit to stop conversions. The currently ongoing conversion is allowed to finish after the STOP bit is set to 1b. After setting the STOP bit, the STOP bit reads back 1b until conversions are stopped. When conversions stopped, the STOP bit reads back 0b to indicate the device transitioned to idle or standby mode.

Writing 1b to both the START and STOP bits at the same time has no effect.

The last conversion result is still available for readout after conversions stopped. The conversion results only clear after a device reset, in power-down mode, or are overwritten when a new conversion result becomes available.

The START bit takes effect at the $\overline{CS}$ rising edge (4-wire SPI mode), or the last SCLK falling edge (3-wire SPI mode) of the SPI frame where the CONVERSION_CTRL register is written. See the *Write Register Command* section for details on the SPI frame of a register write command.

If $\overline{DRDY}$ is low, setting the START bit drives the $\overline{DRDY}$ pin high, however the old conversion data can still be read until the new conversions become available.

When conversions are started or restarted using the START bit, the device hides unsettled conversions and only provides a settled conversion result after the conversion latency period ($t_{LATENCY}$) plus the optional delay time (t_{DELAY}) as shown in Digital Filter Settling Time and Conversion Period. All subsequent conversions have a conversion period of $t_{DATA} = 1 / f_{DATA} = OSR / f_{MOD}$.

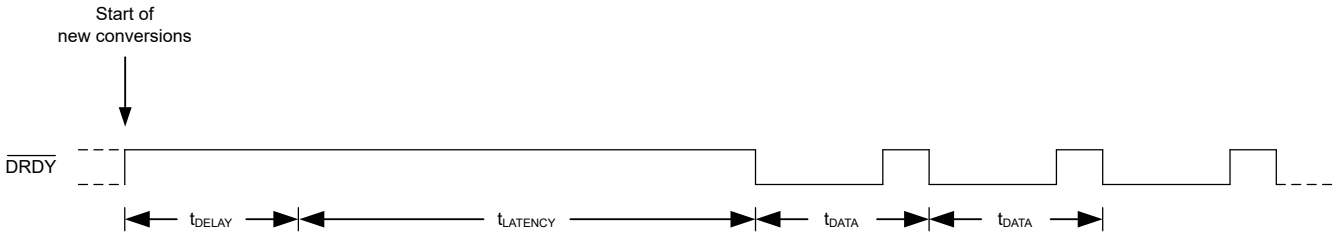


Figure 7-16. Digital Filter Settling Time and Conversion Period

7.4.2.3.2 Single-shot Conversion Mode

In single-shot conversion mode, the ADC performs one single conversion after the START bit is set to 1b. Setting the START bit while a conversion is ongoing aborts the ongoing conversion and restarts a single new conversion. The STOP bit has no effect in single-shot conversion mode.

Equivalent to continuous-conversion mode, the START bits takes affect at the $\overline{CS}$ rising edge (4-wire SPI mode), or the last SCLK falling edge (3-wire SPI mode) of the SPI frame where the CONVERSION_CTRL register is written. See the *Write Register Command* section for details on the SPI frame of a register write command.

Every conversion in single-shot conversion mode is available after the conversion latency period ($t_{LATENCY}$) plus the optional delay time. If an input step change occurs during the conversion process, the conversion result is not always fully settled. Another subsequent single-shot conversion is required in that case to output a settled conversion result.

7.5 Programming

7.5.1 Serial Interface (SPI)

The serial interface is used to read conversion data, configure device registers, and control ADC conversions.

The serial interface consists of four lines: $\overline{CS}$, SCLK, SDI, and SDO/$\overline{DRDY}$. In addition, GPIO3 can be configured as a dedicated $\overline{DRDY}$ output pin. The host always drives SCLK and the device acts as a peripheral. The interface only supports the SPI configuration (CPOL = 0 and CPHA = 1), where SCLK idles low, and data update on SCLK rising edges and are latched on SCLK falling edges.

The interface supports full-duplex operation, meaning input data and output data can be transmitted simultaneously. The interface also supports daisy-chain connection of multiple ADCs.

7.5.2 Serial Interface Signals

7.5.2.1 Chip Select ($\overline{CS}$)

$\overline{CS}$ is an active-low input that enables the interface for communication. A communication frame starts by taking $\overline{CS}$ low and ends by taking $\overline{CS}$ high. When $\overline{CS}$ is taken high, the device ends the frame by interpreting the last 16 bits of input data (24 bits when SPI CRC is enabled) regardless of the total number of bits shifted in. When $\overline{CS}$ is high, the SPI resets, commands are blocked, and SDO/$\overline{DRDY}$ enters a high-impedance state. The dedicated $\overline{DRDY}$ pin, when GPIO3 is configured as $\overline{DRDY}$ output, is an active output regardless of the state of $\overline{CS}$. $\overline{CS}$ can be tied low to operate the interface in 3-wire SPI mode.

7.5.2.2 Serial Clock (SCLK)

SCLK is the serial clock input used to shift data into and out of the ADC. Data on SDO update on the rising edge of SCLK and data on SDI are latched on the falling edge of SCLK. SCLK is a Schmitt-triggered input designed to increase noise immunity. Even though SCLK is noise resistant, keep SCLK as noise-free as possible to avoid unintentional SCLK transitions. Avoid ringing and overshoot on the SCLK input. A series termination resistor at the SCLK driver can reduce ringing.

7.5.2.3 Serial Data Input (SDI)

SDI is the serial interface data input. SDI is used to input data to the device. Input data are latched on the falling edge of SCLK. Idle SDI high or low when not active.

7.5.2.4 Serial Data Output/Data Ready (SDO/$\overline{DRDY}$)

SDO/$\overline{DRDY}$ is a dual-function output pin. This pin is programmable to provide output data only, or to provide output data and the data-ready indication. The SDO_MODE bit selects the mode. The dual-function mode multiplexes output data and data-ready operations on a single pin. This mode can replace the function of the dedicated $\overline{DRDY}$ pin to reduce the number of SPI I/O lines required to interface to the host.

Output data update on the rising edge of SCLK. The SDO/$\overline{DRDY}$ pin is in a high-impedance state when $\overline{CS}$ is high.

When programmed to dual-function mode (SDO_MODE = 1b) and when $\overline{CS}$ is low, SDO/$\overline{DRDY}$ mirrors $\overline{DRDY}$ until the first rising edge of SCLK, at which time the pin changes mode to provide data output. When the data read operation is complete, the pin reverts back to mirroring $\overline{DRDY}$. Figure 7-17 illustrates the behavior of the SDO/$\overline{DRDY}$ pin.

In output data only mode (SDO_MODE = 0b), SDO stays at the level of the last bit sent if the host does not send any extra SCLK pulses after the last data is shifted out on SDO, as shown in Figure 7-17.

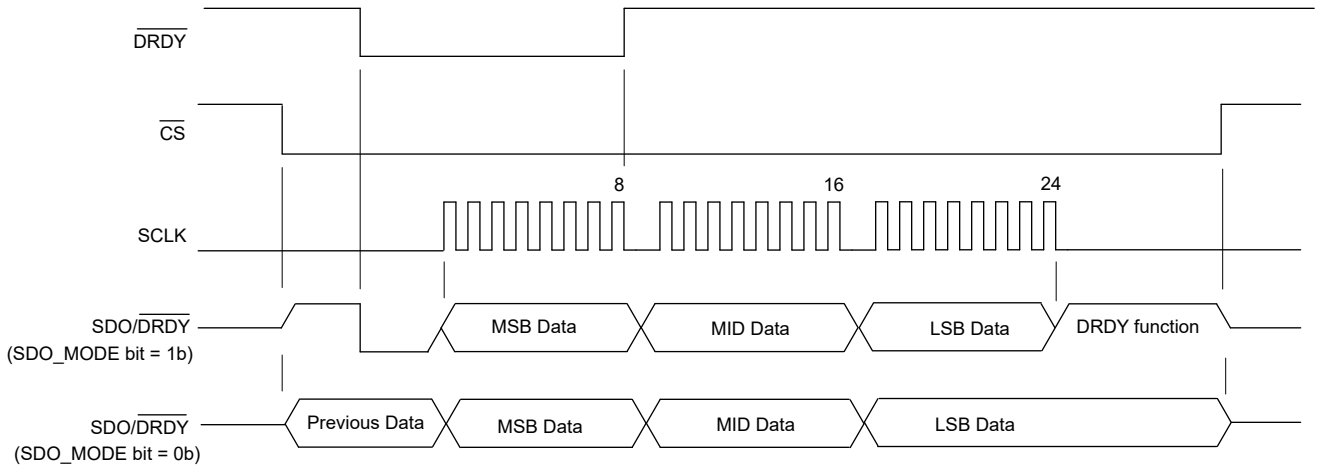


Figure 7-17. SDO/DRDY and DRDY Behavior (24-bit Device, STATUS header and CRC disabled)

7.5.2.5 Data Ready (DRDY) Pin

GPIO3 can be configured as a dedicated DRDY output pin (GPIO3_CFG[1:0] = 10b or 11b, GPIO3_SRC = 1b). DRDY is an active output whether CS is high or low.

DRDY drives high when conversions are started, and drives low when conversion data are ready. DRDY drives back high at the eighth SCLK falling edge of the MSB conversion data read as shown in Figure 7-17. If conversion data are not read, DRDY pulses high $t_{W(DRH)}$ before the next falling edge. Whenever the device is programmed to enter standby mode (STBY_MODE bit = 1b) after conversions stopped, DRDY is driven back high 4 t_{MOD} after transitioning low.

See the *DRDY Pin Behavior* section for further details on the DRDY pin operation.

7.5.3 Serial Interface Communication Structure

7.5.3.1 SPI Frame

Communication through the serial interface is based on the concept of frames. A frame consists of a prescribed number of SCLKs required to shift data in on SDI, or out on SDO. A frame starts by taking $\overline{CS}$ low and ends by taking $\overline{CS}$ high. When $\overline{CS}$ is taken high, the device interprets the last 16 bits (or 24 bits when SPI CRC is enabled) of input data regardless of the amount of data shifted into the device.

The interface is full duplex, meaning that the interface is capable of transmitting data on SDO while simultaneously receiving data on SDI. Typically, the input frame is sized to match the output frame by padding the frame with leading zeros if needed. However, if only writing to the device while ignoring the data on SDO, the frame can be shortened to the minimum size of 16 bits (or 24 bits when SPI CRC is enabled). Figure 7-18 and Figure 7-19 show typical communication frame structures for the 16-bit and 24-bit devices, respectively. In these examples, conversion data are shifted out on SDO. As illustrated, command bytes on SDI (plus the optional CRC-IN byte) are always right aligned within a frame. Data bytes on SDO (plus the optional STATUS header and CRC-OUT byte) are always left aligned within a frame.

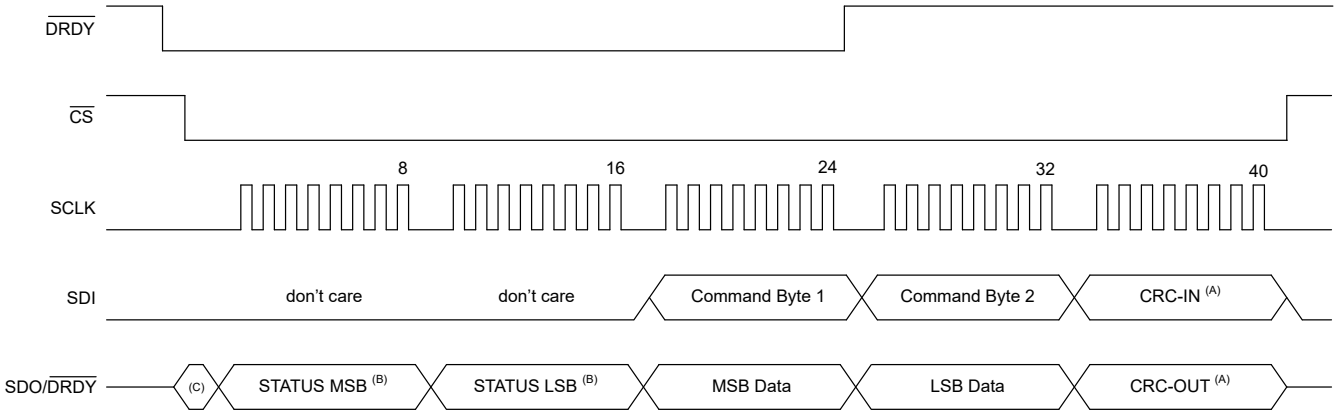
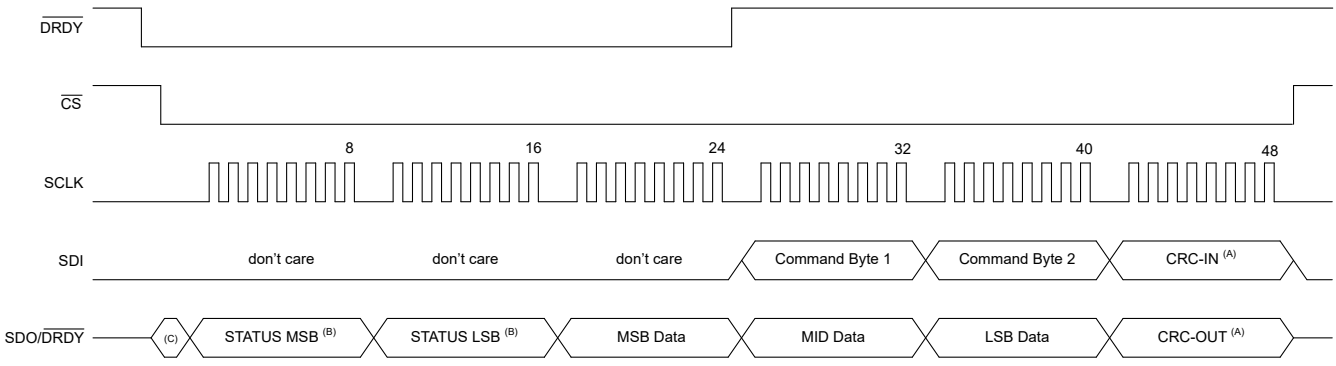


Figure 7-18. Typical Communication Frame (16-Bit Device)



A. Optional CRC byte. If CRC is disabled, the frame shortens by one byte.
B. Optional STATUS header. If STATUS is disabled, the frame shortens by two bytes.
C. If SDO_MODE = 0b, the previous state of SDO/$\overline{DRDY}$ remains until the first SCLK rising edge. Otherwise, SDO/$\overline{DRDY}$ follows $\overline{DRDY}$.

Figure 7-19. Typical Communication Frame (24-Bit Device)

The output frame size, as given in Table 7-9, depends on the data resolution (16 or 24 bits), the optional STATUS header (two bytes), and the optional CRC byte.

Table 7-9. Output Frame Size

RESOLUTION	STATUS HEADER	CRC BYTE	FRAME SIZE
16 bit	No	No	16 bit
16 bit	No	Yes	24 bit
16 bit	Yes	No	32 bit
16 bit	Yes	Yes	40 bit
24 bit	No	No	24 bit
24 bit	No	Yes	32 bit
24 bit	Yes	No	40 bit
24 bit	Yes	Yes	48 bit

In 4-wire SPI mode, when extending the frame beyond the frame size given in Table 7-9, the device starts shifting out data on SDO which was shifted in on SDI at the beginning of the frame. This behavior is to support daisy-chain operation as explained in the *Daisy-Chain Operation* section.

A continuous-read mode is available in 4-wire SPI mode, where an arbitrary number of register data can be retrieved without any transitions of $\overline{CS}$, and the frame extends to accommodate the additional data. See the *Continuous-Read Mode* section for details. In continuous-read mode, the output frame size is unlimited.

In 3-wire SPI mode, the input frame must match the size of the output frame as given in Table 7-9 for the SPI to remain synchronized. See the *3-Wire SPI Mode* section for details.

7.5.3.2 STATUS Header

The ADS1x2S14 output an optional STATUS header as the first two bytes of every frame on SDO. Enable the STATUS header transmission using the STATUS_EN bit. The 16-bit STATUS header is a concatenation of the STATUS_MSB[7:0] and STATUS_LSB[7:0] register bits. The fault flags, DRDY bit, GPIO input data, and the conversion counter are all part of these bits. See the Monitors and Status Flags section and the respective register bit descriptions in the *Registers* section for details.

7.5.3.3 SPI CRC

The SPI cyclic redundancy check (CRC) is a check code used to detect transmission errors to and from the host controller. A CRC-IN byte is transmitted with the ADC input data by the host on SDI and a CRC-OUT byte is transmitted with the output data by the device on SDO. Use the SPI_CRC_EN bit to enable the SPI CRC. In addition, enable the transmission of the STATUS header using the STATUS_EN bit to get notified about any SPI input CRC faults.

The CRC-IN code is calculated by the host over the two command bytes. Any input bytes padded to the start of the frame are not included in the CRC-IN calculation. The ADC checks the input command CRC-IN code against an internal code calculated over the two received input command bytes. If the CRC-IN codes do not match, the command is not executed and the SPI_CRC_FAULTn bit is set to 0b.

The SPI_CRC_FAULTn bit is output as part of the STATUS header to provide immediate indication that a CRC error occurred in the previous frame. The SPI_CRC_FAULTn bit clears automatically in the next SPI frame, assuming no SPI CRC error occurred in the current frame.

The number of bytes used to calculate the output CRC code depends on the amount of data bytes transmitted in the frame on SDO. Table 7-10 shows the number of bytes included in the output CRC calculation.

Table 7-10. Data Covered by Output CRC

ACTION	DEVICE RESOLUTION	STATUS HEADER ENABLED	BYTE COUNT	DATA COVERD BY OUTPUT CRC
Conversion data read	16 bit	No	2	16 bits of conversion data
Conversion data read	16 bit	Yes	4	16 bits STATUS header + 16 bits of conversion data
Register data read	16 bit	No	2	8 bits of register data + 8 bits address byte
Register data read	16 bit	Yes	4	16 bits STATUS header + 8 bits of register data + 8 bits address byte
Conversion data read	24 bit	No	3	24 bits of conversion data
Conversion data read	24 bit	Yes	5	16 bits STATUS header + 24 bits of conversion data
Register data read	24 bit	No	3	8 bits of register data + 8 bits address byte + 8 bits of 00h padding
Register data read	24 bit	Yes	5	16 bits STATUS header + 8 bits of register data + 8 bits address byte + 8 bits of 00h padding

The CRC code calculation is the 8-bit remainder of the bitwise exclusive-OR (XOR) operation of the variable length argument with the CRC polynomial. The CRC is based on the CRC-8-ATM (HEC) polynomial: $X^8 + X^2 + X^1 + 1$. The nine coefficients of the polynomial are: 100000111. The CRC calculation is initialized to all 1s to detect errors in the event that SDI and SDO/$\overline{\text{DRDY}}$ are either stuck high or low.

Figure 7-20 shows a visual representation of the CRC calculation. The following procedure calculates the CRC value:

- Preload the 8-bit shift register, which has XOR blocks located at positions that correspond to the CRC polynomial (07h), with the seed value of FFh.
- Shift in all data bits starting with the most-significant bit (MSB) and re-compute the shift-register value after each bit.
- The resulting shift-register value after all data bits have been shifted in is the computed CRC value.

The example C code available for download *here* includes a potential CRC implementation.

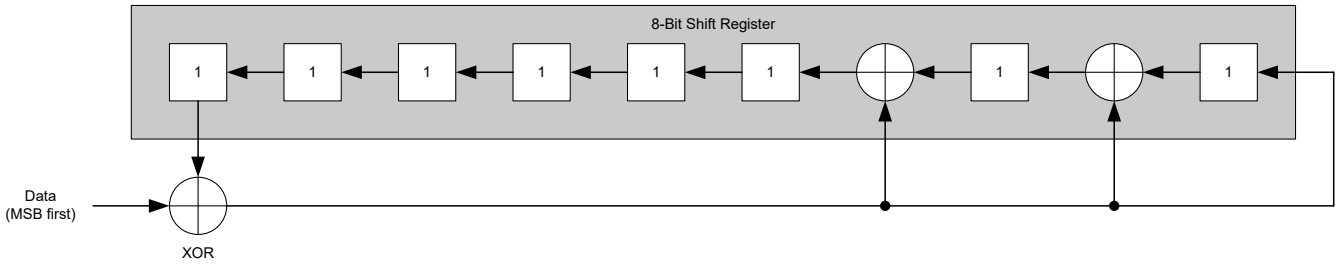


Figure 7-20. Visual Representation of CRC Calculation

7.5.4 Device Commands

Commands are used to read and write register data. The register map consists of a series of one-byte (8 bit) registers, accessible by read and write operations. The minimum frame length of the input command sequence is 16 bit (24 bit when SPI CRC is enabled). If desired, the input command sequence can be padded with leading zeros to match the length of the output data frame. When the SPI CRC is enabled, the device interprets the two bytes preceding the CRC-IN byte at the end of the frame as the command bytes. Table 7-11 shows the ADS1x2S14 commands.

Table 7-11. SPI Commands

DESCRIPTION	BYTE 1	BYTE 2	BYTE 3 (Optional CRC-IN Byte)
No operation (read conversion data)	00h	00h	D7h
Read register command	40h + address [3:0]	Don't care	CRC-IN of byte 1 and byte 2
Write register command	80h + address [3:0]	Register data	CRC -IN of byte 1 and byte 2

The device supports special extended-length bit patterns that are longer than the standard command length. These patterns are used to reset the ADC and to reset the frame in 3-wire SPI mode. The extended bit patterns are explained in the *Reset by SPI Input Pattern* and *3-Wire SPI Mode* sections.

The instance where the commands are latched by the device depend on the SPI mode:

- 4-wire SPI mode: The rising edge of $\overline{CS}$
- 3-wire SPI mode: The last SCLK falling edge of the SPI frame (including the CRC-OUT byte in CRC mode)

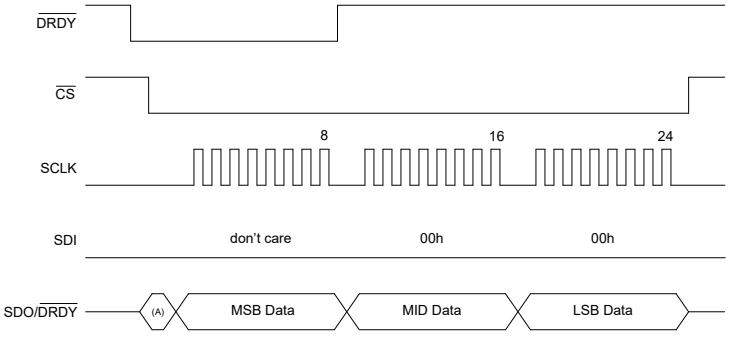
7.5.4.1 No Operation (Read Conversion Data)

The no-operation command bytes are 00h and 00h. Use this command to read conversion data when not sending a read or write register command at the same time. If the SPI CRC check is enabled, the CRC byte is required (byte 3), which is always D7h for bytes 00h and 00h. SDI can be held low during data readback, but in CRC mode the SPI_CRC_FAULTn bit sets to 0b. The SPI_CRC_FAULTn flag can be ignored while reading conversion data, and is updated in every new SPI frame.

Conversion data are buffered, which allows data to be read up to one f_{MOD} clock cycle before the next $\overline{DRDY}$ falling edge. Conversion data can be read multiple times until the next conversion data are ready, and are never corrupted. Register data replace the conversion data if the register read command is sent in the previous frame.

$\overline{DRDY}$ is driven back high at the eighth SCLK falling edge during conversion data read, that is when the transmission of the conversion data MSB byte is complete.

Figure 7-21 shows an example of reading 24-bit conversion data with the STATUS header and CRC byte disabled.



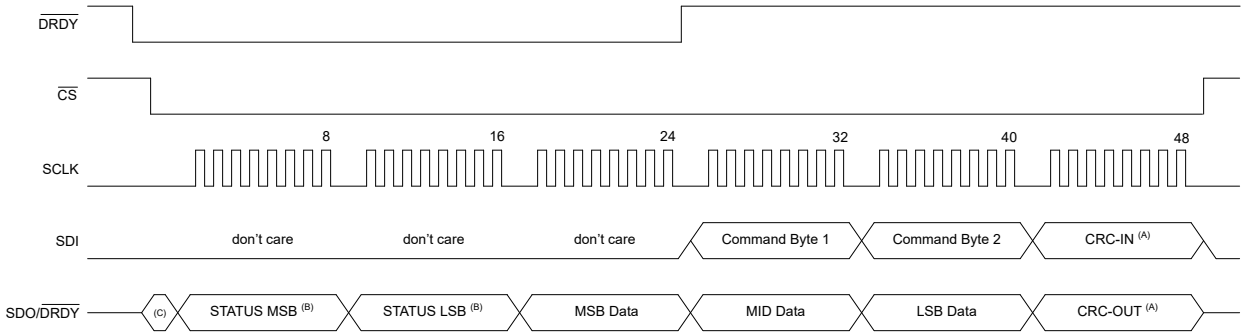
A. If SDO_MODE = 0b, the previous state of SDO/$\overline{DRDY}$ remains until the first SCLK rising edge. Otherwise, SDO/$\overline{DRDY}$ follows $\overline{DRDY}$.

Figure 7-21. Read Conversion Data (24-Bit Device, STATUS Header and CRC Disabled)

Figure 7-22 is an example of a read conversion data operation when the STATUS header and the CRC byte are enabled. This example also shows the optional use of a full-duplex transmission when a command is input at

the same time the conversion data are output. If no input command is desired, the input bytes are 00h, 00h, and D7h. The output CRC (CRC-OUT) code computation includes the STATUS header.

$\overline{\text{DRDY}}$ is driven back high at the 24th SCLK falling edge, when the transmission of the conversion data MSB byte is complete. This is also true if the data is not completely read, that is if the read operation is stopped any time after the transmission of the conversion data MSB byte, but before the end of the frame.



A. Optional CRC byte. If CRC is disabled, the frame shortens by one byte.
B. Optional STATUS header. If STATUS is disabled, the frame shortens by two bytes.
C. If SDO_MODE = 0b, the previous state of SDO/$\overline{\text{DRDY}}$ remains until the first SCLK rising edge. Otherwise, SDO/$\overline{\text{DRDY}}$ follows $\overline{\text{DRDY}}$.

Figure 7-22. Read Conversion Data (24-Bit Device, STATUS Header and CRC Enabled)

Conversion data can be read asynchronous to $\overline{\text{DRDY}}$. However, when conversion data are read close to the $\overline{\text{DRDY}}$ falling edge, there is uncertainty whether previous data or new data are output. If the SCLK shift operation starts at least one f_{MOD} clock cycle before the $\overline{\text{DRDY}}$ falling edge, then old data are provided. If the shift operation starts at least one f_{MOD} clock cycle *after* $\overline{\text{DRDY}}$, then new data are output. In either case, data are not corrupted. When the STATUS header transmission is enabled, the DRDY bit indicates if the data transmitted in the current frame are old (previously read data, DRDY = 0b) or new (DRDY = 1b).

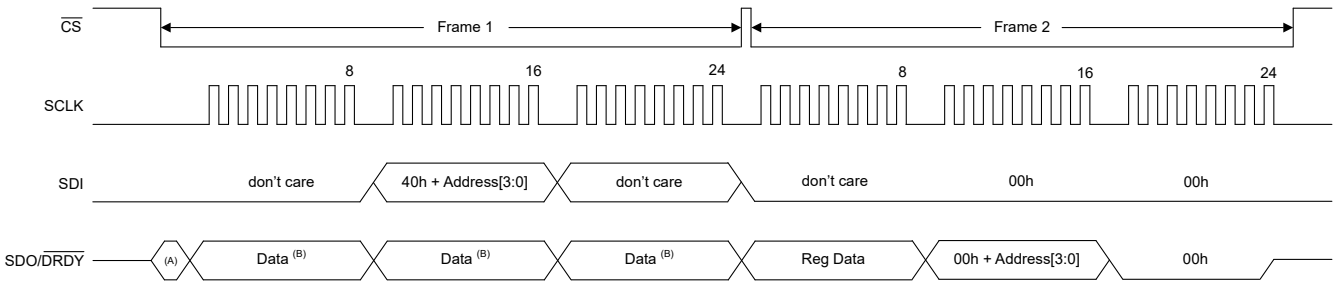
7.5.4.2 Read Register Command

Use the read register command to read register data. The command follows a two-frame protocol in which the read command is sent in one frame and the ADC responds with register data in the next frame. The first byte of the command is the base command value (40h) added to the 4-bit register address. The value of the second command byte is arbitrary, but is used together with the first byte for the CRC calculation.

Figure 7-23 shows an example of reading register data for the 24-bit device with the STATUS header and CRC disabled. Frame 1 is the command frame and frame 2 is the data response frame. The frames are delimited by taking $\overline{\text{CS}}$ high. The data response frame returns the requested register data byte, followed by the register address indication byte, and a 00h padded byte to complete the 24-bit frame. The register data is most-significant-bit first aligned. The 4-bit register address is right-aligned within the register address indication byte (padded with 0000b at the MSB position). If desired, the data response frame can be shortened after the register data byte by taking $\overline{\text{CS}}$ high.

Reading from a register address outside the valid address range returns 00h as the register data and FFh in the register address indication byte to indicate an error.

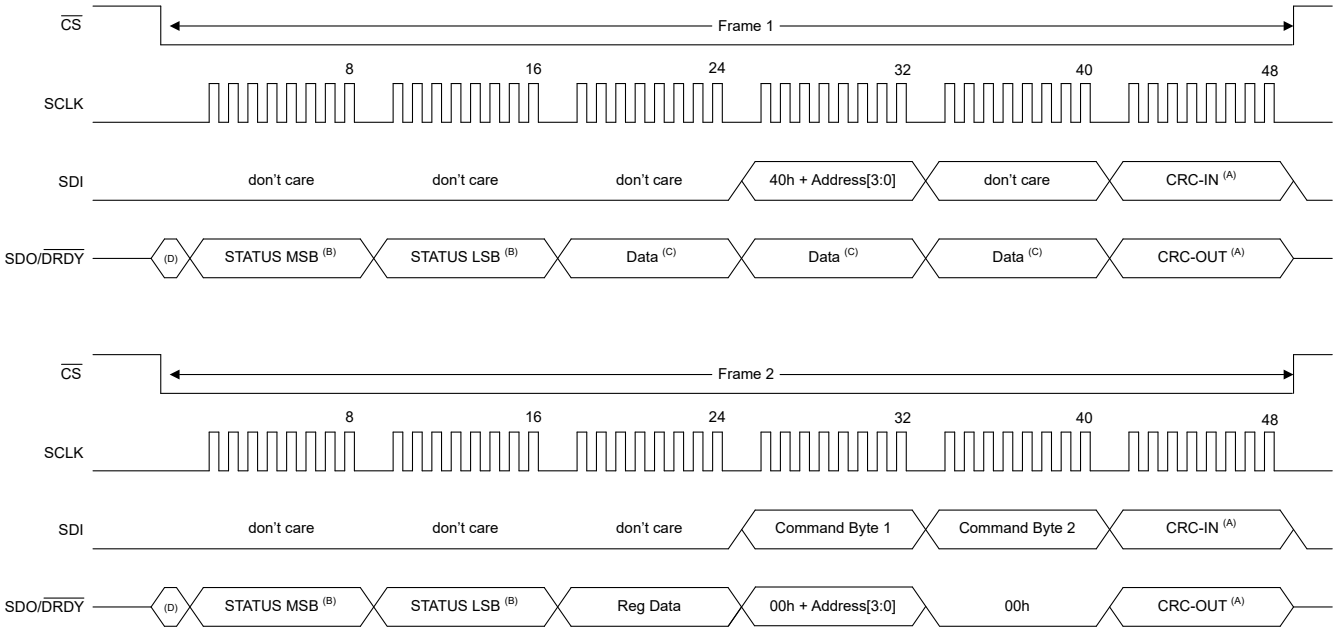
When reading multiple registers, full-duplex operation can be used to double the throughput of the read register operations by inputting the next read register command during the data response frame of the previous register.



A. Previous state of SDO/$\overline{\text{DRDY}}$ before first SCLK.
B. Data are either 24 bits of conversion data, or if the read register command is sent in the prior frame, the data field is the register data byte + address indication byte + 00h padding.

Figure 7-23. Read Register Data (24-Bit Device, STATUS Header and CRC Disabled)

Figure 7-24 shows an example of a register read operation for the 24-bit device with the STATUS header and CRC enabled. In frame 1, conversion data are output at the same time as the read register command is input (when the previous frame is not a read register command). The input command is padded with three don't care bytes to match the length of the output data frame. The padded input bytes are excluded from the CRC-IN code calculation. Frame 2 shows the input of the next command concurrent with the output of the requested register data. The CRC-OUT code includes all preceding bytes within the data output frame.



A. Optional CRC byte. If CRC is disabled, the frame shortens by one byte.
B. Optional STATUS header. If STATUS is disabled, the frame shortens by two bytes.
C. Depending on the previous operation, the data field is either conversion data or the register data byte + address indication byte + 00h padding.
D. Previous state of SDO/$\overline{\text{DRDY}}$ before the first SCLK.

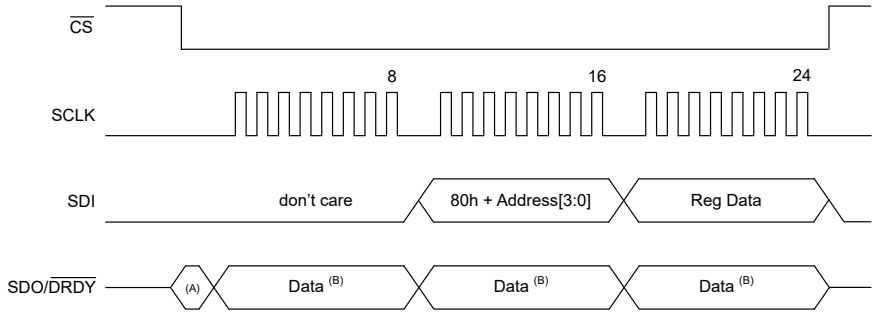
Figure 7-24. Read Register Data (24-Bit Device, STATUS Header and CRC Enabled)

7.5.4.3 Write Register Command

Use the write register command to write register data. The write register operation is performed in a single frame. The first byte of the command is the base value (80h) added to the 4-bit register address. The second byte of the command is the register data.

Writing to registers outside the valid address range is ignored and the REG_WRITE_FAULTn bit is set to 0b to indicate an error.

Figure 7-25 shows an example of a register write operation for the 24-bit device with the STATUS header and CRC disabled. A shortened 16-bit frame can be used to increase throughput if a series of registers need to be configured without reading out conversion data at the same time. Shortened SPI frames cannot be used in 3-wire SPI mode or when operating the device in a daisy-chain.

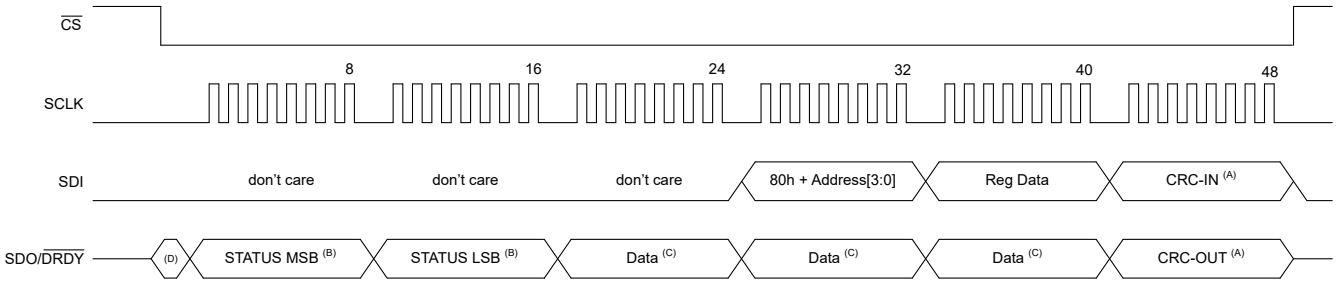


A. Previous state of SDO/DRDY before the first SCLK.
B. Data are either the conversion data, or if the read register command was sent in a prior frame, the data field is register data byte + address indication byte + 00h padding.

Figure 7-25. Write Register Data (24-Bit Device, STATUS Header and CRC Disabled)

Figure 7-26 shows an example of a write register operation for the 24-bit device with the STATUS header and CRC enabled. Full-duplex operation is also illustrated to show simultaneous input of a command and output of conversion data. The input frame is prefixed with three *don't care* bytes to match the output frame so all conversion data bytes are transmitted. A shortened 24-bit frame can be used to increase throughput if a series of registers need to be configured without reading out conversion data at the same time.

Verify successful register write operations by either reading back the register data, or by checking the SPI_CRC_FAULTn bit for input CRC errors. If an SPI CRC input error occurred, the SPI_CRC_FAULTn flag reads 0b in the following frame and the write operation is ignored.



A. Optional CRC byte. If CRC is disabled, the frame shortens by one byte.
B. Optional STATUS header. If STATUS is disabled, the frame shortens by two bytes.
C. The data field is either conversion data, or if the read register command was sent in the prior frame, register data byte + address indication byte + 00h padding.
D. Previous state of SDO/DRDY before the first SCLK.

Figure 7-26. Write Register Data (24-Bit Device, STATUS Header and CRC Enabled)

Writing to the following registers (even the same value) stops any ongoing conversion, resets the digital filter and restarts conversions using the updated device configurations:

- DEVICE_CFG (address 05h)
- DATA_RATE_CFG (address 06h)
- MUX_CFG (address 07h)
- GAIN_CFG (address 08h)
- REFERENCE_CFG (address 09h)
- DIGITAL_CFG (address 0Ah)

This device behavior does for example help when multiplexing through multiple channels with the smallest amount of communication overhead. For that purpose, operate the device in continuous-conversion mode. Start conversions on the first measurement channel using the START bit. After the conversion completes, write a new multiplexer configuration to the MUX_CFG register to select the second channel for measurement. While writing the MUX_CFG register, read the conversion data of the first measurement channel at the same time. The device starts converting on the second measurement channel after the write register command is latched by the device.

When the device is in standby or idle mode, then writing to the above mentioned registers does not start conversions.

7.5.5 Continuous-Read Mode

The ADS1x2S14 offer a continuous-read mode. In continuous-read mode, an arbitrary number of register data can be retrieved without any transitions of $\overline{CS}$, and the frame extends to accommodate the additional data. This simplifies the process of reading a large amount of register data, and reduces the overhead on the microcontroller peripheral which controls the $\overline{CS}$ line.

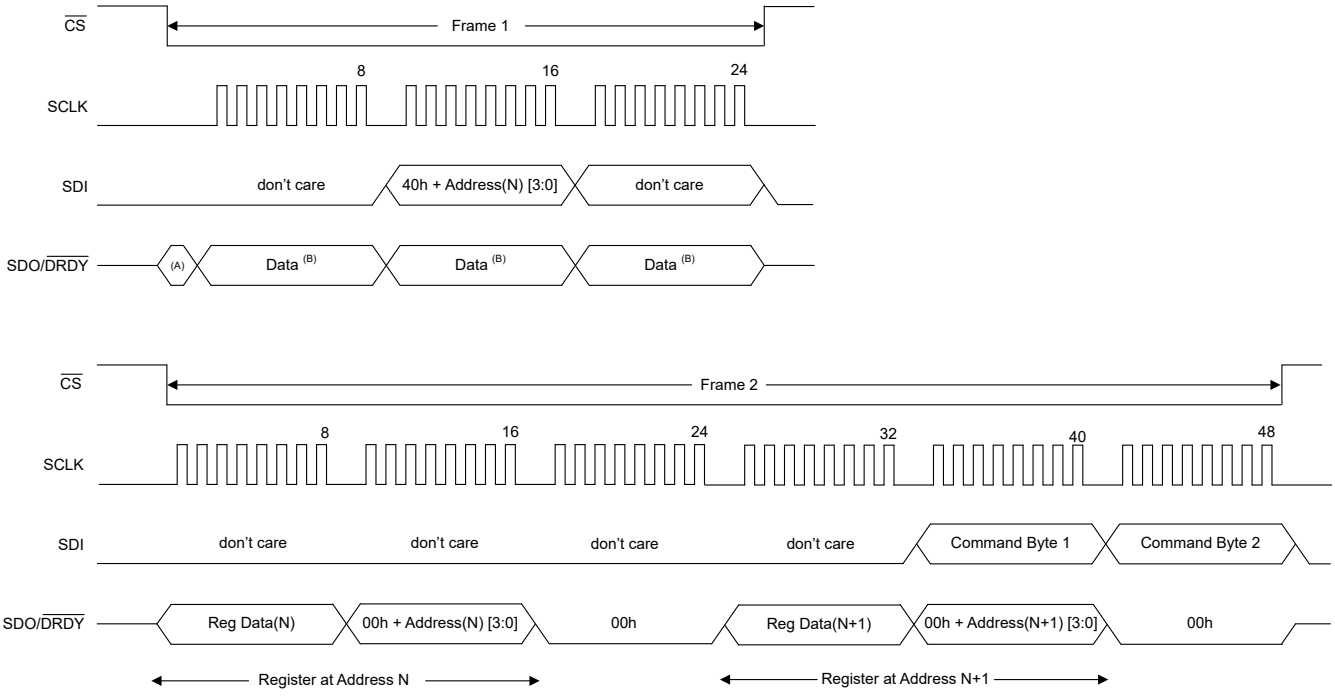
Setting the CONT_READ_EN bit enables continuous-read mode. The SPI switches to continuous-read mode in the next frame following the SPI frame which changed the CONT_READ_EN bit from 0b to 1b.

The SPI returns to the single-read mode by setting the CONT_READ_EN bit back to 0b.

7.5.5.1 Read Registers in Continuous-Read Mode

In continuous-read mode, use the same command frame to read register data as explained in the *Read Register Command* section. The data response frame returns one or multiple register data bytes depending on when $\overline{CS}$ is driven back high. The first register data byte is read from the address specified in the command frame. The register address is then automatically incremented by 1 for each subsequent register read. This is also true if the next register address points to an invalid register. The response to registers outside the valid address range is 00h for the data byte, and FFh for the address indicator byte.

Figure 7-27 shows an example of reading register data in continuous-read mode for the 24-bit device with the STATUS header and CRC disabled. This example shows reading of two consecutive registers N and N+1, however an arbitrary number of registers can be read when holding $\overline{CS}$ low for additional clock periods.

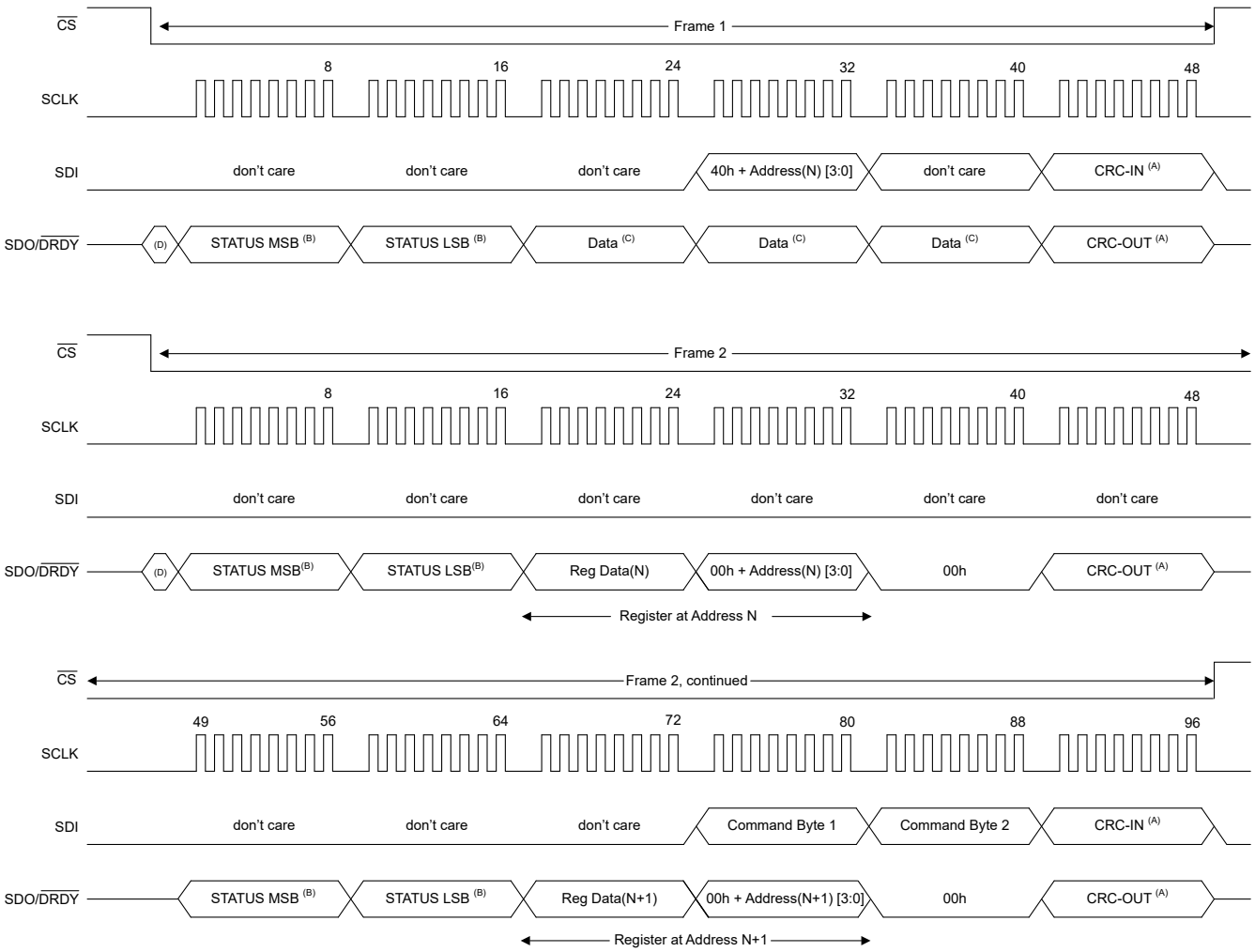


A. Previous state of SDO/$\overline{DRDY}$ before first SCLK.

B. Depending on the previous operation, the data field is either conversion data or the register data byte + address byte + 00h padding.

Figure 7-27. Read Register Data in Continuous-Read Mode (24-Bit Device, STATUS header and CRC disabled)

Figure 7-28 shows an example of the register read operation in continuous-read mode for the 24-bit device with the STATUS header and CRC enabled. In the input and output frame, don't care bytes and 00h pad bytes are used to match the data frame protocol as explained in the *Read Register Command* section. This example shows reading of two consecutive registers N and N+1, however an arbitrary number of registers can be read when holding $\overline{CS}$ low for additional clock periods.



A. Optional CRC byte. If CRC is disabled, the frame shortens by one byte.
B. Optional STATUS header. If STATUS is disabled, the frame shortens by two bytes.
C. Depending on the previous operation, the data field is either conversion data or the register data byte + address byte + 00h padding.
D. Previous state of SDO/$\overline{\text{DRDY}}$ before first SCLK.

Figure 7-28. Read Register Data in Continuous-Read Mode (24-Bit Device, STATUS header and CRC enabled)

7.5.6 Daisy-Chain Operation

In systems using multiple ADCs, the devices can be connected in a daisy-chain string to reduce the number of SPI connections. A daisy-chain connection links together the SPI output (SDO) of one device to the SPI input (SDI) of the next device so the devices in the chain appear as a single logical device to the host controller. There is no special programming required for daisy-chain operation. Apply additional shift clocks to access all devices in the chain. For simplified operation, program the same SPI frame size for each device (for example, when enabling the CRC option of all devices, thus producing a 24-bit (16-bit device), or 32-bit (24-bit device) frame size).

Figure 7-29 shows four devices connected in a daisy-chain configuration. SDI of ADS1x2S14 (1) connects to the host SPI data output, and SDO/$\overline{\text{DRDY}}$ of ADS1x2S14 (4) connects to the host SPI data input. The shift operation is simultaneous for all devices in the chain. After each ADC shifts out the conversion data, the data of SDI appears on SDO/$\overline{\text{DRDY}}$ to drive the SDI of the next device in the chain. The shift operation continues until the last device in the chain is reached. The SPI frame ends when $\overline{\text{CS}}$ is taken high, at which time the data shifted into each device is interpreted. For daisy-chain operation, program the SDO/$\overline{\text{DRDY}}$ pin to data output only mode (SDO_MODE = 0b) and disable continuous-read mode (CONT_READ_EN = 0b).

Connect a pullup resistor on the SDO/$\overline{\text{DRDY}}$ pin of each device to DVDD. When $\overline{\text{CS}}$ is high, SDO/$\overline{\text{DRDY}}$ goes high-Z. The pullup resistors are therefore used to avoid a floating SDI input on the next device in the chain when $\overline{\text{CS}}$ is high.

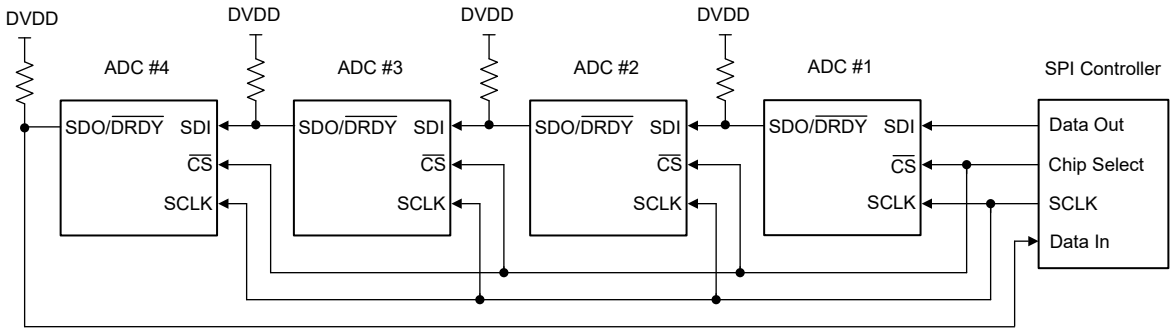


Figure 7-29. Daisy-Chain Connection

Figure 7-30 shows the frame structure for four 24-bit devices connected in a daisy-chain with the STATUS header and CRC disabled.

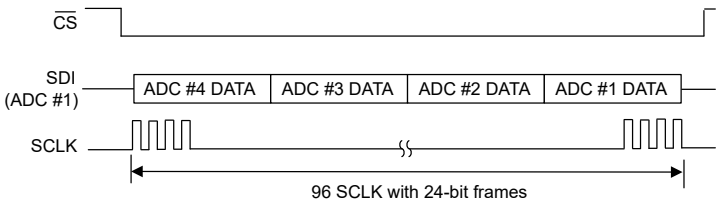
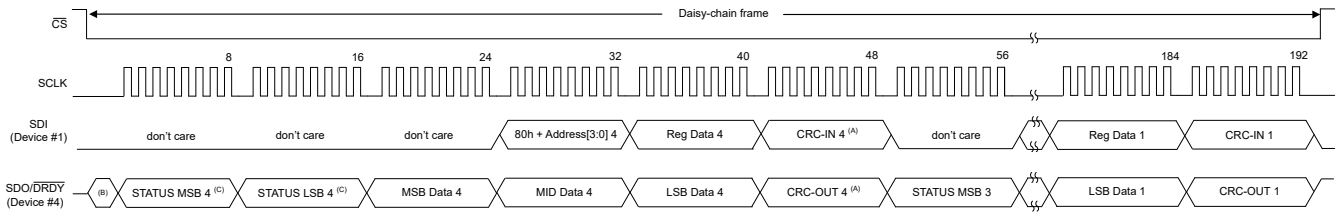


Figure 7-30. Daisy-Chain Data Input Sequence (Four 24-Bit Devices, STATUS Header and CRC Disabled)

To input data, the host first shifts in the data intended for the last device in the chain. The number of input bytes for each ADC is sized to match the output frame size. The default frame size is 24 bits (for a 24-bit device), so initially each ADC requires three bytes by prefixing a pad byte in front of the two command bytes. The input data of ADC #4 is shifted in first, followed by the input data of ADC #3, and so forth.

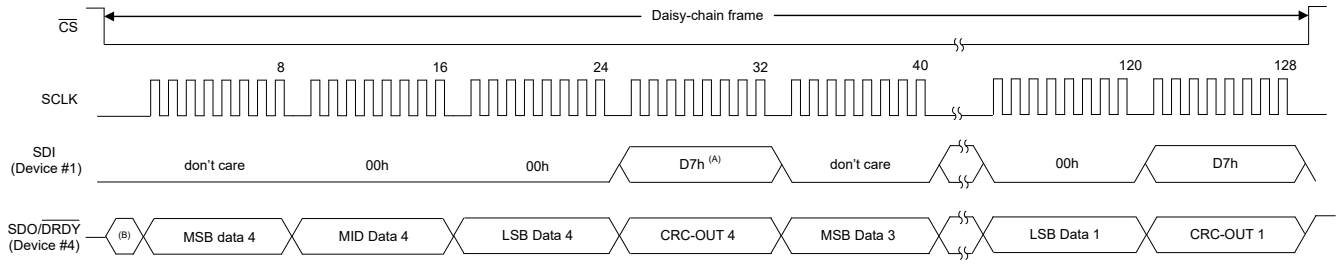
Figure 7-31 shows the detailed input data sequence for the daisy-chain write register operation of Figure 7-29. 48-bit frames for each ADC are shown (24 bits of data, with the STATUS header and CRC enabled). Command operations can be different for each ADC. A register read operation requires a second frame operation to read out the register data.



A. Optional CRC byte. If CRC is disabled, the frame shortens by one byte.
B. Previous state of SDO/$\overline{\text{DRDY}}$ before SCLK is applied.
C. Optional STATUS header. If STATUS is disabled, the frame shortens by two bytes.

Figure 7-31. Write Register Data in Daisy-Chain Connection (Four 24-Bit Devices, STATUS Header and CRC Enabled)

Figure 7-32 shows the data sequence to read conversion data from the device connection provided in Figure 7-29. This example illustrates a 32-bit output frame (24 bits of data, with CRC enabled). The conversion data of ADC (4) is shifted out first in the sequence, followed by the data of ADC (3), and so on. The total number of SCLKs required to shift out the data is given by the number of bits per frame × the number of devices in the chain. In this example, 32-bit output frames × four devices result in 128 total clocks.



A. Optional CRC byte. If CRC is disabled, the frame shortens by one byte.
B. Previous state of SDO/$\overline{\text{DRDY}}$ before SCLK is applied.

Figure 7-32. Read Conversion Data in Daisy-Chain Connection (Four 24-Bit Devices, STATUS Header Disabled, CRC Enabled)

As shown in Equation 13, the maximum number of devices connected in a daisy-chain configuration is limited by the SCLK signal frequency, the selected data rate, and the number of bits per frame.

$$\text{Maximum devices in a chain} = \lfloor f_{SCLK} / (f_{DATA} \times \text{bits per frame}) \rfloor \quad (13)$$

For example, if f_{SCLK} = 10MHz, f_{DATA} = 64kSPS, and 32-bit frames are used, the maximum number of daisy-chain connected devices is the floor of: $\lfloor 10\text{MHz} / (64\text{kHz} \times 32) \rfloor = 4$.

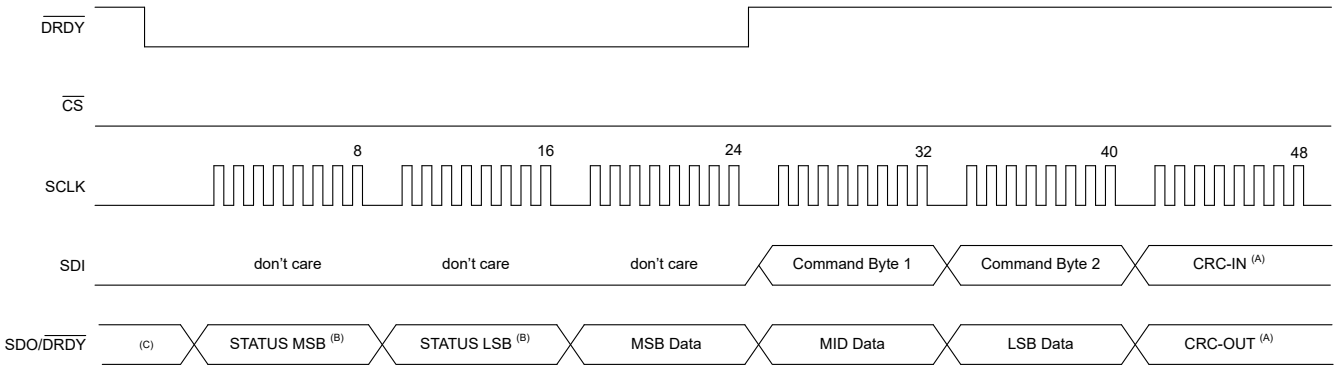
7.5.7 3-Wire SPI Mode

The device can be operated in 3-wire SPI mode by tying the $\overline{CS}$ pin permanently to GND. When $\overline{CS}$ is tied low at power-up or after reset, the device operates in 3-wire SPI mode. The device changes to 4-wire SPI mode any time $\overline{CS}$ is taken high.

Because $\overline{CS}$ no longer controls the frame length in 3-wire SPI mode, SCLKs are counted by the ADC to determine the beginning and ending of a frame. The number of SCLKs must be controlled by the host and must match the size of the output frame. The number of bits per frame depend on the device resolution and configuration. The size of the output frame is shown in Table 7-9. Because frame timing is determined by the number of SCLKs, avoid inadvertent SCLK transitions, such as those possibly occurring at power up.

3-wire SPI mode supports the same command format and clocking as the 4-wire mode, except there is no $\overline{CS}$ toggling. Figure 7-33 shows an example for reading conversion data in 3-wire SPI mode.

Daisy-chain connection of devices is not possible in 3-wire SPI mode, and also continuous-read mode is not available.



A. Optional CRC byte. If CRC is disabled, the frame shortens by one byte.
B. Optional STATUS header. If STATUS is disabled, the frame shortens by two bytes.
C. If SDO_MODE = 0b, the previous state of SDO/$\overline{DRDY}$ remains until the first SCLK rising edge. Otherwise, SDO/$\overline{DRDY}$ follows $\overline{DRDY}$.

Figure 7-33. Read Conversion Data in 3-Wire SPI Mode (24-Bit Device, STATUS Header and CRC Enabled)

7.5.7.1 3-Wire SPI Mode Frame Re-Alignment

In 3-wire SPI mode, an unintended SCLK can misalign the frame, resulting in loss of frame synchronization to the host. As shown in Figure 7-34, the SPI is resynchronized without requiring a device reset by sending an SPI re-align pattern. The re-align pattern is a minimum of 63 consecutive 1s followed by one 0 at the 64th SCLK. The 65th SCLK starts a new SPI frame. The device also accepts a re-align pattern with more than 63 consecutive 1s followed by one 0. In that case, the new frame starts with the SCLK rising edge following the 0. Optionally, the ADC can be completely reset using the reset pattern shown in the *Reset by SPI Input Pattern* section.

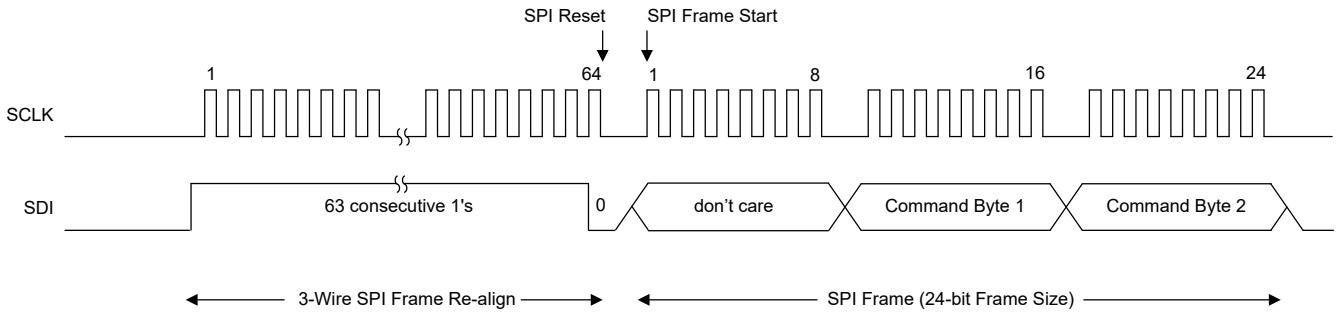


Figure 7-34. 3-Wire Mode SPI Re-Align Pattern (24-Bit Device)

7.5.8 Monitoring for New Conversion Data

There are several methods available to determine when new conversion data are ready for retrieval.

1. Monitor the $\overline{\text{DRDY}}$ or the SDO/$\overline{\text{DRDY}}$ pin.
2. Evaluate the DRDY bit and conversion counter transmitted as part of the STATUS header.
3. Clock counting using an external clock: Count the number of ADC main clocks to predict when data are ready.

7.5.8.1 $\overline{\text{DRDY}}$ Pin or SDO/$\overline{\text{DRDY}}$ Pin Monitoring

$\overline{\text{DRDY}}$ is a dedicated data-ready output pin, and the SDO/$\overline{\text{DRDY}}$ pin is a dual-function output pin. See the *Data Ready ($\overline{\text{DRDY}}$) Pin* section for a description of the $\overline{\text{DRDY}}$ pin and the *Serial Data Output/Data Ready (SDO/$\overline{\text{DRDY}}$)* section for a description of the SDO/$\overline{\text{DRDY}}$ pin.

A falling edge on the $\overline{\text{DRDY}}$ pin indicates that a new conversion completed. Connect the $\overline{\text{DRDY}}$ pin to a falling edge triggered interrupt-capable GPIO of the host controller. After the host detected the falling $\overline{\text{DRDY}}$ signal edge, the host reads the conversion data before the next $\overline{\text{DRDY}}$ falling edge. If an interrupt-capable GPIO is not available, the host can monitor the $\overline{\text{DRDY}}$ pin level. A logic low level indicates that the latest available conversion result has not been read. A logic high level indicates that no new conversion results are available, and that the latest conversion result has been read previously. Conversion data can be read at any time without concern of data corruption.

The SDO/$\overline{\text{DRDY}}$ pin can be used in a similar fashion as the dedicated $\overline{\text{DRDY}}$ pin when the dual function is enabled using the SDO_MODE = 1b setting. However, in contrast to the $\overline{\text{DRDY}}$ pin, the SDO/$\overline{\text{DRDY}}$ pin is only driven when $\overline{\text{CS}}$ is low. That means, the host has to drop the $\overline{\text{CS}}$ line to evaluate the SDO/$\overline{\text{DRDY}}$ signal.

7.5.8.2 Reading DRDY Bit and Conversion Counter

A software method to determine when new data are available for readout is to evaluate the DRDY bit as part of the STATUS header. For that purpose, enable the STATUS header transmission on SDO using the STATUS_EN bit. Two methods to evaluate the DRDY bit can be used:

- The host periodically reads a full SPI frame to receive the STATUS header together with the conversion data. If the DRDY bit in that frame reads 1b, the received conversion data are new. If the DRDY bit is 0b, the host discards the conversion data received in that frame because the same conversion result has been read previously.
- The host periodically sends a short 8-bit SPI frame to read the DRDY bit which is transmitted within the first byte on SDO. Only if the DRDY bit reads 1b, the host sends a full SPI frame to receive the STATUS header together with the new conversion data. This method of short-cycling the SPI frame cannot be used in 3-wire SPI mode or when operating the device in a daisy-chain.

To avoid missing data, evaluate the DRDY bit at least as often as the output data rate.

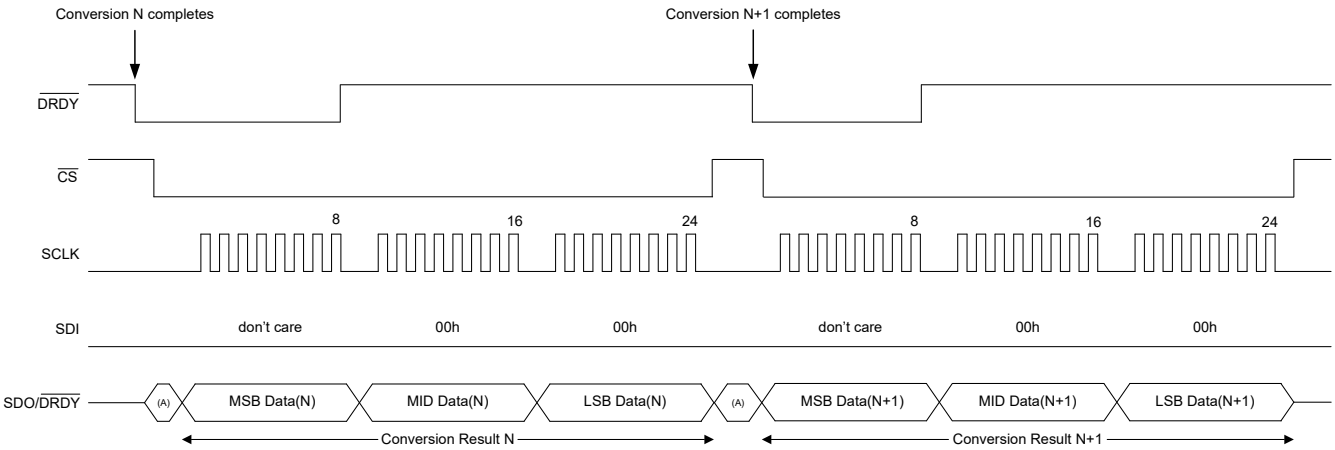
In addition, the conversion counter transmitted as part of the STATUS header indicates the count of the conversion that is retrieved within the current SPI frame. The host evaluates the conversion counter to understand if the host read the same conversion result multiple times or if the host missed to read a conversion result.

7.5.8.3 Clock Counting

Another method to determine when new data are ready is to count ADC main clock cycles, because each conversion requires a deterministic amount of clock cycles. This method is only possible when using an external clock because the internal clock oscillator is not observable. After conversion start, the number of clock cycles required for the first conversion is larger compared to the clock cycles required for all following conversions. The initial number of clock cycles is equal to the latency time of the digital filter as listed in the *Digital Filter Latency* section.

7.5.9 $\overline{\text{DRDY}}$ Pin Behavior

This section provides details about the $\overline{\text{DRDY}}$ pin behavior in various scenarios. $\overline{\text{DRDY}}$ transitions low whenever new conversion data complete. As shown in Figure 7-35, $\overline{\text{DRDY}}$ transitions high at the eighth SCLK falling edge of the conversion data MSB read.

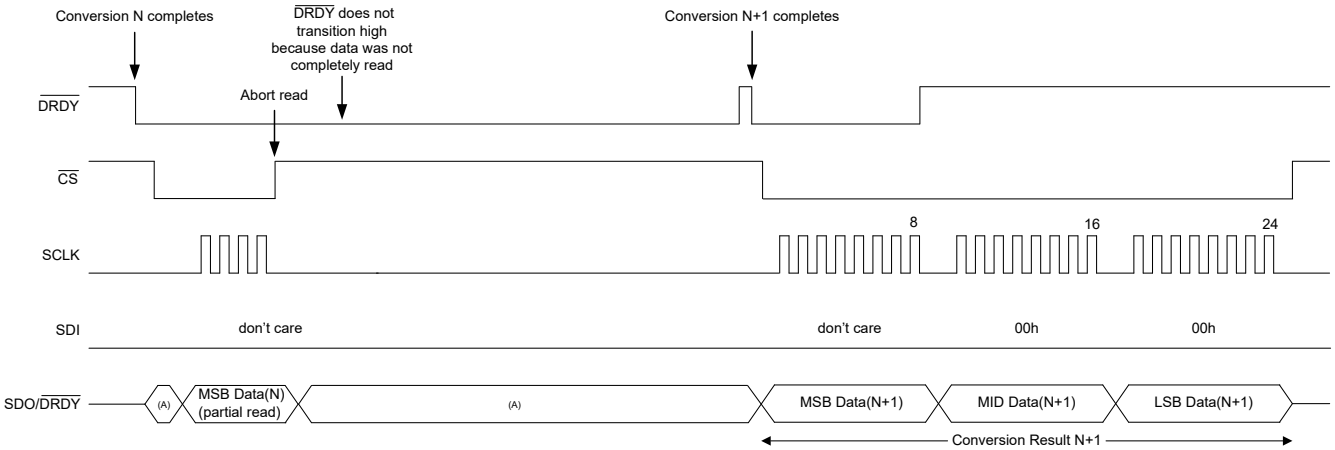


A. If the SDO_MODE bit = 0b, the previous state of SDO/$\overline{\text{DRDY}}$ remains until the first SCLK rising edge. Otherwise, SDO/$\overline{\text{DRDY}}$ follows $\overline{\text{DRDY}}$.

Figure 7-35. $\overline{\text{DRDY}}$ Pin Behavior: Reading Latest Available Conversion Data

If $\overline{\text{DRDY}}$ is low when a new conversion completes, then $\overline{\text{DRDY}}$ drives high $t_{w(DRH)}$ before the $\overline{\text{DRDY}}$ falling edge (see Figure 7-36).

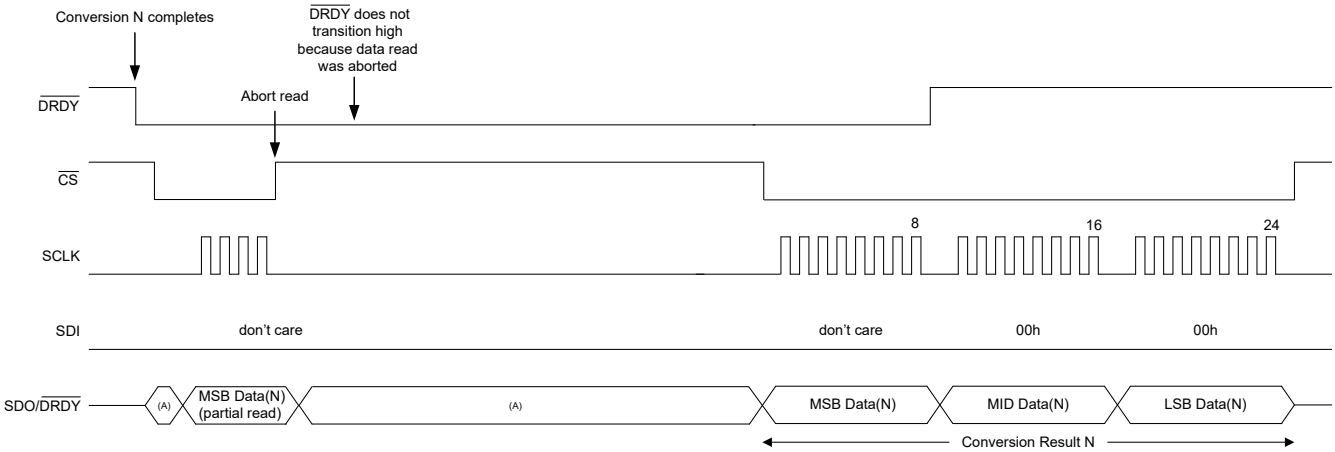
If $\overline{\text{CS}}$ is driven high before the eighth SCLK of the conversion data MSB read, then $\overline{\text{DRDY}}$ stays low, indicating that conversion data was not read (see Figure 7-36 and Figure 7-37).



A. If the SDO_MODE bit = 0b, the previous state of SDO/$\overline{\text{DRDY}}$ remains until the first SCLK rising edge. Otherwise, SDO/$\overline{\text{DRDY}}$ follows $\overline{\text{DRDY}}$.

Figure 7-36. $\overline{\text{DRDY}}$ Pin Behavior: Incomplete Read of Conversion Data Before New Conversion Completes

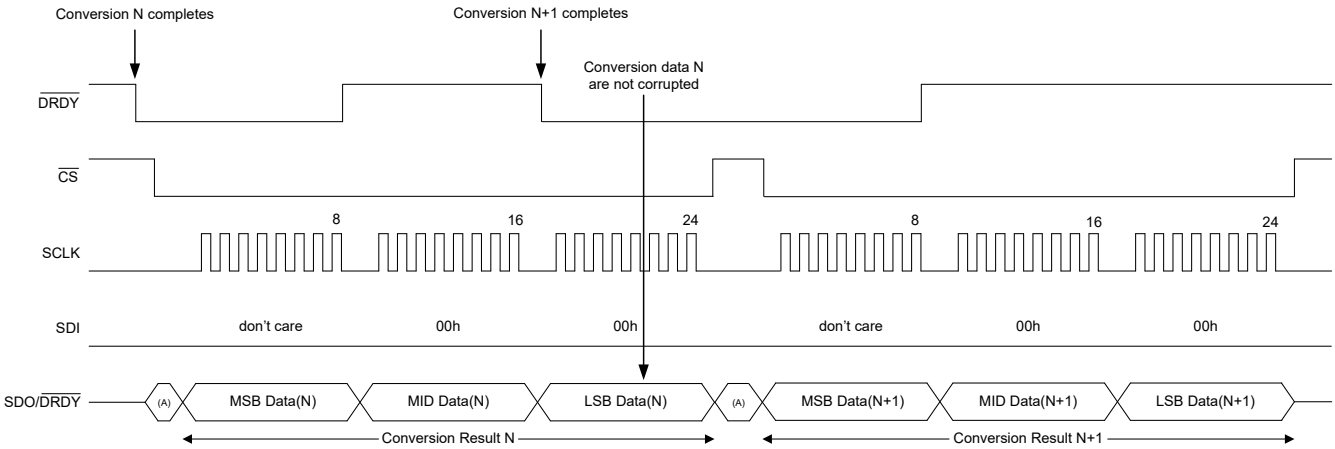
Figure 7-37 shows that the same conversion data can be read multiple times until new conversions complete. The conversion counter (CONV_COUNT[3:0] bits in the STATUS_LSB register) indicates if the same data are read again or if new data are read.



A. If the SDO_MODE bit = 0b, the previous state of SDO/$\overline{\text{DRDY}}$ remains until the first SCLK rising edge. Otherwise, SDO/$\overline{\text{DRDY}}$ follows $\overline{\text{DRDY}}$.

Figure 7-37. $\overline{\text{DRDY}}$ Pin Behavior: Incomplete Read of Conversion Data Followed by Complete Read of Same Conversion Data

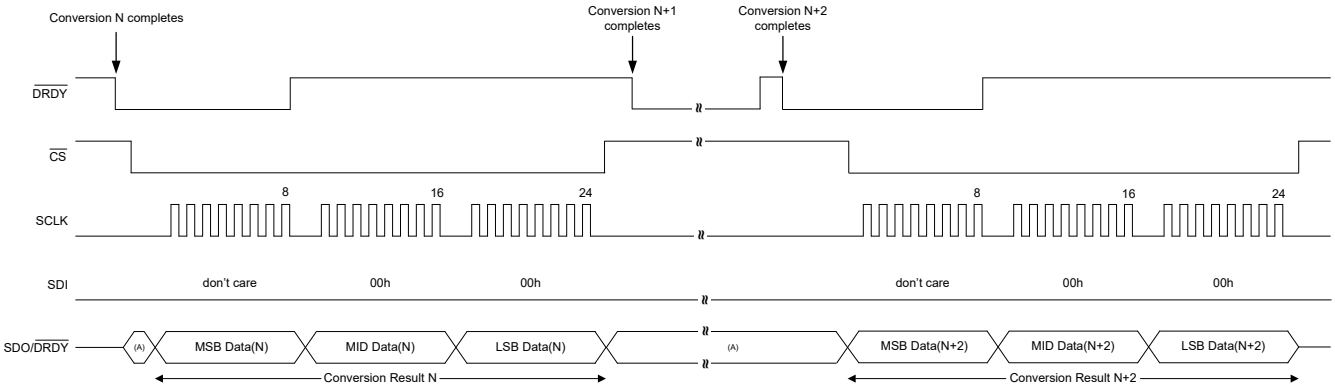
The device avoids data corruption if new conversions N+1 complete while conversion data N are being read. Conversion data N+1 are held in an internal buffer until the read of conversion data N is complete. In the following frame, conversion data N+1 are loaded into the SDO output buffer. $\overline{\text{DRDY}}$ does not transition high after conversion data N have been read in this case to indicate that new conversion data N+1 are available for readout (see Figure 7-38).



A. If the SDO_MODE bit = 0b, the previous state of SDO/$\overline{\text{DRDY}}$ remains until the first SCLK rising edge. Otherwise, SDO/$\overline{\text{DRDY}}$ follows $\overline{\text{DRDY}}$.

Figure 7-38. $\overline{\text{DRDY}}$ Pin Behavior: Reading Conversion Data While New Conversion Completes

Figure 7-39 illustrates that conversion data N+1 are lost when the host does not read the data before conversions N+2 complete. The conversion counter is helpful in this situation to detect if the host missed reading the intermediate conversion results.



A. If the SDO_MODE bit = 0b, the previous state of SDO/$\overline{\text{DRDY}}$ remains until the first SCLK rising edge. Otherwise, SDO/$\overline{\text{DRDY}}$ follows $\overline{\text{DRDY}}$.

Figure 7-39. $\overline{\text{DRDY}}$ Pin Behavior: Missed Reading Intermediate Conversion Results

Whenever the device is programmed to enter standby mode (STBY_MODE bit = 1b) after conversions stopped, $\overline{\text{DRDY}}$ is driven back high 4 t_{MOD} after transitioning low. Figure 7-40 shows an example of the $\overline{\text{DRDY}}$ pin behavior when entering standby mode using single-shot conversion mode.

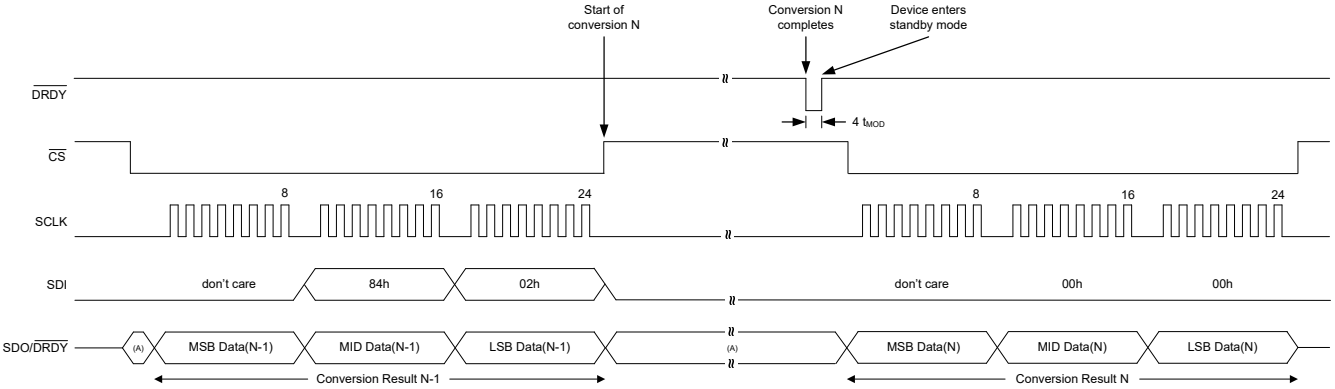


Figure 7-40. $\overline{\text{DRDY}}$ Pin Behavior: Entering Standby Mode (Single-Shot Conversion Mode)

Polling the DRDY bit or the *state* of the $\overline{\text{DRDY}}$ pin to check for the completion of the conversion is not practical in this particular scenario (STBY_MODE bit = 1b) because of the short period the $\overline{\text{DRDY}}$ pin is low. Use one of the other available options to determine when new data are available, such as the $\overline{\text{DRDY}}$ pin falling edge, polling the conversion counter, or waiting a fixed amount of time equal to or longer than the conversion period.

7.5.10 Conversion Data Format

Conversion data are coded depending on the CODING bit setting. By default, conversion data are coded in binary two's-complement format, MSB first (sign bit). Set the CODING bit to 1b for unipolar straight binary format. Table 7-12 and Table 7-13 show the output code for the 16-bit and 24-bit device, respectively. In binary two's-complement format, the conversion data clips to positive and negative full-scale codes when the input signal exceeds the respective positive and negative full-scale values. In unipolar straight binary format, conversion data clips to the full-scale code when the input signal exceeds the full-scale value, or to the zero code when the input signal value is below zero.

Table 7-12. Ideal Output Code Versus Input Signal (16-Bit Device)

DIFFERENTIAL INPUT VOLTAGE (V)	IDEAL OUTPUT CODE(1)	
	BINARY TWO'S-COMPLEMENT FORMAT (CODING = 0b)	UNIPOLAR STRAIGHT BINARY FORMAT (CODING = 1b)
≥ FSR × (2^{16} – 1) / 2^{16}	7FFFh	FFFFh
≥ FSR × (2^{15} – 1) / 2^{15}		FFFEh
FSR / 2^{15}	0001h	0002h
0	0000h	0000h
–FSR / 2^{15}	FFFFh	
–FSR × (2^{15} – 1) / 2^{15}	8001h	
≤ –FSR	8000h	

(1) Ideal output data, excluding offset, gain, linearity, and noise errors.

Table 7-13. Ideal Output Code Versus Input Signal (24-Bit Device)

DIFFERENTIAL INPUT VOLTAGE (V)	IDEAL OUTPUT CODE(1)	
	BINARY TWO'S-COMPLEMENT FORMAT (CODING = 0b)	UNIPOLAR STRAIGHT BINARY FORMAT (CODING = 1b)
≥ FSR × (2^{24} – 1) / 2^{24}	7FFFFFh	FFFFFFh
≥ FSR × (2^{23} – 1) / 2^{23}		FFFFFEh
FSR / 2^{23}	000001h	000002h
0	000000h	000000h
–FSR / 2^{23}	FFFFFFh	
–FSR × (2^{23} – 1) / 2^{23}	800001h	
≤ –FSR	800000h	

(1) Ideal output data, excluding offset, gain, linearity, and noise errors.

7.5.11 Register Map CRC

The register map CRC detects unintended changes in the register map contents. Register addresses 00h to 04h are excluded from the CRC protection. The CRC calculation is performed across the register address space from 05h to 0Eh. Enable the register map CRC using the REG_MAP_CRC_EN bit. When the register map CRC is enabled, the device constantly calculates an 8-bit CRC value across that register map section and compares the internal calculation result against the CRC value provided by the user in the REG_MAP_CRC_VAL[7:0] bit field. If the internal calculation result and the REG_MAP_CRC_VAL[7:0] do not match, the REG_MAP_CRC_FAULTn flag is set to 0b. No other action is taken by the device in the event of a register map CRC fault.

The CRC calculation begins with the MSB of the register at address 05h and ends with the LSB of the register at address 0Eh using the CRC-8-ATM (HEC) polynomial: $X^8 + X^2 + X^1 + 1$. The nine coefficients of the polynomial are: 100000111. See the *SPI CRC* section for details on the CRC calculation. The CRC calculation is initialized with the seed value of FFh.

The REG_MAP_CRC_FAULTn flag does not indicate unintended bit changes immediately because the CRC calculation is implemented serially. Up to $t_{p(REG\_MAP\_CRC)}$ = 640 t_{CLK} cycles can elapse for the REG_MAP_CRC_FAULTn flag to indicate a fault.

Use the following procedure to change register bits without accidentally causing a REG_MAP_CRC_FAULTn indication:

- Disable the register map by setting REG_MAP_CRC_EN = 0b
- Wait the fault response time $t_{p(REG\_MAP\_CRC)}$
- If the REG_MAP_CRC_FAULTn flag is set to 0b, clear the fault flag by writing 1b to the REG_MAP_CRC_FAULTn bit
- Optional: Verify the REG_MAP_CRC_FAULTn fault flag is cleared to 1b
- Change the device register bits as needed
- Update the REG_MAP_CRC_VAL[7:0] bits based on the new register map settings
- Enable the register map CRC by setting REG_MAP_CRC_EN = 1b

Register bits can also be changed while the register map CRC is enabled, as discussed in the following procedure, but can cause unintended REG_MAP_CRC_FAULTn indications.

- Change the register bits as needed while the register map CRC is enabled
- Update the REG_MAP_CRC_VAL[7:0] bits based on the new register map settings
- Wait the fault response time $t_{p(REG\_MAP\_CRC)}$
- If the REG_MAP_CRC_FAULTn flag is set to 0b, clear the fault flag by writing 1b to the REG_MAP_CRC_FAULTn bit
- Optional: Verify the REG_MAP_CRC_FAULTn fault flag is cleared to 1b

8 Registers

Table 8-1 lists the memory-mapped registers for the Registers registers. All register offset addresses not listed in Table 8-1 should be considered as reserved locations and the register contents should not be modified.

Table 8-1. Register Map

Address	Acronym	Reset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ID Registers - not covered by register map CRC										
00h	DEVICE_ID	XXh	DEV_ID[7:0]							
01h	REVISION_ID	XXh	REV_ID[7:0]							
Status Registers - not covered by register map CRC										
02h	STATUS_MSB	3Eh	RESETn	AVDD_UVn	REF_UVn	SPI_CRC_FAULTn	REG_MAP_CRC_FAULTn	MEM_FAULTn	REG_WRITE_FAULTn	DRDY
03h	STATUS_LSB	F0h	CONV_COUNT[3:0]				GPIO3_DAT_IN	GPIO2_DAT_IN	GPIO1_DAT_IN	GPIO0_DAT_IN
Conversion Control Register - not covered by register map CRC										
04h	CONVERSION_CTRL	00h	RESET[5:0]						START	STOP
Device Configuration Registers - covered by register map CRC										
05h	DEVICE_CFG	00h	PWDN	STBY_MODE	BOCS[1:0]		CLK_SEL	CONV_MODE	SPEED_MODE[1:0]	
06h	DATA_RATE_CFG	00h	DELAY[3:0]				GC_EN	FLTR_OSR[2:0]		
07h	MUX_CFG	01h	AINP[3:0]				AINN[3:0]			
08h	GAIN_CFG	01h	SPARE	SYS_MON[2:0]			GAIN[3:0]			
09h	REFERENCE_CFG	00h	REF_UV_EN	RESERVED	REFP_BUF_EN	REFN_BUF_EN	RESERVED	REF_VAL	REF_SEL[1:0]	
0Ah	DIGITAL_CFG	00h	SPARE	REG_MAP_CRC_EN	SPI_CRC_EN	STATUS_EN	FAULT_PIN_BEHAVIOR	CONT_READ_EN	CODING	SDO_MODE
0Bh	GPIO_CFG	00h	GPIO3_CFG[1:0]		GPIO2_CFG[1:0]		GPIO1_CFG[1:0]		GPIO0_CFG[1:0]	
0Ch	GPIO_DATA_OUTPUT	00h	GPIO3_SRC	GPIO2_SRC	RESERVED		GPIO3_DAT_OUT	GPIO2_DAT_OUT	GPIO1_DAT_OUT	GPIO0_DAT_OUT
0Dh	IDAC_MAG_CFG	00h	I2MAG[3:0]				I1MAG[3:0]			
0Eh	IDAC_MUX_CFG	10h	IUNIT	I2MUX[2:0]			RESERVED	I1MUX[2:0]		
Register Map CRC Value Register										
0Fh	REG_MAP_CRC	00h	REG_MAP_CRC_VAL[7:0]							

Complex bit access types are encoded to fit into small table cells. Table 8-2 shows the codes that are used for access types in this section.

Table 8-2. Registers Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.1 DEVICE_ID Register (Address = 00h) [Reset = XXh]

Return to the Summary Table.

Figure 8-1. DEVICE_ID Register

7	6	5	4	3	2	1	0
DEV_ID[7:0]							
R-xxxxxxxxb							

Table 8-3. DEVICE_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DEV_ID[7:0]	R	xxxxxxxxb	Device ID DEV_ID[7:4] bits are subject to change without notice. DEV_ID[3:0] bits always read 1011b for the 24-bit device and 1010b for the 16-bit device.

8.2 REVISION_ID Register (Address = 01h) [Reset = XXh]

Return to the Summary Table.

Figure 8-2. REVISION_ID Register

7	6	5	4	3	2	1	0
REV_ID[7:0]							
R-xxxxxxxxb							

Table 8-4. REVISION_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REV_ID[7:0]	R	xxxxxxxxb	Revision ID Values are subject to change without notice.

8.3 STATUS_MSB Register (Address = 02h) [Reset = 3Eh]

Return to the Summary Table.

Figure 8-3. STATUS_MSB Register

7	6	5	4	3	2	1	0
RESETn	AVDD_UVn	REF_UVn	SPI_CRC_FAULTn	REG_MAP_CRC_FAULTn	MEM_FAULTn	REG_WRITE_FAULTn	DRDY
R/W-0b	R/W-0b	R/W-1b	R-1b	R/W-1b	R-1b	R-1b	R-0b

Table 8-5. STATUS_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESETn	R/W	0b	Reset flag Indicates a device reset occurred. Write 1b to clear bit to 1b. 0b = Reset occurred 1b = No reset occurred
6	AVDD_UVn	R/W	0b	AVDD undervoltage fault flag Indicates the AVDD supply voltage dropped below the AVDD undervoltage threshold. AVDD_UVn always sets to 0b when entering power-down mode even when the AVDD supply did not drop below the AVDD undervoltage threshold. Write 1b to clear bit to 1b. 0b = Undervoltage fault occurred 1b = No undervoltage fault occurred
5	REF_UVn	R/W	1b	Reference voltage undervoltage fault flag Indicates the reference voltage selected by the REF_SEL[1:0] bits dropped below the reference undervoltage threshold. Write 1b to clear bit to 1b. Enable the reference undervoltage monitor using the REF_UV_EN bit. 0b = Undervoltage fault occurred 1b = No undervoltage fault occurred
4	SPI_CRC_FAULTn	R	1b	SPI CRC fault flag Indicates a SPI CRC fault occurred on SDI in the previous SPI frame. The execution of the command in the frame where the SPI CRC fault occurred is blocked. Instead, a no operation command is executed. Commands in following frames are not blocked. This bit updates in every new SPI frame based on the CRC result of the previous SPI frame. Enable the SPI CRC using the SPI_CRC_EN bit. In addition, enable the transmission of the STATUS header using the STATUS_EN bit to get notified about any SPI CRC faults. 0b = SPI CRC fault occurred 1b = No SPI CRC fault occurred
3	REG_MAP_CRC_FAULTn	R/W	1b	Register map CRC fault flag Indicates a register map CRC fault occurred. Write 1b to clear bit to 1b. Enable the register map CRC using the REG_MAP_CRC_EN bit. 0b = Register map CRC fault occurred 1b = No register map CRC fault occurred
2	MEM_FAULTn	R	1b	Memory map CRC fault flag Indicates a memory map CRC fault in the internal memory occurred. Perform a power cycle or reset the device when the bit is 0b. 0b = Memory map CRC fault occurred 1b = No memory map CRC fault occurred
1	REG_WRITE_FAULTn	R	1b	Register access fault flag Indicates a write access to an invalid register address occurred. This flag sets when an invalid register address is written to, and updates at the next register write command. Reading from an invalid register address does not set the flag, but can be detected from the address indication inside the SPI frame of the read command. 0b = Register access fault occurred 1b = No register access fault occurred

Table 8-5. STATUS_MSB Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	DRDY	R	0b	Data-ready indication bit The DRDY bit is the inverse of the $\overline{\text{DRDY}}$ pin. Enable the transmission of the STATUS header using the STATUS_EN bit to leverage the DRDY bit indication. The DRDY bit indicates if the conversion data read within the current SPI frame are new or are repeated data from the last read operation. Polling the DRDY bit using the register read command is not reliable, because the DRDY bit returns to 0b during the first frame of the read register command transmission already. 0b = Data are not new 1b = Data are new

8.4 STATUS_LSB Register (Address = 03h) [Reset = F0h]

Return to the Summary Table.

Figure 8-4. STATUS_LSB Register

7	6	5	4	3	2	1	0
CONV_COUNT[3:0]				GPIO3_DAT_IN	GPIO2_DAT_IN	GPIO1_DAT_IN	GPIO0_DAT_IN
R-1111b				R-0b	R-0b	R-0b	R-0b

Table 8-6. STATUS_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	CONV_COUNT[3:0]	R	1111b	Conversion counter The conversion counter increments every time a new conversion completes. After reaching a counter value of Fh, the counter rolls over to 0h with the completion of the next conversion. The counter only resets to Fh (and the conversion data clear) in power-down mode or after a device reset. At the completion of the first conversion after reset or power down, the counter reads 0h.
3	GPIO3_DAT_IN	R	0b	GPIO3 data Read back value of GPIO3 when AIN7/GPIO3/$\overline{\text{DRDY}}$/CLK is configured as digital input, digital output, or $\overline{\text{DRDY}}$ output. Bit reads 0b when the GPIO function is disabled (GPIO3_CFG[1:0] = 00b) or the clock input function is selected (GPIO3_CFG[1:0] = 01b, CLK_SEL = 1b). 0b = Low 1b = High
2	GPIO2_DAT_IN	R	0b	GPIO2 data Read back value of GPIO2 when AIN6/GPIO2/$\overline{\text{FAULT}}$ is configured as digital input, digital output, or static $\overline{\text{FAULT}}$ output. Bit reads 0b when the GPIO function is disabled (GPIO2_CFG[1:0] = 00b) or when GPIO2 is configured as $\overline{\text{FAULT}}$ output with heart beat function (GPIO2_CFG[1:0] = 10b or 11b, GPIO2_SRC = 1b, FAULT_PIN_BEHAVIOR = 1b). 0b = Low 1b = High
1	GPIO1_DAT_IN	R	0b	GPIO1 data Read back value of GPIO1 when AIN5/REFN/GPIO1 is configured as digital input or output. Bit reads 0b when the GPIO function is disabled (GPIO1_CFG[1:0] = 00b). 0b = Low 1b = High
0	GPIO0_DAT_IN	R	0b	GPIO0 data Read back value of GPIO0 when AIN4/REFP/GPIO0 is configured as digital input or output. Bit reads 0b when the GPIO function is disabled (GPIO0_CFG[1:0] = 00b). 0b = Low 1b = High

8.5 CONVERSION_CTRL Register (Address = 04h) [Reset = 00h]

Return to the Summary Table.

Figure 8-5. CONVERSION_CTRL Register

7	6	5	4	3	2	1	0
RESET[5:0]						START	STOP
R/W-000000b						R/W-0b	R/W-0b

Table 8-7. CONVERSION_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESET[5:0]	R/W	000000b	Reset device Write 010110b to reset the ADC. The START and STOP bits must be set to 0b in the same write operation to reset the ADC. These bits always read 000000b.
1	START	R/W	0b	Start conversion Write 1b to start or restart conversions. In single-shot conversion mode, one conversion is started. In continuous conversion mode, conversions are started and continue until stopped by the STOP bit. Writing 1b while a conversion is ongoing restarts the conversion. Writing 1b to both the START and STOP bits at the same time has no effect. The START bit is self-clearing and always reads 0b. 0b = No operation 1b = Start or restart conversion
0	STOP	R/W	0b	Stop conversion Write 1b to stop conversions in continuous-conversion mode. Ongoing conversions are allowed to complete. The STOP bit has no effect in single-shot conversion mode. Writing 1b to both the START and STOP bits at the same time has no effect. The STOP bit clears to 0b after the ongoing conversion finishes or when the START bit is set before the ongoing conversion finishes, which aborts the ongoing conversion and restarts a new conversion. 0b = No operation 1b = Stop conversion after the current conversion completes

8.6 DEVICE_CFG Register (Address = 05h) [Reset = 00h]

Return to the Summary Table.

Figure 8-6. DEVICE_CFG Register

7	6	5	4	3	2	1	0
PWDN	STBY_MODE	BOCS[1:0]		CLK_SEL	CONV_MODE	SPEED_MODE[1:0]	
R/W-0b	R/W-0b	R/W-00b		R/W-0b	R/W-0b	R/W-00b	

Table 8-8. DEVICE_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PWDN	R/W	0b	Power-down mode selection Powers down all circuitry except for circuitry necessary to retain the user register settings. SPI communication is still possible. In power-down mode, the conversion counter (CONV_COUNT[3:0]) resets to Fh, the conversion data clears, and the START bit is ignored. Setting the PWDN bit to 1b powers the device down immediately; any ongoing conversions are aborted. Any analog inputs configured as GPIO digital outputs transition into a Hi-Z state in power-down mode. To maintain a certain logic level during power down, consider external pullup or pulldown resistors on the respective GPIO pins. 0b = Active mode 1b = Power-down mode
6	STBY_MODE	R/W	0b	Standby mode selection This bit enables the auto engagement of the low-power standby mode after conversions are stopped. 0b = Idle mode; device remains fully powered when conversions stop. 1b = Standby mode; when conversions stop, the ADC, PGA, IDACs, BOCS, REF buffers and REF UV monitor power down and the heart beat output signal of the FAULTn pin, if enabled, stops. The FAULTn pin behaves as if configured for static output in standby mode. The internal VREF and AVDD UV monitor stay powered up. The register map CRC and memory map CRC are disabled in standby mode. Standby mode is exited when conversions restart.
5:4	BOCS[1:0]	R/W	00b	Burnout current source and sink selection Enables and selects the value of the burnout current source and sink. Disable the burnout current sources when using global chop mode (GC_EN = 1b). 00b = Disabled 01b = 0.2µA 10b = 1µA 11b = 10µA
3	CLK_SEL	R/W	0b	Clock source selection Selects the clock source for the device. To change from internal oscillator to external clock, first set GPIO3_CFG = 01b to configure the GPIO3 pin as external clock input, then set CLK_SEL = 1b. 0b = Internal oscillator 1b = External clock
2	CONV_MODE	R/W	0b	Conversion mode selection Selects the conversion mode for the device. 0b = Continuous-conversion mode 1b = Single-shot conversion mode
1:0	SPEED_MODE[1:0]	R/W	00b	Speed mode selection Selects the speed mode for the device. 00b = Speed mode 0 (f_{MOD} = 32kHz) 01b = Speed mode 1 (f_{MOD} = 256kHz) 10b = Speed mode 2 (f_{MOD} = 512kHz) 11b = Speed mode 3 (f_{MOD} = 1024kHz)

8.7 DATA_RATE_CFG Register (Address = 06h) [Reset = 00h]

Return to the Summary Table.

Figure 8-7. DATA_RATE_CFG Register

7	6	5	4	3	2	1	0
DELAY[3:0]				GC_EN	FLTR_OSR[2:0]		
R/W-0000b				R/W-0b	R/W-000b		

Table 8-9. DATA_RATE_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	DELAY[3:0]	R/W	0000b	Programmable conversion start delay selection Sets the programmable conversion start delay time for the first conversion after a digital filter reset. This delay time is also used as the delay between conversions when global-chop mode is enabled. 0000b = 0x t_{MOD} 0001b = 1x t_{MOD} 0010b = 2x t_{MOD} 0011b = 4x t_{MOD} 0100b = 8x t_{MOD} 0101b = 16x t_{MOD} 0110b = 32x t_{MOD} 0111b = 64x t_{MOD} 1000b = 128x t_{MOD} 1001b = 256x t_{MOD} 1010b = 512x t_{MOD} 1011b = 1024x t_{MOD} 1100b = 2048x t_{MOD} 1101b = 4096x t_{MOD} 1110b = 8192x t_{MOD} 1111b = 16384x t_{MOD}
3	GC_EN	R/W	0b	Global-chop mode enable Enables global-chop mode. When enabled, the device automatically swaps the analog inputs and takes the average of two consecutive conversions to cancel the internal offset voltage. 0b = Disabled 1b = Enabled
2:0	FLTR_OSR[2:0]	R/W	000b	Filter OSR selection Selects the OSR of the digital filter or the output data rate. For settings where an OSR is stated, the output data rate calculates to $f_{DATA} = f_{MOD} / OSR$. For the 20SPS and 25SPS data rate settings, the digital filter adjusts the OSR automatically based on the selected speed mode. The 20SPS and 25SPS data rates are valid for a nominal clock frequency of f_{CLK} = 4.096MHz. The data rates scale proportional with the clock frequency. At output data rates of 20SPS and 25SPS the digital filter provides 50Hz and 60Hz line-cycle rejection. 000b = OSR = 16 (Sinc4 OSR = 16) 001b = OSR = 32 (Sinc4 OSR = 32) 010b = OSR = 128 (Sinc4 OSR = 32, Sinc1 OSR = 4) 011b = OSR = 256 (Sinc4 OSR = 32, Sinc1 OSR = 8) 100b = OSR = 512 (Sinc4 OSR = 32, Sinc1 OSR = 16) 101b = OSR = 1024 (Sinc4 OSR = 32, Sinc1 OSR =32) 110b = f_{DATA} = 25SPS (independent of speed mode) 111b = f_{DATA} = 20SPS (independent of speed mode)

8.8 MUX_CFG Register (Address = 07h) [Reset = 01h]

Return to the Summary Table.

Figure 8-8. MUX_CFG Register

7	6	5	4	3	2	1	0
AINP[3:0]				AINN[3:0]			
R/W-0000b				R/W-0001b			

Table 8-10. MUX_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	AINP[3:0]	R/W	0000b	Positive multiplexer input selection Selects the positive analog input for the ADC. Analog inputs AIN4 and AIN5 can still be used as analog inputs, even when the inputs are configured as REFP and REFN inputs, respectively. When an analog input is configured as GPIO, the analog input can still be selected by the Mux and used to measure back the voltage on the GPIO pin. 0000b = AIN0 0001b = AIN1 0010b = AIN2 0011b = AIN3 0100b = AIN4 0101b = AIN5 0110b = AIN6 0111b = AIN7 1000b = GND 1001b = GND 1010b = GND 1011b = GND 1100b = GND 1101b = GND 1110b = GND 1111b = GND
3:0	AINN[3:0]	R/W	0001b	Negative multiplexer input selection Selects the negative analog input for the ADC. Analog inputs AIN4 and AIN5 can still be used as analog inputs, even when the inputs are configured as REFP and REFN inputs, respectively. When an analog input is configured as GPIO, the analog input can still be selected by the Mux and used to measure back the voltage on the GPIO pin. 0000b = AIN0 0001b = AIN1 0010b = AIN2 0011b = AIN3 0100b = AIN4 0101b = AIN5 0110b = AIN6 0111b = AIN7 1000b = GND 1001b = GND 1010b = GND 1011b = GND 1100b = GND 1101b = GND 1110b = GND 1111b = GND

8.9 GAIN_CFG Register (Address = 08h) [Reset = 01h]

Return to the Summary Table.

Figure 8-9. GAIN_CFG Register

7	6	5	4	3	2	1	0
SPARE	SYS_MON[2:0]			GAIN[3:0]			
R/W-0b	R/W-000b			R/W-0001b			

Table 8-11. GAIN_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SPARE	R/W	0b	Spare bit Bit setting has no effect. Provided as R/W bit as a means to check the register map CRC.
6:4	SYS_MON[2:0]	R/W	000b	System monitor selection Selects one of the system monitors as the inputs for the PGA. The AINP[3:0] and AINN[3:0] bits have no effect when one of the system monitors is selected. The analog inputs are disconnected from the PGA when a system monitor is selected. The internal reference with the value set in the REF_VAL bit is automatically selected for settings 010b to 101b. Select an appropriate PGA gain setting for the respective measurement. 000b = Disabled 001b = Internal short of differential PGA inputs to (AVDD / 2) 010b = Internal temperature sensor 011b = External (V_{REFP} – V_{REFN}) / 8 100b = AVDD / 8 101b = DVDD / 8 110b = Do not use 111b = Do not use
3:0	GAIN[3:0]	R/W	0001b	PGA gain selection Selects the gain of the PGA. 0000b = 0.5 0001b = 1 0010b = 2 0011b = 4 0100b = 5 0101b = 8 0110b = 10 0111b = 16 1000b = 20 1001b = 32 1010b = 50 1011b = 64 1100b = 100 1101b = 128 1110b = 200 1111b = 256

8.10 REFERENCE_CFG Register (Address = 09h) [Reset = 00h]

Return to the Summary Table.

Figure 8-10. REFERENCE_CFG Register

7	6	5	4	3	2	1	0
REF_UV_EN	RESERVED	REFP_BUF_EN	REFN_BUF_EN	RESERVED	REF_VAL	REF_SEL[1:0]	
R/W-0b	R-0b	R/W-0b	R/W-0b	R-0b	R/W-0b	R/W-00b	

Table 8-12. REFERENCE_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	REF_UV_EN	R/W	0b	Reference voltage monitor enable Enables the voltage reference monitor to detect when the selected voltage reference, as selected by the REF_SEL[1:0] bits, drops below the reference undervoltage threshold. 0b = Disabled 1b = Enabled
6	RESERVED	R	0b	Reserved Always reads back 0b.
5	REFP_BUF_EN	R/W	0b	Positive reference buffer enable Enables the positive reference buffer. Disable the positive reference buffer when the internal reference or the analog supply is selected as the reference source using the REF_SEL[1:0] bit field. 0b = Disabled 1b = Enabled
4	REFN_BUF_EN	R/W	0b	Negative reference buffer enable Enables the negative reference buffer. Disable the negative reference buffer when the internal reference or the analog supply is selected as the reference source using the REF_SEL[1:0] bit field. 0b = Disabled 1b = Enabled
3	RESERVED	R	0b	Reserved Always reads back 0b.
2	REF_VAL	R/W	0b	Internal reference voltage value selection Selects the voltage of the internal reference. The internal voltage reference is always enabled. 0b = 1.25V 1b = 2.5V
1:0	REF_SEL[1:0]	R/W	00b	Reference voltage selection Selects the reference voltage for the ADC. Set GPIO0_CFG[1:0] = 00b and GPIO1_CFG[1:0] = 00b when the external voltage reference is selected. 00b = Internal voltage reference 01b = External voltage reference 10b = AVDD 11b = AVDD

8.11 DIGITAL_CFG Register (Address = 0Ah) [Reset = 00h]

Return to the Summary Table.

Figure 8-11. DIGITAL_CFG Register

7	6	5	4	3	2	1	0
SPARE	REG_MAP_CRC_EN	SPI_CRC_EN	STATUS_EN	FAULT_PIN_BEHAVIOR	CONT_READ_EN	CODING	SDO_MODE
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 8-13. DIGITAL_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SPARE	R/W	0b	Spare bit Bit setting has no effect. Provided as R/W bit as a means to check the register map CRC.
6	REG_MAP_CRC_EN	R/W	0b	Register map CRC enable Enables the register map CRC for register addresses 05h to 0Eh. 0b = Disabled 1b = Enabled
5	SPI_CRC_EN	R/W	0b	SPI CRC enable Enables the SPI CRC on SDI and SDO. 0b = Disabled 1b = Enabled
4	STATUS_EN	R/W	0b	STATUS header output enable Enables the STATUS header (STATUS_MSB + STATUS_LSB registers) transmission on SDO as the first two bytes of every SPI frame. 0b = Disabled 1b = Enabled
3	FAULT_PIN_BEHAVIOR	R/W	0b	$\overline{\text{FAULT}}$ pin behavior selection Selects the behavior of the $\overline{\text{FAULT}}$ pin, when GPIO2 is configured as $\overline{\text{FAULT}}$ output (GPIO2_CFG = 10b or 11b, GPIO2_SRC = 1b). 0b = Static. Output is low when a fault occurred, otherwise output is high. 1b = Heart beat. Output is low when a fault occurred, otherwise output is a 50% duty-cycle signal with a frequency of f_{MOD} / 256.
2	CONT_READ_EN	R/W	0b	Continuous-read mode enable Enables continuous-read mode to allow reading multiple consecutive registers within a single SPI frame in 4-wire SPI mode. Disable continuous-read mode when operating the device in a daisy chain or in 3-wire SPI mode. 0b = Disabled 1b = Enabled
1	CODING	R/W	0b	Conversion data coding selection Selects the coding of the conversion data. 0b = Binary two's complement 1b = Unipolar straight binary
0	SDO_MODE	R/W	0b	SDO/$\overline{\text{DRDY}}$ mode selection Selects the mode of the SDO/$\overline{\text{DRDY}}$ pin to either data-output function only, or to dual-mode function of data output and data ready. Use the data-output only mode when operating the device in a daisy chain. 0b = Data output only mode 1b = Dual mode: data output and data ready

8.12 GPIO_CFG Register (Address = 0Bh) [Reset = 00h]

Return to the Summary Table.

Figure 8-12. GPIO_CFG Register

7	6	5	4	3	2	1	0
GPIO3_CFG[1:0]		GPIO2_CFG[1:0]		GPIO1_CFG[1:0]		GPIO0_CFG[1:0]	
R/W-00b		R/W-00b		R/W-00b		R/W-00b	

Table 8-14. GPIO_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	GPIO3_CFG[1:0]	R/W	00b	GPIO3 configuration Configures the GPIO3 pin behavior. 00b = Disabled (High-Z) 01b = Digital input (CLK_SEL = 0b) or external clock input (CLK_SEL = 1b) 10b = Push-pull digital output (with readback) 11b = Open-drain digital output (with readback)
5:4	GPIO2_CFG[1:0]	R/W	00b	GPIO2 configuration Configures the GPIO2 pin behavior. 00b = Disabled (High-Z) 01b = Digital input 10b = Push-pull digital output (with readback) 11b = Open-drain digital output (with readback)
3:2	GPIO1_CFG[1:0]	R/W	00b	GPIO1 configuration Configures the GPIO1 pin behavior. 00b = Disabled (High-Z) 01b = Digital input 10b = Push-pull digital output (with readback) 11b = Open-drain digital output (with readback)
1:0	GPIO0_CFG[1:0]	R/W	00b	GPIO0 configuration Configures the GPIO0 pin behavior. 00b = Disabled (High-Z) 01b = Digital input 10b = Push-pull digital output (with readback) 11b = Open-drain digital output (with readback)

8.13 GPIO_DATA_OUTPUT Register (Address = 0Ch) [Reset = 00h]

Return to the Summary Table.

Figure 8-13. GPIO_DATA_OUTPUT Register

7	6	5	4	3	2	1	0
GPIO3_SRC	GPIO2_SRC	RESERVED		GPIO3_DAT_OUT	GPIO2_DAT_OUT	GPIO1_DAT_OUT	GPIO0_DAT_OUT
R/W-0b	R/W-0b	R-00b		R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 8-15. GPIO_DATA_OUTPUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO3_SRC	R/W	0b	GPIO3 data source selection Selects the data source of the GPIO3 pin when GPIO3 is configured as digital output. 0b = GPIO3_DAT_OUT bit 1b = $\overline{\text{DRDY}}$
6	GPIO2_SRC	R/W	0b	GPIO2 data source selection Selects the data source of the GPIO2 pin when GPIO2 is configured as digital output. The $\overline{\text{FAULT}}$ pin is low when any of the AVDD_UVn, REF_UVn, REG_MAP_CRC_FAULTn, or MEM_FAULTn status bits are 0b. 0b = GPIO2_DAT_OUT bit 1b = $\overline{\text{FAULT}}$
5:4	RESERVED	R	00b	Reserved Always reads back 00b.
3	GPIO3_DAT_OUT	R/W	0b	GPIO3 data Write value of GPIO3 when configured as digital output. Bit setting has no effect when GPIO3 is configured as digital input or as digital output with $\overline{\text{DRDY}}$ as the data source. 0b = Low 1b = High
2	GPIO2_DAT_OUT	R/W	0b	GPIO2 data Write value of GPIO2 when configured as digital output. Bit setting has no effect when GPIO2 is configured as digital input or as digital output with $\overline{\text{FAULT}}$ as the data source. 0b = Low 1b = High
1	GPIO1_DAT_OUT	R/W	0b	GPIO1 data Write value of GPIO1 when configured as digital output. Bit setting has no effect when GPIO1 is configured as digital input. 0b = Low 1b = High
0	GPIO0_DAT_OUT	R/W	0b	GPIO0 data Write value of GPIO0 when configured as digital output. Bit setting has no effect when GPIO0 is configured as digital input. 0b = Low 1b = High

8.14 IDAC_MAG_CFG Register (Address = 0Dh) [Reset = 00h]

Return to the Summary Table.

Figure 8-14. IDAC_MAG_CFG Register

7	6	5	4	3	2	1	0
I2MAG[3:0]				I1MAG[3:0]			
R/W-0000b				R/W-0000b			

Table 8-16. IDAC_MAG_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	I2MAG[3:0]	R/W	0000b	IDAC2 magnitude selection Selects the value of the excitation current source, IDAC2. 0000b = Disabled 0001b = 1x IUNIT 0010b = 10x IUNIT 0011b = 20x IUNIT 0100b = 30x IUNIT 0101b = 40x IUNIT 0110b = 50x IUNIT 0111b = 60x IUNIT 1000b = 70x IUNIT 1001b = 80x IUNIT 1010b = 90x IUNIT 1011b = 100x IUNIT 1100b = 100x IUNIT 1101b = 100x IUNIT 1110b = 100x IUNIT 1111b = 100x IUNIT
3:0	I1MAG[3:0]	R/W	0000b	IDAC1 magnitude selection Selects the value of the excitation current source, IDAC1. 0000b = Disabled 0001b = 1x IUNIT 0010b = 10x IUNIT 0011b = 20x IUNIT 0100b = 30x IUNIT 0101b = 40x IUNIT 0110b = 50x IUNIT 0111b = 60x IUNIT 1000b = 70x IUNIT 1001b = 80x IUNIT 1010b = 90x IUNIT 1011b = 100x IUNIT 1100b = 100x IUNIT 1101b = 100x IUNIT 1110b = 100x IUNIT 1111b = 100x IUNIT

8.15 IDAC_MUX_CFG Register (Address = 0Eh) [Reset = 10h]

Return to the Summary Table.

Figure 8-15. IDAC_MUX_CFG Register

7	6	5	4	3	2	1	0
IUNIT	I2MUX[2:0]			RESERVED	I1MUX[2:0]		
R/W-0b	R/W-001b			R-0b	R/W-000b		

Table 8-17. IDAC_MUX_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	IUNIT	R/W	0b	IDAC unit current selection Selects the unit current for the excitation current sources, IDAC1 and IDAC2. 0b = 1µA 1b = 10µA
6:4	I2MUX[2:0]	R/W	001b	IDAC2 output pin selection Selects the output pin for IDAC2. IDAC1 and IDAC2 can be routed to the same pin if needed. An analog input that is used as an IDAC2 output, can still be used as an analog or reference input. 000b = AIN0 001b = AIN1 010b = AIN2 011b = AIN3 100b = AIN4 101b = AIN5 110b = AIN6 111b = AIN7
3	RESERVED	R	0b	Reserved Always reads back 0b.
2:0	I1MUX[2:0]	R/W	000b	IDAC1 output pin selection Selects the output pin for IDAC1. IDAC1 and IDAC2 can be routed to the same pin if needed. An analog input that is used as an IDAC1 output, can still be used as an analog or reference input. 000b = AIN0 001b = AIN1 010b = AIN2 011b = AIN3 100b = AIN4 101b = AIN5 110b = AIN6 111b = AIN7

8.16 REG_MAP_CRC Register (Address = 0Fh) [Reset = 00h]

Return to the Summary Table.

Figure 8-16. REG_MAP_CRC Register

7	6	5	4	3	2	1	0
REG_MAP_CRC_VAL[7:0]							
R/W-00000000b							

Table 8-18. REG_MAP_CRC Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REG_MAP_CRC_VAL[7:0]	R/W	00000000b	Register map CRC value The register map CRC value is the user-computed CRC value of registers 05h to 0Eh. The CRC value written to this register is compared to an internal CRC calculation. If the values do not match, the REG_MAP_CRC_FAULTn bit in the STATUS_MSB register is set. Enable the register map CRC using the REG_MAP_CRC_EN bit.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Serial Interface Connections

Figure 9-1 shows the basic interface connections for the ADS1x2S14.

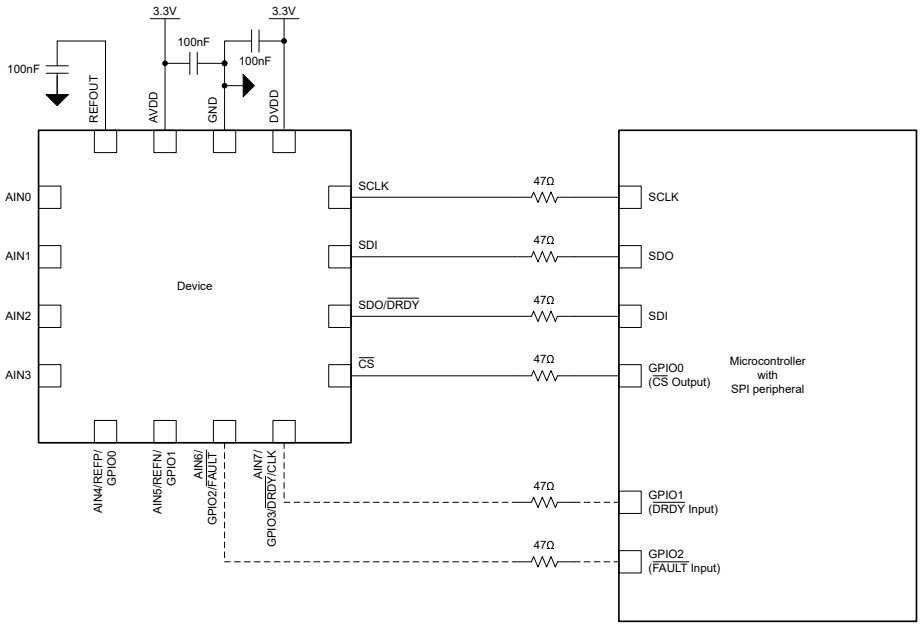


Figure 9-1. Serial Interface Connections

Most microcontroller SPI peripherals can interface with the device. The interface only supports the SPI configuration (CPOL = 0 and CPHA = 1), where SCLK idles low and data are launched or changed on SCLK rising edges; data are latched or read on SCLK falling edges.

The $\overline{\text{CS}}$ pin can be tied to GND permanently to operate the device in 3-wire SPI mode.

Optionally, route the dedicated $\overline{\text{DRDY}}$ pin to a falling edge triggered interrupt-capable GPIO of the host controller in case new data ready indication through an interrupt is desired. For that purpose, configure the AIN7/GPIO3/$\overline{\text{DRDY}}$/CLK pin as a $\overline{\text{DRDY}}$ output (GPIO3_CFG = 10b or 11b and GPIO3_SRC = 1b).

The $\overline{\text{FAULT}}$ pin can be interfaced to the host controller as well in case fault indication through a pin is desired besides the fault indication through the fault flags. For that purpose, configure the AIN6/GPIO2/$\overline{\text{FAULT}}$ pin as a $\overline{\text{FAULT}}$ output (GPIO2_CFG = 10b or 11b and GPIO2_SRC = 1b).

Add pullup resistors at the $\overline{\text{DRDY}}$ or $\overline{\text{FAULT}}$ pins to DVDD in case the pins are configured as open-drain outputs.

Pullup or pulldown resistors can be placed on the digital input and output signal lines in case certain signal levels needs to be driven during power up of the device or the microcontroller.

Optionally, place resistors in series with all digital input and output pins. Typical series resistor values range from 10Ω to 50Ω. This resistance smooths sharp signal transitions, suppresses overshoot, and offers some

overvoltage protection. Care must be taken to meet all SPI timing requirements because the additional resistors interact with the bus capacitance present on the digital signal lines.

9.1.2 Interfacing with Multiple Devices

The ADS1x2S14 offer two methods to operate multiple devices on a single SPI bus:

- Daisy-chaining using a single $\overline{CS}$ signal for all devices as explained in the Daisy-Chain Operation section. The host connects to SDI of the first device in the chain to transmit data. The SDO signal of the first device in the chain connects to the SDI signal of the next device, and so on. The host controller receives data from the SDO signal of the last device in the chain. All devices share the same SCLK signal. This method allows the host to talk to all devices in the chain at the same time. However, depending on the number of devices connected in the chain, the SPI frame can get very long.
- Using a dedicated $\overline{CS}$ signal for each device as shown in Figure 9-2. All devices share the SCLK, SDI and SDO/$\overline{DRDY}$ signals in this case. Only the device with $\overline{CS}$ low drives the SDO/$\overline{DRDY}$ pin. The SDO/$\overline{DRDY}$ outputs of all other devices, which have $\overline{CS}$ high, are in a high-Z state to avoid contention on the SDO line. The host controller interfaces with each device one at a time.

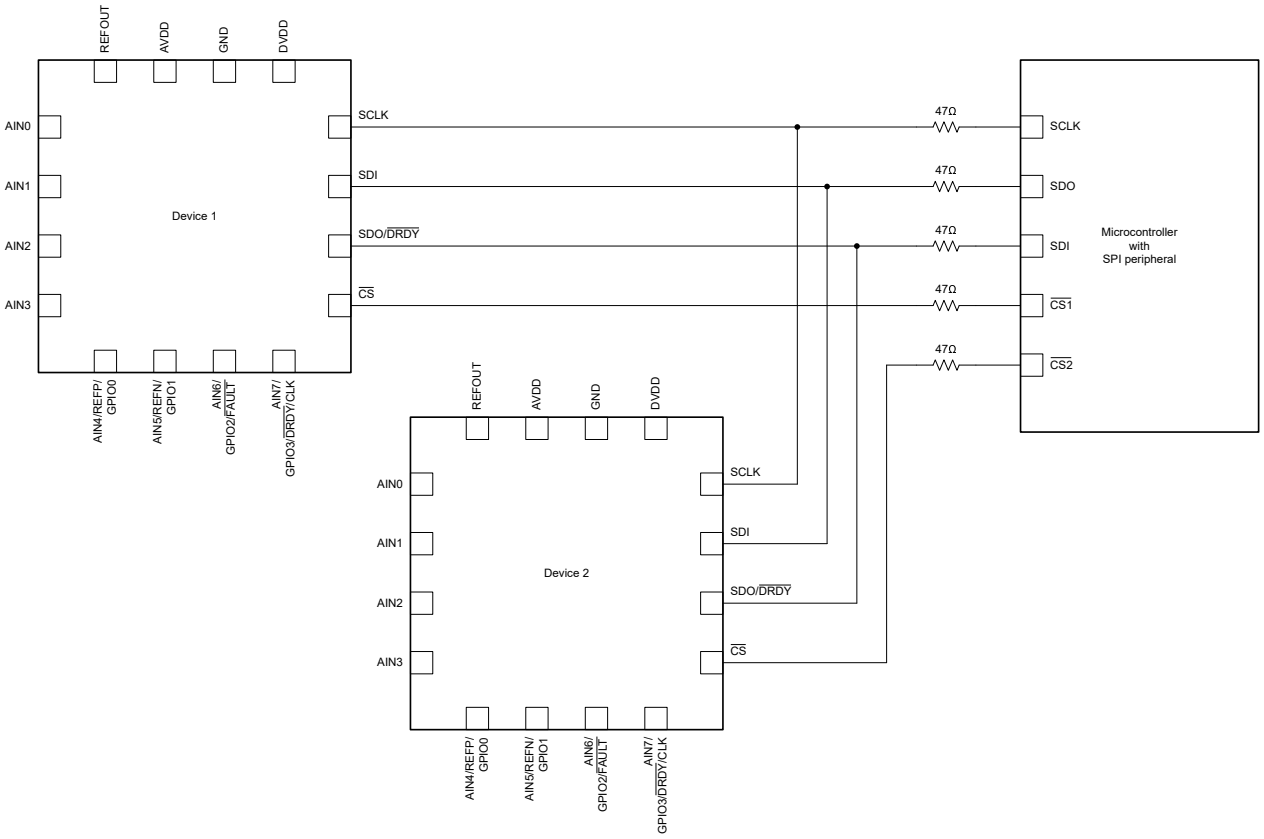


Figure 9-2. Multiple Device Serial Interface Connections using individual $\overline{CS}$ Signals

9.1.3 Unused Inputs and Outputs

Follow these guidelines for unused device pin connections:

- Leave any unused analog inputs floating or connect the unused analog inputs to GND.
- When not using the REFP, REFN, GPIO0, GPIO1, GPIO2, GPIO3, $\overline{FAULT}$, $\overline{DRDY}$, or CLK functions, configure the respective pins as analog inputs (GPIOx_CFG[1:0] = 00b) and follow the guidelines for unused analog inputs above.
- Tie the $\overline{CS}$ pin to GND when using 3-wire SPI mode.

9.1.4 Device Initialization

Figure 9-3 illustrates the sequence steps required to initialize the ADS1x2S14, and to start conversions in continuous-conversion mode. In this example, the device uses the dedicated $\overline{\text{DRDY}}$ pin to indicate availability of new conversion data to the host controller.

Configure the SPI of the host controller to CPOL = 0 and CPHA = 1. Configure the host controller GPIO connected to the device $\overline{\text{DRDY}}$ pin as a falling edge triggered interrupt input.

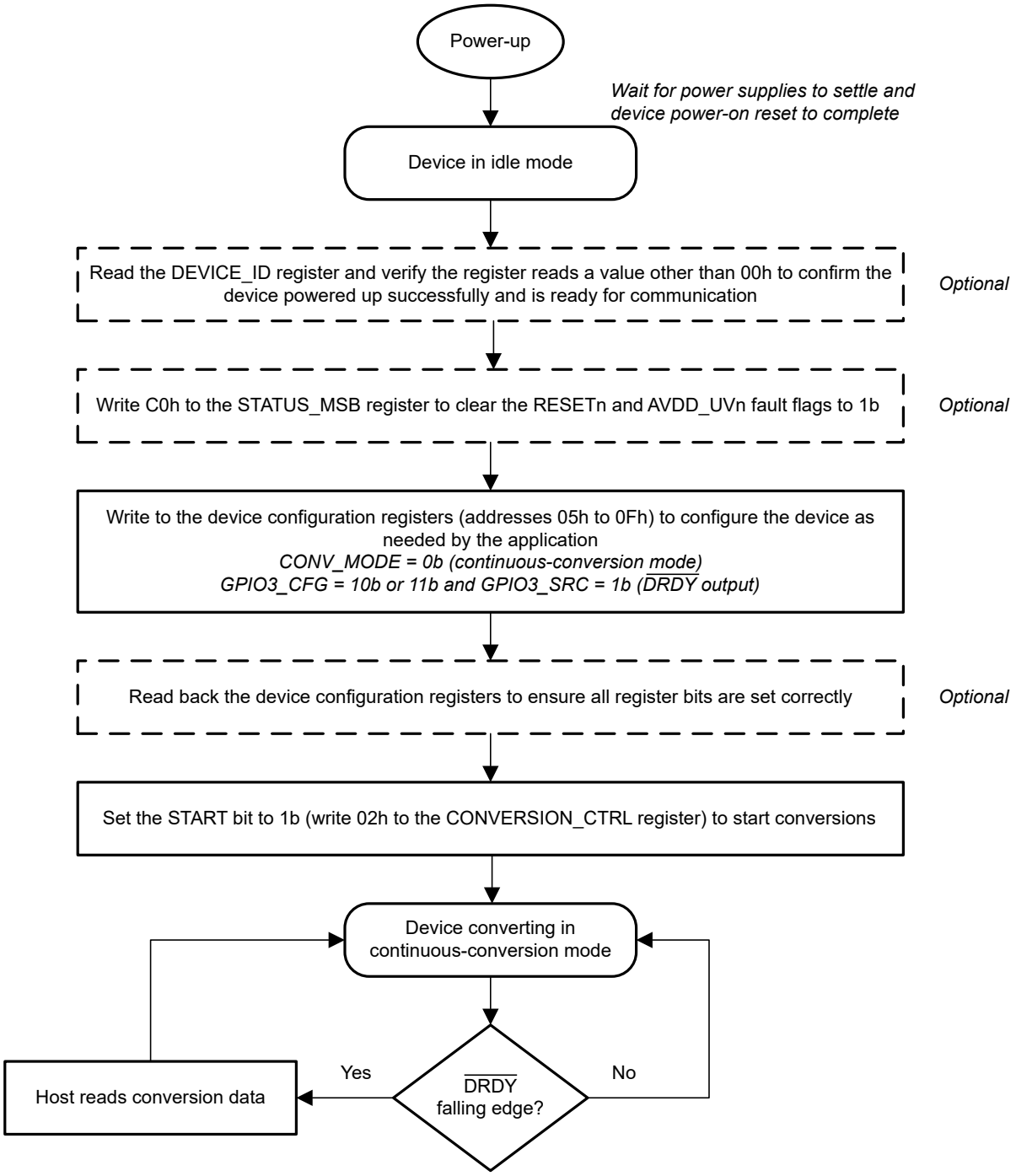


Figure 9-3. Device Initialization Flow Chart

9.2 Typical Applications

9.2.1 Software-Configurable RTD Measurement Input

The ADS1x2S14 integrate all necessary features (such as excitation current sources, buffered external reference inputs, and a PGA) to implement a ratiometric RTD measurement input module, which accommodates 2-, 3-, and 4-wire RTDs by means of software configuration. Figure 9-4 shows an example implementation for such a software-configurable RTD measurement input module.

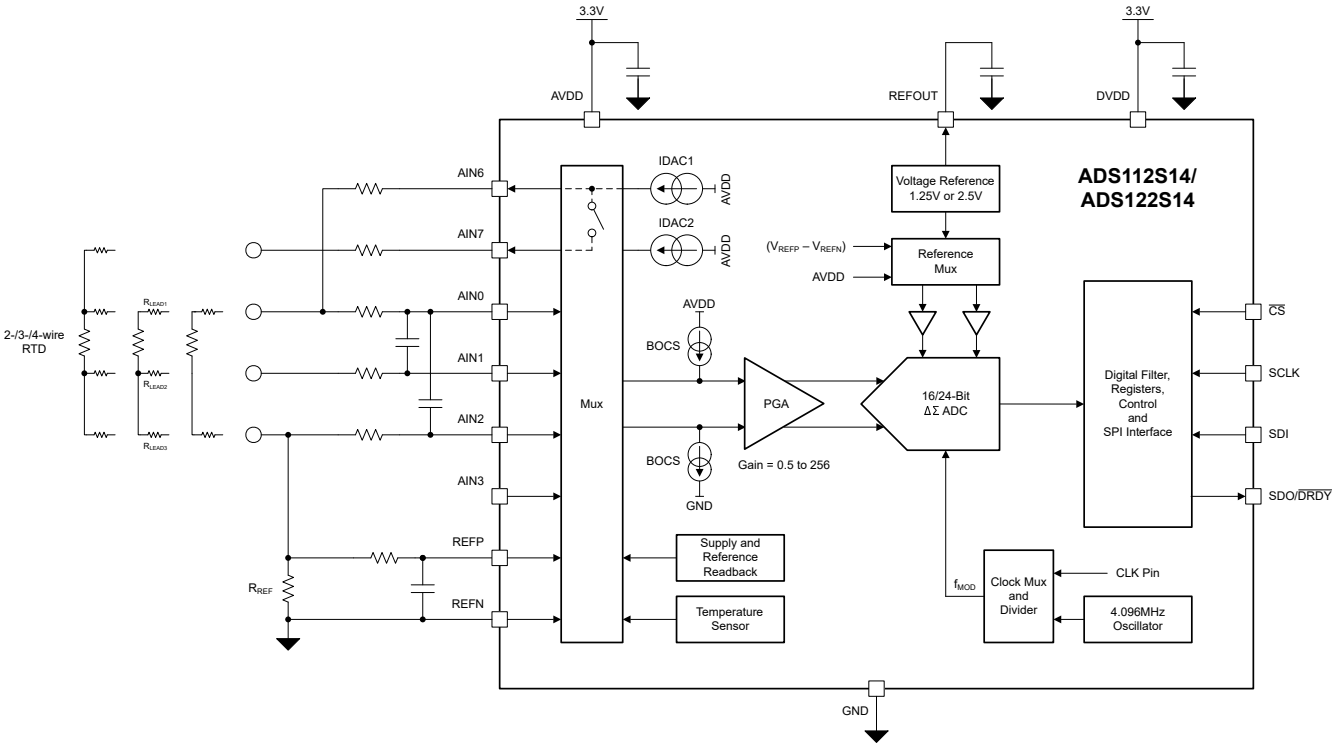


Figure 9-4. Software-Configurable RTD Measurement Input

9.2.1.1 Design Requirements

Table 9-1. Design Parameters

DEISGN PARAMETER	VALUE
Supply voltage	3.3V
Supported RTD types	2-, 3-, 4-wire Pt100
Current consumption	500µA (max)
Temperature measurement range	–200°C to +850°C
Measurement accuracy at T_A = 25°C	±0.1°C
Line-cycle rejection at 50Hz or 60Hz (±1Hz)	80dB (min)
Maximum overvoltage at the RTD terminals	±10V

9.2.1.2 Detailed Design Procedure

The circuit in Figure 9-4 employs a ratiometric measurement configuration. In other words, the sensor signal (that is, the voltage across the RTD in this case) and the reference voltage for the ADC are derived from the same excitation source. Therefore, errors resulting from temperature drift or noise of the excitation source cancel because these errors are common to both the sensor signal and the reference.

To implement a ratiometric RTD measurement using the device, route IDAC1 to either AIN7 (for a 4-wire RTD connection) or to AIN6 (for 2- and 3-wire RTD connections) using the I1MUX[2:0] bits. Select the excitation current source value using the I1MAG[3:0] bits. The excitation current flows through the RTD and a precision, low-drift reference resistor, R_{REF} to ground. The voltage, V_{REF}, generated across the reference resistor (as shown in Equation 14) is used as the ADC reference voltage. For that purpose, select the external voltage reference between pins AIN4/REFP and AIN5/REFN using the REF_SEL[1:0]

$$V_{REF} = I_{IDAC1} \times R_{REF} \quad (14)$$

To simplify the following discussion, the individual lead resistance values of the RTDs (R_{LEADx}) are set to zero. As Equation 15 shows, IDAC1 excites the RTD to produce a voltage (V_{RTD}) proportional to the temperature-dependent RTD value and the IDAC1 value.

$$V_{RTD} = R_{RTD} \times I_{IDAC1} \quad (15)$$

Select the analog inputs using the AINP[3:0] and AINN[3:0] bits to measure V_{RTD} based on the RTD type:

- For a 2-wire RTD, measure between AIN_P = AIN0 and AIN_N = AIN2.
- For a 3- or 4-wire RTD, measure between AIN_P = AIN0 and AIN_N = AIN1.

The device internally amplifies the voltage across the RTD using the PGA and compares the resulting voltage against the reference voltage to produce a digital output code according to Equation 16.

$$Code / 2^n = V_{RTD} \times Gain / V_{REF} = (R_{RTD} \times I_{IDAC1} \times Gain) / (I_{IDAC1} \times R_{REF}) \quad (16)$$

$$Code / 2^n = (R_{RTD} \times Gain) / R_{REF} \quad (17)$$

Where n depends on the selected coding scheme and the ADC resolution:

- n = 15 (16bit ADC, binary two's complement format)
- n = 16 (16bit ADC, unipolar straight binary format)
- n = 23 (24bit ADC, binary two's complement format)
- n = 24 (24bit ADC, unipolar straight binary format)

As shown in Equation 17, the output code only depends on the value of the RTD, the PGA gain, and the reference resistor (R_{REF}), but not on the IDAC1 value. The absolute accuracy and temperature drift of the excitation current therefore does not matter. However, because the value of the reference resistor directly affects the measurement result, choosing a reference resistor with good initial accuracy and very low temperature coefficient is important to limit measurement errors introduced by R_{REF}.

The reference resistor R_{REF} not only serves to generate the reference voltage for the device, but also sets the voltages at the leads of the RTD to within the specified absolute input voltage range of the PGA. This is important in case PGA gains greater than 10 are used, because the PGA needs headroom from GND to operate when using gains greater than 10.

When designing the circuit, care must also be taken to meet the compliance voltage requirement of the IDAC. The IDAC requires that the maximum voltage drop developed across the current path to GND be equal to or less than the specified compliance voltage to operate accurately.

As stated in the Design Requirements, this design example discusses the circuit implementation for a Pt100 element measuring temperatures ranging from –200°C to +850°C. The excitation current for the Pt100 is chosen as I_{IDAC1} = 400µA to meet the required power budget of this example. As mentioned previously, besides creating the reference voltage for the ADC, the voltage across R_{REF} also sets the absolute input voltages for the RTD measurement. In general, select the largest reference voltage possible that maintains the compliance voltage of the IDAC and meets the absolute input voltage requirement of the PGA. Setting the common-mode voltage at or below half the analog supply is a good starting point for a design. 1.6V is used as the target common-mode voltage in this example. Consequently, use Equation 18 to calculate the value for R_{REF}:

$$R_{REF} = V_{REF} / I_{IDAC1} = 1.6V / 400\mu A = 4k\Omega \quad (18)$$

The stability of R_{REF} is critical to achieve good measurement accuracy over temperature and time. Choosing a reference resistor with a temperature coefficient of ±10ppm/°C or better is advisable.

As a last step, select the PGA gain to match the maximum input signal to the FSR of the ADC. The resistance of a Pt100 increases with temperature. Therefore, the maximum voltage to be measured (V_{INMAX}) occurs at the positive temperature extreme. At 850°C, a Pt100 has an equivalent resistance of approximately 391Ω as per the NIST tables. The voltage across the Pt100 equates to Equation 19:

$$V_{INMAX} = V_{RTD\ (at\ 850°C)} = R_{RTD\ (at\ 850°C)} \times I_{IDAC1} = 391\Omega \times 400\mu A = 156.4mV \quad (19)$$

The maximum gain that can be applied when using a 1.6V reference is then calculated as (1.6V / 156.4mV) = 10.23. The next smaller PGA gain setting available in the ADS1x2S14 is 10. At a gain of 10, the device offers an FSR value as described in Equation 20:

$$FSR = \pm V_{REF} / Gain = \pm 1.6V / 10 = \pm 160mV \quad (20)$$

This range allows for margin with respect to initial accuracy and drift of the IDACs and reference resistor.

To keep the ADC power consumption at a minimum, speed mode 0 (f_{MOD} = 32kHz) is selected using the SPEED_MODE[1:0] bits. And to meet the line-cycle rejection requirement at 50Hz and 60Hz, the 20SPS output data rate is chosen using the FLTR_OSR[2:0] bits. The measurement *resolution* (determined by the ADC noise) increases at the expense of higher power consumption, when choosing a faster speed mode with the same 20SPS output data rate setting. However the measurement *accuracy* (determined by the ADC DC errors, such as gain and offset error) is largely unaffected by the speed mode setting.

The primary purpose of the series resistors at the analog and positive reference inputs is to protect the device inputs from any overvoltage conditions. In case overvoltage conditions at the RTD terminals can occur in the application, select the series resistor value such that the currents into the analog and positive reference inputs get limited to less than 10mA. Series resistor values of 2.2kΩ are chosen in this example to limit the input currents to less than 5mA when overvoltages up to ±10V are present at the RTD terminals. Consider the interaction of the series resistors with the input currents into the analog and reference inputs when selecting the resistor values. The voltage drop created across the series resistors causes a potential offset error. In addition, the series resistors together with the input capacitors form first order RC antialiasing filters. The exact corner frequency of the RC filters is not very critical with this delta-sigma ADC. A general recommendation is to select a corner frequency which is at least 10 times lower than the modulator frequency of the ADC.

After selecting the values for the IDAC, R_{REF}, PGA gain, and the series resistors, make sure to double check that the settings meet the absolute input voltage requirements of the PGA and the compliance voltage of the IDAC. Include the voltage drop created by IDAC1 across the RTD lead resistances and the series resistor at the IDAC1 output pin in the calculations.

Lead-wire compensation for 3-wire RTDs in this example is achieved by implementing a two-step measurement approach.

1. In step one, measure the voltage (V_1) between AIN0 and AIN1.
2. In a second measurement step, measure the voltage (V_2) between AIN0 and AIN2.

Equation 21 and Equation 22 represent the two measurements.

$$V_1 = I_{IDAC1} (R_{LEAD1} + R_{RTD}) \quad (21)$$

$$V_2 = I_{IDAC1} (R_{LEAD1} + R_{RTD} + R_{LEAD3}) \quad (22)$$

To assume that all three lead resistances have the same value, R_{LEAD}, is reasonable. Consequently, use Equation 23 to calculate the lead-wire compensated RTD voltage.

$$V_{RTD} = 2 \times V_1 – V_2 = 2 \times [I_{IDAC1} (R_{LEAD} + R_{RTD})] – I_{IDAC1} (2 \times R_{LEAD} + R_{RTD}) = I_{IDAC1} \times R_{RTD} \quad (23)$$

RTD Measurement Register Bit Settings shows the critical register bit settings for the various measurements in this design example.

Table 9-2. RTD Measurement Register Bit Settings

REGISTER BITS	2-WIRE RTD	3-WIRE RTD		4-WIRE RTD
		V_1	V_2	
SPEED_MODE[1:0]	00b (Speed Mode 0)			
FLTR_OSR[2:0]	111b (f_{DATA} = 20SPS)			
GAIN[3:0]	0110b (Gain = 10)			
REFP_BUF_EN	1b (REFP buffer enabled)			
REFN_BUF_EN	0b (REFN buffer disabled)			
REF_SEL[1:0]	01b (External reference)			
IUNIT	1b (IUNIT = 10µA)			
I2MAG[3:0]	0000b (IDAC2 disabled)			
I2MUX[2:0]	Don't care			
I1MAG[3:0]	0101b (I_{IDAC1} = 40 × IUNIT)			
I1MUX[2:0]	110b (AIN6)	110b (AIN6)	110b (AIN6)	111b (AIN7)
AINP[3:0]	0000b (AIN0)	0000b (AIN0)	0000b (AIN0)	0000b (AIN0)
AINN[3:0]	0010b (AIN2)	0001b (AIN1)	0010b (AIN2)	0001b (AIN1)

For more information about RTD measurement circuits and the implementation using TI ADCs see the *A Basic Guide to RTD Measurements* application note. Various strategies for sensor fault detection using features similar to the ones integrated in ADS1x2S14 are discussed in the *RTD Wire-Break Detection Using Precision Delta-Sigma ADCs* application note. A software library using C code showing how to implement the RTD linearization algorithm in the host controller is available *here*.

9.2.1.3 Application Performance Plots

Figure 9-5 and Figure 9-6 show the measurement results for a 4-wire Pt100. The measurements are taken at T_A = 25°C using precision resistors instead of a 4-wire Pt100. Figure 9-5 shows both the resistance measurement error without any calibration and after a system offset and gain calibration. The respective temperature measurement error in Figure 9-6 is calculated from the offset and gain error corrected data in Figure 9-5 using the NIST tables.

The design meets the required temperature measurement accuracy given in the Design Requirements. However, the measurement error shown in Figure 9-6 does not include the error of the RTD.

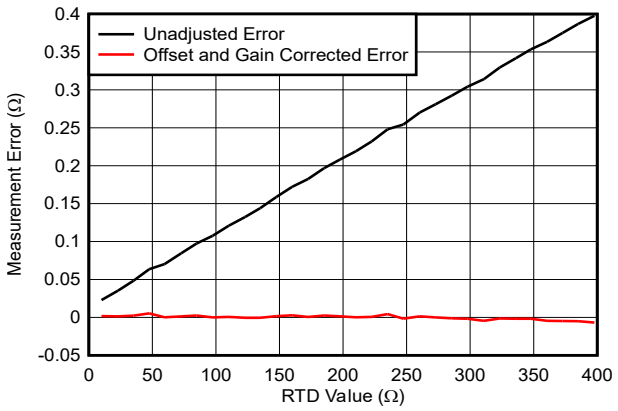


Figure 9-5. Resistance Measurement Error vs RTD Resistance

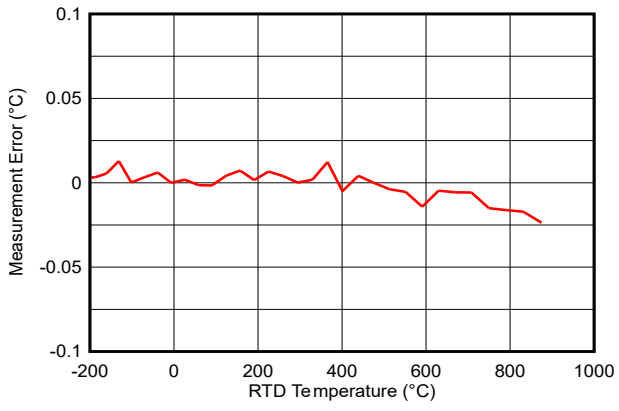


Figure 9-6. Temperature Measurement Error vs RTD Temperature

9.2.1.4 Design Variant – 3-Wire RTD Measurement With Automatic Lead-Wire Compensation Using Two IDACs

The circuit implementation shown in Figure 9-4 requires two measurements to compensate for the lead-wire resistance of a 3-wire RTD. Alternatively, leverage the second IDAC to implement automatic 3-wire RTD lead-wire compensation as shown in Figure 9-7, which does not require a separate lead wire resistance measurement step.

For that purpose, route IDAC2 to AIN3 and connect AIN3 to the point where the terminal connects to the series resistor in front of AIN1. Change both excitation current values from 400µA to 200µA (or the reference resistor value from 4kΩ to 2kΩ) in this configuration and the PGA gain from 10 to 20. A single measurement between AIN0 and AIN1 is sufficient to get a lead-wire compensated RTD value. Use Equation 24 to calculate the resistance of the 3-wire RTD in this implementation.

$$\text{Code} / 2^{n} = (R_{RTD} \times \text{Gain}) / (2 \times R_{REF}) \quad (24)$$

Where n follows the guidelines of Equation 17.

For more details see the *A Basic Guide to RTD Measurements* application note.

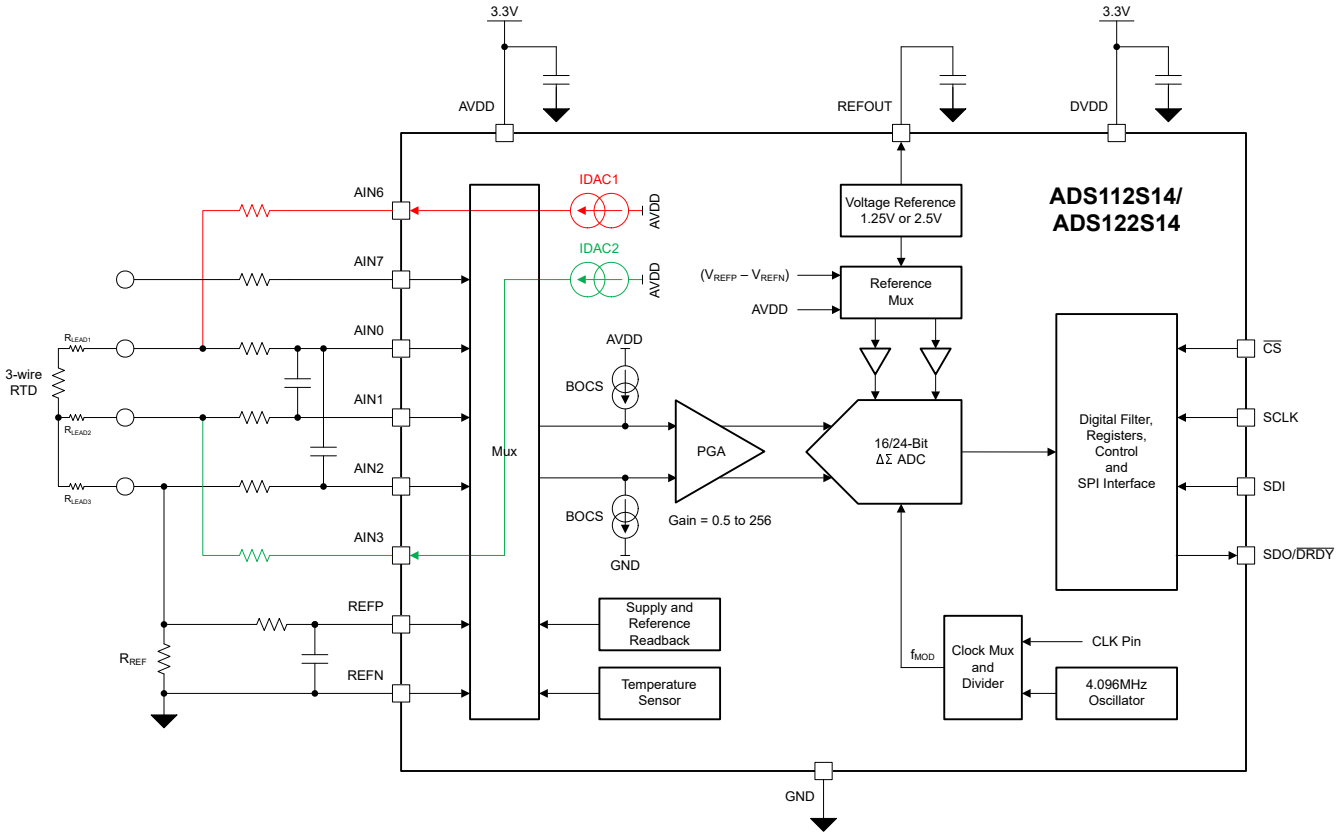


Figure 9-7. 3-wire RTD Measurement Implementation Using Two IDACs for Automatic Lead-Wire Compensation

9.2.2 Thermocouple Measurement With Cold-Junction Compensation Using a 2-wire RTD

Figure 9-8 shows the implementation of a thermocouple measurement using a 2-wire RTD for cold-junction temperature measurement. Other ways to measure the cold-junction temperature can be used with the ADS1x2S14 as well, such as a thermistor (for example TMP61), an analog output temperature sensor (for example LMT70A), or using the integrated temperature sensor.

Equation 25 provides the relationship between ADC codes and the thermocouple voltage (V_{TC}) measured between AIN0 and AIN1.

$$\text{Code} / 2^n = (V_{TC} \times \text{Gain}) / V_{REF} \quad (25)$$

Where n follows the guidelines of Equation 17.

An important aspect of the circuit implementation is the biasing of the thermocouple so that the voltages at the thermocouple terminals meet the input voltage requirements of the ADS1x2S14. In this example pullup and pulldown resistors (typically in the range of 1MΩ to 10MΩ) in front of the RC filter are used to bias the thermocouple output voltage to AVDD / 2. At the same time, the pullup and pulldown resistors serve as a means to detect an open sensor connection. In case of an open sensor connection, the positive analog input (AIN0) is pulled to AVDD, and the negative analog input (AIN1) to GND. This condition leads to a measurement result which is outside the normal measurement range for the thermocouple.

Many other ways to bias the thermocouple can be used as well. For example the reference output voltage can be used by connecting REFOUT to the negative thermocouple terminal instead of the pulldown resistor. For more information about thermocouple measurement circuits and the implementation using TI ADCs see the *A Basic Guide to Thermocouple Measurements* application note. A software library using C code showing how to implement the thermocouple linearization and cold-junction compensation algorithms in the host controller is available *here*.

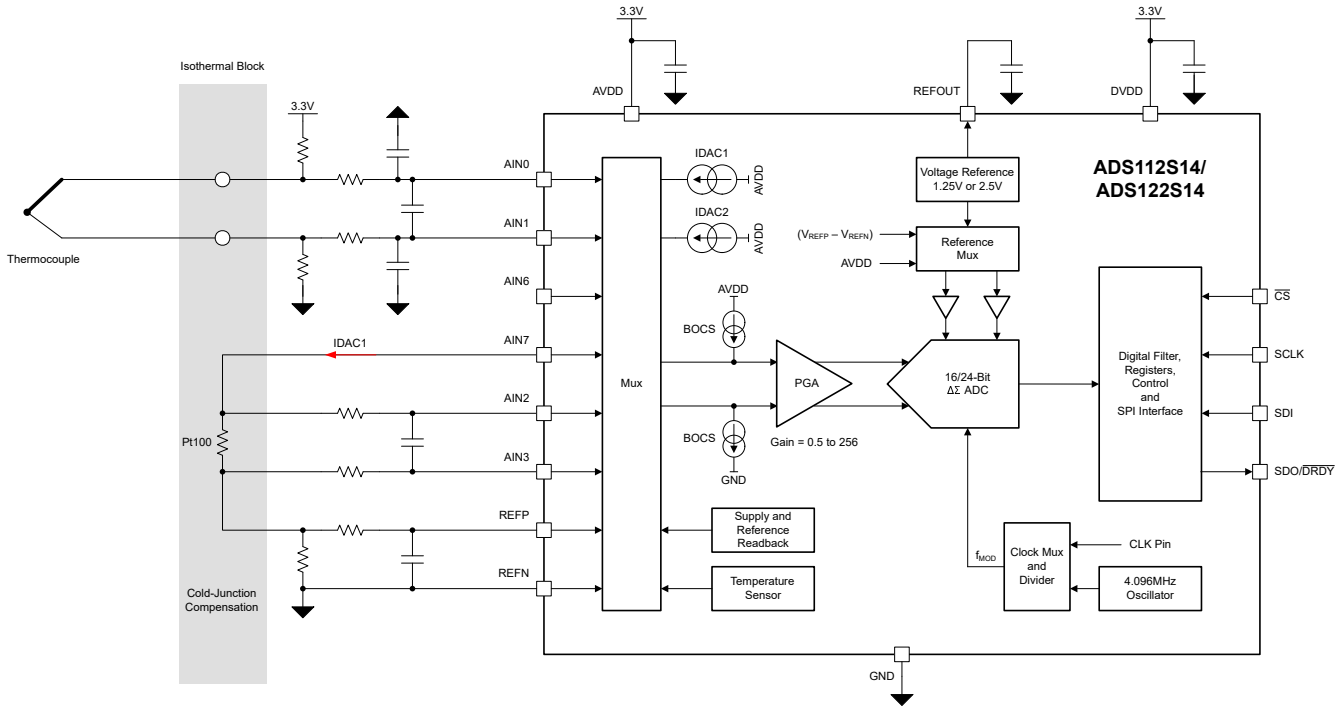


Figure 9-8. Thermocouple Measurement With Cold-Junction Compensation Using a 2-wire RTD

9.2.3 Resistive Bridge Sensor Measurement With Temperature Compensation

Figure 9-9 and Figure 9-10 show two examples of how to implement a resistive bridge sensor measurement with temperature compensation using the ADS1x2S14. The bridge temperature is typically used in the host controller to compensate for the bridge temperature drift.

The circuit implementation in Figure 9-9 uses the analog supply to excite the bridge sensor. Use the bridge excitation voltage as the external reference voltage for the ADC to implement a *ratiometric* bridge measurement. Instead of the analog supply, one of the integrated excitation current sources can be used to excite the bridge as well. Equation 26 through Equation 28 show how to derive the relationship between ADC output codes and the applied bridge signal using a pressure sensor as an example. Equation 28 shows that the output codes are independent of the excitation voltage in this ratiometric circuit implementation.

$$V_{Bridge} = V_{AIN2} - V_{AIN3} = (Pressure_{APL} / Pressure_{MAX}) \times Sensitivity \times V_{Excitation} \quad (26)$$

$$Code / 2^n = V_{Bridge} \times Gain / V_{REF} \quad (27)$$

$$Code / 2^n = (Pressure_{APL} / Pressure_{MAX}) \times Sensitivity \times Gain \quad (28)$$

Where:

- $V_{Excitation} = V_{REF} = AVDD$
- $Pressure_{APL}$ = the applied pressure
- $Pressure_{MAX}$ = the maximum capacity of the pressure sensor. Means the pressure where the bridge sensor outputs the full-scale output signal
- Sensitivity = the sensitivity of the bridge sensor typically given in mV/V of bridge excitation
- n follows the guidelines of Equation 17

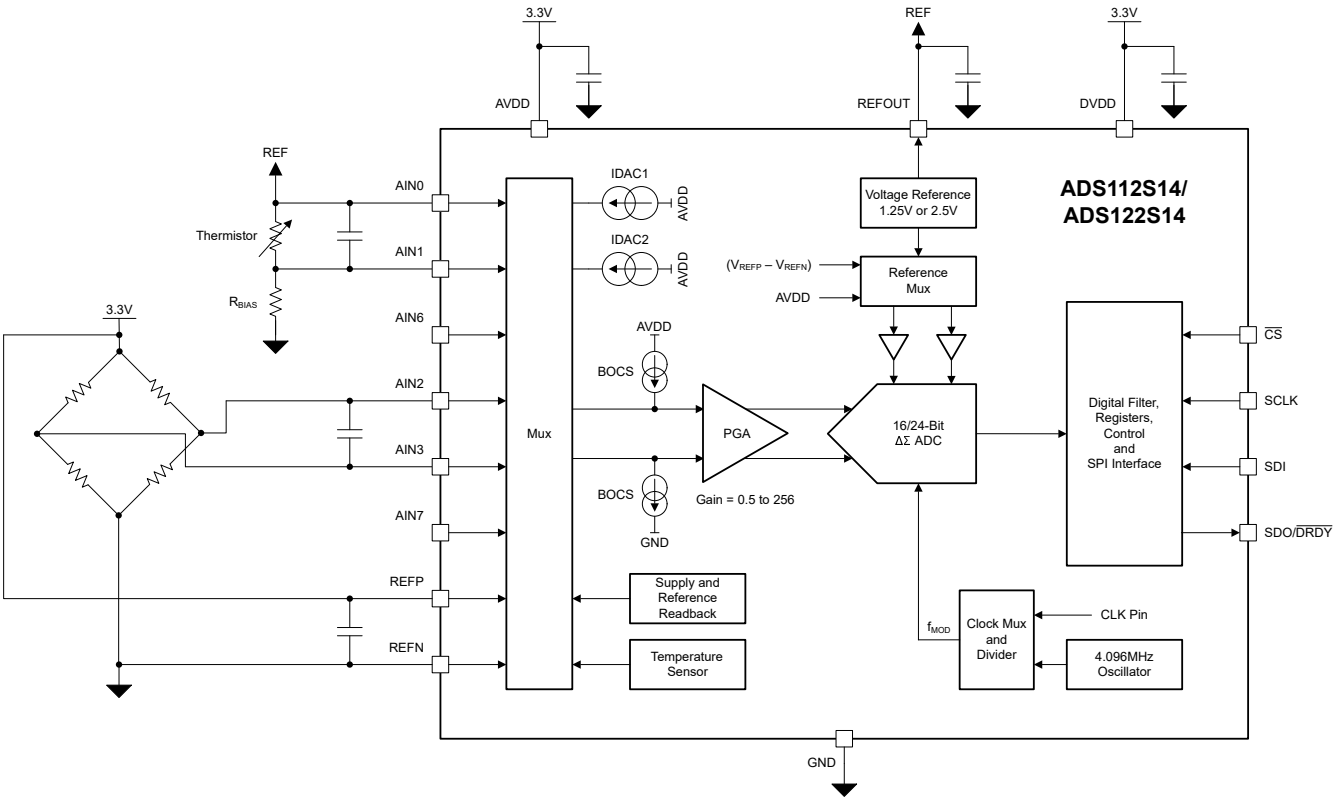


Figure 9-9. Resistive Bridge Sensor Measurement Example 1
(Using the Analog Supply as Bridge Excitation and a Thermistor for Bridge Temperature Measurement)

The example shows a thermistor to measure the bridge temperature. The reference voltage output is used in this case to implement a *ratiometric* thermistor measurement. The conversion result according to Equation 30 is only dependent on the bias resistor (R_{BIAS}) and the PGA gain setting.

$$V_{Thermistor} = V_{AIN0} - V_{AIN1} = V_{REF} \times R_{Thermistor} / (R_{Thermistor} + R_{BIAS}) \quad (29)$$

$$Code / 2^n = (V_{Thermistor} \times Gain) / V_{REF} = (R_{Thermistor} \times Gain) / (R_{Thermistor} + R_{BIAS}) \quad (30)$$

Where n follows the guidelines of Equation 17.

Figure 9-10 shows an alternative circuit implementation where the reference output is used to excite the bridge and the measurement of the temperature-dependent bridge resistance (measurement between AIN0 and AIN3) is used to determine the bridge temperature. Similar to the thermistor measurement above, the bridge resistance measurement is ratiometric and only dependent on the bias resistor and the PGA gain setting as shown in Equation 31.

$$Code / 2^n = (R_{Bridge} \times Gain) / (R_{Bridge} + R_{BIAS}) \quad (31)$$

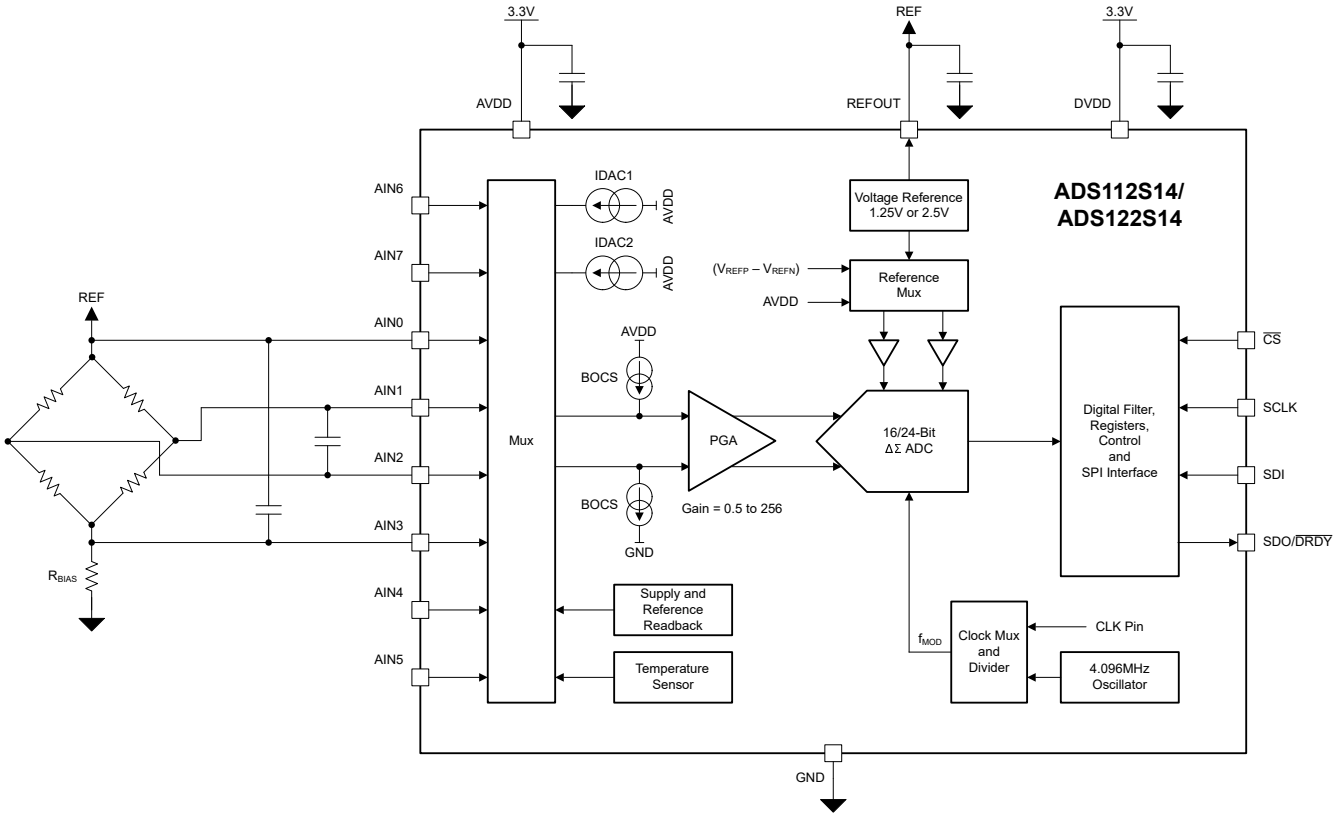


Figure 9-10. Resistive Bridge Sensor Measurement Example 2 (Using the Reference Output as Bridge Excitation and the Bridge Resistance as Temperature Measurement)

Use one of the GPIO outputs to control a switch placed between the bridge sensor and GND for applications where the bridge sensor needs to be powered down periodically to save power.

For more information about resistive bridge sensor measurement circuits and the implementation using TI ADCs see the *A Basic Guide to Bridge Measurements* application note.

9.3 Power Supply Recommendations

9.3.1 Power Supplies

The device requires two power supplies: analog (AVDD) and digital (DVDD). The analog power supply can be independently chosen from the digital power supply. The DVDD supply sets the logic levels for the serial interface pins ($\overline{CS}$, SCLK, SDI, SDO/$\overline{DRDY}$). The AVDD supply sets the logic levels for the GPIOs (GPIO0 to GPIO3).

9.3.2 Power-Supply Sequencing

The power supplies can be sequenced in any order, but in no case must any analog or digital inputs exceed the respective analog or digital power-supply voltage and current limits. Wait $t_{d(POR)}$ after the DVDD supply stabilized before communicating with the device to allow the power-on reset process to complete.

9.3.3 Power-Supply Decoupling

Good power-supply decoupling is important to achieve optimum device performance. As shown in Figure 9-11, AVDD and DVDD must each be decoupled with at least a 100nF capacitor to GND. Place the supply bypass capacitors as close to the device power-supply pins as possible using low-impedance connections. Use multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins can offer enhanced noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes.

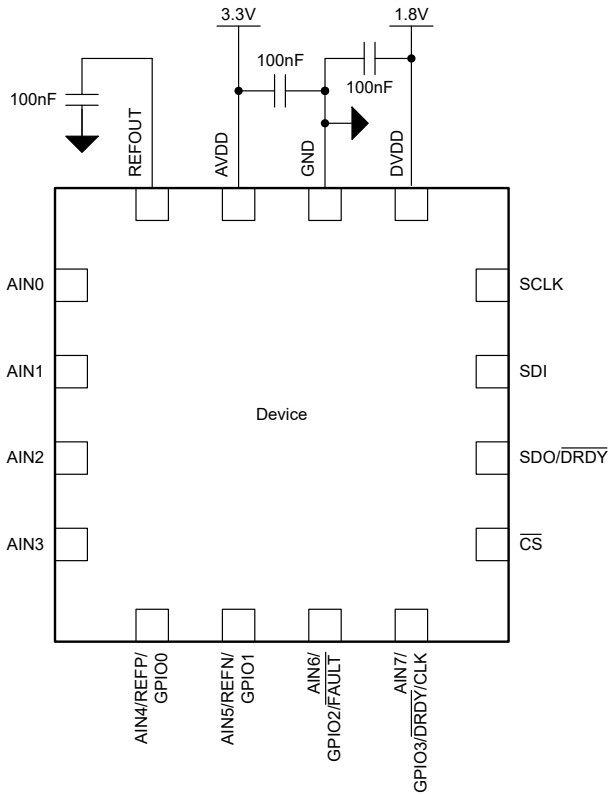


Figure 9-11. Power Supply Decoupling

9.4 Layout

9.4.1 Layout Guidelines

The following basic recommendations for the ADS1x2S14 layout help achieve the best possible performance of the ADC.

- For best performance, dedicate an entire PCB layer to a ground plane and do not route any other signal traces on this layer.
- Use ceramic capacitors (for example, X7R grade) for the power-supply decoupling capacitors. High-K capacitors (Y5V) are not recommended. Place the required capacitors as close as possible to the device pins using short, direct traces. Placing the bypass capacitors on the same layer as close to the device yields the best results.
- Route digital traces away from all analog inputs and associated components to minimize interference.
- Provide good ground return paths. Signal return currents flow on the path of least impedance. If the ground plane is cut or has other traces that block the current from flowing right next to the signal trace, another path must be found to return to the source and complete the circuit. If forced into a larger path, the chance that the signal radiates increases. Sensitive signals are more susceptible to EMI interference.
- Consider the resistance and inductance of the routing. Often, traces for the inputs have resistances that react with the input bias current and cause an added error voltage. Reducing the loop area enclosed by the source signal and the return current reduces the inductance in the path. Reducing the inductance reduces the EMI pickup and reduces the high-frequency impedance at the input of the device.
- Watch for parasitic thermocouples in the layout. Dissimilar metals going from each analog input to the sensor can create a parasitic thermocouple that can add an offset to the measurement. Differential inputs must be matched for both the inputs going to the measurement source.
- Use C0G capacitors for the RC filters on the analog inputs.
- Fill void areas on signal layers with ground fill.
- When applying an external clock, be sure the clock is free of overshoot and glitches. A source-termination resistor placed at the clock buffer often helps reduce overshoot. Glitches present on the clock input can lead to noise within the conversion data.

9.4.2 Layout Example

Figure 9-12 shows a basic layout example for the ADS1x2S14:

- C1 is the required capacitor at the REFOUT pin to GND. Place C1 as close as possible to the REFOUT pin.
- C2 and C3 are the power supply decoupling capacitors. Place C2 and C3 as close as possible to the respective supply pins.
- Connect the GND pin through the decoupling capacitors to the ground plane.
- Differential antialiasing RC-filters are shown for the differential analog input pairs AIN0-AIN1, AIN2-AIN3 and AIN4-AIN5, respectively.
- Optional series resistors (R5 to R8) are shown for the SPI lines. The series resistors help to reduce overshoot and ringing on the digital lines by smoothing the signal edges.

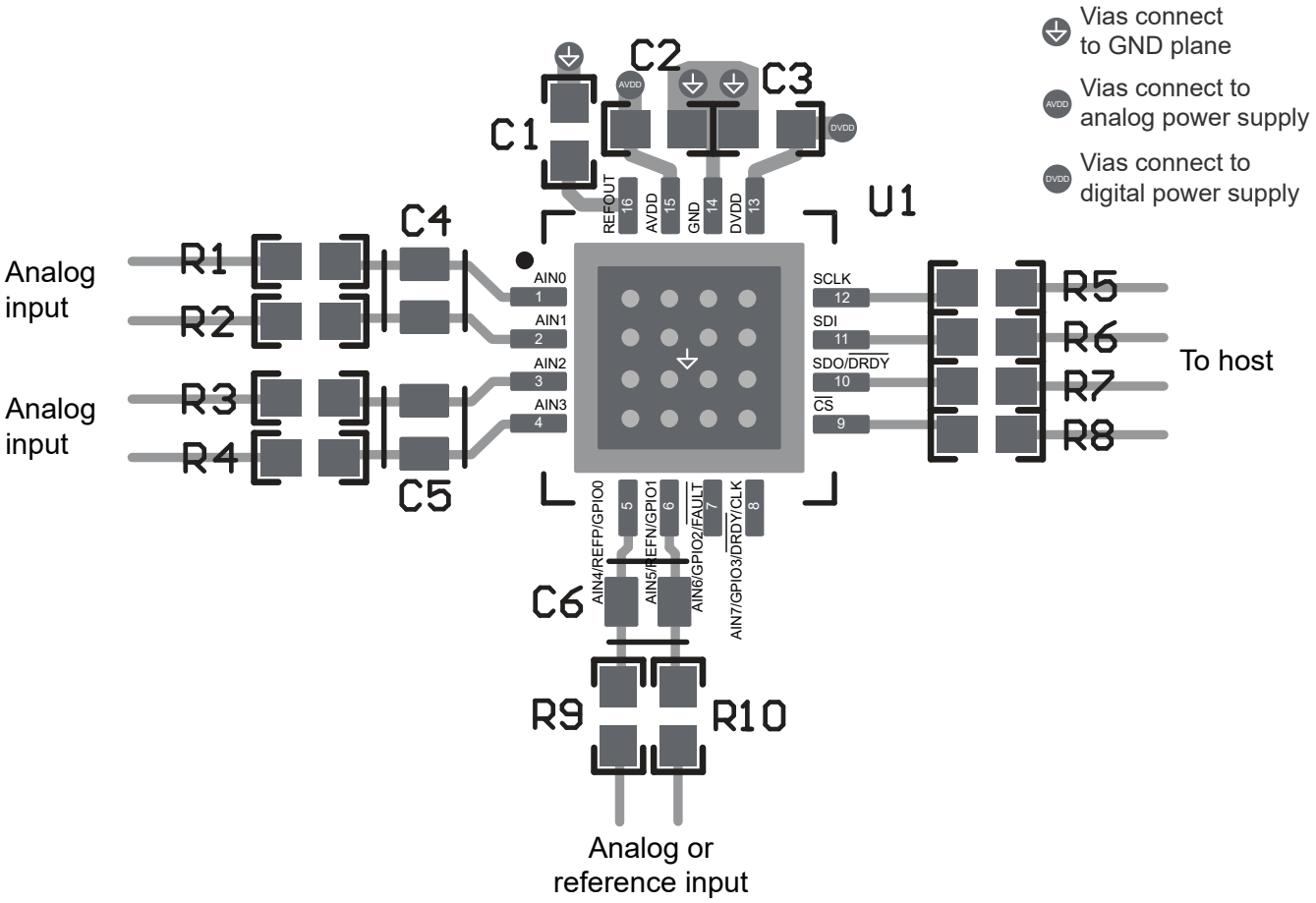


Figure 9-12. Layout Example

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

1. Texas Instruments, *A Basic Guide to RTD Measurements* application note
2. Texas Instruments, *RTD Wire-Break Detection Using Precision Delta-Sigma ADCs* application note
3. Texas Instruments, *A Basic Guide to Thermocouple Measurements* application note
4. Texas Instruments, *A Basic Guide to Bridge Measurements* application note
5. Texas Instruments, *Temperature-sensor (RTD, thermocouple, thermistor) firmware for precision ADCs* tool page

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

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All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2025	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS122S14IRTER	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-50 to 125	A22S14

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

GENERIC PACKAGE VIEW

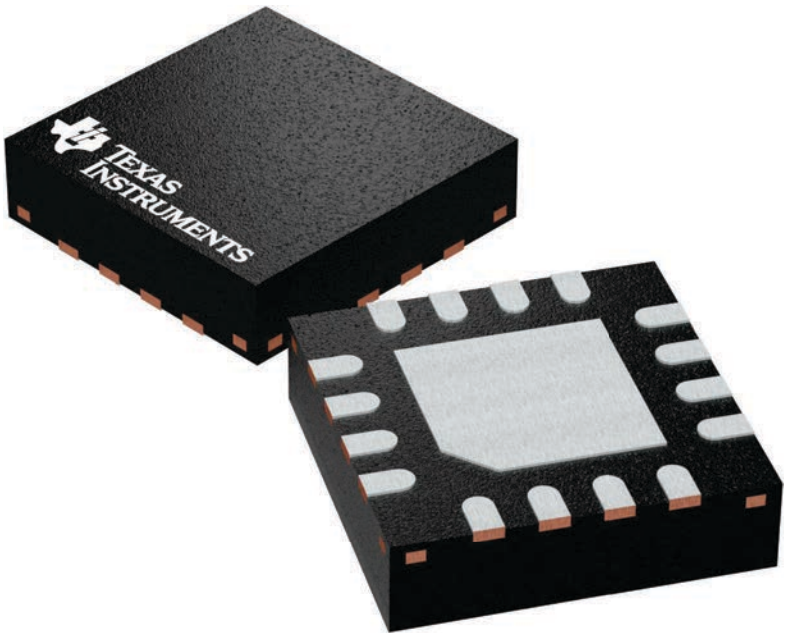
RTE 16

WQFN - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

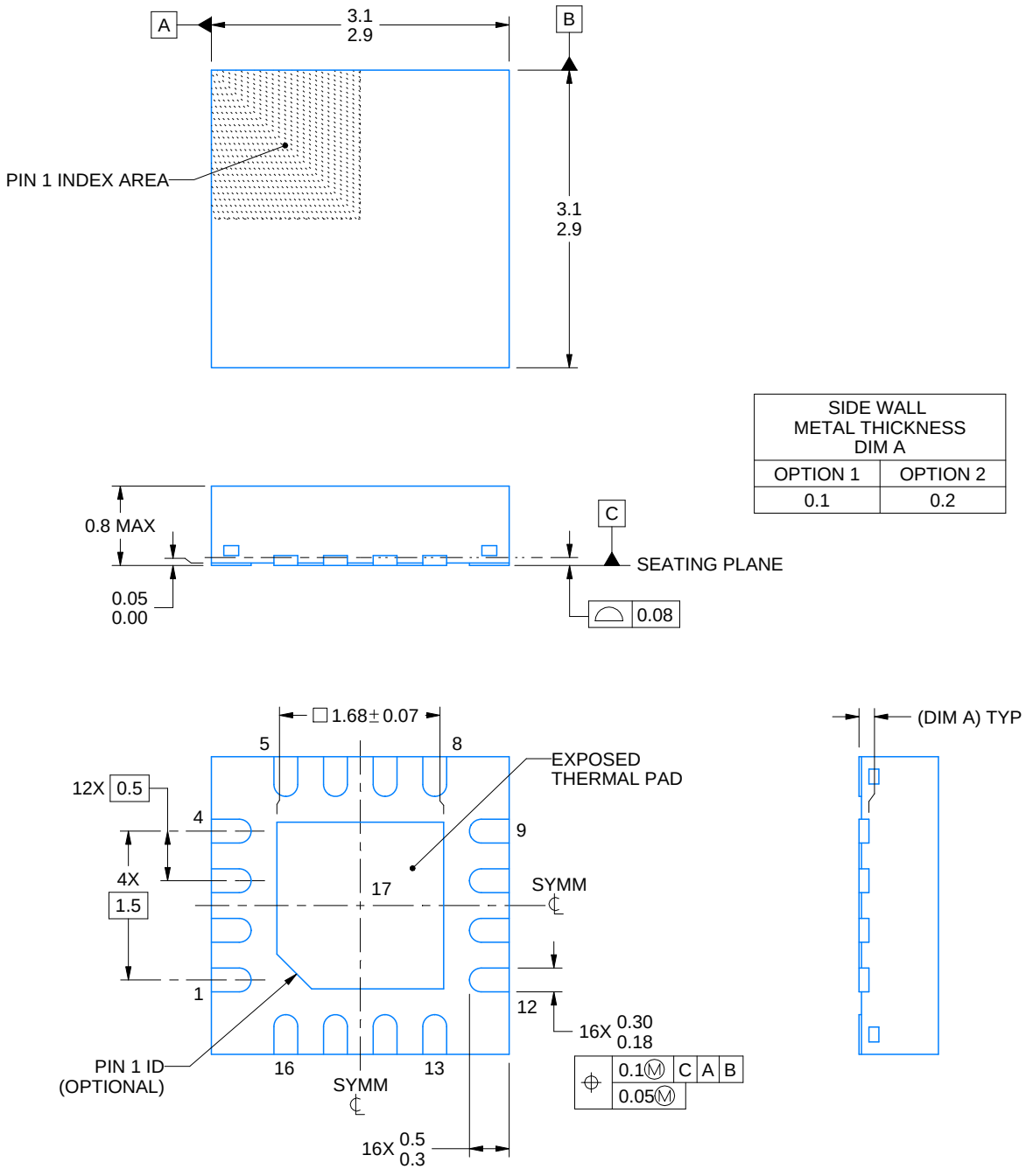


RTE0016C

PACKAGE OUTLINE

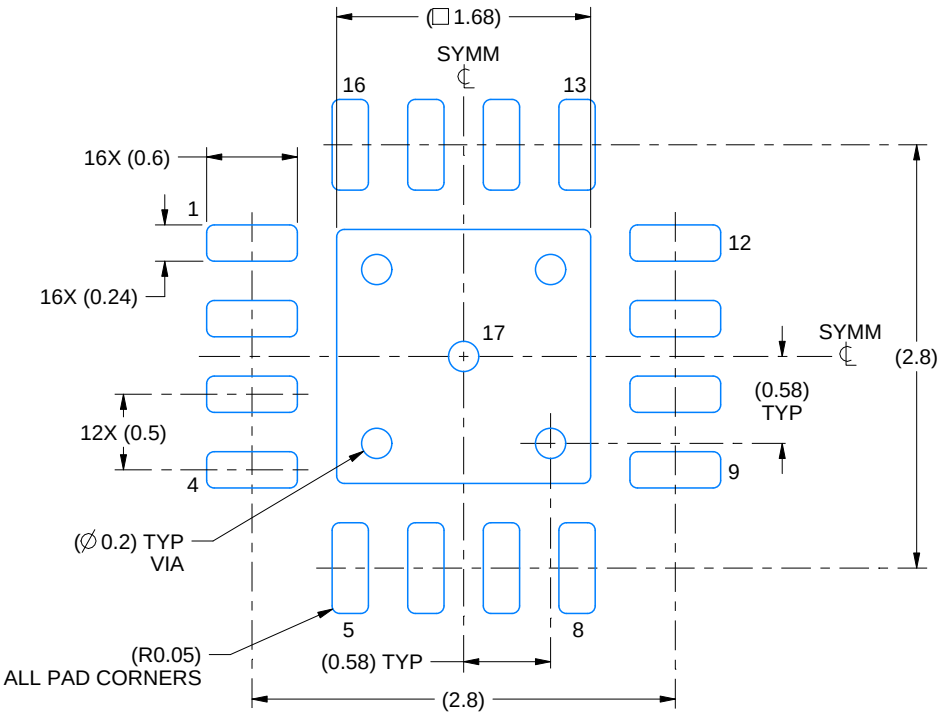
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

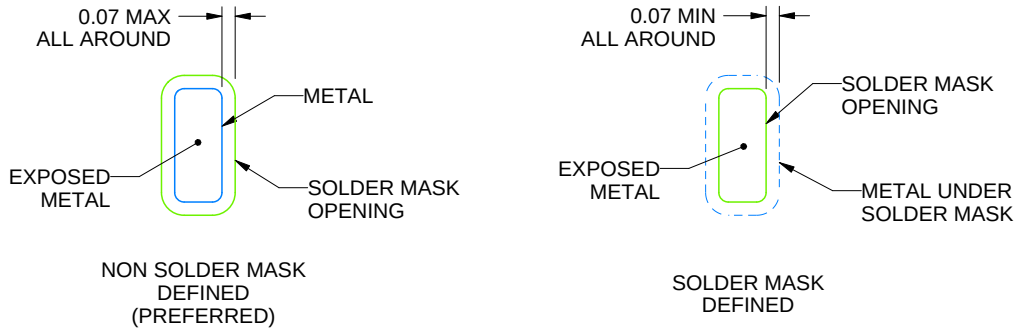


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

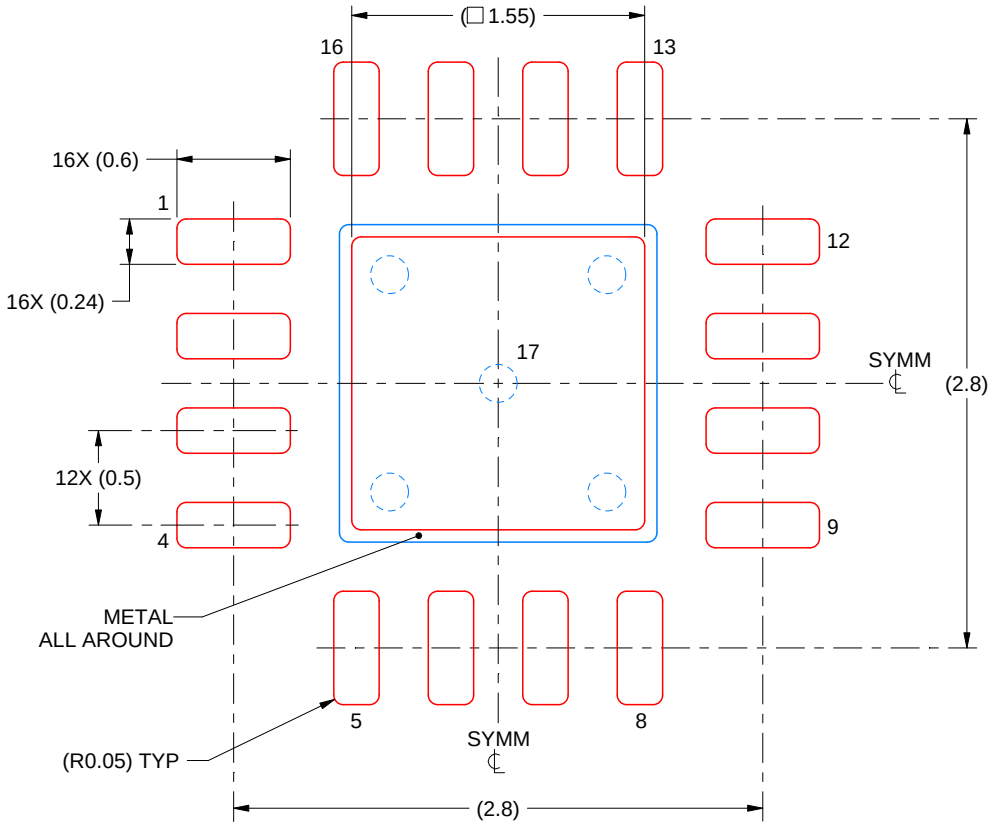


SOLDER MASK DETAILS

4219117/B 04/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219117/B 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Last updated 10/2025