

ADS58J63 Quad-Channel, 14-Bit, 500-MSPS Telecom Receiver Device

1 Features

- Quad Channel
- 14-Bit Resolution
- Maximum Clock Rate: 500 MSPS
- Input Bandwidth (3 dB): 900 MHz
- On-Chip Dither
- Analog Input Buffer with High-Impedance Input
- Output Options:
 - Rx: Decimate-by-2 and -4 Options with Low-Pass Filter
 - 200-MHz Complex Bandwidth or 100-MHz Real Bandwidth Support
 - DPD FB: Burst Mode with 14-Bit Output
- 1.9- V_{PP} Differential Full-Scale Input
- JESD204B Interface:
 - Subclass 1 Support
 - 1 Lane per ADC Up to 10 Gbps
 - Dedicated SYNC pin for pair of channels
- Support for Multi-Chip Synchronization
- 72-Pin VQFN Package (10 mm × 10 mm)
- Key Specifications:
 - Power Dissipation: 675 mW/ch
 - Spectral Performance (Un-decimated)
 - $f_{IN} = 190$ MHz IF at -1 dBFS:
 - SNR: 70.4 dBFS
 - NSD: -154.4 dBFS/Hz
 - SFDR: 86 dBc (HD2, HD3), 95 dBFS (non HD2, HD3)
 - $f_{IN} = 370$ MHz IF at -3 dBFS:
 - SNR: 68.5 dBFS
 - NSD: -152.5 dBFS/Hz
 - SFDR: 81 dBc (HD2, HD3), 86 dBFS (non HD2, HD3)

2 Applications

- Multi-Carrier GSM Cellular Infrastructure Base Stations
- Multi-Carrier Multi-Mode Cellular Infrastructure Base Stations
- Telecommunications Receiver
- Telecom DPD Observation Receiver

3 Description

The ADS58J63 is a low-power, wide-bandwidth, 14-bit, 500-MSPS, quad-channel, telecom receiver device. The ADS58J63 supports a JESD204B serial interface with data rates up to 10 Gbps with one lane per channel. The buffered analog input provides uniform input impedance across a wide frequency range and minimizes sample-and-hold glitch energy. The ADS58J63 provides excellent spurious-free dynamic range (SFDR) over a large input frequency range with very low power consumption. The digital signal processing block includes complex mixers followed by low-pass filters with decimate-by-2 and -4 options supporting up to 200-MHz receive bandwidth. The ADS58J63 also supports a 14-bit, 500-MSPS output in burst-mode making the device suitable for a DPD observation receiver.

The JESD204B interface reduces the number of interface lines, thus allowing high system integration density. An internal phase locked loop (PLL) multiplies the incoming analog-to-digital converter (ADC) sampling clock to derive the bit clock, which is used to serialize the 14-bit data from each channel.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|-----------|---------------------|
| ADS58J63 | VQFN (72) | 10.00 mm x 10.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Block Diagram

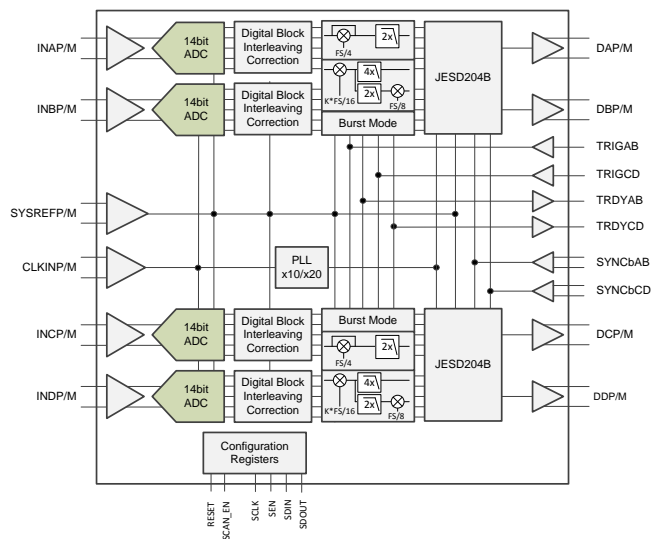


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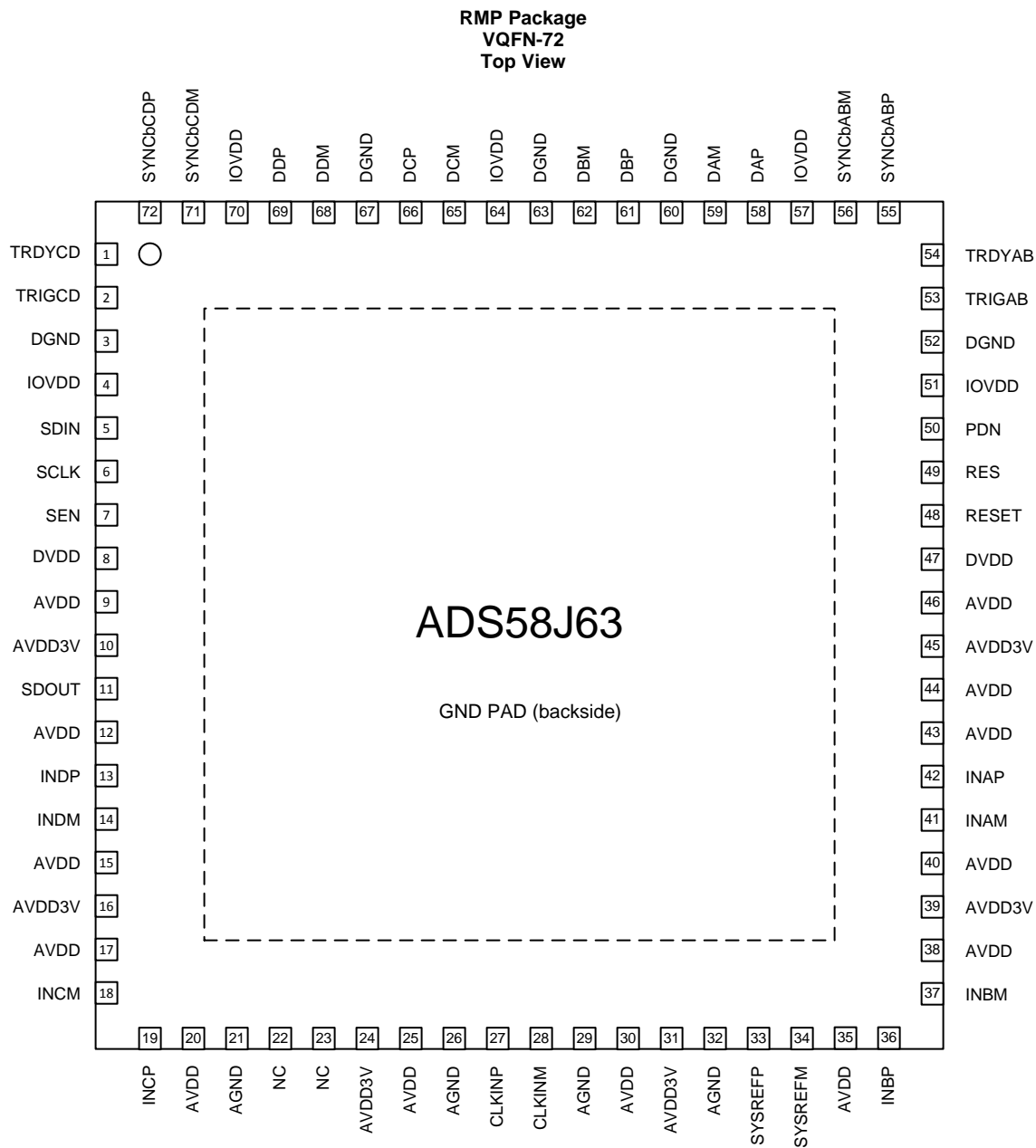
4 Revision History

Changes from Original (June 2015) to Revision A

Page

| | |
|--|---|
| • Changed From Product Preview To Production datasheet | 1 |
|--|---|

5 Pin Configuration and Functions



Pin Functions

| PIN | | I/O | DESCRIPTION |
|------------------------|---|-----|---|
| NAME | NUMBER | | |
| INPUT/REFERENCE | | | |
| INAP/M | 42, 41 | I | Differential analog input for channel A |
| INBP/M | 36, 37 | I | Differential analog input for channel B |
| INCP/M | 19, 18 | I | Differential analog input for channel C |
| INDP/M | 13, 14 | I | Differential analog input for channel D |
| CLOCK/SYNC | | | |
| CLKINP/M | 27, 28 | I | Differential clock input for ADC |
| SYSREFP/M | 33, 34 | I | External sync input |
| CONTROL/SERIAL | | | |
| RESET | 48 | I | Hardware reset. Active high. This pin has an internal 150-kΩ pull-down resistor. |
| SCLK | 6 | I | Serial interface clock input |
| SDIN | 5 | I | Serial interface data input. |
| SEN | 7 | I | Serial interface enable |
| SDOUT | 11 | O | Serial interface data output. |
| PDN | 50 | I/O | Power down. Can be configured via SPI register setting. |
| RES | 49 | – | Reserve Pin. Connect to GND |
| NC | 22, 23 | – | No connect |
| TRDYAB | 54 | O | Trigger ready output for burst mode for channel A,B. Can be configured via SPI to TRDY signal for all four channels in burst mode. Can be left open if not used. |
| TRIGAB | 53 | I | Manual burst mode trigger input channel A,B. Can be configured via SPI to manual trigger input signal for all four channels in burst mode. Can be connected to GND if not used. |
| TRDYCD | 1 | O | Trigger ready output for burst mode for channel C,D. Can be configured via SPI to TRDY signal for all four channels in burst mode. Can be left open if not used. |
| TRIGCD | 2 | I | Manual burst mode trigger input channel C,D. Can be configured via SPI to manual trigger input signal for all four channels in burst mode. Can be connected to GND if not used. |
| DATA INTERFACE | | | |
| DAP/M | 58, 59 | O | JESD204B Serial data output for channel A |
| DBP/M | 61, 62 | O | JESD204B Serial data output for channel B |
| DCP/M | 66, 65 | O | JESD204B Serial data output for channel C |
| DDP/M | 69, 68 | O | JESD204B Serial data output for channel D |
| SYNCbABP/M | 55, 56 | I | Synchronization input for JESD204B port channel A,B. Can be configured via SPI to SYNCb signal for all four channels. Needs external termination. |
| SYNCbCDP/M | 72, 71 | I | Synchronization input for JESD204B port channel C,D. Can be configured via SPI to SYNCb signal for all four channels. Needs external termination. |
| POWER SUPPLY | | | |
| AVDD3V | 10, 16, 24, 31, 39, 45 | I | Analog 3 V for analog buffer |
| AVDD | 9, 12, 15, 17, 20, 25, 30, 35, 38, 40, 43, 44, 46 | I | Analog 1.9-V power supply |
| DVDD | 8, 47 | I | Digital 1.9-V power supply |
| IOVDD | 4, 51, 57, 64, 70 | I | Digital 1.15-V power supply for the JESD204B transmitter |
| AGND | 21, 26, 29, 32 | I | Analog ground |
| DGND | 3, 52, 60, 63, 67 | I | Digital ground |

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|---------------------------------------|---|------|------------|------|
| Supply voltage range: | AVDD3V | -0.3 | 3.6 | V |
| | AVDD | -0.3 | 2.1 | V |
| | DVDD | -0.3 | 2.1 | V |
| | IOVDD | -0.2 | 1.4 | V |
| Voltage between AGND and DGND | | -0.3 | 0.3 | V |
| Voltage applied to input pins | INA/BP, INA/BM, INC/DP, INC/DM | -0.3 | 3 | V |
| | CLKINP, CLKINM | -0.3 | AVDD + 0.3 | V |
| | SYSREFP, SYSREFM, TRIGAB, TRIGCD | -0.3 | AVDD + 0.3 | V |
| | SCLK, SEN, SDIN, RESET, SPL_MODE, SYNCbABP/M, SYNCbCDP/M, PDN | -0.2 | 2 | V |
| Storage temperature, T _{stg} | | -65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

| | | | VALUE | UNIT |
|--------------------|-------------------------|---|-------|------|
| V _(ESD) | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±1 | kV |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|--|---|-----------------------|--------------------|-----|-----------------|
| Supply voltage range: | AVDD3V | 2.85 | 3 | 3.6 | V |
| | AVDD | 1.8 | 1.9 | 2 | V |
| | DVDD | 1.8 | 1.9 | 2 | V |
| | IOVDD | 1.1 | 1.15 | 1.2 | V |
| Analog inputs: | Differential input voltage range | 1.9 | | | V _{PP} |
| | Input common-mode voltage | VCM ± 0.025 | | | V |
| Clock inputs: | Input clock frequency, device clock frequency | | 250 | 500 | MHz |
| | Input clock amplitude differential (V _{CLKP} – V _{CLKM}) | Sine wave, ac-coupled | | 1.5 | V _{PP} |
| | | LVPECL, ac-coupled | | 1.6 | V _{PP} |
| | | LVDS, ac-coupled | | 0.7 | V _{PP} |
| Input device clock duty cycle, default after reset | | 45% | 50% | 55% | |
| Temperature: | Operating free-air, T _A | | -40 | 85 | °C |
| | Operating junction, T _J | | 105 ⁽²⁾ | | 125 |

(1) SYSREF needs to be applied for the device bring up.

(2) Prolonged use above this junction temperature can increase the device failure-in-time (FIT) rate.

6.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | ADS58J63 | UNIT |
|-------------------------------|--|--------------------------|------|
| | | RMP (VQFN ^P) | |
| | | 72 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 22.3 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 5.1 | |
| R _{θJB} | Junction-to-board thermal resistance | 2.4 | |
| ψ _{JT} | Junction-to-top characterization parameter | 0.1 | |
| ψ _{JB} | Junction-to-board characterization parameter | 2.3 | |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | 0.4 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](http://www.ti.com/lit/zip/spra953).

6.5 Electrical Characteristics

Typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = 85°C, ADC Sampling Frequency = 500 Msps, 50% clock duty cycle, AVDD3V = 3 V, AVDD/DVDD = 1.9 V, IOVDD = 1.15 V, –1 -dBFS differential input for IF ≤ 250 MHz, and –3-dBFS differential input for IF > 250 MHz, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------|---------------------------------------|-----------------------------|--|------------------|-------------------------|
| ADC Sampling Rate | | | | 500 | MSPS |
| Resolution | | 14 | | | Bits |
| POWER SUPPLY | | | | | |
| AVDD3V | | 2.85 | 3 | 3.6 | V |
| AVDD | | 1.8 | 1.9 | 2 | V |
| DVDD | | 1.8 | 1.9 | 2 | V |
| IOVDD | | 1.1 | 1.15 | 1.2 | V |
| I _{AVDD3V} | 3-V analog supply current | | 340 | | mA |
| I _{AVDD} | 1.9-V analog supply current | | 365 | | mA |
| I _{DVDD} | 1.9-V digital supply current | 2x Decimation (4 ch) | 370-MHz, full-scale input on all four channels | 190 | mA |
| | | | | 184 | mA |
| I _{IOVDD} | 1.15-V SERDES supply current | Burst Mode (4 ch) | | 533 | mA |
| | | | | P _{dis} | Total power dissipation |
| | | Burst Mode (4 ch) | | | |
| | Global power-down power dissipation | | | 250 | |
| ANALOG INPUTS | | | | | |
| | Differential input full-scale voltage | | 1.9 | | V _{PP} |
| | Input common-mode voltage | | V _{CM} ± 0.025 | | V |
| | Differential input resistance | at f _{IN} = 370MHz | 0.5 | | kΩ |
| | Differential input capacitance | at f _{IN} = 370MHz | 2.5 | | pF |
| | Analog input bandwidth (3 dB) | | 900 | | MHz |

Electrical Characteristics (continued)

Typical values are at $T_A = 25^\circ\text{C}$, full temperature range is from $T_{\text{MIN}} = -40^\circ\text{C}$ to $T_{\text{MAX}} = 85^\circ\text{C}$, ADC Sampling Frequency = 500 Msps, 50% clock duty cycle, $\text{AVDD}3\text{V} = 3\text{ V}$, $\text{AVDD}/\text{DVDD} = 1.9\text{ V}$, $\text{IOVDD} = 1.15\text{ V}$, -1 -dBFS differential input for $\text{IF} \leq 250\text{ MHz}$, and -3 -dBFS differential input for $\text{IF} > 250\text{ MHz}$, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|------------------------|--|--|-----|------|-----|------|------|
| ISOLATION | | | | | | | |
| Crosstalk (1) | Isolation between near channels (CHA and CHB are near to each other. CHC and CHD are near to each other) | $f_{\text{IN}} = 10\text{ MHz}$ | | 105 | | dBFS | |
| | | $f_{\text{IN}} = 100\text{ MHz}$ | | 104 | | dBFS | |
| | | $f_{\text{IN}} = 170\text{ MHz}$ | | 96 | | dBFS | |
| | | $f_{\text{IN}} = 270\text{ MHz}$ | | 97 | | dBFS | |
| | | $f_{\text{IN}} = 370\text{ MHz}$ | | 93 | | dBFS | |
| | | $f_{\text{IN}} = 470\text{ MHz}$ | | 85 | | dBFS | |
| | Isolation between far channels (for CHA and CHB, CHC and CHD are far channels) | $f_{\text{IN}} = 10\text{ MHz}$ | | | 110 | | dBFS |
| | | $f_{\text{IN}} = 100\text{ MHz}$ | | | 107 | | dBFS |
| | | $f_{\text{IN}} = 170\text{ MHz}$ | | | 96 | | dBFS |
| | | $f_{\text{IN}} = 270\text{ MHz}$ | | | 97 | | dBFS |
| | | $f_{\text{IN}} = 370\text{ MHz}$ | | | 95 | | dBFS |
| | | $f_{\text{IN}} = 470\text{ MHz}$ | | | 94 | | dBFS |
| CLOCK INPUT | | | | | | | |
| Internal clock biasing | | CLKINP and CLKINM pins are connected to internal biasing voltage through $400\ \Omega$ | | 1.15 | | V | |

(1) Crosstalk is measured with a -1 -dBFS input signal on aggressor channel and no input on the victim channel.

6.6 AC Performance

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | MIN | TYP | MAX | UNIT |
|----------------------------------|------------------------|----------------------------------|----------------------------------|-----------------------------------|-------|-------|--------------------------------------|-------|-----|-------------|
| | | | | 14-Bit Burst Mode (DDC Mode 8) | | | Decimate-by-2 Filter (DDC Mode 2) | | | |
| SNR | Signal-to-noise ratio | $f_{\text{IN}} = 10\text{ MHz}$ | | | 70.8 | | | 74.1 | | dBFS |
| | | $f_{\text{IN}} = 70\text{ MHz}$ | | | 70.5 | | | 74 | | |
| | | $f_{\text{IN}} = 190\text{ MHz}$ | $A_{\text{IN}} = -1\text{ dBFS}$ | | 69.5 | | | 73.2 | | |
| | | | $A_{\text{IN}} = -3\text{ dBFS}$ | 65.6 | 70.3 | | | 73.6 | | |
| | | $f_{\text{IN}} = 300\text{ MHz}$ | | | 69 | | | 72.6 | | |
| | | $f_{\text{IN}} = 350\text{ MHz}$ | | | 68.7 | | | 72 | | |
| | | $f_{\text{IN}} = 370\text{ MHz}$ | | 64.6 | 68.4 | | | | | |
| NSD | Noise spectral density | $f_{\text{IN}} = 10\text{ MHz}$ | | | 154.8 | | | 154.8 | | dBFS/ Hz |
| | | $f_{\text{IN}} = 70\text{ MHz}$ | | | 154.5 | | | 154.5 | | |
| | | $f_{\text{IN}} = 190\text{ MHz}$ | $A_{\text{IN}} = -1\text{ dBFS}$ | | 153.5 | | | 153.5 | | |
| | | | $A_{\text{IN}} = -3\text{ dBFS}$ | 149.5 | 154.3 | | | 154.3 | | |
| | | $f_{\text{IN}} = 300\text{ MHz}$ | | | 153 | | | 153.0 | | |
| | | $f_{\text{IN}} = 350\text{ MHz}$ | | | 152.7 | | | 152.7 | | |
| | | $f_{\text{IN}} = 370\text{ MHz}$ | | 148.5 | 152.4 | | | 152.4 | | |
| $f_{\text{IN}} = 470\text{ MHz}$ | | | 151.5 | | | 151.5 | | | | |

AC Performance (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | MIN | TYP | MAX | UNIT |
|--------------------|--|--------------------|--------------------|--------------------|------|------|-----|------|------|------|
| SINAD | Signal-to-noise and distortion ratio | $f_{IN} = 10$ MHz | | | 70.7 | | | 73.9 | | dBFS |
| | | $f_{IN} = 70$ MHz | | | 70.4 | | | 73.9 | | |
| | | $f_{IN} = 190$ MHz | $A_{IN} = -1$ dBFS | | 69.4 | | | 73.1 | | |
| | | | | $A_{IN} = -3$ dBFS | | 70.2 | | | 73.5 | |
| | | $f_{IN} = 300$ MHz | | | | 68.9 | | | 72.5 | |
| | | $f_{IN} = 350$ MHz | | | 68.6 | | | 71.7 | | |
| | | $f_{IN} = 370$ MHz | | | 68.2 | | | | | |
| $f_{IN} = 470$ MHz | | | 66.9 | | | 69.7 | | | | |
| SFDR | Spurious-free dynamic range | $f_{IN} = 10$ MHz | | | 89 | | | 88 | | dBc |
| | | $f_{IN} = 70$ MHz | | | 87 | | | 95 | | |
| | | $f_{IN} = 190$ MHz | $A_{IN} = -1$ dBFS | | 86 | | | 97 | | |
| | | | | $A_{IN} = -3$ dBFS | | 78 | 88 | | 96 | |
| | | $f_{IN} = 300$ MHz | | | | 82 | | | 94 | |
| | | $f_{IN} = 350$ MHz | | | 82 | | | 82 | | |
| | | $f_{IN} = 370$ MHz | | | 75 | 81 | | | | |
| $f_{IN} = 470$ MHz | | | 73 | | | 74 | | | | |
| HD2 | Second harmonic distortion | $f_{IN} = 10$ MHz | | | 89 | | | 91 | | dBc |
| | | $f_{IN} = 70$ MHz | | | 94 | | | 103 | | |
| | | $f_{IN} = 190$ MHz | $A_{IN} = -1$ dBFS | | 86 | | | 101 | | |
| | | | | $A_{IN} = -3$ dBFS | | 78 | 88 | | 101 | |
| | | $f_{IN} = 300$ MHz | | | | 82 | | | 97 | |
| | | $f_{IN} = 350$ MHz | | | 82 | | | 82 | | |
| | | $f_{IN} = 370$ MHz | | | 75 | 81 | | | | |
| $f_{IN} = 470$ MHz | | | 73 | | | 74 | | | | |
| HD3 | Third harmonic distortion | $f_{IN} = 10$ MHz | | | 93 | | | 88 | | dBc |
| | | $f_{IN} = 70$ MHz | | | 87 | | | 99 | | |
| | | $f_{IN} = 190$ MHz | $A_{IN} = -1$ dBFS | | 98 | | | 100 | | |
| | | | | $A_{IN} = -3$ dBFS | | 78 | 97 | | 98 | |
| | | $f_{IN} = 300$ MHz | | | | 95 | | | 100 | |
| | | $f_{IN} = 350$ MHz | | | 90 | | | 96 | | |
| | | $f_{IN} = 370$ MHz | | | 75 | 85 | | | | |
| $f_{IN} = 470$ MHz | | | 83 | | | 83 | | | | |
| Non HD2, HD3 | Spurious-free dynamic range (excluding HD2, HD3) | $f_{IN} = 10$ MHz | | | 94 | | | 98 | | dBc |
| | | $f_{IN} = 70$ MHz | | | 94 | | | 95 | | |
| | | $f_{IN} = 190$ MHz | $A_{IN} = -1$ dBFS | | 93 | | | 97 | | |
| | | | | $A_{IN} = -3$ dBFS | | 87 | 93 | | 96 | |
| | | $f_{IN} = 300$ MHz | | | | 92 | | | 94 | |
| | | $f_{IN} = 350$ MHz | | | 91 | | | 94 | | |
| | | $f_{IN} = 370$ MHz | | | 80 | 90 | | | | |
| $f_{IN} = 470$ MHz | | | 87 | | | 93 | | | | |

AC Performance (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | MIN | TYP | MAX | UNIT |
|----------------------------|---------------------------------------|--|----------------------------|-----|-----|-----|-----|-----|-----|------|
| THD | Total harmonic distortion | $f_{IN} = 10 \text{ MHz}$ | | | 88 | | | 86 | | dBc |
| | | $f_{IN} = 70 \text{ MHz}$ | | | 85 | | | 92 | | |
| | | $f_{IN} = 190 \text{ MHz}$ | $A_{IN} = -1 \text{ dBFS}$ | | 85 | | | 92 | | |
| | | | $A_{IN} = -3 \text{ dBFS}$ | | 86 | | | 91 | | |
| | | $f_{IN} = 300 \text{ MHz}$ | | | 81 | | | 89 | | |
| | | $f_{IN} = 350 \text{ MHz}$ | | | 79 | | | 82 | | |
| | | $f_{IN} = 370 \text{ MHz}$ | | | 78 | | | | | |
| $f_{IN} = 470 \text{ MHz}$ | | | 72 | | | 73 | | | | |
| IMD3 | Third-tone intermodulation distortion | $f_{IN} = 185 \text{ MHz}, f_{IN} = 190 \text{ MHz}$ | $A_{IN} = -7 \text{ dBFS}$ | | 89 | | | | | dBFS |
| | | $f_{IN} = 365 \text{ MHz}, f_{IN} = 370 \text{ MHz}$ | $A_{IN} = -7 \text{ dBFS}$ | | 82 | | | | | |
| | | $f_{IN} = 465 \text{ MHz}, f_{IN} = 470 \text{ MHz}$ | $A_{IN} = -7 \text{ dBFS}$ | | 77 | | | | | |

6.7 Digital Characteristics

Typical values are at $T_A = 25^\circ\text{C}$, full temperature range is from $T_{\text{MIN}} = -40^\circ\text{C}$ to $T_{\text{MAX}} = 85^\circ\text{C}$, ADC sampling rate = 500 MSPS, 50% clock duty cycle, $\text{AVDD3V} = 3\text{ V}$, $\text{AVDD} = \text{DVDD} = 1.9\text{ V}$, $\text{IOVDD} = 1.15\text{ V}$, and -1-dBFS differential input, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|--|-----------------------------------|--|---------------------|------|-----|-------------------------|
| DIGITAL INPUTS (RESET, SCLK, SEN, SDIN, PDN)⁽¹⁾ | | | | | | |
| V_{IH} | High-level input voltage | All digital inputs support 1.2-V and 1.8-V logic levels | 0.8 | | | V |
| V_{IL} | Low-level input voltage | All digital inputs support 1.2-V and 1.8-V logic levels | | | 0.4 | V |
| I_{IH} | High-level input current | SEN | | 0 | | μA |
| | | RESET, SCLK, SDIN, PDN | | 100 | | μA |
| I_{IL} | Low-level input current | SEN | | 50 | | μA |
| | | RESET, SCLK, SDIN, PDN | | 0 | | μA |
| DIGITAL INPUTS (SYSREFP, SYSREFM, SYNCbABM, SYNCbABP, SYNCbCDM, SYNCbCDP) | | | | | | |
| V_{D} | Differential Input Voltage | | 0.35 | 0.45 | 1.4 | V |
| $V_{\text{(CM_DIG)}}$ | Common-mode voltage for SYSREF | | | 1.3 | | V |
| DIGITAL OUTPUTS (SDOUT, PDN) | | | | | | |
| V_{OH} | High-level output voltage | | $\text{DVDD} - 0.1$ | DVDD | | V |
| V_{OL} | Low-level output voltage | | | | 0.1 | V |
| DIGITAL OUTPUTS (JESD204B Interface: DxP, DxM)⁽²⁾ | | | | | | |
| V_{OD} | Output differential voltage | With default swing setting. | | 700 | | mV_{PP} |
| V_{OC} | Output common-mode voltage | | | 450 | | mV |
| | Transmitter short-circuit current | Transmitter pins shorted to any voltage between -0.25 V and 1.45 V | -100 | | 100 | mA |
| Z_{OS} | Single-ended output impedance | | | 50 | | Ω |
| | Output capacitance | Output capacitance inside the device, from either output to ground | | 2 | | pF |

- (1) The RESET, SCLK, SDATA, and PDN pins have a 20-k Ω (typical) internal pulldown resistor to ground, and the SEN pin has a 20-k Ω (typical) pull up resistor to IOVDD.
 (2) 50- Ω , single-ended external termination to IOVDD.

6.8 Timing Characteristics

Typical values are at $T_A = 25^\circ\text{C}$, full temperature range is from $T_{\text{MIN}} = -40^\circ\text{C}$ to $T_{\text{MAX}} = 85^\circ\text{C}$, ADC sampling rate = 500 MSPS, 50% clock duty cycle, AVDD3V = 3 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, and -1-dBFS differential input, unless otherwise noted.

| | | MIN | TYP | MAX | UNITS |
|--|---|------|-----------|-----|--------------------|
| SAMPLE TIMING CHARACTERISTICS | | | | | |
| Aperture delay | | 0.75 | | 1.6 | ns |
| Aperture delay matching between two channels on the same device | | | ± 70 | | ps |
| Aperture delay matching between two devices at the same temperature and supply voltage | | | ± 270 | | ps |
| Aperture jitter | | | 135 | | f_s rms |
| Wake-up time to valid data after coming out of global power-down | | | 150 | | μs |
| Data Latency ⁽¹⁾ | ADC sample to digital output | | 77 | | Input Clock Cycles |
| OVR Latency | ADC sample to OVR bit | | 44 | | Input Clock Cycles |
| t_{PDI} | Clock propagation delay Input clock rising edge cross-over to output clock rising edge cross-over | | 4 | | ns |
| $t_{\text{SU_SYSREF}}$ | Setup time for SYSREF, referenced to input clock rising edge | 300 | | 900 | ps |
| $t_{\text{H_SYSREF}}$ | Hold time for SYSREF, referenced to input clock rising edge | 100 | | | ps |
| JESD OUTPUT INTERFACE TIMING CHARACTERISTICS | | | | | |
| Unit interval | | 100 | | 400 | ps |
| Serial output data rate | | 2.5 | | 10 | Gbps |
| Total jitter for BER of 1E-15 and lane rate = 10 Gbps | | | 26 | | ps |
| Random jitter for BER of 1E-15 and lane rate = 10 Gbps | | | 0.75 | | ps rms |
| Deterministic jitter for BER of 1E-15 and lane rate = 10 Gbps | | | 12 | | ps, pk-pk |
| $t_{\text{R}}, t_{\text{F}}$ | Data rise time, data fall time: rise and fall times measured from 20% to 80%, differential output waveform, 2.5 Gbps \leq bit rate \leq 10 Gbps | | 35 | | ps |

(1) Overall ADC Latency = Data Latency + t_{PDI}

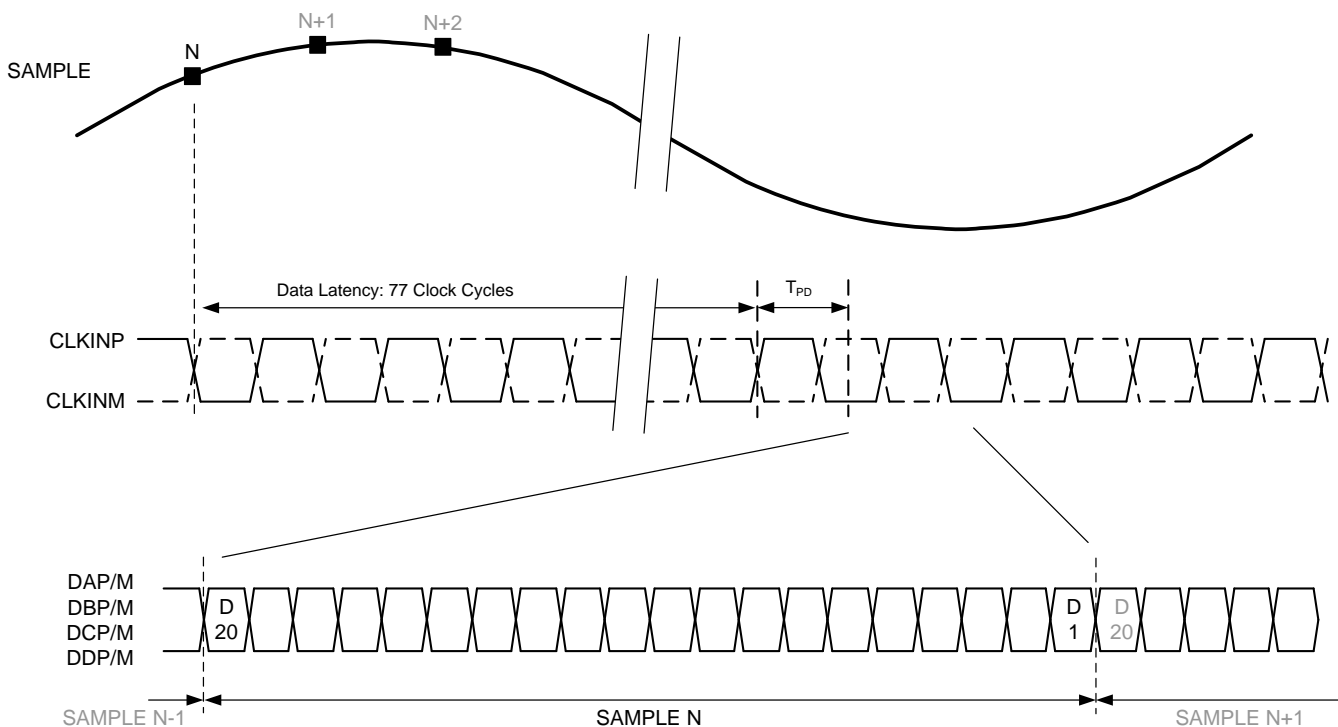


Figure 1. Latency Timing Diagram

6.9 Typical Characteristics: 14-Bit Burst Mode

Typical values are at $T_A = 25^\circ\text{C}$, full temperature range is from $T_{\text{MIN}} = -40^\circ\text{C}$ to $T_{\text{MAX}} = 85^\circ\text{C}$, ADC Sampling Frequency = 500 Msps, 14-bit Resolution, No Decimation Filter, 50% clock duty cycle, $\text{AVDD3V} = 3\text{ V}$, $\text{AVDD} = \text{DVDD} = 1.9\text{ V}$, $\text{IOVDD} = 1.15\text{ V}$, -1 dBFS differential input for $\text{IF} \leq 250\text{ MHz}$, and -3 dBFS differential input for $\text{IF} > 250\text{ MHz}$, unless otherwise noted.

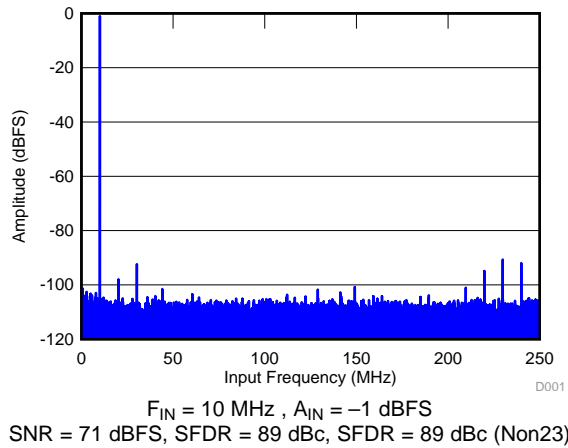


Figure 2. FFT for 10-MHz Input Signal

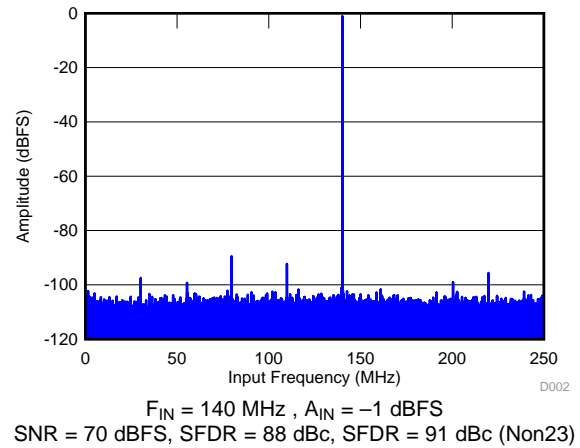


Figure 3. FFT for 140-MHz Input Signal

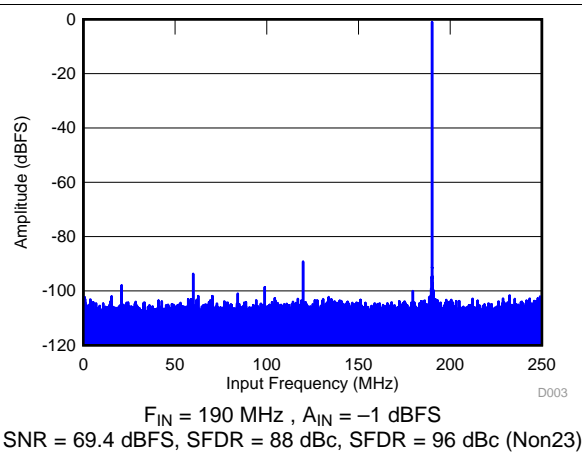


Figure 4. FFT for 190-MHz Input Signal

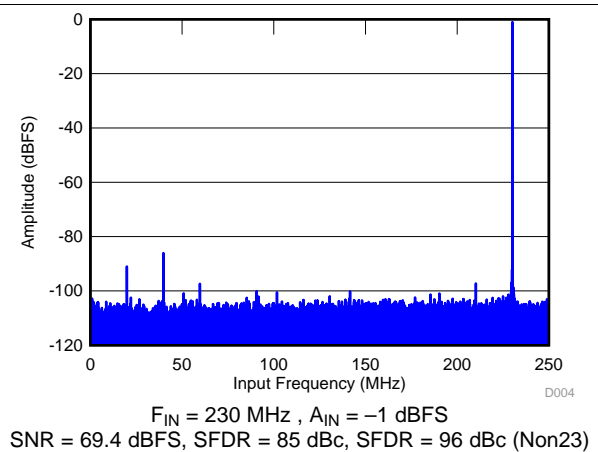


Figure 5. FFT for 230-MHz Input Signal

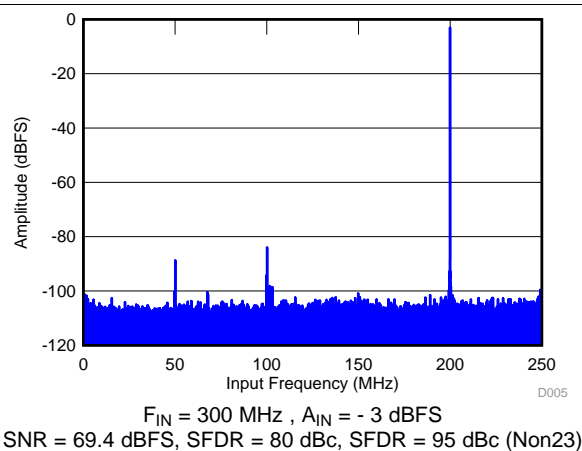


Figure 6. FFT for 300-MHz Input Signal

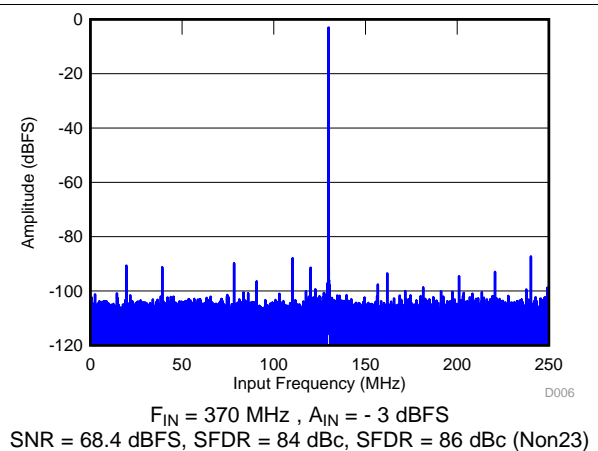
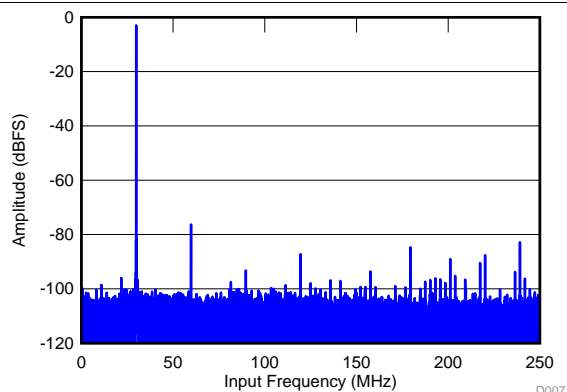


Figure 7. FFT for 370-MHz Input Signal

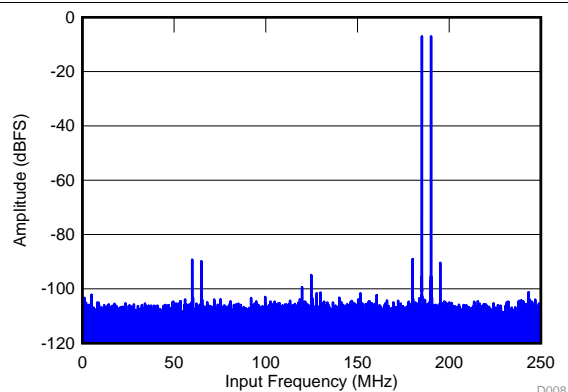
Typical Characteristics: 14-Bit Burst Mode (continued)

Typical values are at $T_A = 25^\circ\text{C}$, full temperature range is from $T_{\text{MIN}} = -40^\circ\text{C}$ to $T_{\text{MAX}} = 85^\circ\text{C}$, ADC Sampling Frequency = 500 Msps, 14-bit Resolution, No Decimation Filter, 50% clock duty cycle, AVDD3V = 3 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, -1-dBFS differential input for $IF \leq 250$ MHz, and -3-dBFS differential input for $IF > 250$ MHz, unless otherwise noted.



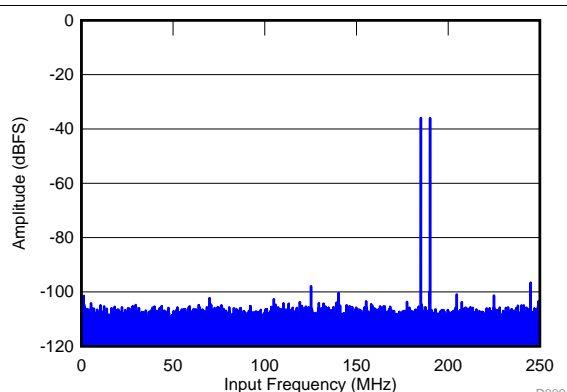
$F_{\text{IN}} = 470$ MHz, $A_{\text{IN}} = -3$ dBFS
SNR = 67.4 dBFS, SFDR = 73 dBc, SFDR = 80 dBc (Non23)

Figure 8. FFT for 470-MHz Input Signal



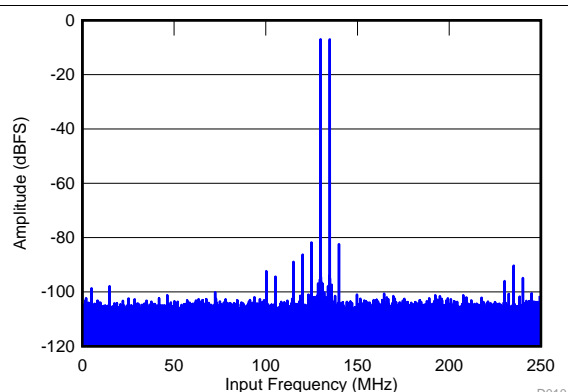
$F_{\text{IN1}} = 185$ MHz, $F_{\text{IN2}} = 190$ MHz, IMD = 89 dBFS
Each tone at -7 dBFS

Figure 9. FFT for Two-Tone Input Signal



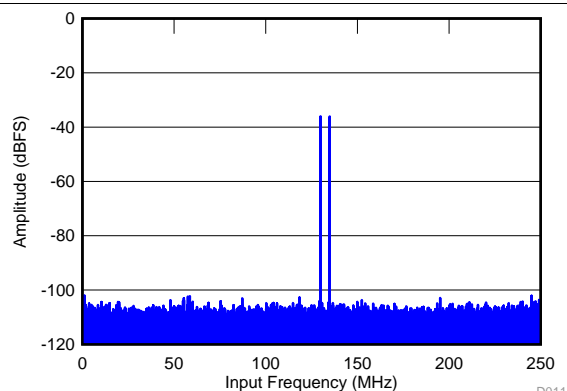
$F_{\text{IN1}} = 185$ MHz, $F_{\text{IN2}} = 190$ MHz, IMD = 103 dBFS
Each tone at -36 dBFS

Figure 10. FFT for Two-Tone Input Signal



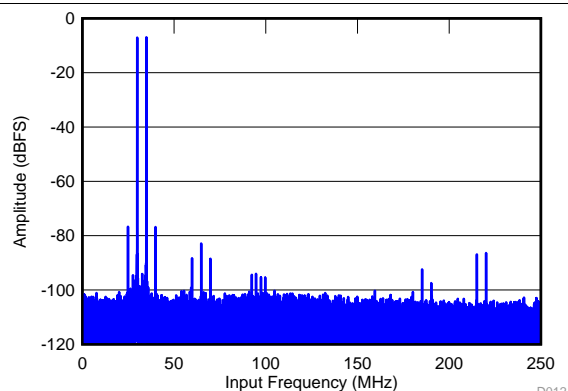
$F_{\text{IN1}} = 370$ MHz, $F_{\text{IN2}} = 365$ MHz, IMD = 81.7 dBFS
Each tone at -7 dBFS

Figure 11. FFT for Two-Tone Input Signal



$F_{\text{IN1}} = 370$ MHz, $F_{\text{IN2}} = 365$ MHz, IMD = 102 dBFS
Each tone at -36 dBFS

Figure 12. FFT for Two-Tone Input Signal



$F_{\text{IN1}} = 470$ MHz, $F_{\text{IN2}} = 465$ MHz, IMD = 76.7 dBFS
Each tone at -7 dBFS

Figure 13. FFT for Two-Tone Input Signal

Typical Characteristics: 14-Bit Burst Mode (continued)

Typical values are at $T_A = 25^\circ\text{C}$, full temperature range is from $T_{\text{MIN}} = -40^\circ\text{C}$ to $T_{\text{MAX}} = 85^\circ\text{C}$, ADC Sampling Frequency = 500 Msps, 14-bit Resolution, No Decimation Filter, 50% clock duty cycle, $\text{AVDD3V} = 3\text{ V}$, $\text{AVDD} = \text{DVDD} = 1.9\text{ V}$, $\text{IOVDD} = 1.15\text{ V}$, -1-dBFS differential input for $\text{IF} \leq 250\text{ MHz}$, and -3-dBFS differential input for $\text{IF} > 250\text{ MHz}$, unless otherwise noted.

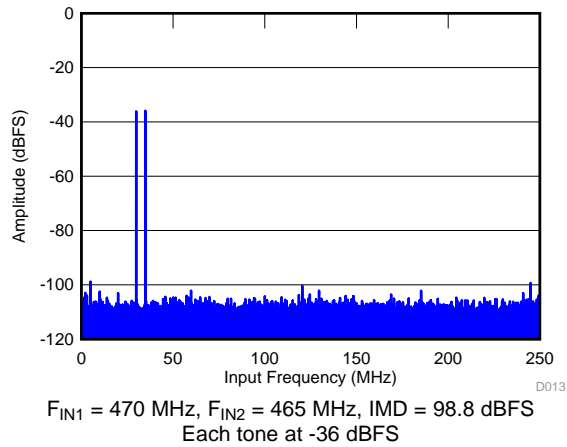


Figure 14. FFT for Two-Tone Input Signal

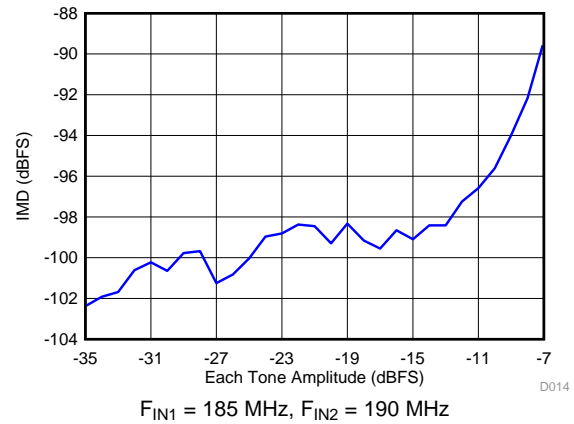


Figure 15. Intermodulation Distortion Vs Input Amplitude

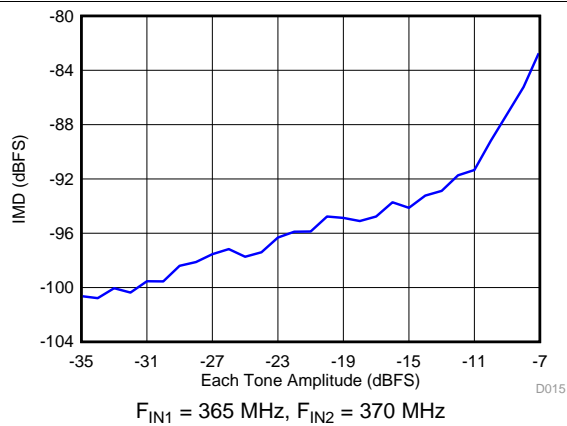


Figure 16. Intermodulation Distortion Vs Input Amplitude

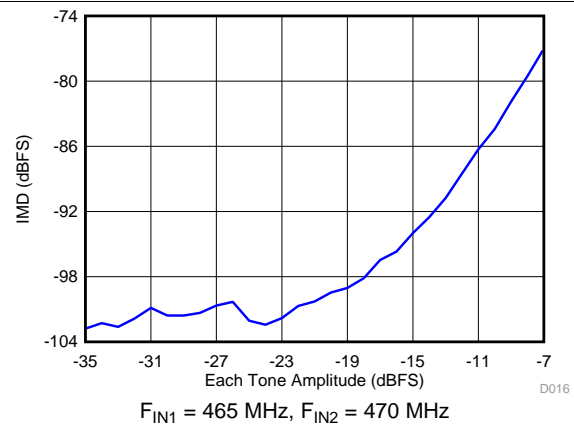


Figure 17. Intermodulation Distortion Vs Input Amplitude

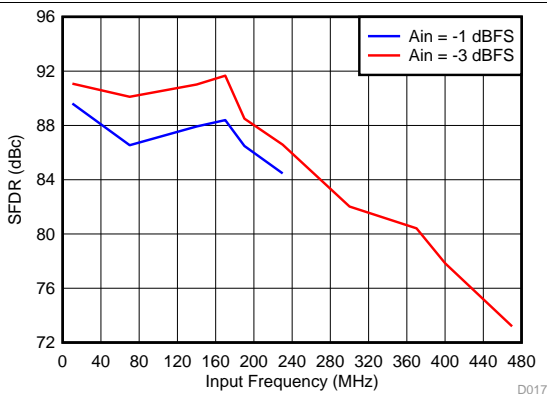


Figure 18. Spurious-Free Dynamic Range vs Input Frequency

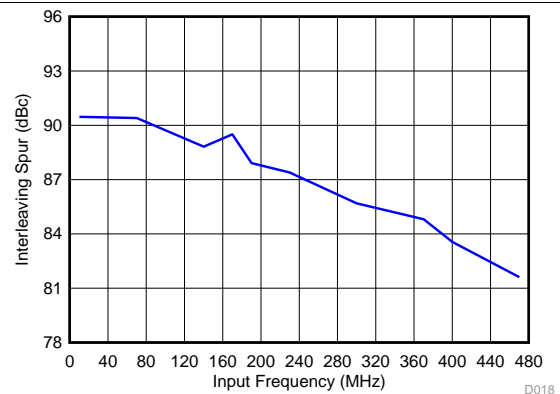


Figure 19. IL Spur Vs Input Frequency

Typical Characteristics: 14-Bit Burst Mode (continued)

Typical values are at $T_A = 25^\circ\text{C}$, full temperature range is from $T_{\text{MIN}} = -40^\circ\text{C}$ to $T_{\text{MAX}} = 85^\circ\text{C}$, ADC Sampling Frequency = 500 Msps, 14-bit Resolution, No Decimation Filter, 50% clock duty cycle, AVDD3V = 3 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, -1-dBFS differential input for $f_{\text{IN}} \leq 250$ MHz, and -3-dBFS differential input for $f_{\text{IN}} > 250$ MHz, unless otherwise noted.

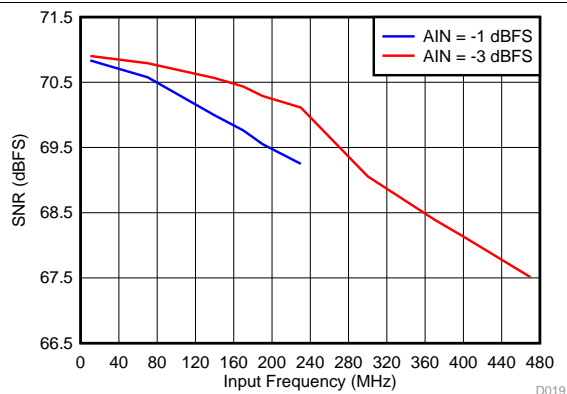


Figure 20. Signal-to-Noise Ratio vs Input Frequency

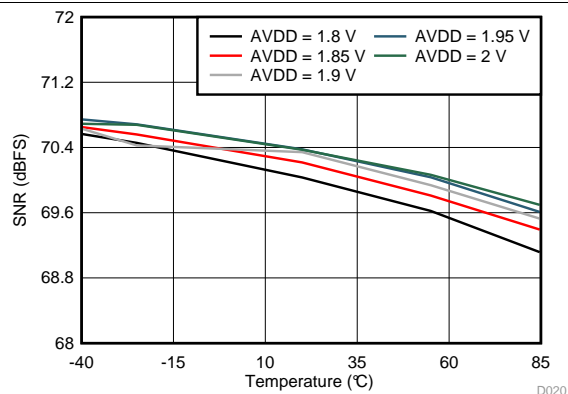


Figure 21. Signal-to-Noise Ratio vs AVDD Supply and Temperature

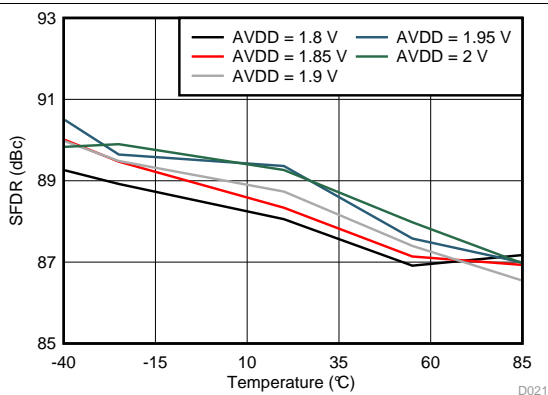


Figure 22. Spurious-Free Dynamic Range vs AVDD Supply and Temperature

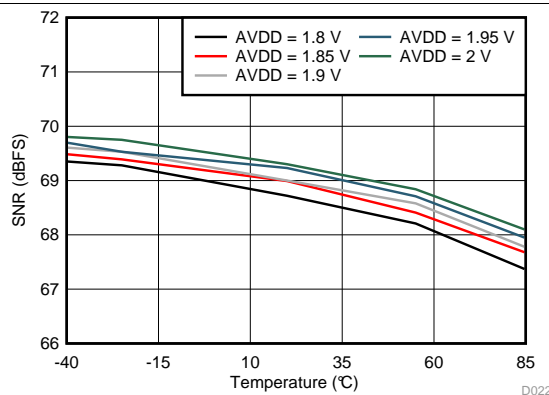


Figure 23. Signal-to-Noise Ratio vs AVDD Supply and Temperature

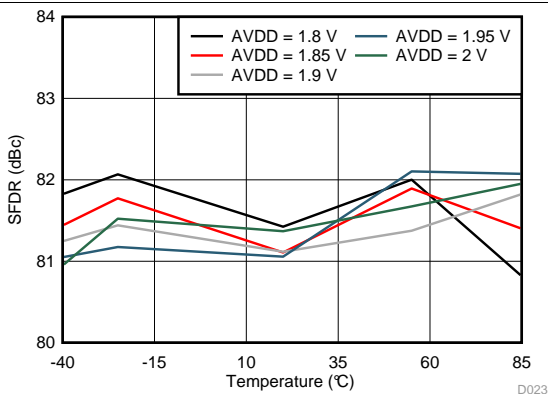


Figure 24. Spurious-Free Dynamic Range vs AVDD Supply and Temperature

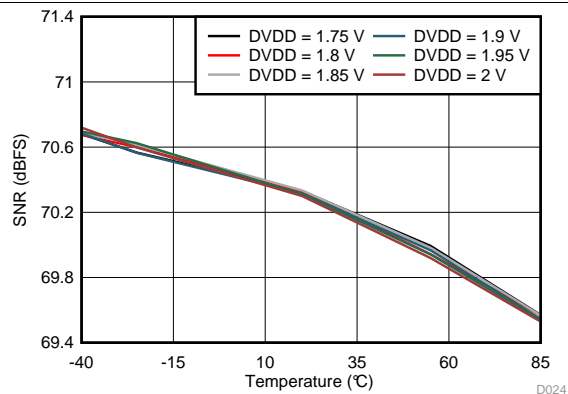


Figure 25. Signal-to-Noise Ratio vs DVDD Supply and Temperature

Typical Characteristics: 14-Bit Burst Mode (continued)

Typical values are at $T_A = 25^\circ\text{C}$, full temperature range is from $T_{\text{MIN}} = -40^\circ\text{C}$ to $T_{\text{MAX}} = 85^\circ\text{C}$, ADC Sampling Frequency = 500 Msps, 14-bit Resolution, No Decimation Filter, 50% clock duty cycle, AVDD3V = 3 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, -1-dBFS differential input for $f_{\text{IN}} \leq 250$ MHz, and -3-dBFS differential input for $f_{\text{IN}} > 250$ MHz, unless otherwise noted.

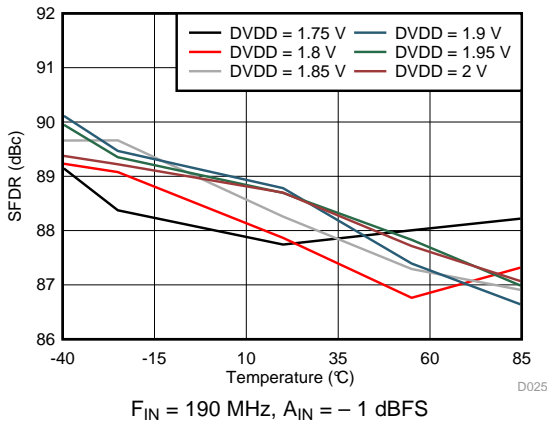


Figure 26. Spurious-Free Dynamic Range vs DVDD Supply and Temperature

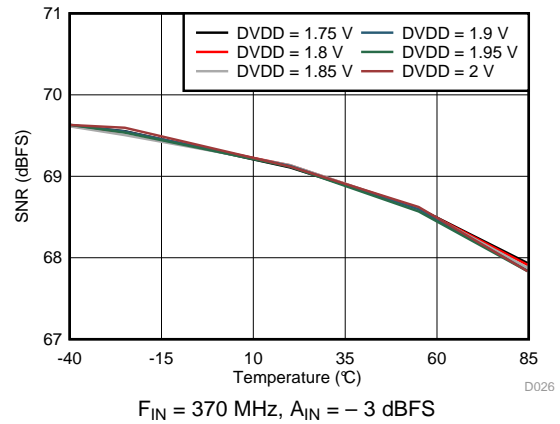


Figure 27. Signal-to-Noise Ratio vs DVDD Supply and Temperature

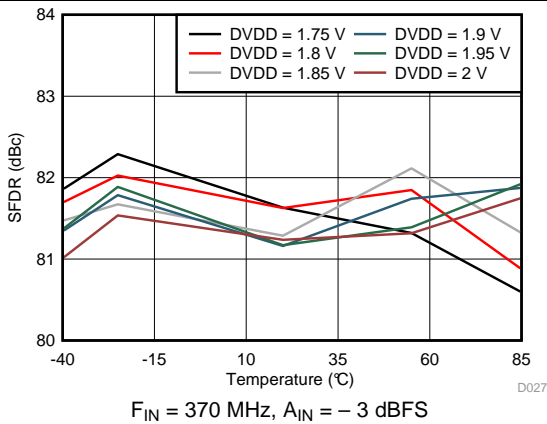


Figure 28. Spurious-Free Dynamic Range vs DVDD Supply and Temperature

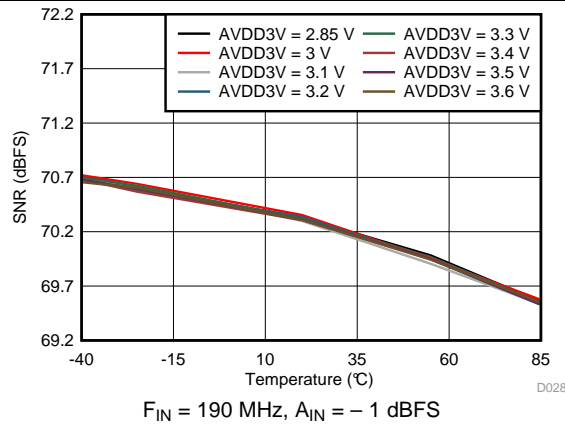


Figure 29. Signal-to-Noise Ratio vs AVDD3V Supply and Temperature

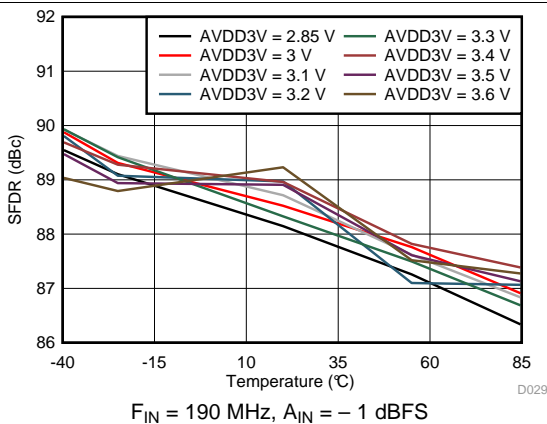


Figure 30. Spurious-Free Dynamic Range vs AVDD3V Supply and Temperature

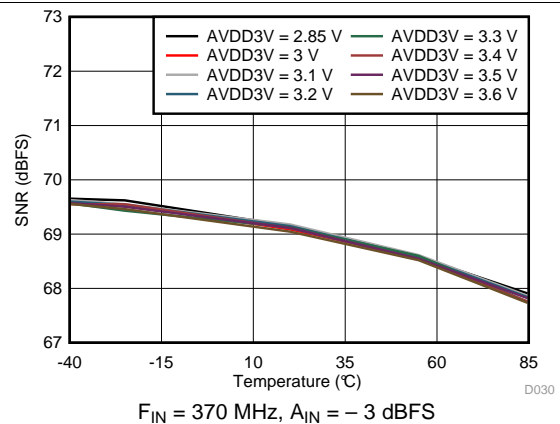
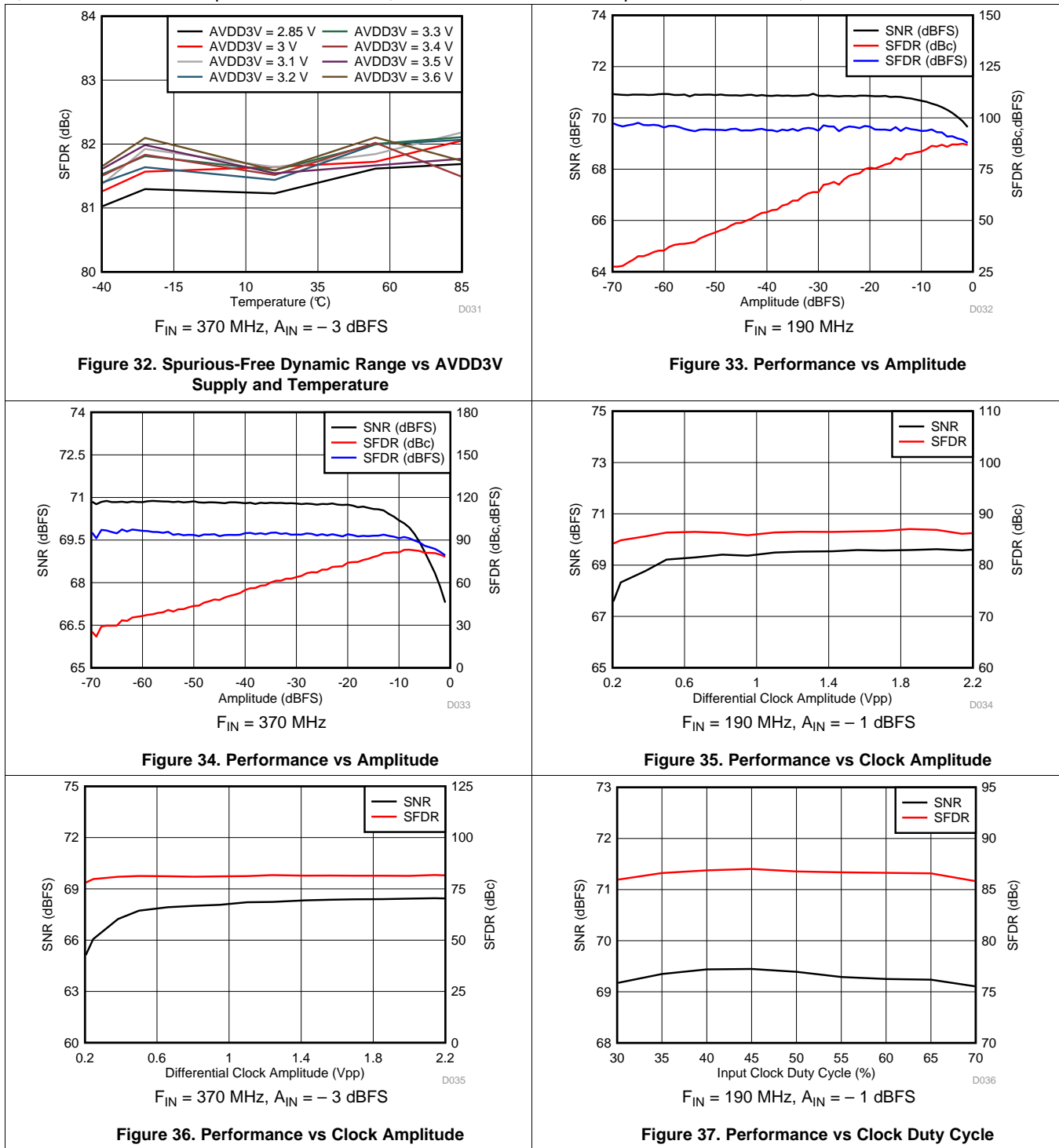


Figure 31. Signal-to-Noise Ratio vs AVDD3V Supply and Temperature

Typical Characteristics: 14-Bit Burst Mode (continued)

Typical values are at $T_A = 25^\circ\text{C}$, full temperature range is from $T_{\text{MIN}} = -40^\circ\text{C}$ to $T_{\text{MAX}} = 85^\circ\text{C}$, ADC Sampling Frequency = 500 Msps, 14-bit Resolution, No Decimation Filter, 50% clock duty cycle, AVDD3V = 3 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, -1-dBFS differential input for $f_{\text{IN}} \leq 250 \text{ MHz}$, and -3-dBFS differential input for $f_{\text{IN}} > 250 \text{ MHz}$, unless otherwise noted.



Typical Characteristics: 14-Bit Burst Mode (continued)

Typical values are at $T_A = 25^\circ\text{C}$, full temperature range is from $T_{\text{MIN}} = -40^\circ\text{C}$ to $T_{\text{MAX}} = 85^\circ\text{C}$, ADC Sampling Frequency = 500 Msps, 14-bit Resolution, No Decimation Filter, 50% clock duty cycle, AVDD3V = 3 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, -1-dBFS differential input for $f_{\text{IN}} \leq 250$ MHz, and -3-dBFS differential input for $f_{\text{IN}} > 250$ MHz, unless otherwise noted.

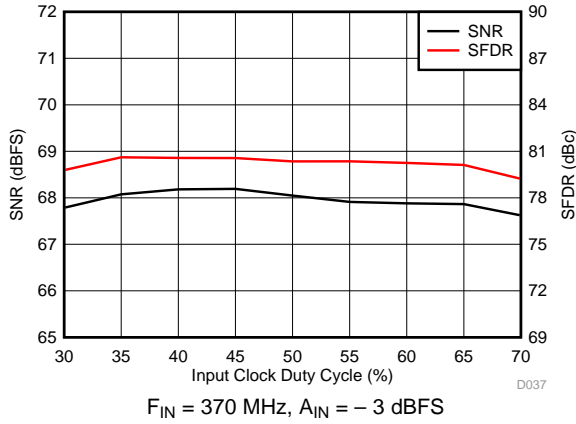


Figure 38. Performance vs Clock Duty Cycle

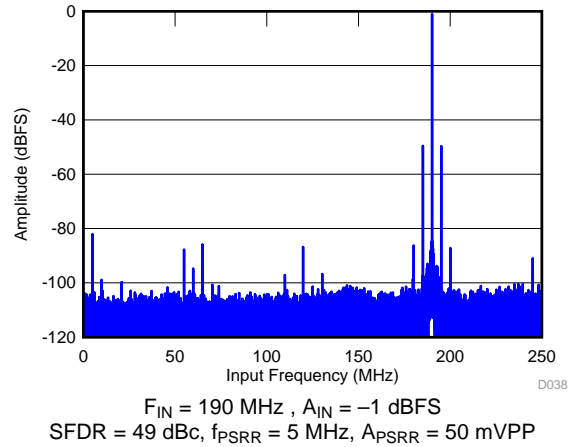


Figure 39. Power-Supply Rejection Ratio FFT for test signal on AVDD Supply

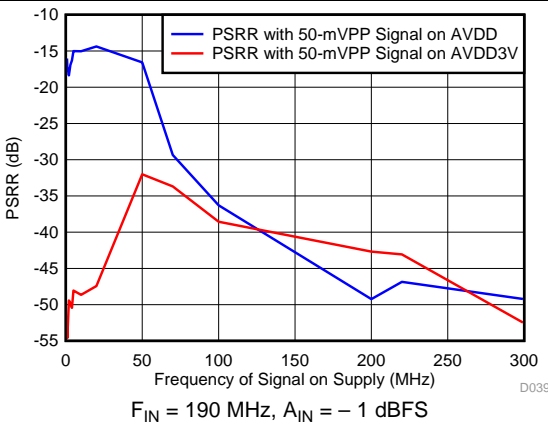


Figure 40. Power-Supply Rejection Ratio vs Supplies

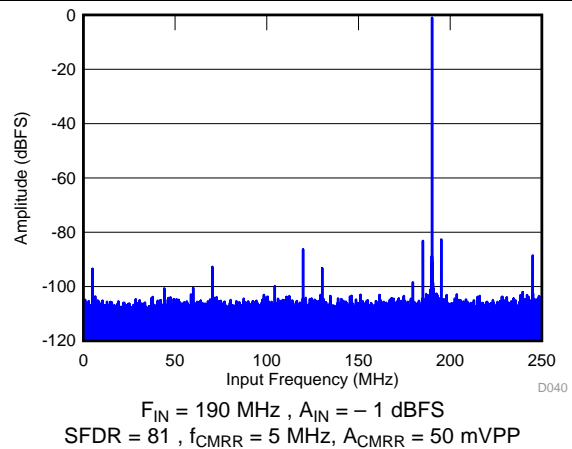


Figure 41. Common-Mode Rejection Ratio FFT

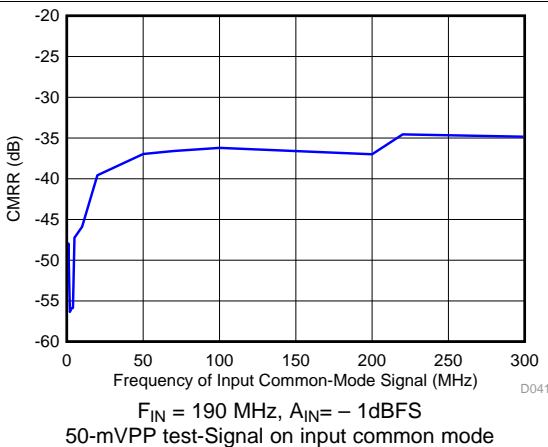


Figure 42. Common-Mode Rejection Ratio

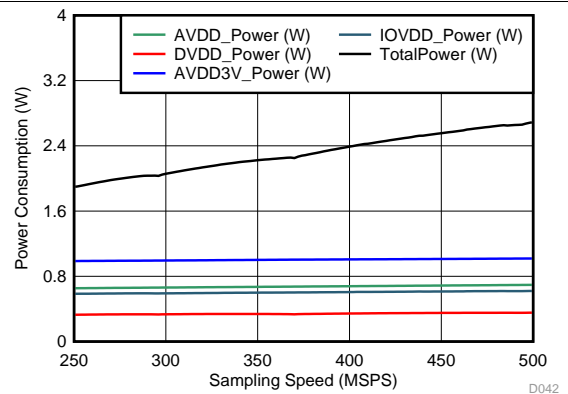
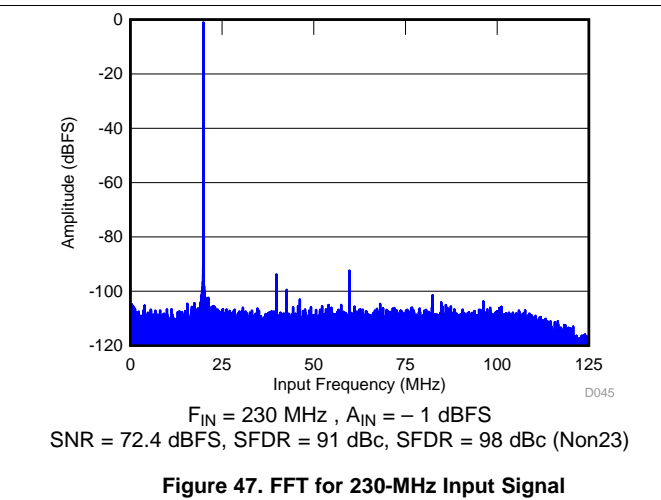
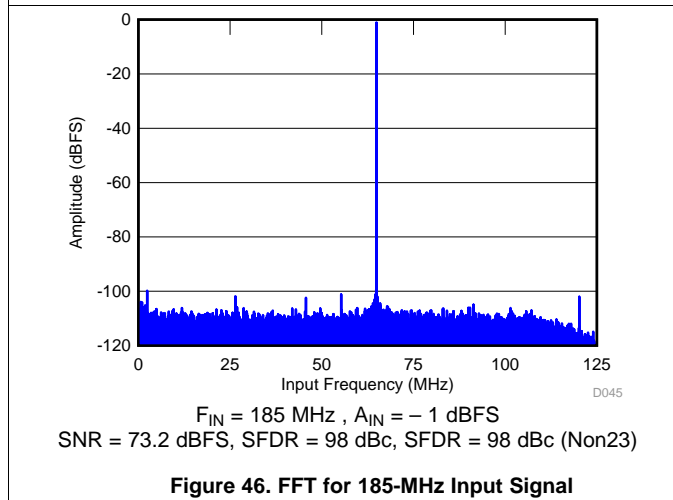
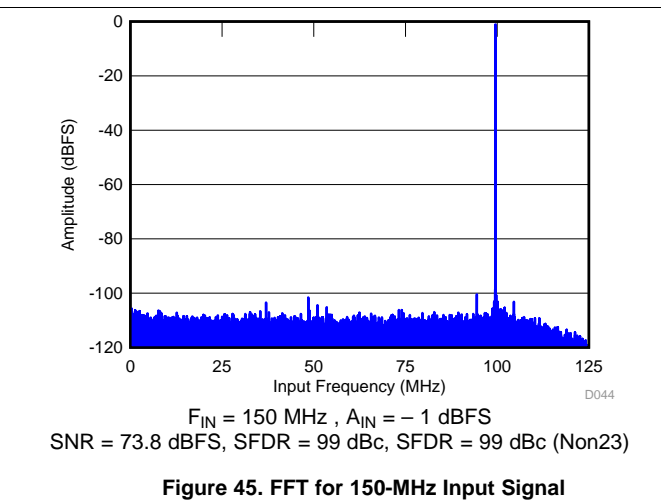
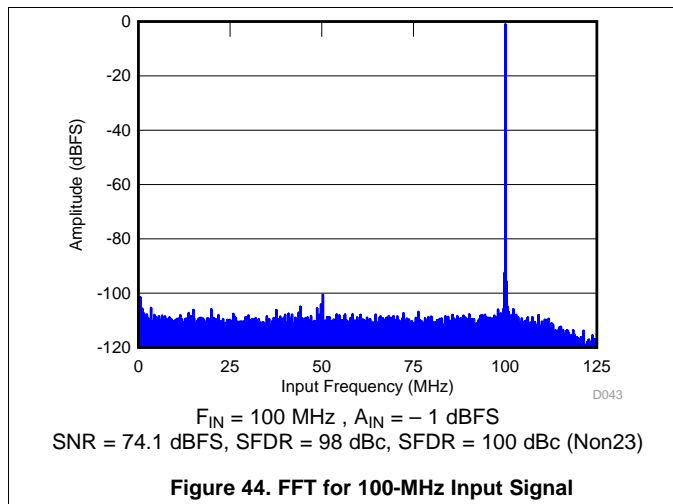


Figure 43. Power vs Chip Clock

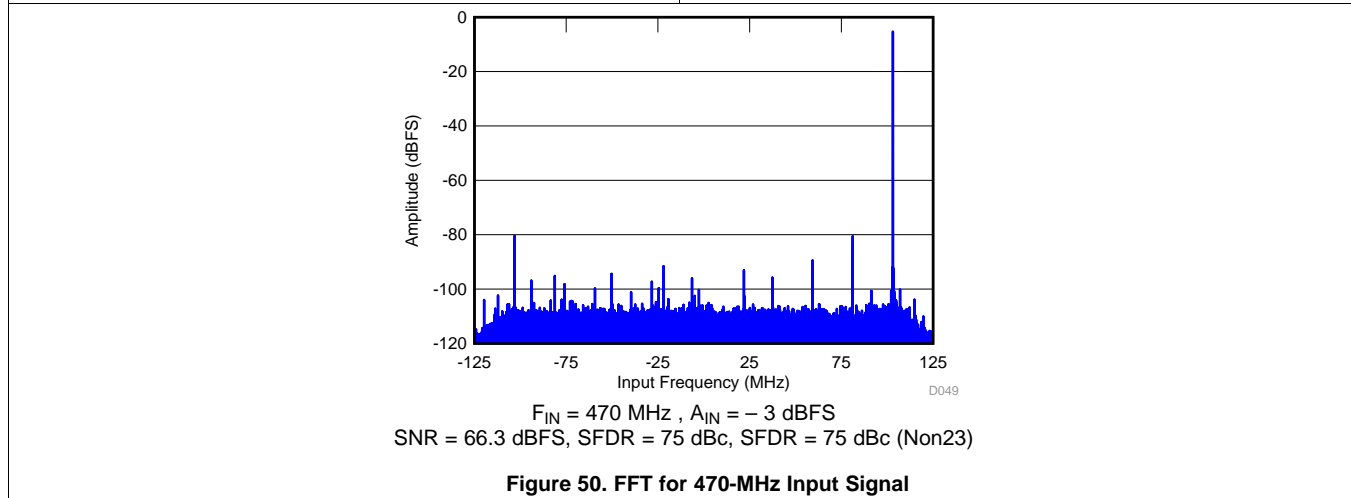
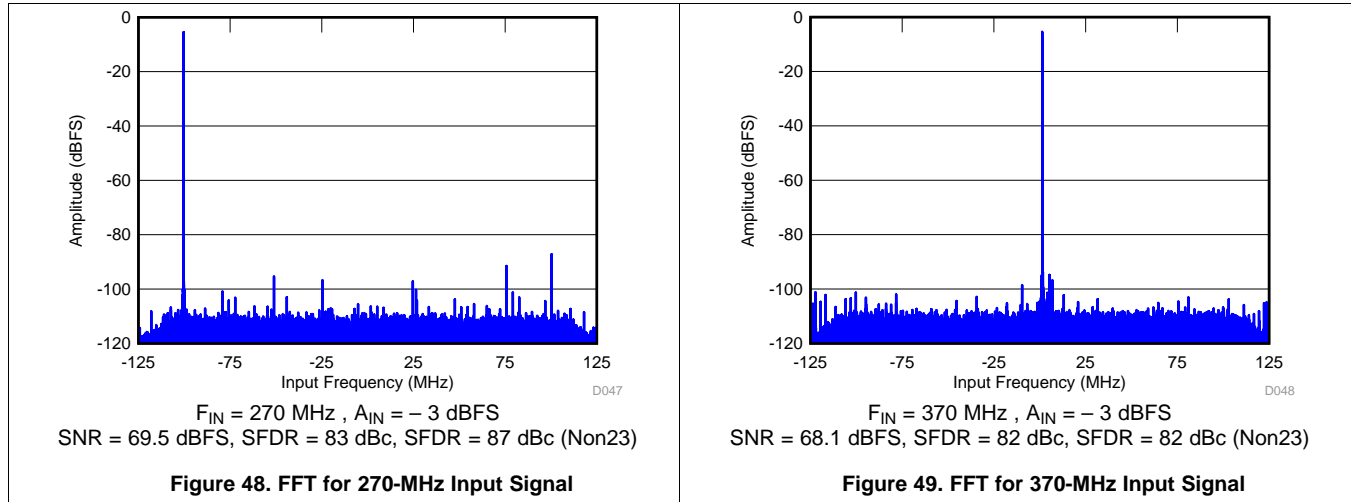
6.10 Typical Characteristics: Mode 2

Low pass or high pass decimation-by-2 filter selected as per input frequency. Typical values are at $T_A = 25^\circ\text{C}$, full temperature range is from $T_{\text{MIN}} = -40^\circ\text{C}$ to $T_{\text{MAX}} = 85^\circ\text{C}$, ADC Sampling Frequency = 500 Mpsps, 14-bit Resolution, No Decimation Filter, 50% clock duty cycle, $\text{AVDD3V} = 3\text{ V}$, $\text{AVDD} = \text{DVDD} = 1.9\text{ V}$, $\text{IOVDD} = 1.15\text{ V}$, -1-dBFS differential input for $\text{IF} \leq 250\text{ MHz}$, and -3-dBFS differential input for $\text{IF} > 250\text{ MHz}$, unless otherwise noted.



6.11 Typical Characteristics: Mode 0

Low-pass decimation-by-2 filter selected, Complex FFT plotted, mixer frequency 125 MHz. Typical values are at $T_A = 25^\circ\text{C}$, full temperature range is from $T_{\text{MIN}} = -40^\circ\text{C}$ to $T_{\text{MAX}} = 85^\circ\text{C}$, ADC Sampling Frequency = 500 Msps, 14-bit Resolution, No Decimation Filter, 50% clock duty cycle, $\text{AVDD}3\text{V} = 3\text{ V}$, $\text{AVDD} = \text{DVDD} = 1.9\text{ V}$, $\text{IOVDD} = 1.15\text{ V}$, -1-dBFS differential input for $\text{IF} \leq 250\text{ MHz}$, and -3-dBFS differential input for $\text{IF} > 250\text{ MHz}$, unless otherwise noted.



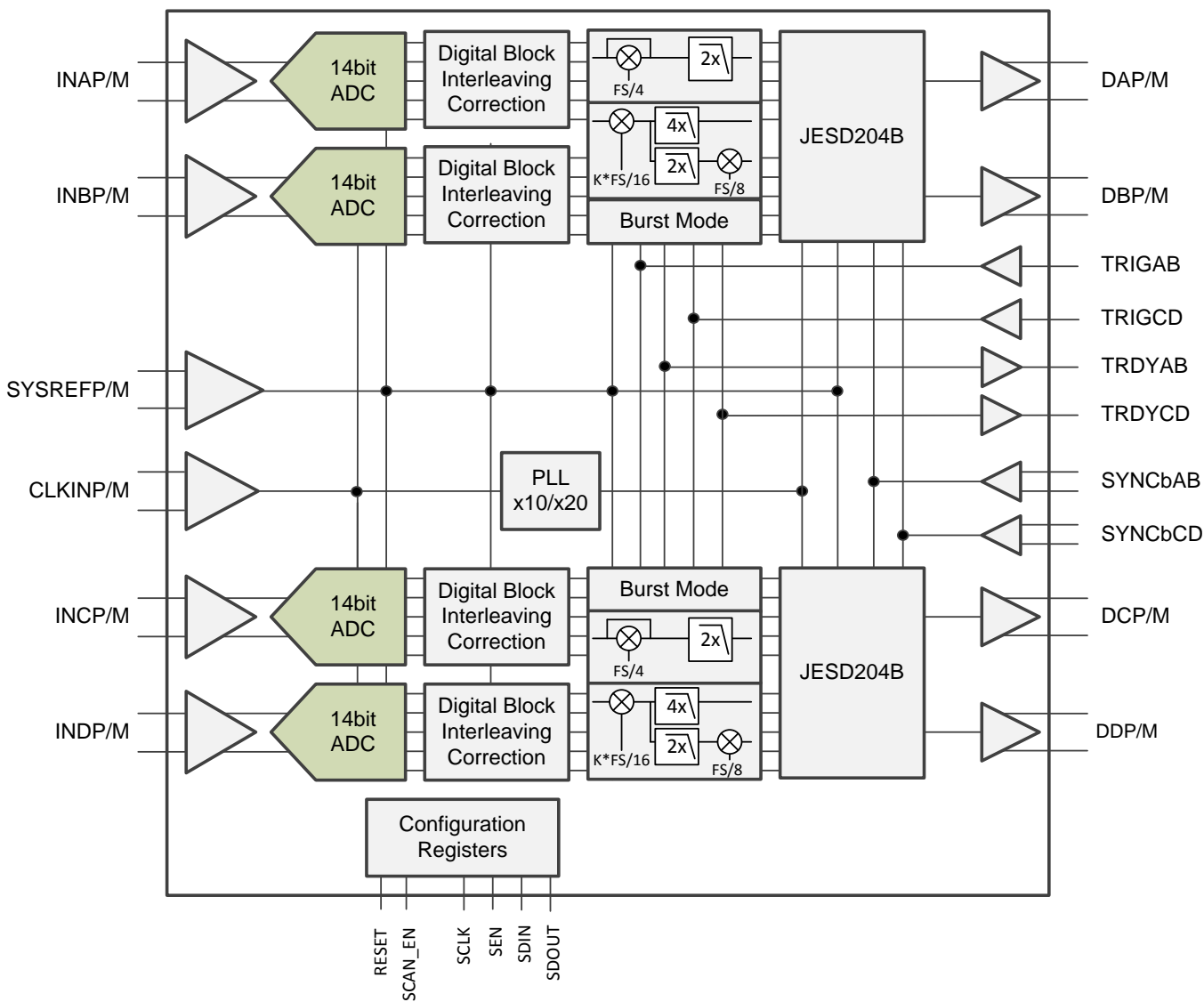
7 Detailed Description

7.1 Overview

The ADS58J63 is a low power, wide bandwidth 14-bit 500 MSPS quad channel telecom receiver IC. It supports the JESD204B serial interface with data rates up to 10 Gbps supporting 1 lane per channel. The buffered analog input provides uniform input impedance across a wide frequency range while minimizing sample-and-hold glitch energy. The ADS58J63 provides excellent spurious-free dynamic range (SFDR) over a large input frequency range with very low power consumption. Its digital block includes a 2x and 4x decimation low pass filter with FS/4 and kxFS/16 mixers to support a receive bandwidth up to 200 MHz and a output burst mode for use as DPD observation receiver.

The JESD204B interface reduces the number of interface lines allowing high system integration density. An internal phase locked loop (PLL) multiplies the incoming ADC sampling clock to derive the bit clock which is used to serialize the 14bit data from each channel.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Analog Inputs

The ADS58J63 analog signal inputs are designed to be driven differentially. The analog input pins have internal analog buffers that drive the sampling circuit. As a result of the analog buffer, the input pins present a high impedance input across a very wide frequency range to the external driving source which enables great flexibility in the external analog filter design as well as excellent 50 Ω matching for RF applications. The buffer also helps to isolate the external driving circuit from the internal switching currents of the sampling circuit which results in a more constant SFDR performance across input frequencies.

The common-mode voltage of the signal inputs is internally biased to 1.9 V using 600- Ω resistors which allows for AC coupling of the input drive network. Each input pin (INP, INM) must swing symmetrically between ($V_{CM} + 0.475$ V) and ($V_{CM} - 0.475$ V), resulting in a 1.9-V_{pp} (default) differential input swing. The input sampling circuit has a 3-dB bandwidth that extends up to 900 MHz.

7.3.2 Recommended Input Circuitry

In order to achieve optimum AC performance the following circuitry is recommended at the analog inputs.

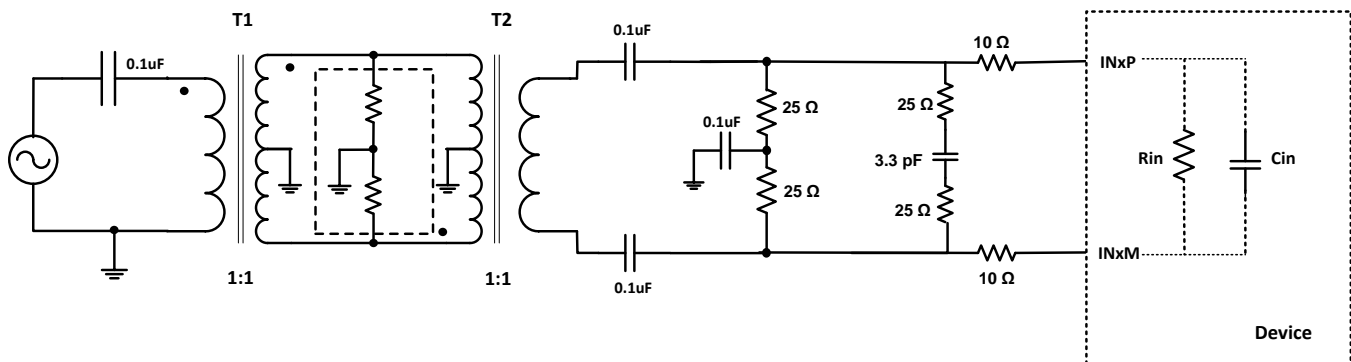


Figure 51. Analog Input Driving Circuit

7.4 Device Functional Modes

7.4.1 Digital Features

The ADS58J63 supports decimation by 2 and 4 and burst mode output. The 4 channels can be configured as pairs (A and B and C and D) to either burst or decimation mode (must be same decimation mode for all 4 channels).

Table 1. Overview of Operating Modes

| OPERATING MODE | DESCRIPTION | DIGITAL MIXER | DECIMATION | BANDWIDTH AT 491MSPs | BANDWIDTH AT 368MSPs | OUTPUT FORMAT | MAX OUTPUT RATE |
|----------------|-------------|-------------------|------------|----------------------|----------------------|---------------|-----------------|
| 0 | Decimation | $\pm f_s/4$ | 2 | 200 MHz | 150 MHz | Complex | 250 Msps |
| 2 | | – | 2 | 100 MHz | 75 MHz | Real | 250 Msps |
| 4 | | $N \times f_s/16$ | 2 | 100 MHz | 75 MHz | Real | 250 Msps |
| 5 | | $N \times f_s/16$ | 2 | 200 MHz | 150 MHz | Complex | 250 Msps |
| 6 | | $N \times f_s/16$ | 4 | 100 MHz | 75 MHz | Complex | 125 Msps |
| 7 | | $N \times f_s/16$ | 2 | 100 MHz | 75 MHz | Real | 500 Msps |
| 8 | Burst Mode | – | – | 245.76 MHz | 184.32 MHz | Real | 500 Msps |

Figure 52 shows signal processing in Digital Down-Conversion (DDC) Block in ADS58J63.

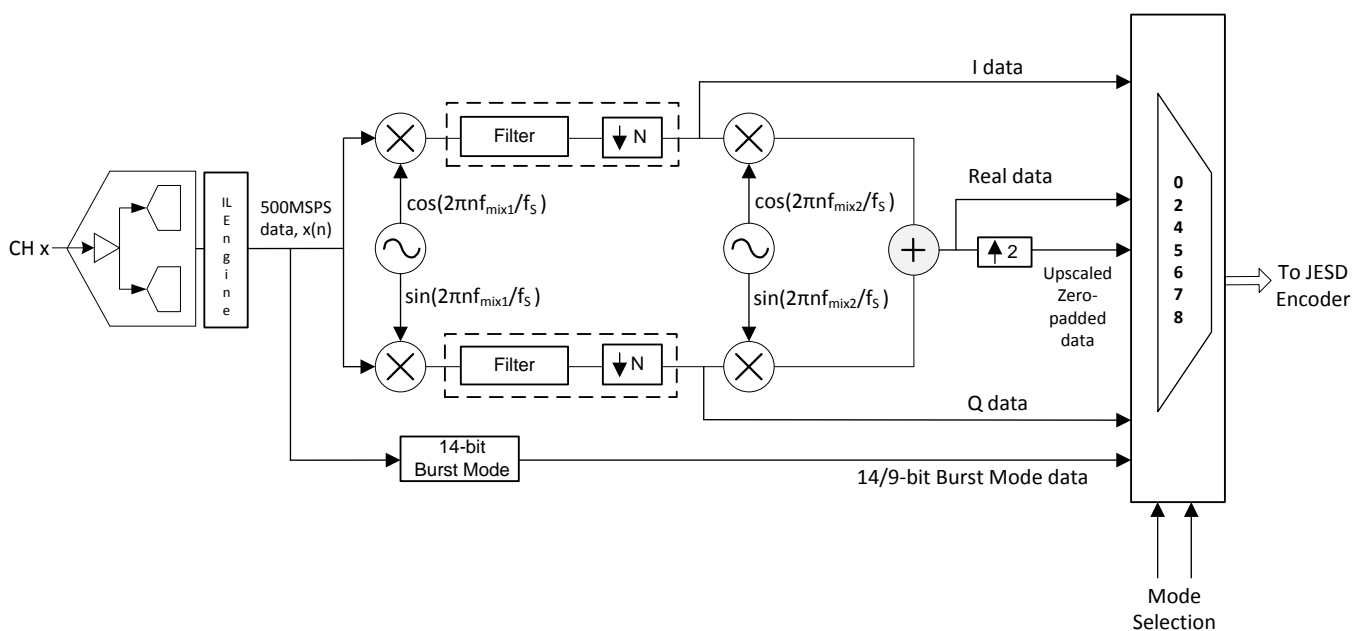


Figure 52. Digital Down-Conversion (DDC) Block

Table 2 shows characteristics of different blocks of DDC signal processing blocks active in different modes.

Table 2. Features of DDC Block in Different Modes

| Mode | f _{mix1} | Filter and Decimation | f _{mix 2} | Output |
|------|-------------------|---|--------------------|---|
| 0 | $f_s/4$ | LPF cut off freq at $f_s/4$, decimation by 2 | not used | I, Q data at 250 MSPS each is given out |
| 2 | not used | LPF or HPF cut off at $f_s/4$, decimation by 2 | not used | Straight 250 MSPS data is given out |
| 4 | $k f_s/16$ | LPF cutoff at $f_s/8$, decimation by 2 | $f_s/8$ | Real data at 250 MSPS is given out |
| 5 | $k f_s/16$ | LPF cutoff at $f_s/8$, decimation by 2 | not used | I, Q data at 250 MSPS each is given out |
| 6 | $k f_s/16$ | LPF cutoff at $f_s/8$, decimation by 4 | not used | I, Q data at 125 MSPS each is given out |
| 7 | $k f_s/16$ | LPF cutoff at $f_s/8$, decimation by 2 | $f_s/8$ | Real data is up-scaled, zero-padded and given out at 500 MSPS |
| 8 | not used | not used | not used | Straight 500 MSPS Burst mode data is given out |

7.4.2 Mode 0 – Decimation by 2 with IQ Outputs for up to 220 MHz of IQ Bandwidth

In this configuration, the DDC block includes a fixed frequency $\pm F_s/4$ complex digital mixer preceding the digital filter – so the IQ passband is $\pm \sim 110$ MHz (3 dB) centered at $F_s/4$. Mixing with $+F_s/4$ inverts the spectrum. The stop band attenuation is approximately 90 dB and the passband flatness is ± 0.1 dB. Figure 53 shows mixing operation in DDC Mode 0.

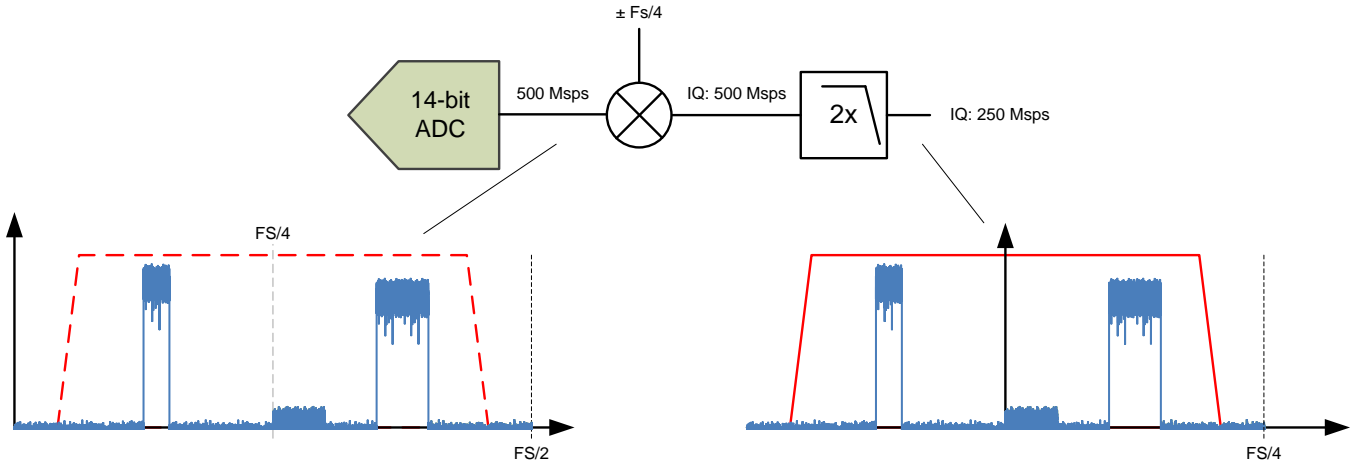
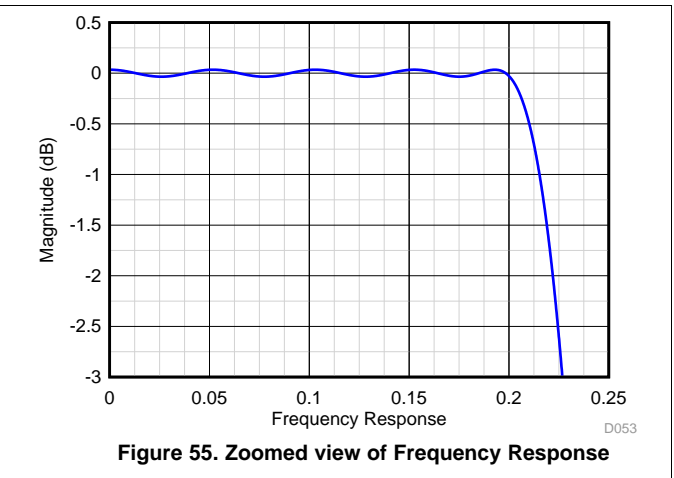
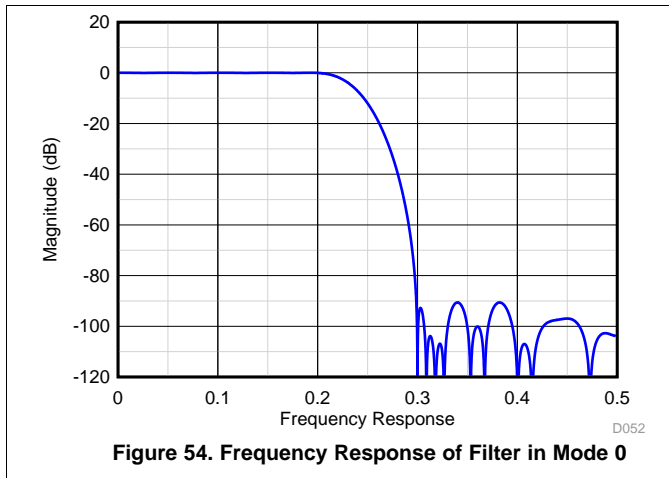


Figure 53. Mixing in Mode 0

Table 3. Filter Specification Details – Mode 0

| CORNERS | LOW PASS |
|---------|---------------|
| -0.1 dB | 0.204 × F_s |
| -0.5 dB | 0.211 × F_s |
| -1 dB | 0.216 × F_s |
| -3 dB | 0.226 × F_s |



7.4.3 Mode 2 – Decimation by 2 for up to 110 MHz of Real Bandwidth

In this configuration, the DDC block only includes a 2x decimation filter (high pass or low pass) with real outputs. The passband is ~110 MHz (3 dB). Figure 56 shows filtering operation in DDC Mode 2.

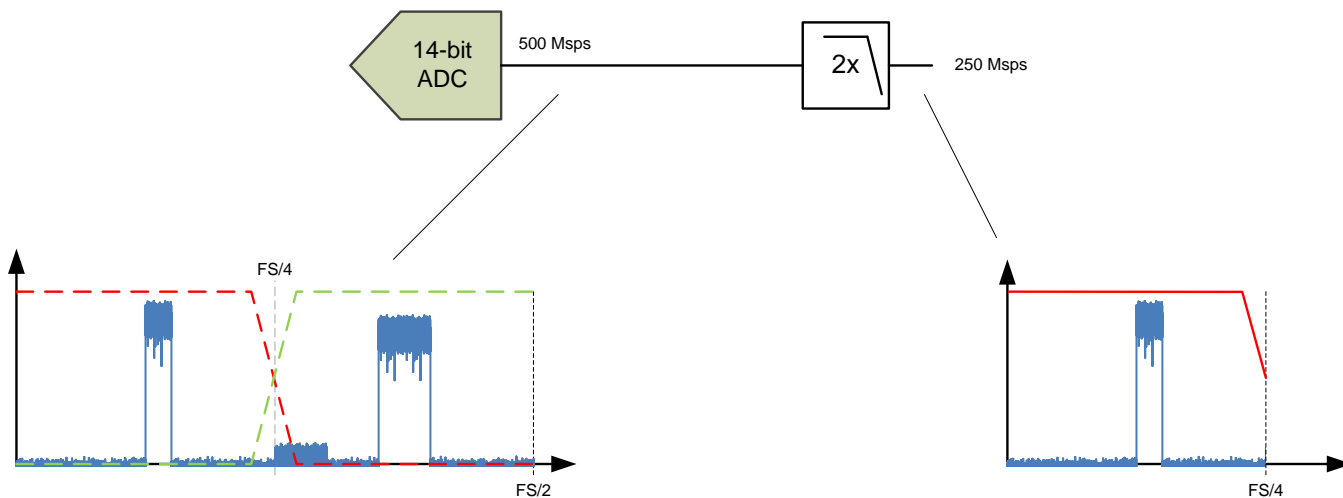


Figure 56. Filtering in Mode 2

Table 4. Filter Specification Details – Mode 2

| CORNERS | LOW PASS | HIGH PASS |
|---------|------------|------------|
| -0.1 dB | 0.204 × Fs | 0.296 × Fs |
| -0.5 dB | 0.211 × Fs | 0.290 × Fs |
| -1 dB | 0.216 × Fs | 0.284 × Fs |
| -3 dB | 0.226 × Fs | 0.274 × Fs |

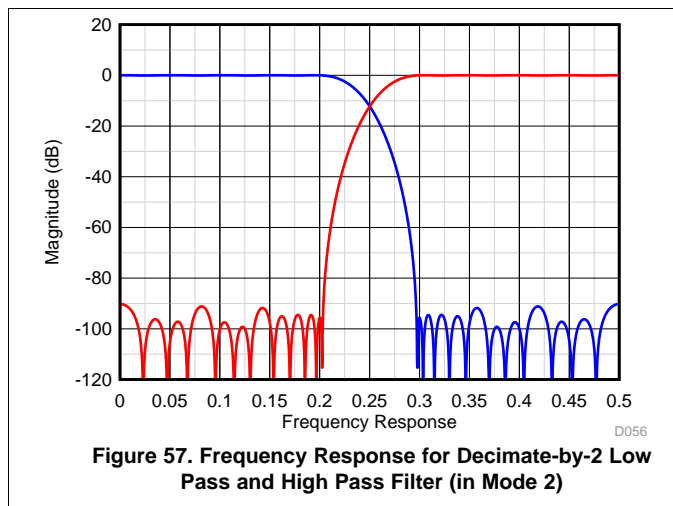


Figure 57. Frequency Response for Decimate-by-2 Low Pass and High Pass Filter (in Mode 2)

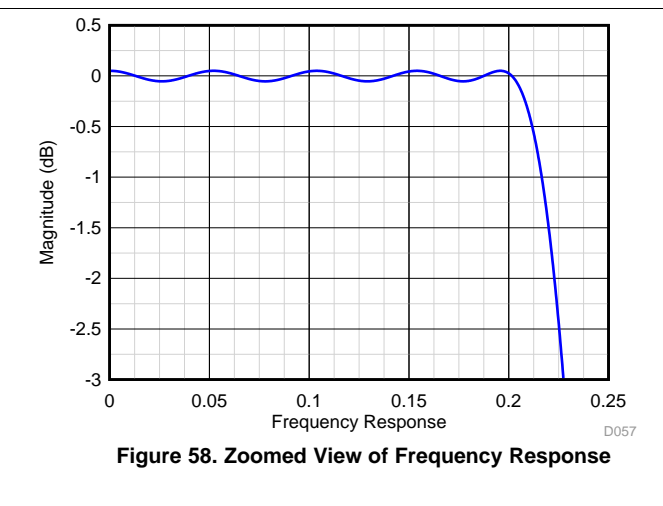


Figure 58. Zoomed View of Frequency Response

7.4.4 Mode 4/7 – Decimation by 2 with Real Outputs for up to 110 MHz of Bandwidth

In this configuration, the DDC block includes a selectable $N \times F_s/16$ complex digital mixer (N from -8 to $+7$) preceding the decimation by 2 digital filter also with an IQ passband of ± 55 MHz (3 dB) centered at $N \times F_s/16$. A positive value for N inverts the spectrum. In addition a $F_s/8$ complex digital mixer is added after the decimation filter transforming the output back to real format while centering the output spectrum within the Nyquist zone.

In addition the ADS58J63 supports a 0-pad feature where a sample with value = 0 gets added after each sample. In that way the output data rate gets interpolated to 500 Msp/s (real) with a 2nd image inverted at $F_s/2 - F_{in}$.

The stop band attenuation is approximately 90 dB for in-band aliases from negative frequencies and ~ 55 dB for out of band aliases. The passband flatness is ± 0.1 dB.

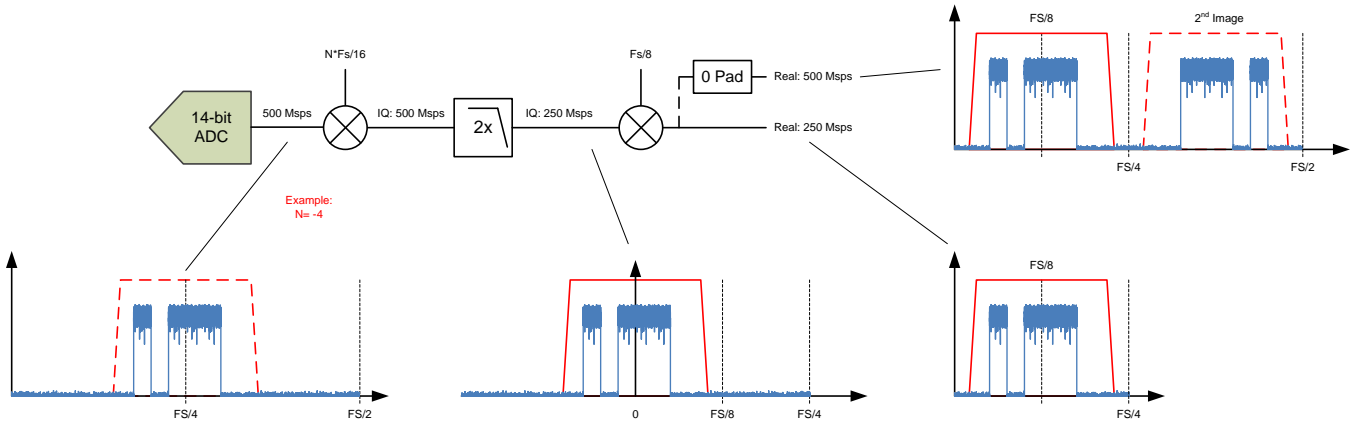


Figure 59. Mixing and Filtering in Mode 4/7

Table 5. Filter Specification Details – Mode 4/7

| CORNERS | LOW PASS |
|---------|--------------------|
| -0.1 dB | $0.102 \times F_s$ |
| -0.5 dB | $0.105 \times F_s$ |
| -1 dB | $0.108 \times F_s$ |
| -3 dB | $0.113 \times F_s$ |

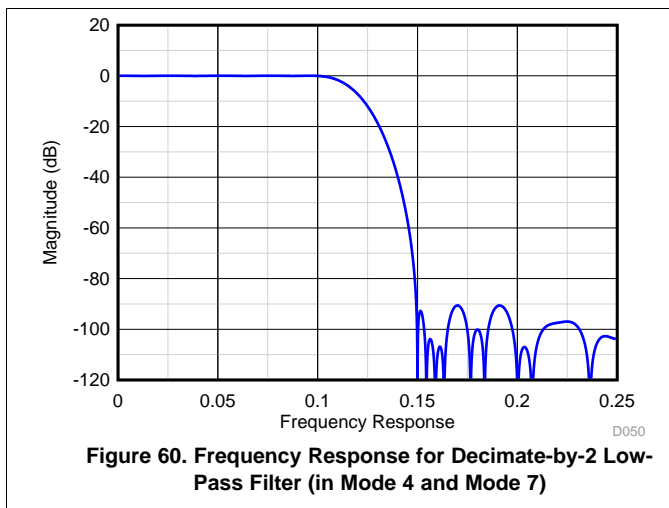


Figure 60. Frequency Response for Decimate-by-2 Low-Pass Filter (in Mode 4 and Mode 7)

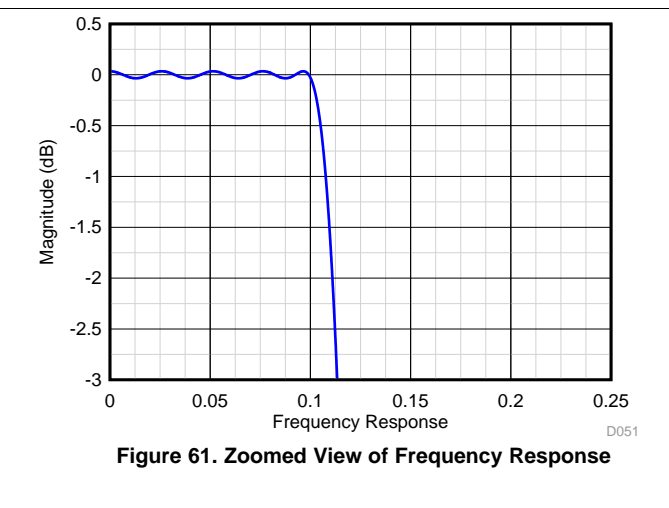


Figure 61. Zoomed View of Frequency Response

7.4.5 Mode 5 – Decimation by 2 with IQ Outputs for up to 110 MHz of IQ Bandwidth

In this configuration, the DDC block includes a selectable $N \times F_s/16$ complex digital mixer (N from -8 to $+7$) preceding the decimation by 2 digital filter – so the IQ passband is $\pm \sim 55$ MHz (3 dB) centered at $N \times F_s/16$. A positive value for N inverts the spectrum.

The stop band attenuation is approximately 90 dB for in-band aliases from negative frequencies. The passband flatness is ± 0.1 dB.

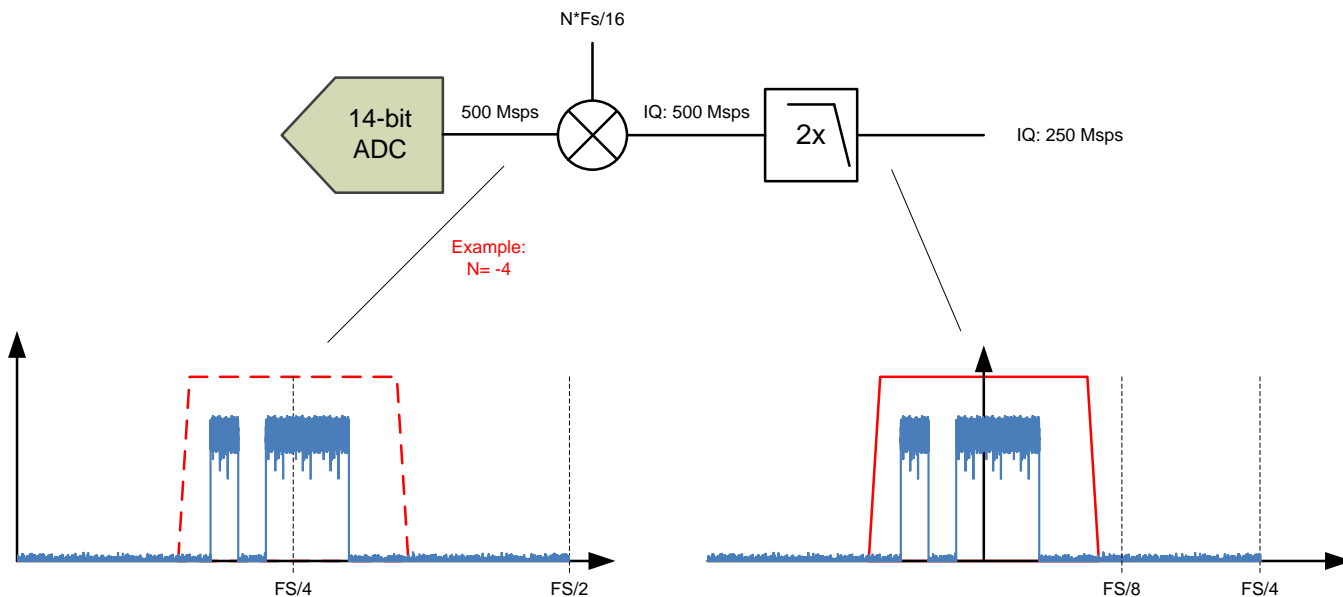
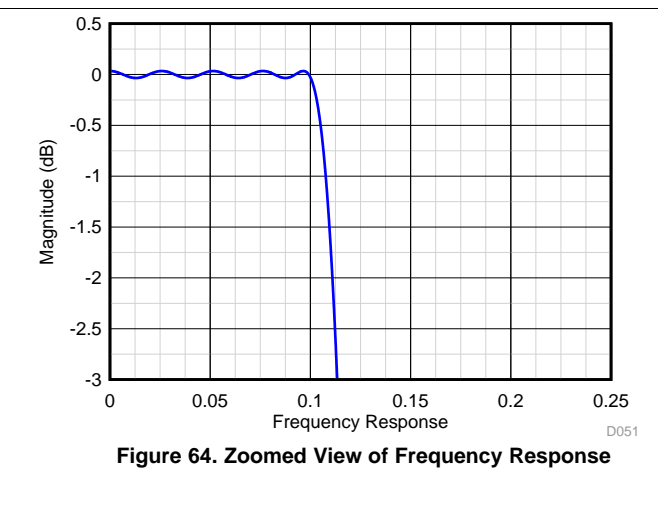
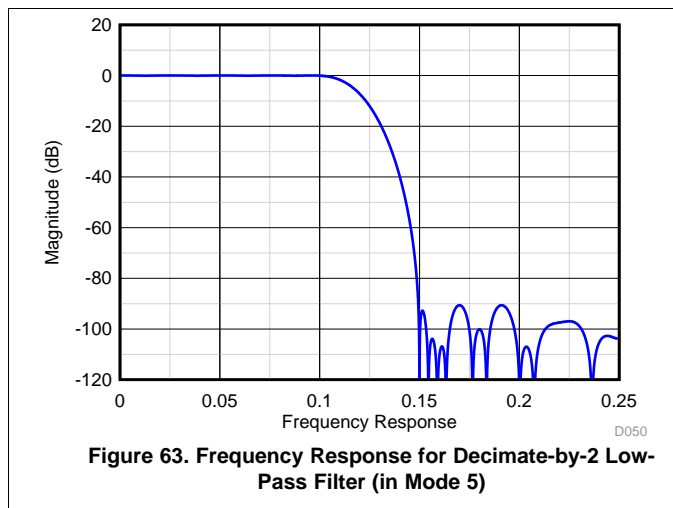


Figure 62. Mixing and Filtering in Mode 5

Table 6. Filter Specification Details – Mode 5

| CORNERS | LOW PASS |
|---------|--------------------|
| -0.1 dB | $0.102 \times F_s$ |
| -0.5 dB | $0.105 \times F_s$ |
| -1 dB | $0.108 \times F_s$ |
| -3 dB | $0.113 \times F_s$ |



7.4.6 Mode 6 – Decimation by 4 with IQ Outputs for up to 110 MHz of IQ Bandwidth

In this configuration, the DDC block includes a selectable $n \times F_s/16$ complex digital mixer (n from -8 to $+7$) preceding the decimation by 4 digital filter – so the IQ passband is $\pm \sim 55$ MHz (3 dB) centered at $n \times F_s/16$. A positive value for N inverts the spectrum. The decimation by 4 filter is a cascade of two decimation by 2 filters with frequency response shown in Figure 66.

The stop band attenuation is approximately 90 dB for in-band aliases from negative frequencies and ~ 55 dB for out of band aliases. The passband flatness is ± 0.1 dB.

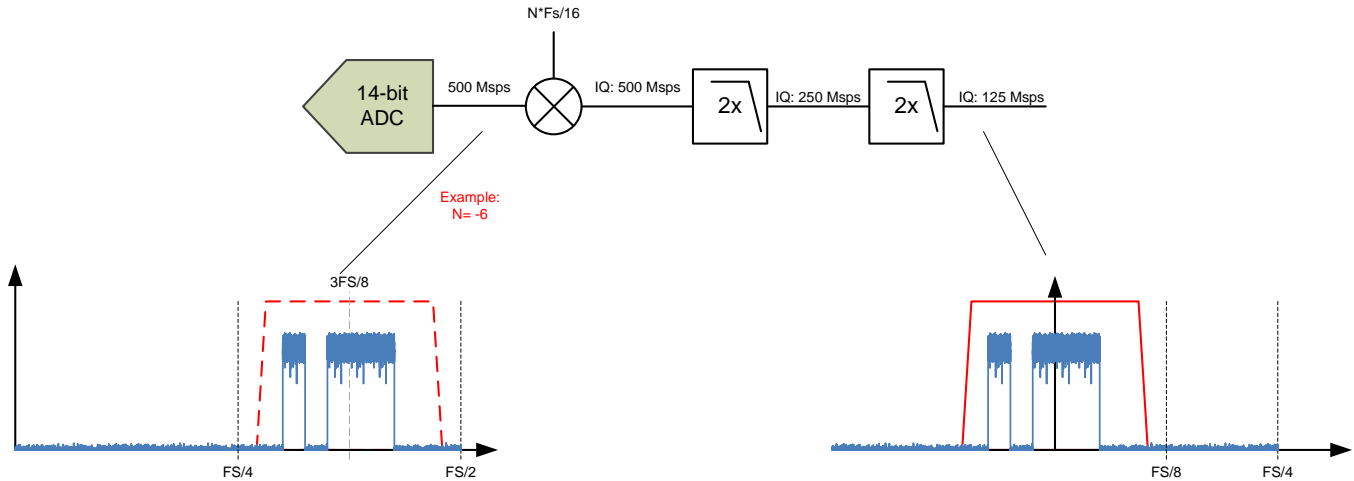


Figure 65. Mixing and Filtering in Mode 6

Table 7. Filter Specification Details – Mode 6

| CORNERS | LOW PASS |
|---------|--------------------|
| -0.1 dB | $0.102 \times F_s$ |
| -0.5 dB | $0.105 \times F_s$ |
| -1 dB | $0.108 \times F_s$ |
| -3 dB | $0.113 \times F_s$ |

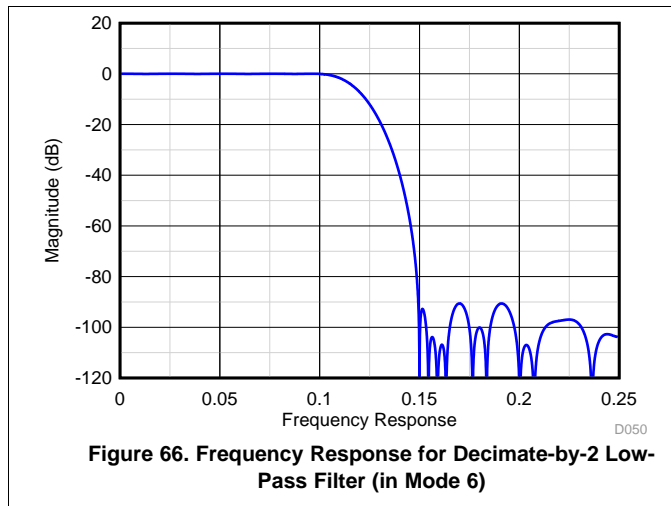


Figure 66. Frequency Response for Decimate-by-2 Low-Pass Filter (in Mode 6)

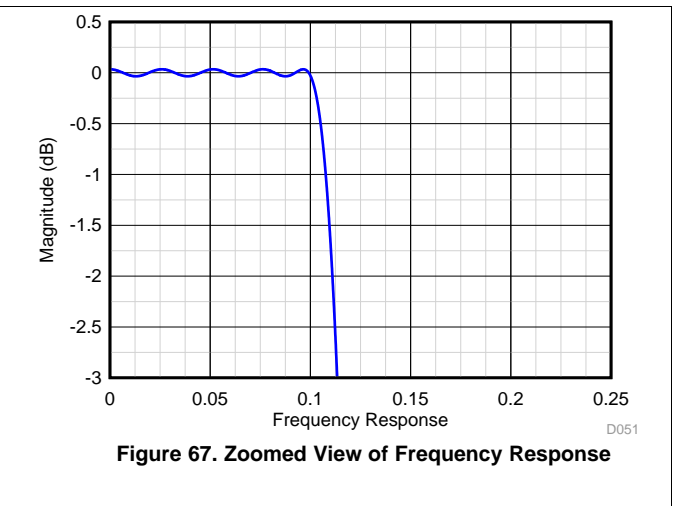


Figure 67. Zoomed View of Frequency Response

7.4.7 Mode 8 – Burst Mode

In burst mode the output data is alternated between low resolution (L, 9-bit) and high resolution (H, 14-bit) output. The burst mode can be configured via SPI register writes independently for channel A/B and channel C/D.

The high resolution output is 14 bit and the number (#) of high and low resolution samples is set with two user programmable counters – one for high resolution (HC) and one for low resolution (LC). There is one counter pair (HC, LC) for channel A/B and one pair for channel C/D. The internal logic checks if the maximum duty cycle is exceeded and if necessary resets the counters to its default values.

Each output cycle starts with a low resolution and the counter values can be reconfigured for the next cycle during prior to the start of the next cycle.

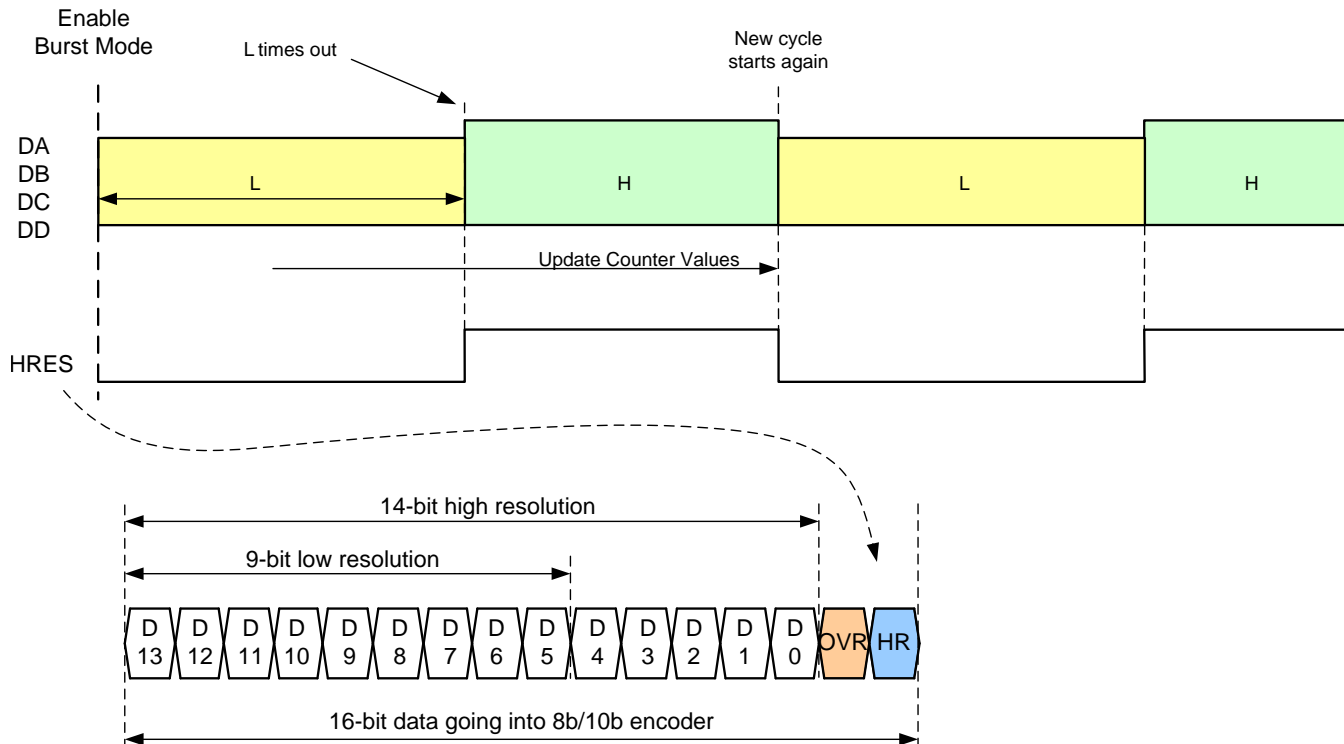


Figure 68. Timing Diagram for 14-bit Burst Mode (DDC Mode 8)

The counter values for high and low resolution can be programmed to:

High resolution counter (HC): 1 to 2^{25}

Low resolution counter (LC); 1 to 2^{28}

The output duty cycle limit is illustrated in Table 8.

Table 8. Output Duty Cycle Limit

| HIGH RESOLUTION OUTPUT | LOW RESOLUTION OUTPUT | MAXIMUM ALLOWED DUTY CYCLE (high : low resolution output) | DEFAULT VALUE HC | DEFAULT VALUE LC |
|------------------------|-----------------------|---|------------------|------------------|
| 14 bit | 9 bit | 1/3 | 1 | 3 |

7.4.8 Trigger Input

The burst mode can be operated in auto trigger or manual trigger mode. In manual trigger mode the TRIGGER input (TRIGAB, TRIGCD) is used to release the high resolution data (HC) burst after the low resolution data counter LC has timed out. In auto trigger mode the high resolution data is released immediately after completion of the last low resolution sample.

Using SPI control the ADS58J63 can be configured to use TRIGAB or TRIGCD as the manual trigger input.

7.4.9 Manual Trigger Mode

Upon enabling manual trigger mode, the ADS58J63 starts transmission of low resolution data. As soon as the LC counter is finished, the manual trigger is unlocked, the trigger ready flag (TRDY) is raised and the high resolution output H can be triggered. Once the low resolution counter LC is finished, the next high resolution output or burst mode sequence can be triggered again. The HRES flag is embedded in the JESD204B output data stream. The counter values can be updated until a new burst mode cycles starts with transmission of low resolution samples.

Example of burst mode with manual trigger:

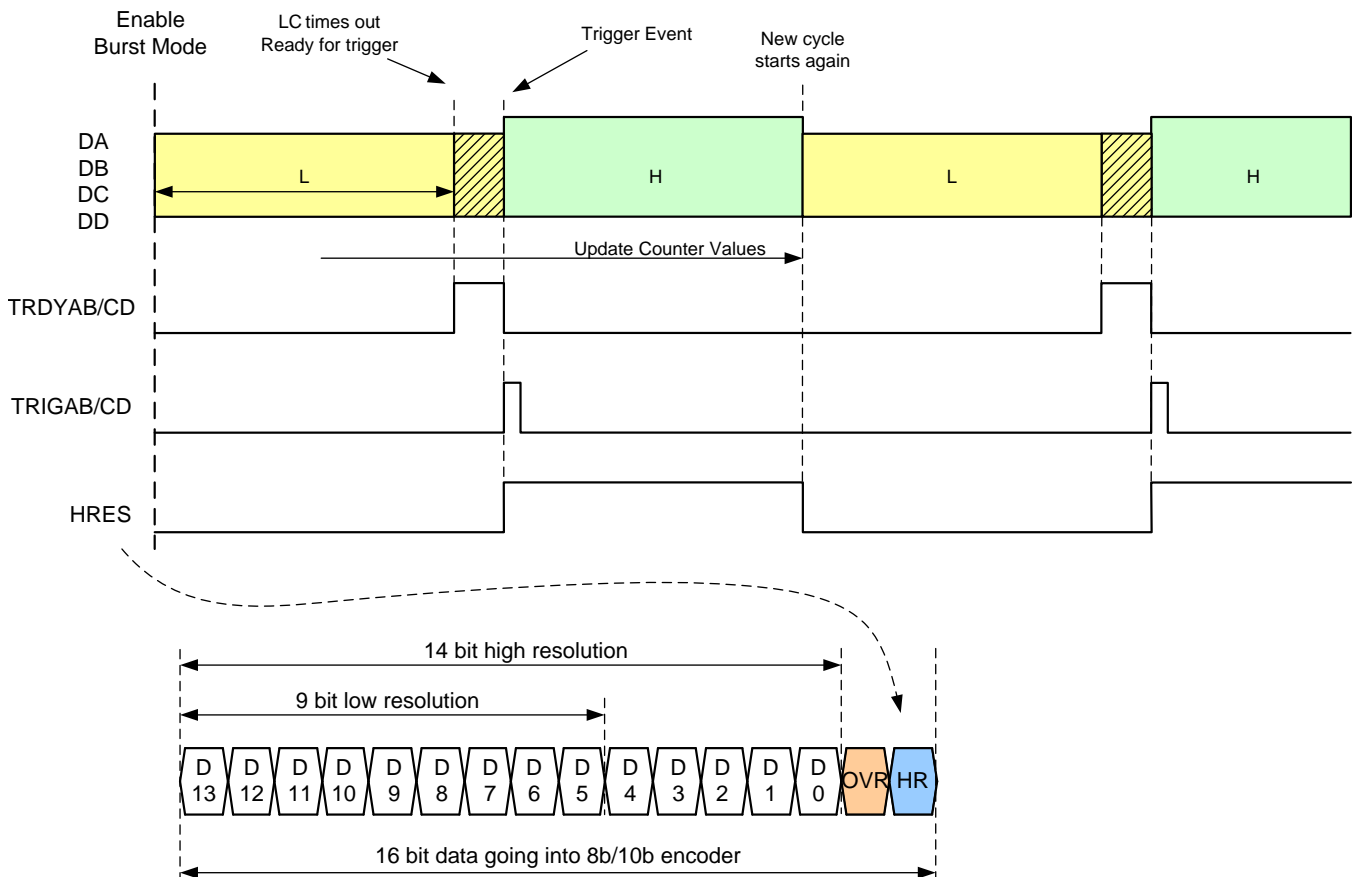


Figure 69. Timing Diagram for Manual Trigger Mode

7.4.10 Auto Trigger Mode

Upon enabling auto trigger mode, the ADS58J63 starts transmission of low resolution data. As soon as the low resolution samples counter (LC) is finished, the ADS58J63 immediately begins transmitting the high resolution output H. The HRES flag can also be embedded in the JESD204B output data stream. The counter values can be updated until a new burst mode cycles starts with transmission of low resolution samples. Any input on the trigger input pins is ignored.

Example of burst mode with automatic trigger:

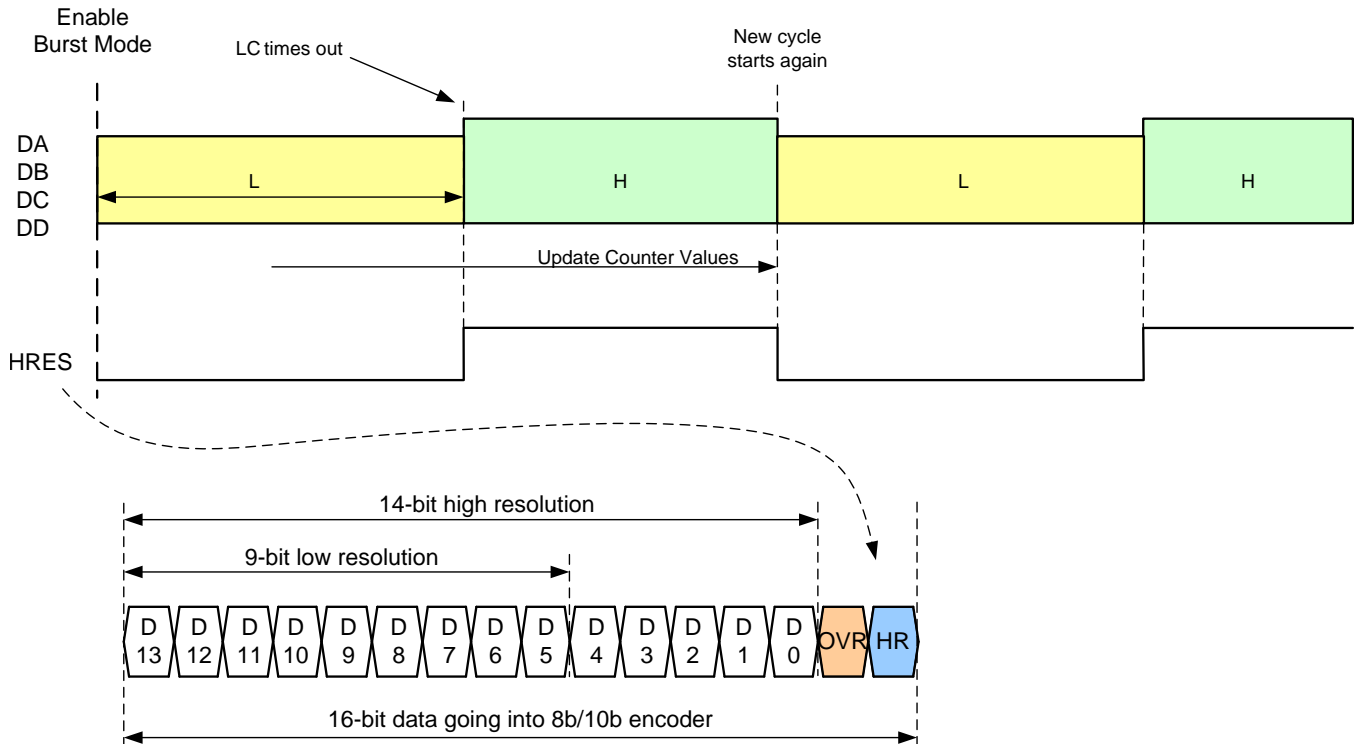


Figure 70. Timing Diagram for Auto Trigger Mode

7.4.11 Over-range Indication

The ADS58J63 provides a fast over-range indication (FOVR) which can be presented in the digital output data stream via SPI configuration. When the FOVR indication is embedded in the output data stream, it replaces the LSB (normal 0) of the 16 bit going to the 8b/10b encoder.

One threshold is set per channel pair A/B and C/D.

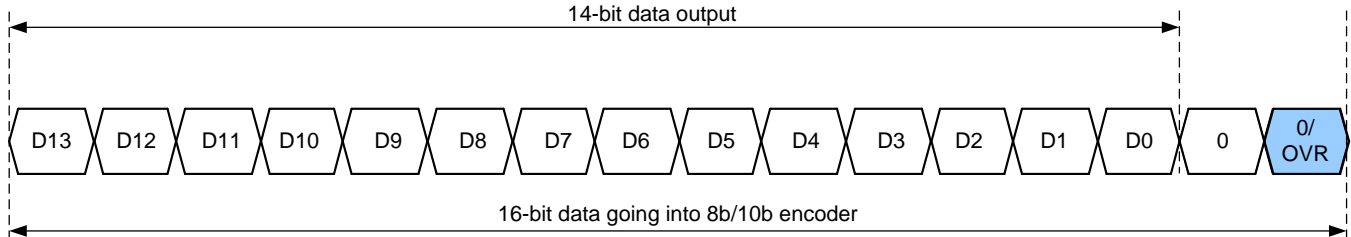


Figure 71. Timing Diagram for FOVR

The fast OVR is triggered if the input voltage exceeds the programmable overrange threshold and it gets presented after just 44 input clock cycles enabling a quicker reaction to an overrange event.

The input voltage level at which the overload is detected is referred to as the threshold. It is programmable using the FOVR THRESHOLD bits.

The input voltage level at which fast OVR is triggered is:
 Full-scale × [the decimal value of the FOVR Threshold bits] / 255)

The default threshold is E3h (227) which corresponds to a threshold of –1 dBFS.

In terms of full scale input, the fast OVR threshold can be calculated as shown in [Equation 1](#):

$$20 \times \log (<FOVR \text{ Threshold}>/255). \quad (1)$$

Following is an example register write to set the FOVR threshold for all 4 channels:

Table 9. Register Sequence for FOVR Configuration

| ADDRESS | DATA | COMMENT |
|---------|------|------------------------------------|
| 11h | 80h | Go to Master page |
| 59h | 20h | Enable FOVR |
| 11h | FFh | Go to ADC page |
| 5Fh | FFh | Set FOVR threshold for chCD to 255 |
| 4004h | 68h | Go to main digital page |
| 4003h | 00h | |
| 60ABh | 01h | Enable bit D0 overwrite |
| 60ADh | 03h | Select FOVR to replace bit D0 |
| 6000h | 01h | Issue and clear digital reset |
| 6000h | 00h | |

7.4.12 Power-Down Mode

The ADS58J63 provides a highly-configurable power-down mode. Power-down can be enabled using the PDN pin or SPI register writes.

A power-down mask can be configured, which allows a trade-off between wake-up time and power consumption in power-down mode. Two independent power-down masks can be configured: MASK 1 and MASK 2 as shown in Table 10. See the master page registers in Table 15 for further details.

Table 10. Register Address for Power-Down Modes

| REGISTER ADDRESS A[7:0] (Hex) | COMMENT | REGISTER DATA | | | | | | | |
|----------------------------------|---------|-----------------|------------------|--------------|----------|--------------|---|---|---|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| MASTER PAGE (80h) | | | | | | | | | |
| 20 | MASK 1 | PDN ADC CHAB | | | | PDN ADC CHCD | | | |
| 21 | | PDN BUFFER CHCD | PDN BUFFER CHAB | 0 | 0 | 0 | 0 | | |
| 23 | MASK 2 | PDN ADC CHAB | | | | PDN ADC CHCD | | | |
| 24 | | PDN BUFFER CHCD | PDN BUFFER CHAB | 0 | 0 | 0 | 0 | | |
| 26 | CONFIG | GLOBAL PDN | OVERRIDE PDN PIN | PDN MASK SEL | 0 | 0 | 0 | 0 | 0 |
| 53 | | 0 | MASK SYSREF | 0 | 0 | 0 | 0 | 0 | 0 |
| 55 | | 0 | 0 | 0 | PDN MASK | 0 | 0 | 0 | 0 |

To save power, the device can be put in complete power down by using the GLOBAL PDN register bit. However, when JESD link must remain up while putting the device in power down, the ADC and analog buffer can be powered down by using the PDN ADC CHx and PDN BUFFER CHx register bits after enabling the PDN MASK register bit. The PDN MASK SEL register bit can be used to select between MASK 1 or MASK 2. Table 11 shows power consumption for different combinations of the GLOBAL PDN, PDN ADC CHx, and PDN BUFF CHx register bits.

Table 11. Power Consumption in Different Power-Down Settings

| REGISTER BIT | COMMENT | IAVDD3V (mA) | IAVDD (mA) | IDVDD (mA) | IIOVDD (mA) | TOTAL POWER (W) |
|--|---|--------------|------------|------------|-------------|-----------------|
| Default | After reset, with a full-scale input signal to both channels | 0.340 | 0.365 | 0.184 | 0.533 | 2.675 |
| GBL PDN = 1 | The device is in complete power-down state | 0.002 | 0.006 | 0.012 | 0.181 | 0.247 |
| GBL PDN = 0, PDN ADC CHx = 1 (x = AB or CD) | The ADCs of one pair of channels are powered down | 0.277 | 0.225 | 0.123 | 0.496 | 2.063 |
| GBL PDN = 0, PDN BUFF CHx = 1 (x = AB or CD) | The input buffers of one pair of channels are powered down | 0.266 | 0.361 | 0.187 | 0.527 | 2.445 |
| GBL PDN = 0, PDN ADC CHx = 1, PDN BUFF CHx = 1 (x = AB or CD) | The ADCs and input buffers of one pair of channels are powered down | 0.200 | 0.224 | 0.126 | 0.492 | 1.830 |
| GBL PDN = 0, PDN ADC CHx = 1, PDN BUFF CHx = 1 (x = AB and CD) | The ADCs and input buffers of all channels are powered down | 0.060 | 0.080 | 0.060 | 0.448 | 0.960 |

7.5 Programming

7.5.1 Device Configuration

The ADS58J63 can be configured using a serial programming interface, as described below. In addition, the device has one dedicated parallel pin (PDN) for controlling the power down modes. The ADS58J63 supports a 24-bit (16-bit address, 8-bit data) SPI operation and uses paging (see detailed register map info) to access all register bits.

7.5.1.1 Details of Serial Interface

The ADC has a set of internal registers that can be accessed by the serial interface formed by the SEN (serial interface enable), SCLK (serial interface clock) and SDIN (serial interface data) pins. Serial shift of bits into the device is enabled when SEN is low. Serial data on SDIN are latched at every SCLK rising edge when SEN is active (low). The interface can work with SCLK frequencies from 5 MHz down to very low speeds (of a few hertz) and also with non-50% SCLK duty cycle.

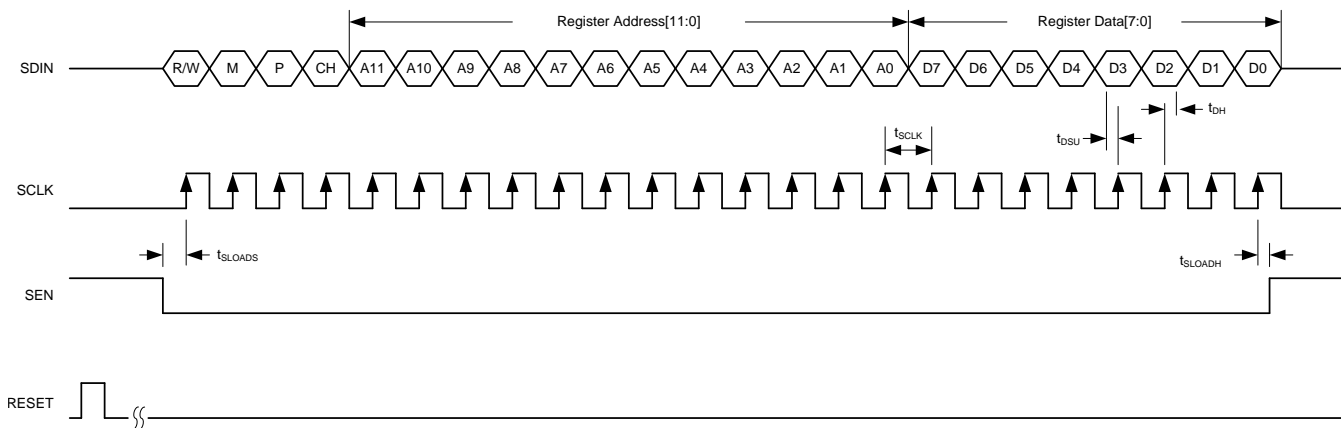


Figure 72. Serial Interface Timing Diagram

Table 12. Programming Details of Serial Interface

| SPI BITS | DESCRIPTION | OPTIONS |
|-------------|---|--|
| R/W | Read/write bit | 0 = SPI write 1 = SPI read back |
| M | SPI bank access | 0 = Analog SPI bank (Master and ADC page) 1 = JDigital SPI bank (Main Digital, Analog JESD, and Digital JESD pages) |
| P | JESD page selection bit | 0 = Page access 1 = Register access |
| CH | SPI access for a specific channel of the digital SPI bank | 0 = Channel AB 1 = Channel CD By default, both channels are being addressed. |
| ADDR [11:0] | SPI address bits | — |
| DATA [7:0] | SPI data bits | — |

7.5.1.2 Serial Register Write: Analog Bank

The analog SPI bank contains of two pages (the master and ADC page). The internal register of the ADS58J63 analog SPI bank can be programmed by:

1. Drive the SEN pin low.
2. Initiate a serial interface cycle specifying the page address of the register whose content must be written.
 - Master page: write address 0011h with 80h.
 - ADC page: write address 0011h with 0Fh.
3. Write the register content as shown in [Figure 73](#). When a page is selected, multiple writes into the same page can be done.

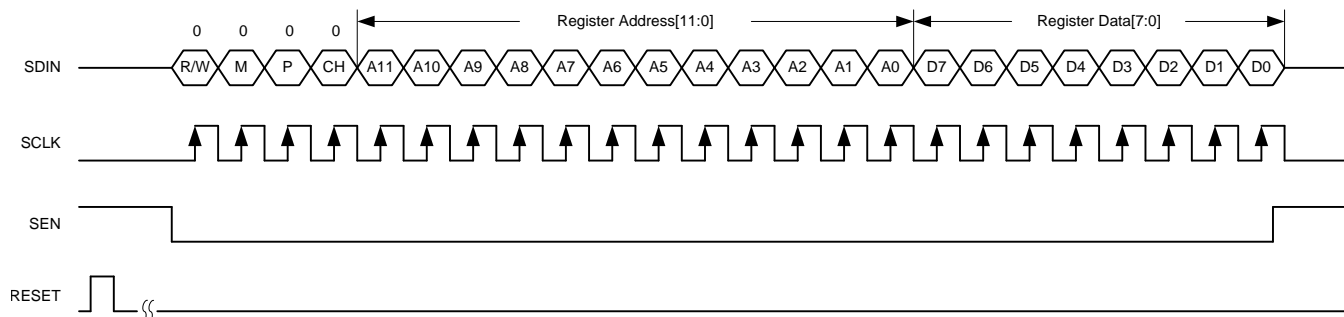


Figure 73. Serial Register Write Timing Diagram

7.5.1.3 Serial Register Readout: Analog Bank

The content from one of the two analog banks can be read out by:

1. Drive the SEN pin low.
2. Select the page address of the register whose content must be read.
 - Master page: write address 0011h with 80h.
 - ADC page: write address 0011h with 0Fh.
3. Set the R/W bit to 1 and write the address to be read back.
4. Read back the register content on the SDOUT pin, as shown in [Figure 74](#). When a page is selected, multiple read backs from the same page can be done.

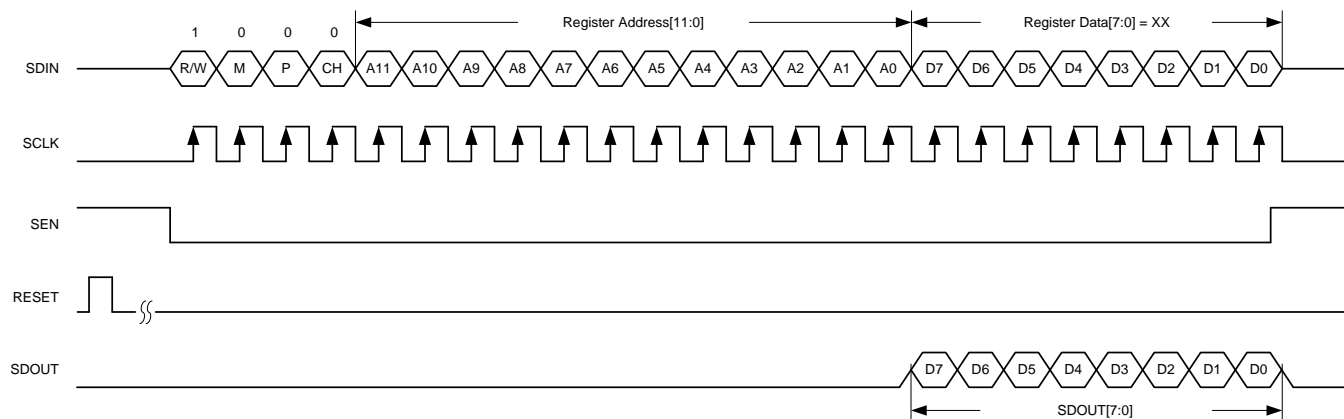


Figure 74. Serial Register Read Timing Diagram

7.5.1.4 JESD Bank SPI Page Selection

The JESD SPI bank contains four pages (main digital, interleaving engine, digital, and analog JESD pages). The individual pages can be selected by:

1. Drive the SEN pin low.
2. Set the M bit to 1 and specify the page with two register writes. Note that the P bit must be set to 0, as shown in [Figure 75](#).
 - Write address 4003h with 00h (LSB byte of page address).
 - Write address 4004h with the MSB byte of the page address.
 - For Main digital page: write address 4004h with 68h.
 - For Digital JESD page: write address 4004h with 69h.
 - For Analog JESD page: write address 4004h with 6Ah.
 - For Interleaving engine page: write address 4004h with 61h.

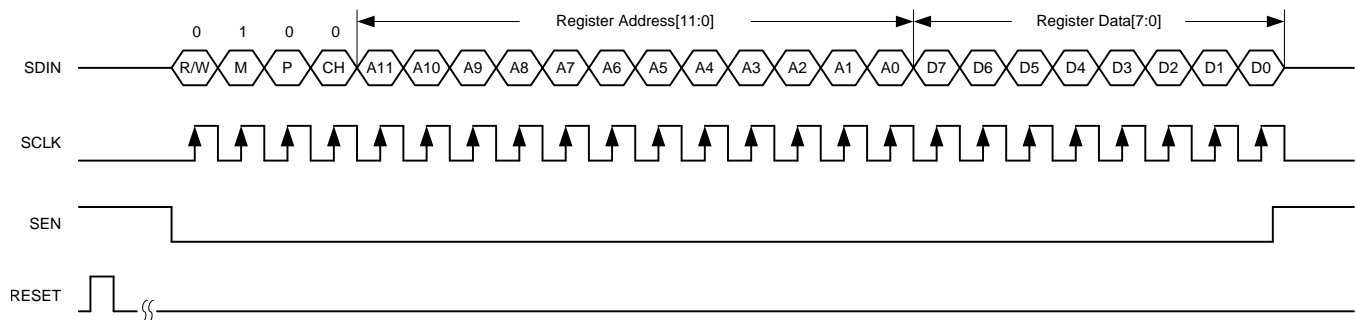


Figure 75. SPI Page Selection

7.5.1.5 Serial Register Write: Analog Bank

The analog SPI bank contains two pages (Master and ADC page). The internal register of the ADS58J63 analog SPI bank can be programmed following these steps:

1. Drive the SEN pin low.
2. Initiate a serial interface cycle specifying the page address of the register whose content has to be written
 - Master page: write address 11h with 80h
 - ADC page: write address 11h with 0Fh
3. Write register content. Once a page is selected, multiple writes into the same page can be done.

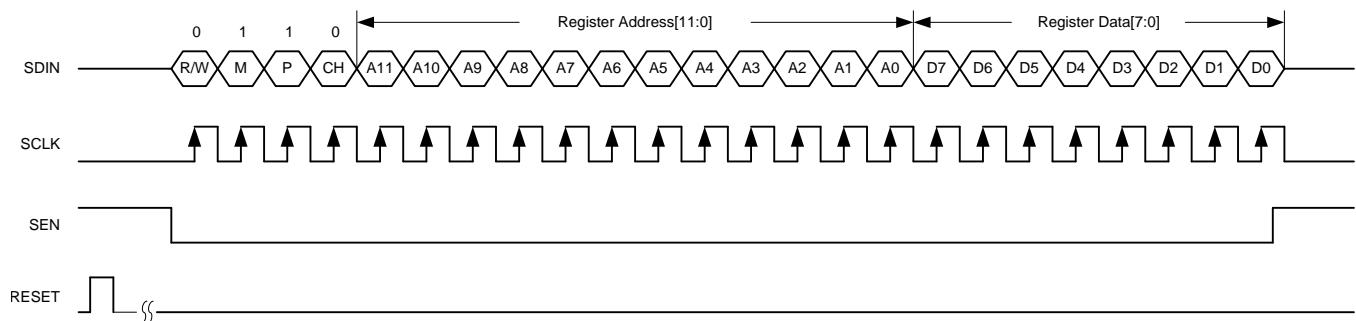


Figure 76. Serial Register Write Timing Diagram

7.5.1.6 Serial Register Readout: Analog Bank

SPI read out of content in one of the two analog banks can be accomplished with the following steps:

1. Drive the SEN pin low.
2. Select the page address of the register which content has to be read.
 - Master page: write Address = 11h with 80h
 - ADC page: write Address 11h with 0Fh.
3. Set the R/W bit to '1' and write the address to be read back.
4. Read back register content on the SDOUT pin. Once a page is selected, multiple read backs from the same page can be done.

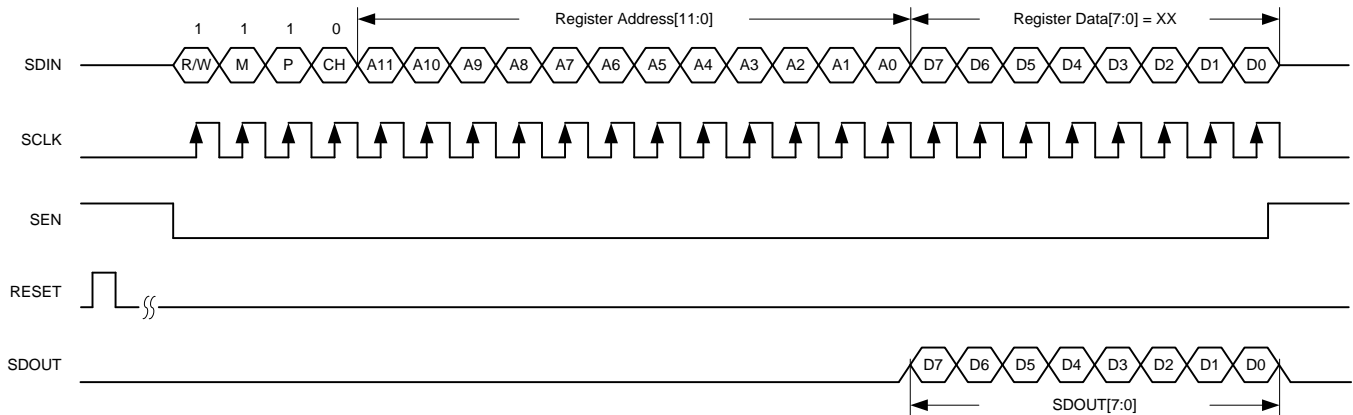


Figure 77. Serial Register Read Timing Diagram

7.5.1.7 Digital Bank SPI Page Selection

The Digital SPI bank contains five pages (Main digital, Interleaving Engine, Decimation filter, JESD digital, and JESD analog). The individual pages can be selected following these steps:

1. Drive the SEN pin low.
2. Set the M bit to '1' and specify the page with two register writes (Note: P bit set to 0)
 - Write address 4003h with 00h (LSB byte of page address)
 - Write address 4004h MSB byte of page address
 - Main digital page: write Address = 4004h with 68h (default)
 - Digital JESD page: write Address = 4004h with 69h
 - Analog JESD page: write Address = 4004h with 6Ah
 - Interleaving Engine page: write Address = 4004h with 61h
 - Decimation Filter page: write Address = 4004h with 61h and 4003h with 41h

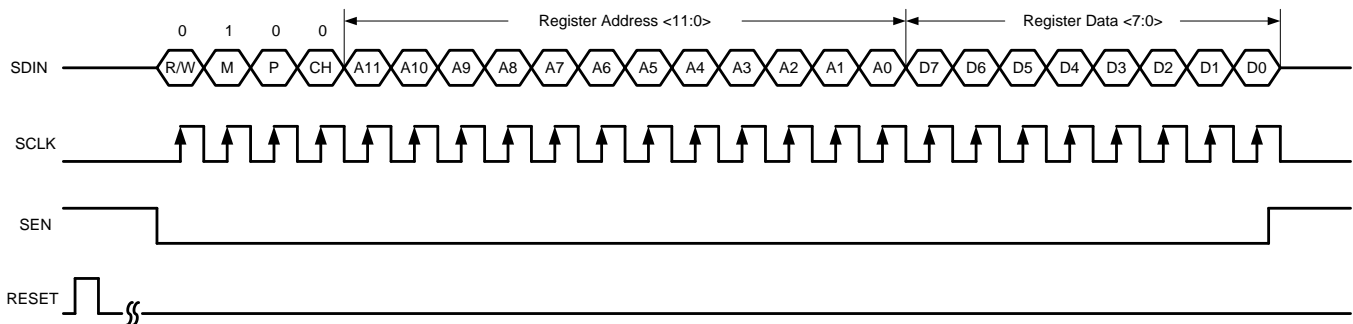


Figure 78. SPI Timing Diagram for Digital Bank Page Selection

7.5.1.8 Serial Register Write – Digital Bank

The ADS58J63 is a quad channel device and the JESD204B portion is configured individually for 2 channel (A/B and C/D) using the CH bit. Note the P bit needs to be set to 1 for register writes.

1. Drive the SEN pin low.
2. Select the digital bank page (Note: M bit = 1, P bit = 0)
 - Write address 4003h with 00h
 - Main digital page: write Address = 4004h with 68h (default)
 - Digital JESD page: write Address = 4004h with 69h
 - Analog JESD page: write Address = 4004h with 6Ah
 - Interleaving Engine page: write Address = 4004h with 61h
 - Decimation Filter page: write Address = 4004h with 61h and 4003h with 41h
3. Set M and P bit to 1 and select ChAB (CH=0) or ChCD (CH=1) and write register content. Once a page is selected, multiple writes into the same page can be done.

By default, register writes are applied to both channel pairs (broadcast mode). To disable broadcast mode and enable individual channel writes, write address 4005h with 01h (default is 00h).

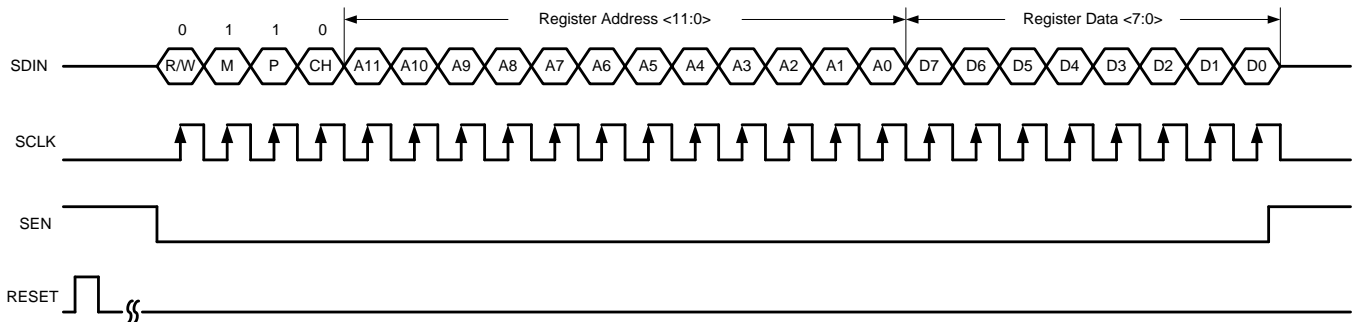


Figure 79. Serial Register Write Timing Diagram

7.5.1.9 Individual Channel Programming

By default, register writes are applied to both channels. To enable individual channel writes, write address 4005h with 01h (default is 00h).

7.5.1.10 Serial Register Readout – Digital Bank

SPI read out of content in one of the three digital banks can be accomplished with the following steps:

1. Drive the SEN pin low.
2. Select the digital bank page (Note: M bit = 1, P bit = 0)
 - Write address 4003h with 00h
 - Main digital page: write Address = 4004h with 68h
 - Digital JESD page: write Address = 4004h with 69h
 - Analog JESD page: write Address = 4004h with 6Ah
 - Interleaving Engine page: write Address = 4004h with 61h
 - Decimation Filter page: write Address = 4004h with 61h and 4003h with 41h
3. Set the R/W bit, M and P bit to '1' and select ChAB) or ChCD) and write the address to be read back.
4. Read back register content on the SDOOUT pin. Once a page is selected, multiple read backs from the same page can be done.

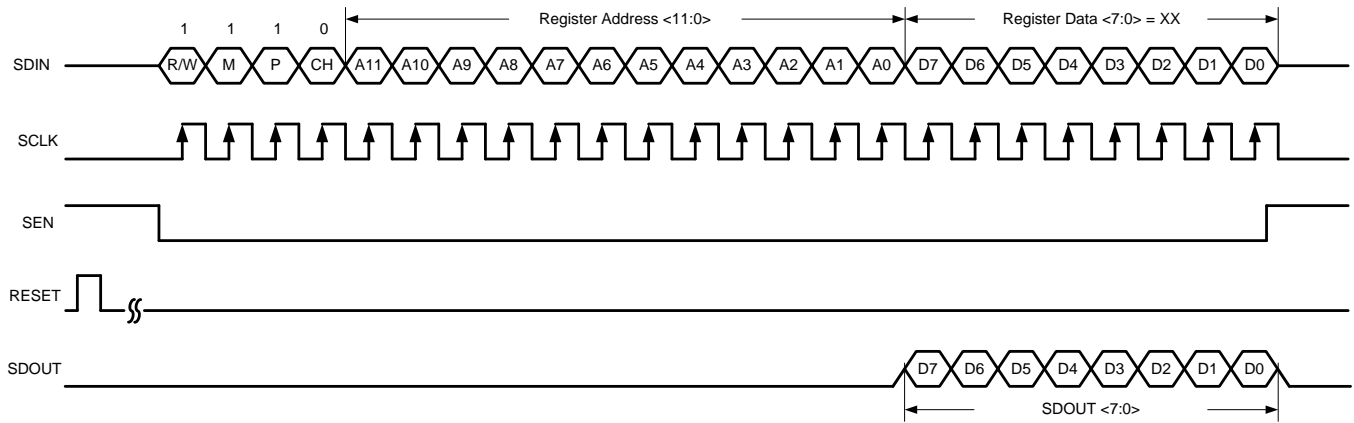


Figure 80. Serial Register Read Timing Diagram

7.5.2 JESD204B Interface

The ADS58J63 supports device subclass 1 with a maximum output data rate of 10 Gbps for each serial transmitter.

An external SYSREF signal is used to align all internal clock phases and the local multi frame clock to a specific sampling clock edge. This allows synchronization of multiple devices in a system and minimizes timing and alignment uncertainty. The ADS58J63 supports single (for all 4 JESD links) or dual (for channel A/B and C/D) SYNCb inputs and can be configured via SPI.

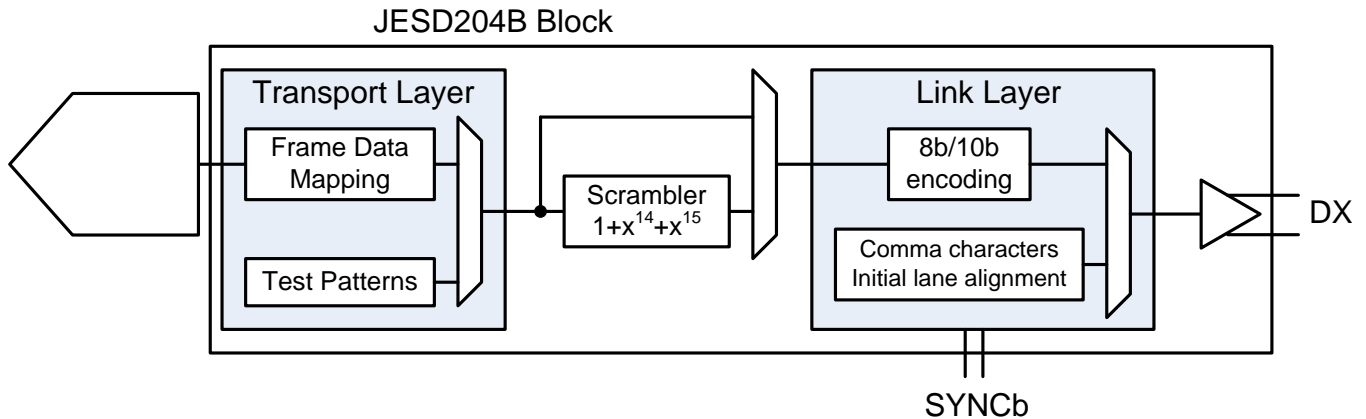


Figure 81. JESD Interface Block Diagram

Depending on the ADC sampling rate, the JESD204B output interface can be operated with 1 lane per channel. The JESD204B setup and configuration of the frame assembly parameters is handled via SPI interface.

The JESD204B transmitter block consists of the transport layer, the data scrambler and the link layer. The transport layer maps the ADC output data into the selected JESD204B frame data format and manages if the ADC output data or test patterns are being transmitted. The link layer performs the 8b/10b data encoding as well as the synchronization and initial lane alignment using the SYNC input signal. Optionally data from the transport layer can be scrambled.

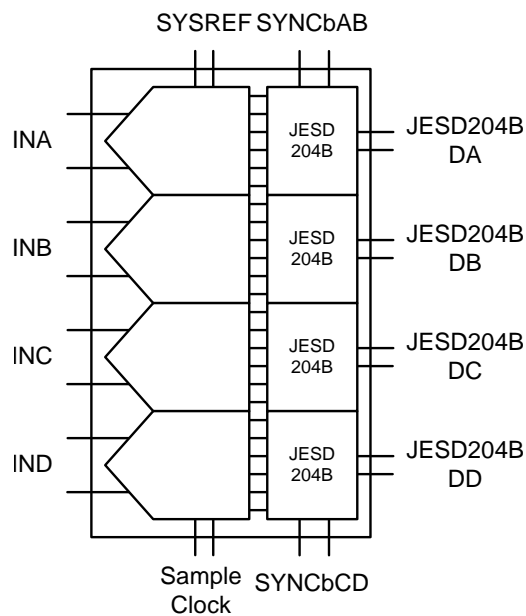


Figure 82. JESD204B Transmitter Block

7.5.2.1 JESD204B Initial Lane Alignment (ILA)

The initial lane alignment process is started by the receiving device by de-asserting the SYNCb signal. Upon detecting a logic low on the SYNC input pins, the ADS58J63 starts transmitting comma (K28.5) characters to establish code group synchronization.

Once synchronization is completed the receiving device re-asserts the SYNCb signal and the ADS58J63 starts the initial lane alignment sequence with the next local multi frame clock boundary. The ADS58J63 transmits 4 multi-frames each containing K frames (K is SPI programmable). Each of the multi-frames contains the frame start and end symbols and the 2nd multi-frame also contains the JESD204 link configuration data.

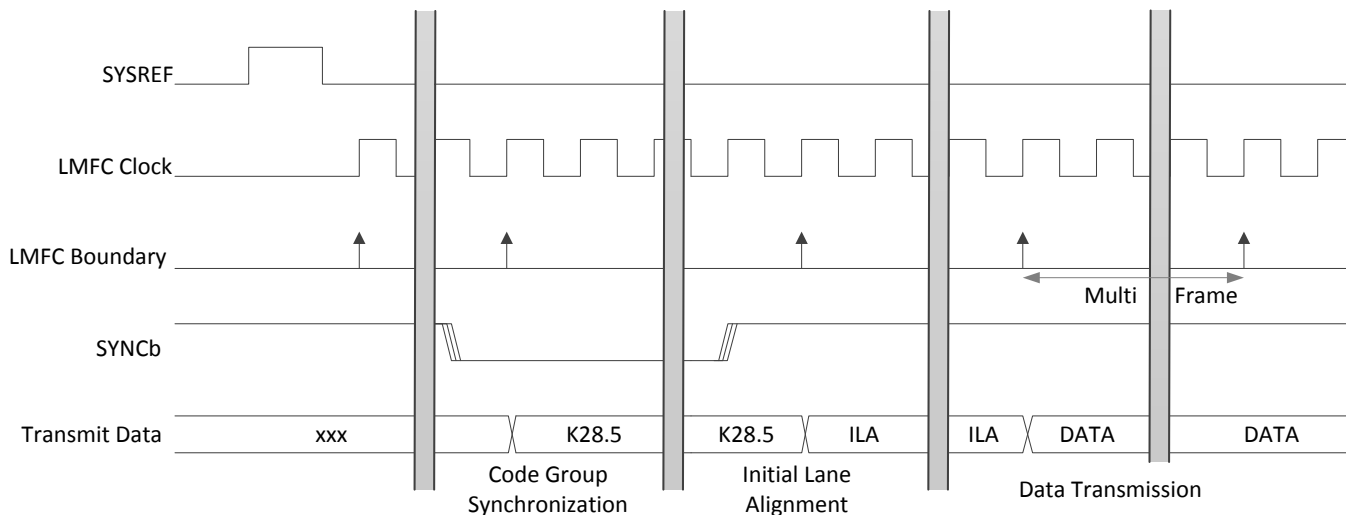


Figure 83. ILA Sequence

7.5.2.2 JESD204B Frame Assembly

The JESD204B standard defines the following parameters:

- L is the number of lanes per link.
- M is the number of converters per device.
- F is the number of octets per frame clock period.
- S is the number of samples per frame.

Table 13 lists the available JESD204B formats and valid ranges for the ADS58J63. The ranges are limited by the Serdes line rate and the maximum ADC sample frequency.

Table 13. Available JESD204B Formats and Valid Ranges for the ADS58J63

| L | M | F | S | OPERATING MODE | DIGITAL MODE | OUTPUT FORMAT | JESD MODE (69h, 01h) | JESD PLL MODE (6Ah, 01h6) | MAX ADC OUTPUT RATE (MSPS) | MAX f _{SERDES} (Gbps) |
|---|---|---|---|----------------|----------------------------|---------------|----------------------|---------------------------|----------------------------|--------------------------------|
| 4 | 8 | 4 | 1 | 0,5 | 2x Decimation | Complex | 40 x | 40 x | 250 | 10.0 |
| 4 | 4 | 2 | 1 | 2,4 | 2x Decimation | Real | 20 x | 20 x | 250 | 5.0 |
| 2 | 4 | 4 | 1 | 2,4 | 2x Decimation | Real | 40 x | 40 x | 250 | 10.0 |
| 4 | 8 | 4 | 1 | 6 | 4x Decimation | Complex | 40 x | 20 x | 125 | 5.0 |
| 2 | 8 | 8 | 1 | 6 | 4x Decimation | Complex | 80 x | 40 x | 125 | 10.0 |
| 4 | 4 | 2 | 1 | 7 | 2x Decimation with '0-Pad' | Real | 20 x | 40 x | 500 | 10.0 |
| 4 | 4 | 2 | 1 | 8 | Burst Mode | Real | 20 x | 40 x | 500 | 10.0 |

The detailed frame assembly is shown in [Table 14](#).

Table 14. Detailed Frame Assembly

| | LMFS = 4841 | | | | LMFS = 4421 | | | | LMFS = 4421 (0-Pad) | | | |
|----|-------------|----------|----------------|----------|-------------|---------|----------|---------|---------------------|---------|--------------|--------------|
| DA | A10[15:8] | A10[7:0] | AQ0[15:8]] | AQ0[7:0] | A0[15:8] | A0[7:0] | A1[15:8] | A1[7:0] | A0[15:8] | A0[7:0] | 0000 0000 | 0000 0000 |
| DB | B10[15:8] | B10[7:0] | BQ0[15:8]] | BQ0[7:0] | B0[15:8] | B0[7:0] | B1[15:8] | B1[7:0] | B0[15:8] | B0[7:0] | 0000 0000 | 0000 0000 |
| DC | C10[15:8] | C10[7:0] | CQ0[15:8]] | CQ0[7:0] | C0[15:8] | C0[7:0] | C1[15:8] | C1[7:0] | C0[15:8] | C0[7:0] | 0000 0000 | 0000 0000 |
| DD | D10[15:8] | D10[7:0] | DQ0[15:8]] | DQ0[7:0] | D0[15:8] | D0[7:0] | D1[15:8] | D1[7:0] | D0[15:8] | D0[7:0] | 0000 0000 | 0000 0000 |

| | LMFS = 2441 | | | | LMFS = 2881 | | | | | | | |
|----|-------------|---------|----------|---------|-------------|----------|-----------|----------|-----------|----------|-----------|----------|
| DB | A0[15:8] | A0[7:0] | B0[15:8] | B0[7:0] | A10[15:8] | A10[7:0] | AQ0[15:8] | AQ0[7:0] | B10[15:8] | B10[7:0] | BQ0[15:8] | BQ0[7:0] |
| DC | C0[15:8] | C0[7:0] | D0[15:8] | D0[7:0] | C10[15:8] | C10[7:0] | CQ0[15:8] | CQ0[7:0] | D10[15:8] | D10[7:0] | DQ0[15:8] | DQ0[7:0] |

7.5.2.3 JESD Output Switch

The ADS58J63 provides a digital cross point switch in the JESD204B block which allows internal routing of any output of the 2 ADCs within one channel pair to any of the 2 JESD204B serial transmitters in order to ease layout constraints. The cross point switch routing is configured via SPI (address 21h in JESD digital page).

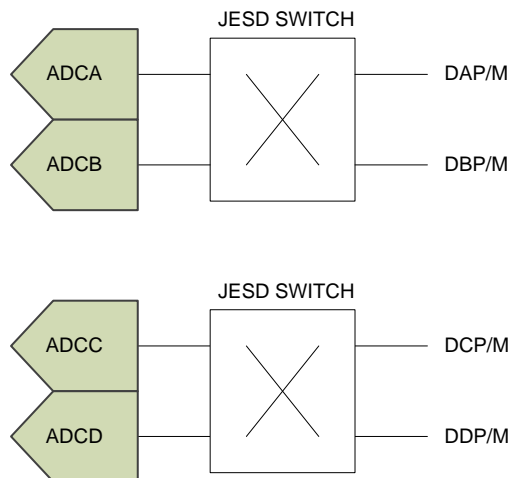


Figure 84. Switching the Output Lanes

7.5.2.3.1 Serdes Transmitter Interface

Each of the 10 Gbps serdes transmitter outputs requires AC coupling between transmitter and receiver. The differential pair should be terminated with $100\ \Omega$ as close to the receiving device as possible to avoid unwanted reflections and signal degradation.

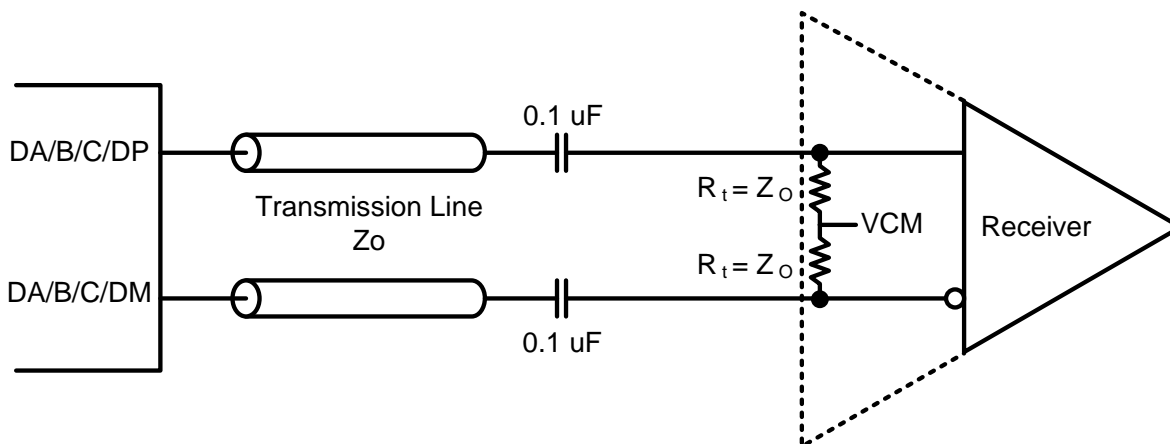


Figure 85. Serdes Transmitter Connection to Receiver

7.5.2.3.2 SYNCb Interface

The ADS58J63 supports single (either SYNCb input controls all 4 JESD204B links) or dual (1 SYNCb input controls 2 JESD204B lanes (DA/DB and DC/DD) SYNCb control. When using single SYNCb control, the unused input should be connected to differential logic low (SYNCbxxP = 0 V, SYNCbxxM = IOVDD).

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7.5.2.3.3 Eye Diagram

Figure 86 to Figure 89 show the serial output eye diagrams of the ADS58J63 at 5 Gbps and 10 Gbps with default and increased output voltage swing against the JESD204B mask.

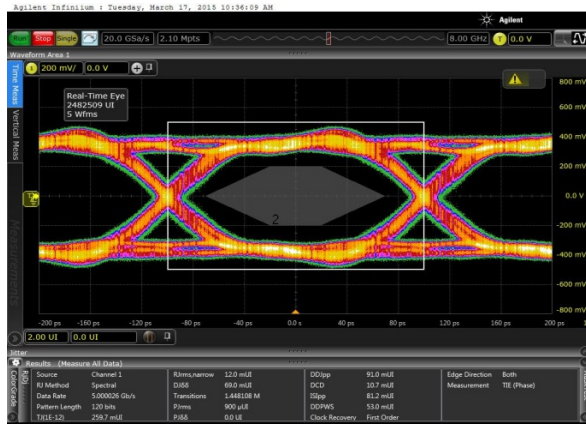


Figure 86. Eye at 5-Gbps Bit Rate with Default Output Swing



Figure 87. Eye at 5-Gbps Bit Rate with Increased Output Swing

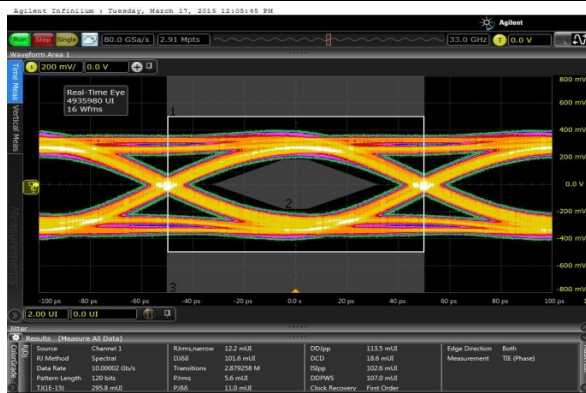


Figure 88. Eye at 10-Gbps Bit Rate with Default Output Swing

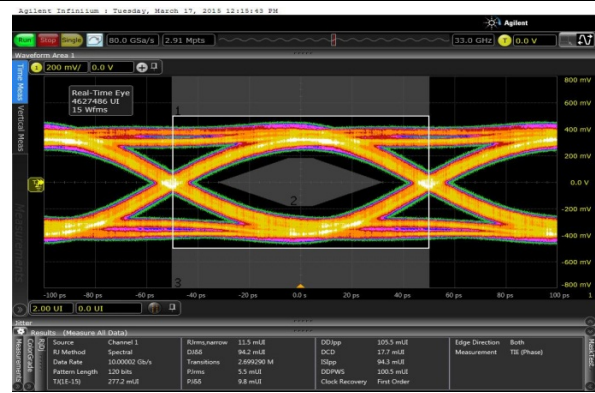


Figure 89. Eye at 10-Gbps Bit Rate with Increased Output Swing

7.6 Register Maps

The conceptual diagram of Serial Registers is shown in Figure 90.

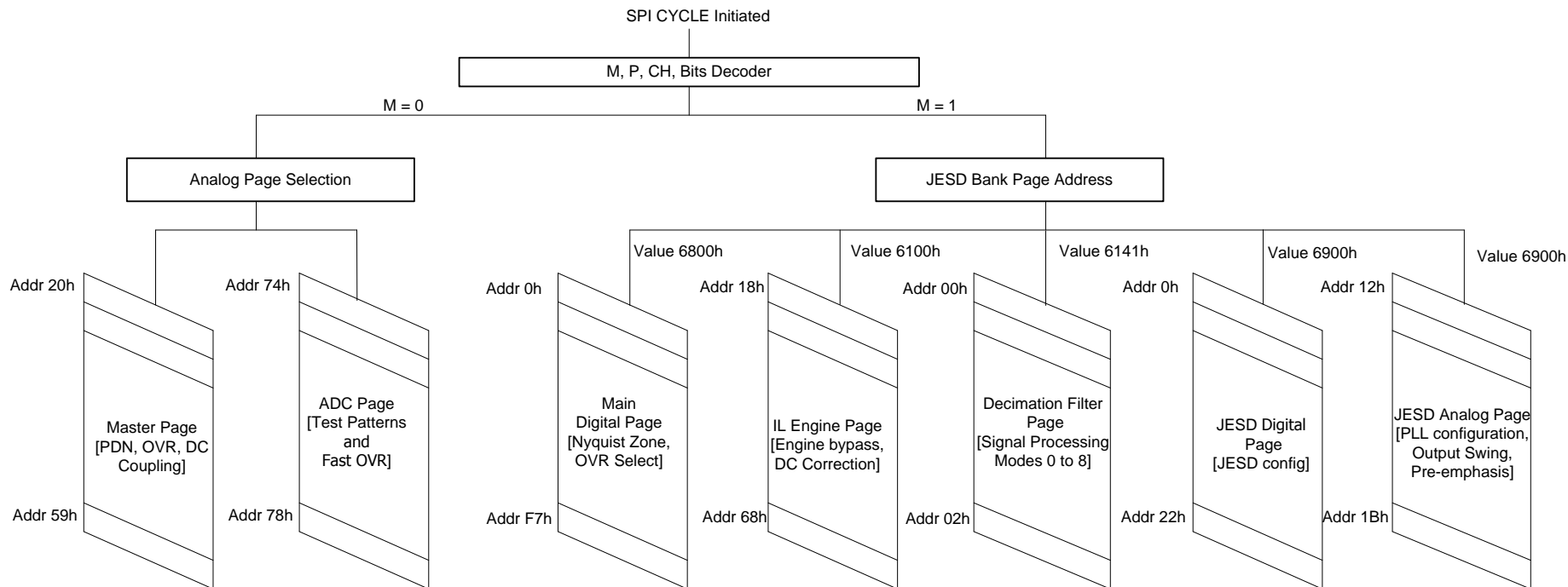


Figure 90. Serial Interface Registers

7.6.1 Detailed Register Info

The ADS58J63 contains two main SPI banks. The analog SPI bank gives access to the ADC cores while the digital SPI bank controls the serial interface. The analog SPI bank is divided into two pages (MASTER and ADC) while the digital SPI bank is divided into five pages (Main digital, Interleaving Engine, Decimation filter, JESD digital, and JESD analog).

Table 15. Register Map

| Register Address | Register Data | | | | | | | |
|------------------|---------------------------|----|----|----|----|----|----|---------------|
| A7-A0 in hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0 | RESET | 0 | 0 | 0 | 0 | 0 | 0 | RESET |
| 3 | JESD BANK PAGE SEL [7:0] | | | | | | | |
| 4 | JESD BANK PAGE SEL [15:8] | | | | | | | |
| 5 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DIS BROADCAST |

Register Maps (continued)
Table 15. Register Map (continued)

| Register Address | Register Data | | | | | | | |
|----------------------------------|-----------------------------|----------------------|-----------------|------------------|--------------------|----------------|--------------|------------------|
| A7-A0 in hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 11 | ANALOG PAGE SELECTION [7:0] | | | | | | | |
| MASTER PAGE (80h) | | | | | | | | |
| 20 | PDN ADC CHAB | | | | PDN ADC CHCD | | | |
| 21 | PDN BUFFER CHCD | | PDN BUFFER CHAB | | 0 | 0 | 0 | 0 |
| 23 | PDN ADC CHAB | | | | PDN ADC CHCD | | | |
| 24 | PDN BUFFER CHCD | | PDN BUFFER CHAB | | 0 | 0 | 0 | 0 |
| 26 | GLOBAL PDN | VERRIDE PDN PIN | PDN MASK SEL | 0 | 0 | 0 | 0 | 0 |
| 3A | 0 | BUFFER CURR INCREASE | 0 | 0 | 0 | 0 | 0 | 0 |
| 39 | ALWAYS WRITE 1 | | 0 | 0 | 0 | 0 | 0 | 0 |
| 53 | CLK DIV | MASK SYSREF | 0 | 0 | 0 | 0 | 0 | 0 |
| 55 | 0 | 0 | 0 | PDN MASK | 0 | 0 | 0 | 0 |
| 56 | 0 | 0 | 0 | 0 | INPUT BUFF CURR EN | 0 | 0 | 0 |
| 59 | 0 | 0 | ALWAYS WRITE 1 | 0 | 0 | 0 | 0 | 0 |
| ADC PAGE (0Fh) | | | | | | | | |
| 5F | FOVR CHCD THRESH | | | | | | | |
| 60 | 0 | 0 | 0 | PULSE BIT CHC | 0 | 0 | 0 | 0 |
| 61 | 0 | 0 | 0 | HD3_NYQ2_CHCD | 0 | 0 | 0 | PULSE BIT CHD |
| 6C | 0 | 0 | 0 | PULSE_BIT_CHA | 0 | 0 | 0 | 0 |
| 6D | 0 | 0 | 0 | HD3_NYQ2_CHAB | 0 | 0 | 0 | PULSE BIT CHB |
| 74 | TEST PATTERN ON CHANNEL | | | | 0 | 0 | 0 | 0 |
| 75 | CUSTOM PATTERN 1 [13:6] | | | | | | | |
| 76 | CUSTOM PATTERN 1 [5:0] | | | | | | 0 | 0 |
| 77 | CUSTOM PATTERN 2 [13:6] | | | | | | | |
| 78 | CUSTOM PATTERN 2 [5:0] | | | | | | 0 | 0 |
| INTERLEAVING ENGINE PAGE (6100h) | | | | | | | | |
| 18 | 0 | 0 | 0 | 0 | 0 | 0 | IL BYPASS | |
| 68 | 0 | 0 | 0 | 0 | 0 | DC CORR DIS | | 0 |
| DECIMATION FILTER PAGE (6141h) | | | | | | | | |
| 0 | CHB/C FINE MIX | | | | DDC MODE | | | |
| 1 | 0 | 0 | 0 | 0 | DDC MODE6 EN1 | ALWAYS WRITE 1 | CHB/C HPF EN | CHB/C COARSE MIX |
| 2 | 0 | 0 | CHA/D HPF EN | CHA/D COARSE MIX | CHA/D FINE MIX | | | |
| MAIN DIGITAL PAGE (6800h) | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | IL RESET |
| 42 | 0 | 0 | 0 | 0 | 0 | NYQUIST ZONE | | |
| 4E | CTRL NYQUIST ZONE | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| AB | 0 | 0 | 0 | 0 | 0 | 0 | 0 | OVR EN |
| AD | 0 | 0 | 0 | 0 | OVR ON LSB | | | |

Register Maps (continued)
Table 15. Register Map (continued)

| Register Address | Register Data | | | | | | | |
|---------------------------|---------------------|-----------------|--------------------|----------------------------|--------------------|-------------|--------------------|-------------|
| A7-A0 in hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| F7 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DIG RESET |
| JESD DIGITAL PAGE (6900h) | | | | | | | | |
| 0 | CTRL K | JESD MODE EN | DDC MODE6 EN2 | TESTMODE EN | 0 | LANE ALIGN | FRAME ALIGN | TX LINK DIS |
| 1 | SYNC REG | SYNC REG EN | SYNCB SEL AB/CD | 0 | DDC MODE6 EN3 | 0 | JESD MODE | |
| 2 | LINK LAYER TESTMODE | | | LINK LAYER RPAT | LMFC MASK RESET | 0 | 0 | 0 |
| 3 | FORCE LMFC COUNT | LMFC COUNT INIT | | | | | RELEASE ILANE SEQ | |
| 5 | SCRAMBLE EN | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 6 | 0 | 0 | 0 | FRAMES PER MULTI FRAME (K) | | | | |
| 17 | HIRES FLAG ON LSB | | 0 | TRIG SET AB/CD | AUTO TRIG EN | 0 | RATIO INVALID | 0 |
| 19 | 0 | 0 | 0 | 0 | LC [27:24] | | | |
| 1A | LC [23:16] | | | | | | | |
| 1B | LC [15:8] | | | | | | | |
| 1C | LC [7:0] | | | | | | | |
| 1D | 0 | 0 | 0 | 0 | HC [27:24] | | | |
| 1E | HC [23:16] | | | | | | | |
| 1F | HC [15:8] | | | | | | | |
| 20 | HC [7:0] | | | | | | | |
| 21 | OUPUT CHA MUX SEL | | OUTPUT CHB MUX SEL | | OUTPUT CHC MUX SEL | | OUTPUT CHD MUX SEL | |
| 22 | 0 | 0 | 0 | 0 | OUT CHA INV | OUT CHB INV | OUT CHC INV | OUT CHD INV |
| JESD ANALOG PAGE (6A00h) | | | | | | | | |
| 12 | SEL EMP LANE A/D | | | | | | 0 | 0 |
| 13 | SEL EMP LANE B/C | | | | | | 0 | 0 |
| 16 | 0 | 0 | 0 | 0 | 0 | 0 | JESD PLL MODE | |
| 1B | JESD SWING | | | 0 | 0 | 0 | 0 | 0 |

7.6.2 Example Register Writes

Global Power Down

| ADDRESS | DATA | COMMENT |
|---------|------|-----------------------|
| 11h | 80h | Set Master Page |
| 00h26 | 80h | Set Global Power Down |

Change decimation mode 0 (default) to mode 4 adjusting both the LMFS configuration (LMFS = 4841 to 4421) as well as serial output data rate (10 Gbps to 5 Gbps).

| ADDRESS | DATA | COMMENT |
|---------|------|--|
| 4004h | 69h | Select digital JESD page |
| 4003h | 00h | |
| 6000h | 40h | Enables JESD mode overwrite |
| 6001h | 01h | Select digital to 20x mode |
| 4004h | 6Ah | Select analog JESD page |
| 6016h | 00h | Set serdes PLL to 20x mode |
| 4004h | 61h | Select decimation filter page |
| 4003h | 41h | |
| 6000h | CCh | Select mode 4 Digital mixer for chAB set to -4 (FS/4) |
| 6002h | 0Ch | Digital mixer for chCD set to -4 (FS/4) |

7.6.3 Register Descriptions

7.6.3.1 Register 0h (offset = 0h) [reset = 0h]

Figure 91. Register 0h

| A7-A0 in Hex | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|-------|---|---|---|---|---|---|-------|
| 0 | RESET | 0 | 0 | 0 | 0 | 0 | 0 | RESET |

LEGEND: W = Write only; -n = value after reset

Table 16. Register 0h Field Description

| Bit ⁽¹⁾ | Name | Type | Reset | Description |
|--------------------|-------|------|-------|---|
| D7 | RESET | R/W | 0 | 0 = Normal operation 1 = Internal software reset, clears back to 0 |
| D0 | RESET | R/W | 0 | 0 = Normal operation 1 = Internal software reset, clears back to 0 |

(1) Both bits (D7, D0) must be set simultaneously to exercise reset

7.6.3.2 Register 3h/4h (offset = 3h/4h) [reset = 0h]

Figure 92. Register 3h/4h

| A7-A0 in Hex | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|---------------------------|---|---|---|---|---|---|---|
| 3 | JESD BANK PAGE SEL [7:0] | | | | | | | |
| 4 | JESD BANK PAGE SEL [16:8] | | | | | | | |

LEGEND: W = Write only; -n = value after reset

Table 17. Register 3h/4h Field Description

| Bit | Name | Type | Reset | Description |
|---------|--------------------|------|-------|---|
| D7 - D0 | JESD BANK PAGE SEL | R/W | 0 | Program these bits to access desired page in JESD Bank 6100h = Interleaving Engine Page selected 6141h = Decimation Filter Page Selected 6800h = Main Digital Page Selected 6900h = JESD Digital Page selected 6A00h = JESD Analog Page selected |

7.6.3.3 Register 5h (offset = 5h) [reset = 0h]

Figure 93. Register 5h

| A7-A0 in Hex | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|---|---|---|---|---|---|---|---------------|
| 5 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DIS BROADCAST |

LEGEND: W = Write only; -n = value after reset

Table 18. Register 5h Field Description

| Bit | Name | Type | Reset | Description |
|-----|---------------|------|-------|--|
| D0 | DIS BROADCAST | R/W | 0 | 0 = Normal operation. Channel A and B are programmed as a pair. Channel C and D are programmed as a pair. 1 = channel A and B can be individually programmed based on bit 'CH'. Similarly channel C and D can be individually programmed based on bit 'CH'. |

7.6.3.4 Register 11h (offset = 11h) [reset = 0h]

Figure 94. Register 11h

| A7-A0 in Hex | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|-----------------------------|---|---|---|---|---|---|---|
| 11 | ANALOG PAGE SELECTION [7:0] | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 19. Register 11h Field Descriptions

| Bit | Name | Type | Reset | Description |
|-------|-----------------------------|------|-------|---|
| D7-D0 | ANALOG PAGE SELECTION [7:0] | R/W | 0 | Register page (only one page at a time can be addressed). Master page = 80h ADC page = 0Fh The 5 digital pages (Main digital, Interleaving Engine, Analog JESD, Digital JESD, and Decimation filter) are selected via the M bit. See Serial Interface Read/Write section for more details. |

7.6.3.5 Master Page (80h)

7.6.3.5.1 Register 20h (address = 20h) [reset = 0h] , Master Page (080h)

Figure 95. Register 20h

| A7-A0 in Hex | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|--------------|---|---|---|--------------|---|---|---|
| | PDN ADC CHAB | | | | PDN ADC CHCD | | | |
| | R/W-0h | | | | R/W-0h | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 20. Registers 20h Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|--|
| 7-4 | PDN ADC CHAB | R/W | 0h | There are two power-down masks that are controlled via the PDN mask register bit in address 55h. The power-down mask 1 or mask 2 are selected via register bit 5 in address 26h. Power-down mask 1: addresses 20h and 21h. Power-down mask 2: addresses 23h and 24h. See Power-Down Mode for details. |
| 3-0 | PDN ADC CHCD | R/W | 0h | |

7.6.3.5.2 Register 21h (address = 21h) [reset = 0h] , Master Page (080h)
Figure 96. Register 21h

| A7-A0 in Hex | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|-----------------|---|-----------------|---|------|--------|--------|------|
| | PDN BUFFER CHCD | | PDN BUFFER CHAB | | 0 | 0 | 0 | 0 |
| | R/W-0h | | R/W-0h | | W-0h | R/W-0h | R/W-0h | W-0h |

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 21. Register 21h Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------|------|-------|---|
| 7-6 | PDN BUFFER CHCD | R/W | 0h | There are two power-down masks that are controlled via the PDN mask register bit in address 55h. The power-down mask 1 or mask 2 are selected via register address 26h, bit 5. Power-down mask 1: addresses 20h and 21h. Power-down mask 2: addresses 23h and 24h. See Power-Down Mode for details. |
| 5-4 | PDN BUFFER CHAB | R/W | 0h | |
| 3 | 0 | W | 0h | |
| 2-0 | 0 | W | 0h | Must write 0. |

7.6.3.5.3 Register 23h (address = 23h), Master Page (080h)
Figure 97. Register 23h

| A7-A0 in Hex | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|-----------------|---|--------|---|-----------------|--------|--------|------|
| | PDN BUFFER CHAB | | | | PDN BUFFER CHCD | | | |
| | R/W-0h | | R/W-0h | | W-0h | R/W-0h | R/W-0h | W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 22. Register 23h Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|---|
| 7-4 | PDN ADC CHAB | R/W | 0h | There are two power-down masks that are controlled via the PDN mask register bit in address 55h. The power-down mask 1 or mask 2 are selected via register bit 5 in address 26h. Power-down mask 1: addresses 20h and 21h. Power-down mask 2: addresses 23h and 24h. See Power-Down Mode for details. |
| 3-0 | PDN ADC CHCD | R/W | 0h | |

7.6.3.5.4 Register 24h (address = 24h) [reset = 0h] , Master Page (080h)
Figure 98. Register 24h

| A7-A0 in Hex | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|-----------------|---|-----------------|---|------|--------|--------|--------|
| | PDN BUFFER CHCD | | PDN BUFFER CHAB | | 0 | 0 | 0 | 0 |
| | R/W-0h | | R/W-0h | | W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 23. Register 24h Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------|------|-------|---|
| 7-6 | PDN BUFFER CHCD | R/W | 0h | There are two power-down masks that are controlled via the PDN mask register bit in address 55h. The power-down mask 1 or mask 2 are selected via register address 26h, bit 5. Power-down mask 1: addresses 20h and 21h. Power-down mask 2: addresses 23h and 24h. See Power-Down Mode for details. |
| 5-4 | PDN BUFFER CHAB | R/W | 0h | |
| 3 | 0 | W | 0h | |
| 2-0 | 0 | W | 0h | Must write 0. |

7.6.3.5.5 Register 26h (address = 26h), Master Page (080h)
Figure 99. Register 26h

| A7-A0 in Hex | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|------------|------------------|--------------|--------|--------|--------|--------|--------|
| | GLOBAL PDN | OVERRIDE PDN PIN | PDN MASK SEL | 0 | 0 | 0 | 0 | 0 |
| | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 24. Register 26h Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------------|------|-------|--|
| 7 | GLOBAL PDN | R/W | 0h | Bit 6 (OVERRIDE PDN PIN) must be set before this bit can be programmed. 0 = Normal operation 1 = Global power-down via the SPI |
| 6 | OVERRIDE PDN PIN | R/W | 0h | This bit ignores the power-down pin control. 0 = Normal operation 1 = Ignores inputs on the power-down pin |
| 5 | PDN MASK SEL | R/W | 0h | This bit selects power-down mask 1 or mask 2. 0 = Power-down mask 1 1 = Power-down mask 2 |
| 4-0 | 0 | R/W | 0h | Must write 0 |

7.6.3.5.6 Register 3Ah (address = 3Ah) [reset = 0h] , Master Page (80h)
Figure 100. Register 3Ah

| A7-A0 in Hex | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------------|---|----------------------|---|---|---|---|---|---|
| MASTER PAGE (80h) | | | | | | | | |
| 3Ah | 0 | BUFFER CURR INCREASE | 0 | 0 | 0 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 25. Register 3Ah Field Descriptions

| Bit | Name | Type | Reset | Description |
|----------|----------------------|------|-------|--|
| 7, [5-0] | 0 | W | 0h | Must write 0 |
| 6 | BUFFER CURR INCREASE | R/W | 0h | 0 = normal operation 1 = Increases AVDD3V current by 30 mA., improves HD3, helpful for second Nyquist application. Ensure that regiset bit INPUT BUF CUR EN is also set to 1. |

7.6.3.5.7 Register 39h (address = 39h) [reset = 0h] , Master Page (80h)
Figure 101. Register 39h

| A7-A0 in Hex | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------------|----------------|---|---|---|---|---|---|---|
| MASTER PAGE (80h) | | | | | | | | |
| 39h | ALWAYS WRITE 1 | | 0 | 0 | 0 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 26. Register 39h Field Descriptions

| Bit | Name | Type | Reset | Description |
|-------|----------------|------|-------|------------------------------|
| [7:5] | ALWAYS WRITE 1 | R/W | 0h | Always set these bits to 11. |
| [5-0] | 0 | W | 0h | Must write 0 |

7.6.3.5.8 Register 53h (address = 53h) [reset = 0h] , Master Page (80h)
Figure 102. Register 53h Register

| A7-A0 in Hex | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------------|---------|-------------|---|---|---|---|---|---|
| MASTER PAGE (80h) | | | | | | | | |
| 53h | CLK DIV | MASK SYSREF | 0 | 0 | 0 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write; -n = value after reset

Table 27. Register 53h Field Descriptions

| Bit | Name | Type | Reset | Description |
|-----|-------------|------|-------|---|
| 7 | CLK DIV | R/W | 0 | Configures input clock divider 0 = Divide by 4 1 = Divide by 2 (must be enabled for proper operation of ADS58J63) |
| 6 | MASK SYSREF | R/W | 0 | 0 = normal operation 1 = ignores SYSREF input |

7.6.3.5.9 Register 55h (address = 55h) [reset = 0h] , Master Page (80h)
Figure 103. Register 55h

| A7-A0 in Hex | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------------|---|---|---|----------|---|---|---|---|
| MASTER PAGE (80h) | | | | | | | | |
| 55h | 0 | 0 | 0 | PDN MASK | 0 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 28. Register 55h Field Descriptions

| Bit | Name | Type | Reset | Description |
|-----|----------|------|-------|---|
| 4 | PDN MASK | R/W | 0 | Power down via register bit 0 = normal operation 1 = power down enabled powering down internal blocks specified in the selected power down mask |

7.6.3.5.10 Register 56h (address = 56h) [reset = 0h] , Master Page (80h)
Figure 104. Register 56h

| A7-A0 in Hex | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------------|---|---|---|---|-----------------------|---|---|---|
| MASTER PAGE (80h) | | | | | | | | |
| 56h | 0 | 0 | 0 | 0 | INPUT BUFF CURR EN | 0 | 0 | 0 |

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 29. Register 56h Field Descriptions

| Bit | Name | Type | Reset | Description |
|-----|--------------------|------|-------|--|
| 3 | INPUT BUFF CURR EN | R/W | 0 | 0 = normal operation 1 = Increases AVDD3V current by 30 mA., improves HD3, helpful for second Nyquist application. Ensure that regiset bit BUFFER CURR INCREASE is also set to 1. |

7.6.3.5.11 Register 59h (address = 59h) [reset = 0h] , Master Page (80h)
Figure 105. Register 59h

| A7-A0 in Hex | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------------|---|---|-------------------|---|---|---|---|---|
| MASTER PAGE (80h) | | | | | | | | |
| 39h | 0 | 0 | ALWAYS WRITE 1 | 0 | 0 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 30. Register 59h Field Descriptions

| Bit | Name | Type | Reset | Description |
|-----|----------------|------|-------|-----------------------------|
| 5 | ALWAYS WRITE 1 | R/W | 0h | Always set these bits to 1. |

7.6.3.6 ADC Page (0Fh)

7.6.3.6.1 Register 5Fh (address = 5Fh) [reset = 0h] , ADC Page (0Fh)

Figure 106. Register 5Fh

| A7-A0 in Hex | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------------|------------------|---|---|---|---|---|---|---|
| ADC Page (0Fh) | | | | | | | | |
| 5Fh | FOVR CHCD THRESH | | | | | | | |

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 31. Register 5Fh Field Descriptions

| Bit | Name | Type | Reset | Description |
|---------|------------------|------|-------|---|
| D [7:0] | FOVR CHCD THRESH | R/W | 0h | Controls the location of FAST OVR threshold for channel C and D. Refer to Over-range Indication . |

7.6.3.6.2 Register 60h (address = 60h) [reset = 0h] , ADC Page (0Fh)

Figure 107. Register 60h

| A7-A0 in Hex | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------------|---|---|---|---------------|---|---|---|---|
| ADC Page (0Fh) | | | | | | | | |
| 60Fh | 0 | 0 | 0 | PULSE BIT CHC | 0 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 32. Register 60h Field Descriptions

| Bit | Name | Type | Reset | Description |
|-----|---------------|------|-------|---|
| 4 | PULSE BIT CHC | R/W | 0h | Pulse ⁽¹⁾ this bit to improve HD3 for 2nd Nyquist frequencies ($f_{IN} > 250$ MHz) for channel C. Before pulsing this bit, register bit HD3 NYQ2 CHCD must be set to 1. |

(1) Pulsing = Set the bit to 1 and then reset to 0.

7.6.3.6.3 Register 60h (address = 61h) [reset = 0h], ADC Page (0Fh)

Figure 108. Register 61h

| A7-A0 in Hex | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------------|---|---|---|---------------|---|---|---|---------------|
| ADC Page (0Fh) | | | | | | | | |
| 61Fh | 0 | 0 | 0 | HD3 NYQ2 CHCD | 0 | 0 | 0 | PULSE BIT CHD |

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 33. Register 61h Field Descriptions

| Bit | Name | Type | Reset | Description |
|-----|---------------|------|-------|---|
| 4 | HD3 NYQ2 CHCD | R/W | 0h | Se this bit to improve HD3 for 2nd Nyquist frequencies ($f_{IN} > 250$ MHz) for channel C and D. Once this bit is set, it is required to pulse the PULSE BIT CHx register bits to see the improvement in corresponding channels. |
| 0 | PULSE BIT CHD | R/W | 0h | Pulse ⁽¹⁾ this bit to improve HD3 for 2nd Nyquist frequencies ($f_{IN} > 250$ MHz) for channel D. Before pulsing this bit, register bit HD3 NYQ2 CHCD must be set to 1. |

(1) Pulsing = Set the bit to 1 and then reset to 0.

7.6.3.6.4 Register 6Ch (address = 6Ch) [reset = 0h], ADC Page (0Fh)
Figure 109. Register 6Ch

| A7-A0 in Hex | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------------|---|---|---|------------------|---|---|---|---|
| ADC Page (0Fh) | | | | | | | | |
| 6Ch | 0 | 0 | 0 | PULSE BIT CHA | 0 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 34. Register 6Ch Field Descriptions

| Bit | Name | Type | Reset | Description |
|-----|---------------|------|-------|---|
| 4 | PULSE BIT CHA | R/W | 0h | Pulse ⁽¹⁾ this bit to improve HD3 for 2nd Nyquist frequencies ($f_{IN} > 250$ MHz) for channel A. Before pulsing this bit, register bit HD3 NYQ2 CHCAB must be set to 1. |

(1) Pulsing = Set the bit to 1 and then reset to 0.

7.6.3.6.5 Register 6Dh (address = 6Dh) [reset = 0h], ADC Page (0Fh)
Figure 110. Register 6Dh

| A7-A0 in Hex | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------------|---|---|---|------------------|---|---|---|------------------|
| ADC Page (0Fh) | | | | | | | | |
| 6Dh | 0 | 0 | 0 | HD3 NYQ2 CHAB | 0 | 0 | 0 | PULSE BIT CHB |

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 35. Register 6Dh Field Descriptions

| Bit | Name | Type | Reset | Description |
|-----|---------------|------|-------|---|
| 4 | HD3 NYQ2 CHAB | R/W | 0h | Se this bit to improve HD3 for 2nd Nyquist frequencies ($f_{IN} > 250$ MHz) for channel A and B. Once this bit is set, it is required to pulse the PULSE BIT CHx register bits to see the improvement in corresponding channels. |
| 0 | PULSE BIT CHB | R/W | 0h | Pulse ⁽¹⁾ this bit to improve HD3 for 2nd Nyquist frequencies ($f_{IN} > 250$ MHz) for channel B. Before pulsing this bit, register bit HD3 NYQ2 CHAB must be set to 1. |

(1) Pulsing = Set the bit to 1 and then reset to 0.

7.6.3.6.6 Register 74h(address = 74h) [reset = 0h], ADC Page (0Fh)
Figure 111. Register 74h

| A7-A0 in Hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----------------------|-------------------------|----|----|----|----|----|----|----|
| ADC Page (0Fh) | | | | | | | | |
| 74 | TEST PATTERN ON CHANNEL | | | | 0 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write; -n = value after reset

Table 36. Register 74h Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------|------|-------|--|
| D7-D4 | TEST PATTERN ON CHANNEL | R/W | 0000 | Test pattern output on channel A and B 0000 Normal Operation using ADC output data 0001 Outputs all 0s 0010 Outputs all 1s 0011 Outputs toggle pattern: Output data are an alternating sequence of 101010101010 and 010101010101 0100 Output digital ramp: output data increments by one LSB every clock cycle from code 0 to 16384 0110 Single pattern: output data is custom pattern 1 (75h and 76h) 0111 Double pattern: output data alternates between custom patter 1 and custom pattern 2 1000 Deskew pattern: output data is 2AAAh 1001 SYNC pattern: output data is 3FFFh See ADC Test Pattern for more details. |

7.6.3.6.7 Register 75h/76h/77h/78h (address = 75h/76h/77h/78h) [reset = 0h], ADC Page (0Fh)
Figure 112. Register 75h/76h/77h/78h

| A7-A0 in Hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----------------------|------------------------|----|----|----|----|----|----|----|
| ADC Page (0Fh) | | | | | | | | |
| 75 | CUSTOM PATTERN 1[13:6] | | | | | | | |
| 76 | CUSTOM PATTERN 1[5:0] | | | | | | 0 | 0 |
| 77 | CUSTOM PATTERN 2[13:6] | | | | | | | |
| 78 | CUSTOM PATTERN 2[5:0] | | | | | | 0 | 0 |

LEGEND: R/78W = Read/Write; -n = value after reset

Table 37. Register 75h/76h/77h/78h Field Descriptions

| Bit | Name | Type | Reset | Description |
|-----|----------------|------|-------|--|
| 7-0 | CUSTOM PATTERN | R/W | 0 | Address 75/76/77/78 Sets the custom pattern (13:6, 5:0) for all channels. See ADC Test Pattern for more details. |

7.6.3.7 Interleaving Engine Page (6100h)

7.6.3.7.1 Register 18h (address = 18h) [reset = 0h], Interleaving Engine Page (6100h)

Figure 113. Register 18h

| A7-A0 in hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|----|----|----|----|----|----|----|-----------|
| INTERLEAVING ENGINE PAGE (6100h) | | | | | | | | |
| 18 | 0 | 0 | 0 | 0 | 0 | 0 | | IL BYPASS |

LEGEND: R/W = Read/Write; -n = value after reset

Table 38. Register 18h Field Descriptions

| Bit | Name | Type | Reset | Description |
|-------|-----------|------|-------|--|
| D1-D0 | IL BYPASS | R/W | 00 | Allows bypassing of the interleaving correction. To be used when ADC test patterns are enabled. 00 = interleaving correction enabled 11 = interleaving correction bypassed |

7.6.3.7.2 Register 68h (address = 68h) [reset = 0h], Interleaving Engine Page (6100h)

Figure 114. Register 68h

| A7-A0 in hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|----|----|----|----|----|----|-------------|----|
| INTERLEAVING ENGINE PAGE (6100h) | | | | | | | | |
| 68 | 0 | 0 | 0 | 0 | 0 | | DC CORR DIS | 0 |

LEGEND: R/W = Read/Write; -n = value after reset

Table 39. Register 68h Field Descriptions

| Bit | Name | Type | Reset | Description |
|-----|-------------|------|-------|--|
| D2 | DC CORR DIS | R/W | 0 | Enables DC offset correction loop. 00 = DC offset correction enabled 11 = DC offset correction disabled Others = Do not use |

7.6.3.8 Decimation Filter Page (6141h) Registers

7.6.3.8.1 Register 0h (address = 0h) [reset = 0h]

Figure 115. Register 0h

| A7-A0 in hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---------------------------------------|----------------|----|----|----------|----|----|----|----|
| DECIMATION FILTER PAGE (6141h) | | | | | | | | |
| 0 | CHB/C FINE MIX | | | DDC MODE | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 40. 0h Field Descriptions

| Bit | Field | Type | Reset | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------|----------------|--|-------|--|---------|------|-------------|-----|---|---|-----|---|-----|-----|---|---|-----|---|-----|-----|---|---|-----|---|--|-----|---|--|-----|---|---|------|---|-----------------------------|--------|---|------------|
| D7-D4 | CHB/C FINE MIX | R/W | 0000 | Selects fine mixing frequency for $N \times f_s/16$ mixer where N is a 2's complement number varyinig from -8 to 7. 0000 = N is 0 0001 = N is 1 0010 = N is 2 ... 0111 = N is 7 1000 = N is -8 ... 1111 = N is -1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D3-D0 | DDC MODE | R/W | 0h | Selects the DDC Mode for all channels | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | <table border="1"> <thead> <tr> <th>SETTING</th> <th>MODE</th> <th>DESCRIPTION</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>0</td> <td>$f_s/4$ mixing with decimation by 2, complex output</td> </tr> <tr> <td>001</td> <td>–</td> <td>N/A</td> </tr> <tr> <td>010</td> <td>2</td> <td>Decimation by 2, high or low pass filter, real output</td> </tr> <tr> <td>011</td> <td>–</td> <td>N/A</td> </tr> <tr> <td>100</td> <td>4</td> <td>Decimation by 2, $N \times f_s/16$ mixer, real output</td> </tr> <tr> <td>101</td> <td>5</td> <td>Decimation by 2, $N \times f_s/16$ mixer, complex output</td> </tr> <tr> <td>110</td> <td>6</td> <td>Decimation by 4, $N \times f_s/16$ mixer, complex output. Ensure that register bits DDC MODE 6 EN [3:1] are also set to '111'.</td> </tr> <tr> <td>111</td> <td>7</td> <td>Decimation by 2, $N \times f_s/16$ mixer, insert 0, real output</td> </tr> <tr> <td>1000</td> <td>8</td> <td>14-bit burst mode selected.</td> </tr> <tr> <td>Others</td> <td>–</td> <td>Do not use</td> </tr> </tbody> </table> | SETTING | MODE | DESCRIPTION | 000 | 0 | $f_s/4$ mixing with decimation by 2, complex output | 001 | – | N/A | 010 | 2 | Decimation by 2, high or low pass filter, real output | 011 | – | N/A | 100 | 4 | Decimation by 2, $N \times f_s/16$ mixer, real output | 101 | 5 | Decimation by 2, $N \times f_s/16$ mixer, complex output | 110 | 6 | Decimation by 4, $N \times f_s/16$ mixer, complex output. Ensure that register bits DDC MODE 6 EN [3:1] are also set to '111'. | 111 | 7 | Decimation by 2, $N \times f_s/16$ mixer, insert 0, real output | 1000 | 8 | 14-bit burst mode selected. | Others | – | Do not use |
| SETTING | MODE | DESCRIPTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 000 | 0 | $f_s/4$ mixing with decimation by 2, complex output | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 001 | – | N/A | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 010 | 2 | Decimation by 2, high or low pass filter, real output | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 011 | – | N/A | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 100 | 4 | Decimation by 2, $N \times f_s/16$ mixer, real output | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 101 | 5 | Decimation by 2, $N \times f_s/16$ mixer, complex output | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 110 | 6 | Decimation by 4, $N \times f_s/16$ mixer, complex output. Ensure that register bits DDC MODE 6 EN [3:1] are also set to '111'. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 111 | 7 | Decimation by 2, $N \times f_s/16$ mixer, insert 0, real output | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1000 | 8 | 14-bit burst mode selected. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Others | – | Do not use | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

7.6.3.8.2 Register 1h (address = 1h) [reset = 0h]
Figure 116. Register 1h

| A7-A0 in hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---------------------------------------|----|----|----|----|---------------|----------------|--------------|------------------|
| DECIMATION FILTER PAGE (6141h) | | | | | | | | |
| 1 | 0 | 0 | 0 | 0 | DDC MODE6 EN1 | ALWAYS WRITE 1 | CHB/C HPF EN | CHB/C COARSE MIX |

LEGEND: R/W = Read/Write; -n = value after reset

Table 41. Register 1h Field Descriptions

| Bit | Name | Type | Reset | Description |
|-------|------------------|------|-------|---|
| D7-D4 | 0 | W | 0 | |
| D3 | DDC MODE6 EN1 | R/W | 0 | Set this bit along with register bits DDC MODE6 EN2 and DDC MODE6 EN3 for proper operation of Mode 6. 0 = Default 1 = Use for proper operation of DDC Mode 6. |
| D2 | ALWAYS WRITE 1 | R/W | 0 | Always write this bit to 1. |
| D1 | CHB/C HPF EN | R/W | 0 | Enables high pass filter for DDC Mode 2 for channel B and C. 0 = Low pass filter enabled 1 = High pass filter enabled |
| D0 | CHB/C COARSE MIX | R/W | 0 | Selects $f_s/4$ mixer phase for DDC Mode 0 for channel B and C. 0 = Mix with $+f_s/4$ 1 = Mix with $-f_s/4$ |

7.6.3.8.3 Register 2h (address = 2h) [reset = 0h]
Figure 117. Register 2h

| A7-A0 in hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---------------------------------------|----|----|--------------|------------------|----|----------------|----|----|
| DECIMATION FILTER PAGE (6141h) | | | | | | | | |
| 2 | 0 | 0 | CHA/D HPF EN | CHA/D COARSE MIX | | CHA/D FINE MIX | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 42. 2h Field Descriptions

| Bit | Name | Type | Reset | Description |
|-------|------------------|------|-------|---|
| D7-D6 | 0 | | | |
| D5 | CHA/D HPF EN | R/W | 0 | Enables high pass filter for DDC Mode 2 for channel A and D. 0 = Low pass filter enabled 1 = High pass filter enabled |
| D4 | CHA/D COARSE MIX | R/W | 0 | Selects $f_s/4$ mixer phase for DDC Mode 0 for channel A and D. 0 = Mix with $+f_s/4$ 1 = Mix with $-f_s/4$ |
| D3-D0 | CHA/D FINE MIX | R/W | 0000 | Selects fine mixing frequency for $N \times f_s/16$ mixer where N is a 2's complement number varyinig from -8 to 7. 0000 = N is 0 0001 = N is 1 0010 = N is 2 ... 0111 = N is 7 1000 = N is -8 ... 1111 = N is -1 |

7.6.3.9 Main Digital Page (6800h) Registers

7.6.3.9.1 Register 0h (address = 0h) [reset = 0h], Main Digital Page (6800h)

Figure 118. Register 0h

| A7-A0 in hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------------------------------|----|----|----|----|----|----|----|----------|
| MAIN DIGITAL PAGE (6800h) | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | IL RESET |

LEGEND: R/W = Read/Write; -n = value after reset

Table 43. Register 0h Field Descriptions

| Bit | Name | Type | Reset | Description |
|-----|----------|------|-------|---|
| D0 | IL RESET | R/W | 0 | Resets the interleaving engine. This bit is not a self-clearing bit and must be pulsed ⁽¹⁾ . Any register bit in Main Digital Page (6800h) takes effect only after this bit is pulsed. Also, note that pulsing this bit clears registers in interleaving page (6100h). 0 = normal operation 0 → 1 → 0 = interleaving engine reset. |

(1) Pulsing = Set the bit to 1 and then reset to 0.

7.6.3.9.2 Register 42h (address = 42h) [reset = 0h], Main Digital Page (6800h)

Figure 119. Register 42h

| A7-A0 in hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------------------------------|----|----|----|----|----|----|----|--------------|
| MAIN DIGITAL PAGE (6800h) | | | | | | | | |
| 42 | 0 | 0 | 0 | 0 | 0 | | | NYQUIST ZONE |

LEGEND: R/W = Read/Write; -n = value after reset

Table 44. Register 42h Field Descriptions

| Bit | Name | Type | Reset | Description |
|-------|--------------|------|-------|---|
| D2-D0 | NYQUIST ZONE | R/W | 000 | Provide Nyquist zone information to IL engine. Ensure that register bit CTRL NYQUIST is set to 1. 000 = 1 st Nyquist zone (input frequencies between 0 to $f_s/2$) 001 = 2 nd Nyquist zone (input frequencies between $f_s/2$ to f_s) 010 = 3 rd Nyquist zone (input frequencies between f_s to $3f_s/2$) ... 111 = 8 th Nyquist zone (input frequencies between $7f_s/2$ to $4f_s$) |

7.6.3.9.3 Register 4Eh (address = 4Eh) [reset = 0h], Main Digital Page (6800h)

Figure 120. Register 4Eh

| A7-A0 in hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------------------------------|--------------|----|----|----|----|----|----|----|
| MAIN DIGITAL PAGE (6800h) | | | | | | | | |
| 4E | CTRL NYQUIST | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write; -n = value after reset

Table 45. Register 4Eh Field Descriptions

| Bit | Name | Type | Reset | Description |
|-----|--------------|------|-------|---|
| D7 | CTRL NYQUIST | R/W | 0 | Enables Nyquist zone control using register bits NYQUIST ZONE. 0 = Selection disabled 1 = Selection enabled |

7.6.3.9.4 Register ABh (address = ABh) [reset = 0h], Main Digital Page (6800h)
Figure 121. Register ABh

| A7-A0 in hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------------------|----|----|----|----|----|----|----|--------|
| MAIN DIGITAL PAGE (68h) | | | | | | | | |
| AB | 0 | 0 | 0 | 0 | 0 | 0 | 0 | OVR EN |

LEGEND: R/W = Read/Write; -n = value after reset

Table 46. Register ABh Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------|------|-------|---|
| D0 | OVR EN | R/W | 0 | Set this bit to enable register bit OVR ON LSB. 0 = normal operation 1 = OVR ON LSB enabled |

7.6.3.9.5 Register ADh (address = ADh) [reset = 0h], Main Digital Page (6800h)
Figure 122. Register ADh

| A7-A0 in hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------------------|----|----|----|----|----|----|----|------------|
| MAIN DIGITAL PAGE (68h) | | | | | | | | |
| AD | 0 | 0 | 0 | 0 | | | | OVR ON LSB |

LEGEND: R/W = Read/Write; -n = value after reset

Table 47. Register ADh Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------|------|-------|--|
| D0 | OVR EN | R/W | 0 | Set this bit to bring OVR on two LSBs of 16-bit output. Ensure that register bit OVR EN is set to 1 0000 = Bits D0 and D1 of 16-bit data are noise bits 0011 = OVR comes on bit D0 of 16-bit data 1100 = OVR comes on bit D1 of 16-bit data 1111 = OVR comes on both D0 and D1 bits of 16-bit data |

7.6.3.9.6 Register F7h (address = F7h) [reset = 0h], Main Digital Page (68h)
Figure 123. Register F7h

| A7-A0 in hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------------------|----|----|----|----|----|----|----|-----------|
| MAIN DIGITAL PAGE (68h) | | | | | | | | |
| F7 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DIG RESET |

LEGEND: R/W = Read/Write; -n = value after reset

Table 48. Register F7h Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------|------|-------|---|
| D0 | DIG RESET | R/W | 0 | Self clearing reset for the digital block. Does not include the interleaving correction. 0 = normal operation 1 = digital reset |

7.6.3.10 JESD Digital Page (6900h) Registers

7.6.3.10.1 Register 0h (address = 0h) [reset = 0h], JESD Digital Page (6900h)

Figure 124. Register 0h

| A7-A0 in hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------------------------------|--------|--------------|---------------|-------------|----|------------|-------------|-------------|
| JESD DIGITAL PAGE (6900h) | | | | | | | | |
| 0 | CTRL K | JESD MODE EN | DDC MODE6 EN2 | TESTMODE EN | 0 | LANE ALIGN | FRAME ALIGN | TX LINK DIS |

LEGEND: R/W = Read/Write; -n = value after reset

Table 49. Register 0h Field Descriptions

| Bit | Name | Type | Reset | Description |
|-----|---------------|------|-------|---|
| D7 | CTRL K | R/W | 0 | Enable bit for a number of frames per multi frame. 0 = Default is 5 frames per multi frame 1 = Frames per multi frame can be set in register 06h |
| D6 | JESD MODE EN | R/W | 0 | Allows changing the JESD MODE setting in register 01h (D1-D0) 0 = Disabled 1 = Enables changing the JESD MODE setting |
| D5 | DDC MODE6 EN2 | R/W | 0 | Set this bit along with register bits DDC MODE6 EN1 and DDC MODE6 EN3 for proper operation of Mode 6. 0 = Default 1 = Use for proper operation of DDC Mode 6. |
| D4 | TESTMODE EN | R/W | 0 | This bit generates the long transport layer test pattern mode, as per section 5.1.6.3 of the JESD204B specification. 0 = Test mode disabled 1 = Test mode enabled |
| D2 | LANE ALIGN | R/W | 0 | This bit inserts the lane alignment character (K28.3) for the receiver to align to lane boundary, as per section 5.3.3.5 of the JESD204B specification. 0 = Normal operation 1 = Inserts lane alignment characters |
| D1 | FRAME ALIGN | R/W | 0 | This bit inserts the lane alignment character (K28.7) for the receiver to align to lane boundary, as per section 5.3.3.5 of the JESD204B specification. 0 = Normal operation 1 = Inserts frame alignment characters |
| D0 | TX LINK DIS | R/W | 0 | This bit disables sending the initial link alignment (ILA) sequence when SYNC is de-asserted. 0 = Normal operation 1 = ILA disabled |

7.6.3.10.2 Register 1h (address = 1h) [reset = 0h], JESD Digital Page (6900h)

Figure 125. Register 1h

| A7-A0 in hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------------------------------|----------|-------------|-----------------|----|---------------|----|-----------|----|
| JESD DIGITAL PAGE (6900h) | | | | | | | | |
| 1 | SYNC REG | SYNC REG EN | SYNCB SEL AB/CD | 0 | DDC MODE6 EN3 | 0 | JESD MODE | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 50. Register 1h Field Descriptions

| Bit | Name | Type | Reset | Description |
|-------|-----------------|------|-------|--|
| D7 | SYNC REG | R/W | 0 | SYNC Register (Bit D6 must be enabled) 0 = Normal operation 1 = ADC output data are replaced with K28.5 characters. |
| D6 | SYNC REG EN | R/W | 0 | Enables bit for SYNC operation 0 = Normal operation 1 = ADC output data over-write enabled |
| D5 | SYNCB SEL AB/CD | R/W | 0 | Selects which SYNCb input controls the JESD interface. Needs to be configured for chAB and chCD 0 = SYLNCbAB 1 = SYNCbCD |
| D5 | DDC MODE6 EN3 | R/W | 0 | Set this bit along with register bits DDC MODE6 EN1 and DDC MODE6 EN2 for proper operation of Mode 6. 0 = Default 1 = Use for proper operation of DDC Mode 6. |
| D1-D0 | JESD MODE | R/W | 0 | Selects number of serial JESD output lanes per ADC. Also need to set the JESD MODE EN (00h) and JESD PLL MODE register (JESD ANALOG page, register 16h) accordingly. 01 = 20x mode 10 = 40x mode 11 = 80x mode All others = Not used |

7.6.3.10.3 Register 2h (address = 2h) [reset = 0h], JESD Digital Page (6900h)

Figure 126. Register 2h

| A7-A0 in hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------------------------------|---------------------|----|----|-----------------|-----------------|----|----|----|
| JESD DIGITAL PAGE (6900h) | | | | | | | | |
| 2 | LINK LAYER TESTMODE | | | LINK LAYER RPAT | LMFC MASK RESET | 0 | 0 | 0 |

LEGEND: R/W = Read/Write; -n = value after reset

Table 51. Register 2h Field Descriptions

| Bit | Name | Type | Reset | Description |
|-------|---------------------|------|-------|--|
| D7-D5 | LINK LAYER TESTMODE | R/W | 000 | These bits generate a pattern according to clause 5.3.3.8.2 of the JESD204B document. 000 = Normal ADC data 001 = D21.5 (high-frequency jitter pattern) 010 = K28.5 (mixed-frequency jitter pattern) 011 = Repeat initial lane alignment (generates a K28.5 character and continuously repeats lane alignment sequences) 100 = 12 octet RPAT jitter pattern |
| D4 | LINK LAYER RPAT | R/W | 0 | This bit changes the running disparity in the modified RPAT pattern test mode (only when the link layer test mode = 100). 0 = Normal operation 1 = Changes disparity |
| D3 | LMFC MASK RESET | R/W | 0 | 0 = Default 1 = Resets LMFC mask |

7.6.3.10.4 Register 3h (address = 3h) [reset = 0h], JESD Digital Page (6900h)
Figure 127. Register 3h

| A7-A0 in hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|--------------------------------|------------------|----|-----------------|----|----|----|-------------------|----|
| JESD DIGITAL PAGE (69h) | | | | | | | | |
| 3 | FORCE LMFC COUNT | | LMFC COUNT INIT | | | | RELEASE ILANE SEQ | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 52. 3h Field Descriptions

| Bit | Name | Type | Reset | Description |
|-------|-------------------|------|-------|---|
| D7 | FORCE LMFC COUNT | R/W | 0 | Force LMFC count. 0 = Normal operation 1 = Enables using a different starting value for the LMFC counter |
| D6-D2 | LMFC COUNT INIT | R/W | 00000 | SYSREF coming to the digital block will reset the LMFC count to 0 and K28.5 will stop coming when the LMFC count reaches 31. The initial value to which LMFC count resets to can be set using LMFC COUNT INIT. This way the Rx can get synchronized early since it will get the LANE ALIGNMENT SEQUENCE early. Register bit FORCE LMFC COUNT must be enabled. |
| D1-D0 | RELEASE ILANE SEQ | R/W | 00 | Delays the generation of lane alignment sequence by 0, 1, 2, or 3 multi frames after code group synchronization. 00 = 0 01 = 1 10 = 2 11 = 3 |

7.6.3.10.5 Register 5h (address = 5h) [reset = 0h], JESD Digital Page (6900h)
Figure 128. Register 5h

| A7-A0 in hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|--------------------------------|-------------|----|----|----|----|----|----|----|
| JESD DIGITAL PAGE (69h) | | | | | | | | |
| 5h | SCRAMBLE EN | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write; -n = value after reset

Table 53. 5h Field Descriptions

| Bit | Name | Type | Reset | Description |
|-----|-------------|------|-------|---|
| D7 | SCRAMBLE EN | R/W | | Scramble enable bit in the JESD204B interface. 0 = Scrambling disabled 1 = Scrambling enabled |

7.6.3.10.6 Register 6h (address = 6h) [reset = 0h], JESD Digital Page (6900h)
Figure 129. Register 6h

| A7-A0 in hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|--------------------------------|----|----|----|----------------------------|----|----|----|----|
| JESD DIGITAL PAGE (69h) | | | | | | | | |
| 6 | 0 | 0 | 0 | FRAMES PER MULTI FRAME (K) | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 54. 6h Field Descriptions

| Bit | Name | Type | Reset | Description |
|-------|----------------------------|------|-------|--|
| D7-D5 | | | | |
| D4-D0 | FRAMES PER MULTI FRAME (K) | R/W | 00000 | set the number of multi frames. Actual K is the value in hex + 1 (that is, 0Fh is K = 16). |

7.6.3.10.7 Register 17h (address = 17h) [reset = 0h], JESD Digital Page (6900h)
Figure 130. Register 17h

| A7-A0 in hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|--------------------------------|-------------------|----|----|----------------|--------------|----|---------------|----|
| JESD DIGITAL PAGE (69h) | | | | | | | | |
| 17 | HIRES FLAG ON LSB | | 0 | TRIG SET AB/CD | AUTO TRIG EN | 0 | RATIO INVALID | 0 |

LEGEND: R/W = Read/Write; -n = value after reset

Table 55. 17h Field Descriptions

| Bit | Name | Type | Reset | Description |
|---------|-------------------|------|-------|---|
| D7 - D6 | HIRES FLAG ON LSB | R/W | 0 | Applicable only in 14-bit Burst mode. Program two LSBs of 16-bit data as flag for 14-bit high resolution samples. Flag is '1' when the sample belongs to 14-bit resolution. 00 = LSB Bits D0 and D1 of 16-bit data noise bits. 01 = Bit D0 carries high-resolution flag. 10 = Bit D1 carries high-resolution flag. 11 = Both bits D0 and D1 carry high-resolution flag. |
| D4 | TRIG SET AB/CD | R/W | 0 | Determines if triggerAB or triggerCD pin is used for burst mode. Needs to be configured individually for chAB and chCD with paging. 0 = uses TRIGGERAB pin 1 = uses TRIGGERCD pin |
| D3 | AUTO TRIG EN | R/W | 0 | Enables automatic trigger in burst mode (ignores TRIGGERAB/CD inputs) 0 = auto trigger disabled 1 = auto trigger enabled |
| D1 | RATIO INVALID | R/W | 0 | Alarm flag when duty cycle ratio between high and low resolution counter is set incorrectly. |

7.6.3.10.8 Register 19h/1Ah/1Bh/1Ch (address = 19h/1Ah/1Bh/1Ch) [reset = 0h], JESD Digital Page (6900h)
Figure 131. Register 19h/1Ah/1Bh/1Ch

| A7-A0 in hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|--------------------------------|----|----|----|----|-----------|-----------|----|----|
| JESD DIGITAL PAGE (69h) | | | | | | | | |
| 19 | 0 | 0 | 0 | 0 | | LC[27:24] | | |
| 1A | | | | | LC[23:16] | | | |
| 1B | | | | | LC[15:8] | | | |
| 1C | | | | | LC[7:0] | | | |

Table 56. 19h/1Ah/1Bh/1Ch Field Descriptions

| Bit | Name | Type | Reset | Description |
|-------|------------|------|-------|--|
| D7-D0 | LC [xx:xx] | R/W | 0 | Sets the low resolution counter value. While programming LC[27:0], first program LC[7:0], then LC[15:8], then LC[23:16], and then LC[27:24] in the same order. |

7.6.3.10.8.1 Register 1Dh/1Eh/1Fh/20h (address = 1Dh/1Eh/1Fh/20h) [reset = 0h], JESD Digital Page (6900h)
Figure 132. Register 1Dh/1Eh/1Fh/20h

| A7-A0 in hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|--------------------------------|----|----|----|----|-----------|-----------|----|----|
| JESD DIGITAL PAGE (69h) | | | | | | | | |
| 1D | 0 | 0 | 0 | 0 | | HC[27:24] | | |
| 1E | | | | | HC[23:16] | | | |
| 1F | | | | | HC[15:8] | | | |
| 20 | | | | | HC[7:0] | | | |

Table 57. 1Dh/1Eh/1Fh/20h Field Descriptions

| Bit | Name | Type | Reset | Description |
|-------|------------|------|-------|---|
| D7-D0 | HC [xx:xx] | R/W | 0 | Sets the high resolution counter value. While programming HC[27:0], first program HC[7:0], then HC[15:8], then HC[23:16], and then HC[27:24] in the same order. |

7.6.3.10.8.2 Register 21h (address = 21h) [reset = 0h], JESD Digital Page (6900h)
Figure 133. Register 21h

| A7-A0 in hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|--------------------------------|--------------------|----|--------------------|----|--------------------|----|--------------------|----|
| JESD DIGITAL PAGE (69h) | | | | | | | | |
| 21 | OUTPUT CHA MUX SEL | | OUTPUT CHB MUX SEL | | OUTPUT CHC MUX SEL | | OUTPUT CHD MUX SEL | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 58. 21h Field Descriptions

| Bit | Name | Type | Reset | Description |
|-------|--------------------|------|-------|---|
| D7-D6 | OUTPUT CHA MUX SEL | R/W | 00 | Serdes lane swap with chB 00 = ChA is output on lane DA 10 = ChA is output on lane DB 01/11 = Do not use |
| D5-D4 | OUTPUT CHB MUX SEL | R/W | 00 | Serdes lane swap with chA 00 = ChB is output on lane DB 10 = ChB is output on lane DA 01/11 = Do not use |
| D3-D2 | OUTPUT CHC MUX SEL | R/W | 00 | Serdes lane swap with chD 00 = ChC is output on lane DC 10 = ChC is output on lane DD 01/11 = Do not use |
| D1-D0 | OUTPUT CHD MUX SEL | R/W | 00 | Serdes lane swap with chC 00 = ChD is output on lane DD 10 = ChD is output on lane DC 01/11 = Do not use |

7.6.3.10.8.3 Register 22h (address = 22h) [reset = 0h], JESD Digital Page (6900h)
Figure 134. Register 22h

| A7-A0 in hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------------------------------|----|----|----|----|----------------|----------------|----------------|-------------|
| JESD DIGITAL PAGE (6900h) | | | | | | | | |
| 22 | 0 | 0 | 0 | 0 | OUT CHA INV | OUT CHB INV | OUT CHC INV | OUT CHD INV |

LEGEND: R/W = Read/Write; -n = value after reset

Table 59. 22h Field Descriptions

| Bit | Name | Type | Reset | Description |
|-------|-------------|------|-------|--|
| D7-D4 | | | 0 | |
| D3 | OUT CHA INV | R/W | 0 | Polarity inversion of JESD output of chA 0 = normal operation 1 = output polarity inverted |
| D2 | OUT CHB INV | R/W | 0 | Polarity inversion of JESD output of chB 0 = normal operation 1 = output polarity inverted |
| D1 | OUT CHC INV | R/W | 0 | Polarity inversion of JESD output of chC 0 = normal operation 1 = output polarity inverted |
| D0 | OUT CHD INV | R/W | 0 | Polarity inversion of JESD output of chD 0 = normal operation 1 = output polarity inverted |

7.6.3.11 JESD Analog Page (6A00h) Register
7.6.3.11.1 Register 12h/13h (address 12h/13h) [reset = 0h], JESD Analog Page (6Ah)
Figure 135. Register 12h/13h

| A7-A0 in hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---------------------------------|----|----|--------------------|----|----|----|----|----|
| JESD ANALOG PAGE (6A00h) | | | | | | | | |
| 12 | | | SEL EMP LANE DA/DD | | | | 0 | 0 |
| 13 | | | SEL EMP LANE DB/DC | | | | 0 | 0 |

LEGEND: R/W = Read/Write; -n = value after reset

Table 60. 12h/13h Field Descriptions

| Bit | Name | Type | Reset | Description |
|-------|--|------|--------|---|
| D7-D2 | SEL EMP LANE DA/DD SEL EMP LANE DB/DC | R/W | 000000 | Selects the amount of de-emphasis for the JESD output transmitter. The de-emphasis value in dB is measured as the ratio between the peak value after the signal transition to the settled value of the voltage in one bit period. 0 = 0 dB 1 = -1 dB 3 = -2 dB 7 = -4.1 dB 15 = -6.2 dB 31 = -8.2 dB 63 = -11.5 dB |

7.6.3.11.2 16h (address = 16h) [reset = 0h], JESD Analog Page (6A00h)
Figure 136. Register 16h

| A7-A0 in hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---------------------------------|----|----|----|----|----|----|----|---------------|
| JESD ANALOG PAGE (6A00h) | | | | | | | | |
| 16 | 0 | 0 | 0 | 0 | 0 | 0 | | JESD PLL MODE |

LEGEND: R/W = Read/Write; -n = value after reset

Table 61. 16h Field Descriptions

| Bit | Name | Type | Reset | Description |
|-------|---------------|------|-------|--|
| D7-D1 | | | | |
| D0 | JESD PLL MODE | R/W | 0 | Selects the JESD PLL multiplication factor 0 = 20x mode 1 = 40x mode |

7.6.3.11.3 Register 1Bh (address = 1Bh) [reset = 0h], JESD Analog Page (6Ah)
Figure 137. Register 1Bh

| A7-A0 in hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------------------------|----|------------|----|----|----|----|----|----|
| JESD ANALOG PAGE (6Ah) | | | | | | | | |
| 1B | | JESD SWING | | 0 | 0 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write; -n = value after reset

Table 62. 1Bh Field Descriptions

| Bit | Name | Type | Reset | Description |
|-------|------------|------|-------|--|
| D7-D5 | JESD SWING | R/W | 000 | Programs SERDES output swing 0 = 860 mVPP 1 = 810 mVPP 2 = 770 mVPP 3 = 745 mVPP 4 = 960 mVPP 5 = 930 mVPP 6 = 905 mVPP 7 = 880 mVPP |
| D4-D3 | 0 | | | |

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Start-Up Sequence

The following steps are recommended as the power up sequence with the ADS58J63 in 2x complex decimation mode (DDC Mode 0) with LMFS = 4841 (shown in [Table 63](#)).

Table 63. Recommended Power-Up Sequence

| STEP | DESCRIPTION | REGISTER ADDRESS | REGISTER DATA | COMMENT |
|------|--|--|--|---|
| 1 | Supply all supply voltages. There is no required power supply sequence for the 1.15-V supply, 1.9-V supply and 3-V supply, and these may be supplied in any order. | — | — | — |
| 2 | Pulse a hardware reset (low to high to low) on pin 48. | — | — | — |
| | Alternatively it can be reset with: Analog reset and Digital reset | 00h 4004h 4003h 4002h 4001h 60F7h | 81h 68h 00h 00h 00h 01h | |
| 3 | Set input clock divider | 11h 53h | 80h 80h | Select master page Set clock divider to /2 |
| 4 | Reset interleaving correction engine. Register access default into page 68h | 6000h 6000h | 01h 00h | Channel AB (and channel CD since device is in broadcast mode) |
| 5 | Default registers for JESD analog page | 4003h | 00h | Select JESD analog page |
| | | 4004h 6016h | 6Ah 02h | PLL mode 40x for Channel AB and CD |
| 6 | Default registers for JESD digital page | 4003h | 00h | Select JESD digital page |
| | | 4004h 6000h 6006h | 69h 80h 0Fh | Set CTRL K for channel AB and CD Set K to 16 |
| 7 | Enable single SYNCb input (SYNCAB) | 4005h | 01h | Disable broadcast mode |
| | | 7001h | 22h | Use SYNCAB for channel C/D |
| 8 | Pulse SYNCb (pin 55/56) from low to high to transmit data from k28.5 sync mode | — | — | — |

8.1.2 Hardware Reset

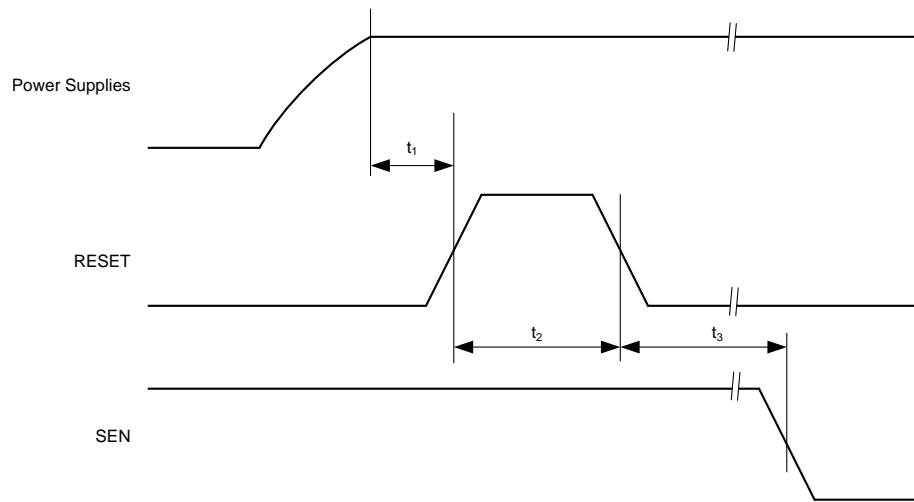


Figure 138. Hardware Reset Timing Diagram

Table 64. Timing Requirements for Figure 138

| | | | MIN | TYP | MAX | UNIT |
|-------|----------------------|--|-----|-----|-----|------|
| t_1 | Power-on delay | Delay from power up to active high RESET pulse | 1 | | | ms |
| t_2 | Reset pulse duration | Active high RESET pulse duration | 10 | | | ns |
| t_3 | Register write delay | Delay from RESET disable to SEN active | 100 | | | ns |

8.1.3 SNR and Clock Jitter

The signal to noise ratio of the ADC is limited by three different factors: the quantization noise is typically not noticeable in pipeline converters and is 84 dB for a 14-bit ADC. The thermal noise limits the SNR at low input frequencies while the clock jitter sets the SNR for higher input frequencies.

$$SNR_{ADC}[dBc] = -20 \log \sqrt{\left(10^{-\frac{SNR_{Quantization\ Noise}}{20}}\right)^2 + \left(10^{-\frac{SNR_{Thermal\ Noise}}{20}}\right)^2 + \left(10^{-\frac{SNR_{Jitter}}{20}}\right)^2} \quad (2)$$

The SNR limitation resulting from sample clock jitter can be calculated following:

$$SNR_{jitter}[dBc] = -20 \log(2\pi \times f_{in} \times T_{jitter}) \quad (3)$$

The total clock jitter (T_{jitter}) has two components – the internal aperture jitter (120 fs for ADS58J63) which is set by the noise of the clock input buffer and the external clock jitter. It can be calculated as following:

$$T_{jitter} = \sqrt{(T_{jitter, Ext_Clock_Input})^2 + (T_{Aperture_ADC})^2} \quad (4)$$

External clock jitter can be minimized by using high-quality clock sources and jitter cleaners as well as band-pass filters at the clock input while a faster clock slew rate also improves the ADC aperture jitter.

The ADS58J63 has a thermal noise of approximately 72 dBFS and an internal aperture jitter of 120 fs.

8.1.4 ADC Test Pattern

The ADS58J63 provides several different options to output test patterns instead of the actual output data of the ADC in order to simplify bring up of the JESD204B digital interface link. The output data path is shown in Figure 139

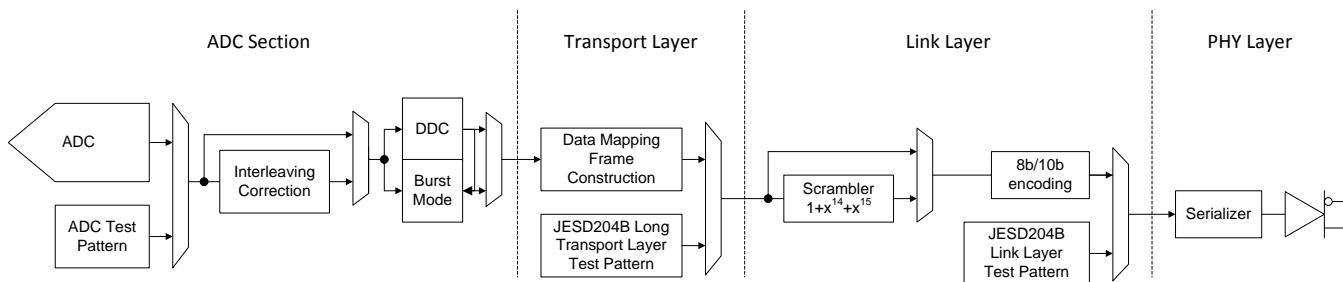


Figure 139. ADC Test Pattern

8.1.4.1 ADC Section

The ADC test pattern replaces the actual output data of the ADC. The following test patterns are available in register 74h. In order to get the test pattern output properly, the interleaving correction needs to be disabled (6100h, address 18h) and burst mode enabled (DDC disabled).

Burst mode only supports LMFS = 4421 (DDC Modes have different configurations) and test pattern switches between 9-bit (low resolution) and 14-bit (high resolution) output. See Table 65

Table 65. ADC Test Pattern Settings

| Bit | Name | Default | Description |
|-------|--------------|---------|--|
| D7-D4 | TEST PATTERN | 0000 | Test pattern output on channel A and B 0000 Normal Operation using ADC output data 0001 Outputs all 0s 0010 Outputs all 1s 0011 Outputs toggle pattern: Output data are an alternating sequence of 101010101010 and 010101010101 0100 Output digital ramp: output data increments by one LSB every clock cycle from code 0 to 16384 0110 Single pattern: output data is custom pattern 1 (75h and 76h) 0111 Double pattern: output data alternates between custom patter 1 and custom pattern 2 1000 Deskew pattern: output data is 2AAAh 1001 SYNC pattern: output data is 3FFFh |

8.1.4.2 Transport Layer Pattern

The Transport Layer maps the ADC output data into 8bit octets and constructs the JESD204B frames using the LMFS parameters. Tail bits or '0's are added when needed. Alternatively the JESD204B long transport layer test pattern can be substituted as shown in Table 66 .

Table 66. Transport Layer Test-mode

| Bit | Name | Default | Description |
|-----|-------------|---------|---|
| D4 | TESTMODE EN | 0 | Generates long transport layer test pattern mode according to clause 5.1.6.3 of JESD204B specification 0 = test mode disabled 1 = test mode enabled |

8.1.4.3 Link Layer Pattern

The Link Layer contains the scrambler and the 8b/10b encoding of any data passed on from the Transport Layer. Additionally it also handles the initial lane alignment sequence which can be manually restarted. The Link Layer test patterns are intended for testing the quality of the link (jitter testing etc). The test patterns do not pass through the 8b/10b encoder and contain the options shown in [Table 67](#).

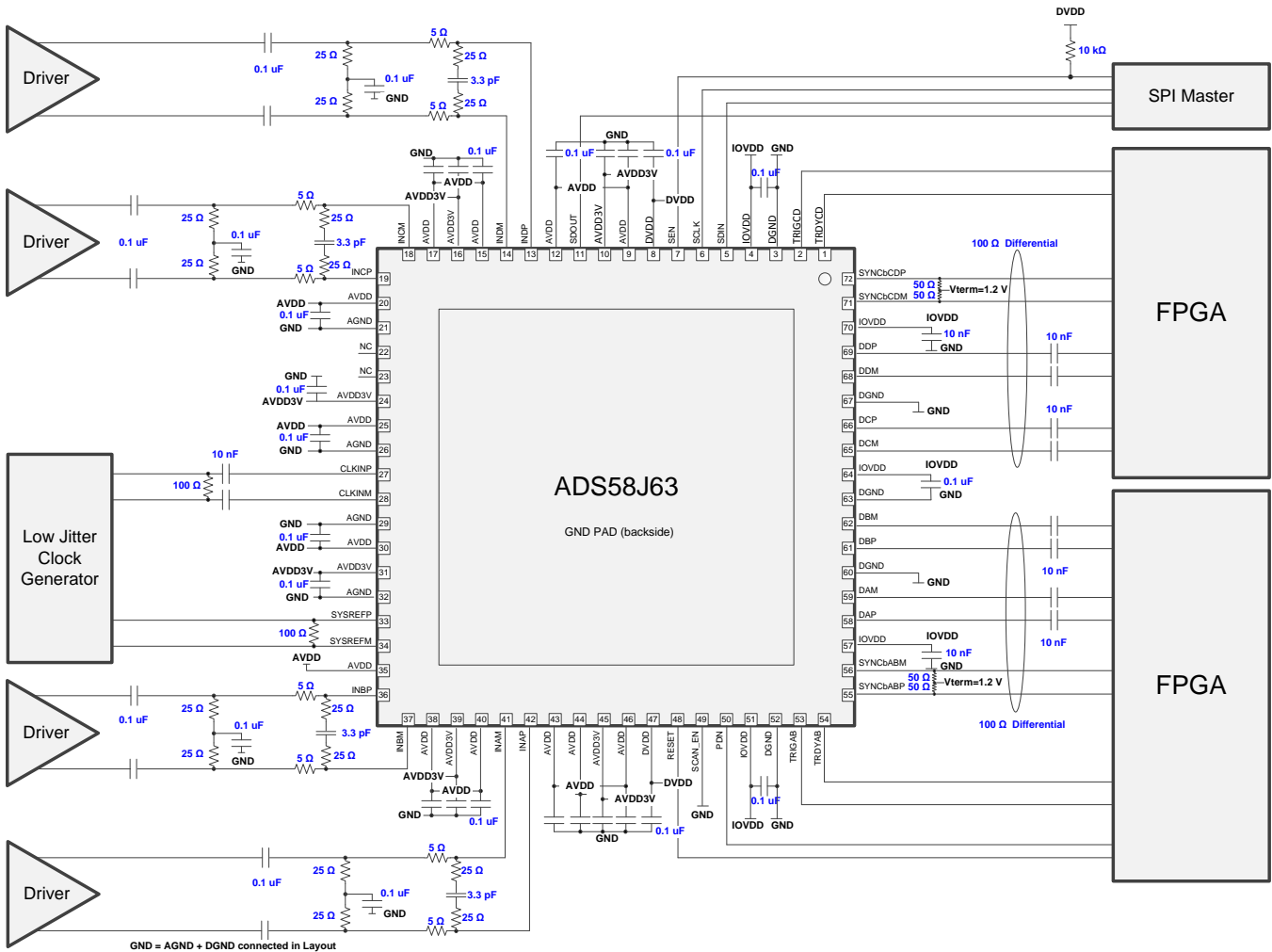
Table 67. Link Layer Test-mode

| Bit | Name | Default | Description |
|-------|---------------------|---------|--|
| D7-D5 | LINK LAYER TESTMODE | 000 | Generates pattern according to clause 5.3.3.8.2 of the JESD204B document 000 normal ADC data 001 D21.5 (high frequency jitter pattern) 010 K28.5 (mixed frequency jitter pattern) 011 Repeat initial lane alignment (generates K28.5 character and repeat lane alignment sequences continuously) 100 12 octet RPAT jitter pattern |

Furthermore a 2^{15} PRBS can be enabled by setting up a custom test pattern (AAAA) in the ADC section and running that through the 8b/10b encoder with scrambling enabled.

8.2 Typical Application

The ADS58J63 is designed for wideband receiver applications demanding excellent dynamic range over a large input frequency range. A typical schematic for an AC coupled dual receiver (dual FPGA with dual SYNC) is shown below.



NOTE: GND = AGND and DGND connected in the PCB layout.

Figure 140. Application Diagram ADS58J63

8.2.1 Design Requirements

By using the simple drive circuit of Figure 140 (when AMP drives ADC) or Figure 51 (when transformers drive ADC), uniform performance can be obtained over a wide frequency range. The buffers present at the analog inputs of the device help isolate the external drive source from the switching currents of the sampling circuit.

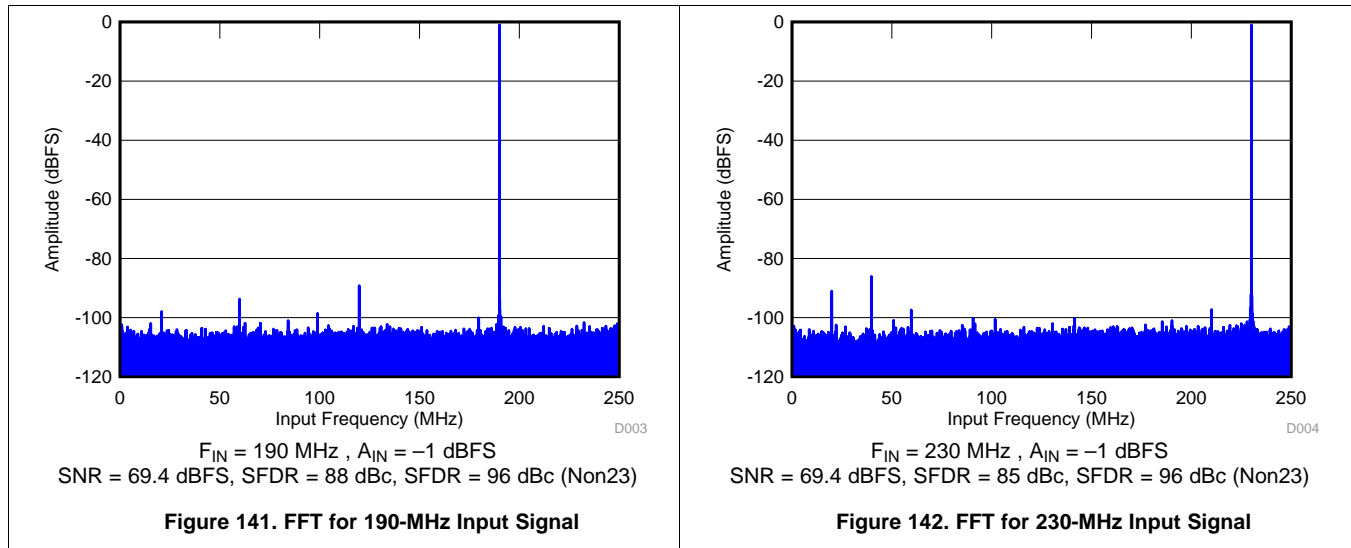
8.2.2 Detailed Design Procedure

For optimum performance, the analog inputs must be driven differentially. This architecture improves the common-mode noise immunity and even-order harmonic rejection. A small resistor (5 Ω to 10 Ω) in series with each input pin is recommended to damp out ringing caused by package parasitics, as shown in Figure 140.

Typical Application (continued)

8.2.3 Application Curves

Figure 141 and Figure 142 show the typical performance at 190 MHz and 230 MHz, respectively.



9 Power Supply Recommendations

The device requires a 1.9-V nominal supply for DVDD, a 1.9-V nominal supply for AVDD, and a 3-V nominal supply for AVDD3V. There is no specific sequence for power-supply requirements during device power-up. AVDD, DVDD, and AVDD3V can power-up in any order.

10 Layout

10.1 Layout Guidelines

The device evaluation module (EVM) layout can be used as a reference layout to obtain the best performance. A layout diagram of the EVM top layer is provided in [Figure 143](#). Complete layout of EVM is available at [ADS58J63's EVM folder](#). Some important points to remember during board layout are:

- Analog inputs are located on opposite sides of the device pinout to ensure minimum crosstalk on the package level. To minimize crosstalk onboard, the analog inputs must exit the pinout in opposite directions, as shown in the reference layout of [Figure 143](#) as much as possible.
- In the device pinout, the sampling clock is located on a side perpendicular to the analog inputs in order to minimize coupling between them. This configuration is also maintained on the reference layout of [Figure 143](#) as much as possible.
- Keep digital outputs away from the analog inputs. When these digital outputs exit the pinout, the digital output traces must not be kept parallel to the analog input traces because this configuration can result in coupling from the digital outputs to the analog inputs and degrade performance. All digital output traces to the receiver [such as a field-programmable gate array (FPGA) or an application-specific integrated circuit (ASIC)] must be matched in length to avoid skew among outputs.
- At each power-supply pin (AVDD, DVDD, or AVDDD3V), keep a 0.1- μ F decoupling capacitor close to the device. A separate decoupling capacitor group consisting of a parallel combination of 10- μ F, 1- μ F, and 0.1- μ F capacitors can be kept close to the supply source.

10.2 Layout Example

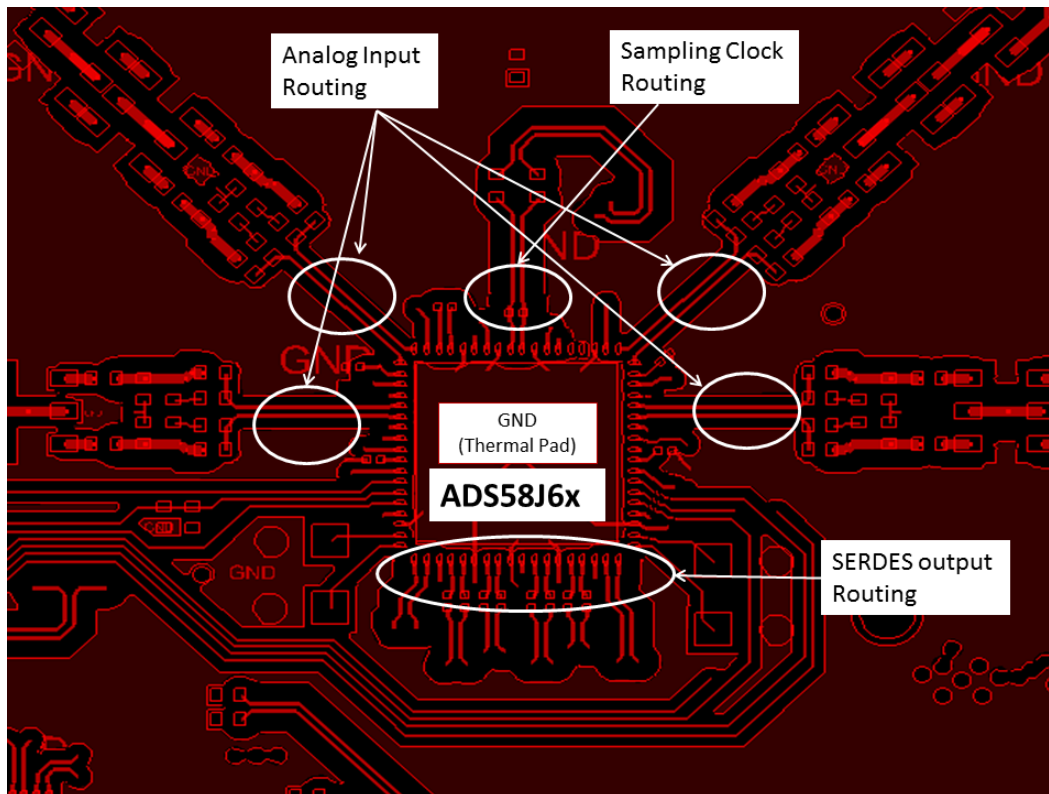


Figure 143. ADS58J63 EVM Layout

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| ADS58J63IRMPR | Active | Production | VQFN (RMP) 72 | 1500 LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | AZ58J63 |
| ADS58J63IRMPR.A | Active | Production | VQFN (RMP) 72 | 1500 LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | AZ58J63 |
| ADS58J63IRMPT | Active | Production | VQFN (RMP) 72 | 250 SMALL T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | AZ58J63 |
| ADS58J63IRMPT.A | Active | Production | VQFN (RMP) 72 | 250 SMALL T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | AZ58J63 |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| ADS58J63IRMPR | VQFN | RMP | 72 | 1500 | 330.0 | 24.4 | 10.25 | 10.25 | 2.25 | 16.0 | 24.0 | Q2 |
| ADS58J63IRMPT | VQFN | RMP | 72 | 250 | 180.0 | 24.4 | 10.25 | 10.25 | 2.25 | 16.0 | 24.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

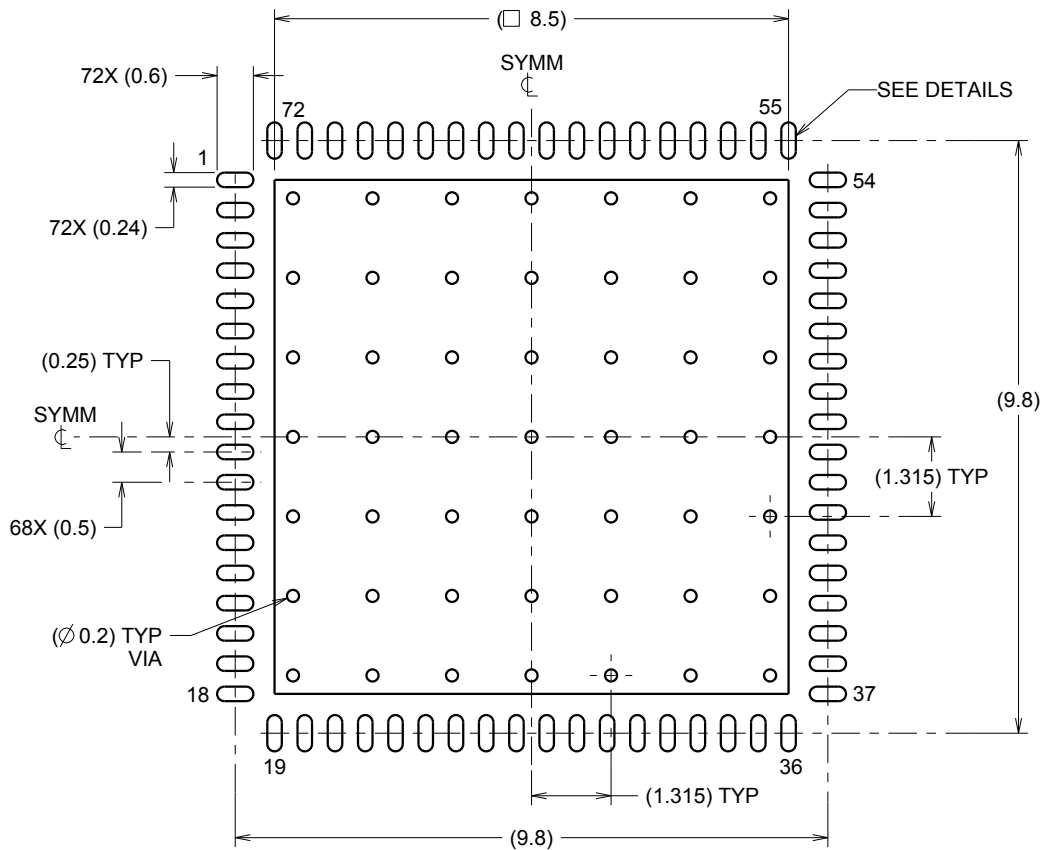
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| ADS58J63IRMPR | VQFN | RMP | 72 | 1500 | 350.0 | 350.0 | 43.0 |
| ADS58J63IRMPT | VQFN | RMP | 72 | 250 | 213.0 | 191.0 | 55.0 |

EXAMPLE BOARD LAYOUT

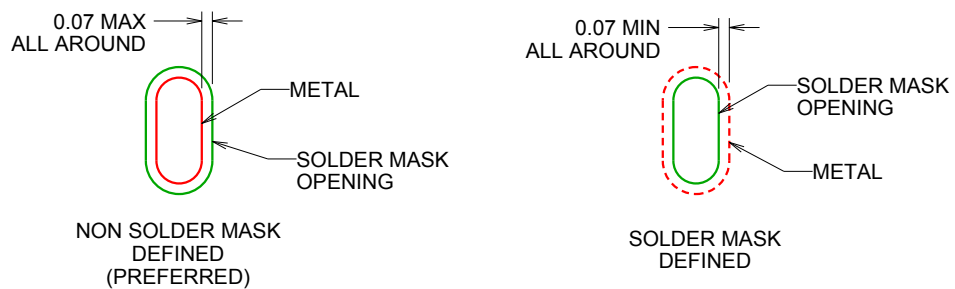
RMP0072A

VQFN - 0.9 mm max height

VQFN



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4221047/B 02/2014

NOTES: (continued)

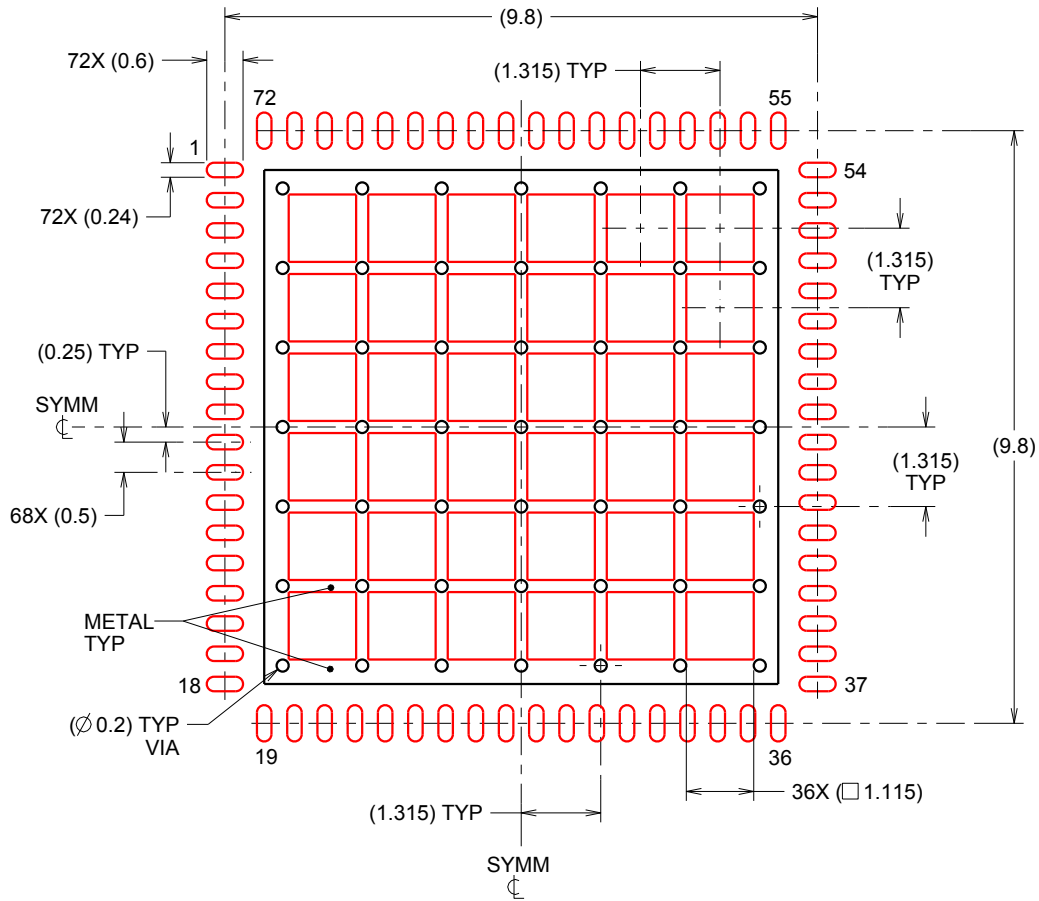
- This package is designed to be soldered to a thermal pad on the board. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/sluea271).

EXAMPLE STENCIL DESIGN

RMP0072A

VQFN - 0.9 mm max height

VQFN



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
62% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

4221047/B 02/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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