14-Bit, Input-Buffered, 160-MSPS, Analog-to-Digital Converter with JESD204A Output Interface

Check for Samples: ADS61JB46

FEATURES

- **Output Interface:**
  - **Single-Lane and Dual-Lane Interfaces**
  - **Maximum Data Rate: 3.125 Gbps**
  - **Meets JEDEC JESD204A Specification**
  - **CML Outputs with Current Programmable from 2 mA to 32 mA**
- **Power Dissipation:**
  - **583 mW at 160 MSPS in Dual-Lane Mode**
  - **Power Scales Down with Clock Rate**
- **Input Interface: Buffered Analog Inputs**
- **SNR at 185-MHz IF: –72.7 dBFS**
- **Analog Input Dynamic Range: 2 V_{PP}**
- **Reference Support: External and Internal (Trimmed)**
- **Supply:**
  - **Analog and Digital: 1.8 V**
  - **Input Buffer: 3.3 V**
- **Programmable Digital Gain: 0 dB to 6 dB**
- **Output: Straight Offset Binary or Twos Complement**
- **Package: 6-mm × 6-mm QFN-40**

APPLICATIONS

- **Wireless Base-Station Infrastructures**
- **Test and Measurement Instrumentation**

DESCRIPTION

The ADS61JB46 is a high-performance, low-power, single-channel, analog-to-digital converter with an integrated JESD204A output interface. Available in a 6-mm × 6-mm QFN package, with both single-lane and dual-lane output modes, the device offers an unprecedented level of compactness. The output interface is compatible to the JESD204A standard, with an additional mode (as per the IEEE standard 802.3-2002 part 3, clause 36.2.4.12) to interface seamlessly to the TI TLK family of SERDES transceivers. Equally impressive is the inclusion of an on-chip analog input buffer, providing isolation between the sample-and-hold switches and higher and more consistent input impedance.

The device is specified over the industrial temperature range (–40°C to +85°C).

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS(1)

		VALUE	UNIT
Supply voltage range	AVDD	–0.3 to +2.2	V
	DRVDD	–0.3 to +2.2	V
	IOVDD	–0.3 to +2.2	V
	AVDD_3V	–0.3 to +3.9	V
Voltage between AGND and DRGND		–0.3 to +0.3	V
Voltage applied to:	External VCM pin	–0.3 to +2.2	V
	Analog input pins	–0.3 to min (3, AVDD_3V + 0.3)	V
	Digital input pins	–0.3 to AVDD + 0.3	V
	Clock input pins(2)	–0.3 to AVDD + 0.3	V
Operating free-air temperature range, T_A		–40 to +85	°C
Junction temperature		+105	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) When AVDD is turned off, TI recommends switching off the input clock (or ensuring the voltage on CLKP, CLKM is less than |0.3 V|). This setting prevents the electrostatic discharge (ESD) protection diodes at the clock input pins from turning on.

THERMAL INFORMATION

THERMAL METRIC(1)		ADS61JB46 RHA (QFN)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	30.7	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	17	
θ_{JB}	Junction-to-board thermal resistance	5.7	
ψ_{JT}	Junction-to-top characterization parameter	0.2	
ψ_{JB}	Junction-to-board characterization parameter	5.7	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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RECOMMENDED OPERATING CONDITIONS

			MIN	TYP	MAX	UNIT
SUPPLIES, ANALOG INPUTS, AND REFERENCE VOLTAGES						
AVDD	Analog supply voltage		1.7	1.8	1.9	V
DRVDD	Digital supply voltage		1.7	1.8	1.9	V
IOVDD	CML buffer supply voltage		1.7	1.8	1.9	V
AVDD_3V	Analog buffer supply voltage		3.0	3.3	3.6	V
	Differential input voltage range			2		V_{PP}
	Input common-mode voltage			VCM ± 0.05		V
	VCM (output), internal reference mode(1)			1.95		V
	VCM (input), external reference mode			1.4		V
CLOCK INPUT						
	Input clock rate	In JESD204A single-lane mode	15.625		156.3	MSPS
		In JESD204A dual-lane mode	31.25		160	MSPS
	Input clock amplitude differential ($V_{CLKP} – V_{CLKM}$)	Sine wave, ac-coupled	0.2	3.0		V_{PP}
		LVPECL, ac-coupled		1.6		V_{PP}
		LVDS, ac-coupled		0.7		V_{PP}
		CMOS, single-ended, ac-coupled		1.5		V
	Input clock duty cycle		35%	50%	65%	
DIGITAL OUTPUTS						
	Output data rate	In single-lane mode	312.5	20x (sample rate)	3125	Mbps
		In dual-lane mode	312.5	10x (sample rate)	1600	Mbps
C_{LOAD}	Maximum external load capacitance from each pin to DRGND			5		pF
R_{LOAD}	External termination from each output pin to IOVDD			50		Ω
T_A	Operating free-air temperature		–40		+85	°C

(1) Typical VCM reduces to 1.85 V after HIGH_SFDR_MODE (register address 02h) is written.

Table 1. HIGH_SFDR_MODE Summary

MODE	DESCRIPTION
HIGH_SFDR_MODE	Write register 02h, value 71h, to obtain best HD3 for input frequencies between 150 MHz to 250 MHz.

ELECTRICAL CHARACTERISTICS

Typical values are at +25°C, minimum and maximum values are across the full temperature range of T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.8 V, AVDD_3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, clock frequency = 160 MSPS, 10x mode, 50% clock duty cycle, –1-dBFS differential analog input, internal reference mode, and CML buffer current setting = 16 mA, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE VOLTAGES (Internal)						
	VCM analog input common-mode voltage (output)			1.95		V
	VCM output current (resulting in a VCM change of ±50 mV)			2.5		mA
REFERENCE VOLTAGES (External)						
	VCM reference voltage (input)			1.4 ± 0.1		V
ANALOG INPUT						
	Differential input voltage range			2.0		V_{PP}
	Differential input capacitance			3		pF
	Analog input bandwidth			480		MHz
	Analog input common-mode range			VCM ± 0.05		V
	Analog input common-mode current (per input pin)			1.6		µA
DC ACCURACY						
E_O	Offset error		–20		20	mV
E_{GREF}	Gain error due to internal reference inaccuracy alone		–2.5		2.5	%FS
E_{GCHAN}	Gain error of channel alone			5		%FS
	Gain error temperature coefficient			0.006		mV/°C
PSRR	AC power-supply rejection ratio	50-mV_{PP} signal on AVDD supply		> 30		dB
POWER-DOWN MODES						
	Complete power-down mode			10		mW
	Fast recovery power-down mode			230		mW
	Power with no clock			115		mW
DNL	Differential nonlinearity		–0.95	±0.6		LSB
INL	Integral nonlinearity			±2	±4.5	LSB
POWER-SUPPLY CURRENTS						
I_{AVDD}	AVDD current			132	160	mA
I_{AVDD_3V}	AVDD_3V current			42	55	mA
I_{DRVDD}	DRVDD current			79	100	mA
I_{IOVDD}	IOVDD current (in 10x mode)			31	40	mA
	Total power			583	700	mW
DYNAMIC PERFORMANCE(1)(2)						
SFDR	Spurious-free dynamic range	f_{IN} = 10 MHz		75		dBc
		f_{IN} = 185 MHz	71.5	77		dBc
SNR	Signal-to-noise ratio	f_{IN} = 10 MHz		75		dBFS
		f_{IN} = 185 MHz	69.2	72.7		dBFS
SINAD	Signal-to-noise and distortion ratio	f_{IN} = 10 MHz		72.1		dBFS
		f_{IN} = 185 MHz		71.5		dBFS
HD3	Third-order harmonic distortion	f_{IN} = 10 MHz		75		dBc
		f_{IN} = 185 MHz	71.5	77		dBc
HD2	Second-order harmonic distortion	f_{IN} = 10 MHz		90		dBc
		f_{IN} = 185 MHz	71.5	81		dBc
	Worst spur (excluding HD2, HD3)	f_{IN} = 10 MHz		95		dBc
		f_{IN} = 185 MHz	81	90		dBc

(1) HIGH_SFDR_MODE is enabled.
(2) f_S = 156.25 MSPS, 20x mode.

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DIGITAL CHARACTERISTICS

The dc specifications refer to the condition where the digital outputs do not switch, but are permanently at a valid logic level '0' or '1'.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS						
V_{IH}	High-level input voltage		1.2			V
V_{IL}	Low-level input voltage				0.6	V
I_{IH}	High-level input current	SEN		0		µA
		SCLK, SDATA, RESET, PDN, PDN_ANA		10		µA
I_{IL}	Low-level input current	SEN		10		µA
		SCLK, SDATA, RESET, PDN, PDN_ANA		0		µA
DIGITAL OUTPUTS (SDOUT)						
V_{OH}	High-level output voltage		DRVDD – 0.1	DRVDD		V
V_{OL}	Low-level output voltage			0	0.1	V
CML OUTPUTS (50-Ω single-ended external termination to IOVDD)						
	IOVDD supply range		1.7	1.8	1.9	V
	High-level output voltage			IOVDD		V
	Low-level output voltage			IOVDD – 0.4		V
|VOD|	Output differential voltage			0.4		V
V_{OCM}	Output common-mode voltage			IOVDD – 0.2		V
	Transmitter short-circuit current	Transmitter terminals shorted to any voltage between –0.25 V and 1.45 V	–90		50	mA
	Single-ended output impedance			50		Ω
UI	Unit interval		625		3200	UI
T_J	Total jitter			0.35		p-pUI
t_{RISE}, t_{FALL}	Rise time, Fall time	5-pF, single-ended load capacitance to ground		175		ps

WAKE-UP TIMING CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{WAKE}	Wake-up time	Time to valid data after coming out of complete power-down mode		50		µs
		Time to valid data after coming out of fast-recovery power-down mode		50		µs
		Time to valid data after coming out of software power-down mode		10		µs
		Time to valid data after stopping and restarting the input clock		5		µs

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PARAMETRIC MEASUREMENT INFORMATION

JESD204A OUTPUT INTERFACE

The 14-bit analog-to-digital converter (ADC) output is padded with four zeros on the LSB side to form a 16-bit output. Two 8B10B codes are formed; one from the eight MSBs and the other from the six LSBs and the two padded zeros, as shown in Figure 1.

Figure 1. ADC Output Mapping to Two 8B10B Codes

The two octets can be either transmitted on the same lane (single-lane interface, Figure 2) or on two lanes (dual-lane interface, Figure 3). By default, the device operates in single-lane interface.

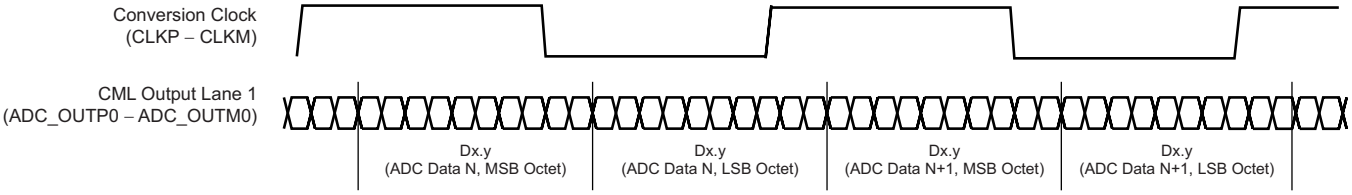

Figure 2. Single-Lane Interface Timing Diagram

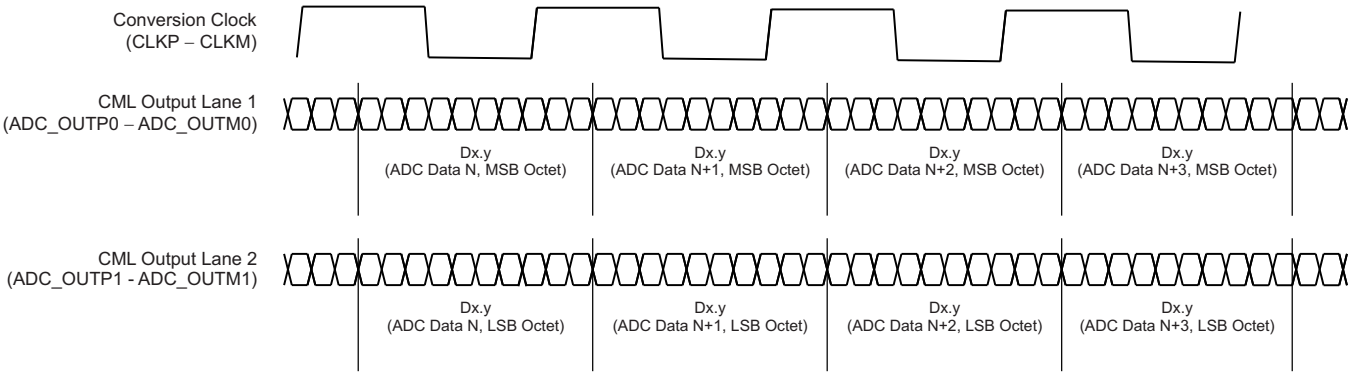

Figure 3. Dual-Lane Interface Timing Diagram

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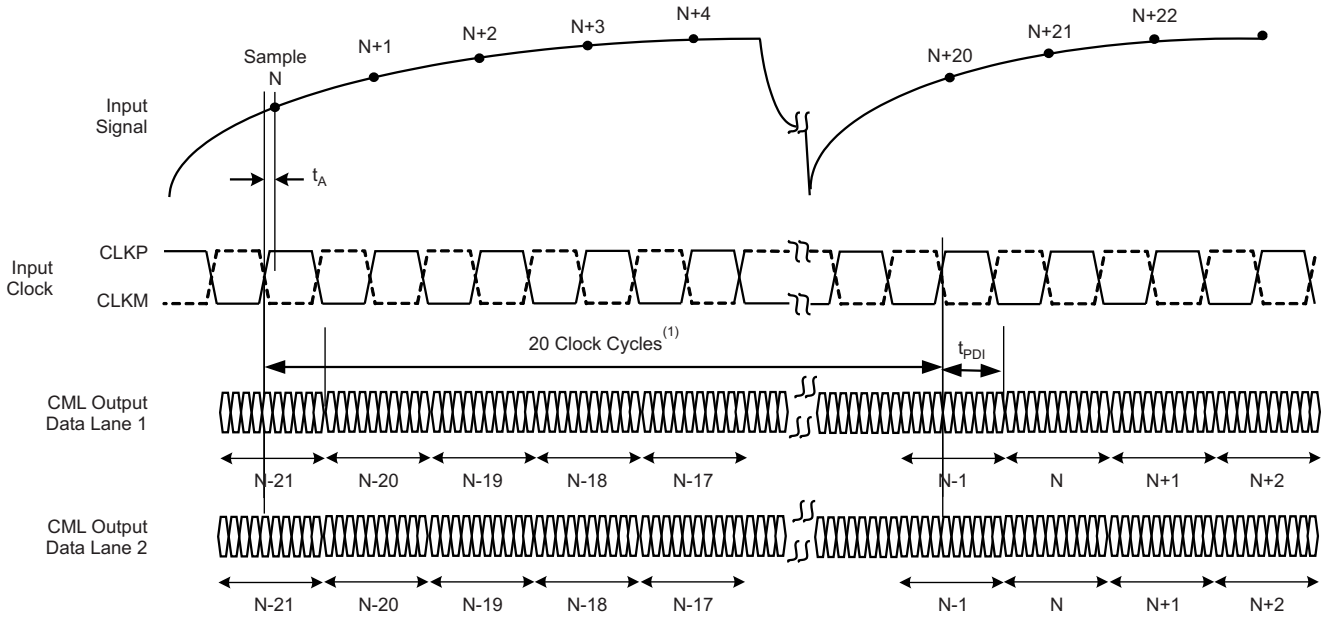
PARAMETRIC MEASUREMENT INFORMATION (continued)

A detailed dual-lane mode timing diagram is shown in Figure 4.



(1) These clock cycles comprise the ADC latency. At higher sampling frequencies, t_{PDI} > 1 clock cycle and overall latency = ADC latency + 1.

Figure 4. Dual-Lane Mode Timing Diagram

PARAMETER		30 MSPS	40 MSPS	60 MSPS	160 MSPS	UNIT
T_A	Aperture delay	560	560	560	560	ps
T_J	Aperture jitter (RMS)	125	125	125	125	f_S
	Latency	20	20	20	20	Clocks
t_{PDI}	Data propagation delay	33.3	26.2	18.9	15.3	ns

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The receiver issues a synchronization request through the SYNC~P, SYNC~M pins whenever the frame boundary of the output data stream must be synchronized to. Figure 5 shows how the transmission switches from normal data (D) to code group synchronization symbols K28.5 symbols during and after a synchronization request.

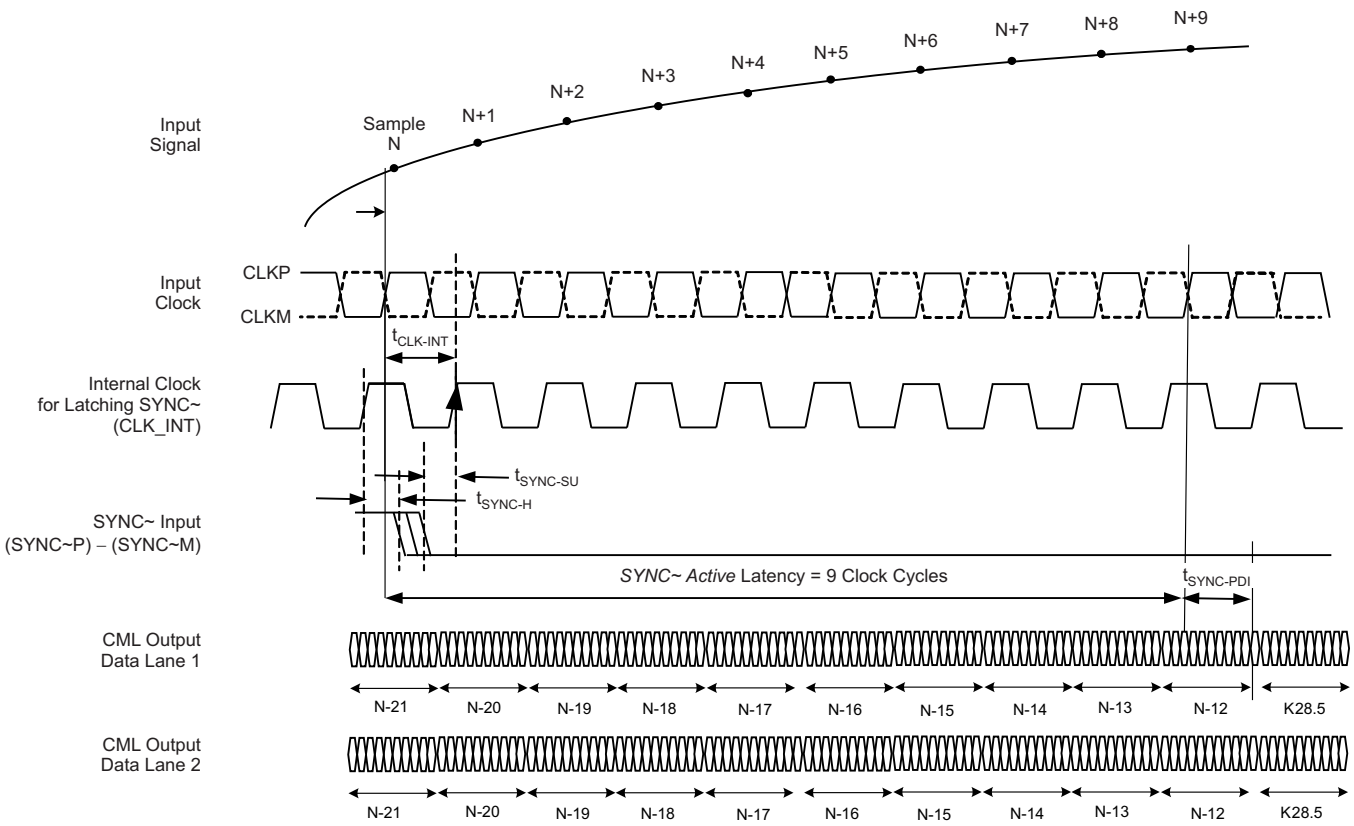

Figure 5. SYNC~ Active Timing Diagram

Table 2. SYNC~ Falling Edge Timing at 160 MSPS

PARAMETER		DESCRIPTION	TYP	UNIT
$t_{CLK-INT}$		Delay from the input clock rising edge to the internal clock (CLK_INT) rising edge used to latch the SYNC~ falling edge	10.5	ns
$t_{SYNC-SU}$	SYNC~ active edge setup time	Minimum delay required from SYNC~ falling edge to CLK_INT rising edge	2	ns
t_{SYNC-H}	SYNC~ active edge hold time	Minimum delay required from CLK_INT rising edge to SYNC~ falling edge	2	ns
	SYNC~ active latency	Number of clocks for K28.5 to appear at the output after a SYNC~ request	9	clocks
$t_{SYNC-PDI}$	SYNC~ data propagation delay	Similar to data propagation delay	15.3	ns

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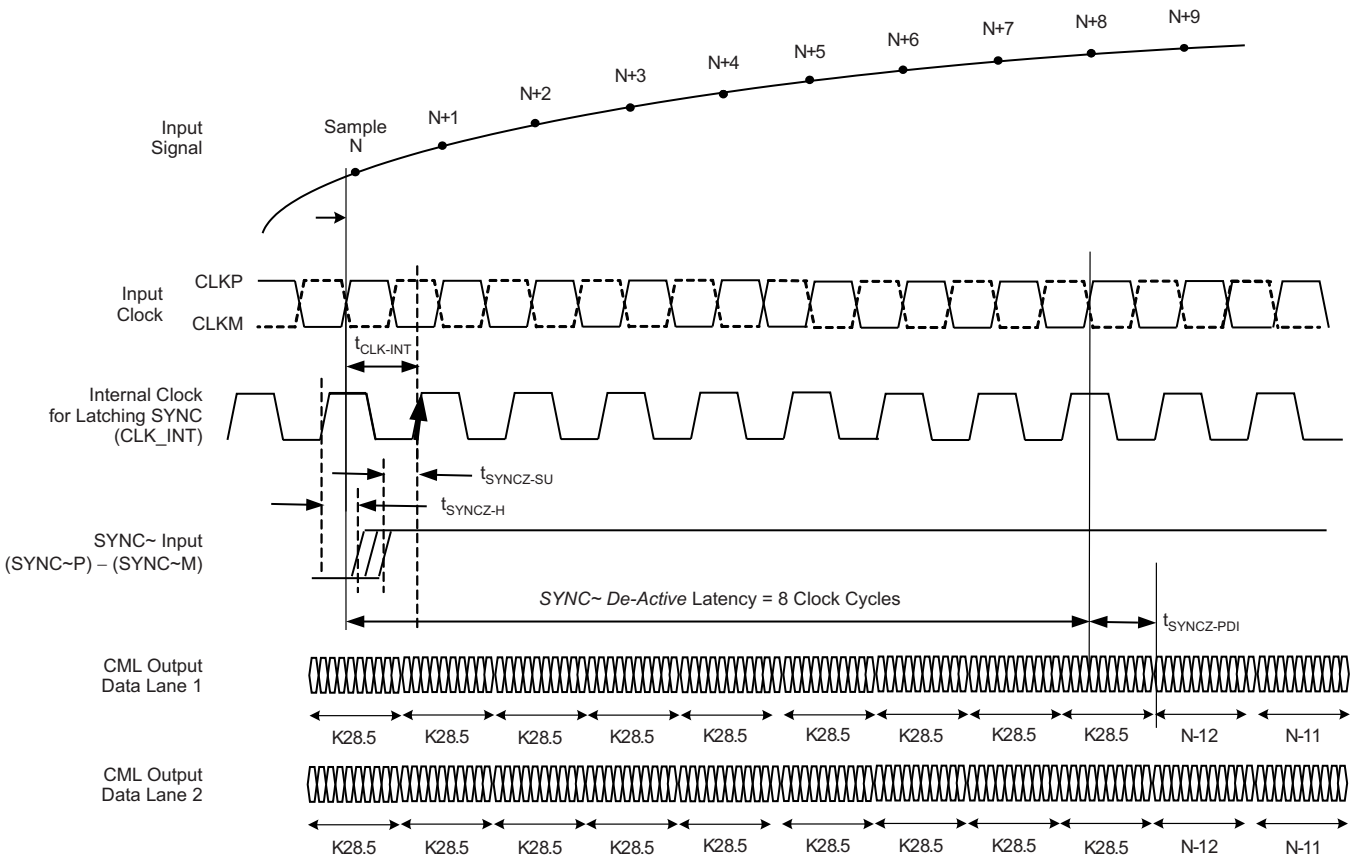

Figure 6. SYNC~ De-Active Timing Diagram

Table 3. SYNC~ Rising Edge Timing at 160 MSPS

PARAMETER		DESCRIPTION	TYP	UNIT
$t_{CLK-INT}$		Delay from input clock rising edge to the internal clock (CLK_INT) rising edge used to latch the SYNC~ rising edge	10.5	ns
$t_{SYNCZ-SU}$	SYNC~ active edge setup time	Minimum delay required from SYNC~ rising edge to CLK_INT rising edge	2	ns
$t_{SYNCZ-H}$	SYNC~ active edge hold time	Minimum delay required from CLK_INT rising edge to SYNC~ rising edge	2	ns
	SYNC~ de-active latency	Number of clocks for normal data to appear at the output after a SYNC~ de-activate request	8	Clocks
$t_{SYNCZ-PDI}$	SYNC~ de-active data propagation delay	Similar to data propagation delay	15.3	ns

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4-LEVEL CONTROL

The DFS_EXTREF and MODE pins function as 4-level control pins in the device, as described in Table 4 and Table 5. A simple scheme to generate a 4-level voltage is shown in Figure 7.

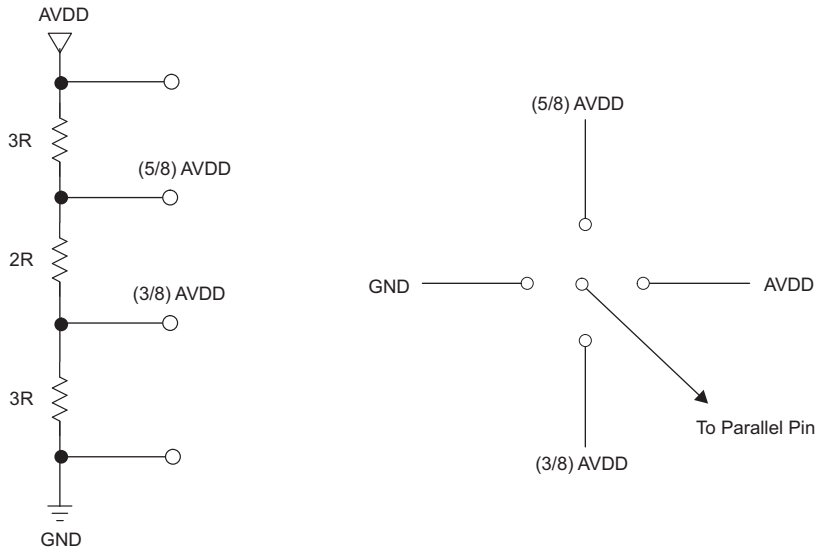

Figure 7. Simple Scheme to Configure 4-Level Control Pins

Table 4. DFS_EXTREF Pin (Pin 3)

DFS_EXTREF	DESCRIPTION
0 +150 mV / 0 mV	EXTREF = 0, DFS = 0
(3/8) AVDD ±150 mV	EXTREF = 1, DFS = 0
(5/8) AVDD ±150 mV	EXTREF = 1, DFS = 1
AVDD 0 mV / –150 mV	EXTREF = 0, DFS = 1

Key:

EXTREF: 0 = Internal reference mode,
1 = External reference mode

DFS: 0 = Twos complement output,
1 = Offset binary output

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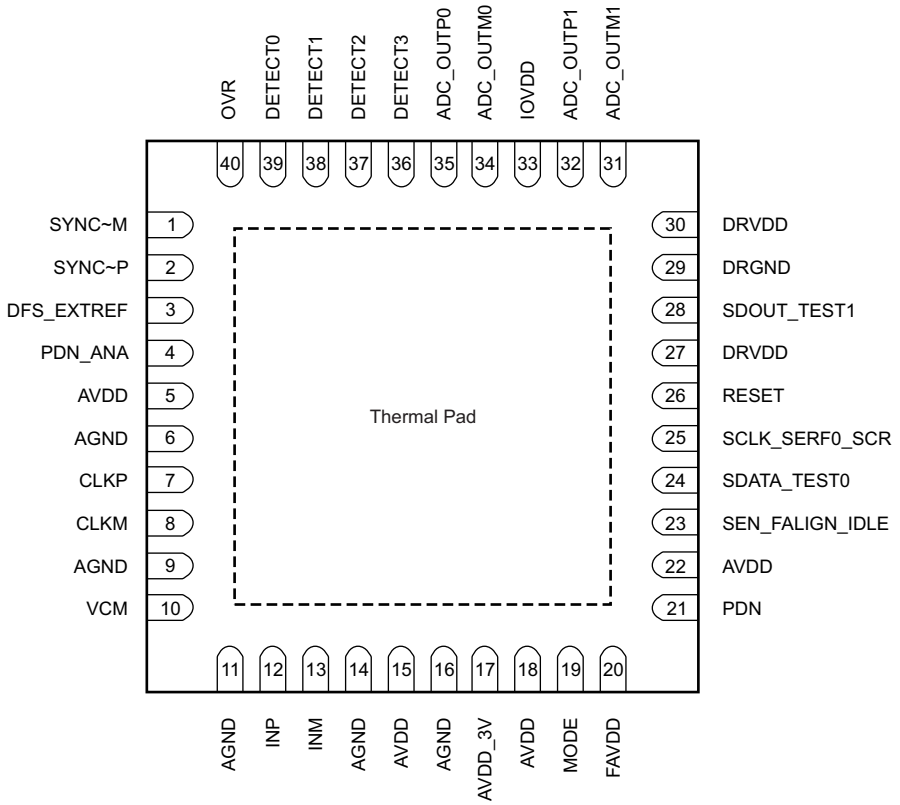
PIN CONFIGURATION

RHA PACKAGE
QFN-40
(Top View)



NOTE: The thermal pad is connected to DRGND.

PIN FUNCTIONS

PIN		DESCRIPTION
NAME	NO.	
ADC_OUTM0	34	CML output lane 1, negative output
ADC_OUTM1	31	CML output lane 2, negative output
ADC_OUTP0	35	CML output lane 1, positive output
ADC_OUTP1	32	CML output lane 2, positive output
AGND	5, 6, 9, 11, 14, 16,	Analog ground
AVDD	15, 18, 22	Analog supply, 1.8 V
AVDD_3V	17	Analog supply for input buffer, 3.3 V
CLKM	8	Conversion clock, negative input
CLKP	7	Conversion clock, positive input
DETECT3	36	Signal level-detect output pins in 1.8-V CMOS logic level. These pins can be used to either output a 4-bit ADC code with low latency or to output a 16-level RMS power estimate.
DETECT2	37	
DETECT1	38	
DETECT0	39	
DFS_EXTREF	3	4-level analog control for data format selection and internal and external reference mode
DRGND	29	Digital ground
DRVDD	27, 30	Digital supply, 1.8 V
FAVDD	20	Fuse supply, connect externally to AVDD, 1.8 V
INM	13	Analog input, Negative
INP	12	Analog input, Positive
IOVDD	33	CML buffer supply, 1.7 V to 1.9 V
MODE	19	4-level control for selecting the serial and parallel interface modes
OVR	40	Over-range output in 1.8-V CMOS logic levels.
PDN	21	Full chip power-down (also referred to as complete power-down mode)
PDN_ANA	4	Analog section power-down; JESD interface is still active. This mode is referred to as fast-recovery power-down mode.
RESET	26	Serial interface RESET input. When using the serial interface mode, the internal registers must be initialized through a hardware RESET by applying a high pulse on this pin or by using the S_RESET register bit; refer to the *Serial Interface* section. In parallel interface mode, the RESET pin must be permanently tied high. In this mode, the SEN_FALIGN_IDLE, SCLK_SERF0_SCR, and SDATA_TEST0 pins function as parallel pins with their functionality described in Table 6, Table 7, and Table 8, respectively.
SCLK_SERF0_SCR	25	Serial clock input in serial interface mode. In parallel interface mode, this pin provides a 4-level control for all JESD modes (single-lane, dual-lane, and scrambling modes).
SDATA_TEST0	24	Serial data input in serial interface mode. In parallel interface mode, this pin provides a JESD test mode.
SDOUT_TEST1	28	Serial data out in serial interface mode. In parallel interface mode, this pin provides a JESD test mode.
SEN_FALIGN_IDLE	23	Serial enable input in serial interface mode. In parallel interface mode, this pin provides a 4-level control for JESD modes.
SYNC~M	1	JESD synchronization request, negative input
SYNC~P	2	JESD synchronization request, positive input
VCM	10	Common-mode output for setting the input common-mode. 1.95 V, reference input in external reference mode.

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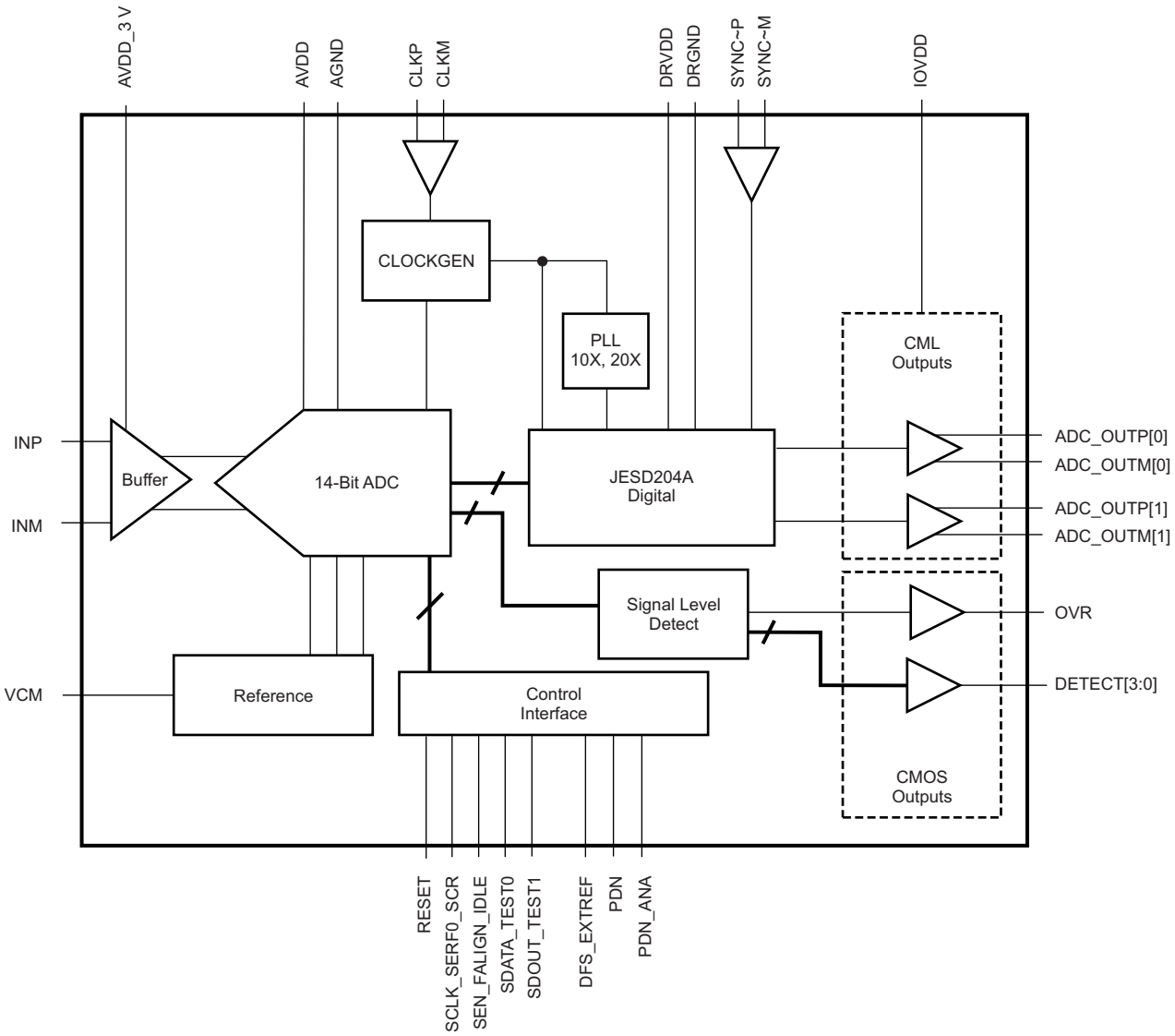
FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

At +25°C, AVDD = 1.8 V, AVDD_3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, f_S = 153.6 MSPS, sine-wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, 16-mA CML current, and 32k-point FFT, unless otherwise noted. Note that after reset, the device is in 0-dB gain mode.

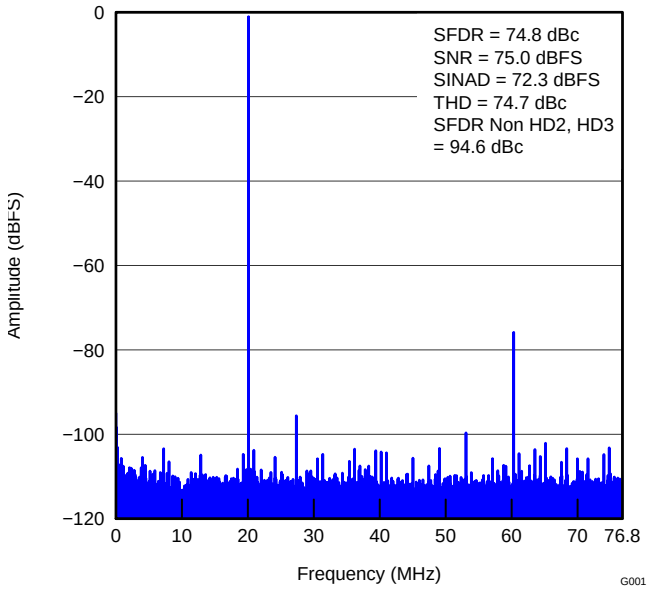


Figure 8. AMPLITUDE vs FREQUENCY (20-MHz IF)

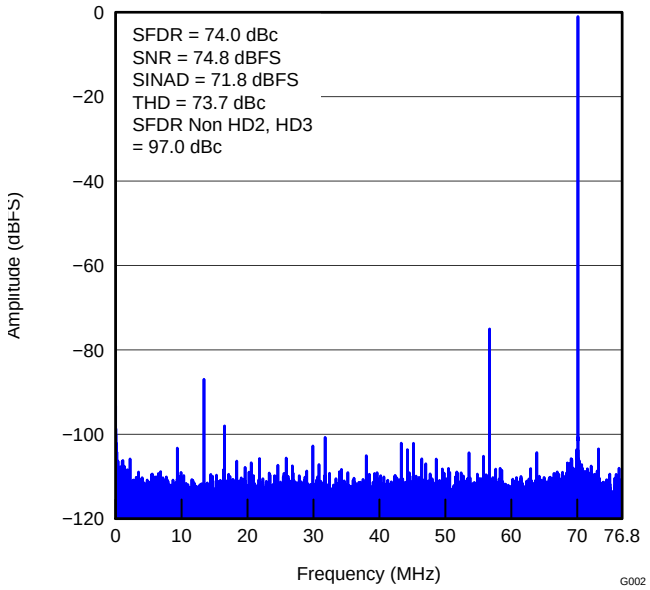


Figure 9. AMPLITUDE vs FREQUENCY (70-MHz IF)

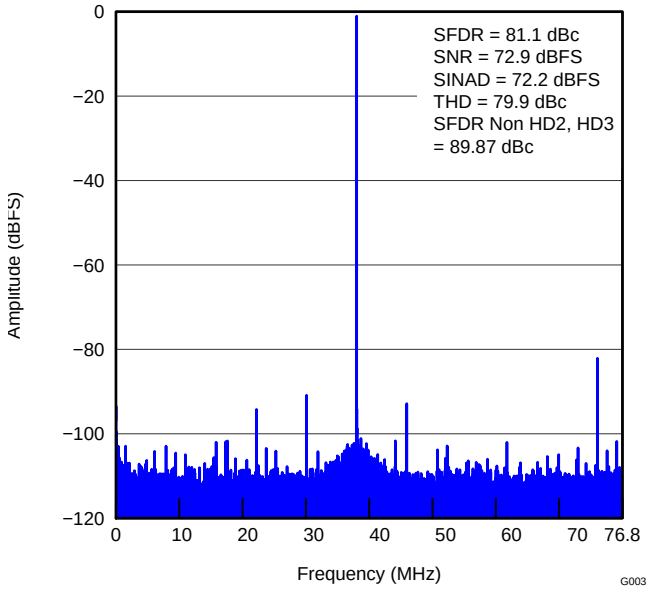


Figure 10. AMPLITUDE vs FREQUENCY (190-MHz IF)

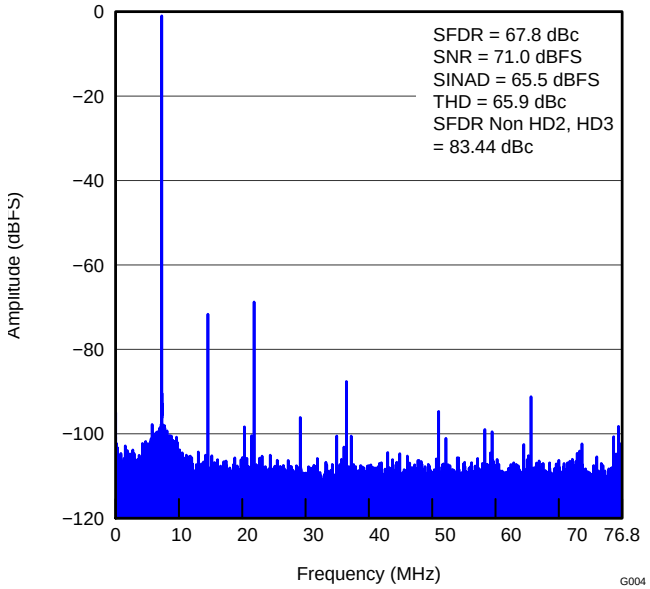


Figure 11. AMPLITUDE vs FREQUENCY (300-MHz IF)

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TYPICAL CHARACTERISTICS (continued)

At +25°C, AVDD = 1.8 V, AVDD_3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, f_S = 153.6 MSPS, sine-wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, 16-mA CML current, and 32k-point FFT, unless otherwise noted. Note that after reset, the device is in 0-dB gain mode.

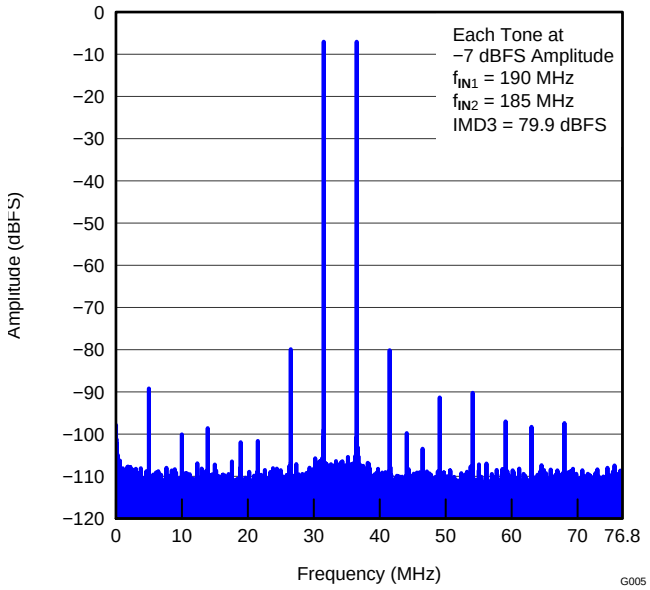

Figure 12. AMPLITUDE vs FREQUENCY (Two-Tone Input Signal)

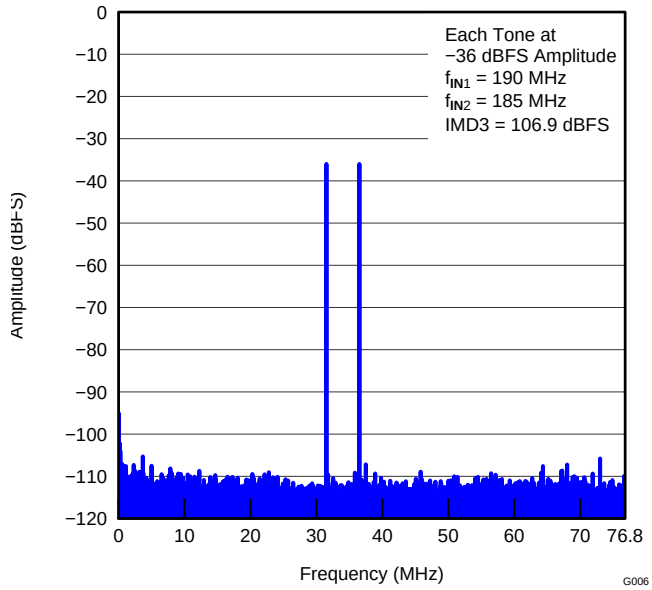

Figure 13. AMPLITUDE vs FREQUENCY (Two-Tone Input Signal)

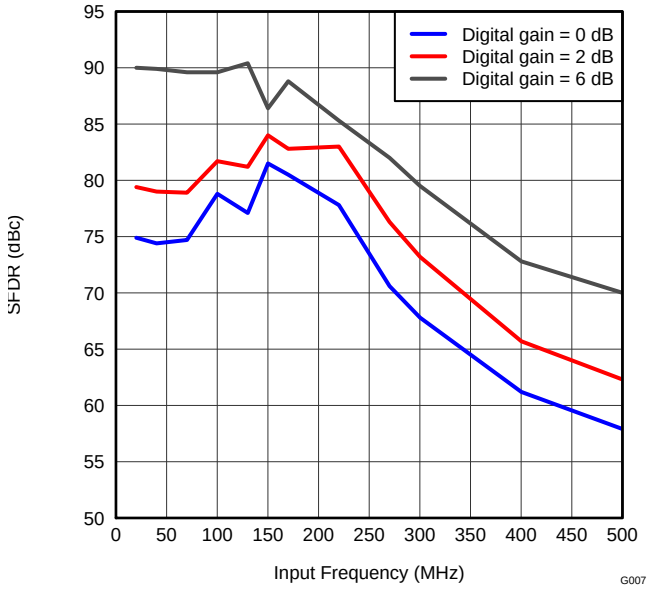

Figure 14. SPURIOUS-FREE DYNAMIC RANGE vs INPUT FREQUENCY

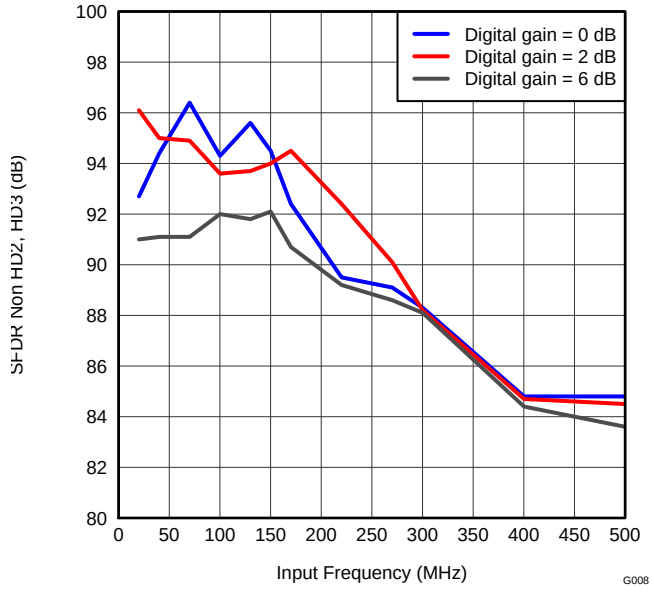

Figure 15. SPURIOUS-FREE DYNAMIC RANGE (NON HD2, HD3) vs INPUT FREQUENCY

TYPICAL CHARACTERISTICS (continued)

At +25°C, AVDD = 1.8 V, AVDD_3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, f_S = 153.6 MSPS, sine-wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, 16-mA CML current, and 32k-point FFT, unless otherwise noted. Note that after reset, the device is in 0-dB gain mode.

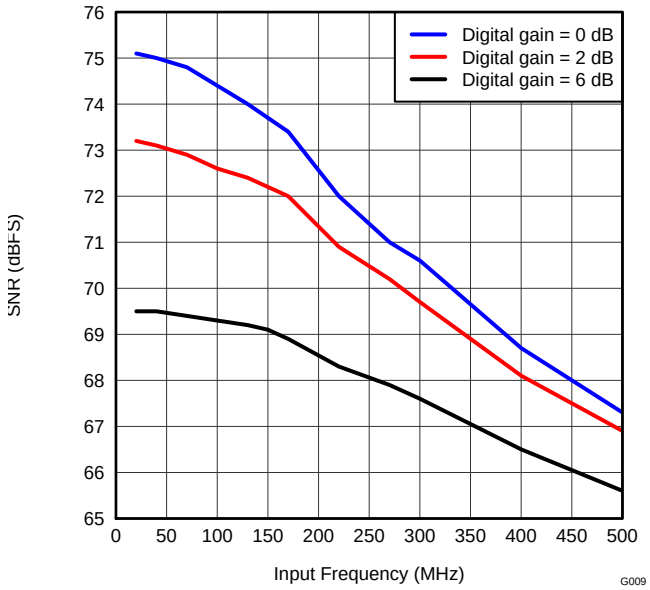

Figure 16. SIGNAL-TO-NOISE RATIO vs INPUT FREQUENCY

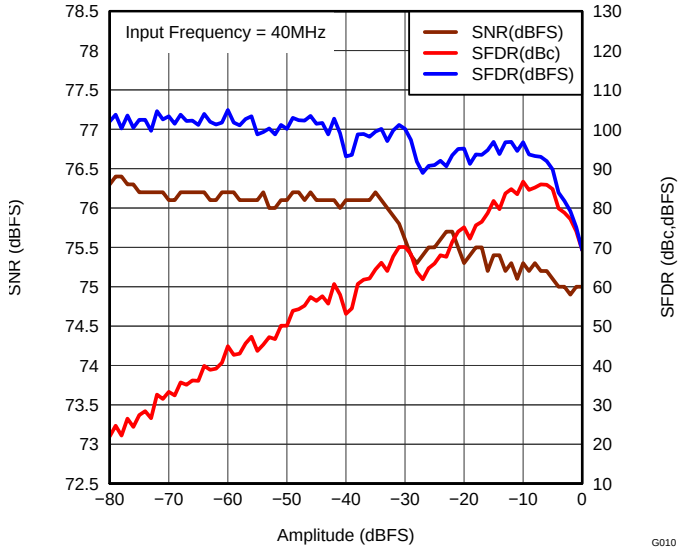

Figure 17. PERFORMANCE ACROSS INPUT AMPLITUDE

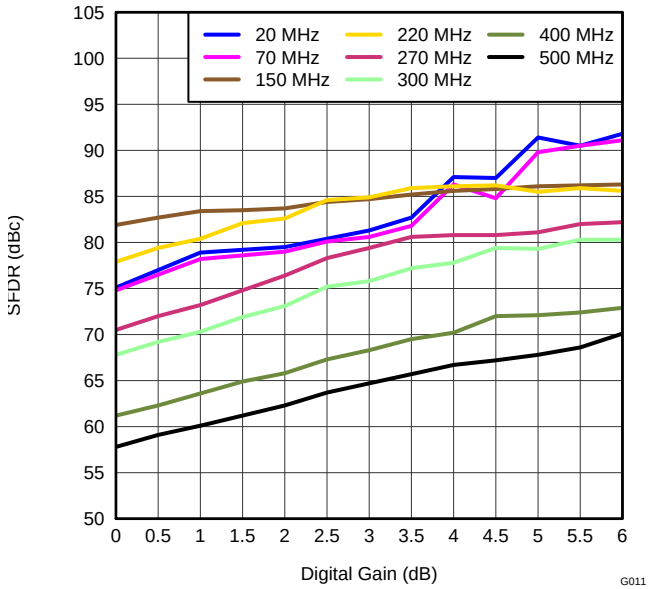

Figure 18. SPURIOUS-FREE DYNAMIC RANGE vs DIGITAL GAIN

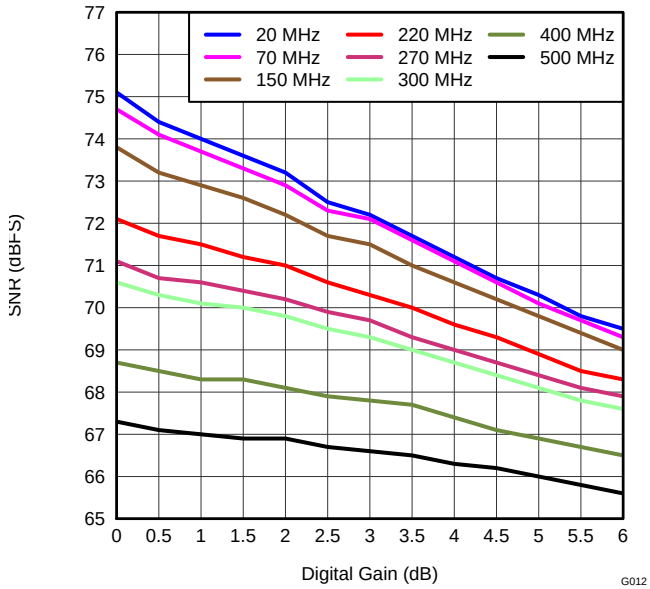

Figure 19. SIGNAL-TO-NOISE RATIO vs DIGITAL GAIN

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TYPICAL CHARACTERISTICS (continued)

At +25°C, AVDD = 1.8 V, AVDD_3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, f_S = 153.6 MSPS, sine-wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, 16-mA CML current, and 32k-point FFT, unless otherwise noted. Note that after reset, the device is in 0-dB gain mode.

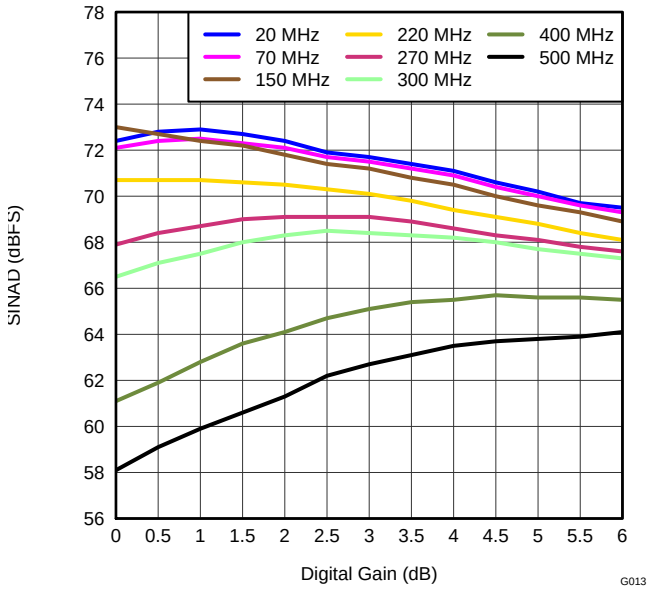

Figure 20. SIGNAL-TO-NOISE AND DISTORTION RATIO vs DIGITAL GAIN

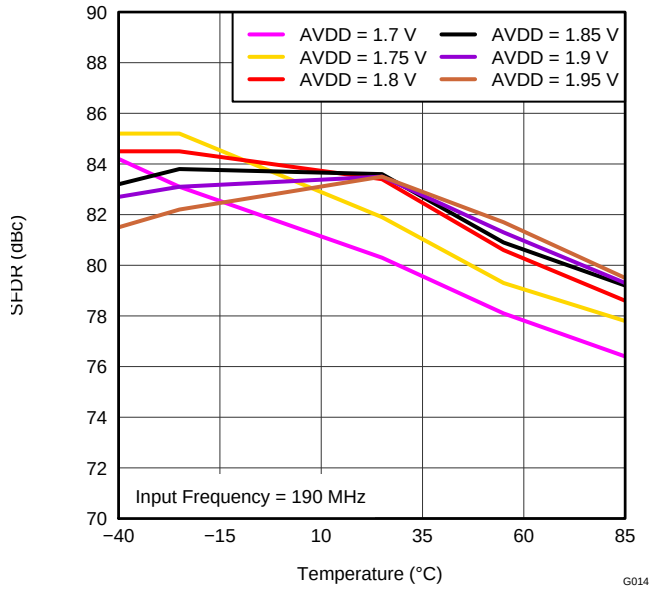

Figure 21. SPURIOUS-FREE DYNAMIC RANGE vs AVDD SUPPLY AND TEMPERATURE

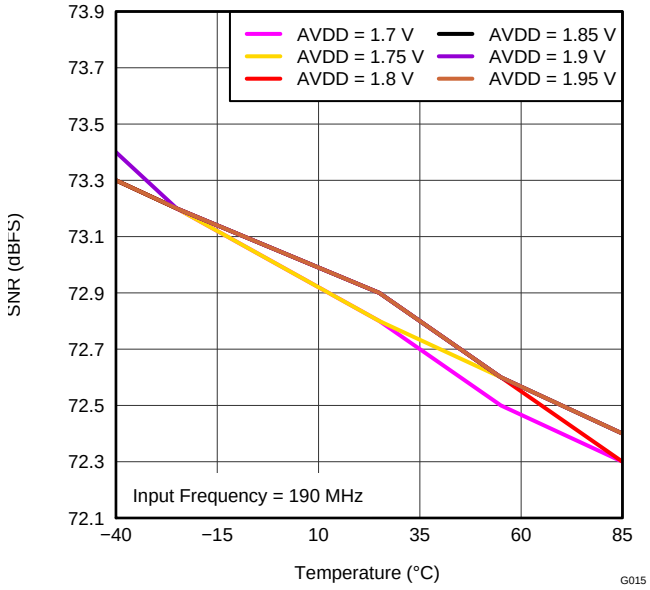

Figure 22. SIGNAL-TO-NOISE RATIO vs AVDD SUPPLY AND TEMPERATURE

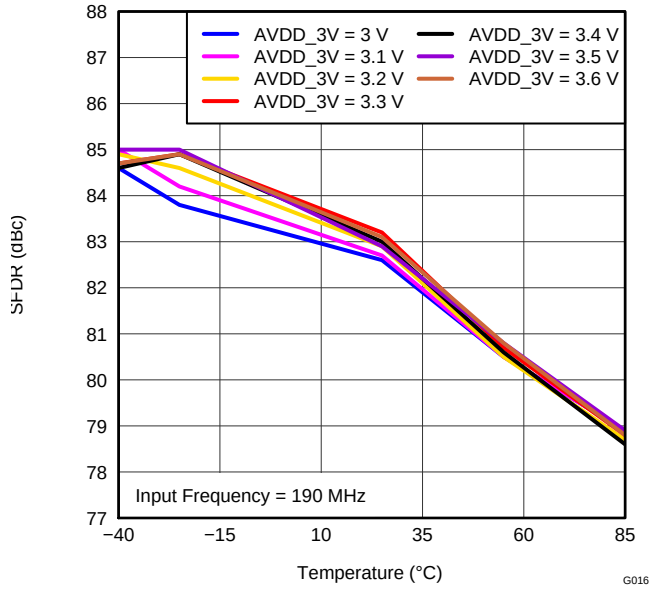

Figure 23. SPURIOUS-FREE DYNAMIC RANGE vs AVDD_3V SUPPLY AND TEMPERATURE

TYPICAL CHARACTERISTICS (continued)

At +25°C, AVDD = 1.8 V, AVDD_3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, f_S = 153.6 MSPS, sine-wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, 16-mA CML current, and 32k-point FFT, unless otherwise noted. Note that after reset, the device is in 0-dB gain mode.

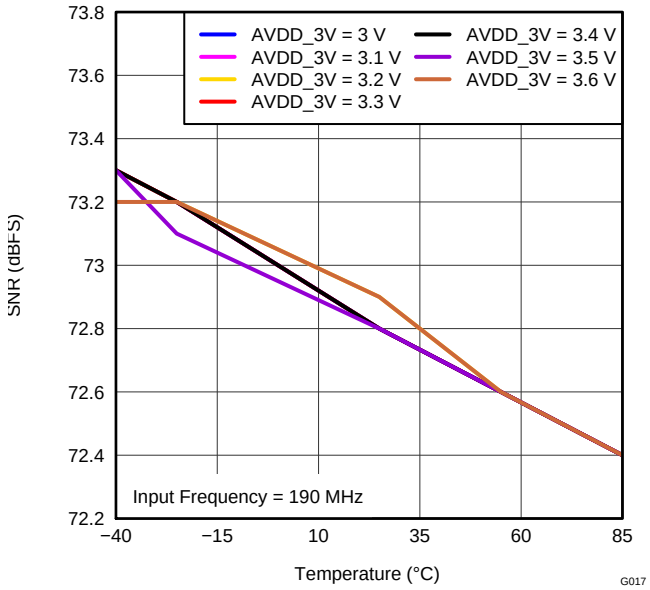

Figure 24. SIGNAL-TO-NOISE RATIO vs AVDD_3V SUPPLY AND TEMPERATURE

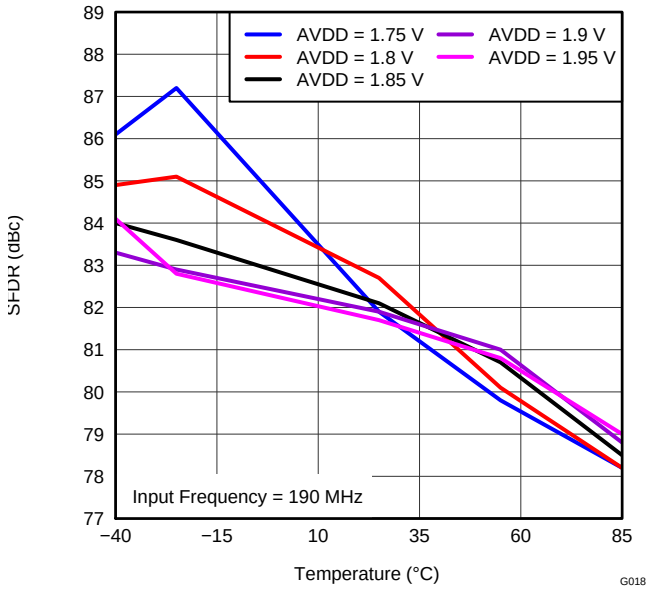

Figure 25. SPURIOUS-FREE DYNAMIC RANGE vs DRVDD SUPPLY AND TEMPERATURE

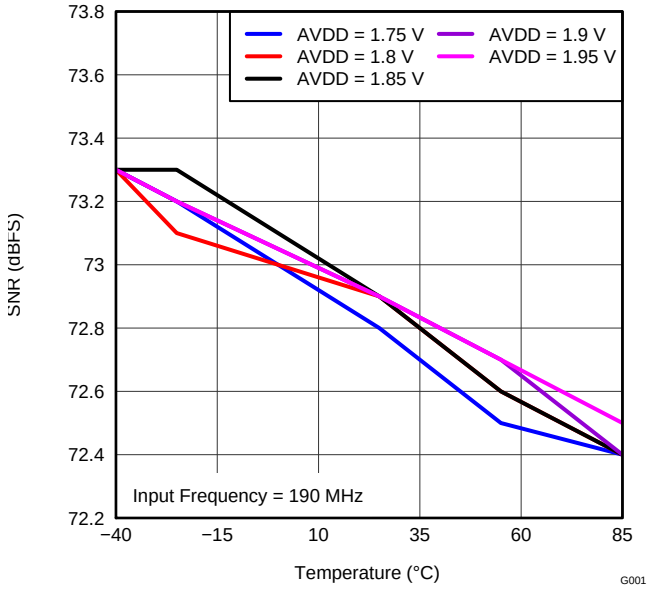

Figure 26. SIGNAL-TO-NOISE RATIO vs DRVDD SUPPLY AND TEMPERATURE

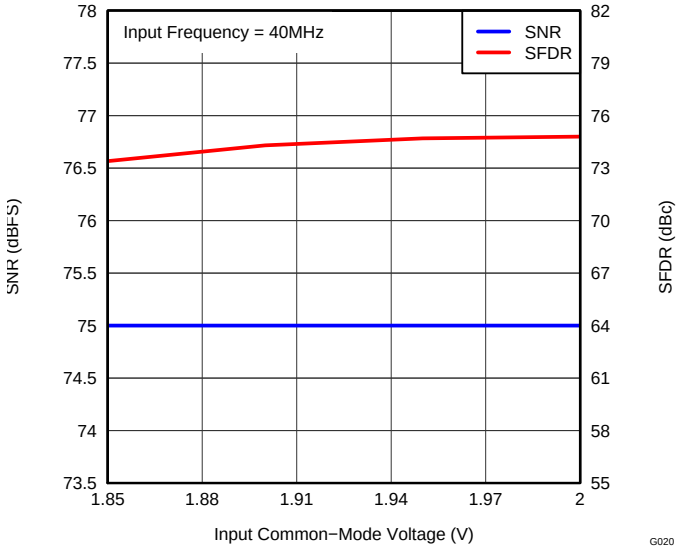

Figure 27. PERFORMANCE vs INPUT COMMON-MODE VOLTAGE

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TYPICAL CHARACTERISTICS (continued)

At +25°C, AVDD = 1.8 V, AVDD_3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, f_S = 153.6 MSPS, sine-wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, 16-mA CML current, and 32k-point FFT, unless otherwise noted. Note that after reset, the device is in 0-dB gain mode.

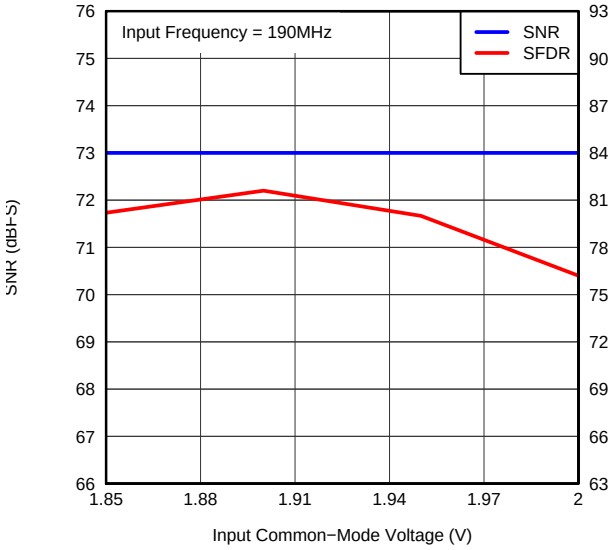

Figure 28. PERFORMANCE vs INPUT COMMON-MODE VOLTAGE

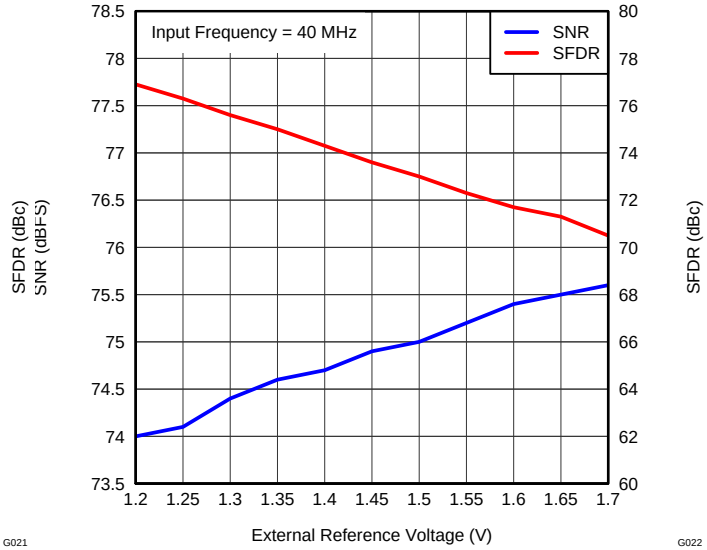

Figure 29. PERFORMANCE vs EXTERNAL REFERENCE VOLTAGE

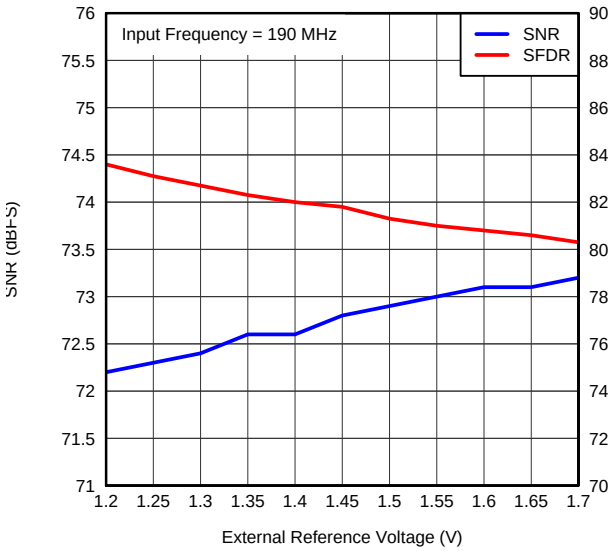

Figure 30. PERFORMANCE vs EXTERNAL REFERENCE VOLTAGE

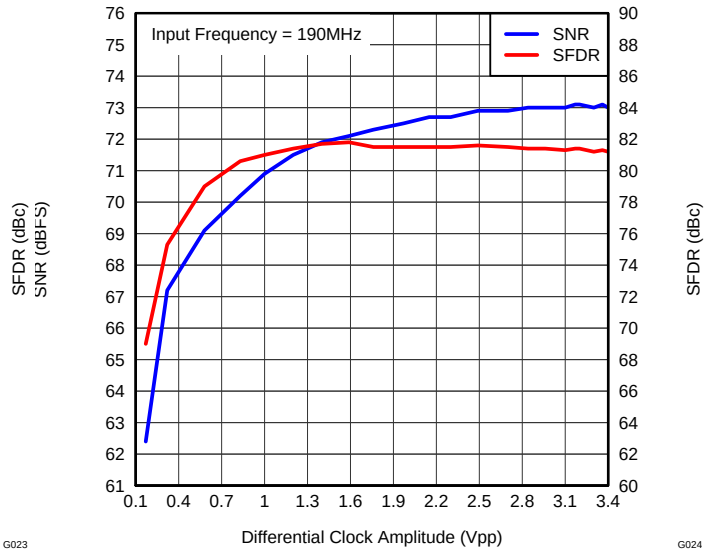

Figure 31. PERFORMANCE vs DIFFERENTIAL CLOCK AMPLITUDE

TYPICAL CHARACTERISTICS (continued)

At +25°C, AVDD = 1.8 V, AVDD_3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, f_S = 153.6 MSPS, sine-wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, 16-mA CML current, and 32k-point FFT, unless otherwise noted. Note that after reset, the device is in 0-dB gain mode.

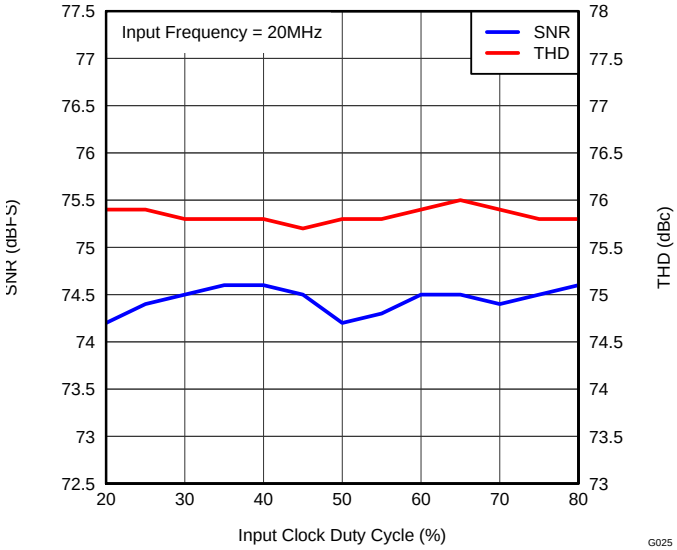

Figure 32. PERFORMANCE vs INPUT CLOCK DUTY CYCLE

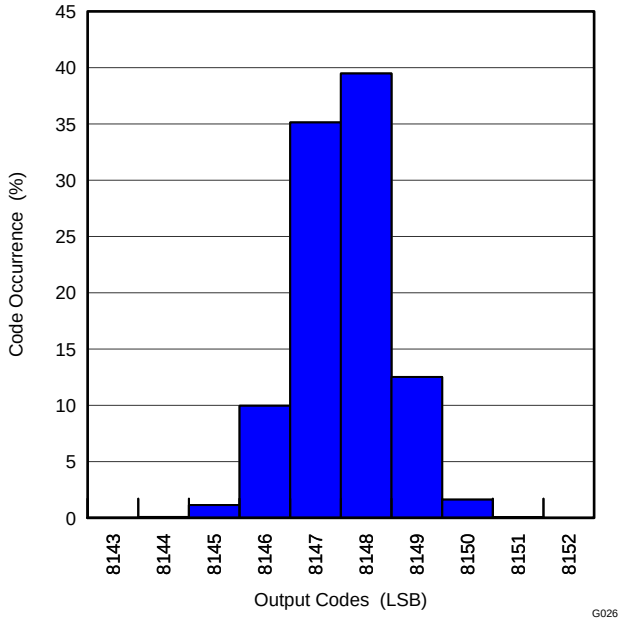

Figure 33. OUTPUT CODES HISTOGRAM WITH IDLE CHANNEL INPUT

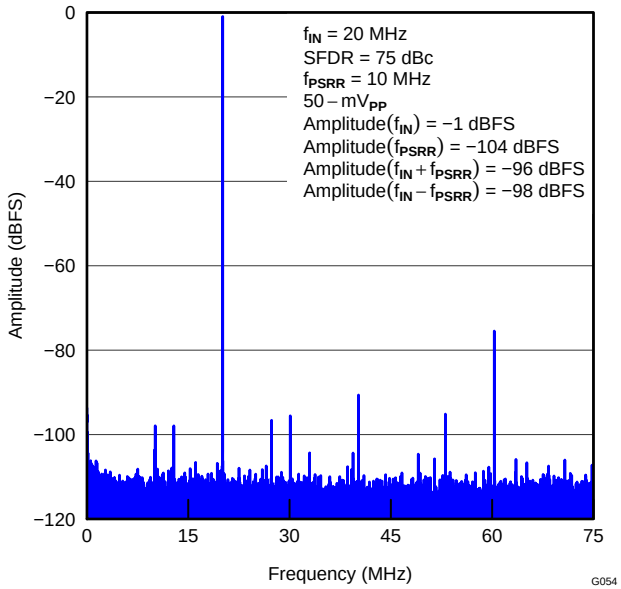

Figure 34. POWER-SUPPLY REJECTION RATIO SPECTRUM FOR AVDD SUPPLY

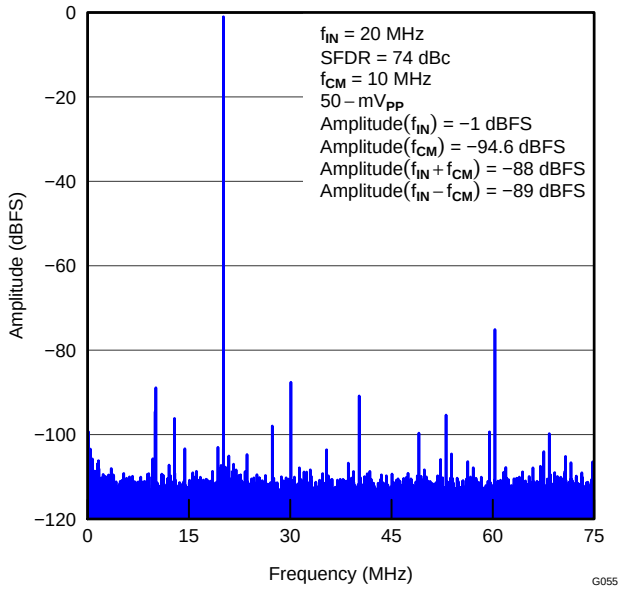

Figure 35. COMMON-MODE REJECTION RATIO SPECTRUM FOR AVDD SUPPLY

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TYPICAL CHARACTERISTICS (continued)

At +25°C, AVDD = 1.8 V, AVDD_3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, f_S = 153.6 MSPS, sine-wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, 16-mA CML current, and 32k-point FFT, unless otherwise noted. Note that after reset, the device is in 0-dB gain mode.

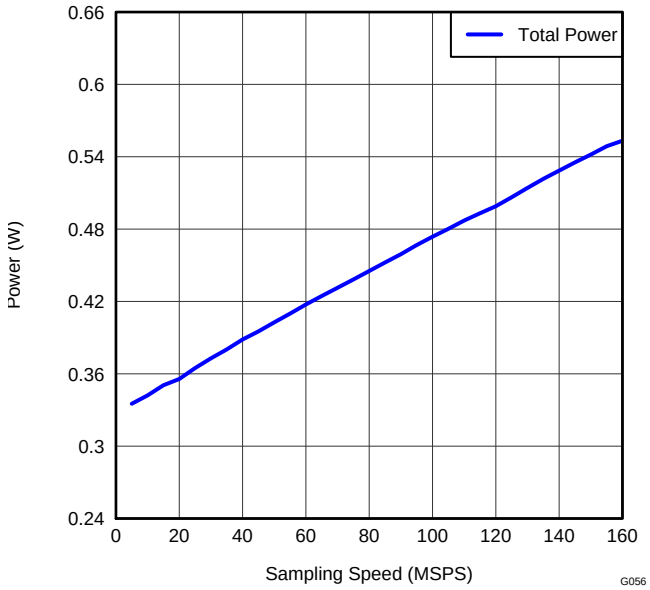

Figure 36. TOTAL POWER vs SAMPLING SPEED

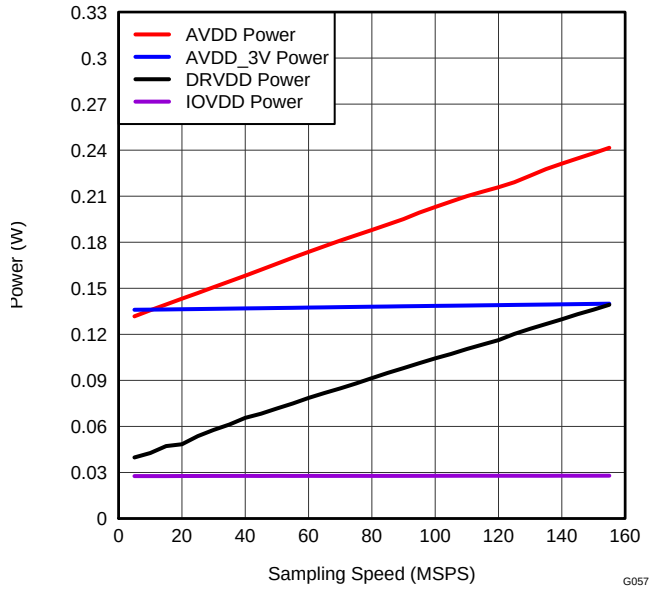

Figure 37. POWER BREAK-UP vs SAMPLING SPEED

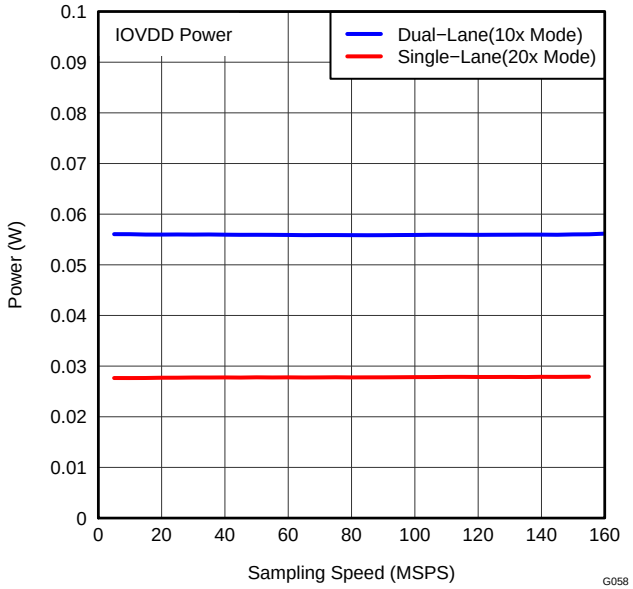

Figure 38. IOVDD POWER vs SAMPLING SPEED

TYPICAL CHARACTERISTICS: CONTOUR

At +25°C, AVDD = 1.8 V, AVDD_3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, f_S = 153.6 MSPS, sine-wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, 16-mA CML current, and 32k-point FFT, unless otherwise noted. Note that after reset, the device is in 0-dB gain mode.

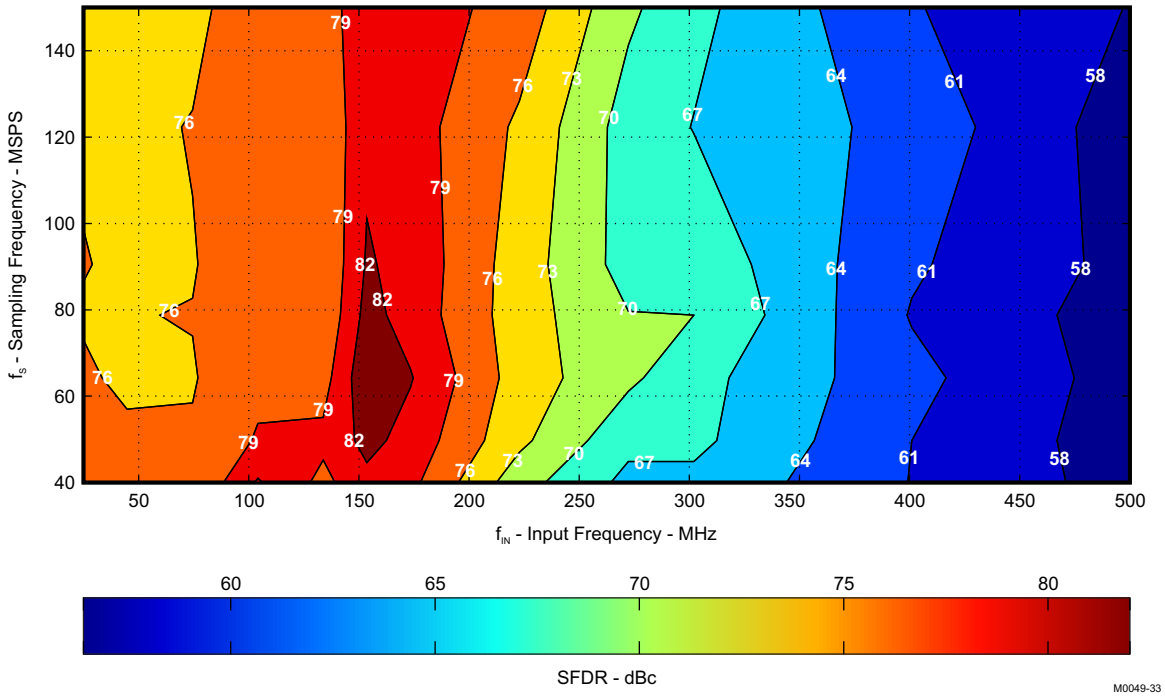

Figure 39. SFDR ACROSS INPUT AND SAMPLING FREQUENCIES

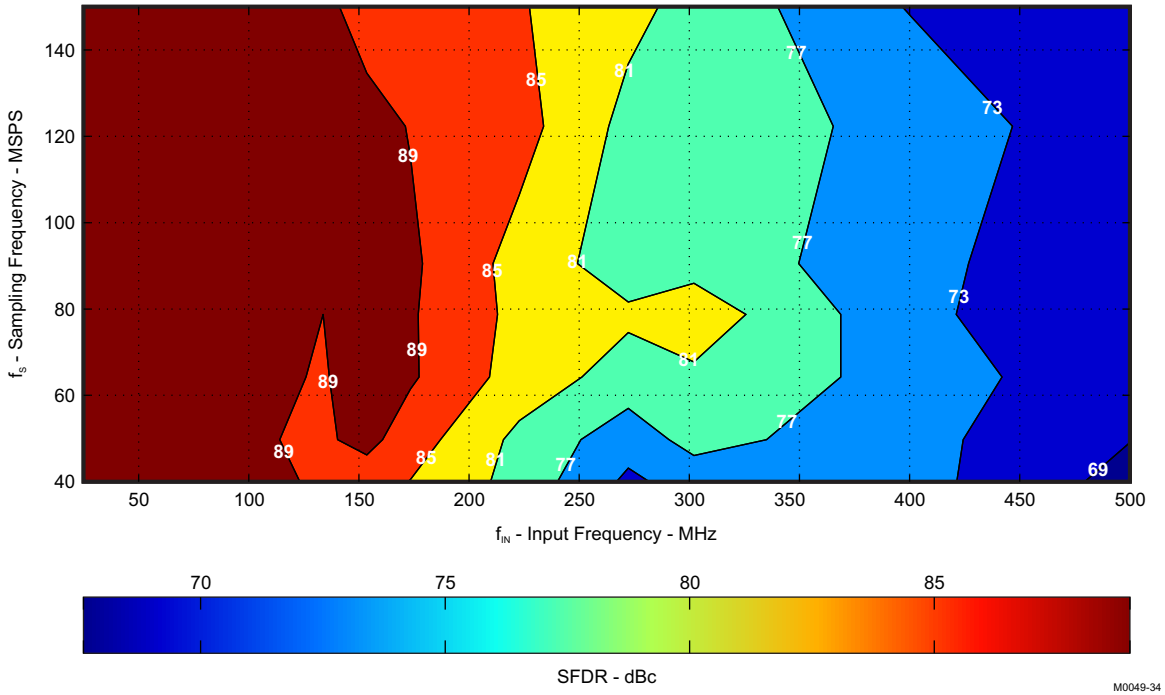

Figure 40. SFDR ACROSS INPUT AND SAMPLING FREQUENCIES (6-dB Gain)

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TYPICAL CHARACTERISTICS: CONTOUR (continued)

At +25°C, AVDD = 1.8 V, AVDD_3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, f_S = 153.6 MSPS, sine-wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, 16-mA CML current, and 32k-point FFT, unless otherwise noted. Note that after reset, the device is in 0-dB gain mode.

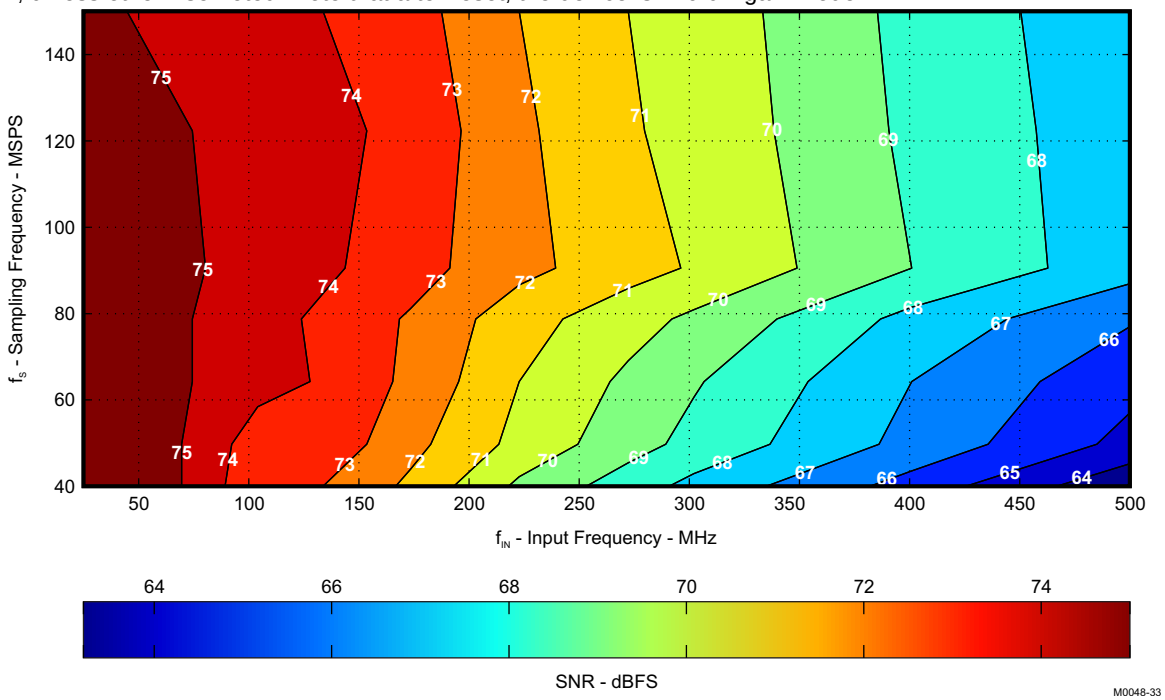

Figure 41. SNR ACROSS INPUT AND SAMPLING FREQUENCIES

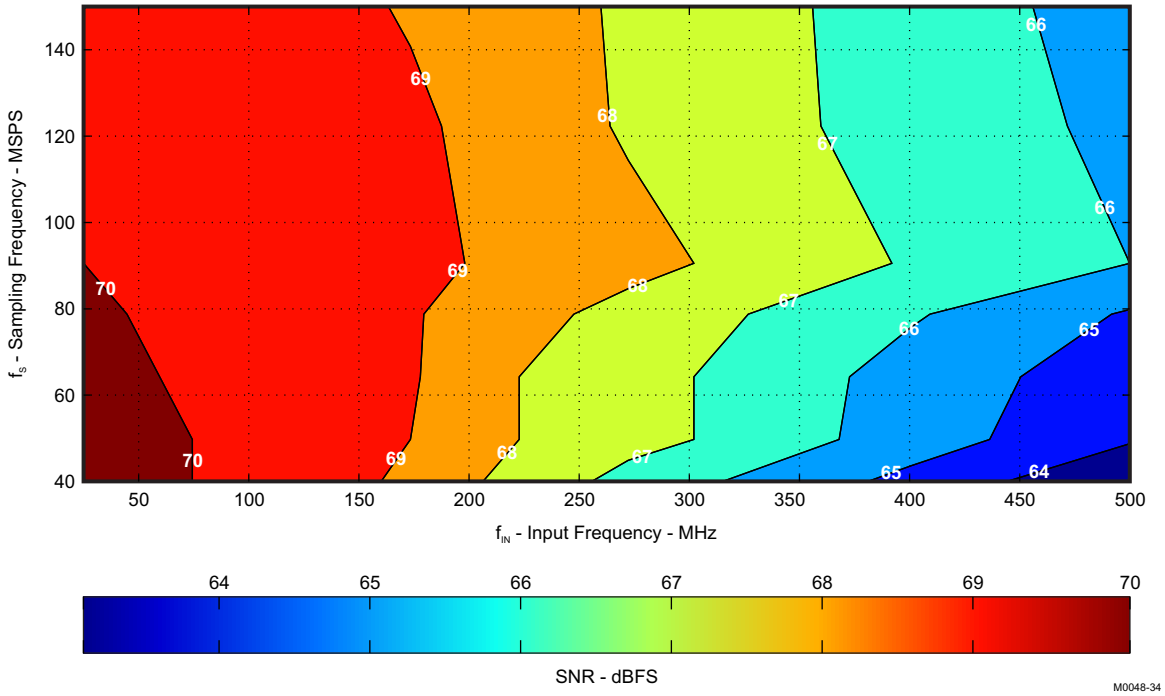

Figure 42. SNR ACROSS INPUT AND SAMPLING FREQUENCIES (6-dB Gain)

DEVICE CONFIGURATION

PARALLEL INTERFACE MODE

The device operates in parallel interface mode when a suitable voltage is applied on the MODE pin, as described in Table 5. In parallel interface mode, the SEN, SDATA, SCLK, and SDOUT pins functionality differs from the serial interface mode. In this mode, the SEN_FALIGN_IDLE and SCLK_SERF0_SCR pins turn into four level-control pins for the JESD interface (as described in Table 6 and Table 7), whereas the SDATA_TEST0 and SDOUT_TEST1 pins turn into 2-level control pins, as described in Table 8.

Table 5. MODE Pin (Pin 19)

MODE	DESCRIPTION
0 +150 mV/–0 mV	Serial interface mode. Pins 23, 24, and 25 are configured as SEN, SDATA, SCLK. Pins 36, 37, 38, and 39 are configured to output either an early-signal estimate or a signal power estimate (selection is based on register settings).
(3/8)AVDD ±150 mV	Do not use
(5/8)AVDD ±150 mV	Parallel interface mode. Pins 23, 24 and 25 are configured as parallel input pins for controlling the JESD204A modes. Pins 36, 37, 38, and 39 always output an early-signal estimate.
AVDD +0 mV/–150 mV	Do not use

Table 6. SEN_FALIGN_IDLE Pin, in Parallel Interface Mode (Pin 23)

SEN_FALIGN_IDLE	DESCRIPTION
0 +150 mV / 0 mV	FALIGN = 0, IDLE = 0
(3/8) AVDD ±150 mV	FALIGN = 1, IDLE = 0
(5/8) AVDD ±150 mV	FALIGN = 1, IDLE = 1
AVDD 0 mV / –150 mV	FALIGN = 0, IDLE = 1

Key:

FALIGN: When the last octet of the current frame is the same as the last octet of the previous frame, then FALIGN determines whether the last octet of the current frame is transmitted as is, or if the last octet is replaced by a K28.7 control symbol.
0 = Last octet transmitted as is
1 = Last octet is replaced with a K28.7 control symbol

IDLE: IDLE determines the synchronization characters transmitted during and immediately after a SYNC event.
0 = The device transmits K28.5 as per the JESD204A specification
1 = The device alternately transmits K28.5 and D5.6/D16.2 characters as per the IEEE standard 802.3-2002 (part 3, clause 36.2.4.12). This setting is the case for both single- and dual-lane modes.

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Table 7. SCLK_SERF0_SCR Pin, in Parallel Interface Mode (Pin 25)

SCLK_SERF0_SCR	DESCRIPTION
0 +150 mV / 0 mV	SERF0 = 0, SCR = 0
(3/8) AVDD ±150 mV	SERF0 = 1, SCR = 0
(5/8) AVDD ±150 mV	SERF0 = 1, SCR = 1
AVDD 0 mV / –150 mV	SERF0 = 0, SCR = 1

Key:

SERF0: Output serialization factor.
0 = The device transmits two octets per frame (an entire ADC channel in a single lane) with an output serialization factor of 20
1 = The device transmits one octet per frame (one ADC channel over two lanes) with an output serialization factor of 10

SCR: 0 = Scrambling disabled
1 = Scrambling enabled (as per JESD204A)

Table 8. SDATA_TEST0 and SDOUT_TEST1 Pins, in Parallel Interface Mode (Pins 24 and 28)

TEST1	TEST0	MODE
0	0	Normal mode. JESD204A encoder input is ADC data.
0	1	JESD204A encoder input is B5B5. Output is a stream of D21.5 (alternating 1s and 0s).
1	0	JESD204A encoder input is FF00.
1	1	JESD204A encoder input is a pseudo random pattern $1 + X^{14} + X^{15}$ (regardless of whether the scrambler is enabled or not).

SERIAL INTERFACE

The analog-to-digital converter (ADC) has a set of internal registers that can be accessed by the serial interface formed by the serial interface enable (SEN), serial interface clock (SCLK), and serial interface data (SDATA) pins. Serially shifting bits into the device is enabled when SEN is low. SDATA serial data are latched at every SCLK falling edge when SEN is active (low). The serial data are loaded into the register at every 16th SCLK falling edge when SEN is low. If the word length exceeds a multiple of 16 bits, the excess bits are ignored. Data can be loaded in multiples of 16-bit words within a single active SEN pulse.

The first eight bits form the register address and the remaining eight bits are the register data. The interface can function with SCLK frequencies from 20 MHz down to very low speeds (of few Hertz) and also with a non-50% SCLK duty cycle.

Register Initialization

After power-up, the internal registers must be initialized to the default values. This initialization can be accomplished in one of two ways:

1. Either through a hardware reset by applying a high-going pulse on RESET pin (of widths greater than 10 ns), as shown in Figure 43,

   or

2. By applying a software reset. Using the serial interface, set the S_RESET bit (bit D1 in register 00h) high. This setting initializes the internal registers to the default values and then self-resets the S_RESET bit low. In this case, the RESET pin is kept low.

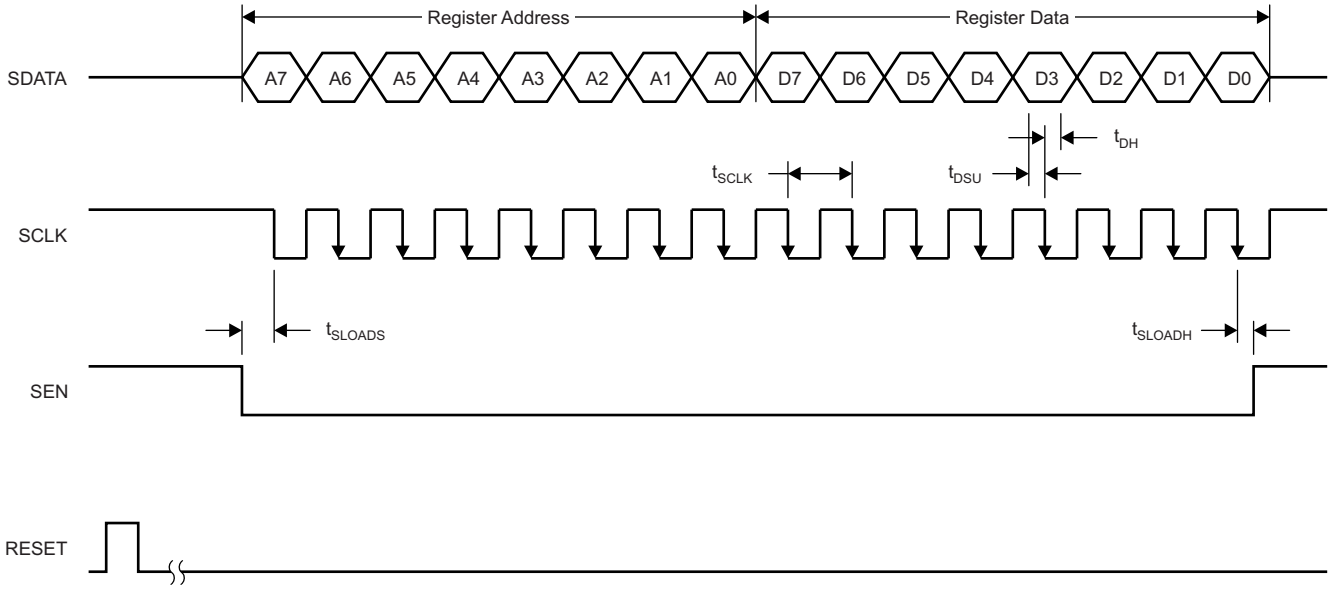

Figure 43. Serial Interface Timing Diagram

Table 9. Timing Characteristics for Figure 43(1)

PARAMETER		MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK frequency (= 1/ t_{SCLK})	> DC		20	MHz
t_{SLOADS}	SEN to SCLK setup time	25			ns
t_{SLOADH}	SCLK to SEN hold time	25			ns
t_{DS}	SDATA setup time	25			ns
t_{DH}	SDATA hold time	25			ns

(1) Typical values are at T_A = +25°C, minimum and maximum values are across the full temperature range of T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.8 V, AVDD_3V = 3.3 V, DRVDD = 1.8 V, and IOVDD = 1.8 V, unless otherwise noted.

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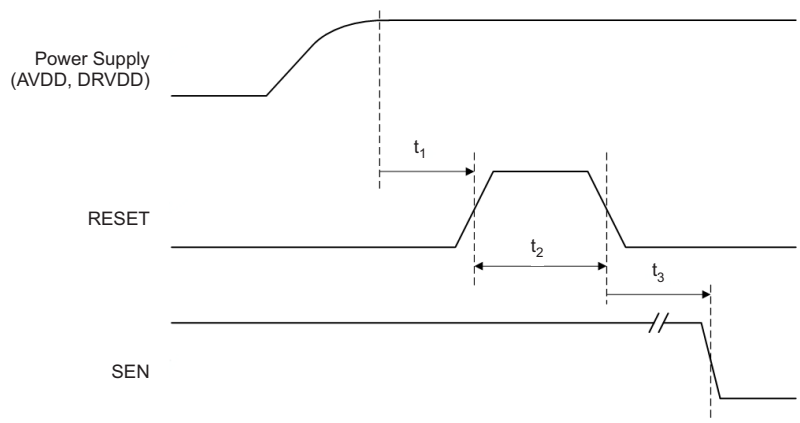
Serial Register Readout

The device includes an option where the contents of the internal registers can be read back. This readback may be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC.

1. First, set the SERIAL_READOUT register bit = 1. This setting also disables any further register writes (except for writes to the SERIAL_READOUT register bit).
2. Initiate a serial interface cycle specifying the address of the register (A[7:0]) whose content must be read.
3. The device outputs the contents (D[7:0]) of the selected register on the SDOUT_TEST1 pin.
4. The external controller latches the contents at the SCLK falling edge.
5. To enable register writes, reset the SERIAL_READOUT register bit = 0.

Reset Timing

Figure 44 shows a reset timing diagram.



NOTE: A high-going pulse on the RESET pin is required for initialization through a hardware reset.

Figure 44. Reset Timing Diagram

Table 10. Timing Characteristics for Figure 44(1)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Power-on delay	Delay from power-up of AVDD and DRVDD to RESET pulse active		1		ms
t_2	Reset pulse duration	Pulse duration of the active RESET signal that resets the serial registers	10			
t_3	Serial interface delay	Delay from RESET disable to SEN active	100			ns

(1) Typical values are at T_A = +25°C and minimum and maximum values are across the full temperature range of T_{MIN} = –40°C to T_{MAX} = +85°C, unless otherwise noted.

SERIAL INTERFACE REGISTER MAP

REGISTER BIT NAME	BIT LOCATION		DESCRIPTION
	ADDRESS (Hex)	BIT	
S_RESET	00	1	Software reset. This mode has the same function as a hardware reset.
SERIAL_READOUT	00	0	0 = Serial interface write (default) 1 = Serial readout
HIGH_SFDR_MODE	02	6:4, 0	Set these bits to obtain the best HD3 when the input frequency is between 150 MHz to 250 MHz.
DFS_OVERRIDE	3C	7	This bit provides the override control mode for the DFS_EXTREF pin when controlling the DFS select mode. This bit controls the DFS_EXTREF pin with the DFS_REG register bit. 0 = DFS functionality determined by DFS_EXTREF pin 1 = DFS functionality determined by DFS_REG pin
DFS_REG	3C	6	This bit is the register bit for DFS control. 0 = Output format is twos complement. 1 = Output format is offset binary. This setting takes effect when DFS_OVERRIDE is set to '1'.
CUSTOM_PAT[13:6]	3E	7:0	Eight MSBs of the 14-bit custom pattern can be programmed.
CUSTOM_PAT[5:0]	3F	7:2	Six LSBs of the 14-bit custom pattern can be programmed.
INT_REF_OVERRIDE	44	3	This bit is the override control for DFS_EXTREF pin when controlling the internal/external reference select mode. This bit controls the DFS_EXTREF pin with the INT_REF_REG register bit. 0 = Internal/external reference mode is determined by the DFS_EXTREF pin 1 = Internal/external reference mode is determined by the INT_REF_REG
INT_REF_REG	44	2	This bit is the register bit for internal/external reference mode control. 0 = Internal reference mode. 1 = External reference mode. This setting takes effect when INT_REF_OVERRIDE is set to '1'.
S_PDN	44	6	Software power-down.
FINE_GAIN[3:0]	45	7:4	0-dB to 6-dB digital gain in 0.5-dB steps (default gain is 0 dB). Refer to the *Fine-Gain Control* section for further details.
BYPASS_FINE_GAIN	45		Digital gain bypass. Digital gain is enabled by default. When this bit set to '1', digital gain (fine gain) is bypassed.
ADC_TEST_PAT[2:0]	45	2:0	These bits control the output test patterns. 000 = ADC output data bus is input to JESD204A encoder block 001 = ADC bus is replaced by the minimum code (*00000000000000* in offset binary). 010 = ADC bus replaced by the maximum code (*11111111111111* in offset binary). 100 = ADC bus replaced by a ramping code pattern that increments by 1 LSB every four clocks (and folds back to the minimum code when the maximum code is reached). 101 = ADC bus is replaced by custom patterns. The patterns are programmed by registers 3E and 3F. 011, 110, 111 = Do not use
TXMIT_LINKDATA_EN	A0	0	0 = Initial lane alignment sequence is not transmitted (default) 1 = Initial lane alignment sequence (as per JESD204A) is sent after the code group sync in both single- and dual-lane interfaces
S_FALIGN	A0	1	Software Frame Align control. This bit enables frame alignment monitoring. When scrambling is enabled and this bit is '1', this bit is encoded as K28.7 when the last scrambled octet in a frame equals FC. S_FALIGN bit control is similar to the FALIGN pin control. When this bit is 0 = There is no replacement. 1 = When scrambling is off, if the last octet in the previous frame is the same as the last octet in the current frame, then the last octet in the current frame is replaced with a frame alignment symbol K28.7
MFALIGN	A0	2	Multiframe align control. This bit functions similarly to S_FALIGN, but refers to multiframe instead. The multiframe alignment symbol is K28.3.

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REGISTER BIT NAME	BIT LOCATION		DESCRIPTION
	ADDRESS (Hex)	BIT	
FLIP_ADC_BUS	A0	3	By default, the last octet in the frame is derived from the data octet on the LSB side. The occurrence of consecutive *last octets* may be rare because the LSB octets usually switch more (frame-to-frame) than the MSB octets. This condition can lead to an infrequent occurrence of frame alignment symbols. To increase the rate of consecutive last octets (and thereby the rate of frame and multiframe alignment symbols), this bit can be set to '1'. Setting this bit to '1' flips the bit order of the ADC inputs (N bits) to the JESD204A logic. Note that the two zeros padded at the end to cause the JESD204A logic input to remain unchanged.
TESTMODE_EN	A0	4	This bit enables the transmission of the test sequence mentioned in the JESD204A document.
S_IDLE	A0	5	Software idle generation control. Normally the output during code group synchronization is K28.5. When S_IDLE is set to '1', the device output is a K28.5 comma followed by either a D5.6 or a D16.2 alignment symbol. This configuration is as per IEEE standard 802.3-2002 (part 3, clause 36.2.4.12) and enables compatibility with TI's TLK family of devices. This bit control is similar to the IDLE pin control (see Table 6).
S_TEST0	A0	6	These two bit controls are similar to the TEST1 and TEST0 pin controls.
S_TEST1	A0	7	
CTRL_F	A1	0	This bit enables writes into register A6h, bits 7:0.
CTRL_K	A1	1	This bit enables writes into register A7h, bits 4:0.
S_SCR	A5	7	Software scrambling enable. This bit control is similar to the SCR pin control.
F[7:0]	A6	7:0	These bits control the number of octets per frame. Default is set to 00000001 (2 – 1), which is two octets per frame (single-lane mode). For a two-lane output (one octet per frame), set these bits to 00000000. Note that in order to override default, CTRL_F must be set to '1'.
K[4:0]	A7	4:0	These bits control the number of frames per each multiframe (minus 1). Default depends on value of bits F[7:0]. When F = 0 (10x mode), K = 16 (17 frames per multiframe) When F = 1 (20x mode), K = 8 (nine frames per multiframe) Note that to override the default value of bits K[4:0], CTRL_K must be set to '1'. When CTRL_K is set to '1', the value programmed in bits A7[4:0] denotes the number of frames per multiframe (minus 1). For example, to set the number of frames per multiframe to 23, set CTRL_K = 1 and A7[4:0] = 10110.
CML_I[3:0]	B0	3:0	CML buffer current select. Default (0000) is 16 mA. Current is calculated as: 16 mA +16 mA × bit 3 – 8 mA × bit 2 – 4 mA × bit 1 – 2 mA × bit 0
FORCE_OUT_LANE1	B4	3	This bit replaces the output of the 8b/10b coder (corresponding to the MSB octet) with a 10-bit word specified in the OUT_WORD_LANE1[9:0] bits.
OUT_WORD_LANE1[9:0]	B6	7:0	These bits are a 10-bit word replacing the output of the 8b/10b coder when FORCE_OUT_LANE1 is set to '1'.
	B7	7:6	
FORCE_OUT_LANE2	B4	6	This bit replaces the output of the 8b/10b coder (corresponding to the LSB octet) with a 10-bit word specified in the OUT_WORD_LANE2[9:0] bits.
OUT_WORD_LANE2[9:0]	B8	7:4	These bits are a 10-bit word replacing the output of the 8b/10b coder when FORCE_OUT_LANE2 is set to '1'.
	B9	7:2	
EN_SIG_EST	D6	0	This bit outputs a 4-bit ADC code with low latency on the DETECT[3:0] bits.
EN_PWR_EST	D6	5	This bit outputs a 4-bit average power estimate of the input signal on the DETECT[3:0] bits. Power estimate is in dB scale in steps of approximately 1 dB. Refer to the *Signal Power Estimation* section.
SAMPLES_PWR_EST[2:0]	D6	4:2	These bits determine the number of samples to average for power estimation. These bits are programmable from 1K to 16K.

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REGISTER MODES

A brief summary of different register modes and respective locations in the digital processing flow of the ADS61JB46 is shown in Figure 45 and Figure 46.

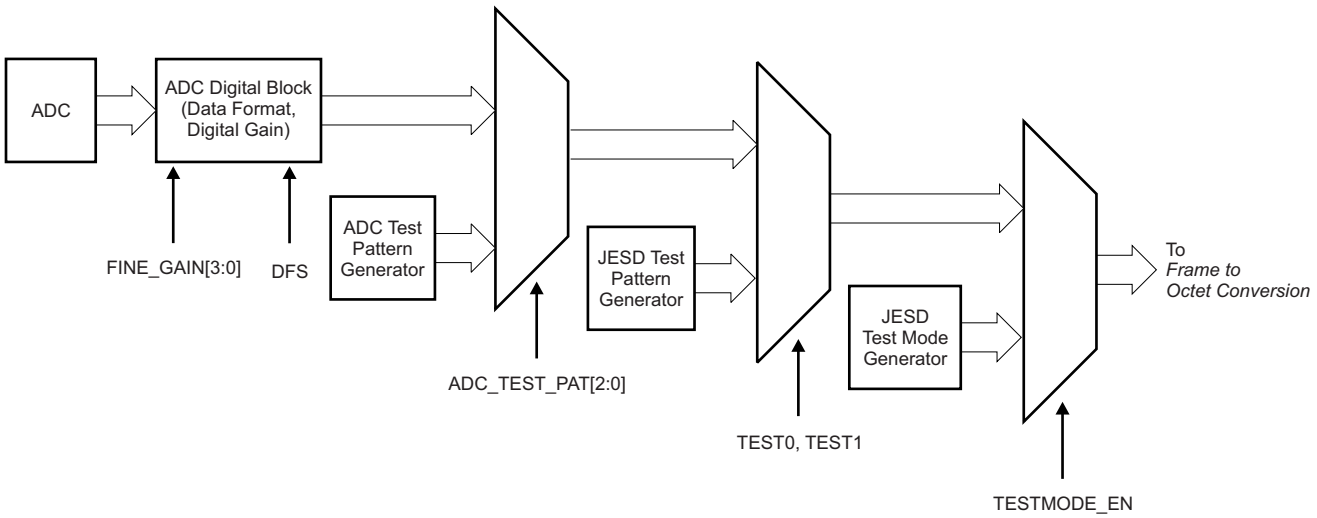

Figure 45. Register Modes Before Frame to Octet Conversion Block

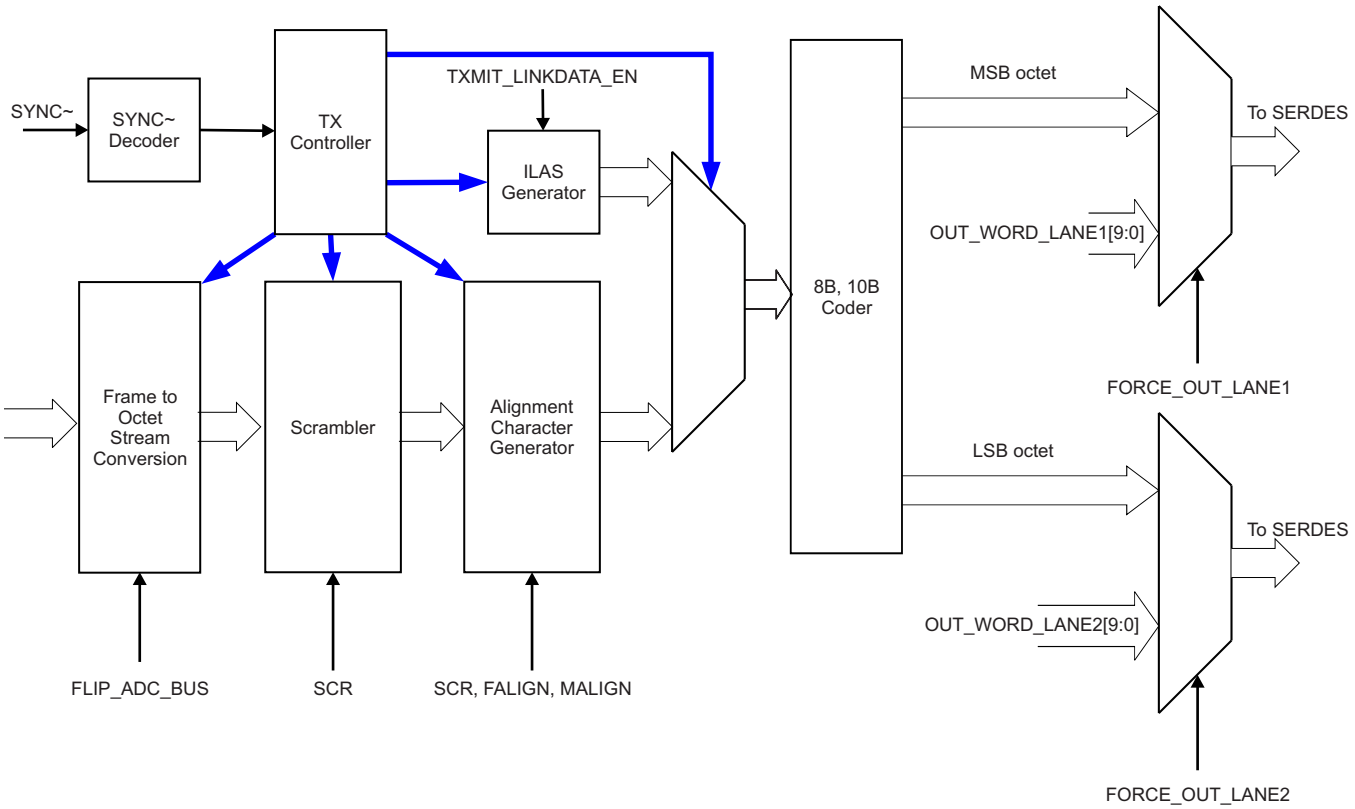

Figure 46. Register Modes After Frame to Octet Conversion Block

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INITIAL LANE ALIGNMENT SEQUENCE

By default, the initial lane alignment sequence is not transmitted. To enable transmission of the initial lane alignment sequence, for the two settings of F, the mapping of the link configuration fields to octets of the JESD204A specification is shown in Table 11.

Table 11. Link Configuration Fields Mapping to Octets

CONFIGURATION OCTET NO.	MSB	6	5	4	3	2	1	LSB
F = 1 (20x Mode)								
0	DID[7:0] = 00000000							
1	X	X	X	X	BID[3:0] = 0000			
2	X	X	X	LID[4:0] = 00000				
3	SCR[0], set by S_SCR	X	X	L[4:0] = 00000				
4	F[7:0] = 00000001							
5	X	X	X	K[4:0] = 01000 (or programmed value of A7[4:0] if CTRL_K = 1)				
6	M[7:0] = 00000000							
7	CS[1:0] = 00		X	N[4:0] = 01101				
8	X	X	X	N'[4:0] = 01111				
9	X	X	X	S[4:0] = 00000				
10	HD[0] = 0	X	X	CF[4:0] = 00000				
11	RES1[7:0], set to all 0s							
12	RES2[7:0], set to all 0s							
13	FCHK[7:0]							
F = 0 (10x Mode)								
0	DID[7:0] = 00000000							
1	X	X	X	X	BID[3:0] = 0000			
2	X	X	X	LID[4:0] = 00000 for lane 1 and 00001 for lane 2				
3	SCR[0], set by S_SCR	X	X	L[4:0] = 00001				
4	F[7:0] = 00000000							
5	X	X	X	K[4:0] = 10000 (or programmed value of A7[4:0] if CTRL_K = 1)				
6	M[7:0] = 00000000							
7	CS[1:0] = 00		X	N[4:0] = 01101				
8	X	X	X	N'[4:0] = 01111				
9	X	X	X	S[4:0] = 00000				
10	HD[0] = 0	X	X	CF[4:0] = 00000				
11	RES1[7:0], set to all 0s							
12	RES2[7:0], set to all 0s							
13	FCHK[7:0]							

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APPLICATION INFORMATION

THEORY OF OPERATION

The ADS61JB46 is a buffered analog input, ultralow power ADC with maximum sampling rates up to 160 MSPS. The conversion process is initiated by a rising edge of the external input clock and the analog input signal is also sampled. The sampled signal is sequentially converted by a series of small-resolution stages, with the outputs combined in a digital correction logic block. At every clock edge the sample propagates through the pipeline, resulting in a data latency of 20 clock cycles. The output is available as 14-bit data, coded in either straight offset binary or binary twos complement format, with a JESD207A interface in CML logic levels.

ANALOG INPUTS

The analog input pins have analog buffers (running off of the AVDD3V supply) that internally drive the differential sampling circuit. As a result of the analog buffer, the input pins present high input impedance to the external driving source (10-kΩ dc resistance and 3-pF input capacitance). The buffer helps isolate the external driving source from the switching currents of the sampling circuit. This buffering makes driving buffered inputs easier when compared to an ADC without the buffer.

The input common-mode is set internally using a 5-kΩ resistor from each input pin to 1.95 V, so the input signal can be ac-coupled to the pins. Each input pin (INP, INM) must swing symmetrically between (VCM + 0.5 V) and (VCM – 0.5 V), resulting in a 2-V_{PP} differential input swing.

The input sampling circuit has a high 3-dB bandwidth that extends up to 450 MHz (measured from the input pins to the sampled voltage). Figure 47 shows an equivalent circuit for the analog input.

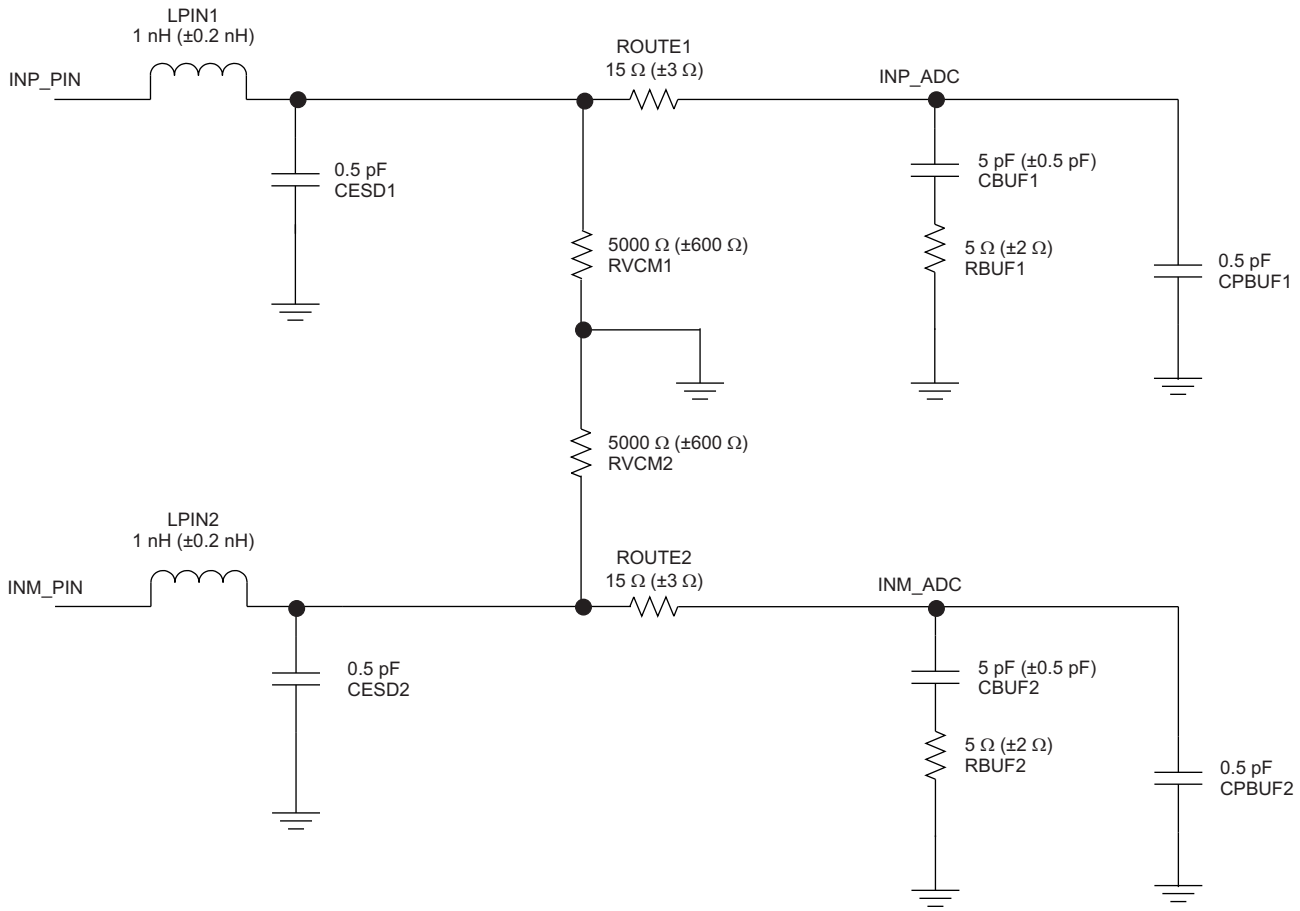

Figure 47. Analog Input Equivalent Circuit

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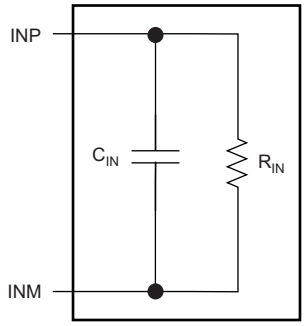
DRIVE CIRCUIT REQUIREMENTS

For optimum performance, the analog inputs must be driven differentially. This technique improves the common-mode noise immunity and even-order harmonic rejection. A small resistor (5 Ω) in series with each input pin is recommended to damp out ringing caused by package parasitics.

Figure 48 and Figure 49 show the differential impedance ($Z_{IN} = R_{IN} || C_{IN}$) at the ADC input pins. The presence of the analog input buffer results in an almost constant input capacitance up to 1 GHz.



Note that at frequency (f), the real part of input impedance (input resistance) = R_{IN}, the imaginary part of input impedance = 1 / (2 × πF × C_{IN}), and input capacitance = C_{IN}.

Figure 48. Analog Input Equivalent Impedance Model

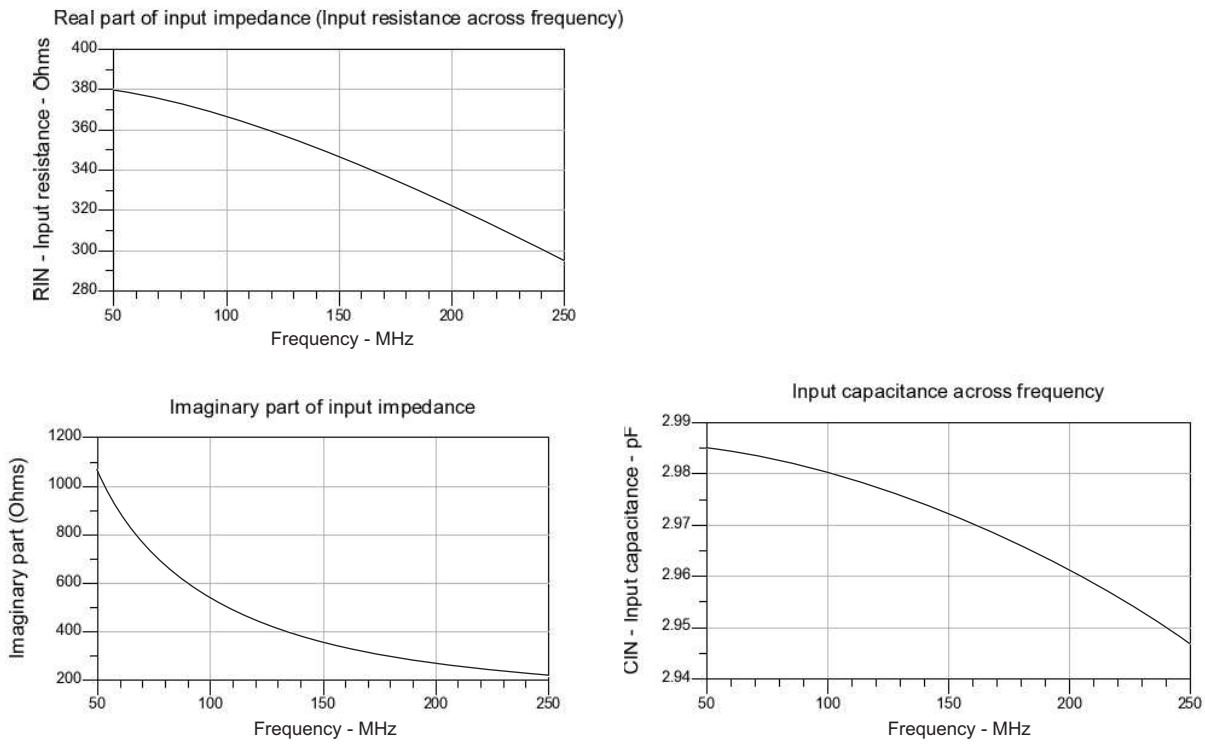


Figure 49. R_{IN} and C_{IN} versus Frequency

EXAMPLE DRIVING CIRCUITS

Two example driving circuit configurations are shown in Figure 50 and Figure 51, one optimized for low input frequencies and the other for high input frequencies. The presence of internal analog buffers makes the ADS61JB46 simple to drive by absorbing any ADC kick-back noise. The mismatch in the transformer parasitic capacitance (between the windings) results in degraded even-order harmonic performance. Connecting two identical RF transformers back-to-back helps minimize this mismatch and good performance is obtained in the input frequency range of interest.

The drive circuit for low input frequencies (< 200 MHz) in Figure 50 uses two back-to-back connected ADT1-1 transformers terminated by 50 Ω near the ADC side. An additional termination resistor pair may be required between the two transformers to improve even-order harmonic performance, as shown in drive circuit for high input frequencies (> 200 MHz) in Figure 51. The center point of this termination is connected to ground to improve the balance between the P (positive) and M (negative) sides. The example circuit in Figure 51 uses two back-to-back connected ADTL2-18 transformers with a 200-Ω termination between them and a secondary 100 Ω at the second transformer to obtain an effective 50 Ω (for a 50-Ω source impedance). The ac-coupling capacitors allow the analog inputs to self-bias around the required common-mode voltage.

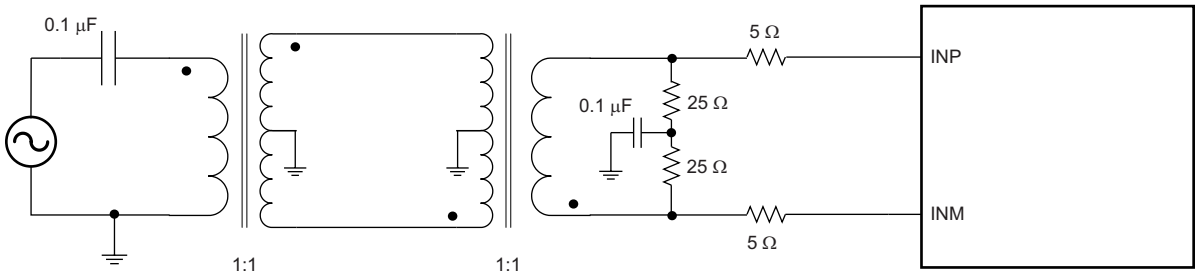


Figure 50. Drive Circuit with Low Bandwidth (for Low Input Frequencies)

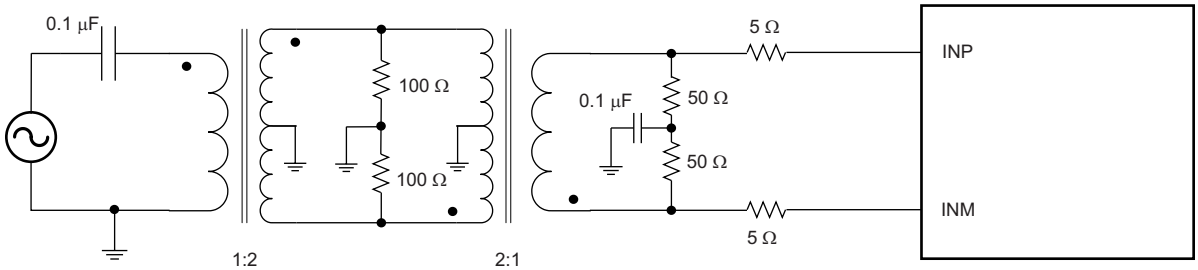


Figure 51. Drive Circuit with High Bandwidth (for High Input Frequencies)

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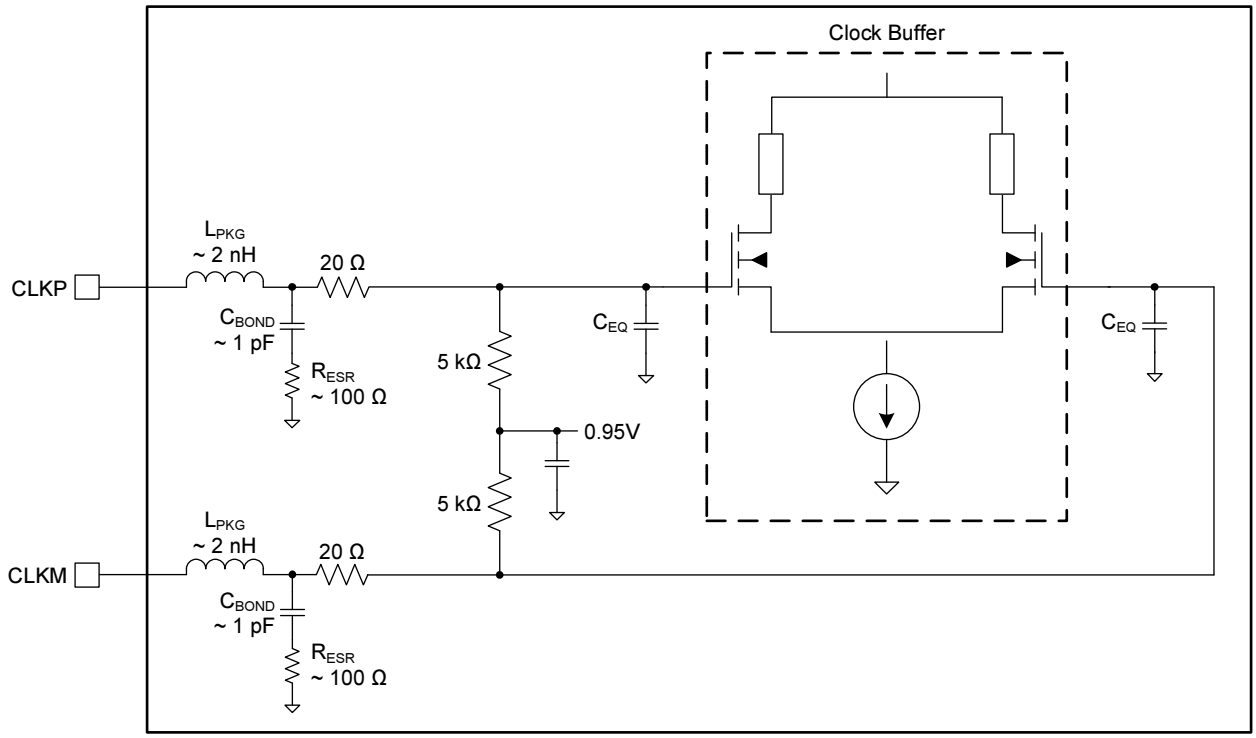
CLOCK INPUT

The ADS61JB46 clock inputs can be driven differentially by a sine, LVPECL, or LVDS source with little or no difference in performance between them. The common-mode voltage of the clock inputs is set to 0.95 V using internal 5-kΩ resistors, as shown in Figure 52. This setting allows the use of transformer-coupled drive circuits for a sine-wave clock or ac-coupling for LVPECL and LVDS clock sources (see Figure 53, Figure 54, and Figure 55). For best performance, the clock inputs must be driven differentially, thereby reducing susceptibility to common-mode noise. TI recommends keeping the differential voltage between clock inputs less than 1.8 V_{PP} to obtain best performance. For high input frequency sampling, TI recommends using a clock source with very low jitter. Band-pass filtering of the clock source can help reduce the effects of jitter. There is no change in performance with a non-50% duty cycle clock input.



NOTE: C_{EQ} is 1 pF to 3 pF and is the equivalent input capacitance of the clock buffer.

Figure 52. Internal Clock Buffer

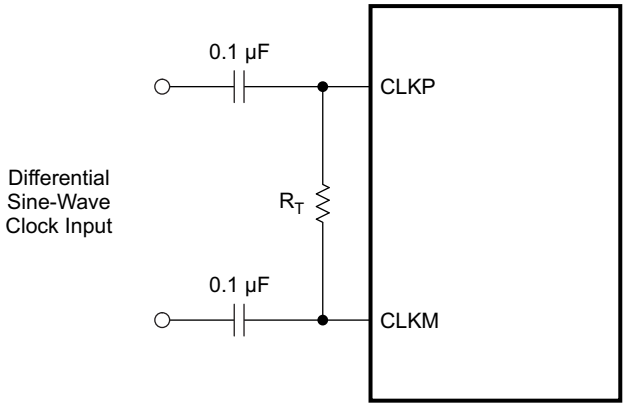


Figure 53. Differential Sine-Wave Clock Driving Circuit

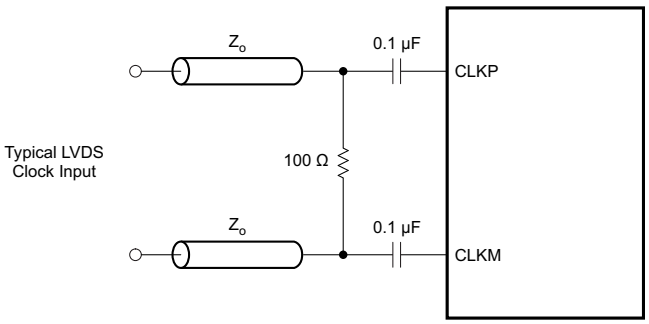


Figure 54. LVDS Clock Driving Circuit

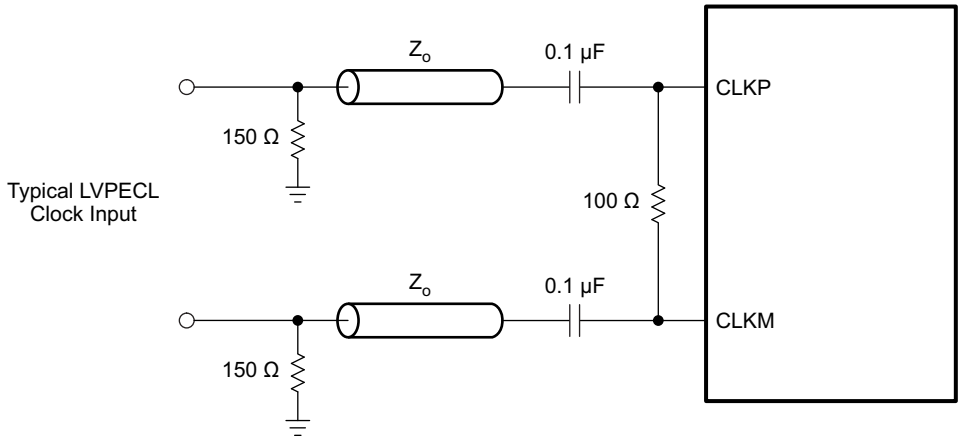


Figure 55. LVPECL Clock Driving Circuit

FINE-GAIN CONTROL

The ADS61JB46 includes gain settings that can be used to obtain improved SFDR performance (compared to no gain). The gain is programmable from 0 dB to 6 dB (in 0.5-dB steps). For each gain setting, the analog input full-scale range scales proportionally, as shown in Table 12.

SFDR improvement is achieved at the expense of SNR; for each gain setting, SNR degrades approximately 0.5 dB. SNR degradation is reduced at high input frequencies. As a result, fine gain is very useful at high input frequencies because SFDR improvement is significant with marginal degradation in SNR. Therefore, fine gain can be used to trade-off between SFDR and SNR. Note that the default gain after reset is 0 dB.

Table 12. Full-Scale Range Across Gains

FINE_GAIN[3:0]	GAIN (dB)	TYPE	FULL-SCALE (V_{PP})
0000	0	Fine gain, programmable (default after reset)	2.00
0001	0.5		1.89
0010	1		1.78
0011	1.5		1.68
0100	2		1.59
0101	2.5		1.5
0110	3		1.42
0111	3.5		1.34
1000	4		1.26
1001	4.5		1.19
1010	5		1.12
1011	5.5		1.06
1100	6		1.00
1101	Do not use		
1110			
1111			

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SIGNAL POWER ESTIMATION

The device includes a power estimation circuit that can be used to obtain a coarse power estimate (accurate to within a dB) of the input signal averaged over a programmable number of samples. Enable the EN_PWR_EST bit in order to make the power estimate available on the DETECT[3:0] pins. The states of the DETECT[3:0] bits map to the input signal power as shown in Table 13.

Table 13. State of DETECT[3:0] Versus Input Signal Power

INPUT SIGNAL POWER RANGE (dBFS)	DETECT[3:0]	INPUT SIGNAL POWER RANGE (dBFS)	DETECT[3:0]
–Inf to –12.5	0001	–6.5 to –5.5	1000
–12.5 to –11.5	0010	–5.5 to –4.5	1001
–11.5 to –10.5	0011	–4.5 to –3.5	1010
–10.5 to –9.5	0100	–3.5 to –2.5	1011
–9.5 to –8.5	0101	–2.5 to –1.5	1100
–8.5 to –7.5	0110	–1.5 to 0	1101
–7.5 to –6.5	0111	0 to +1	1110

The number of samples used for computing the average power is set by SAMPLES_PWR_EST[2:0], as shown in Table 14.

Table 14. Number of Samples Used for Power Estimation

SAMPLES_PWR_EST[2:0]	NUMBER OF SAMPLES
000	1K
001	2K
010	4K
011	8K
100	16K

DEFINITION OF SPECIFICATIONS

Analog Bandwidth: The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low-frequency value.

Aperture Delay: The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs. This delay is different across channels. The maximum variation is specified as aperture delay variation (channel-to-channel).

Aperture Uncertainty (Jitter): The sample-to-sample variation in aperture delay.

Clock Pulse Duration and Duty Cycle: The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse duration) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine-wave clock results in a 50% duty cycle.

Maximum Conversion Rate: The maximum sampling rate at which certified operation is given. All parametric testing is performed at this sampling rate unless otherwise noted.

Minimum Conversion Rate: The minimum sampling rate at which the ADC functions.

Differential Nonlinearity (DNL): An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. DNL is the deviation of any single step from this ideal value, measured in units of LSBs.

Integral Nonlinearity (INL): INL is the deviation of the ADC transfer function from a best-fit line determined by a least-squares-curve fit of that transfer function, measured in units of LSBs.

Gain Error: Gain error is the deviation of the ADC actual input full-scale range from its ideal value. Gain error is given as a percentage of the ideal input full-scale range. Gain error has two components: error resulting from reference inaccuracy and error resulting from the channel. Both errors are specified independently as E_{GREF} and E_{GCHAN}, respectively.

To a first-order approximation, the total gain error is $E_{TOTAL} \sim E_{GREF} + E_{GCHAN}$.

For example, if $E_{TOTAL} = \pm 0.5\%$, the full-scale input varies from $(1 - 0.5 / 100) \times FS_{ideal}$ to $(1 + 0.5 / 100) \times FS_{ideal}$.

Offset Error: Offset error is the difference, given in number of LSBs, between the ADC actual average idle channel output code and the ideal average idle channel output code. This quantity is often mapped into millivolts.

Temperature Drift: The temperature drift coefficient (with respect to gain and offset error) specifies the change per degree Celsius of the parameter from T_{MIN} to T_{MAX}. The coefficient is calculated by dividing the maximum deviation of the parameter across the T_{MIN} to T_{MAX} range by the difference of $T_{MAX} - T_{MIN}$.

Signal-to-Noise Ratio (SNR): SNR is the ratio of the power of the fundamental (P_S) to the noise floor power (P_N), excluding the power at dc and the first nine harmonics.

$$SNR = 10Log^{10} \frac{P_S}{P_N} \tag{1}$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

Signal-to-Noise and Distortion (SINAD): SINAD is the ratio of the power of the fundamental (P_S) to the power of all other spectral components including noise (P_N) and distortion (P_D), but excluding dc.

$$SINAD = 10Log^{10} \frac{P_S}{P_N + P_D} \tag{2}$$

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

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Effective Number of Bits (ENOB): ENOB is a measure of the converter performance as compared to the theoretical limit based on quantization noise.

$$ENOB = \frac{SINAD - 1.76}{6.02} \tag{3}$$

Total Harmonic Distortion (THD): THD is the ratio of the power of the fundamental (P_S) to the power of the first nine harmonics (P_D).

$$THD = 10Log^{10} \frac{P_S}{P_N} \tag{4}$$

THD is typically given in units of dBc (dB to carrier).

Spurious-Free Dynamic Range (SFDR): SFDR is the ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier).

Two-Tone Intermodulation Distortion (IMD3): IMD3 is the ratio of the power of the fundamental (at frequencies f_1 and f_2) to the power of the worst spectral component at either frequency ($2f_1 – f_2$) or ($2f_2 – f_1$). IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

DC Power-Supply Rejection Ratio (DC PSRR): DC PSSR is the ratio of the change in offset error to a change in analog supply voltage. DC PSRR is typically given in units of millivolts per volt.

AC Power-Supply Rejection Ratio (AC PSRR): AC PSRR is the measure of rejection of variations in the supply voltage by the ADC. If ΔV_{SUP} is the change in supply voltage and ΔV_{OUT} is the resultant change of the ADC output code (referred to the input), then:

$$PSRR = 20Log^{10} \frac{\Delta V_{OUT}}{\Delta V_{SUP}} \text{ (Expressed in dBc)} \tag{5}$$

Voltage Overload Recovery: The number of clock cycles taken to recover to less than 1% error after an overload on the analog inputs. This overload recovery is tested by separately applying a sine-wave signal with a 6-dB positive and negative overload. The deviation of the first few samples after the overload (from the expected values) is noted.

Common Mode Rejection Ratio (CMRR): CMRR is the measure of rejection of variation in the analog input common-mode by the ADC. If ΔV_{CM_IN} is the change in the common-mode voltage of the input pins and ΔV_{OUT} is the resultant change of the ADC output code (referred to the input), then:

$$CMRR = 20Log^{10} \frac{\Delta V_{OUT}}{\Delta V_{CM}} \text{ (Expressed in dBc)} \tag{6}$$

Crosstalk (only for multichannel ADCs): Crosstalk is a measure of the internal coupling of a signal from adjacent channel into the channel of interest. Crosstalk is specified separately for coupling from the immediate neighboring channel (near-channel) and for coupling from a channel across the package (far-channel). Crosstalk is usually measured by applying a full-scale signal in the adjacent channel. Crosstalk is the ratio of the power of the coupling signal (as measured at the output of the channel of interest) to the power of the signal applied at the adjacent channel input. Crosstalk is typically expressed in dBc (dB to carrier).

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REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (October 2013) to Revision B **Page**

- Changed document status from Product Preview to Production Data 1
- Changed Power-Down Modes, *Fast recovery power-down mode*, *DNL*, and *INL* parameter specifications in Electrical Characteristics table 4
- Changed Power-Supply Currents, I_{IOVDD} parameter name in Electrical Characteristics table 4
- Changed f_S value in footnote 2 of Electrical Characteristics table 4
- Changed CML Outputs, *IOVDD supply range* parameter minimum specification in Digital Characteristics table 5
- Changed description of DETECT[3:0], OVR, and RESET pins in Pin Functions table 12
- Changed DAC to ADC in functional block diagram 13
- Deleted *Differential Nonlinearity (DNL)* and *Integrated Nonlinearity (INL)* curves from Typical Characteristics 19
- Changed legend in Figure 38 21
- Changed footnote 1 in Table 9 26
- Changed *Serial Register Readout* section into two sections: *Serial Register Readout* and *Reset Timing* 27
- Changed number of clock cycles for data latency in *Theory of Operation* section 32
- Changed *2-pF input capacitance* to *3-pF input capacitance* in *Analog Inputs* section 32

Changes from Original (September 2013) to Revision A **Page**

- Changed data rate value in 1st Features bullet 1
- Changed dual-lane mode value in 2nd Features bullet 1
- Changed 4th and 5th Features bullets 1
- Added Recommended Operating Conditions table and Table 1 3
- Added Electrical Characteristics tables 4
- Added *Parametric Measurement Information* section 6
- Added *Pin Configuration* section 11
- Added *Functional Block Diagram* section 13
- Added *Typical Characteristics* sections 14
- Added *Device Configuration* section 24
- Added *Application Information* section 32

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS61JB46IRHAR	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	61JB46
ADS61JB46IRHAR.A	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	61JB46
ADS61JB46IRHAT	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	61JB46
ADS61JB46IRHAT.A	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	61JB46

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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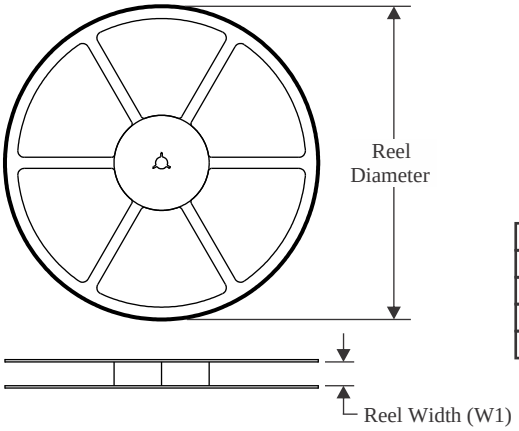
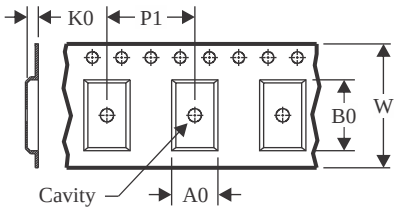
TAPE AND REEL INFORMATION

REEL DIMENSIONS

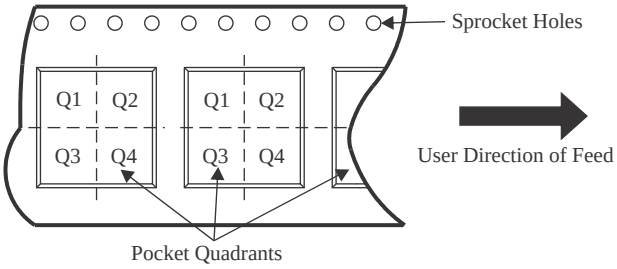


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

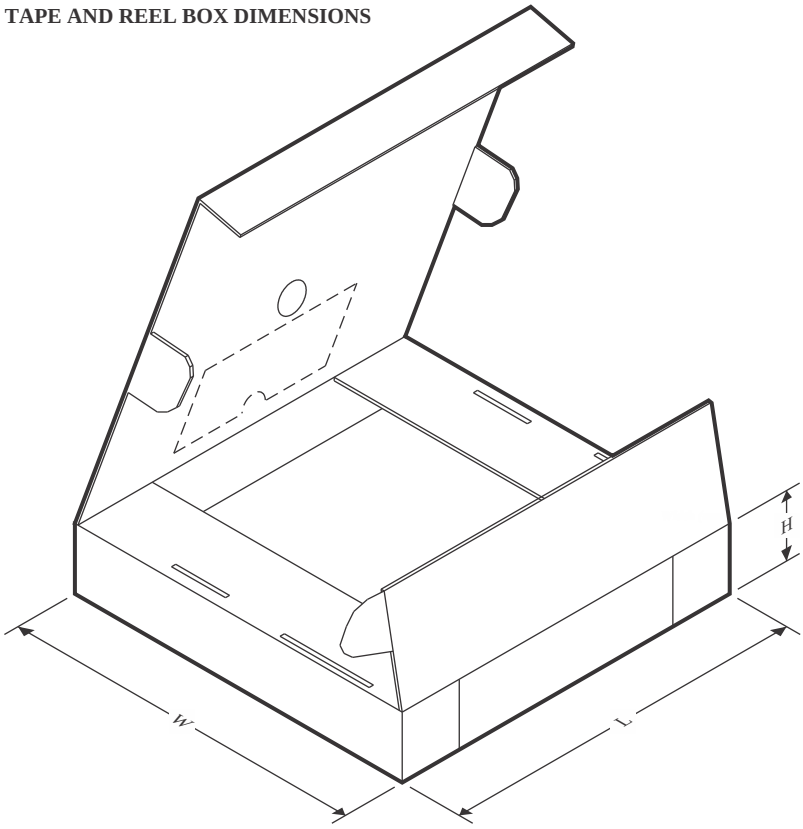
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS61JB46IRHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS61JB46IRHAR	VQFN	RHA	40	2500	350.0	350.0	43.0

GENERIC PACKAGE VIEW

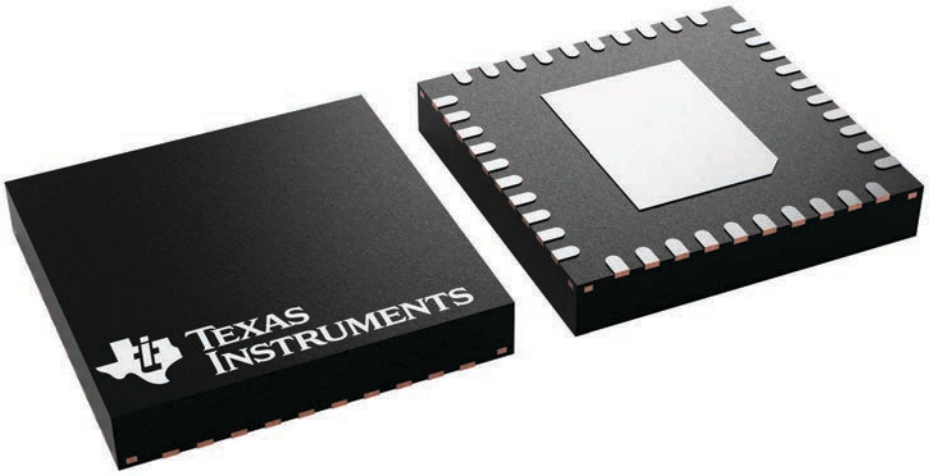
RHA 40

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

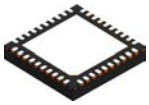
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225870/A

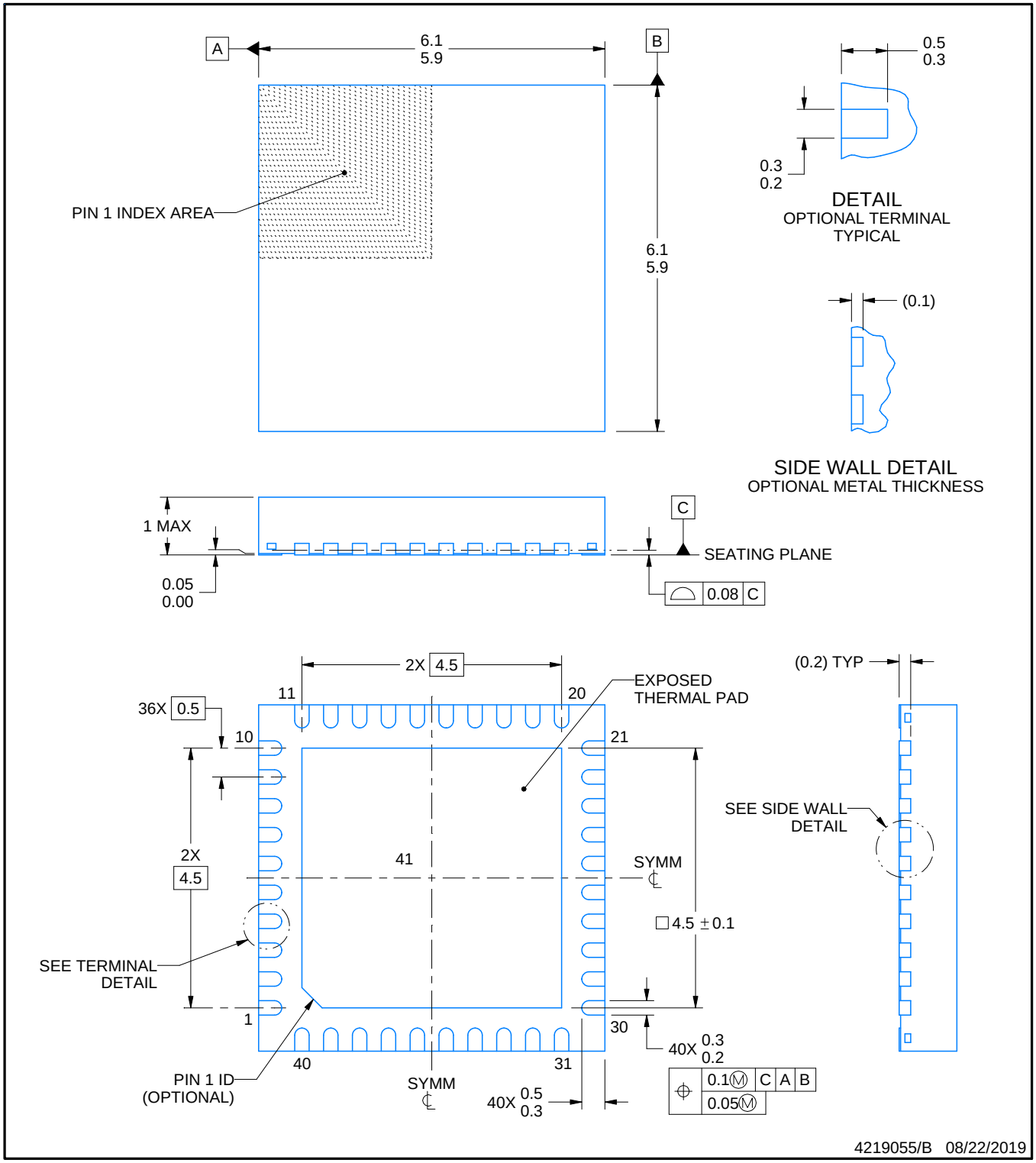
RHA0040H



PACKAGE OUTLINE

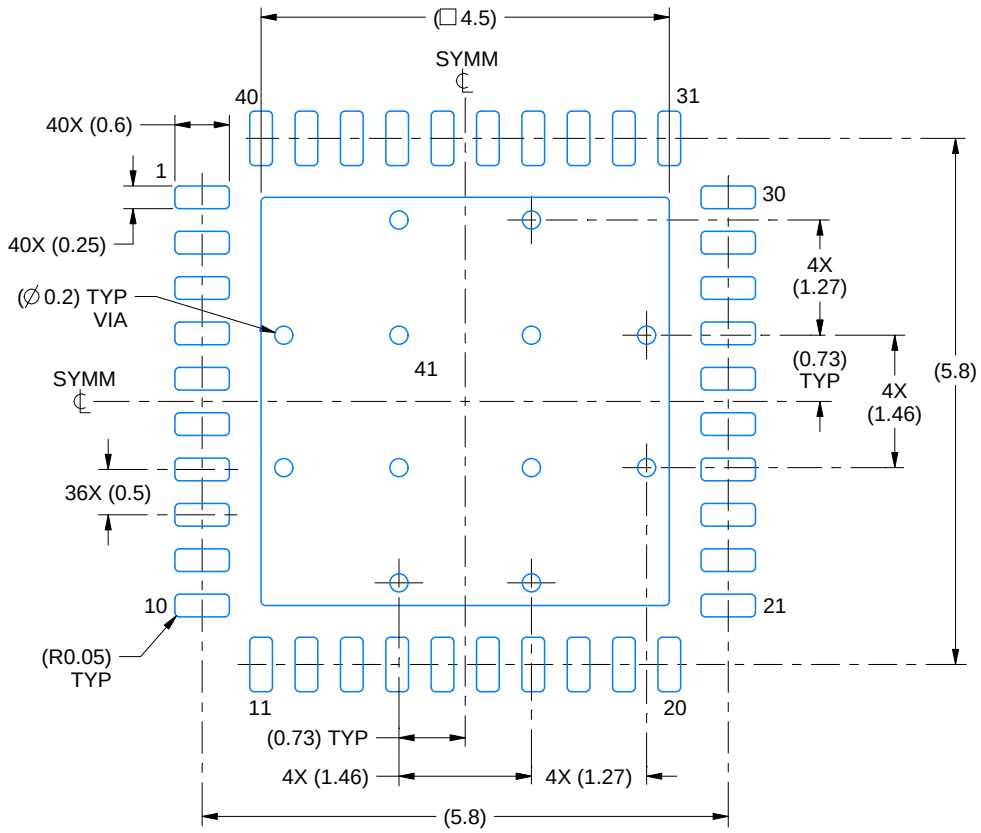
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

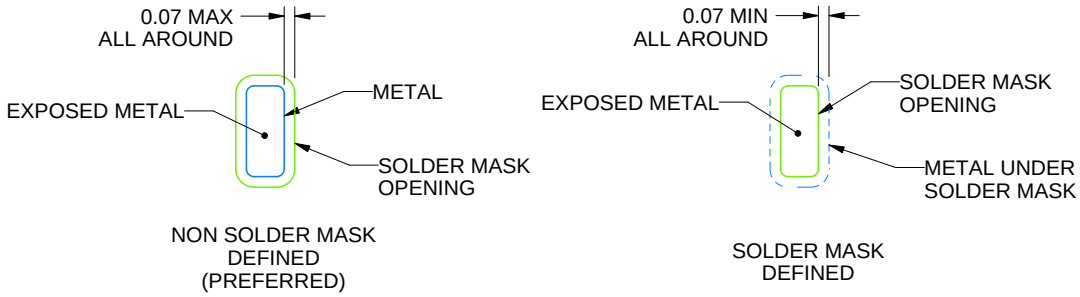


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X



SOLDER MASK DETAILS

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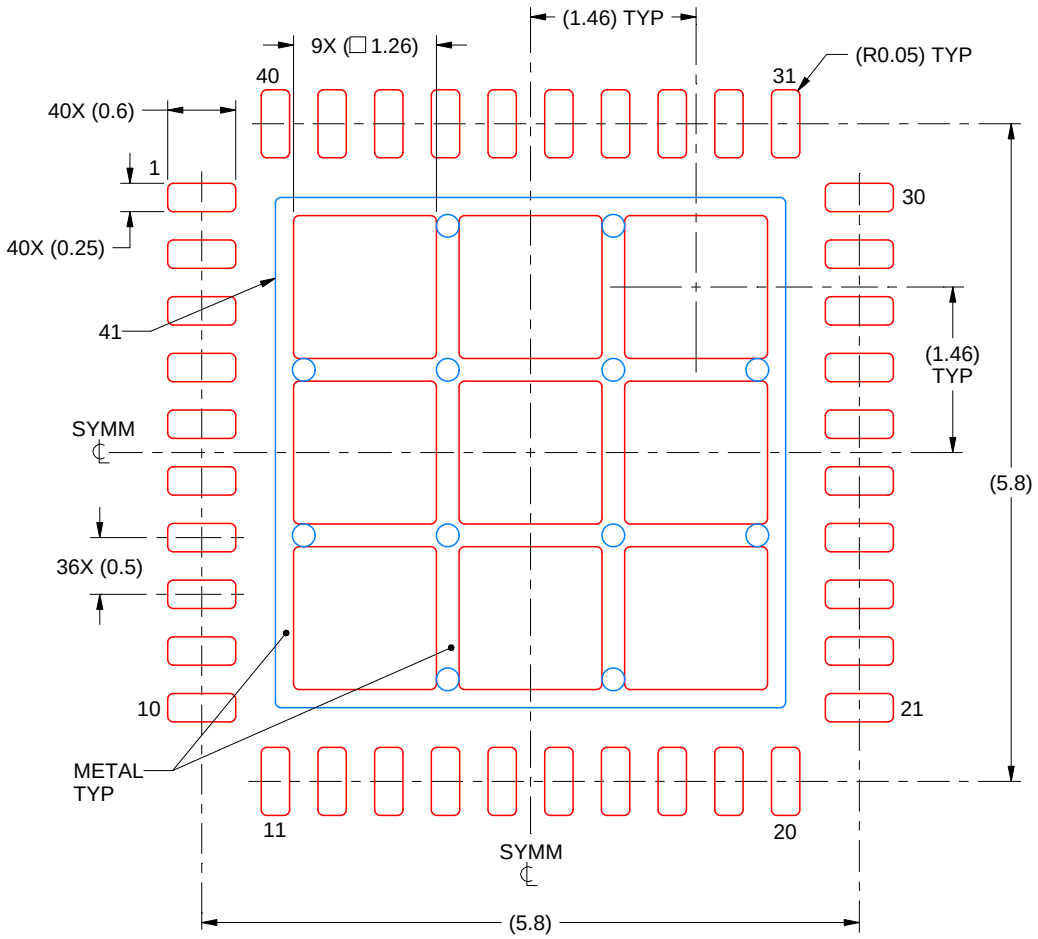
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 41:
70% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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