AFE58JD32 32-Channel Ultrasound AFE With 35-mW/Channel Power, 2.1 nV/√Hz Noise, 12-Bit, 40-MSPS or 10-Bit, 50-MSPS Output, Passive CW Mixer, LVDS and JESD204B Interface, and Digital Demodulator

1 Features

- 32-Channel, AFE for Ultrasound Applications:
  - Input Attenuator, LNA, LPF, ADC, Digital I/Q Demodulator and CW Mixer
  - Digital Time Gain Compensation (DTGC)
  - Total Gain Range: 12 dB to 51 dB
  - Linear Input Range: 800 mV_{PP}
- Input Attenuator With DTGC:
  - 8-dB to 0-dB Attenuation With 0.125-dB Step
  - Supports Matched Impedance for:
    - 50-Ω to 800-Ω Source Impedance
- Low-Noise Amplifier (LNA) With DTGC:
  - 20-dB to 51-dB Gain With 0.125-dB Step
  - Low Input Current Noise: 1.2 pA/√Hz
- 3rd-Order, Linear-Phase, Low-Pass Filter (LPF):
  - 5 MHz, 7.5 MHz, 10 MHz, and 12.5 MHz
- 16 ADCs Converting at 12-Bit, 80 MSPS or 10-bit, 100 MSPS:
  - Each ADC Converts Two Sets of Inputs at Half Rate
  - 12-Bit ADC: 72-dBFS SNR
  - 10-Bit ADC: 61-dBFS SNR
- Optimized for Noise and Power:
  - 35 mW/Ch at 2.1 nV/√Hz, 40 MSPS
  - 42 mW/Ch at 1.4 nV/√Hz, 40 MSPS
  - 52 mW/Ch at 1.3 nV/√Hz, 40 MSPS
  - 60 mW/Ch in CW Mode
- Excellent Device-to-Device Gain Matching:
  - ±0.5 dB (Typical)
- Low Harmonic Distortion: –55 dBc
- Fast and Consistent Overload Recovery
- Continuous Wave (CW) Path With:
  - Low Close-In Phase Noise of –151 dBc/Hz at 1-kHz Frequency Offset Off 2.5-MHz Carrier
  - Phase Resolution: λ / 16
  - Supports 16X CW Clock
  - 12-dB Suppression on Third and Fifth Harmonics
- Digital I/Q Demodulator After ADC:
  - Decimation Filter M = 1 to 63
  - Data Throughput Reduction After Decimation
  - On-Chip RAM with 32 Preset Profiles
- LVDS Interface With a Speed Up to 1 Gbps
- 5-Gbps JESD Interface:
  - JESD204B Subclass 0, 1, and 2
  - 2, 4, or 8 Channels per JESD Lane
- Small Package: 15-mm × 15-mm NFBGA-289

2 Applications

- Medical Ultrasound Imaging
- Nondestructive Evaluation Equipment
- Sonar Imaging Equipment
- Multichannel, High-Speed Data Acquisition

3 Description

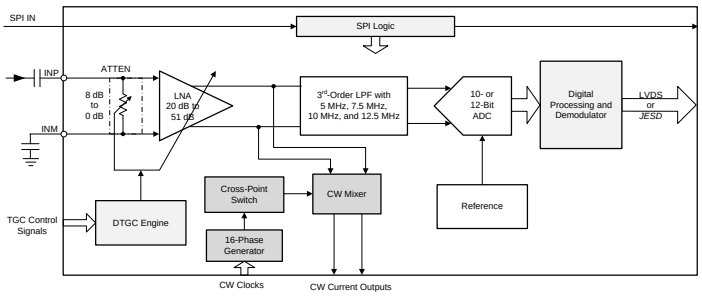
The AFE58JD32 device is a highly-integrated, analog front-end solution specifically designed for ultrasound systems where high performance, low power, and small size are required.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
AFE58JD32	NFBGA (289)	15.00 mm × 15.00 mm

(1) For all available packages, see the package option addendum at the end of the datasheet.

Simplified Block Diagram



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4 Revision History

Changes from Original (August 2017) to Revision A **Page**

- Changed *Power* and *Noise* values in the Title 1
- Added values for Ultra low-power mode in *Features* section 1

5 Description (continued)

The AFE58JD32 is an integrated analog front-end (AFE) optimized for medical ultrasound application. The device is realized through a multichip module (MCM) with three dies: two voltage-controlled amplifier (VCA) dies and one analog-to-digital converter (ADC) die. Each VCA die has 16 channels and the ADC die converts all of the 32 channels.

Each channel in the VCA die is configured in either of two modes: time gain compensation (TGC) mode or continuous wave (CW) mode. In TGC mode, each channel includes an input attenuator (ATTEN), a low-noise amplifier (LNA) with variable-gain, and a third-order, low-pass filter (LPF). The attenuator supports an attenuation range of 8 dB to 0 dB, and the LNA supports gain ranges from 20 dB to 51 dB. The LPF cutoff frequency can be configured at 5 MHz, 7.5 MHz, 10 MHz, or 12.5 MHz to support ultrasound applications with different frequencies. In CW mode, each channel includes an LNA with a fixed gain of 18 dB, and a low-power passive mixer with 16 selectable phase delays. Different phase delays can be applied to each analog input signal to perform an on-chip beamforming operation. A harmonic filter in the CW mixer suppresses the third and fifth harmonic to enhance the sensitivity of the CW Doppler measurement.

The ADC die has 16 physical ADCs. Each ADC converts two sets of outputs – one from each VCA die. The ADC is configured to operate with a resolution of 12 bits or 10 bits. The ADC resolution can be traded off with conversion rate, and operates at maximum speeds of 80 MSPS and 100 MSPS at 12-bit and 10-bit resolution, respectively. The ADC is designed to scale its power with sampling rate. The output interface of the ADC comes out through a low-voltage differential signaling (LVDS) which can easily interface with low-cost field-programmable gate arrays (FPGAs).

The AFE58JD32 includes an optional digital demodulator and JESD204B data packing blocks. The digital in-phase and quadrature (I/Q) demodulator with programmable decimation filters accelerates computationally-intensive algorithms at low power. The device also supports an optional JESD204B interface that runs up to 5-Gbps and further reduces the circuit-board routing challenges in high-channel count systems.

The AFE58JD32 also allows various power and noise combinations to be selected for optimizing system performance. Therefore, this device is a suitable ultrasound AFE solution for systems with strict battery-life requirements.

6 Device and Documentation Support

6.1 Documentation Support

6.1.1 Related Documentation

For related documentation see the following:

- *AFE5818 16-Channel, Ultrasound, Analog Front-End with 140-mW/Channel Power, 0.75-nV/√Hz Noise, 14-Bit, 65-MSPS or 12-Bit, 80-MSPS ADC, and Passive CW Mixer*
- *ADS8413 16-BIT, 2-MSPS, LVDS SERIAL INTERFACE, SAR ANALOG-TO-DIGITAL CONVERTER*
- *ADS8472 16-BIT, 1-MSPS, PSEUDO-BIPOLAR, FULLY DIFFERENTIAL INPUT, MICROPOWER SAMPLING ANALOG-TO-DIGITAL CONVERTER WITH PARALLEL INTERFACE, REFERENCE*
- *CDCE72010 Ten Output High Performance Clock Synchronizer, Jitter Cleaner, and Clock Distributor*
- *CDCM7005 3.3-V High Performance Clock Synchronizer and Jitter Cleaner*
- *ISO724x High-Speed, Quad-Channel Digital Isolators*
- *LMK0480x Low-Noise Clock Jitter Cleaner with Dual Loop PLLs*
- *OPA1632 High-Performance, Fully-Differential Audio Operational Amplifier*
- *OPA2x11 1.1-nv/√Hz Noise, Low Power, Precision Operational Amplifier*
- *SN74AUP1T04 LOW POWER, 1.8/2.5/3.3-V INPUT, 3.3-V CMOS OUTPUT, SINGLE INVERTER GATE*
- *THS413x High-Speed, Low-Noise, Fully-Differential I/O Amplifiers*
- *MicroStar BGA Packaging Reference Guide*

6.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.4 Trademarks

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6.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

6.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Tray Information

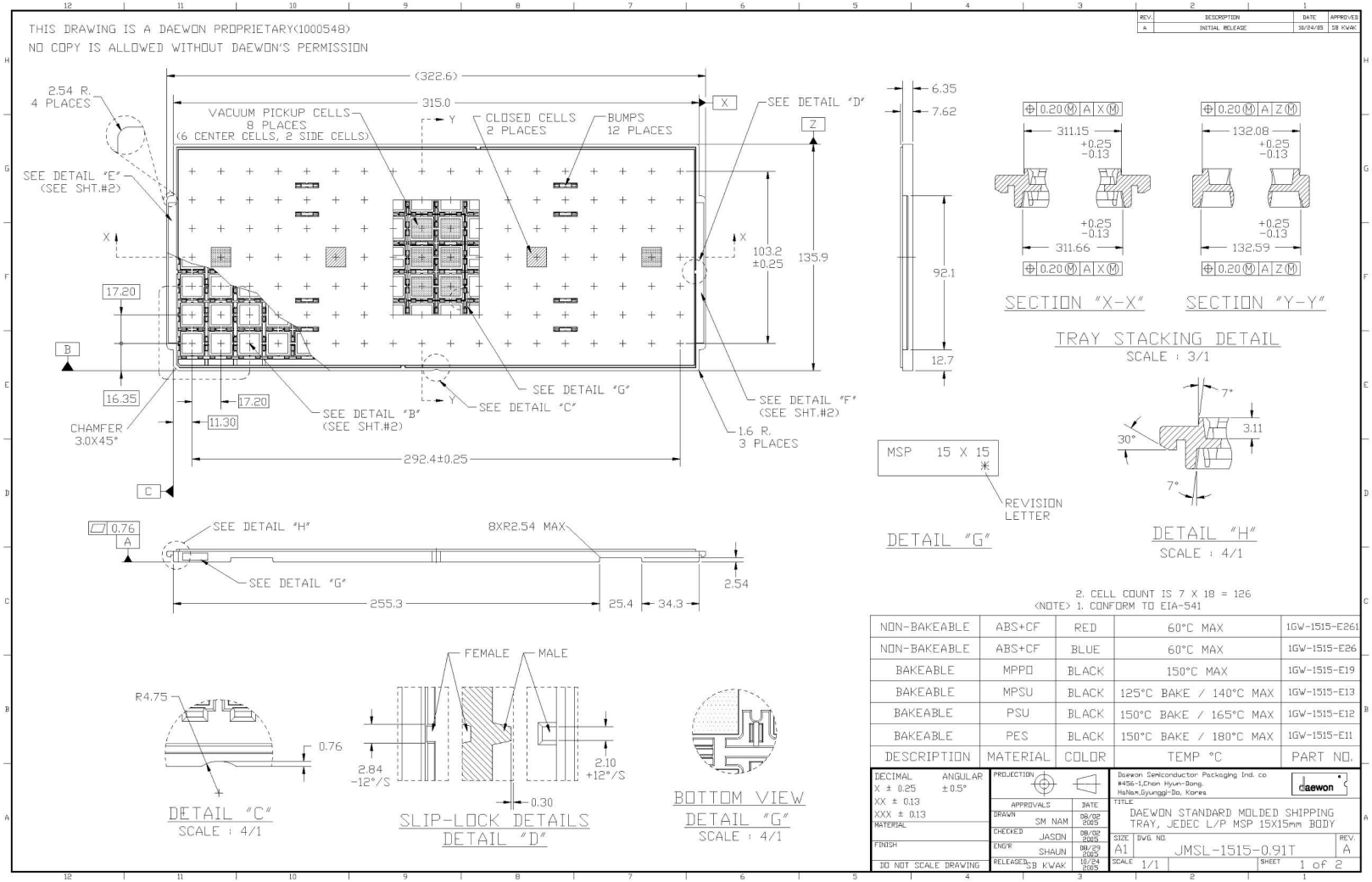


Figure 1. Tray Diagram, Section 1

Tray Information (continued)

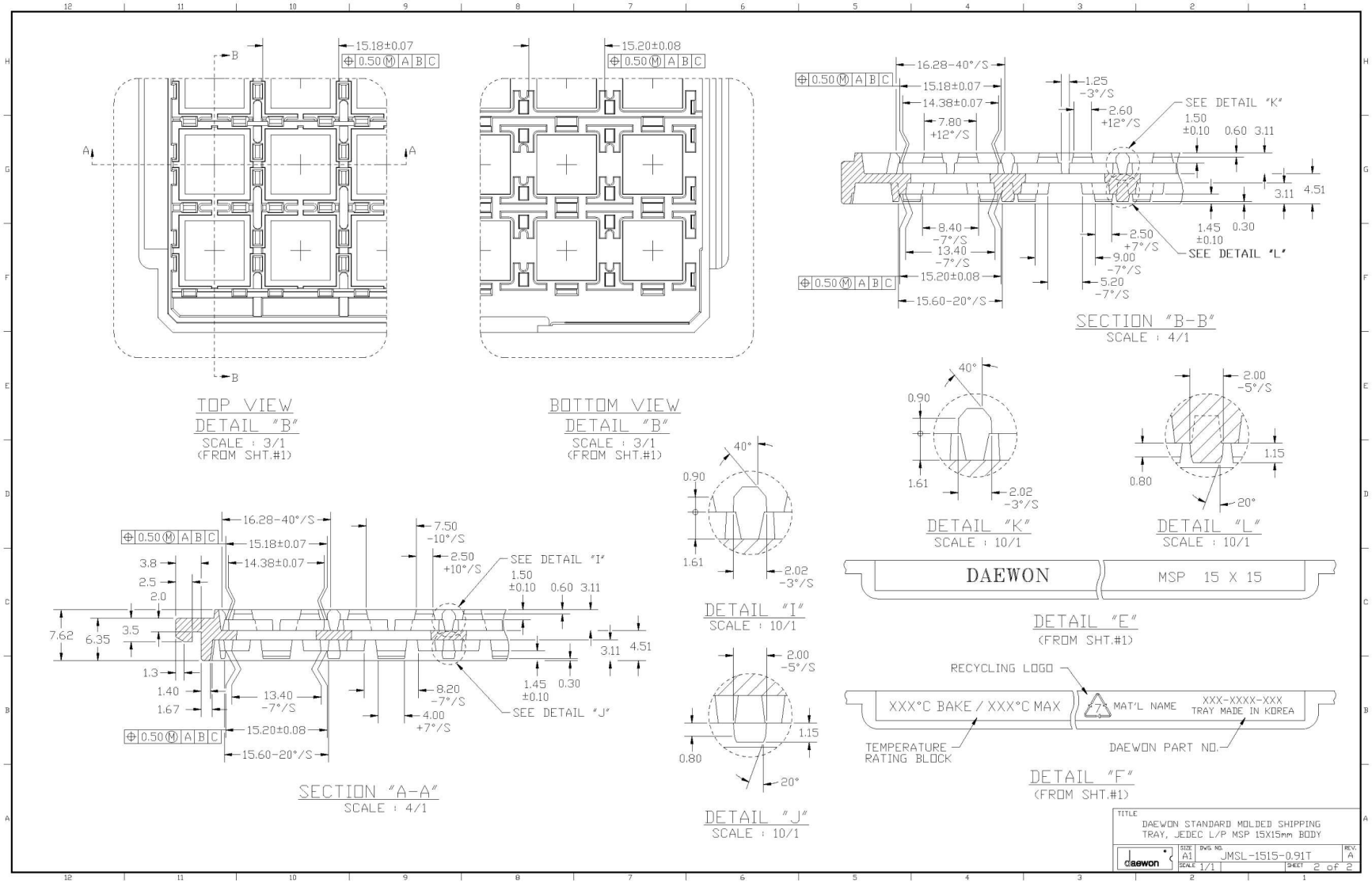


Figure 2. Tray Diagram, Section 2

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AFE58JD32ZBV	Active	Production	NFBGA (ZBV) | 289	126 | JEDEC TRAY (5+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	AFE58JD32
AFE58JD32ZBV.A	Active	Production	NFBGA (ZBV) | 289	126 | JEDEC TRAY (5+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	AFE58JD32
AFE58JD32ZBV.B	Active	Production	NFBGA (ZBV) | 289	126 | JEDEC TRAY (5+1)	-	Call TI	Call TI	-40 to 85	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

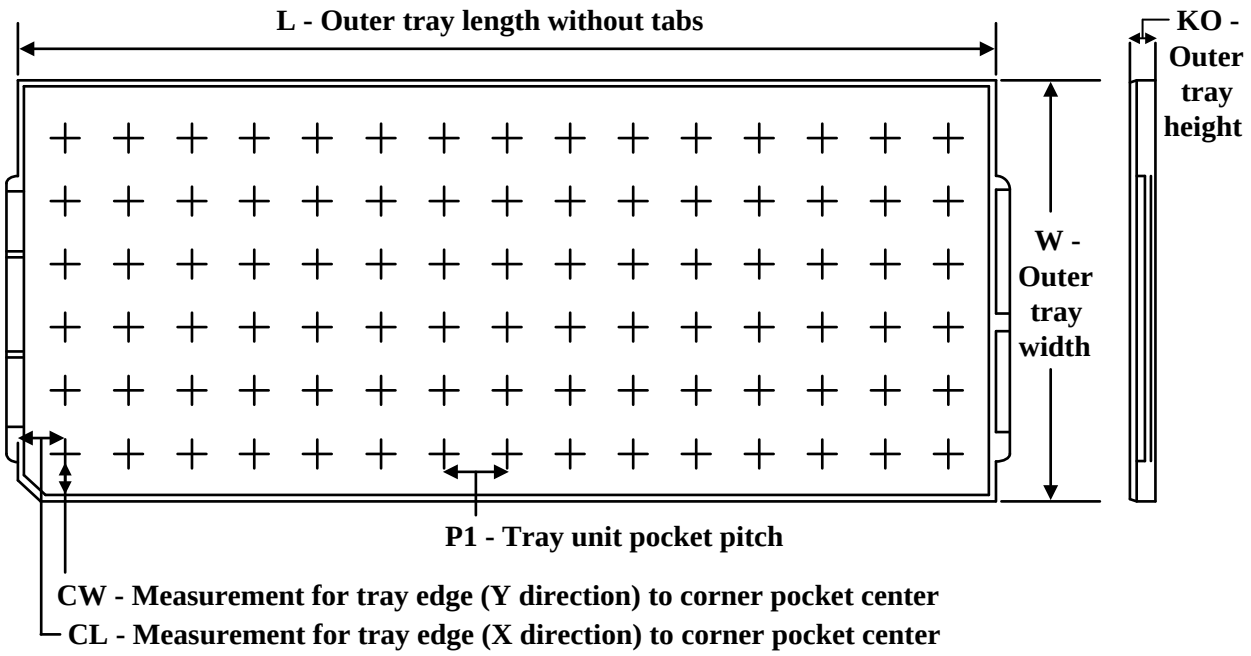
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TRAY

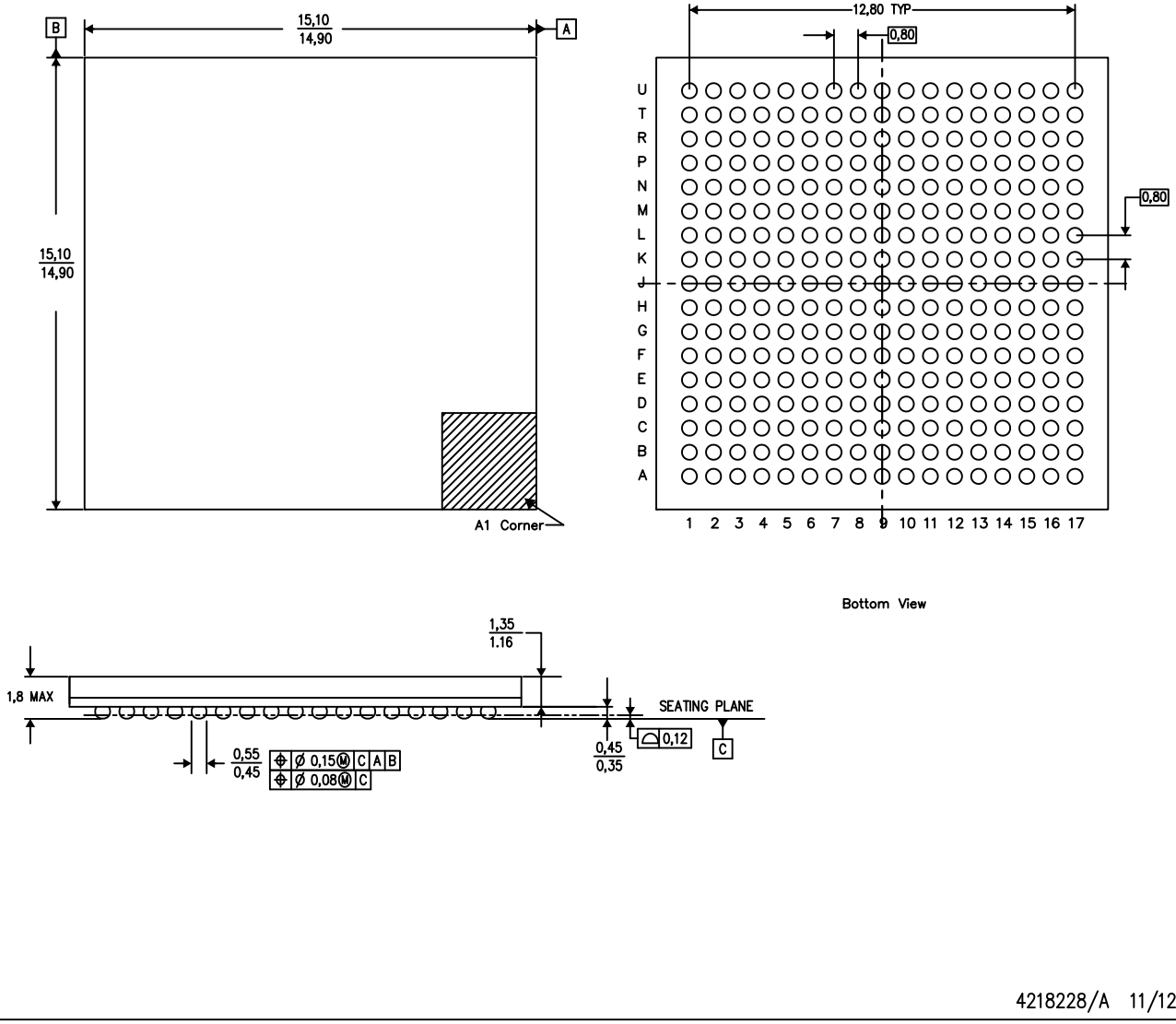


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
AFE58JD32ZBV	ZBV	NFBGA	289	126	7 X 18	150	315	135.9	7620	17.2	11.3	16.35
AFE58JD32ZBV.A	ZBV	NFBGA	289	126	7 X 18	150	315	135.9	7620	17.2	11.3	16.35

ZBV (S–PBGA–N289) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This is a Pb–free solder ball design.

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