AM275x Signal Processing Microcontrollers

1 Features

Processor Cores:

- Dual or Quad-core Arm® Cortex® R5F CPU with each core running up to 1GHz
  - 32KB I-Cache with 64-bit ECC per CPU core
    - 4x8KB association
    - Single Error Correction, Double Error Detection ECC protected per 64 bits
  - 32KB D-cache with 64-bit ECC per CPU core
    - 4x8KB association
    - Single Error Correction, Double Error Detection ECC protected per 64 bits
  - 64KB Tightly Coupled Memory (TCM) per core, with 32-bit ECC
    - Single Error Correction, Double Error Detection ECC protected per 64 bits
    - Two Banks, A and B, 32KB each
      - Bank B split into B0 and B1, 16KB each
    - 128KB TCM for CPU0 in lockstep mode
  - Up to 128KB Remote L2 Cache
    - 32B cache line
    - Up to 128KB L2 cache covering up to 16MB cacheable space
    - Read only, 8-way cache
    - Fast Local Copy (FLC) support
  - For each cluster, lockstep or independent dual core operation supported
- Single or Dual C7x DSP core with each core running up to 1GHz
  - L1 memory architecture
    - 32KB I-Cache per core
    - 64KB D-Cache per core
  - L2 memory architecture
    - 2.25MB with ECC protection on L2 SRAM
      - 2MB "Main" segment
      - 256KB "Auxiliary" segment
  - Matrix Multiply Accelerator Version 2f (MMA2F) on DSP0
- 2x Asynchronous Audio Sample Rate Converter (ASRC)
  - 140dB Signal-to-Noise ratio (SNR)
  - Up to 8 pairs of input and output streams (up to 16 channels total) per ASRC
  - Input and output sample rates from 8KHz to 216KHz
  - 16-, 18-, 20-, 24-bit data input/output

Memory Subsystem:

- Up to 6MB of On-Chip Shared SRAM
- Remote Low latency L2 cache (RL2), software programmable, allocated from SRAM
- 432KB of On-Chip SRAM in SMS Subsystem
  - 256KB of On-Chip RAM with SECDED ECC in SMS Subsystem
  - 176KB of On-Chip RAM with SECDED ECC in SMS Subsystem for TI security firmware

Flash and Memory Interfaces:

- 2 × Flash Sub Systems (FSS) that support Octal Serial Peripheral Interface (OSPI) at up to 166MHz SDR and 166MHz DDR at 1.8V and 3.3V with XIP (eXecute In Place) which can be used for
  - 1x FSS supporting OSPI OptiFlash memory technology, Firmware Over-The-Air upgrades (FOTA), and On The Fly Advanced Encryption Standard (OTFA)
  - 1x FSS supporting OSPI or HyperRAM
  - RAM expansion
- 1 × 8-bit Multi-Media Card/Secure Digital (eMMC/SD) interface

General Connectivity:

- 5 × Multichannel Audio Serial Ports (McASP)
  - Transmit and Receive Clocks up to 50MHz
  - Up to 26 Serial Data Pins across 5x McASP with Independent TX and RX Clocks
  - Supports Time Division Multiplexing (TDM), Inter-IC Sound (I2S) and Similar Formats
  - Supports Digital Audio Interface Transmission (SPDIF, IEC60958-1, and AES-3 Formats)
  - FIFO Buffers for Transmit and Receive (256 Bytes)
  - Support for audio reference output clock
- 8 × Universal Asynchronous RX-TX (UART) modules
- 5 × Serial Peripheral Interface (SPI) controllers
- 8 × Inter-Integrated Circuit (I2C) ports
- 5 × Modular Controller Area Network (MCAN) modules with CAN-FD support
- 3 × Enhanced Pulse Width Modulation (ePWM) modules
- 6 × Enhanced Capture (ECAP) modules
- 1 × 12-bit Analog to Digital Converters (ADC) with 4MSPS maximum sampling rate
- Up to 167 General Purpose I/O (GPIO)

High Speed Interfaces

- Integrated Ethernet Switch supporting (total 2 external ports)

  - RMII (10/100) or RGMII (10/100/1000)
  - IEEE 1588 (Annex D, Annex E, Annex F with 802.1AS PTP)
  - Supports 802.1Qav (eAVB)
  - Clause 45 MDIO PHY management
  - Packet Classifier based on ALE engine with 512 classifiers
  - Priority flow control
  - Four CPU hardware interrupt pacing
  - IP/ UDP/ TCP checksum offload in hardware
- USB 2.0
  - Port configurable as USB host, USB device, or USB Dual-Role device
  - Integrated USB VBUS detection

Security:

- Hardware Security Module (HSM)
  - Dedicated dual-core ARM Cortex-M4F Security co-processor with dedicated interconnect for security
  - Dedicated security DMA and IPC subsystem for isolated processing
- Secure boot support
  - Hardware-enforced Root-of-Trust (RoT)
  - Support to switch RoT via backup key
  - Support for takeover protection, IP protection, and anti-roll back protection
- Cryptographic acceleration supported
  - Session-aware cryptographic engine with ability to auto-switch key-material based on incoming data stream
  - Supports cryptographic cores
    - AES - 128/192/256-bit key sizes
    - SHA2 - 224/256/384/512-bit support
    - DRBG with true random number generator
    - PKA (Public Key Accelerator) to Assist in RSA/ECC processing: RSA-4096 bits, ECDSA, SM2DSA, Curve25519/448
    - Supports Chinese crypto algorithms: SM3 and SM4
  - DMA support
- Debugging security
  - Secure software controlled debug access
  - Security aware debugging
- Trusted Execution Environment (TEE) supported
  - Arm TrustZone® based TEE
  - Extensive firewall support for isolation
  - Secure watchdog/timer/IPC
- Secure storage support
- On-the-Fly encryption and support for OSPI interface in XIP mode

Functional Safety:

- Functional Safety-Compliant targeted [Automotive]
  - Developed for functional safety applications
  - Documentation to be made available to aid ISO 26262 functional safety system design
  - Systematic capability up to ASIL-D targeted
  - Hardware integrity up to ASIL-B targeted
  - Safety-related certification
    - ISO 26262 planned

Power Management:

- Power modes supported by Device Manager:
  - Active
  - Standby
  - IO Retention

Boot Options:

- UART
- I2C EEPROM
- OSPI NOR/NAND Flash
- SD Card
- eMMC
- USB (host) Mass Storage
- USB (device) boot from external host (DFU mode)
- Ethernet

Technology / Package:

- AEC-Q100 qualified for automotive applications
- 16-nm FinFET technology
- 15.8mm x 15.8mm, 0.8mm pitch 361-pin FCCSP

2 Applications

- Automotive:
  - Premium Audio
  - Audio Amplifiers
  - Audio Gateway
  - AVAS - Acoustic Vehicle Alert System
  - Active/Road Noise Cancellation
  - Digital Cockpit

3 Description

The AM275x family of highly-integrated, high-performance microcontrollers is based on the Arm® Cortex R5F and C7x floating point DSP cores. The microcontrollers enable original equipment manufacturers (OEM) and original design manufacturers (ODM) to quickly bring to market devices with robust software support and rich user interfaces. The device offers the maximum flexibility of a fully integrated, mixed processor design

Key features and benefits:

- Extensive audio interfacing with 5x McASP peripherals
- Peripherals supporting system level connectivity such as 2-port Gigabit Ethernet, USB, OSPI/QSPI, CAN-FD, UARTs, SPI and GPIOs.
- Supports the latest cybersecurity requirements with the built-in Hardware Security Module (HSM).
- One or two dual-core R5F clusters with 128KB TCM per cluster (64KB per core) and up to two C7x DSP cores with 2.25MB of L2 SRAM per C7x DSP, greatly reducing the need for external memory.

Package Information

Part Number	Package(1)	Body Size and Pitch(2)
AM275xxxxxxxxxxQ1	ANJ (FCCSP, 361)	15.8mm × 15.8mm with 0.8mm pitch, ball count 361

(1) For more information, see Mechanical, Packaging, and Orderable Information.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

3.1 Functional Block Diagram

Figure 3-1 is functional block diagram of AM275x.

Figure 3-1. Functional Block Diagram

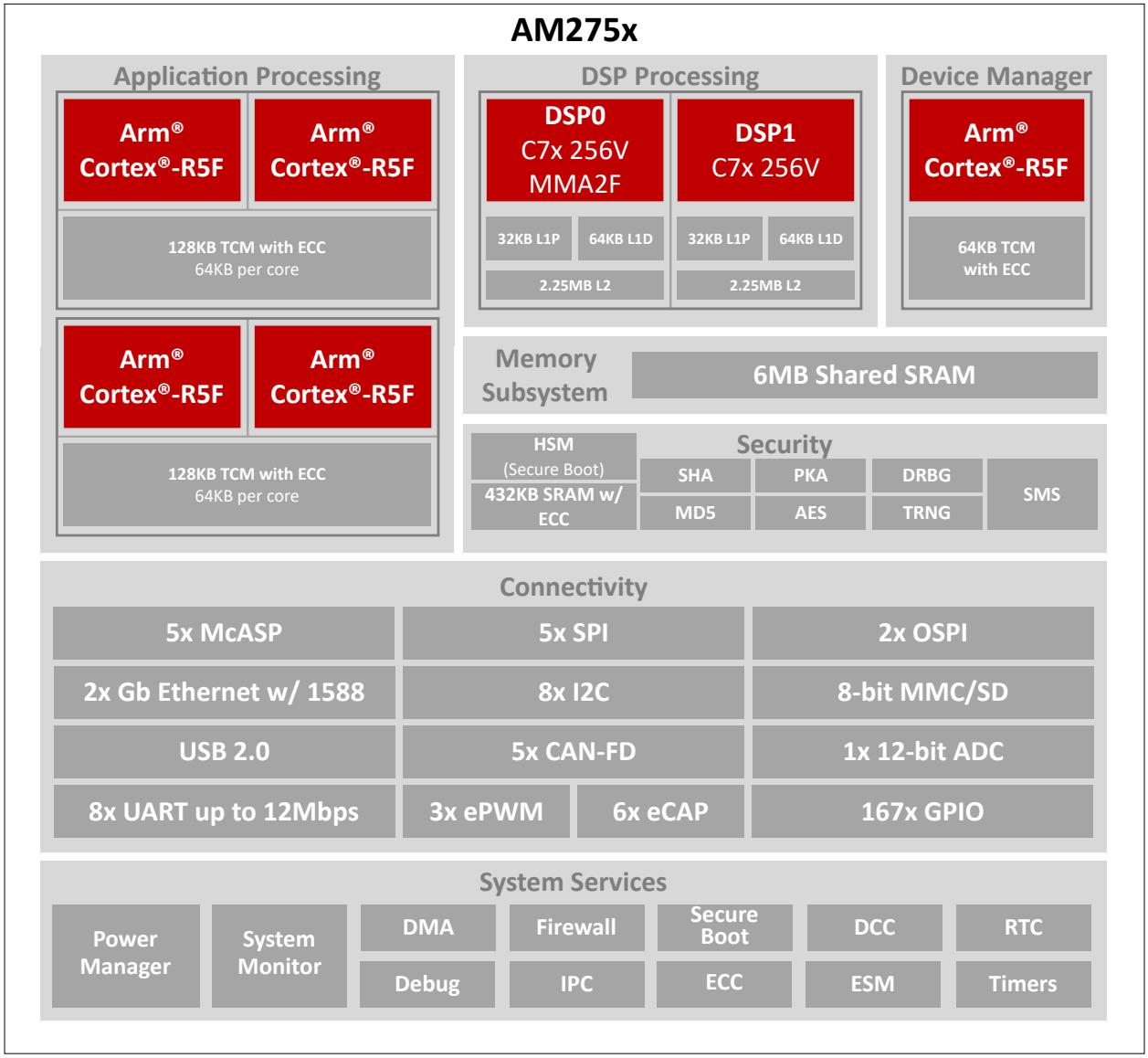


Table of Contents

4 Device Comparison

Table 4-1 shows a comparison between devices, highlighting the differences.

Note

Availability of features listed in this table are a function of shared IO pins, where IO signals associated with many of the features are multiplexed to a limited number of pins. The SysConfig tool should be used to assign signal functions to pins. This will provide a better understanding of limitations associated with pin multiplexing.

Table 4-1. Device Comparison

FEATURES	REFERENCE NAME	AM27542	AM27522	AM27521
WKUP_CTRL_MMR_CFG0_JTAG_USER_ID[31:13] Register bit values by device "Features" code (See Device Naming Convention for more information on device features)				
PROCESSORS AND ACCELERATORS				
Speed Grades		See Device Speed Grades		
Arm Cortex-R5F in MAIN domain	R5FSS	Quad Core	Dual Core	
Device Management Subsystem	WKUP_R5F	Single Core		
Hardware Security Module	HSM	Yes		
Crypto Accelerators	Security	Yes		
C7x Floating Point, Vector DSP	C7x256V DSP	Dual Core		Single Core
Asynchronous Audio Sample Rate Converter	ASRC	Two		One
SAFETY AND SECURITY				
AEC-Q100 Qualified	Q1	Yes(1)		
PROGRAM AND DATA STORAGE				
On-Chip Shared Memory (RAM)	OCSRAM	Up to 6MB(2) see Device Naming Convention		
R5F Tightly Coupled Memory (TCM)	TCM	256KB		
PERIPHERALS				
Modular Controller Area Network Interface with Full CAN-FD	MCAN	5		
General-Purpose I/O	GPIO	Up to 177 (up to 21 IO Retention capable)		
Inter-Integrated Circuit Interface	I2C	8(3)		
Multichannel Audio Serial Port	MCASP	5		
Multichannel Serial Peripheral Interface	MCSPI	5		
Multi-Media Card/Secure Digital Interface	MMC/SD	1x eMMC (8-bits) or 1x SD/SDIO (4-bits)		
Flash Subsystem (FSS)(4)	OSPI/QSPI	FSS0 additionally supports OptiFlash, FOTA, and FLC		
		FSS1 additionally supports HyperRAM		
Gigabit Ethernet Interface	CPSW3G	2 Ports (RGMII/RMII)		
General-Purpose Timers	TIMER	22 (16 in Main, 2 in WKUP, 4 in Security)		
Enhanced Pulse-Width Modulator Module	EPWM	3		
Enhanced Capture Module	ECAP	6		
Universal Asynchronous Receiver and Transmitter	UART	8(5)		
USB2.0 Controller with PHY	USB 2.0	1		
Analog-to-Digital Converter	ADC	1		
Media Local Bus (MOST50)	MLB	1		

(1) AEC-Q100 qualification is applicable to select part number variants as indicated by the Automotive Designator (Q1) identifier in the Device Naming Convention.
(2) Exact amount of On-Chip SRAM depends on the part number variant as indicated by the SRAM Memory (f) identifier in theDevice Naming Convention .
(3) 7x I2C instances are in the MAIN domain. 1x I2C instance is in the WKUP domain.
(4) Two flash interfaces, independently configured as OSPI or QSPI. FSS0 supports OptiFlash, FOTA and and FLC, FSS1 supports HyperRAM, and both FSS0 and FSS1 support XIP.
(5) 7x UART instances are in the MAIN domain. 1x UART instance is in the WKUP domain..

4.1 Related Products

Signal Processing Microcontrollers Broad family of scalable processors based on Arm® Cortex®-R cores with DSP cores, flexible accelerators, peripherals, connectivity and unified software support – designed for high end audio applications.

Products to complete your design:

- Audio Amplifiers
- Audio Converters
- Ethernet PHYs
- Power Management / PMICs
- Clocks and Timing
- Power Switches
- CAN Transceivers
- ESD Protection

Please reference the AM275 EVM Schematic for details of how these devices are implemented in a system design, and bill of materials for specific part number recommendations.

5 Terminal Configuration and Functions

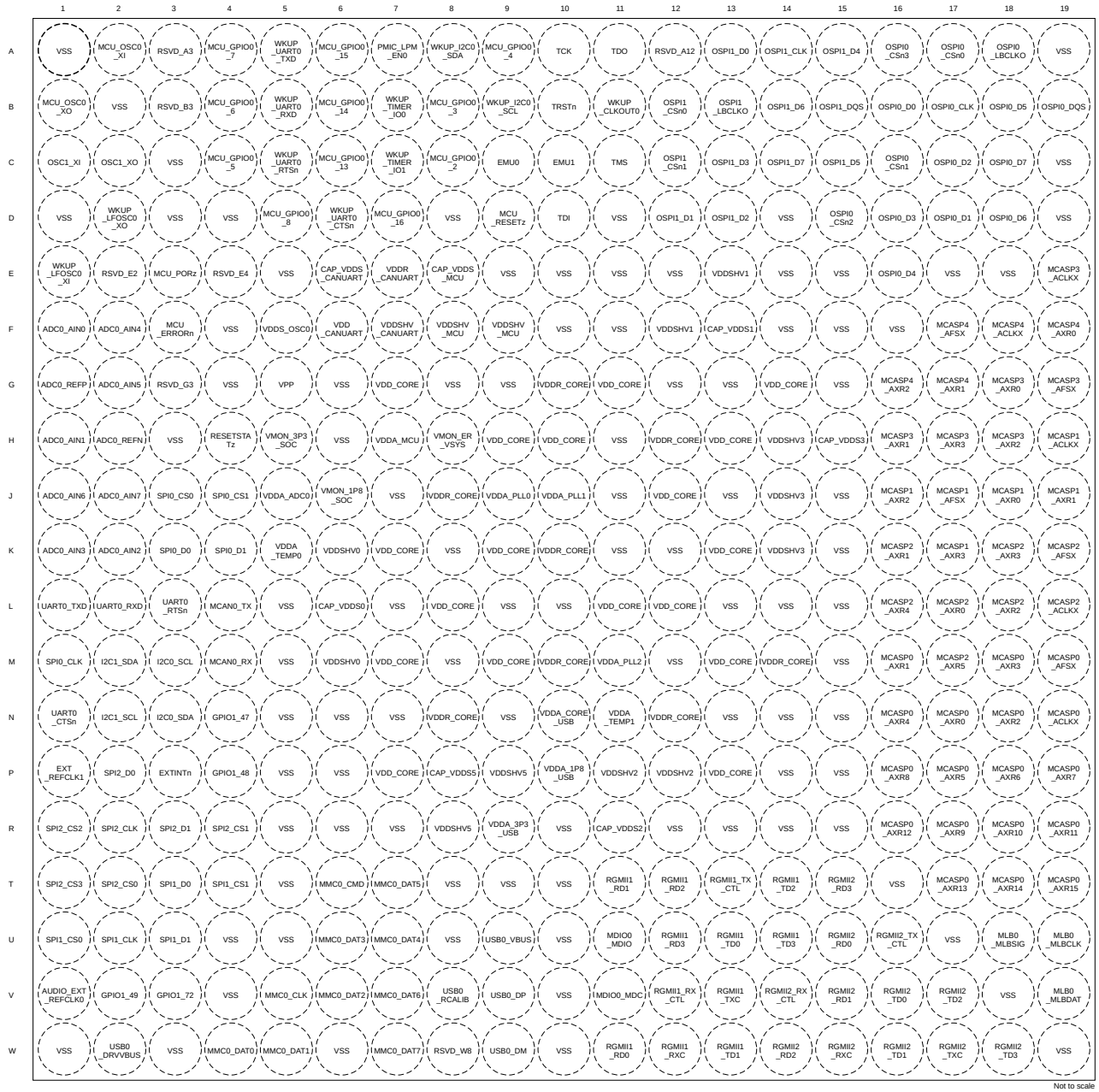
5.1 Pin Diagram

Note

The terms "ball", "pin", and "terminal" are used interchangeably throughout the document. An attempt is made to use "ball" only when referring to the physical package.

The diagrams in this section are used in conjunction with the other Terminal Configuration and Functions tables to locate signal names and ball grid numbers. The HTML version of this document provides additional information when hovering your cursor over a ball.

5.1.1 ANJ Pin Diagram



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
A	VSS	MCU_OSC0_XI	RSVD_A3	MCU_GPIO0_7	WKUP_UART0_TXD	MCU_GPIO0_15	PMIC_LPM_EN0	WKUP_I2C0_SDA	MCU_GPIO0_4	TCK	TDO	RSVD_A12	OSPI1_D0	OSPI1_CLK	OSPI1_D4	OSPI0_CSn3	OSPI0_CSn0	OSPI0_LBCLKO	VSS
B	MCU_OSC0_XO	VSS	RSVD_B3	MCU_GPIO0_6	WKUP_UART0_RXD	MCU_GPIO0_14	WKUP_TIMER_IO0	MCU_GPIO0_3	WKUP_I2C0_SCL	TRSTn	WKUP_CLKOUT0	OSPI1_CSn0	OSPI1_LBCLKO	OSPI1_D6	OSPI1_DQS	OSPI0_D0	OSPI0_CLK	OSPI0_D5	OSPI0_DQS
C	OSC1_XI	OSC1_XO	VSS	MCU_GPIO0_5	WKUP_UART0_RTSn	MCU_GPIO0_13	WKUP_TIMER_IO1	MCU_GPIO0_2	EMU0	EMU1	TMS	OSPI1_CSn1	OSPI1_D3	OSPI1_D7	OSPI1_D5	OSPI0_CSn1	OSPI0_D2	OSPI0_D7	VSS
D	VSS	WKUP_LFOSC0_XO	VSS	VSS	MCU_GPIO0_8	WKUP_UART0_CTSn	MCU_GPIO0_16	VSS	MCU_RESETz	TDI	VSS	OSPI1_D1	OSPI1_D2	VSS	OSPI0_CSn2	OSPI0_D3	OSPI0_D1	OSPI0_D6	VSS
E	WKUP_LFOSC0_XI	RSVD_E2	MCU_PORz	RSVD_E4	VSS	CAP_VDDS_CANUART	VDDR_CANUART	CAP_VDDS_MCU	VSS	VSS	VSS	VSS	VDDSHV1	VSS	VSS	OSPI0_D4	VSS	VSS	MCASP3_ACLKX
F	ADC0_AIN0	ADC0_AIN4	MCU_ERRORn	VSS	VDDS_OSC0	VDD_CANUART	VDDSHV_CANUART	VDDSHV_MCU	VDDSHV_MCU	VSS	VSS	VDDSHV1	CAP_VDDS1	VSS	VSS	VSS	MCASP4_AFSX	MCASP4_ACLKX	MCASP4_AXR0
G	ADC0_REFP	ADC0_AIN5	RSVD_G3	VSS	VPP	VSS	VDD_CORE	VSS	VSS	VDDR_CORE	VDD_CORE	VSS	VSS	VDD_CORE	VSS	MCASP4_AXR2	MCASP4_AXR1	MCASP3_AXR0	MCASP3_AFSX
H	ADC0_AIN1	ADC0_REFN	VSS	RESETSTATz	VMON_3P3_SOC	VSS	VDDA_MCU	VMON_ERR_VSYS	VDD_CORE	VDD_CORE	VSS	VDDR_CORE	VDD_CORE	VDDSHV3	CAP_VDDS3	MCASP3_AXR1	MCASP3_AXR3	MCASP3_AXR2	MCASP1_ACLKX
J	ADC0_AIN6	ADC0_AIN7	SPI0_CS0	SPI0_CS1	VDDA_ADC0	VMON_1P8_SOC	VSS	VDDR_CORE	VDDA_PLL0	VDDA_PLL1	VSS	VDD_CORE	VSS	VDDSHV3	VSS	MCASP1_AXR2	MCASP1_AFSX	MCASP1_AXR0	MCASP1_AXR1
K	ADC0_AIN3	ADC0_AIN2	SPI0_D0	SPI0_D1	VDDA_TEMP0	VDDSHV0	VDD_CORE	VSS	VDD_CORE	VDDR_CORE	VSS	VSS	VDD_CORE	VDDSHV3	VSS	MCASP2_AXR1	MCASP1_AXR3	MCASP2_AXR3	MCASP2_AFSX
L	UART0_TXD	UART0_RXD	UART0_RTSn	MCAN0_TX	VSS	CAP_VDDS0	VSS	VDD_CORE	VSS	VSS	VDD_CORE	VDD_CORE	VSS	VSS	VSS	MCASP2_AXR4	MCASP2_AXR0	MCASP2_AXR2	MCASP2_ACLKX
M	SPI0_CLK	I2C1_SDA	I2C0_SCL	MCAN0_RX	VSS	VDDSHV0	VDD_CORE	VSS	VDD_CORE	VDDR_CORE	VDDA_PLL2	VSS	VDD_CORE	VDDR_CORE	VSS	MCASP0_AXR1	MCASP2_AXR5	MCASP0_AXR3	MCASP0_AFSX
N	UART0_CTSn	I2C1_SCL	I2C0_SDA	GPIO1_47	VSS	VSS	VSS	VDDR_CORE	VSS	VDDA_CORE_USB	VDDA_TEMP1	VDDR_CORE	VSS	VSS	VSS	MCASP0_AXR4	MCASP0_AXR0	MCASP0_AXR2	MCASP0_ACLKX
P	EXT_REFCLK1	SPI2_D0	EXTINTn	GPIO1_48	VSS	VSS	VDD_CORE	CAP_VDDS5	VDDSHV5	VDDA_1P8_USB	VDDSHV2	VDDSHV2	VDD_CORE	VSS	VSS	MCASP0_AXR8	MCASP0_AXR5	MCASP0_AXR6	MCASP0_AXR7
R	SPI2_CS2	SPI2_CLK	SPI2_D1	SPI2_CS1	VSS	VSS	VSS	VDDSHV5	VDDA_3P3_USB	VSS	CAP_VDDS2	VSS	VSS	VSS	VSS	MCASP0_AXR12	MCASP0_AXR9	MCASP0_AXR10	MCASP0_AXR11
T	SPI2_CS3	SPI2_CS0	SPI1_D0	SPI1_CS1	VSS	MMC0_CMD	MMC0_DAT5	VSS	VSS	VSS	RGMII1_RD1	RGMII1_RD2	RGMII1_TX_CTL	RGMII1_TD2	RGMII2_RD3	VSS	MCASP0_AXR13	MCASP0_AXR14	MCASP0_AXR15
U	SPI1_CS0	SPI1_CLK	SPI1_D1	VSS	VSS	MMC0_DAT3	MMC0_DAT4	VSS	USB0_VBUS	VSS	MDIO0_MDIO	RGMII1_RD3	RGMII1_TD0	RGMII1_TD3	RGMII2_RD0	RGMII2_TX_CTL	VSS	MLB0_MLBSIG	MLB0_MLBCLK
V	AUDIO_EXT_REFCLK0	GPIO1_49	GPIO1_72	VSS	MMC0_CLK	MMC0_DAT2	MMC0_DAT6	USB0_RCALIB	USB0_DP	VSS	MDIO0_MDC	RGMII1_RX_CTL	RGMII1_TXC	RGMII2_RX_CTL	RGMII2_RD1	RGMII2_TD0	RGMII2_TD2	VSS	MLB0_MLBDAT
W	VSS	USB0_DRVVBUS	VSS	MMC0_DAT0	MMC0_DAT1	VSS	MMC0_DAT7	RSVD_W8	USB0_DM	VSS	RGMII1_RD0	RGMII1_RXC	RGMII1_TD1	RGMII2_RD2	RGMII2_RXC	RGMII2_TD1	RGMII2_TXC	RGMII2_TD3	VSS

Not to scale

5.2 Pin Attributes

The following list describes the contents of each column in the *Pin Attributes* table:

1. **Ball Number:** Ball numbers assigned to each terminal of the Ball Grid Array package.
2. **Ball Name:** Ball name assigned to each terminal of the Ball Grid Array package (this name is typically taken from the primary MUXMODE 0 signal function).
3. **Signal Name:** Signal name of all dedicated and pin multiplexed signal functions associated with a ball.

Note

The *Pin Attributes* table, defines the SoC pin multiplexed signal function implemented at the pin and **does not** define secondary multiplexing of signal functions implemented in device subsystems. Secondary multiplexing of signal functions are not described in this table. For more information on secondary multiplexed signal functions, see the respective peripheral chapter of the device TRM.

4. **Mux Mode:** The MUXMODE value associated with each pin multiplexed signal function:
   - MUXMODE 0 is the primary pin multiplexed signal function. However, the primary pin multiplexed signal function is not necessarily the default pin multiplexed signal function.
   - MUXMODE values 1 through 15 are possible for pin multiplexed signal functions. However, not all MUXMODE values have been implemented. The only valid MUXMODE values are those defined as pin multiplexed signal functions within the Pin Attributes table. Only defined valid values of MUXMODE can be used.
   - Bootstrap defines SOC configuration pins, where the logic state applied to each pin is latched on the rising edge of PORz. These input signal functions are fixed to their respective pins and are not programmable via MUXMODE.
   - An empty box or "-" means Not Applicable.

Note

- The value found in the MUX MODE AFTER RESET column defines the default pin multiplexed signal function selected when PORz is deasserted.
- Configuring two pins to the same pin multiplexed signal function can yield unexpected results and is not supported. This can be prevented with proper software configuration.
- Configuring a pad to an undefined multiplexing mode results in undefined behavior and must be avoided.

5. **Type:** Signal type and direction:
   - I = Input
   - O = Output
   - ID = Input, with open-drain output function
   - OD = Output, with open-drain output function
   - IO = Input, Output, or simultaneously Input and Output
   - IOD = Input, Output, or simultaneously Input and Output, with open-drain output function
   - IOZ = Input, Output, or simultaneously Input and Output, with three-state output function
   - OZ = Output with three-state output function
   - A = Analog
   - CAP = LDO capacitor
   - PWR = Power
   - GND = Ground
6. **Ball State During Reset (RX/TX/PULL):** State of the terminal while PORz or WARMRSTn is asserted, where RX defines the state of the input buffer, TX defines the state of the output buffer, and PULL defines the state of internal pull resistors:
   - RX (Input buffer)
     - Off: The input buffer is **disabled**.

  - On: The input buffer is **enabled**.
- TX (Output buffer)
  - Off: The output buffer is **disabled**.
  - Low: The output buffer is **enabled** and drives V_{OL}.
- PULL (Internal pull resistors)
  - Off: Internal pull resistors are turned **off.**
  - Up: Internal **pull-up** resistor is turned on.
  - Down: Internal **pull-down** resistor is turned on.
  - NA: No internal pull resistor.
- An empty box, or "-" means Not Applicable.

7. **Ball State After Reset (RX/TX/PULL):** State of the terminal after PORz or WARMRSTn is deasserted, where RX defines the state of the input buffer, TX defines the state of the output buffer, and PULL defines the state of internal pull resistors:
   - RX (Input buffer)
     - Off: The input buffer is **disabled**.
     - On: The input buffer is **enabled**.
   - TX (Output buffer)
     - Off: The output buffer is **disabled**.
     - SS: The subsystem selected with MUXMODE determines the output buffer state.
   - PULL (Internal pull resistors)
     - Off: Internal pull resistors are turned **off.**
     - Up: Internal **pull-up resistor** is turned on.
     - Down: Internal **pull-down resistor** is turned on.
     - NA: No internal pull resistor.
   - An empty box, NA, or "-" means Not Applicable.
8. **Mux Mode After Reset:** The value found in this column defines the **default** pin multiplexed signal function after PORz is deasserted.
   - An empty box, NA, or "-" means Not Applicable.
9. **I/O Voltage**: This column describes I/O **operating voltage** options of the respective power supply, when applicable.
   - An empty box, NA, or "-" means Not Applicable.

   For more information, see valid operating voltage range defined for each power supply in *Recommended Operating Conditions*.
10. **Power:** The power supply of the associated I/O, when applicable.
    - An empty box, NA, or "-" means Not Applicable.
11. **Hys:** Indicates if the input buffer associated with this I/O has hysteresis:
    - Yes: Hysteresis Support
    - No: **No** Hysteresis Support
    - An empty box, NA, or "-" means Not Applicable.

    For more information, see the hysteresis values in *Electrical Characteristics*.
12. **Pull Type:** Indicates the presence of an internal pull-up or pull-down resistor. Internal resistors can be enabled or disabled via software.
    - PU: Internal pull-up Only
    - PD: Internal pull-down Only
    - PU/PD: Internal pull-up and pull-down
    - An empty box, NA, or "-" means No internal pull.

Note

Configuring two pins to the same pin multiplexed signal function is not supported as this yields unexpected results. Issues can be easily prevented with the proper software configuration.

When a pad is set into a multiplexing mode which is not defined by pin multiplexing, that pad's behavior is undefined. This must be avoided.

13. **Buffer Type:** This column defines the buffer type associated with a terminal. This information can be used to determine the applicable Electrical Characteristics table.
    - An empty box, NA, or "-" means Not Applicable.

    For electrical characteristics, refer to the appropriate buffer type table in *Electrical Characteristics*.
14. **Pad Configuration Register Name:** This is the name of the device pad/pin configuration register.
15. **Pad Configuration Register Address:** This is the memory address of the device pad/pin configuration register.
16. **Pad Configuration Register Default Value**: This is the default value of the register device pad/pin configuration register after PORz is deasserted.

Table 5-1. Pin Attributes (ANJ Package)

BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/ DOWN TYPE [13]
H2	ADC0_REFN	ADC0_REFN	0	A			0	1.8 V	VDDA_ADC0		Analog	
G1	ADC0_REFP	ADC0_REFP	0	A			0	1.8 V	VDDA_ADC0		Analog	
F1	ADC0_AIN0	ADC0_AIN0	0	A			0	1.8 V	VDDA_ADC0		Analog	
	PADCONFIG172 000F 42B0h 0000 0000h	GPIO1_74	7	I								
H1	ADC0_AIN1	ADC0_AIN1	0	A			0	1.8 V	VDDA_ADC0		Analog	
	PADCONFIG173 000F 42B4h 0000 0000h	GPIO1_75	7	I								
K2	ADC0_AIN2	ADC0_AIN2	0	A			0	1.8 V	VDDA_ADC0		Analog	
	PADCONFIG174 000F 42B8h 0000 0000h	GPIO1_76	7	I								
K1	ADC0_AIN3	ADC0_AIN3	0	A			0	1.8 V	VDDA_ADC0		Analog	
	PADCONFIG175 000F 42BCh 0000 0000h	GPIO1_77	7	I								
F2	ADC0_AIN4	ADC0_AIN4	0	A			0	1.8 V	VDDA_ADC0		Analog	
	PADCONFIG176 000F 42C0h 0000 0000h	GPIO1_78	7	I								
G2	ADC0_AIN5	ADC0_AIN5	0	A			0	1.8 V	VDDA_ADC0		Analog	
	PADCONFIG177 000F 42C4h 0000 0000h	GPIO1_79	7	I								
J1	ADC0_AIN6	ADC0_AIN6	0	A			0	1.8 V	VDDA_ADC0		Analog	
	PADCONFIG178 000F 42C8h 0000 0000h	GPIO1_80	7	I								
J2	ADC0_AIN7	ADC0_AIN7	0	A			0	1.8 V	VDDA_ADC0		Analog	
	PADCONFIG179 000F 42CCh 0000 0000h	GPIO1_81	7	I								
V1	AUDIO_EXT_REFCLK0	AUDIO_EXT_REFCLK0	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
	PADCONFIG104 000F 41A0h 0821 4007h	AUDIO_EXT_REFCLK0	2	IO								
		EPWM1_B	6	IO								
		GPIO1_10	7	IO								
L6	CAP_VDDS0	CAP_VDDS0		PWR				1.8 V/3.3 V				
F13	CAP_VDDS1	CAP_VDDS1		PWR				1.8 V/3.3 V				
R11	CAP_VDDS2	CAP_VDDS2		PWR				1.8 V/3.3 V				
H15	CAP_VDDS3	CAP_VDDS3		PWR				1.8 V/3.3 V				
P8	CAP_VDDS5	CAP_VDDS5		PWR				1.8 V/3.3 V				

Table 5-1. Pin Attributes (ANJ Package) (continued)

BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/ DOWN TYPE [13]
E6	CAP_VDDS_CANUART	CAP_VDDS_CANUART		PWR				1.8 V/3.3 V				
E8	CAP_VDDS_MCU	CAP_VDDS_MCU		PWR				1.8 V/3.3 V				
C9	EMU0 MCU_PADCONFIG30 0408 4078h 1026 4000h	EMU0	0	IO	On / Off / Up	On / Off / Up	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
		MCU_GPIO0_24	7	IO								
		MCU_GPIO0_112	10	IO								
C10	EMU1 MCU_PADCONFIG31 0408 407Ch 1026 4000h	EMU1	0	IO	On / Off / Up	On / Off / Up	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
		MCU_GPIO0_25	7	IO								
		MCU_GPIO0_113	10	IO								
P3	EXTINTn PADCONFIG125 000F 41F4h 0821 4007h	EXTINTn	0	I	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	I2C OPEN DRAIN	
		GPIO1_31	7	IOD								
P1	EXT_REFCLK1 PADCONFIG124 000F 41F0h 0821 4007h	EXT_REFCLK1	0	I	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		SYNC1_OUT	1	O								
		SPI2_CS3	2	IO								
		SYSCLKOUT0	3	O								
		TIMER_IO4	4	IO								
		CLKOUT0	5	O								
		CP_GEMAC_CPTS0_RFT_CLK	6	I								
		GPIO1_30	7	IO								
		ECAP0_IN_APWM_OUT	8	IO								
N4	GPIO1_47 PADCONFIG143 000F 423Ch 0821 4007h	GPIO1_47	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		TIMER_IO5	2	IO								
		UART3_TXD	3	O								
		ADC_EXT_TRIGGER0	4	I								
		MCAN3_TX	5	O								
		GPIO1_47	7	IO								
		SPI1_CS2	8	IO								
P4	GPIO1_48 PADCONFIG144 000F 4240h 0821 4007h	GPIO1_48	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		UART6_RXD	1	I								
		TIMER_IO6	2	IO								
		UART3_RTSn	3	O								
		I2C4_SCL	5	IOD								
		ECAP3_IN_APWM_OUT	6	IO								
		GPIO1_48	7	IO								

Table 5-1. Pin Attributes (ANJ Package) (continued)

BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/ DOWN TYPE [13]
V2	GPIO1_49 PADCONFIG145 000F 4244h 0821 4007h	GPIO1_49	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		UART6_TXD	1	O								
		TIMER_IO7	2	IO								
		UART3_CTSn	3	I								
		ADC_EXT_TRIGGER0	4	I								
		I2C4_SDA	5	IOD								
		GPIO1_49	7	IO								
V3	GPIO1_72 PADCONFIG171 000F 42ACh 0821 4007h	GPIO1_72	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		AUDIO_EXT_REFCLK2	1	IO								
		ECAP4_IN_APWM_OUT	3	IO								
		MCAN3_RX	5	I								
		GPIO1_72	7	IO								
		SPI1_CS3	8	IO								
M3	I2C0_SCL PADCONFIG120 000F 41E0h 0821 4007h	I2C0_SCL	0	IOD	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		SYNC0_OUT	2	O								
		OBSCLK1	3	O								
		UART1_DCDn	4	I								
		EPWM_SOCA	6	O								
		GPIO1_26	7	IO								
		ECAP1_IN_APWM_OUT	8	IO								
		SPI2_CS0	9	IO								
N3	I2C0_SDA PADCONFIG121 000F 41E4h 0821 4007h	I2C0_SDA	0	IOD	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		SPI2_CS2	2	IO								
		TIMER_IO5	3	IO								
		UART1_DSRn	4	I								
		EPWM_SOCB	6	O								
		GPIO1_27	7	IO								
		ECAP2_IN_APWM_OUT	8	IO								
N2	I2C1_SCL PADCONFIG122 000F 41E8h 0821 4007h	I2C1_SCL	0	IOD	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		UART1_RXD	1	I								
		TIMER_IO0	2	IO								
		SPI2_CS1	3	IO								
		EPWM0_SYNCI	4	I								
		ECAP4_IN_APWM_OUT	5	IO								
		GPIO1_28	7	IO								
		MMC0_SDCD	9	I								

Table 5-1. Pin Attributes (ANJ Package) (continued)

BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/ DOWN TYPE [13]
M2	I2C1_SDA PADCONFIG123 000F 41ECh 0821 4007h	I2C1_SDA	0	IOD	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		UART1_TXD	1	O								
		TIMER_IO1	2	IO								
		SPI2_CLK	3	IO								
		EPWM0_SYNCO	4	O								
		ECAP3_IN_APWM_OUT	5	IO								
		GPIO1_29	7	IO								
		MMC0_SDWP	9	I								
M4	MCAN0_RX PADCONFIG119 000F 41DCh 0821 4007h	MCAN0_RX	0	I	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		UART5_TXD	1	O								
		TIMER_IO3	2	IO								
		SYNC3_OUT	3	O								
		UART1_RIn	4	I								
		I2C5_SDA	5	IOD								
		GPIO1_25	7	IO								
		EPWM_TZn_IN4	9	I								
L4	MCAN0_TX PADCONFIG118 000F 41D8h 0821 4007h	MCAN0_TX	0	O	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		UART5_RXD	1	I								
		TIMER_IO2	2	IO								
		SYNC2_OUT	3	O								
		UART1_DTRn	4	O								
		I2C5_SCL	5	IOD								
		GPIO1_24	7	IO								
		EPWM_TZn_IN3	9	I								
N19	MCASP0_ACLKX PADCONFIG15 000F 403Ch 0825 4007h	MCASP0_ACLKX	0	IO	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		TRC_CLK	6	O								
		GPIO0_15	7	IO								
		GPIO1_112	10	IO								
		BOOTMODE00	Bootstrap	IO								
M19	MCASP0_AFSX PADCONFIG16 000F 4040h 0825 4007h	MCASP0_AFSX	0	IO	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		TRC_CTL	6	O								
		GPIO0_16	7	IO								
		GPIO1_113	10	IO								
		BOOTMODE01	Bootstrap	IO								
H19	MCASP1_ACLKX PADCONFIG34 000F 4088h 0821 4007h	MCASP1_ACLKX	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		TRC_DATA8	6	O								
		GPIO0_33	7	IO								

Table 5-1. Pin Attributes (ANJ Package) (continued)

BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/ DOWN TYPE [13]
J17	MCASP1_AFSX PADCONFIG35 000F 408Ch 0821 4007h	MCASP1_AFSX	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		TRC_DATA9	6	O								
		GPIO0_34	7	IO								
L19	MCASP2_ACLKX PADCONFIG40 000F 40A0h 0821 4007h	MCASP2_ACLKX	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		UART6_TXD	3	O								
		TRC_DATA13	6	O								
		GPIO0_39	7	IO								
K19	MCASP2_AFSX PADCONFIG41 000F 40A4h 0821 4007h	MCASP2_AFSX	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		MAIN_ERRORn	5	IO								
		TRC_DATA14	6	O								
		GPIO0_40	7	IO								
E19	MCASP3_ACLKX PADCONFIG48 000F 40C0h 0821 4007h	MCASP3_ACLKX	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		UART3_RXD	6	I								
		GPIO0_47	7	IO								
G19	MCASP3_AFSX PADCONFIG49 000F 40C4h 0821 4007h	MCASP3_AFSX	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		UART3_TXD	6	O								
		GPIO0_48	7	IO								
F18	MCASP4_ACLKX PADCONFIG56 000F 40E0h 0821 4007h	MCASP4_ACLKX	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		UART1_TXD	2	O								
		UART0_CTSn	3	I								
		MCASP3_ACLKR	4	IO								
		UART6_RTSn	6	O								
		GPIO0_55	7	IO								
F17	MCASP4_AFSX PADCONFIG57 000F 40E4h 0821 4007h	MCASP4_AFSX	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		UART1_RXD	2	I								
		UART0_RTSn	3	O								
		MCASP3_AFSR	4	IO								
		UART6_CTSn	6	I								
		GPIO0_56	7	IO								
N17	MCASP0_AXR0 PADCONFIG17 000F 4044h 0825 4007h	MCASP0_AXR0	0	IO	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		TRC_DATA0	6	O								
		GPIO0_17	7	IO								
		GPIO1_114	10	IO								
		BOOTMODE02	Bootstrap	IO								

Table 5-1. Pin Attributes (ANJ Package) (continued)

BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/ DOWN TYPE [13]
M16	MCASP0_AXR1 PADCONFIG18 000F 4048h 0825 4007h	MCASP0_AXR1	0	IO	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		TRC_DATA1	6	O								
		GPIO0_18	7	IO								
		GPIO1_115	10	IO								
		BOOTMODE03	Bootstrap	IO								
N18	MCASP0_AXR2 PADCONFIG19 000F 404Ch 0825 4007h	MCASP0_AXR2	0	IO	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		TRC_DATA2	6	O								
		GPIO0_19	7	IO								
		GPIO1_116	10	IO								
		BOOTMODE04	Bootstrap	IO								
M18	MCASP0_AXR3 PADCONFIG20 000F 4050h 0825 4007h	MCASP0_AXR3	0	IO	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		TRC_DATA3	6	O								
		GPIO0_20	7	IO								
		GPIO1_117	10	IO								
		BOOTMODE05	Bootstrap	IO								
N16	MCASP0_AXR4 PADCONFIG21 000F 4054h 0825 4007h	MCASP0_AXR4	0	IO	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		TRC_DATA4	6	O								
		GPIO0_21	7	IO								
		GPIO1_118	10	IO								
		BOOTMODE06	Bootstrap	IO								
P17	MCASP0_AXR5 PADCONFIG22 000F 4058h 0825 4007h	MCASP0_AXR5	0	IO	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		TRC_DATA5	6	O								
		GPIO0_22	7	IO								
		GPIO1_119	10	IO								
		BOOTMODE07	Bootstrap	IO								
P18	MCASP0_AXR6 PADCONFIG23 000F 405Ch 0825 4007h	MCASP0_AXR6	0	IO	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		UART2_RXD	2	I								
		GPIO0_23	7	IO								
		GPIO1_120	10	IO								
		BOOTMODE08	Bootstrap	IO								
P19	MCASP0_AXR7 PADCONFIG24 000F 4060h 0825 4007h	MCASP0_AXR7	0	IO	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		UART2_TXD	2	O								
		GPIO0_24	7	IO								
		GPIO1_121	10	IO								
		BOOTMODE09	Bootstrap	IO								

Table 5-1. Pin Attributes (ANJ Package) (continued)

BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/ DOWN TYPE [13]
P16	MCASP0_AXR8 PADCONFIG25 000F 4064h 0825 4007h	MCASP0_AXR8	0	IO	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		UART3_RXD	2	I								
		GPIO0_25	7	IO								
		OBSCLK0	8	O								
		GPIO1_122	10	IO								
		BOOTMODE10	Bootstrap	IO								
R17	MCASP0_AXR9 PADCONFIG26 000F 4068h 0825 4007h	MCASP0_AXR9	0	IO	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		UART3_TXD	2	O								
		TRC_DATA23	6	O								
		GPIO0_26	7	IO								
		BOOTMODE11	Bootstrap	IO								
R18	MCASP0_AXR10 PADCONFIG27 000F 406Ch 0825 4007h	MCASP0_AXR10	0	IO	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		UART4_RXD	2	I								
		MCASP1_AXR9	3	IO								
		MCASP4_ACLKR	4	IO								
		TRC_DATA22	6	O								
		GPIO0_27	7	IO								
		GPIO1_123	10	IO								
		BOOTMODE12	Bootstrap	IO								
R19	MCASP0_AXR11 PADCONFIG28 000F 4070h 0825 4007h	MCASP0_AXR11	0	IO	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		UART4_TXD	2	O								
		MCASP1_AXR8	3	IO								
		MCASP4_AFSR	4	IO								
		TRC_DATA21	6	O								
		GPIO0_28	7	IO								
		GPIO1_124	10	IO								
		BOOTMODE13	Bootstrap	IO								
R16	MCASP0_AXR12 PADCONFIG29 000F 4074h 0825 4007h	MCASP0_AXR12	0	IO	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		UART5_RXD	2	I								
		MCASP1_AXR7	3	IO								
		MCASP0_ACLKR	4	IO								
		TRC_DATA20	6	O								
		GPIO0_29	7	IO								
		UART2_CTSn	8	I								
		GPIO1_125	10	IO								
		BOOTMODE14	Bootstrap	IO								

Table 5-1. Pin Attributes (ANJ Package) (continued)

BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/ DOWN TYPE [13]
T17	MCASP0_AXR13 PADCONFIG30 000F 4078h 0825 4007h	MCASP0_AXR13	0	IO	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		UART5_TXD	2	O								
		MCASP1_AXR6	3	IO								
		MCASP0_AFSR	4	IO								
		TRC_DATA19	6	O								
		GPIO0_30	7	IO								
		UART2_RTSn	8	O								
		GPIO1_126	10	IO								
		BOOTMODE15	Bootstrap	IO								
T18	MCASP0_AXR14 PADCONFIG31 000F 407Ch 0821 4007h	MCASP0_AXR14	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		MCASP1_AXR5	3	IO								
		MCASP1_ACLKR	4	IO								
		MCASP3_AXR4	5	IO								
		TRC_DATA6	6	O								
		GPIO0_31	7	IO								
		GPIO1_127	10	IO								
T19	MCASP0_AXR15 PADCONFIG33 000F 4084h 0821 4007h	MCASP0_AXR15	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		AUDIO_EXT_REFCLK2	2	IO								
		MCASP1_AXR4	3	IO								
		MCASP1_AFSR	4	IO								
		MCASP3_AXR5	5	IO								
		TRC_DATA7	6	O								
		GPIO0_32	7	IO								
J18	MCASP1_AXR0 PADCONFIG36 000F 4090h 0821 4007h	MCASP1_AXR0	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		TRC_DATA10	6	O								
		GPIO0_35	7	IO								
J19	MCASP1_AXR1 PADCONFIG37 000F 4094h 0821 4007h	MCASP1_AXR1	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		TRC_DATA11	6	O								
		GPIO0_36	7	IO								
J16	MCASP1_AXR2 PADCONFIG38 000F 4098h 0821 4007h	MCASP1_AXR2	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		TRC_DATA12	6	O								
		GPIO0_37	7	IO								
K17	MCASP1_AXR3 PADCONFIG39 000F 409Ch 0821 4007h	MCASP1_AXR3	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		UART6_RXD	3	I								
		GPIO0_38	7	IO								

Table 5-1. Pin Attributes (ANJ Package) (continued)

BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/ DOWN TYPE [13]
L17	MCASP2_AXR0 PADCONFIG42 000F 40A8h 0821 4007h	MCASP2_AXR0	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		TRC_DATA15	6	O								
		GPIO0_41	7	IO								
K16	MCASP2_AXR1 PADCONFIG43 000F 40ACh 0821 4007h	MCASP2_AXR1	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		TRC_DATA16	6	O								
		GPIO0_42	7	IO								
L18	MCASP2_AXR2 PADCONFIG44 000F 40B0h 0821 4007h	MCASP2_AXR2	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		I2C2_SCL	1	IOD								
		UART4_RXD	3	I								
		MCAN1_TX	5	O								
		TRC_DATA17	6	O								
		GPIO0_43	7	IO								
K18	MCASP2_AXR3 PADCONFIG45 000F 40B4h 0821 4007h	MCASP2_AXR3	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		I2C2_SDA	1	IOD								
		UART4_TXD	3	O								
		MCAN1_RX	5	I								
		TRC_DATA18	6	O								
		GPIO0_44	7	IO								
L16	MCASP2_AXR4 PADCONFIG46 000F 40B8h 0821 4007h	MCASP2_AXR4	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		UART4_RTSn	3	O								
		UART2_RXD	6	I								
		GPIO0_45	7	IO								
M17	MCASP2_AXR5 PADCONFIG47 000F 40BCh 0821 4007h	MCASP2_AXR5	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		AUDIO_EXT_REFCLK1	2	IO								
		UART4_CTSn	3	I								
		UART2_TXD	6	O								
		GPIO0_46	7	IO								
G18	MCASP3_AXR0 PADCONFIG50 000F 40C8h 0821 4007h	MCASP3_AXR0	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		UART4_RXD	6	I								
		GPIO0_49	7	IO								
H16	MCASP3_AXR1 PADCONFIG51 000F 40CCh 0821 4007h	MCASP3_AXR1	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		UART4_TXD	6	O								
		GPIO0_50	7	IO								
H18	MCASP3_AXR2 PADCONFIG52 000F 40D0h 0821 4007h	MCASP3_AXR2	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		UART5_RXD	6	I								
		GPIO0_51	7	IO								

Table 5-1. Pin Attributes (ANJ Package) (continued)

BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/ DOWN TYPE [13]
H17	MCASP3_AXR3 PADCONFIG53 000F 40D4h 0821 4007h	MCASP3_AXR3	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		UART5_TXD	6	O								
		GPIO0_52	7	IO								
F19	MCASP4_AXR0 PADCONFIG58 000F 40E8h 0821 4007h	MCASP4_AXR0	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		UART6_RXD	2	I								
		UART0_RXD	3	I								
		UART5_RTSn	6	O								
		GPIO0_57	7	IO								
G17	MCASP4_AXR1 PADCONFIG59 000F 40ECh 0821 4007h	MCASP4_AXR1	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		I2C6_SCL	2	IOD								
		MCASP2_ACLKR	4	IO								
		UART5_CTSn	6	I								
		GPIO0_58	7	IO								
G16	MCASP4_AXR2 PADCONFIG60 000F 40F0h 0821 4007h	MCASP4_AXR2	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		I2C6_SDA	2	IOD								
		MCASP1_AXR10	3	IO								
		MCASP2_AFSR	4	IO								
		UART3_RTSn	6	O								
		GPIO0_59	7	IO								
F3	MCU_ERRORn MCU_PADCONFIG24 0408 4060h 0004 4000h	MCU_ERRORn	0	IO	Off / Off / Down	On / SS / Down	0	1.8 V	VDDS_OSC0	Yes	LVCMOS	PU/PD
C8	MCU_GPIO0_2 MCU_PADCONFIG2 0408 4008h 0821 4007h	MCU_GPIO0_2	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
		MCU_GPIO0_2	7	IO								
B8	MCU_GPIO0_3 MCU_PADCONFIG3 0408 400Ch 0821 4007h	MCU_GPIO0_3	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
		MCU_GPIO0_3	7	IO								
A9	MCU_GPIO0_4 MCU_PADCONFIG4 0408 4010h 0821 4007h	MCU_GPIO0_4	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
		MCU_GPIO0_4	7	IO								
C4	MCU_GPIO0_5 MCU_PADCONFIG5 0408 4014h 0821 4007h	MCU_GPIO0_5	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_CANUART	Yes	LVCMOS	PU/PD
		MCAN0_TX	2	O								
		MCU_GPIO0_5	7	IO								

Table 5-1. Pin Attributes (ANJ Package) (continued)

BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/ DOWN TYPE [13]
B4	MCU_GPIO0_6 MCU_PADCONFIG6 0408 4018h 0821 4007h	MCU_GPIO0_6	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_CANUART	Yes	LVCMOS	PU/PD
		MCAN0_RX	2	I								
		MCU_GPIO0_6	7	IO								
A4	MCU_GPIO0_7 MCU_PADCONFIG7 0408 401Ch 0821 4007h	MCU_GPIO0_7	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_CANUART	Yes	LVCMOS	PU/PD
		MCAN1_TX	2	O								
		MCU_GPIO0_7	7	IO								
D5	MCU_GPIO0_8 MCU_PADCONFIG8 0408 4020h 0821 4007h	MCU_GPIO0_8	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_CANUART	Yes	LVCMOS	PU/PD
		MCAN1_RX	2	I								
		MCU_GPIO0_8	7	IO								
C6	MCU_GPIO0_13 MCU_PADCONFIG13 0408 4034h 0821 4007h	MCU_GPIO0_13	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_CANUART	Yes	LVCMOS	PU/PD
		WKUP_TIMER_IO0	1	IO								
		MCAN4_TX	2	O								
		UART3_RXD	3	I								
		MCU_GPIO0_13	7	IO								
B6	MCU_GPIO0_14 MCU_PADCONFIG14 0408 4038h 0821 4007h	MCU_GPIO0_14	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_CANUART	Yes	LVCMOS	PU/PD
		MCAN4_RX	2	I								
		UART3_TXD	3	O								
		MCU_GPIO0_14	7	IO								
A6	MCU_GPIO0_15 MCU_PADCONFIG15 0408 403Ch 0821 4007h	MCU_GPIO0_15	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_CANUART	Yes	LVCMOS	PU/PD
		UART2_RXD	3	I								
		MCU_EXT_REFCLK0	4	I								
		MCU_GPIO0_15	7	IO								
D7	MCU_GPIO0_16 MCU_PADCONFIG16 0408 4040h 0821 4007h	MCU_GPIO0_16	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_CANUART	Yes	LVCMOS	PU/PD
		UART2_TXD	3	O								
		MCU_GPIO0_16	7	IO								
A2	MCU_OSC0_XI	MCU_OSC0_XI	0	I				1.8 V	VDDS_OSC0		N16FFC_HFXOSC	
B1	MCU_OSC0_XO	MCU_OSC0_XO	0	O				1.8 V	VDDS_OSC0		N16FFC_HFXOSC	
E3	MCU_PORz MCU_PADCONFIG22 0408 4058h 0801 4000h	MCU_PORz	0	I			0	1.8 V	VDDS_OSC0	Yes	LVCMOS	PU/PD
D9	MCU_RESETz MCU_PADCONFIG21 0408 4054h 1026 4000h	MCU_RESETz	0	I	On / Off / Up	On / Off / Up	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD

Table 5-1. Pin Attributes (ANJ Package) (continued)

BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/ DOWN TYPE [13]
V11	MDIO0_MDC PADCONFIG88 000F 4160h 0821 4007h	MDIO0_MDC	0	O	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		GPIO0_86	7	IO								
U11	MDIO0_MDIO PADCONFIG87 000F 415Ch 0821 4007h	MDIO0_MDIO	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		GPIO0_85	7	IO								
U19	MLB0_MLBCLK PADCONFIG64 000F 4100h 0821 4007h	MLB0_MLBCLK	0	I	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		MCASP4_AXR4	1	IO								
		I2C5_SCL	2	IOD								
		UART0_TXD	3	O								
		UART2_RTSn	6	O								
		GPIO0_63	7	IO								
V19	MLB0_MLBDAT PADCONFIG65 000F 4104h 0821 4007h	MLB0_MLBDAT	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		MCASP4_AXR5	1	IO								
		I2C5_SDA	2	IOD								
		UART2_CTSn	6	I								
		GPIO0_64	7	IO								
U18	MLB0_MLBSIG PADCONFIG63 000F 40FCh 0821 4007h	MLB0_MLBSIG	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		MCASP4_AXR3	1	IO								
		UART6_TXD	2	O								
		ECAP5_IN_APWM_OUT	3	IO								
		UART3_CTSn	6	I								
		GPIO0_62	7	IO								
V5	MMC0_CLK PADCONFIG134 000F 4218h 0821 4007h	MMC0_CLK	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV5	Yes	SDIO	PU/PD
		I2C3_SCL	1	IOD								
		EPWM2_A	2	IO								
		MCAN0_TX	3	O								
		SPI4_CS1	5	IO								
		TIMER_IO4	6	IO								
		GPIO1_40	7	IO								

Table 5-1. Pin Attributes (ANJ Package) (continued)

BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/ DOWN TYPE [13]
T6	MMC0_CMD PADCONFIG136 000F 4220h 0821 4007h	MMC0_CMD	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV5	Yes	SDIO	PU/PD
		I2C3_SDA	1	IOD								
		EPWM2_B	2	IO								
		MCAN0_RX	3	I								
		SPI4_CS2	5	IO								
		TIMER_IO5	6	IO								
		GPIO1_41	7	IO								
W4	MMC0_DAT0 PADCONFIG133 000F 4214h 0821 4007h	MMC0_DAT0	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV5	Yes	SDIO	PU/PD
		UART3_CTSn	1	I								
		EPWM_TZn_IN1	2	I								
		MCAN4_RX	3	I								
		SPI3_CLK	6	IO								
		GPIO1_39	7	IO								
W5	MMC0_DAT1 PADCONFIG132 000F 4210h 0821 4007h	MMC0_DAT1	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV5	Yes	SDIO	PU/PD
		UART3_RTSn	1	O								
		EPWM1_B	2	IO								
		MCAN4_TX	3	O								
		SPI4_CS3	5	IO								
		SPI3_CS0	6	IO								
		GPIO1_38	7	IO								
V6	MMC0_DAT2 PADCONFIG131 000F 420Ch 0821 4007h	MMC0_DAT2	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV5	Yes	SDIO	PU/PD
		UART3_TXD	1	O								
		EPWM1_A	2	IO								
		MCAN3_RX	3	I								
		SPI4_CLK	5	IO								
		TIMER_IO0	6	IO								
		GPIO1_37	7	IO								
U6	MMC0_DAT3 PADCONFIG130 000F 4208h 0821 4007h	MMC0_DAT3	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV5	Yes	SDIO	PU/PD
		UART3_RXD	1	I								
		EPWM0_B	2	IO								
		MCAN3_TX	3	O								
		SPI4_CS0	5	IO								
		SPI3_CS2	6	IO								
		GPIO1_36	7	IO								

Table 5-1. Pin Attributes (ANJ Package) (continued)

BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/ DOWN TYPE [13]
U7	MMC0_DAT4 PADCONFIG129 000F 4204h 0821 4007h	MMC0_DAT4	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV5	Yes	SDIO	PU/PD
		UART2_CTSn	1	I								
		EPWM0_A	2	IO								
		MCAN2_RX	3	I								
		I2C6_SDA	5	IOD								
		SPI3_D1	6	IO								
		GPIO1_35	7	IO								
T7	MMC0_DAT5 PADCONFIG128 000F 4200h 0821 4007h	MMC0_DAT5	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV5	Yes	SDIO	PU/PD
		UART2_RTSn	1	O								
		EPWM_TZn_IN2	2	I								
		MCAN2_TX	3	O								
		I2C6_SCL	5	IOD								
		SPI3_D0	6	IO								
		GPIO1_34	7	IO								
V7	MMC0_DAT6 PADCONFIG127 000F 41FCh 0821 4007h	MMC0_DAT6	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV5	Yes	SDIO	PU/PD
		UART2_TXD	1	O								
		EPWM0_SYNCO	2	O								
		MCAN1_RX	3	I								
		SPI4_D1	5	IO								
		SPI3_CS3	6	IO								
		GPIO1_33	7	IO								
W7	MMC0_DAT7 PADCONFIG126 000F 41F8h 0821 4007h	MMC0_DAT7	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV5	Yes	SDIO	PU/PD
		UART2_RXD	1	I								
		EPWM0_SYNCI	2	I								
		MCAN1_TX	3	O								
		SPI4_D0	5	IO								
		SPI3_CS1	6	IO								
		GPIO1_32	7	IO								
C1	OSC1_XI	OSC1_XI	0	I				1.8 V	VDDS_OSC0		N16FFC_HFXOSC	
C2	OSC1_XO	OSC1_XO	0	O				1.8 V	VDDS_OSC0		N16FFC_HFXOSC	
B17	OSPI0_CLK PADCONFIG0 000F 4000h 0821 4007h	OSPI0_CLK	0	O	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		GPIO0_0	7	IO								

Table 5-1. Pin Attributes (ANJ Package) (continued)

BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/ DOWN TYPE [13]
B19	OSPI0_DQS PADCONFIG2 000F 4008h 0821 4007h	OSPI0_DQS	0	I	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		UART5_CTSn	5	I								
		GPIO0_2	7	IO								
		HYPERBUS0_INTn	8	I								
A18	OSPI0_LBCLKO PADCONFIG1 000F 4004h 0821 4007h	OSPI0_LBCLKO	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		UART5_RTSn	5	O								
		GPIO0_1	7	IO								
		HYPERBUS0_RESETOn	8	I								
A14	OSPI1_CLK PADCONFIG66 000F 4108h 0821 4007h	OSPI1_CLK	0	O	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		UART5_RXD	3	I								
		GPIO0_65	7	IO								
		HYPERBUS0_CK	8	O								
B15	OSPI1_DQS PADCONFIG68 000F 4110h 0821 4007h	OSPI1_DQS	0	I	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		GPIO0_67	7	IO								
		HYPERBUS0_RWDS	8	IO								
B13	OSPI1_LBCLKO PADCONFIG67 000F 410Ch 0821 4007h	OSPI1_LBCLKO	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		UART5_TXD	3	O								
		GPIO0_66	7	IO								
		HYPERBUS0_CKn	8	O								
A17	OSPI0_CSn0 PADCONFIG11 000F 402Ch 0821 4007h	OSPI0_CSn0	0	O	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		GPIO0_11	7	IO								
C16	OSPI0_CSn1 PADCONFIG12 000F 4030h 0821 4007h	OSPI0_CSn1	0	O	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		GPIO0_12	7	IO								
D15	OSPI0_CSn2 PADCONFIG13 000F 4034h 0821 4007h	OSPI0_CSn2	0	O	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		SPI1_CS1	1	IO								
		OSPI0_RESET_OUT1	2	O								
		HYPERBUS0_WPn	4	O								
		UART5_RXD	5	I								
		ADC_EXT_TRIGGER0	6	I								
		GPIO0_13	7	IO								
		HYPERBUS0_RESETOn	8	I								
		OSPI1_RESET_OUT0	9	O								

Table 5-1. Pin Attributes (ANJ Package) (continued)

BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/ DOWN TYPE [13]
A16	OSPI0_CSn3 PADCONFIG14 000F 4038h 0821 4007h	OSPI0_CSn3	0	O	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		OSPI0_RESET_OUT0	1	O								
		OSPI0_ECC_FAIL	2	I								
		HYPERBUS0_RESETn	3	O								
		HYPERBUS0_WPn	4	O								
		UART5_TXD	5	O								
		GPIO0_14	7	IO								
		HYPERBUS0_INTn	8	I								
		OSPI1_RESET_OUT1	9	O								
B16	OSPI0_D0 PADCONFIG3 000F 400Ch 0821 4007h	OSPI0_D0	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		GPIO0_3	7	IO								
D17	OSPI0_D1 PADCONFIG4 000F 4010h 0821 4007h	OSPI0_D1	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		GPIO0_4	7	IO								
C17	OSPI0_D2 PADCONFIG5 000F 4014h 0821 4007h	OSPI0_D2	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		GPIO0_5	7	IO								
D16	OSPI0_D3 PADCONFIG6 000F 4018h 0821 4007h	OSPI0_D3	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		GPIO0_6	7	IO								
E16	OSPI0_D4 PADCONFIG7 000F 401Ch 0821 4007h	OSPI0_D4	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		SPI1_CS0	1	IO								
		UART6_RXD	3	I								
		GPIO0_7	7	IO								
B18	OSPI0_D5 PADCONFIG8 000F 4020h 0821 4007h	OSPI0_D5	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		SPI1_CLK	1	IO								
		UART6_TXD	3	O								
		GPIO0_8	7	IO								
D18	OSPI0_D6 PADCONFIG9 000F 4024h 0821 4007h	OSPI0_D6	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		SPI1_D0	1	IO								
		UART6_RTSn	3	O								
		GPIO0_9	7	IO								

Table 5-1. Pin Attributes (ANJ Package) (continued)

BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/ DOWN TYPE [13]
C18	OSPI0_D7 PADCONFIG10 000F 4028h 0821 4007h	OSPI0_D7	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		SPI1_D1	1	IO								
		UART6_CTSn	3	I								
		GPIO0_10	7	IO								
B12	OSPI1_CSn0 PADCONFIG73 000F 4124h 0821 4007h	OSPI1_CSn0	0	O	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		UART4_RXD	3	I								
		GPIO0_72	7	IO								
		HYPERBUS0_CSn0	8	O								
C12	OSPI1_CSn1 PADCONFIG74 000F 4128h 0821 4007h	OSPI1_CSn1	0	O	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		UART4_TXD	3	O								
		HYPERBUS0_CSn1	4	O								
		GPIO0_92	7	IO								
		HYPERBUS0_RESETn	8	O								
		OSPI1_ECC_FAIL	9	I								
A13	OSPI1_D0 PADCONFIG69 000F 4114h 0821 4007h	OSPI1_D0	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		GPIO0_68	7	IO								
		HYPERBUS0_DQ0	8	IO								
D12	OSPI1_D1 PADCONFIG70 000F 4118h 0821 4007h	OSPI1_D1	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		UART6_RXD	3	I								
		GPIO0_69	7	IO								
		HYPERBUS0_DQ1	8	IO								
D13	OSPI1_D2 PADCONFIG71 000F 411Ch 0821 4007h	OSPI1_D2	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		GPIO0_70	7	IO								
		HYPERBUS0_DQ2	8	IO								
C13	OSPI1_D3 PADCONFIG72 000F 4120h 0821 4007h	OSPI1_D3	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		UART6_TXD	3	O								
		GPIO0_71	7	IO								
		HYPERBUS0_DQ3	8	IO								
A15	OSPI1_D4 PADCONFIG180 000F 42D0h 0821 4007h	OSPI1_D4	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		I2C2_SCL	3	IOD								
		GPIO1_82	7	IO								
		HYPERBUS0_DQ4	8	IO								
C15	OSPI1_D5 PADCONFIG181 000F 42D4h 0821 4007h	OSPI1_D5	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		I2C2_SDA	3	IOD								
		GPIO1_83	7	IO								
		HYPERBUS0_DQ5	8	IO								

Table 5-1. Pin Attributes (ANJ Package) (continued)

BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/ DOWN TYPE [13]
B14	OSPI1_D6 PADCONFIG182 000F 42D8h 0821 4007h	OSPI1_D6	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		UART4_RTSn	3	O								
		GPIO1_84	7	IO								
		HYPERBUS0_DQ6	8	IO								
C14	OSPI1_D7 PADCONFIG183 000F 42DCh 0821 4007h	OSPI1_D7	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		UART4_CTSn	3	I								
		GPIO1_85	7	IO								
		HYPERBUS0_DQ7	8	IO								
A7	PMIC_LPM_EN0 MCU_PADCONFIG32 0408 4080h 0801 4000h	PMIC_LPM_EN0	0	O	Off / Off / Off	Off / SS / Off	0	1.8 V/3.3 V	VDDSHV_CANUART	Yes	LVCMOS	PU/PD
		MCU_GPIO0_22	7	IO								
H4	RESETSTATz PADCONFIG147 000F 424Ch 0801 4000h	RESETSTATz	0	O	Off / Low / Off	Off / SS / Off	0	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
W12	RGMII1_RXC PADCONFIG82 000F 4148h 0821 4007h	RGMII1_RXC	0	I	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		RMII1_REF_CLK	1	I								
		GPIO0_80	7	IO								
V12	RGMII1_RX_CTL PADCONFIG81 000F 4144h 0821 4007h	RGMII1_RX_CTL	0	I	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		RMII1_RX_ER	1	I								
		GPIO0_79	7	IO								
V13	RGMII1_TXC PADCONFIG76 000F 4130h 0821 4007h	RGMII1_TXC	0	O	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		RMII1_CRS_DV	1	I								
		GPIO0_74	7	IO								
T13	RGMII1_TX_CTL PADCONFIG75 000F 412Ch 0821 4007h	RGMII1_TX_CTL	0	O	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		RMII1_TX_EN	1	O								
		GPIO0_73	7	IO								
W15	RGMII2_RXC PADCONFIG96 000F 4180h 0821 4007h	RGMII2_RXC	0	I	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		RMII2_REF_CLK	1	I								
		EPWM2_B	2	IO								
		GPIO1_2	7	IO								
V14	RGMII2_RX_CTL PADCONFIG95 000F 417Ch 0821 4007h	RGMII2_RX_CTL	0	I	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		RMII2_RX_ER	1	I								
		EPWM2_A	2	IO								
		GPIO1_1	7	IO								

Table 5-1. Pin Attributes (ANJ Package) (continued)

BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/ DOWN TYPE [13]
W17	RGMII2_TXC PADCONFIG90 000F 4168h 0821 4007h	RGMII2_TXC	0	O	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		RMII2_CRS_DV	1	I								
		I2C2_SDA	2	IOD								
		GPIO0_88	7	IO								
U16	RGMII2_TX_CTL PADCONFIG89 000F 4164h 0821 4007h	RGMII2_TX_CTL	0	O	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		RMII2_TX_EN	1	O								
		I2C2_SCL	2	IOD								
		GPIO0_87	7	IO								
W11	RGMII1_RD0 PADCONFIG83 000F 414Ch 0821 4007h	RGMII1_RD0	0	I	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		RMII1_RXD0	1	I								
		GPIO0_81	7	IO								
T11	RGMII1_RD1 PADCONFIG84 000F 4150h 0821 4007h	RGMII1_RD1	0	I	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		RMII1_RXD1	1	I								
		GPIO0_82	7	IO								
T12	RGMII1_RD2 PADCONFIG85 000F 4154h 0821 4007h	RGMII1_RD2	0	I	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		GPIO0_83	7	IO								
U12	RGMII1_RD3 PADCONFIG86 000F 4158h 0821 4007h	RGMII1_RD3	0	I	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		GPIO0_84	7	IO								
U13	RGMII1_TD0 PADCONFIG77 000F 4134h 0821 4007h	RGMII1_TD0	0	O	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		RMII1_TXD0	1	O								
		GPIO0_75	7	IO								
W13	RGMII1_TD1 PADCONFIG78 000F 4138h 0821 4007h	RGMII1_TD1	0	O	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		RMII1_TXD1	1	O								
		GPIO0_76	7	IO								
T14	RGMII1_TD2 PADCONFIG79 000F 413Ch 0821 4007h	RGMII1_TD2	0	O	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		GPIO0_77	7	IO								
U14	RGMII1_TD3 PADCONFIG80 000F 4140h 0821 4007h	RGMII1_TD3	0	O	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		CLKOUT0	1	O								
		GPIO0_78	7	IO								

Table 5-1. Pin Attributes (ANJ Package) (continued)

BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/ DOWN TYPE [13]
U15	RGMII2_RD0 PADCONFIG97 000F 4184h 0821 4007h	RGMII2_RD0	0	I	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		RMII2_RXD0	1	I								
		I2C3_SCL	2	IOD								
		GPIO1_3	7	IO								
V15	RGMII2_RD1 PADCONFIG98 000F 4188h 0821 4007h	RGMII2_RD1	0	I	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		RMII2_RXD1	1	I								
		I2C3_SDA	2	IOD								
		GPIO1_4	7	IO								
W14	RGMII2_RD2 PADCONFIG99 000F 418Ch 0821 4007h	RGMII2_RD2	0	I	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		GPIO1_5	7	IO								
T15	RGMII2_RD3 PADCONFIG100 000F 4190h 0821 4007h	RGMII2_RD3	0	I	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		AUDIO_EXT_REFCLK0	2	IO								
		GPIO1_6	7	IO								
V16	RGMII2_TD0 PADCONFIG91 000F 416Ch 0821 4007h	RGMII2_TD0	0	O	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		RMII2_TXD0	1	O								
		EPWM0_A	2	IO								
		GPIO0_89	7	IO								
W16	RGMII2_TD1 PADCONFIG92 000F 4170h 0821 4007h	RGMII2_TD1	0	O	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		RMII2_TXD1	1	O								
		EPWM0_B	2	IO								
		GPIO0_90	7	IO								
V17	RGMII2_TD2 PADCONFIG93 000F 4174h 0821 4007h	RGMII2_TD2	0	O	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		EPWM1_A	2	IO								
		GPIO0_91	7	IO								
W18	RGMII2_TD3 PADCONFIG94 000F 4178h 0821 4007h	RGMII2_TD3	0	O	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		CLKOUT0	1	O								
		EPWM1_B	2	IO								
		GPIO1_0	7	IO								
A3	RSVD_A3	RSVD_A3	0	RSVD					RSVD		RSVD	
A12	RSVD_A12	RSVD_A12	0	RSVD					RSVD		RSVD	
B3	RSVD_B3	RSVD_B3	0	RSVD					RSVD		RSVD	
E2	RSVD_E2	RSVD_E2	0	RSVD					RSVD		RSVD	
E4	RSVD_E4	RSVD_E4	0	RSVD					RSVD		RSVD	
G3	RSVD_G3	RSVD_G3	0	RSVD					RSVD		RSVD	
W8	RSVD_W8	RSVD_W8	0	RSVD					RSVD		RSVD	

Table 5-1. Pin Attributes (ANJ Package) (continued)

BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/ DOWN TYPE [13]
M1	SPI0_CLK PADCONFIG111 000F 41BCh 0821 4007h	SPI0_CLK	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		CP_GEMAC_CPTS0_TS_SYNC	1	O								
		EPWM1_A	2	IO								
		GPIO1_17	7	IO								
U2	SPI1_CLK PADCONFIG139 000F 422Ch 0821 4007h	SPI1_CLK	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		CP_GEMAC_CPTS0_HW1TSPUSH	1	I								
		TIMER_IO2	2	IO								
		UART2_RTSn	3	O								
		ECAP1_IN_APWM_OUT	4	IO								
		I2C5_SCL	5	IOD								
		GPIO1_44	7	IO								
R2	SPI2_CLK PADCONFIG108 000F 41B0h 0821 4007h	SPI2_CLK	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		UART1_TXD	2	O								
		EPWM0_B	6	IO								
		GPIO1_14	7	IO								
J3	SPI0_CS0 PADCONFIG109 000F 41B4h 0821 4007h	SPI0_CS0	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		EPWM0_A	2	IO								
		GPIO1_15	7	IO								
J4	SPI0_CS1 PADCONFIG110 000F 41B8h 0821 4007h	SPI0_CS1	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		CP_GEMAC_CPTS0_TS_COMP	1	O								
		EPWM0_B	2	IO								
		ECAP0_IN_APWM_OUT	3	IO								
		MAIN_ERRORn	5	IO								
		GPIO1_16	7	IO								
		EPWM_TZn_IN5	9	I								
K3	SPI0_D0 PADCONFIG112 000F 41C0h 0821 4007h	SPI0_D0	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		CP_GEMAC_CPTS0_HW1TSPUSH	1	I								
		EPWM1_B	2	IO								
		GPIO1_18	7	IO								
K4	SPI0_D1 PADCONFIG113 000F 41C4h 0821 4007h	SPI0_D1	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		CP_GEMAC_CPTS0_HW2TSPUSH	1	I								
		EPWM_TZn_IN0	2	I								
		GPIO1_19	7	IO								

Table 5-1. Pin Attributes (ANJ Package) (continued)

BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/ DOWN TYPE [13]
U1	SPI1_CS0 PADCONFIG137 000F 4224h 0821 4007h	SPI1_CS0	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		CP_GEMAC_CPTS0_TS_COMP	1	O								
		TIMER_IO0	2	IO								
		UART2_RXD	3	I								
		ECAP4_IN_APWM_OUT	4	IO								
		GPIO1_42	7	IO								
T4	SPI1_CS1 PADCONFIG138 000F 4228h 0821 4007h	SPI1_CS1	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		CP_GEMAC_CPTS0_TS_SYNC	1	O								
		TIMER_IO1	2	IO								
		UART2_TXD	3	O								
		ECAP5_IN_APWM_OUT	4	IO								
		GPIO1_43	7	IO								
T3	SPI1_D0 PADCONFIG140 000F 4230h 0821 4007h	SPI1_D0	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		CP_GEMAC_CPTS0_HW2TSPUSH	1	I								
		TIMER_IO3	2	IO								
		UART2_CTSn	3	I								
		ECAP2_IN_APWM_OUT	4	IO								
		I2C5_SDA	5	IOD								
		GPIO1_45	7	IO								
U3	SPI1_D1 PADCONFIG141 000F 4234h 0821 4007h	SPI1_D1	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		TIMER_IO4	2	IO								
		UART3_RXD	3	I								
		ECAP3_IN_APWM_OUT	4	IO								
		GPIO1_46	7	IO								
T2	SPI2_CS0 PADCONFIG107 000F 41ACh 0821 4007h	SPI2_CS0	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		UART1_RXD	2	I								
		EPWM0_A	6	IO								
		GPIO1_13	7	IO								
R4	SPI2_CS1 PADCONFIG105 000F 41A4h 0821 4007h	SPI2_CS1	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		ECAP2_IN_APWM_OUT	2	IO								
		MCAN4_TX	3	O								
		I2C4_SCL	5	IOD								
		GPIO1_11	7	IO								

Table 5-1. Pin Attributes (ANJ Package) (continued)

BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/ DOWN TYPE [13]
R1	SPI2_CS2 PADCONFIG103 000F 419Ch 0821 4007h	SPI2_CS2	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		ECAP1_IN_APWM_OUT	2	IO								
		MAIN_ERRORn	5	IO								
		EPWM1_A	6	IO								
		GPIO1_9	7	IO								
T1	SPI2_CS3 PADCONFIG106 000F 41A8h 0821 4007h	SPI2_CS3	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		AUDIO_EXT_REFCLK1	2	IO								
		MCAN4_RX	3	I								
		I2C4_SDA	5	IOD								
		GPIO1_12	7	IO								
P2	SPI2_D0 PADCONFIG101 000F 4194h 0821 4007h	SPI2_D0	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		UART1_CTSn	2	I								
		UART6_RXD	3	I								
		ECAP1_IN_APWM_OUT	5	IO								
		GPIO1_7	7	IO								
R3	SPI2_D1 PADCONFIG102 000F 4198h 0821 4007h	SPI2_D1	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		UART1_RTSn	2	O								
		UART6_TXD	3	O								
		ECAP2_IN_APWM_OUT	5	IO								
		GPIO1_8	7	IO								
A10	TCK MCU_PADCONFIG25 0408 4064h 0826 4000h	TCK	0	I	On / NA / Up	On / Off / Up	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
D10	TDI MCU_PADCONFIG27 0408 406Ch 0826 4000h	TDI	0	I	On / Off / Up	On / Off / Up	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
A11	TDO MCU_PADCONFIG28 0408 4070h 0802 4000h	TDO	0	OZ	Off / Off / Up	Off / SS / Up	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
C11	TMS MCU_PADCONFIG29 0408 4074h 0826 4000h	TMS	0	I	On / Off / Up	On / Off / Up	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
B10	TRSTn MCU_PADCONFIG26 0408 4068h 0824 4000h	TRSTn	0	I	On / NA / Down	On / Off / Down	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD

Table 5-1. Pin Attributes (ANJ Package) (continued)

BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/ DOWN TYPE [13]
N1	UART0_CTSn PADCONFIG116 000F 41D0h 0821 4007h	UART0_CTSn	0	I	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		SPI0_CS2	1	IO								
		I2C3_SCL	2	IOD								
		UART2_RXD	3	I								
		TIMER_IO6	4	IO								
		AUDIO_EXT_REFCLK0	5	IO								
		GPIO1_22	7	IO								
		MMC0_SDCD	9	I								
L3	UART0_RTSn PADCONFIG117 000F 41D4h 0821 4007h	UART0_RTSn	0	O	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		SPI0_CS3	1	IO								
		I2C3_SDA	2	IOD								
		UART2_TXD	3	O								
		TIMER_IO7	4	IO								
		AUDIO_EXT_REFCLK1	5	IO								
		GPIO1_23	7	IO								
		MMC0_SDWP	9	I								
L2	UART0_RXD PADCONFIG114 000F 41C8h 0821 4007h	UART0_RXD	0	I	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		ECAP1_IN_APWM_OUT	1	IO								
		SPI2_D0	2	IO								
		EPWM2_A	3	IO								
		GPIO1_20	7	IO								
L1	UART0_TXD PADCONFIG115 000F 41CCh 0821 4007h	UART0_TXD	0	O	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		ECAP2_IN_APWM_OUT	1	IO								
		SPI2_D1	2	IO								
		EPWM2_B	3	IO								
		GPIO1_21	7	IO								
W9	USB0_DM	USB0_DM	0	IO				1.8 V/3.3 V	VDDA_3P3_USB, VDDA_1P8_USB, VDDA_CORE_USB		USB2PHY	
V9	USB0_DP	USB0_DP	0	IO				1.8 V/3.3 V	VDDA_3P3_USB, VDDA_1P8_USB, VDDA_CORE_USB		USB2PHY	
W2	USB0_DRVVBUS PADCONFIG149 000F 4254h 0020 4007h	USB0_DRVVBUS	0	O	Off / Off / Down	Off / Off / Down	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		ECAP5_IN_APWM_OUT	3	IO								
		GPIO1_50	7	IO								
V8	USB0_RCALIB	USB0_RCALIB	0	IO				1.8 V/3.3 V	VDDA_3P3_USB, VDDA_1P8_USB, VDDA_CORE_USB		USB2PHY	

Table 5-1. Pin Attributes (ANJ Package) (continued)

BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/ DOWN TYPE [13]
U9	USB0_VBUS	USB0_VBUS	0	A				1.8 V/3.3 V	VDDA_3P3_USB, VDDA_1P8_USB, VDDA_CORE_USB		USB2PHY	
P10	VDDA_1P8_USB	VDDA_1P8_USB		PWR				1.8 V				
R9	VDDA_3P3_USB	VDDA_3P3_USB		PWR				3.3 V				
J5	VDDA_ADC0	VDDA_ADC0		PWR				1.8 V				
N10	VDDA_CORE_USB	VDDA_CORE_USB		PWR				0.75 V/0.85 V				
H7	VDDA_MCU	VDDA_MCU		PWR				1.8 V				
J9	VDDA_PLL0	VDDA_PLL0		PWR				1.8 V				
J10	VDDA_PLL1	VDDA_PLL1		PWR				1.8 V				
M11	VDDA_PLL2	VDDA_PLL2		PWR				1.8 V				
K5	VDDA_TEMP0	VDDA_TEMP0		PWR				1.8 V				
N11	VDDA_TEMP1	VDDA_TEMP1		PWR				1.8 V				
E7	VDDR_CANUART	VDDR_CANUART		PWR				0.75 V/0.85 V				
G10, H12, J8, K10, M10, M14, N12, N8	VDDR_CORE	VDDR_CORE		PWR				0.85 V				
K6, M6	VDDSHV0	VDDSHV0		PWR				1.8 V/3.3 V				
E13, F12	VDDSHV1	VDDSHV1		PWR				1.8 V/3.3 V				
P11, P12	VDDSHV2	VDDSHV2		PWR				1.8 V/3.3 V				
H14, J14, K14	VDDSHV3	VDDSHV3		PWR				1.8 V/3.3 V				
P9, R8	VDDSHV5	VDDSHV5		PWR				1.8 V/3.3 V				
F7	VDDSHV_CANUART	VDDSHV_CANUART		PWR				1.8 V/3.3 V				
F8, F9	VDDSHV_MCU	VDDSHV_MCU		PWR				1.8 V/3.3 V				
F5	VDDS_OSC0	VDDS_OSC0		PWR				1.8 V				
F6	VDD_CANUART	VDD_CANUART		PWR				0.75 V/0.85 V				
G11, G14, G7, H10, H13, H9, J12, K13, K7, K9, L11, L12, L8, M13, M7, M9, P13, P7	VDD_CORE	VDD_CORE		PWR				0.75 V/0.85 V				
J6	VMON_1P8_SOC	VMON_1P8_SOC		PWR				1.8 V				
H5	VMON_3P3_SOC	VMON_3P3_SOC		PWR				3.3 V				
H8	VMON_ER_VSYS	VMON_ER_VSYS		PWR								

Table 5-1. Pin Attributes (ANJ Package) (continued)

BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/ DOWN TYPE [13]
G5	VPP	VPP		PWR				1.8 V				
A1, A19, B2, C19, C3, D1, D11, D14, D19, D3, D4, D8, E10, E11, E12, E14, E15, E17, E18, E5, E9, F10, F11, F14, F15, F16, F4, G12, G13, G15, G4, G6, G8, G9, H11, H3, H6, J11, J13, J15, J7, K11, K12, K15, K8, L10, L13, L14, L15, L5, L7, L9, M12, M15, M5, M8, N13, N14, N15, N5, N6, N7, N9, P14, P15, P5, P6, R10, R12, R13, R14, R15, R5, R6, R7, T10, T16, T5, T8, T9, U10, U17, U4, U5, U8, V10, V18, V4, W1, W10, W19, W3, W6	VSS	VSS		GND				VSS				
B11	WKUP_CLKOUT0	WKUP_CLKOUT0	0	O	Off / Off / Off	Off / SS / Off	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
	MCU_PADCONFIG33 0408 4084h 0801 4000h	MCU_GPIO0_23	7	IO								
B9	WKUP_I2C0_SCL	WKUP_I2C0_SCL	0	IOD	Off / Off / Off	On / SS / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	I2C OPEN DRAIN	
	MCU_PADCONFIG19 0408 404Ch 0805 4007h	MCU_GPIO0_19	7	IOD								

Table 5-1. Pin Attributes (ANJ Package) (continued)

BALL NUMBER [1]	BALL NAME [2]/ IOMUX REGISTER [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	POWER [10]	HYS [11]	BUFFER TYPE [12]	PULL UP/ DOWN TYPE [13]
A8	WKUP_I2C0_SDA MCU_PADCONFIG20 0408 4050h 0805 4007h	WKUP_I2C0_SDA	0	IOD	Off / Off / Off	On / SS / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	I2C OPEN DRAIN	
		MCU_GPIO0_20	7	IOD								
E1	WKUP_LFOSC0_XI	WKUP_LFOSC0_XI	0	I				1.8 V	VDDS_OSC0		N16FFC_LFXOSC	
D2	WKUP_LFOSC0_XO	WKUP_LFOSC0_XO	0	O				1.8 V	VDDS_OSC0		N16FFC_LFXOSC	
B7	WKUP_TIMER_IO0 MCU_PADCONFIG0 0408 4000h 0821 4007h	WKUP_TIMER_IO0	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
		MCU_GPIO0_0	7	IO								
C7	WKUP_TIMER_IO1 MCU_PADCONFIG1 0408 4004h 0821 4007h	WKUP_TIMER_IO1	0	IO	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
		MCU_OBSCLK0	1	O								
		MCU_SYSCLKOUT0	2	O								
		MCU_EXT_REFCLK0	3	I								
		MCU_GPIO0_1	7	IO								
D6	WKUP_UART0_CTSn MCU_PADCONFIG11 0408 402Ch 0821 4007h	WKUP_UART0_CTSn	0	I	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_CANUART	Yes	LVCMOS	PU/PD
		WKUP_TIMER_IO0	1	IO								
		MCAN3_TX	2	O								
		UART4_RXD	3	I								
		MCU_GPIO0_11	7	IO								
C5	WKUP_UART0_RTSn MCU_PADCONFIG12 0408 4030h 0821 4007h	WKUP_UART0_RTSn	0	O	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_CANUART	Yes	LVCMOS	PU/PD
		WKUP_TIMER_IO1	1	IO								
		MCAN3_RX	2	I								
		UART4_TXD	3	O								
		MCU_GPIO0_12	7	IO								
B5	WKUP_UART0_RXD MCU_PADCONFIG9 0408 4024h 0821 4007h	WKUP_UART0_RXD	0	I	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_CANUART	Yes	LVCMOS	PU/PD
		MCAN2_TX	2	O								
		MCU_GPIO0_9	7	IO								
A5	WKUP_UART0_TXD MCU_PADCONFIG10 0408 4028h 0821 4007h	WKUP_UART0_TXD	0	O	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_CANUART	Yes	LVCMOS	PU/PD
		MCAN2_RX	2	I								
		MCU_GPIO0_10	7	IO								

5.3 Signal Descriptions

Many signals are available on multiple pins, according to the software configuration of the pin multiplexing options.

The following list describes the column headers:

1. **SIGNAL NAME:** The name of the signal passing through the pin.

Note

Signal names and descriptions provided in each Signal Descriptions table, represent the pin multiplexed signal function which is implemented at the pin and selected via IOMUX pad configuration registers. Some device subsystems provide secondary multiplexing of signal functions, which are not described in these tables. For more information on secondary multiplexed signal functions, see the respective peripheral chapter of the device TRM.

2. **SIGNAL TYPE:** Signal direction and type:
   - I = Input
   - O = Output
   - IO = Input, Output, or simultaneously Input and Output
   - ID = Input with open-drain output function
   - OD = Output, with open-drain output function
   - IOD = Input, Output, or simultaneously Input and Output, with open-drain output function
   - IOZ = Input, Output, or simultaneously Input and Output, with three-state output function
   - OZ = Output with three-state output function
   - A = Analog
   - CAP = LDO capacitor
   - PWR = Power
   - GND = Ground
3. **DESCRIPTION:** Description of the signal
4. **BALL:** Associated ball number

For more information on the I/O cell configurations, see the *Pad Configuration Registers* section within the *Device Configuration* chapter of the device TRM.

5.3.1 ADC

Table 5-2. ADC0 Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
ADC0_REFN	A	ADC Reference (Negative)	H2
ADC0_REFP	A	ADC Reference (Positive)	G1
ADC0_AIN0	A	ADC Analog Input 0	F1
ADC0_AIN1	A	ADC Analog Input 1	H1
ADC0_AIN2	A	ADC Analog Input 2	K2
ADC0_AIN3	A	ADC Analog Input 3	K1
ADC0_AIN4	A	ADC Analog Input 4	F2
ADC0_AIN5	A	ADC Analog Input 5	G2
ADC0_AIN6	A	ADC Analog Input 6	J1
ADC0_AIN7	A	ADC Analog Input 7	J2
ADC_EXT_TRIGGER0	I	ADC External Trigger	D15, N4, V2

5.3.2 Audio Clock References

Table 5-3. Audio Clock Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
AUDIO_EXT_REFCLK0	IO	Audio Clock Reference Input/Output 0	N1, T15, V1
AUDIO_EXT_REFCLK1	IO	Audio Clock Reference Input/Output 1	L3, M17, T1
AUDIO_EXT_REFCLK2	IO	Audio Clock Reference Input/Output 2	T19, V3
OSC1_XI	I	Audio Frequency (24.576 MHz) Oscillator Input	C1
OSC1_XO	O	Audio Frequency (24.576 MHz) Oscillator Output	C2

5.3.3 CPSW

Table 5-4. RGMII1 Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
RGMII1_RXC	I	RGMII Receive Clock	W12
RGMII1_RX_CTL	I	RGMII Receive Control	V12
RGMII1_TXC	O	RGMII Transmit Clock	V13
RGMII1_TX_CTL	O	RGMII Transmit Control	T13
RGMII1_RD0	I	RGMII Receive Data 0	W11
RGMII1_RD1	I	RGMII Receive Data 1	T11
RGMII1_RD2	I	RGMII Receive Data 2	T12
RGMII1_RD3	I	RGMII Receive Data 3	U12
RGMII1_TD0	O	RGMII Transmit Data 0	U13
RGMII1_TD1	O	RGMII Transmit Data 1	W13
RGMII1_TD2	O	RGMII Transmit Data 2	T14
RGMII1_TD3	O	RGMII Transmit Data 3	U14

Table 5-5. RGMII2 Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
RGMII2_RXC	I	RGMII Receive Clock	W15
RGMII2_RX_CTL	I	RGMII Receive Control	V14
RGMII2_TXC	O	RGMII Transmit Clock	W17
RGMII2_TX_CTL	O	RGMII Transmit Control	U16
RGMII2_RD0	I	RGMII Receive Data 0	U15
RGMII2_RD1	I	RGMII Receive Data 1	V15
RGMII2_RD2	I	RGMII Receive Data 2	W14
RGMII2_RD3	I	RGMII Receive Data 3	T15

Table 5-5. RGMII2 Signal Descriptions (continued)

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
RGMII2_TD0	O	RGMII Transmit Data 0	V16
RGMII2_TD1	O	RGMII Transmit Data 1	W16
RGMII2_TD2	O	RGMII Transmit Data 2	V17
RGMII2_TD3	O	RGMII Transmit Data 3	W18

Table 5-6. RMII1 Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
RMII1_CRS_DV	I	RMII Carrier Sense / Data Valid	V13
RMII1_REF_CLK	I	RMII Reference Clock	W12
RMII1_RX_ER	I	RMII Receive Data Error	V12
RMII1_TX_EN	O	RMII Transmit Enable	T13
RMII1_RXD0	I	RMII Receive Data 0	W11
RMII1_RXD1	I	RMII Receive Data 1	T11
RMII1_TXD0	O	RMII Transmit Data 0	U13
RMII1_TXD1	O	RMII Transmit Data 1	W13

Table 5-7. RMII2 Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
RMII2_CRS_DV	I	RMII Carrier Sense / Data Valid	W17
RMII2_REF_CLK	I	RMII Reference Clock	W15
RMII2_RX_ER	I	RMII Receive Data Error	V14
RMII2_TX_EN	O	RMII Transmit Enable	U16
RMII2_RXD0	I	RMII Receive Data 0	U15
RMII2_RXD1	I	RMII Receive Data 1	V15
RMII2_TXD0	O	RMII Transmit Data 0	V16
RMII2_TXD1	O	RMII Transmit Data 1	W16

Table 5-8. MDIO Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
MDIO0_MDC	O	MDIO Clock	V11
MDIO0_MDIO	IO	MDIO Data	U11

5.3.4 CPTS

Table 5-9. CPTS Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
CP_GEMAC_CPTS0_RFT_CLK	I	CPTS Reference Clock Input to CPSW0 CPTS	P1
CP_GEMAC_CPTS0_TS_COMP	O	CPTS Time Stamp Counter Compare Output from CPSW0 CPTS	J4, U1
CP_GEMAC_CPTS0_TS_SYNC	O	CPTS Time Stamp Counter Bit Output from CPSW0 CPTS	M1, T4
CP_GEMAC_CPTS0_HW1TSPUSH	I	CPTS Hardware Time Stamp Push Input to CPSW0 CPTS	K3, U2
CP_GEMAC_CPTS0_HW2TSPUSH	I	CPTS Hardware Time Stamp Push Input to CPSW0 CPTS	K4, T3
SYNC0_OUT	O	CPTS Time Stamp Generator Bit 0 Output from Time Sync Router	M3
SYNC1_OUT	O	CPTS Time Stamp Generator Bit 1 Output from Time Sync Router	P1
SYNC2_OUT	O	CPTS Time Stamp Generator Bit 2 Output from Time Sync Router	L4
SYNC3_OUT	O	CPTS Time Stamp Generator Bit 3 Output from Time Sync Router	M4

5.3.5 ECAP

Table 5-10. ECAP0 Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
ECAP0_IN_APWM_OUT	IO	Enhanced Capture (ECAP) Input or ECAP Auxiliary PWM (APWM) Output	J4, P1

Table 5-11. ECAP1 Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
ECAP1_IN_APWM_OUT	IO	Enhanced Capture (ECAP) Input or ECAP Auxiliary PWM (APWM) Output	L2, M3, P2, R1, U2

Table 5-12. ECAP2 Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
ECAP2_IN_APWM_OUT	IO	Enhanced Capture (ECAP) Input or ECAP Auxiliary PWM (APWM) Output	L1, N3, R3, R4, T3

Table 5-13. ECAP3 Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
ECAP3_IN_APWM_OUT	IO	Enhanced Capture (ECAP) Input or ECAP Auxiliary PWM (APWM) Output	M2, P4, U3

Table 5-14. ECAP4 Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
ECAP4_IN_APWM_OUT	IO	Enhanced Capture (ECAP) Input or ECAP Auxiliary PWM (APWM) Output	N2, U1, V3

Table 5-15. ECAP5 Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
ECAP5_IN_APWM_OUT	IO	Enhanced Capture (ECAP) Input or ECAP Auxiliary PWM (APWM) Output	T4, U18, W2

5.3.6 Emulation and Debug

Table 5-16. JTAG Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
EMU0	IO	Emulation Control 0	C9
EMU1	IO	Emulation Control 1	C10
TCK	I	JTAG Test Clock Input	A10
TDI	I	JTAG Test Data Input	D10
TDO	OZ	JTAG Test Data Output	A11
TMS	I	JTAG Test Mode Select Input	C11
TRSTn	I	JTAG Reset	B10

Table 5-17. TRACE Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
TRC_CLK	O	Trace Clock	N19
TRC_CTL	O	Trace Control	M19
TRC_DATA0	O	Trace Data 0	N17
TRC_DATA1	O	Trace Data 1	M16
TRC_DATA2	O	Trace Data 2	N18
TRC_DATA3	O	Trace Data 3	M18
TRC_DATA4	O	Trace Data 4	N16
TRC_DATA5	O	Trace Data 5	P17

Table 5-17. TRACE Signal Descriptions (continued)

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
TRC_DATA6	O	Trace Data 6	T18
TRC_DATA7	O	Trace Data 7	T19
TRC_DATA8	O	Trace Data 8	H19
TRC_DATA9	O	Trace Data 9	J17
TRC_DATA10	O	Trace Data 10	J18
TRC_DATA11	O	Trace Data 11	J19
TRC_DATA12	O	Trace Data 12	J16
TRC_DATA13	O	Trace Data 13	L19
TRC_DATA14	O	Trace Data 14	K19
TRC_DATA15	O	Trace Data 15	L17
TRC_DATA16	O	Trace Data 16	K16
TRC_DATA17	O	Trace Data 17	L18
TRC_DATA18	O	Trace Data 18	K18
TRC_DATA19	O	Trace Data 19	T17
TRC_DATA20	O	Trace Data 20	R16
TRC_DATA21	O	Trace Data 21	R19
TRC_DATA22	O	Trace Data 22	R18
TRC_DATA23	O	Trace Data 23	R17

5.3.7 EPWM

Table 5-18. EPWM Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
EPWM_SOCA	O	EPWM Start of Conversation A	M3
EPWM_SOCB	O	EPWM Start of Conversation B	N3
EPWM_TZn_IN0	I	EPWM Trip Zone Input 0 (active low)	K4
EPWM_TZn_IN1	I	EPWM Trip Zone Input 1 (active low)	W4
EPWM_TZn_IN2	I	EPWM Trip Zone Input 2 (active low)	T7
EPWM_TZn_IN3	I	EPWM Trip Zone Input 3 (active low)	L4
EPWM_TZn_IN4	I	EPWM Trip Zone Input 4 (active low)	M4
EPWM_TZn_IN5	I	EPWM Trip Zone Input 5 (active low)	J4

Table 5-19. EPWM0 Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
EPWM0_A	IO	EPWM Output A	J3, T2, U7, V16
EPWM0_B	IO	EPWM Output B	J4, R2, U6, W16
EPWM0_SYNCI	I	EPWM Sync Input	N2, W7
EPWM0_SYNCO	O	EPWM Sync Output	M2, V7

Table 5-20. EPWM1 Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
EPWM1_A	IO	EPWM Output A	M1, R1, V17, V6
EPWM1_B	IO	EPWM Output B	K3, V1, W18, W5

Table 5-21. EPWM2 Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
EPWM2_A	IO	EPWM Output A	L2, V14, V5
EPWM2_B	IO	EPWM Output B	L1, T6, W15

5.3.8 GPIO

Table 5-22. GPIO0 Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
GPIO0_0	IO	General Purpose Input/Output	B17
GPIO0_1	IO	General Purpose Input/Output	A18
GPIO0_2	IO	General Purpose Input/Output	B19
GPIO0_3	IO	General Purpose Input/Output	B16
GPIO0_4	IO	General Purpose Input/Output	D17
GPIO0_5	IO	General Purpose Input/Output	C17
GPIO0_6	IO	General Purpose Input/Output	D16
GPIO0_7	IO	General Purpose Input/Output	E16
GPIO0_8	IO	General Purpose Input/Output	B18
GPIO0_9	IO	General Purpose Input/Output	D18
GPIO0_10	IO	General Purpose Input/Output	C18
GPIO0_11	IO	General Purpose Input/Output	A17
GPIO0_12	IO	General Purpose Input/Output	C16
GPIO0_13	IO	General Purpose Input/Output	D15
GPIO0_14	IO	General Purpose Input/Output	A16
GPIO0_15	IO	General Purpose Input/Output	N19
GPIO0_16	IO	General Purpose Input/Output	M19
GPIO0_17	IO	General Purpose Input/Output	N17
GPIO0_18	IO	General Purpose Input/Output	M16
GPIO0_19	IO	General Purpose Input/Output	N18
GPIO0_20	IO	General Purpose Input/Output	M18
GPIO0_21	IO	General Purpose Input/Output	N16
GPIO0_22	IO	General Purpose Input/Output	P17
GPIO0_23	IO	General Purpose Input/Output	P18
GPIO0_24	IO	General Purpose Input/Output	P19
GPIO0_25	IO	General Purpose Input/Output	P16
GPIO0_26	IO	General Purpose Input/Output	R17
GPIO0_27	IO	General Purpose Input/Output	R18
GPIO0_28	IO	General Purpose Input/Output	R19
GPIO0_29	IO	General Purpose Input/Output	R16
GPIO0_30	IO	General Purpose Input/Output	T17
GPIO0_31	IO	General Purpose Input/Output	T18
GPIO0_32	IO	General Purpose Input/Output	T19
GPIO0_33	IO	General Purpose Input/Output	H19
GPIO0_34	IO	General Purpose Input/Output	J17
GPIO0_35	IO	General Purpose Input/Output	J18
GPIO0_36	IO	General Purpose Input/Output	J19
GPIO0_37	IO	General Purpose Input/Output	J16
GPIO0_38	IO	General Purpose Input/Output	K17
GPIO0_39	IO	General Purpose Input/Output	L19
GPIO0_40	IO	General Purpose Input/Output	K19
GPIO0_41	IO	General Purpose Input/Output	L17
GPIO0_42	IO	General Purpose Input/Output	K16
GPIO0_43	IO	General Purpose Input/Output	L18
GPIO0_44	IO	General Purpose Input/Output	K18
GPIO0_45	IO	General Purpose Input/Output	L16
GPIO0_46	IO	General Purpose Input/Output	M17
GPIO0_47	IO	General Purpose Input/Output	E19

Table 5-22. GPIO0 Signal Descriptions (continued)

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
GPIO0_48	IO	General Purpose Input/Output	G19
GPIO0_49	IO	General Purpose Input/Output	G18
GPIO0_50	IO	General Purpose Input/Output	H16
GPIO0_51	IO	General Purpose Input/Output	H18
GPIO0_52	IO	General Purpose Input/Output	H17
GPIO0_55	IO	General Purpose Input/Output	F18
GPIO0_56	IO	General Purpose Input/Output	F17
GPIO0_57	IO	General Purpose Input/Output	F19
GPIO0_58	IO	General Purpose Input/Output	G17
GPIO0_59	IO	General Purpose Input/Output	G16
GPIO0_62	IO	General Purpose Input/Output	U18
GPIO0_63	IO	General Purpose Input/Output	U19
GPIO0_64	IO	General Purpose Input/Output	V19
GPIO0_65	IO	General Purpose Input/Output	A14
GPIO0_66	IO	General Purpose Input/Output	B13
GPIO0_67	IO	General Purpose Input/Output	B15
GPIO0_68	IO	General Purpose Input/Output	A13
GPIO0_69	IO	General Purpose Input/Output	D12
GPIO0_70	IO	General Purpose Input/Output	D13
GPIO0_71	IO	General Purpose Input/Output	C13
GPIO0_72	IO	General Purpose Input/Output	B12
GPIO0_73	IO	General Purpose Input/Output	T13
GPIO0_74	IO	General Purpose Input/Output	V13
GPIO0_75	IO	General Purpose Input/Output	U13
GPIO0_76	IO	General Purpose Input/Output	W13
GPIO0_77	IO	General Purpose Input/Output	T14
GPIO0_78	IO	General Purpose Input/Output	U14
GPIO0_79	IO	General Purpose Input/Output	V12
GPIO0_80	IO	General Purpose Input/Output	W12
GPIO0_81	IO	General Purpose Input/Output	W11
GPIO0_82	IO	General Purpose Input/Output	T11
GPIO0_83	IO	General Purpose Input/Output	T12
GPIO0_84	IO	General Purpose Input/Output	U12
GPIO0_85	IO	General Purpose Input/Output	U11
GPIO0_86	IO	General Purpose Input/Output	V11
GPIO0_87	IO	General Purpose Input/Output	U16
GPIO0_88	IO	General Purpose Input/Output	W17
GPIO0_89	IO	General Purpose Input/Output	V16
GPIO0_90	IO	General Purpose Input/Output	W16
GPIO0_91	IO	General Purpose Input/Output	V17
GPIO0_92	IO	General Purpose Input/Output	C12

Table 5-23. GPIO1 Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
GPIO1_0	IO	General Purpose Input/Output	W18
GPIO1_1	IO	General Purpose Input/Output	V14
GPIO1_2	IO	General Purpose Input/Output	W15
GPIO1_3	IO	General Purpose Input/Output	U15
GPIO1_4	IO	General Purpose Input/Output	V15

Table 5-23. GPIO1 Signal Descriptions (continued)

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
GPIO1_5	IO	General Purpose Input/Output	W14
GPIO1_6	IO	General Purpose Input/Output	T15
GPIO1_7	IO	General Purpose Input/Output	P2
GPIO1_8	IO	General Purpose Input/Output	R3
GPIO1_9	IO	General Purpose Input/Output	R1
GPIO1_10	IO	General Purpose Input/Output	V1
GPIO1_11	IO	General Purpose Input/Output	R4
GPIO1_12	IO	General Purpose Input/Output	T1
GPIO1_13	IO	General Purpose Input/Output	T2
GPIO1_14	IO	General Purpose Input/Output	R2
GPIO1_15	IO	General Purpose Input/Output	J3
GPIO1_16	IO	General Purpose Input/Output	J4
GPIO1_17	IO	General Purpose Input/Output	M1
GPIO1_18	IO	General Purpose Input/Output	K3
GPIO1_19	IO	General Purpose Input/Output	K4
GPIO1_112	IO	General Purpose Input/Output	N19
GPIO1_113	IO	General Purpose Input/Output	M19
GPIO1_114	IO	General Purpose Input/Output	N17
GPIO1_115	IO	General Purpose Input/Output	M16
GPIO1_116	IO	General Purpose Input/Output	N18
GPIO1_117	IO	General Purpose Input/Output	M18
GPIO1_118	IO	General Purpose Input/Output	N16
GPIO1_119	IO	General Purpose Input/Output	P17
GPIO1_120	IO	General Purpose Input/Output	P18
GPIO1_121	IO	General Purpose Input/Output	P19
GPIO1_122	IO	General Purpose Input/Output	P16
GPIO1_123	IO	General Purpose Input/Output	R18
GPIO1_124	IO	General Purpose Input/Output	R19
GPIO1_125	IO	General Purpose Input/Output	R16
GPIO1_126	IO	General Purpose Input/Output	T17
GPIO1_127	IO	General Purpose Input/Output	T18
GPIO1_20	IO	General Purpose Input/Output	L2
GPIO1_21	IO	General Purpose Input/Output	L1
GPIO1_22	IO	General Purpose Input/Output	N1
GPIO1_23	IO	General Purpose Input/Output	L3
GPIO1_24	IO	General Purpose Input/Output	L4
GPIO1_25	IO	General Purpose Input/Output	M4
GPIO1_26	IO	General Purpose Input/Output	M3
GPIO1_27	IO	General Purpose Input/Output	N3
GPIO1_28	IO	General Purpose Input/Output	N2
GPIO1_29	IO	General Purpose Input/Output	M2
GPIO1_30	IO	General Purpose Input/Output	P1
GPIO1_31	IOD	General Purpose Input/Output	P3
GPIO1_32	IO	General Purpose Input/Output	W7
GPIO1_33	IO	General Purpose Input/Output	V7
GPIO1_34	IO	General Purpose Input/Output	T7
GPIO1_35	IO	General Purpose Input/Output	U7
GPIO1_36	IO	General Purpose Input/Output	U6
GPIO1_37	IO	General Purpose Input/Output	V6
GPIO1_38	IO	General Purpose Input/Output	W5

Table 5-23. GPIO1 Signal Descriptions (continued)

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
GPIO1_39	IO	General Purpose Input/Output	W4
GPIO1_40	IO	General Purpose Input/Output	V5
GPIO1_41	IO	General Purpose Input/Output	T6
GPIO1_42	IO	General Purpose Input/Output	U1
GPIO1_43	IO	General Purpose Input/Output	T4
GPIO1_44	IO	General Purpose Input/Output	U2
GPIO1_45	IO	General Purpose Input/Output	T3
GPIO1_46	IO	General Purpose Input/Output	U3
GPIO1_47	IO	General Purpose Input/Output	N4
GPIO1_48	IO	General Purpose Input/Output	P4
GPIO1_49	IO	General Purpose Input/Output	V2
GPIO1_50	IO	General Purpose Input/Output	W2
GPIO1_72	IO	General Purpose Input/Output	V3
GPIO1_74	I	General Purpose Input/Output	F1
GPIO1_75	I	General Purpose Input/Output	H1
GPIO1_76	I	General Purpose Input/Output	K2
GPIO1_77	I	General Purpose Input/Output	K1
GPIO1_78	I	General Purpose Input/Output	F2
GPIO1_79	I	General Purpose Input/Output	G2
GPIO1_80	I	General Purpose Input/Output	J1
GPIO1_81	I	General Purpose Input/Output	J2
GPIO1_82	IO	General Purpose Input/Output	A15
GPIO1_83	IO	General Purpose Input/Output	C15
GPIO1_84	IO	General Purpose Input/Output	B14
GPIO1_85	IO	General Purpose Input/Output	C14

Table 5-24. MCU GPIO Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
MCU_GPIO0_0	IO	General Purpose Input/Output	B7
MCU_GPIO0_1	IO	General Purpose Input/Output	C7
MCU_GPIO0_2	IO	General Purpose Input/Output	C8
MCU_GPIO0_3	IO	General Purpose Input/Output	B8
MCU_GPIO0_4	IO	General Purpose Input/Output	A9
MCU_GPIO0_5	IO	General Purpose Input/Output	C4
MCU_GPIO0_6	IO	General Purpose Input/Output	B4
MCU_GPIO0_7	IO	General Purpose Input/Output	A4
MCU_GPIO0_8	IO	General Purpose Input/Output	D5
MCU_GPIO0_9	IO	General Purpose Input/Output	B5
MCU_GPIO0_10	IO	General Purpose Input/Output	A5
MCU_GPIO0_11	IO	General Purpose Input/Output	D6
MCU_GPIO0_12	IO	General Purpose Input/Output	C5
MCU_GPIO0_13	IO	General Purpose Input/Output	C6
MCU_GPIO0_14	IO	General Purpose Input/Output	B6
MCU_GPIO0_15	IO	General Purpose Input/Output	A6
MCU_GPIO0_16	IO	General Purpose Input/Output	D7
MCU_GPIO0_19	IOD	General Purpose Input/Output	B9
MCU_GPIO0_112	IO	General Purpose Input/Output	C9
MCU_GPIO0_113	IO	General Purpose Input/Output	C10
MCU_GPIO0_20	IOD	General Purpose Input/Output	A8

Table 5-24. MCU GPIO Signal Descriptions (continued)

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
MCU_GPIO0_22	IO	General Purpose Input/Output	A7
MCU_GPIO0_23	IO	General Purpose Input/Output	B11
MCU_GPIO0_24	IO	General Purpose Input/Output	C9
MCU_GPIO0_25	IO	General Purpose Input/Output	C10

5.3.9 HYPERBUS

Table 5-25. HYPERBUS Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
HYPERBUS0_CK	O	HYPERBUS Differential Clock	A14
HYPERBUS0_CKn	O	HYPERBUS Differential Clock	B13
HYPERBUS0_INTn	I	HYPERBUS Interrupt (active low)	A16, B19
HYPERBUS0_RESETn	O	HYPERBUS Controller Reset Output (active low)	A16, C12
HYPERBUS0_RESETOn	I	HYPERBUS Peripheral Reset Input (active low)	A18, D15
HYPERBUS0_RWDS	IO	HYPERBUS Read Write Data Strobe	B15
HYPERBUS0_WPn	O	HYPERBUS Write Protect (active low)	A16, D15
HYPERBUS0_CSn0	O	HYPERBUS Chip Select 0 (active low)	B12
HYPERBUS0_CSn1	O	HYPERBUS Chip Select 1 (active low)	C12
HYPERBUS0_DQ0	IO	HYPERBUS Data Bit 0	A13
HYPERBUS0_DQ1	IO	HYPERBUS Data Bit 1	D12
HYPERBUS0_DQ2	IO	HYPERBUS Data Bit 2	D13
HYPERBUS0_DQ3	IO	HYPERBUS Data Bit 3	C13
HYPERBUS0_DQ4	IO	HYPERBUS Data Bit 4	A15
HYPERBUS0_DQ5	IO	HYPERBUS Data Bit 5	C15
HYPERBUS0_DQ6	IO	HYPERBUS Data Bit 6	B14
HYPERBUS0_DQ7	IO	HYPERBUS Data Bit 7	C14

5.3.10 I2C

Table 5-26. I2C0 Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
I2C0_SCL	IOD	I2C Clock	M3
I2C0_SDA	IOD	I2C Data	N3

Table 5-27. I2C1 Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
I2C1_SCL	IOD	I2C Clock	N2
I2C1_SDA	IOD	I2C Data	M2

Table 5-28. I2C2 Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
I2C2_SCL	IOD	I2C Clock	A15, L18, U16
I2C2_SDA	IOD	I2C Data	C15, K18, W17

Table 5-29. I2C3 Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
I2C3_SCL	IOD	I2C Clock	N1, U15, V5
I2C3_SDA	IOD	I2C Data	L3, T6, V15

Table 5-30. I2C4 Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
I2C4_SCL	IOD	I2C Clock	P4, R4
I2C4_SDA	IOD	I2C Data	T1, V2

Table 5-31. I2C5 Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
I2C5_SCL	IOD	I2C Clock	L4, U19, U2
I2C5_SDA	IOD	I2C Data	M4, T3, V19

Table 5-32. I2C6 Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
I2C6_SCL	IOD	I2C Clock	G17, T7
I2C6_SDA	IOD	I2C Data	G16, U7

Table 5-33. WKUP I2C Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
WKUP_I2C0_SCL	IOD	I2C Clock	B9
WKUP_I2C0_SDA	IOD	I2C Data	A8

5.3.11 MCAN

Table 5-34. MCAN0 Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
MCAN0_RX	I	MCAN Receive Data	B4, M4, T6
MCAN0_TX	O	MCAN Transmit Data	C4, L4, V5

Table 5-35. MCAN1 Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
MCAN1_RX	I	MCAN Receive Data	D5, K18, V7
MCAN1_TX	O	MCAN Transmit Data	A4, L18, W7

Table 5-36. MCAN2 Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
MCAN2_RX	I	MCAN Receive Data	A5, U7
MCAN2_TX	O	MCAN Transmit Data	B5, T7

Table 5-37. MCAN3 Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
MCAN3_RX	I	MCAN Receive Data	C5, V3, V6
MCAN3_TX	O	MCAN Transmit Data	D6, N4, U6

Table 5-38. MCAN4 Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
MCAN4_RX	I	MCAN Receive Data	B6, T1, W4
MCAN4_TX	O	MCAN Transmit Data	C6, R4, W5

5.3.12 MCASP

Table 5-39. McASP0 Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
MCASP0_ACLKR	IO	McASP Receive Bit Clock	R16

Table 5-39. McASP0 Signal Descriptions (continued)

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
MCASP0_ACLKX	IO	McASP Transmit Bit Clock	N19
MCASP0_AFSR	IO	McASP Receive Frame Sync	T17
MCASP0_AFSX	IO	McASP Transmit Frame Sync	M19
MCASP0_AXR0	IO	McASP Audio Transmit/Receive 0	N17
MCASP0_AXR1	IO	McASP Audio Transmit/Receive 1	M16
MCASP0_AXR2	IO	McASP Audio Transmit/Receive 2	N18
MCASP0_AXR3	IO	McASP Audio Transmit/Receive 3	M18
MCASP0_AXR4	IO	McASP Audio Transmit/Receive 4	N16
MCASP0_AXR5	IO	McASP Audio Transmit/Receive 5	P17
MCASP0_AXR6	IO	McASP Audio Transmit/Receive 6	P18
MCASP0_AXR7	IO	McASP Audio Transmit/Receive 7	P19
MCASP0_AXR8	IO	McASP Audio Transmit/Receive 8	P16
MCASP0_AXR9	IO	McASP Audio Transmit/Receive 9	R17
MCASP0_AXR10	IO	McASP Audio Transmit/Receive 10	R18
MCASP0_AXR11	IO	McASP Audio Transmit/Receive 11	R19
MCASP0_AXR12	IO	McASP Audio Transmit/Receive 12	R16
MCASP0_AXR13	IO	McASP Audio Transmit/Receive 13	T17
MCASP0_AXR14	IO	McASP Audio Transmit/Receive 14	T18
MCASP0_AXR15	IO	McASP Audio Transmit/Receive 15	T19

Table 5-40. McASP1 Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
MCASP1_ACLKR	IO	McASP Receive Bit Clock	T18
MCASP1_ACLKX	IO	McASP Transmit Bit Clock	H19
MCASP1_AFSR	IO	McASP Receive Frame Sync	T19
MCASP1_AFSX	IO	McASP Transmit Frame Sync	J17
MCASP1_AXR0	IO	McASP Audio Transmit/Receive 0	J18
MCASP1_AXR1	IO	McASP Audio Transmit/Receive 1	J19
MCASP1_AXR2	IO	McASP Audio Transmit/Receive 2	J16
MCASP1_AXR3	IO	McASP Audio Transmit/Receive 3	K17
MCASP1_AXR4	IO	McASP Audio Transmit/Receive 4	T19
MCASP1_AXR5	IO	McASP Audio Transmit/Receive 5	T18
MCASP1_AXR6	IO	McASP Audio Transmit/Receive 6	T17
MCASP1_AXR7	IO	McASP Audio Transmit/Receive 7	R16
MCASP1_AXR8	IO	McASP Audio Transmit/Receive 8	R19
MCASP1_AXR9	IO	McASP Audio Transmit/Receive 9	R18
MCASP1_AXR10	IO	McASP Audio Transmit/Receive 10	G16

Table 5-41. McASP2 Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
MCASP2_ACLKR	IO	McASP Receive Bit Clock	G17
MCASP2_ACLKX	IO	McASP Transmit Bit Clock	L19
MCASP2_AFSR	IO	McASP Receive Frame Sync	G16
MCASP2_AFSX	IO	McASP Transmit Frame Sync	K19
MCASP2_AXR0	IO	McASP Audio Transmit/Receive 0	L17
MCASP2_AXR1	IO	McASP Audio Transmit/Receive 1	K16
MCASP2_AXR2	IO	McASP Audio Transmit/Receive 2	L18
MCASP2_AXR3	IO	McASP Audio Transmit/Receive 3	K18
MCASP2_AXR4	IO	McASP Audio Transmit/Receive 4	L16

Table 5-41. McASP2 Signal Descriptions (continued)

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
MCASP2_AXR5	IO	McASP Audio Transmit/Receive 5	M17

Table 5-42. McASP3 Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
MCASP3_ACLKR	IO	McASP Receive Bit Clock	F18
MCASP3_ACLKX	IO	McASP Transmit Bit Clock	E19
MCASP3_AFSR	IO	McASP Receive Frame Sync	F17
MCASP3_AFSX	IO	McASP Transmit Frame Sync	G19
MCASP3_AXR0	IO	McASP Audio Transmit/Receive 0	G18
MCASP3_AXR1	IO	McASP Audio Transmit/Receive 1	H16
MCASP3_AXR2	IO	McASP Audio Transmit/Receive 2	H18
MCASP3_AXR3	IO	McASP Audio Transmit/Receive 3	H17
MCASP3_AXR4	IO	McASP Audio Transmit/Receive 4	T18
MCASP3_AXR5	IO	McASP Audio Transmit/Receive 5	T19

Table 5-43. McASP4 Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
MCASP4_ACLKR	IO	McASP Receive Bit Clock	R18
MCASP4_ACLKX	IO	McASP Transmit Bit Clock	F18
MCASP4_AFSR	IO	McASP Receive Frame Sync	R19
MCASP4_AFSX	IO	McASP Transmit Frame Sync	F17
MCASP4_AXR0	IO	McASP Audio Transmit/Receive 0	F19
MCASP4_AXR1	IO	McASP Audio Transmit/Receive 1	G17
MCASP4_AXR2	IO	McASP Audio Transmit/Receive 2	G16
MCASP4_AXR3	IO	McASP Audio Transmit/Receive 3	U18
MCASP4_AXR4	IO	McASP Audio Transmit/Receive 4	U19
MCASP4_AXR5	IO	McASP Audio Transmit/Receive 5	V19

5.3.13 MLB

Table 5-44. MLB Signal Desriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
MLB0_MLBCLK	I	Media Local Bus Clock	U19
MLB0_MLBDAT	IO	Media Local Bus Data	V19
MLB0_MLBSIG	IO	Media Local Bus Signal	U18

5.3.14 MMC

Table 5-45. MMC Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
MMC0_CLK	IO	MMC/SD/SDIO Clock	V5
MMC0_CMD	IO	MMC/SD/SDIO Command	T6
MMC0_SDCD	I	SD Card Detect	N1, N2
MMC0_SDWP	I	SD Write Protect	L3, M2
MMC0_DAT0	IO	MMC/SD/SDIO Data	W4
MMC0_DAT1	IO	MMC/SD/SDIO Data	W5
MMC0_DAT2	IO	MMC/SD/SDIO Data	V6
MMC0_DAT3	IO	MMC/SD/SDIO Data	U6
MMC0_DAT4	IO	MMC/SD/SDIO Data	U7
MMC0_DAT5	IO	MMC/SD/SDIO Data	T7
MMC0_DAT6	IO	MMC/SD/SDIO Data	V7

Table 5-45. MMC Signal Descriptions (continued)

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
MMC0_DAT7	IO	MMC/SD/SDIO Data	W7

5.3.15 OSPI

Table 5-46. OSPI0 Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
OSPI0_CLK	O	OSPI Clock	B17
OSPI0_DQS	I	OSPI Data Strobe (DQS) or Loopback Clock Input	B19
OSPI0_ECC_FAIL	I	OSPI ECC Status	A16
OSPI0_LBCLKO	IO	OSPI Loopback Clock Output	A18
OSPI0_CSn0	O	OSPI Chip Select 0	A17
OSPI0_CSn1	O	OSPI Chip Select 1	C16
OSPI0_CSn2	O	OSPI Chip Select 2	D15
OSPI0_CSn3	O	OSPI Chip Select 3	A16
OSPI0_D0	IO	OSPI Data 0	B16
OSPI0_D1	IO	OSPI Data 1	D17
OSPI0_D2	IO	OSPI Data 2	C17
OSPI0_D3	IO	OSPI Data 3	D16
OSPI0_D4	IO	OSPI Data 4	E16
OSPI0_D5	IO	OSPI Data 5	B18
OSPI0_D6	IO	OSPI Data 6	D18
OSPI0_D7	IO	OSPI Data 7	C18
OSPI0_RESET_OUT0	O	OSPI Reset	A16
OSPI0_RESET_OUT1	O	OSPI Reset	D15

Table 5-47. OSPI1 Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
OSPI1_CLK	O	OSPI Clock	A14
OSPI1_DQS	I	OSPI Data Strobe (DQS) or Loopback Clock Input	B15
OSPI1_ECC_FAIL	I	OSPI ECC Status	C12
OSPI1_LBCLKO	IO	OSPI Loopback Clock Output	B13
OSPI1_CSn0	O	OSPI Chip Select 0	B12
OSPI1_CSn1	O	OSPI Chip Select 1	C12
OSPI1_D0	IO	OSPI Data 0	A13
OSPI1_D1	IO	OSPI Data 1	D12
OSPI1_D2	IO	OSPI Data 2	D13
OSPI1_D3	IO	OSPI Data 3	C13
OSPI1_D4	IO	OSPI Data 4	A15
OSPI1_D5	IO	OSPI Data 5	C15
OSPI1_D6	IO	OSPI Data 6	B14
OSPI1_D7	IO	OSPI Data 7	C14
OSPI1_RESET_OUT0	O	OSPI Reset	D15
OSPI1_RESET_OUT1	O	OSPI Reset	A16

5.3.16 Power Supply

Table 5-48. Power Supply Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
CAP_VDDS0	PWR	External capacitor connection for IO group 0	L6
CAP_VDDS1	PWR	External capacitor connection for IO group 1	F13
CAP_VDDS2	PWR	External capacitor connections for IO group 2	R11

Table 5-48. Power Supply Signal Descriptions (continued)

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
CAP_VDDS3	PWR	External capacitor connections for IO group 3	H15
CAP_VDDS5	PWR	External capacitor connections for IO group 5	P8
CAP_VDDS_CANUART	PWR	External capacitor connection for IO group CANUART	E6
CAP_VDDS_MCU	PWR	External capacitor connection for IO group MCU	E8
VDDA_1P8_USB	PWR	USB 1.8V analog supply	P10
VDDA_3P3_USB	PWR	USB 3.3V analog supply	R9
VDDA_ADC0	PWR	Analog supply for ADC	J5
VDDA_CORE_USB	PWR	USB core analog supply	N10
VDDA_MCU	PWR	MCU Analog supply	H7
VDDA_PLL0	PWR	Analog supply for PLL0	J9
VDDA_PLL1	PWR	Analog supply for PLL1	J10
VDDA_PLL2	PWR	Analog supply for PLL2	M11
VDDA_TEMP0	PWR	TEMP0 analog supply	K5
VDDA_TEMP1	PWR	TEMP1 analog supply	N11
VDDR_CANUART	PWR	Core RAM supply for CANUART Domain	E7
VDDR_CORE	PWR	Core RAM supply	G10, H12, J8, K10, M10, M14, N12, N8
VDDSHV0	PWR	IO supply for IO group 0	K6, M6
VDDSHV1	PWR	IO supply for IO group 1	E13, F12
VDDSHV2	PWR	IO supply for IO group 2	P11, P12
VDDSHV3	PWR	IO supply for IO group 3	H14, J14, K14
VDDSHV5	PWR	IO supply for IO group 5	P9, R8
VDDSHV_CANUART	PWR	IO supply for IO group CANUART	F7
VDDSHV_MCU	PWR	IO supply for IO group MCU	F8, F9
VDDS_OSC0	PWR	Oscillator supply	F5
VDD_CANUART	PWR	Core supply for CANUART Domain	F6
VDD_CORE	PWR	Core supply	G11, G14, G7, H10, H13, H9, J12, K13, K7, K9, L11, L12, L8, M13, M7, M9, P13, P7
VMON_1P8_SOC	PWR	Voltage monitor input for 1.8V SoC power supply	J6
VMON_3P3_SOC	PWR	Voltage monitor input for 3.3V SoC power supply	H5
VMON_ER_VSYS	PWR	Voltage monitor input, fixed 0.45 V (+/-3%) threshold. Use with external precision voltage divider to monitor a higher voltage rail such as the PMIC input supply.	H8
VPP	PWR	VPP supply	G5
VSS	GND	Ground	A1, A19, B2, C19, C3, D1, D11, D14, D19, D3, D4, D8, E10, E11, E12, E14, E15, E17, E18, E5, E9, F10, F11, F14, F15, F16, F4, G12, G13, G15, G4, G6, G8, G9, H11, H3, H6, J11, J13, J15, J7, K11, K12, K15, K8, L10, L13, L14, L15, L5, L7, L9, M12, M15, M5, M8, N13, N14, N15, N5, N6, N7, N9, P14, P15, P5, P6, R10, R12, R13, R14, R15, R5, R6, R7, T10, T16, T5, T8, T9, U10, U17, U4, U5, U8, V10, V18, V4, W1, W10, W19, W3, W6

5.3.17 Reserved and No Connect

Table 5-49. Reserved Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
RSVD_A3	RSVD	Reserved, must be left unconnected	A3
RSVD_A12	RSVD	Reserved, must be left unconnected	A12
RSVD_B3	RSVD	Reserved, must be left unconnected	B3
RSVD_E2	RSVD	Reserved, must be left unconnected	E2
RSVD_E4	RSVD	Reserved, must be left unconnected	E4
RSVD_G3	RSVD	Reserved, must be left unconnected	G3
RSVD_W8	RSVD	Reserved, must be left unconnected	W8

5.3.18 System and Miscellaneous

Table 5-50. Sysboot Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
BOOTMODE00	IO	Bootmode Pin 0	N19
BOOTMODE01	IO	Bootmode Pin 1	M19
BOOTMODE02	IO	Bootmode Pin 2	N17
BOOTMODE03	IO	Bootmode Pin 3	M16
BOOTMODE04	IO	Bootmode Pin 4	N18
BOOTMODE05	IO	Bootmode Pin 5	M18
BOOTMODE06	IO	Bootmode Pin 6	N16
BOOTMODE07	IO	Bootmode Pin 7	P17
BOOTMODE08	IO	Bootmode Pin 8	P18
BOOTMODE09	IO	Bootmode Pin 9	P19
BOOTMODE10	IO	Bootmode Pin 10	P16
BOOTMODE11	IO	Bootmode Pin 11	R17
BOOTMODE12	IO	Bootmode Pin 12	R18
BOOTMODE13	IO	Bootmode Pin 13	R19
BOOTMODE14	IO	Bootmode Pin 14	R16
BOOTMODE15	IO	Bootmode Pin 15	T17

Table 5-51. System Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
CLKOUT0	O	Clock Output 0	P1, U14, W18
EXTINTn	I	External Interrupt	P3
EXT_REFCLK1	I	External Clock Input to Main Domain	P1
MAIN_ERRORn	IO	Error Signal Output from the MAIN Domain	J4, K19, R1
OBSCLK0	O	Main Domain Observation clock output for test and debug purposes	P16
OBSCLK1	O	Main Domain Observation clock output for test and debug purposes	M3
RESETSTATz	O	Main Domain warm reset status output	H4
SYSCLKOUT0	O	Main Domain system clock output (divided by 4) for test and debug purposes only	P1

Table 5-52. WKUP System Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
PMIC_LPM_EN0	O	PMIC Enable Pin	A7
WKUP_CLKOUT0	O	WKUP Domain CLKOUT0 output	B11
WKUP_LFOSC0_XI	I	Low frequency (32.768 KHz) oscillator input	E1
WKUP_LFOSC0_XO	O	Low frequency (32.768 KHz) oscillator output	D2

Table 5-53. MCU System Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
MCU_ERRORn	IO	Error Signal Output from the MCU Domain	F3
MCU_EXT_REFCLK0	I	External Clock Input to MCU Domain	A6, C7
MCU_OBSCLK0	O	MCU Domain Observation Clock Output for test and debug purposes only	C7
MCU_OSC0_XI	I	High frequency (25 MHz) oscillator input	A2
MCU_OSC0_XO	O	High frequency (25 MHz) oscillator output	B1
MCU_PORz	I	MCU and Main Domain cold reset	E3
MCU_RESETz	I	MCU and Main Domain warm reset	D9
MCU_SYSCLKOUT0	O	MCU Domain system clock output (divided by 4) for test and debug purposes only	C7

5.3.19 SPI

Table 5-54. SPI0 Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
SPI0_CLK	IO	SPI Clock	M1
SPI0_CS0	IO	SPI Chip Select 0	J3
SPI0_CS1	IO	SPI Chip Select 1	J4
SPI0_CS2	IO	SPI Chip Select 2	N1
SPI0_CS3	IO	SPI Chip Select 3	L3
SPI0_D0	IO	SPI Data 0	K3
SPI0_D1	IO	SPI Data 1	K4

Table 5-55. SPI1 Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
SPI1_CLK	IO	SPI Clock	B18, U2
SPI1_CS0	IO	SPI Chip Select 0	E16, U1
SPI1_CS1	IO	SPI Chip Select 1	D15, T4
SPI1_CS2	IO	SPI Chip Select 2	N4
SPI1_CS3	IO	SPI Chip Select 3	V3
SPI1_D0	IO	SPI Data 0	D18, T3
SPI1_D1	IO	SPI Data 1	C18, U3

Table 5-56. SPI2 Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
SPI2_CLK	IO	SPI Clock	M2, R2
SPI2_CS0	IO	SPI Chip Select 0	M3, T2
SPI2_CS1	IO	SPI Chip Select 1	N2, R4
SPI2_CS2	IO	SPI Chip Select 2	N3, R1
SPI2_CS3	IO	SPI Chip Select 3	P1, T1
SPI2_D0	IO	SPI Data 0	L2, P2
SPI2_D1	IO	SPI Data 1	L1, R3

Table 5-57. SPI3 Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
SPI3_CLK	IO	SPI Clock	W4
SPI3_CS0	IO	SPI Chip Select 0	W5
SPI3_CS1	IO	SPI Chip Select 1	W7
SPI3_CS2	IO	SPI Chip Select 2	U6
SPI3_CS3	IO	SPI Chip Select 3	V7
SPI3_D0	IO	SPI Data 0	T7

Table 5-57. SPI3 Signal Descriptions (continued)

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
SPI3_D1	IO	SPI Data 1	U7

Table 5-58. SPI4 Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
SPI4_CLK	IO	SPI Clock	V6
SPI4_CS0	IO	SPI Chip Select 0	U6
SPI4_CS1	IO	SPI Chip Select 1	V5
SPI4_CS2	IO	SPI Chip Select 2	T6
SPI4_CS3	IO	SPI Chip Select 3	W5
SPI4_D0	IO	SPI Data 0	W7
SPI4_D1	IO	SPI Data 1	V7

5.3.20 TIMER

Table 5-59. TIMER Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
TIMER_IO0	IO	Timer Inputs and Outputs (not tied to single timer instance)	N2, U1, V6
TIMER_IO1	IO	Timer Inputs and Outputs (not tied to single timer instance)	M2, T4
TIMER_IO2	IO	Timer Inputs and Outputs (not tied to single timer instance)	L4, U2
TIMER_IO3	IO	Timer Inputs and Outputs (not tied to single timer instance)	M4, T3
TIMER_IO4	IO	Timer Inputs and Outputs (not tied to single timer instance)	P1, U3, V5
TIMER_IO5	IO	Timer Inputs and Outputs (not tied to single timer instance)	N3, N4, T6
TIMER_IO6	IO	Timer Inputs and Outputs (not tied to single timer instance)	N1, P4
TIMER_IO7	IO	Timer Inputs and Outputs (not tied to single timer instance)	L3, V2

Table 5-60. WKUP TIMER Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
WKUP_TIMER_IO0	IO	Timer Inputs and Outputs (not tied to single timer instance)	B7, C6, D6
WKUP_TIMER_IO1	IO	Timer Inputs and Outputs (not tied to single timer instance)	C5, C7

5.3.21 UART

Table 5-61. UART0 Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
UART0_CTSn	I	UART Clear to Send (active low)	F18, N1
UART0_RTSn	O	UART Request to Send (active low)	F17, L3
UART0_RXD	I	UART Receive Data	F19, L2
UART0_TXD	O	UART Transmit Data	L1, U19

Table 5-62. UART1 Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
UART1_CTSn	I	UART Clear to Send (active low)	P2
UART1_DCDn	I	UART Data Carrier Detect (active low)	M3
UART1_DSRn	I	UART Data Set Ready (active low)	N3
UART1_DTRn	O	UART Data Terminal Ready (active low)	L4
UART1_RIn	I	UART Ring Indicator	M4
UART1_RTSn	O	UART Request to Send (active low)	R3
UART1_RXD	I	UART Receive Data	F17, N2, T2
UART1_TXD	O	UART Transmit Data	F18, M2, R2

Table 5-63. UART2 Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
UART2_CTSn	I	UART Clear to Send (active low)	R16, T3, U7, V19
UART2_RTSn	O	UART Request to Send (active low)	T17, T7, U19, U2
UART2_RXD	I	UART Receive Data	A6, L16, N1, P18, U1, W7
UART2_TXD	O	UART Transmit Data	D7, L3, M17, P19, T4, V7

Table 5-64. UART3 Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
UART3_CTSn	I	UART Clear to Send (active low)	U18, V2, W4
UART3_RTSn	O	UART Request to Send (active low)	G16, P4, W5
UART3_RXD	I	UART Receive Data	C6, E19, P16, U3, U6
UART3_TXD	O	UART Transmit Data	B6, G19, N4, R17, V6

Table 5-65. UART4 Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
UART4_CTSn	I	UART Clear to Send (active low)	C14, M17
UART4_RTSn	O	UART Request to Send (active low)	B14, L16
UART4_RXD	I	UART Receive Data	B12, D6, G18, L18, R18
UART4_TXD	O	UART Transmit Data	C12, C5, H16, K18, R19

Table 5-66. UART5 Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
UART5_CTSn	I	UART Clear to Send (active low)	B19, G17
UART5_RTSn	O	UART Request to Send (active low)	A18, F19
UART5_RXD	I	UART Receive Data	A14, D15, H18, L4, R16
UART5_TXD	O	UART Transmit Data	A16, B13, H17, M4, T17

Table 5-67. UART6 Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
UART6_CTSn	I	UART Clear to Send (active low)	C18, F17
UART6_RTSn	O	UART Request to Send (active low)	D18, F18
UART6_RXD	I	UART Receive Data	D12, E16, F19, K17, P2, P4
UART6_TXD	O	UART Transmit Data	B18, C13, L19, R3, U18, V2

Table 5-68. WKUP UART Signal Descriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
WKUP_UART0_CTSn	I	UART Clear to Send (active low)	D6
WKUP_UART0_RTSn	O	UART Request to Send (active low)	C5
WKUP_UART0_RXD	I	UART Receive Data	B5
WKUP_UART0_TXD	O	UART Transmit Data	A5

5.3.22 USB

Table 5-69. USB Signal Descpriptions

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
USB0_DM	IO	USB 2.0 Differential Data (negative)	W9
USB0_DP	IO	USB 2.0 Differential Data (positive)	V9
USB0_DRVVBUS	O	USB VBUS control output (active high)	W2
USB0_RCALIB	IO	Pin to connect to calibration resistor	V8

Table 5-69. USB Signal Descpriptions (continued)

SIGNAL NAME [1]	SIGNAL TYPE [2]	DESCRIPTION [3]	ANJ PIN [4]
USB0_VBUS	A	USB Level-shifted VBUS Input	U9

5.4 Pin Connectivity Requirements

Ball Number	Ball Name	Pin Connectivity Requirements
F3 B10	MCU_ERRORn TRSTn	Each of these balls must be connected to VSS through separate external pull resistors to ensure the inputs associated with these balls are held to a valid logic low level if a PCB signal trace is connected and not actively driven by an attached device. The internal pull-down can be used to hold a valid logic low level if no PCB signal trace is connected to the ball.
C9 C10 D9 P3 A10 D10 C11	EMU0 EMU1 MCU_RESETz EXTINTn TCK TDI TMS	Each of these balls must be connected to the corresponding power supply(1) through separate external pull resistors to ensure the inputs associated with these balls are held to a valid logic high level if a PCB signal trace is connected and not actively driven by an attached device. The internal pull-up can be used to hold a valid logic high level if no PCB signal trace is connected to the ball.
B9 A8	WKUP_I2C0_SCL WKUP_I2C0_SDA	Each of these balls must be connected to the corresponding power supply(1) through separate external pull resistors to ensure the inputs associated with these balls are held to a valid logic high level.
N10 P10 R9	VDDA_CORE_USB VDDA_1P8_USB VDDA_3P3_USB	If USB0 is not used, each of these balls must be connected directly to VSS.
W9 V9 V8 U9	USB0_DM USB0_DP USB0_RCALIB USB0_VBUS	If USB0 is not used, leave the DM, DP, and VBUS balls unconnected. Note: The USB0_RCALIB ballcan only be left unconnected when VDDA_CORE_USB, VDDA_1P8_USB, and VDDA_3P3_USB are connected to VSS. The USB0_RCALIB ball must be connected to VSS through an appropriate external resistor when VDDA_CORE_USB, VDDA_1P8_USB, and VDDA_3P3_USB are connected to power sources.
H8	VMON_ER_VSYS	If VMON_ER_VSYS is not used, this ball must be connected directly to VSS.
J6	VMON_1P8_SOC	If VMON_1P8_SOC is not used to monitor the SOC power rail, this ball must remain connected to a 1.8-V power supply.
H5	VMON_3P3_SOC	If VMON_3P3_SOC is not used to monitor the SOC power rail, this ball must remain connected to a 3.3-V power rail or connected directly to VSS.
A3 A12 B3 E2 E4 G3 W8	RSVD_A3 RSVD_A12 RSVD_B3 RSVD_E2 RSVD_E4 RSVD_G3 RSVD_W8	Each of these balls must be left unconnected.
LVCMOS PIN	Any LVCMOS Voltage Buffer Pin	If an associated IOMUX pad configuration register exists for a given pin, it may remain unconnected. After PORz, the LVCMOS voltage buffer is configured to a default state compatible with an unconnected ball.

(1) To determine which power supply is associated with any IO, see the POWER column of the *Pin Attributes* table.

6 Specifications

Note

All specifications listed are preliminary and may change during device characterization.

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)[1] [2]

PARAMETER		MIN	MAX	UNIT
VDD_CORE	Core supply	–0.3	1.05	V
VDDR_CORE	RAM core Supply	–0.3	1.05	V
VDD_CANUART	CANUART core supply	–0.3	1.05	V
VDDR_CANUART	CANUART RAM core supply	–0.3	1.05	V
VDDA_CORE_USB	USB0 core supply	–0.3	1.05	V
VDDS_OSC0	MCU_OSC0, OSC1, and WKUP_LFOSC0 supply	–0.3	1.98	V
VDDA_MCU	MCU PLL, RC Oscillator, Supply Detectors analog supply	–0.3	1.98	V
VDDA_PLL0	Main PLL analog supply	–0.3	1.98	V
VDDA_PLL1	Audio PLL analog supply	–0.3	1.98	V
VDDA_PLL2	C7x PLL analog supply	–0.3	1.98	V
VDDA_ADC0	ADC analog supply	–0.3	1.98	V
VDDA_1P8_USB	USB0 1.8 V analog supply	–0.3	1.98	V
VDDA_TEMP0	Analog supply for temperature sensor 0	–0.3	1.98	V
VDDA_TEMP1	Analog supply for temperature sensor 1	–0.3	1.98	V
VPP	eFuse ROM programming supply	–0.3	1.98	V
VDDSHV_MCU	IO supply for IO group MCU	–0.3	3.63	V
VDDSHV_CANUART	IO supply for IO group CANUART	–0.3	3.63	V
VDDSHV0	IO supply for IO group 0	–0.3	3.63	V
VDDSHV1	IO supply for IO group 1	–0.3	3.63	V
VDDSHV2	IO supply for IO group 2	–0.3	3.63	V
VDDSHV3	IO supply for IO group 3	–0.3	3.63	V
VDDSHV5	IO supply for IO group 5	–0.3	3.63	V
VDDA_3P3_USB	USB0 3.3 V analog supply	–0.3	3.63	V
Steady-state max voltage at all fail-safe IO pins	MCU_PORz	–0.3	3.63	V
	WKUP_I2C0_SDA and WKUP_I2C0_SCL, EXTINTn When operating at 1.8 V	–0.3	1.98[3]	V
	WKUP_I2C0_SDA and WKUP_I2C0_SCL, EXTINTn When operating at 3.3 V	–0.3	3.63[3]	v
	VMON_1P8_SOC	–0.3	1.98	V
	VMON_3P3_SOC	–0.3	3.63	V
	VMON_ER_VSYS	–0.3[4]	1.98	V
Steady-state max voltage at all other IO pins[5]	USB0_VBUS[6]	–0.3	3.6	V
	All other IO pins	–0.3	IO supply voltage + 0.3	V
Transient overshoot and undershoot at IO pin	20% of IO supply voltage for up to 20% of the signal period		0.2 × VDD[7]	V
Latch-up performance[8]	I-Test	–100	100	mA
	Over-Voltage (OV) Test		1.5 × VDD[7]	V

over operating junction temperature range (unless otherwise noted)(1) (2)

PARAMETER		MIN	MAX	UNIT
Storage temperature	T_{stg}	–55	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to VSS, unless otherwise noted.
(3) The absolute maximum ratings for these fail-safe pins depends on their IO supply operating voltage. Therefore, this value is also defined by the maximum VIH value found in the I2C Open-Drain, and Fail-Safe (I2C OD FS) Electrical Characteristics section, where the electrical characteristics table has separate parameter values for 1.8 V mode and 3.3 V mode.
(4) The VMON_ER_VSYS pin provides a way to monitor the system power supply. For more information, see *System Power Supply Monitor Design Guidelines*.
(5) This parameter applies to all IO pins which are not fail-safe and the requirement applies to all values of IO supply voltage. For example, if the voltage applied to a specific IO supply is 0 volts the valid input voltage range for any IO powered by that supply will be –0.3 to +0.3 volts. Special attention should be applied anytime peripheral devices are not powered from the same power sources used to power the respective IO supply. It is important the attached peripheral never sources a voltage outside the valid input voltage range, including power supply ramp-up and ramp-down sequences.
(6) An external resistor divider is required to limit the voltage applied to this device pin. For more information, see *USB Design Guidelines*.
(7) VDD is the voltage on the corresponding power-supply pin(s) for the IO.
(8) For current pulse injection (I-Test):
• Pins stressed per JEDEC JESD78 (Class II) and passed with specified I/O pin injection current and clamp voltage of 1.5 times maximum recommended I/O voltage and negative 0.5 times maximum recommended I/O voltage.
For over-voltage performance (Over-Voltage (OV) Test):
• Supplies stressed per JEDEC JESD78 (Class II) and passed specified voltage injection.

6.2 Electrostatic Discharge (ESD) for AEC - Q100 devices

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic Discharge (ESD)	Human body model (HBM), per AEC-Q100-002(1)		±1000	V
		Charged device model (CDM), per AEC-Q100-011	Corner pins (A1, A19, W1, W19)	±750	
			All other pins	±250	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification

6.3 Electrostatic Discharge (ESD) for non AEC - Q100 devices

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic Discharge (ESD)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±250	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.4 Power-On Hours (POH) Summary

over recommended operating conditions (unless otherwise noted)(1) (2) (3)

PARAMETER	INDUSTRIAL	AUTOMOTIVE
Operating Junction Temperature	–40°C to 105°C	–40°C to 125°C
POH @ Temp Profile	100K @ 90°C (100% @ 90°C)	20K @ Automotive Temp Profile(4)

(1) This information is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.
(2) Unless specified in the table above, all voltage domains and operating conditions are supported in the device at the noted temperatures.
(3) POH is a function of voltage, temperature, and time. Usage at higher voltages and temperatures will result in a reduction in POH.
(4) See *Automotive Temperature Profile* section

6.5 Automotive Temperature Profile

T_J (°C)	HOURS	DAYS	YEARS	PERCENT OF TIME
–40	1000	~41	~0.11	5%
70	13000	~541	~1.48	65%
110	4000	~166	~0.45	20%
125	2000	~83	~0.22	10%
Total	20000	~833	~2.28	100%

6.6 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

Parameter	DESCRIPTION		MIN(1)	NOM	MAX(1)	UNIT
VDD_CORE(2) VDDA_CORE_USB(2)	Core supply USB0 core supply	0.75-V operation	0.715	0.75	0.79	V
		0.85-V operation	0.81	0.85	0.895	V
VDD_CANUART(3)	CANUART core supply	0.75-V operation	0.715	0.75	0.79	V
		0.85-V operation	0.81	0.85	0.895	V
VDDR_CORE	RAM core supply		0.81	0.85	0.895	V
VDDR_CANUART	CANUART RAM core supply		0.81	0.85	0.895	V
VDDS_OSC0	MCU_OSC0, OSC1, and WKUP_LFOSC0 supply		1.71	1.8	1.89	V
VDDA_MCU	MCU PLL, RC Oscillator, Supply Detectors analog supply		1.71	1.8	1.89	V
VDDA_PLL0	Main PLL analog supply		1.71	1.8	1.89	V
VDDA_PLL1	Audio PLL analog supply		1.71	1.8	1.89	V
VDDA_PLL2	C7x PLL analog supply		1.71	1.8	1.89	V
VDDA_ADC0	ADC analog supply		1.71	1.8	1.89	V
VDDA_1P8_USB	USB0 1.8 V analog supply		1.71	1.8	1.89	V
VDDA_TEMP0	Analog supply for temperature sensor 0		1.71	1.8	1.89	V
VDDA_TEMP1	Analog supply for temperature sensor 1		1.71	1.8	1.89	V
VPP	eFuse ROM programming supply		see(4)	see(4)	see(4)	V
VMON_1P8_SOC	Voltage monitor for 1.8-V SoC Power Supply		1.71	1.8	1.89	V
VDDA_3P3_USB	USB0 3.3-V analog supply		3.135	3.3	3.465	V
VMON_3P3_SOC	Voltage monitor for 3.3-V SoC power supply		3.135	3.3	3.465	V
VMON_ER_VSYS	Voltage monitor for system power supply		0	see(5)	1	V
USB0_VBUS	USB0 Level-shifted VBUS Input		0	see(6)	3.465	V
VDDSHV_CANUART(7)	Dual-voltage IO supply for IO group CANUART	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.135	3.3	3.465	V
VDDSHV_MCU	Dual-voltage IO supply for IO group MCU	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.135	3.3	3.465	V
VDDSHV0	Dual-voltage IO supply for IO group 0	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.135	3.3	3.465	V
VDDSHV1	Dual-voltage IO supply for IO group 1	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.135	3.3	3.465	V
VDDSHV2	Dual-voltage IO supply for IO group 2	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.135	3.3	3.465	V
VDDSHV3	Dual-voltage IO supply for IO group 3	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.135	3.3	3.465	V
VDDSHV5	Dual-voltage IO supply for IO group 5	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.135	3.3	3.465	V

over operating junction temperature range (unless otherwise noted)

Parameter	DESCRIPTION		MIN(1)	NOM	MAX(1)	UNIT
T_J	Operating junction temperature range	Industrial	–40		105	°C
		Automotive	–40		125	°C

(1) The voltage at the device ball must never drop below the MIN voltage or rise above the MAX voltage for any amount of time during normal device operation.
(2) VDD_CORE and VDDA_CORE_USB shall be sourced from the same power source. Care should be taken to ensure that voltage differential between VDD_CORE and VDDA_CORE_USB is within ±1%.
(3) VDD_CANUART shall be connected to an always on power source when using Partial IO low power mode. VDD_CANUART shall be connected to the same power source as VDD_CORE and VDDA_CORE_USB when not using Partial IO low power mode.
(4) Refer to the *VPP Specifications* table for VPP supply voltages based on eFuse usage.
(5) The VMON_ER_VSYS pin provides a way to monitor the system power supply. For more information, see *System Power Supply Monitor Design Guidelines*.
(6) An external resistor divider is required to limit the voltage applied to this device pin. For more information, see *USB Design Guidelines*.
(7) VDDSHV_CANUART shall be connected to an always on power source when using Partial IO low power mode. VDDSHV_CANUART shall be connected to any valid IO power supply source when not using Partial IO low power mode.

6.7 Device Speed Grades

This section describes the operating conditions of the device.

Speed Grade	VDD_CORE (V)(1)	MAXIMUM OPERATING FREQUENCY (MHz)						
		R5FSS0/1 (MHz)	DSP0/1 (MHz)	R5F SYSCLK (MHz)	Device Manager R5F (MHz)	ASRC0/1 (MHz)	Main CBASS SYSCLK1 (MHz)	L3 SRAM (MB)
F	0.75-V	800	850	400	800	200	500	6
	0.85-V	1000	1000	500	800	200	500	
E	0.75-V	800	750	400	800	200	500	5.5
	0.85-V							
D	0.75-V	800	500	400	800	200	500	4.5
	0.85-V							
C	0.75-V	800	400	400	400	200	500	2.5
	0.85-V							
B	0.75-V	400	400	200	400	200	500	2
	0.85-V							
A	0.75-V	400	250	200	400	200	500	1
	0.85-V							

(1) Nominal operating voltage, see *Recommended Operating Conditions*.

6.8 Power Consumption Summary

For information on the device power consumption contact your TI Representative.

6.9 Electrical Characteristics

Note

The interfaces or signals described in Section 6.9 correspond to the interfaces or signals available in multiplexing mode 0 (Primary Signal Function).

All interfaces or signals multiplexed on the balls described in these tables have the same DC electrical characteristics, unless multiplexing involves a PHY and GPIO combination, in which case different DC electrical characteristics are specified for the different multiplexing modes (Functions).

6.9.1 I2C Open-Drain and Fail-Safe (I2C OD FS) Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
1.8 V Mode						
V_{IL}	Input Low Voltage				0.3 × VDD(1)	V
V_{ILSS}	Input Low Voltage Steady State				0.3 × VDD(1)	V
V_{IH}	Input High Voltage		0.7 × VDD(1)		1.98(2)	V
V_{IHSS}	Input High Voltage Steady State		0.7 × VDD(1)			V
V_{HYS}	Input Hysteresis Voltage		0.1 × VDD(1)			V
I_{IN}	Input Leakage Current	V_I = 1.8 V or V_I = 0 V			±10	µA
V_{OL}	Output Low Voltage				0.2 × VDD(1)	V
I_{OL} (3)	Low Level Output Current	$V_{OL(MAX)}$	10			mA
SR_I (5)	Input Slew Rate		18f(4) or 1.8E+6			V/s
3.3 V Mode (6)						
V_{IL}	Input Low Voltage				0.3 × VDD(1)	V
V_{ILSS}	Input Low Voltage Steady State				0.25 × VDD(1)	V
V_{IH}	Input High Voltage		0.7 × VDD(1)		3.63(2)	V
V_{IHSS}	Input High Voltage Steady State		0.7 × VDD(1)			V
V_{HYS}	Input Hysteresis Voltage		0.05 × VDD(1)			V
I_{IN}	Input Leakage Current	V_I = 3.3 V or V_I = 0 V			±10	µA
V_{OL}	Output Low Voltage				0.4	V
I_{OL} (3)	Low Level Output Current	$V_{OL(MAX)}$	10			mA
SR_I (5)	Input Slew Rate		33f(4) or 3.3E+6			V/s

(1) VDD stands for corresponding power supply. For more information ont he power supply name and the corresponding ball(s), see POWER column of the *Pin Attributes* table.
(2) This value also defines the Absolute Maximum Ratings value for the IO
(3) The I_{OL} parameter defines the minimum Low Level Output Current for which the device is able to maintain the specified V_{OL} value.
(4) f = toggle frequency of the input signal in Hz.
(5) This MIN parameter only applies to input signal functions which are not defined in their respective *Timing and Switching Characteristics* sections. Select the MIN parameter which results in the largest value.
(6) I2C Hs-mode is not supported when operating the IO in 3.3 V mode.

6.9.2 Fail-Safe Reset (FS RESET) Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Input Low Voltage				0.3 × VDDS_OSC0	V
V_{ILSS}	Input Low Voltage Steady State				0.3 × VDDS_OSC0	V
V_{IH}	Input High Voltage		0.7 × VDDS_OSC0			V
V_{IHSS}	Input High Voltage Steady State		0.7 × VDDS_OSC0			V
V_{HYS}	Input Hysteresis Voltage		200			mV
I_{IN}	Input Leakage Current	V_I = 1.8 V or V_I = 0 V			±10	µA
SR_I (2)	Input Slew Rate		18f(1) or 1.8E+6			V/s

(1) f = toggle frequency of the input signal in Hz.
(2) This MIN parameter only applies to input signal functions which are not defined in their respective *Timing and Switching Characteristics* sections. Select the MIN parameter which results in the largest value.

6.9.3 High-Frequency Oscillators (MCU_OSC0 and OSC1) Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Input Low Voltage				0.35 × VDDS_OSC0	V
V_{IH}	Input High Voltage		0.65 × VDDS_OSC0			V
V_{HYS}	Input Hysteresis Voltage			49		mV
I_{IN}	Input Leakage Current	V_I = 1.8 V or V_I = 0 V			±10	µA

6.9.4 Low-Frequency Oscillator (WKUP_LFOSC0) Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Input Low Voltage				0.3 × VDDS_OSC0	V
V_{IH}	Input High Voltage		0.7 × VDDS_OSC0			V
V_{HYS}	Input Hysteresis Voltage	Active Mode		85		mV
		Bypass Mode		324		mV
I_{IN}	Input Leakage Current	V_I = 1.8 V or V_I = 0 V			±10	µA

6.9.5 SDIO Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
1.8 V Mode						
V_{IL}	Input Low Voltage				0.58	V

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ILSS}	Input Low Voltage Steady State				0.58	V
V_{IH}	Input High Voltage		1.27			V
V_{IHSS}	Input High Voltage Steady State		1.7			V
V_{HYS}	Input Hysteresis Voltage		150			mV
I_{IN}	Input Leakage Current	V_I = 1.8 V or V_I = 0 V			±10	µA
R_{PU}	Pull-up Resistor		40	50	60	kΩ
R_{PD}	Pull-down Resistor		40	50	60	kΩ
V_{OL}	Output Low Voltage				0.45	V
V_{OH}	Output High Voltage		VDDSHV5 – 0.45			V
I_{OL} (1)	Low Level Output Current	$V_{OL(MAX)}$	4			mA
I_{OH} (3)	High Level Output Current	$V_{OH(MIN)}$	4			mA
SR_I (3)	Input Slew Rate		18f(2) or 1.8E+6			V/s
3.3 V Mode						
V_{IL}	Input Low Voltage				0.25 × VDDHV5	V
V_{ILSS}	Input Low Voltage Steady State				0.15 × VDDHV5	V
V_{IH}	Input High Voltage		0.625 × VDDHV5			V
V_{IHSS}	Input High Voltage Steady State		0.625 × VDDHV5			V
V_{HYS}	Input Hysteresis Voltage		150			mV
I_{IN}	Input Leakage Current	V_I = 3.3 V or V_I = 0 V			±10	µA
R_{PU}	Pull-up Resistor		40	50	60	kΩ
R_{PD}	Pull-down Resistor		40	50	60	kΩ
V_{OL}	Output Low Voltage				0.125 × VDDHV5	V
V_{OH}	Output High Voltage		0.75 × VDDHV5			V
I_{OL} (1)	Low Level Output Current	$V_{OL(MAX)}$	6			mA
I_{OH} (3)	High Level Output Current	$V_{OH(MIN)}$	10			mA
SR_I (3)	Input Slew Rate		33f(2) or 3.3E+6			V/s

(1) The I_{OL} and I_{OH} parameters defines the minimum Low Level Output Current and High Level Output Current for which the device is able to maintain the specified V_{OL} and V_{OH} values. Values defined by these parameters should be considered the maximum current available to a system implementation which needs to maintain the specified V_{OL} and V_{OH} values for attached components.
(2) f = toggle frequency of the input signal in Hz.
(3) This MIN parameter only applies to input signal functions which are not defined in their respective *Timing and Switching Characteristics* sections. Select the MIN parameter which results in the largest value.

6.9.6 Analog-to-Digital Converter (ADC)

over operating junction temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analog Input						
$V_{MCU\_ADC0[7:0]}$	Full-scale Input Range		VSS		VDDA_ADC0	V
DNL	Differential Non-Linearity		–1	0.5	4	LSB
INL	Integral Non-Linearity			±1	±4	LSB
$LSB_{GAIN-ERROR}$	Gain Error			±2		LSB
$LSB_{OFFSET-ERROR}$	Offset Error			±2		LSB
C_{IN}	Input Sampling Capacitance			5.5		pF
SNR	Signal-to-Noise Ratio	Input Signal: 200 kHz sine wave at -0.5dB Full Scale		70		dB
THD	Total Harmonic Distortion	Input Signal: 200 kHz sine wave at -0.5dB Full Scale		73		dB
SFDR	Spurious Free Dynamic Range	Input Signal: 200 kHz sine wave at -0.5dB Full Scale		76		dB
$SNR_{(PLUS)}$	Signal-to-Noise Plus Distortion	Input Signal: 200 kHz sine wave at -0.5dB Full Scale		69		dB
$R_{MCU\_ADC0\_AIN[7:0]}$	Input Impedance of MCU_ADC0_AIN[7:0]	f = input frequency		$[1/((65.97 \times 10^{-12}) \times f_{SMPL\_CLK})]$		LSBs
I_{IN}	Input Leakage	MCU_ADC0_AIN[7:0] = VSS			–10	µA
		MCU_ADC0_AIN[7:0] = VDDA_ADC0			24	µA
Sampling Dynamics						
F_{SMPL_CLK}	SMPL_CLK Frequency			60		MHz
t_C	Conversion Time			13		ADC0 SMPL_CLK Cycles
t_{ACQ}	Acquisition time		2		257	ADC0 SMPL_CLK Cycles
T_R	Sampling Rate	ADC0 SMPL_CLK = 60 MHz		4		MSPS
CCISO	Channel to Channel Isolation			100		dB
General Purpose Input Mode (1)						
V_{IL}	Input low-level threshold				0.35 × VDDA_ADC0	V
V_{ILSS}	Input low-level threshold steady state				0.35 × VDDA_ADC0	V
V_{IH}	Input high-level threshold		0.65 × VDDA_ADC0			V
V_{IHSS}	Input high-level threshold steady state		0.65 × VDDA_ADC0			V

over operating junction temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{HYS}	Input Hysteresis Voltage		200			mV
I_{IN}	Input Leakage Current	V_I = 1.8 V or 0 V			6	µA

(1) MCU_ADC0 can be configured to operate in General Purpose Input mode, where all MCU_ADC0_AIN[7:0] inputs are globally enabled to operate as digital inputs via the ADC0_CTRL register (gpi_mode_en = 1)

6.9.7 LVCMOS Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
1.8 V Mode						
V_{IL}	Input Low Voltage				0.35 × VDD(1)	V
V_{ILSS}	Input Low Voltage Steady State				0.3 × VDD(1)	V
V_{IH}	Input High Voltage		0.65 × VDD(1)			V
V_{IHSS}	Input High Voltage Steady State		0.85 × VDD(1)			V
V_{HYS}	Input Hysteresis Voltage		150			mV
I_{IN}	Input Leakage Current	V_I = 1.8 V or V_I = 0 V			±10	µA
R_{PU}	Pull-up Resistor		15	22	30	kΩ
R_{PD}	Pull-down Resistor		15	22	30	kΩ
V_{OL}	Output Low Voltage				0.45	V
V_{OH}	Output High Voltage		VDD(1) – 0.45			V
I_{OL} (2)	Low Level Output Current	$V_{OL(MAX)}$	3			mA
I_{OH} (4)	High Level Output Current	$V_{OH(MIN)}$	3			mA
SR_I (4)	Input Slew Rate		18f(3) or 1.8E+6			V/s
3.3 V Mode						
V_{IL}	Input Low Voltage				0.8	V
V_{ILSS}	Input Low Voltage Steady State				0.6	V
V_{IH}	Input High Voltage		2.0			V
V_{IHSS}	Input High Voltage Steady State		2.0			V
V_{HYS}	Input Hysteresis Voltage		150			mV
I_{IN}	Input Leakage Current	V_I = 1.8 V or V_I = 0 V			±10	µA
R_{PU}	Pull-up Resistor		15	22	30	kΩ
R_{PD}	Pull-down Resistor		15	22	30	kΩ
V_{OL}	Output Low Voltage				0.4	V
V_{OH}	Output High Voltage		2.4			V
I_{OL} (2)	Low Level Output Current	$V_{OL(MAX)}$	5			mA
I_{OH} (4)	High Level Output Current	$V_{OH(MIN)}$	9			mA
SR_I (4)	Input Slew Rate		33f(3) or 3.3E+6			V/s

(1) VDD stands for corresponding power supply. For more information on the power supply name and the corresponding ball(s), see POWER column of the *Pin Attributes* table.

(2) The I_{OL} and I_{OH} parameters defines the minimum Low Level Output Current and High Level Output Current for which the device is able to maintain the specified V_{OL} and V_{OH} values. Values defined by these parameters should be considered the maximum current available to a system implementation which needs to maintain the specified V_{OL} and V_{OH} values for attached components.

(3) f = toggle frequency of the input signal in Hz.
(4) This MIN parameter only applies to input signal functions which are not defined in their respective *Timing and Switching Characteristics* sections. Select the MIN parameter which results in the largest value.

6.9.8 USB2PHY Electrical Characteristics

Note

The USB0 interface is compliant with Universal Serial Bus Revision 2.0 Specification dated April 27, 2000 including ECNs and Errata as applicable.

6.10 VPP Specifications for One-Time Programmable (OTP) eFuses

This section specifies the operating conditions required for programming the OTP eFuses.

6.10.1 VPP Specifications

over recommended operating conditions (unless otherwise noted)

PARAMETER	DESCRIPTION	MIN	NOM	MAX	UNIT
VDD_CORE	Supply voltage range for the core domain during OTP operation; OPP NOM (BOOT)	See *Recommended Operating Conditions*			V
VPP	Supply voltage range for the eFuse ROM domain during normal operation without hardware support to program eFuse ROM		NC(1)		V
	Supply voltage range for the eFuse ROM domain during normal operation with hardware support to program eFuse ROM		0		
	Supply voltage range for the eFuse ROM domain during OTP programming(2)	1.71	1.8	1.89	V
$I_{(VPP)}$	VPP Current			400	mA
$SR_{(VPP)}$	VPP Slew Rate			6E + 4	V/s
T_J	Operating junction temperature range while programming eFuse ROM	0	25	85	℃

(1) NC indicates No Connect
(2) Supply voltage range includes DC errors and peak-to-peak noise.

6.10.2 Hardware Requirements

The following hardware requirements must be met when programming keys in the OTP eFuses:

- The VPP power supply must be disabled when not programming OTP registers.
- The VPP power supply must be ramped up after the proper device power-up sequence (for more details, see Section 6.12.2.2 - *Power Supply Sequencing*).

6.10.3 Programming Sequence

Programming sequence for OTP eFuses:

- Power on the board per the power-up sequencing. No voltage should be applied on the VPP terminal during power up and normal operation.
- Load the OTP write software required to program the eFuse (contact your local TI representative for the OTP software package).
- Apply the voltage on the VPP terminal according to the specification in VPP Specifications.
- Run the software that programs the OTP registers.
- After validating the content of the OTP registers, remove the voltage from the VPP terminal.

6.10.4 Impact to Your Hardware Warranty

You accept that e-Fusing the TI Devices with security keys permanently alters them. You acknowledge that the e-Fuse can fail, for example, due to incorrect or aborted program sequence or if you omit a sequence step. Further the TI Device may fail to secure boot if the error code correction check fails for the Production Keys or if the image is not signed and optionally encrypted with the current active Production Keys. These types of situations will render the TI Device inoperable and TI will be unable to confirm whether the TI Devices conformed to their specifications prior to the attempted e-Fuse. CONSEQUENTLY, TI WILL HAVE NO LIABILITY (WARRANTY OR OTHERWISE) FOR ANY TI DEVICES THAT HAVE BEEN e-FUSED WITH SECURITY KEYS.

6.11 Thermal Resistance Characteristics

This section provides the thermal resistance characteristics used on this device.

For reliability and operability concerns, the maximum junction temperature of the device has to be at or below the T_J value identified in Recommended Operating Conditions.

6.11.1 Package Thermal Characteristics

It is recommended to perform thermal simulations at the system level with the worst-case device power consumption.

NO.	PARAMETER	DESCRIPTION	℃/W(1) (2)	AIR FLOW (m/s)(3)
T1	$R\Theta_{JC}$	Junction-to-case	1.2	N/A
T2	$R\Theta_{JB}$	Junction-to-board	3.8	N/A
T3	$R\Theta_{JA}$	Junction-to-free air	14.4	0
T4		Junction-to-moving air	10.0	1
T5			8.9	2
T6			8.3	3
T7	Ψ_{JT}	Junction-to-package top	0.46	0
T8			0.47	1
T9			0.48	2
T10			0.49	3
T11	Ψ_{JB}	Junction-to-board	3.7	0
T12			3.3	1
T13			3.2	2
T14			3.2	3

(1) These values are based on a JEDEC defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air)
- JESD51-3, Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
- JESD51-6, Integrated Circuit Thermal Test Method Environmental Conditions - Forced Convection (Moving Air)
- JESD51-7, High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
- JESD51-9, Test Boards for Area Array Surface Mount Packages

(2) ℃/W = degrees Celsius per watt
(3) m/s = meters per second

6.12 Timing and Switching Characteristics

Note

The Timing Requirements and Switching Characteristics values can change following the silicon characterization result.

Note

The default SLEWRATE settings in each pad configuration register must be used to provide timings, unless specific instructions are given otherwise.

6.12.1 Timing Parameters and Information

The timing parameter symbols used in Section 6.12, *Timing and Switching Characteristics* are created in accordance with JEDEC Standard 100. To shorten the symbols, some pin names and other related terminologies have been abbreviated in Table 6-1:

Table 6-1. Timing Parameters Subscripts

SYMBOL	PARAMETER
c	Cycle time (period)
d	Delay time
dis	Disable time
en	Enable time
h	Hold time
su	Setup time
START	Start bit
t	Transition time
v	Valid time
w	Pulse duration (width)
X	Unknown, changing, or don't care level
F	Fall time
H	High
L	Low
R	Rise time
V	Valid
IV	Invalid
AE	Active Edge
FE	First Edge
LE	Last Edge
Z	High impedance

6.12.2 Power Supply Requirements

This section describes the power supply requirements to ensure proper device operation.

Note

All power balls must be supplied with the voltages specified in the Recommended Operating Conditions section, unless otherwise specified in Signal Descriptions and Pin Connectivity Requirements.

6.12.2.1 Power Supply Slew Rate Requirement

To maintain the safe operating range of the internal ESD protection devices, TI recommends limiting the maximum slew rate of supplies to be less than 18 mV/µs. For instance, as shown in Figure 6-1, TI recommends having the supply ramp slew for a 1.8-V supply of more than 100 µs.

Figure 6-1 describes the Power Supply Slew Rate Requirement in the device.

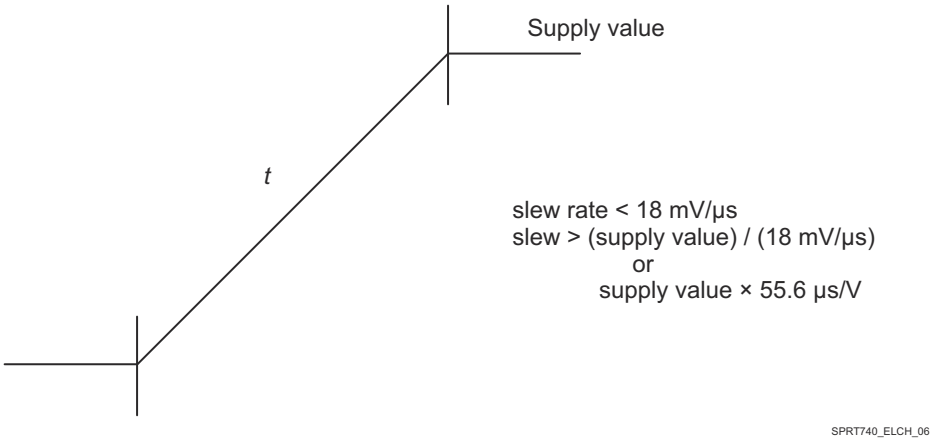


Figure 6-1. Power Supply Slew and Slew Rate

6.12.2.2 Power Supply Sequencing

This section describes power sequence requirements using power sequence diagrams and associated notes. Each power sequence diagram demonstrates the sequential order expected for each device power rail. This is done by assigning each device power rail to one or more waveform. A dual-voltage power rail may be associated with more than one waveform and the associated note will describe which waveform is applicable. Each waveform defines a transition region for the associated power rails and shows its sequential relationship to the transition regions of other power rails. The notes associated with the power sequence diagram provides further detail of these requirements. See the *Power-up Sequence* section for details on power-up requirements, and the *Power-down Sequence* section for details on power-down requirements.

Two types of power supply transition regions are used to simplify the power supply sequencing diagrams. The legends shown in Figure 6-2 and Figure 6-3 along with their descriptions are provided to clarify what each transition regions represents.

Figure 6-2 defines a transition region with multiple power rails which may be sourced from multiple power supplies or a single power supply. Transitions shown within the transition region represent a use case where multiple power supplies are used to source power rails associated with this waveform, and these power supplies are allowed to ramp at different times within the region since they do not have any specific sequence requirement relative to each other.

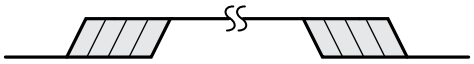


Figure 6-2. Multiple Power Supply Transition Legend

Figure 6-3 defines a transition region with one or more power rails which must be sourced from a single common power supply. No transitions are shown within the region to represent a single ramp within the transition region.

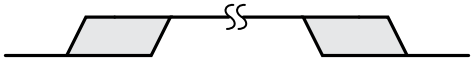


Figure 6-3. Single Common Power Supply Transition Legend

6.12.2.2.1 Power-Up Sequencing without IO Retention

Table 6-2 and Figure 6-4 describes the device power-up sequencing.

Table 6-2. Power-Up Sequencing – Supply / Signal Assignments

See: Figure 6-4

WAVEFORM	SUPPLY / SIGNAL NAME
A	VSYS(1), VMON_ER_VSYS(2)
B	VDDA_3P3_USB, VDDSHV_CANUART(3), VDDSHV_MCU(3), VDDSHV0(3), VDDSHV1(3), VDDSHV2(3), VDDSHV3(3), VMON_3P3_SOC(4)
C	VDDA_MCU, VDDA_PLL0, VDDA_PLL1, VDDA_PLL2, VDDA_1P8_USB, VDDA_ADC0, VDDA_TEMP0, VDDA_TEMP1, VDDSHV_CANUART(5), VDDSHV_MCU(5), VDDSHV0(5), VDDSHV1(5), VDDSHV2(5), VDDSHV3(5), VDDS_OSC0, VMON_1P8_SOC(6)
D	VDDSHV5(7)
E	VDD_CANUART(8)
F	VDD_CORE(8) (10), VDDA_CORE_USB0(8)
G	VDD_CORE(9) (10), VDDA_CORE_USB0(9), VDDR_CORE(10), VDDR_CANUART(9)
H	VPP(11)
I	MCU_PORz
J	MCU_OSC0_XI, MCU_OSC0_XI

(1) VSYS represents the name of a supply which sources power to the entire system. This supply is expected to be a pre-regulated supply that sources power management devices which source all other supplies.

(2) VMON_ER_VSYS input is used to monitor VSYS via an external resistor divider circuit. For more information, see System Power Supply Monitor Design Guidelines.

(3) VDDSHV_CANUART, VDDSHV_MCU, and VDDSHVx [x=0-3] are dual voltage IO supplies which can be operated at 1.8V or 3.3V depending on the application requirements.

When any of the VDDSHV_CANUART, VDDSHV_MCU, and VDDSHVx [x=0-3] IO supplies are operating at 3.3V, they shall be ramped up with other 3.3V supplies during the 3.3V ramp period defined by this waveform.

(4) The VMON_3P3_SOC input is used to monitor supply voltage and shall be connected to the respective 3.3V supply source.

(5) VDDSHV_CANUART, VDDSHV_MCU, and VDDSHVx [x=0-3] are dual voltage IO supplies which can be operated at 1.8V or 3.3V depending on the application requirements.

When any of the VDDSHV_CANUART, VDDSHV_MCU, and VDDSHVx [x=0-3] IO supplies are operating at 1.8V, they shall be ramped up with other 1.8V supplies during the 1.8V ramp period defined by this waveform.

(6) The VMON_1P8_SOC input is used to monitor supply voltage and shall be connected to the respective 1.8V supply source.

(7) VDDSHV5 is designed to support power-up, power-down, or dynamic voltage change without any dependency on other power rails. This capability is required to support UHS-I SD Cards.

(8) VDD_CANUART shall be connected to the same power source as VDD_CORE and VDDA_CORE_USB when not using Partial IO low power mode.

VDD_CANUART, VDD_CORE, and VDDA_CORE_USB can be operated at 0.75V or 0.85V. When these supplies are operating at 0.75V, they shall be ramped up prior to VDDR_CORE as defined by this waveform.

(9) VDD_CANUART shall be connected to the same power source as VDD_CORE, and VDDA_CORE_USB when not using Partial IO low power mode.

VDD_CANUART, VDD_CORE, and VDDA_CORE_USB can be operated at 0.75V or 0.85V. When these supplies are operating at 0.85V, they shall be powered from the same source as VDDR_CORE and ramped during the 0.85V ramp period defined by this waveform.

(10) The potential applied to VDDR_CORE must never be greater than the potential applied to VDD_CORE + 0.18V during power-up or power-down. This requires VDD_CORE to ramp up before and ramp down after VDDR_CORE when VDD_CORE is operating at 0.75V. VDD_CORE does not have any ramp requirements beyond the one defined for VDDR_CORE.

VDD_CORE and VDDR_CORE are expected to be powered by the same source so they ramp together when VDD_CORE is operating at 0.85V.

(11) VPP is the 1.8V eFuse programming supply, which shall be left floating (HiZ) or grounded during power-up/down sequences and during normal device operation. This supply shall only be sourced while programming eFuse.

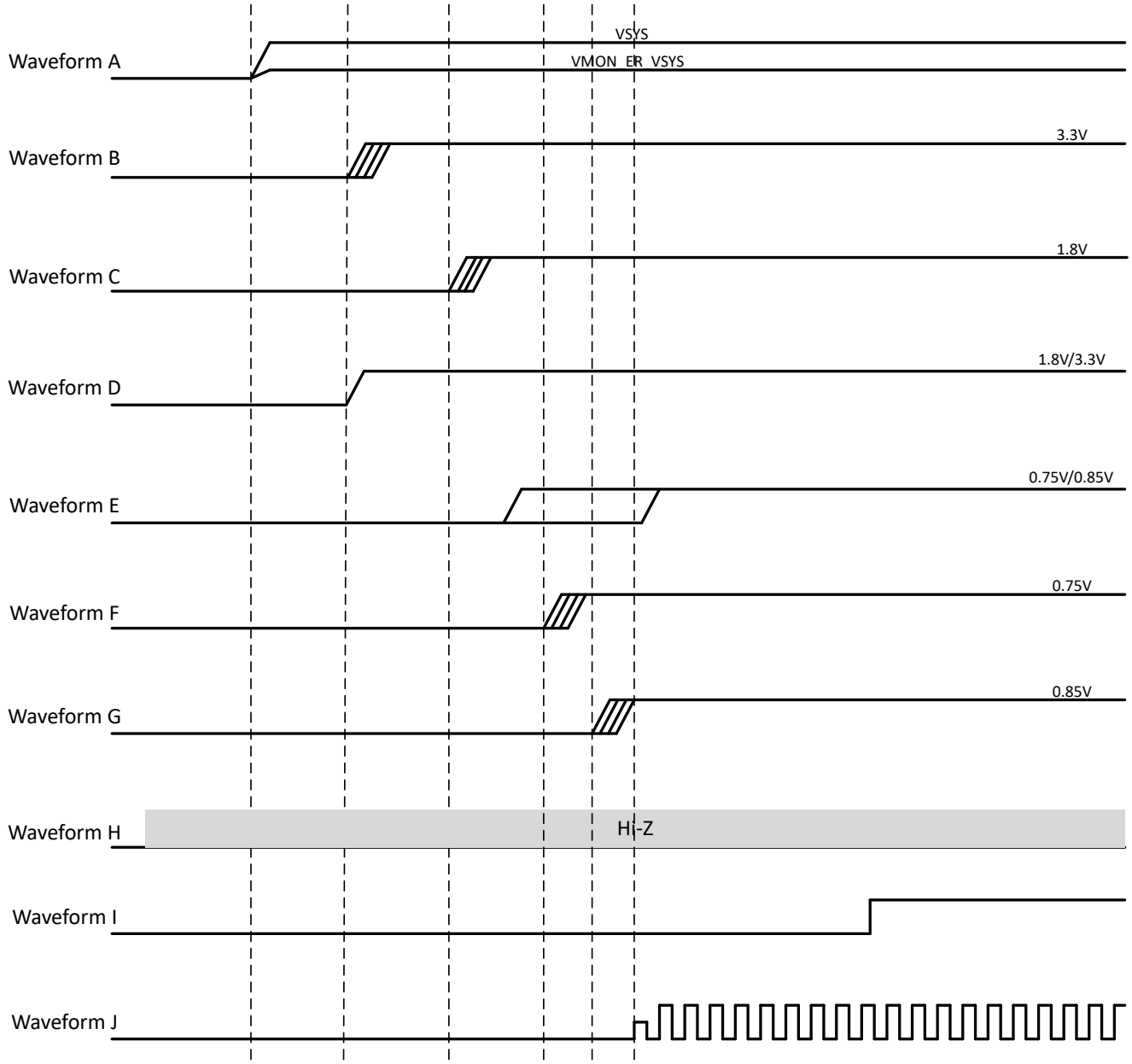


Figure 6-4. Power-Up Sequencing

6.12.2.2.2 Power-Up Sequencing with IO Retention

Power-Up Sequencing with IO Retention – Supply / Signal Assignments and Figure 6-5 describes the device power-up sequencing.

Table 6-3. Power-Up Sequencing with IO Retention – Supply / Signal Assignments

See: Figure 6-5

WAVEFORM	SUPPLY / SIGNAL NAME
A	VSYS(1), VMON_ER_VSYS(2)
B	VDDA_3P3_USB, VDDSHV_CANUART(3), VDDSHV_MCU(3), VDDSHV0(3), VDDSHV1(3), VDDSHV2(3), VDDSHV3(3), VMON_3P3_SOC(4)
C	VDDA_MCU, VDDA_PLL0, VDDA_PLL1, VDDA_PLL2, VDDA_1P8_USB, VDDA_ADC0, VDDA_TEMP0, VDDA_TEMP1, VDDSHV_CANUART(5), VDDSHV_MCU(5), VDDSHV0(5), VDDSHV1(5), VDDSHV2(5), VDDSHV3(5), VDDS_OSC0, VMON_1P8_SOC(6)
D	VDDSHV5(7)
E	VDD_CANUART(8)
F	VDDR_CANUART(9)
G	VDD_CORE(10) (12), VDDA_CORE_USB0(10)
H	VDD_CORE(11) (12), VDDA_CORE_USB0(11), VDDR_CORE(12)
I	VPP(13)
J	MCU_PORz
K	MCU_OSC0_XI, MCU_OSC0_XI

(1) VSYS represents the name of a supply which sources power to the entire system. This supply is expected to be a pre-regulated supply that sources power management devices which source all other supplies.

(2) VMON_ER_VSYS input is used to monitor VSYS via an external resistor divider circuit. For more information, see System Power Supply Monitor Design Guidelines.

(3) VDDSHV_CANUART, VDDSHV_MCU, and VDDSHVx [x=0-3] are dual voltage IO supplies which can be operated at 1.8V or 3.3V depending on the application requirements.

VDDSHV_CANUART shall be connected to an always-on power source when using Partial IO low power mode.

When any of the VDDSHV_MCU, VDDSHV_CANUART, and VDDSHVx [x=0-3] IO supplies are operating at 3.3V, they shall be ramped up with other 3.3V supplies during the 3.3V ramp period defined by this waveform.

(4) The VMON_3P3_SOC input is used to monitor supply voltage and shall be connected to the respective 3.3V supply source.

(5) VDDSHV_CANUART, VDDSHV_MCU, and VDDSHVx [x=0-3] are dual voltage IO supplies which can be operated at 1.8V or 3.3V depending on the application requirements.

VDDSHV_CANUART shall be connected to an always-on power source when using Partial IO low power mode.

When any of the VDDSHV_MCU, VDDSHV_CANUART, and VDDSHVx [x=0-3] IO supplies are operating at 1.8V, they shall be ramped up with other 1.8V supplies during the 1.8V ramp period defined by this waveform.

(6) The VMON_1P8_SOC input is used to monitor supply voltage and shall be connected to the respective 1.8V supply source.

(7) VDDSHV5 is designed to support power-up, power-down, or dynamic voltage change without any dependency on other power rails. This capability is required to support UHS-I SD Cards.

(8) VDD_CANUART can be operated at 0.75V or 0.85V. VDD_CANUART shall be connected to an always-on power source when using Partial IO low power mode.

When VDD_CANUART is connected to an always-on power source, the potential applied to VDD_CORE must never be greater than the potential applied to VDD_CANUART + 0.18V during power-up or power-down. This requires VDD_CANUART to ramp up before and ramp down after VDD_CORE. VDD_CANUART does not have any ramp requirements beyond the one defined for VDD_CORE.

(9) VDDR_CANUART must be operated at 0.85V. VDDR_CANUART can be tied to the same 0.85V supply as VDD_CANUART at the board level when VDD_CANUART is operated at 0.85V.

(10) VDD_CORE, and VDDA_CORE_USB can be operated at 0.75V or 0.85V. When these supplies are operating at 0.75V, they shall be ramped up prior to VDDR_CORE as defined by this waveform.

(11) VDD_CORE, and VDDA_CORE_USB can be operated at 0.75V or 0.85V. When these supplies are operating at 0.85V, they shall be powered from the same source as VDDR_CORE and ramped during the 0.85V ramp period defined by this waveform.

(12) The potential applied to VDDR_CORE must never be greater than the potential applied to VDD_CORE + 0.18V during power-up or power-down. This requires VDD_CORE to ramp up before and ramp down after VDDR_CORE when VDD_CORE is operating at 0.75V. VDD_CORE does not have any ramp requirements beyond the one defined for VDDR_CORE.

VDD_CORE and VDDR_CORE are expected to be powered by the same source so they ramp together when VDD_CORE is operating at 0.85V.

(13) VPP is the 1.8V eFuse programming supply, which shall be left floating (HiZ) or grounded during power-up/down sequences and during normal device operation. This supply shall only be sourced while programming eFuse.

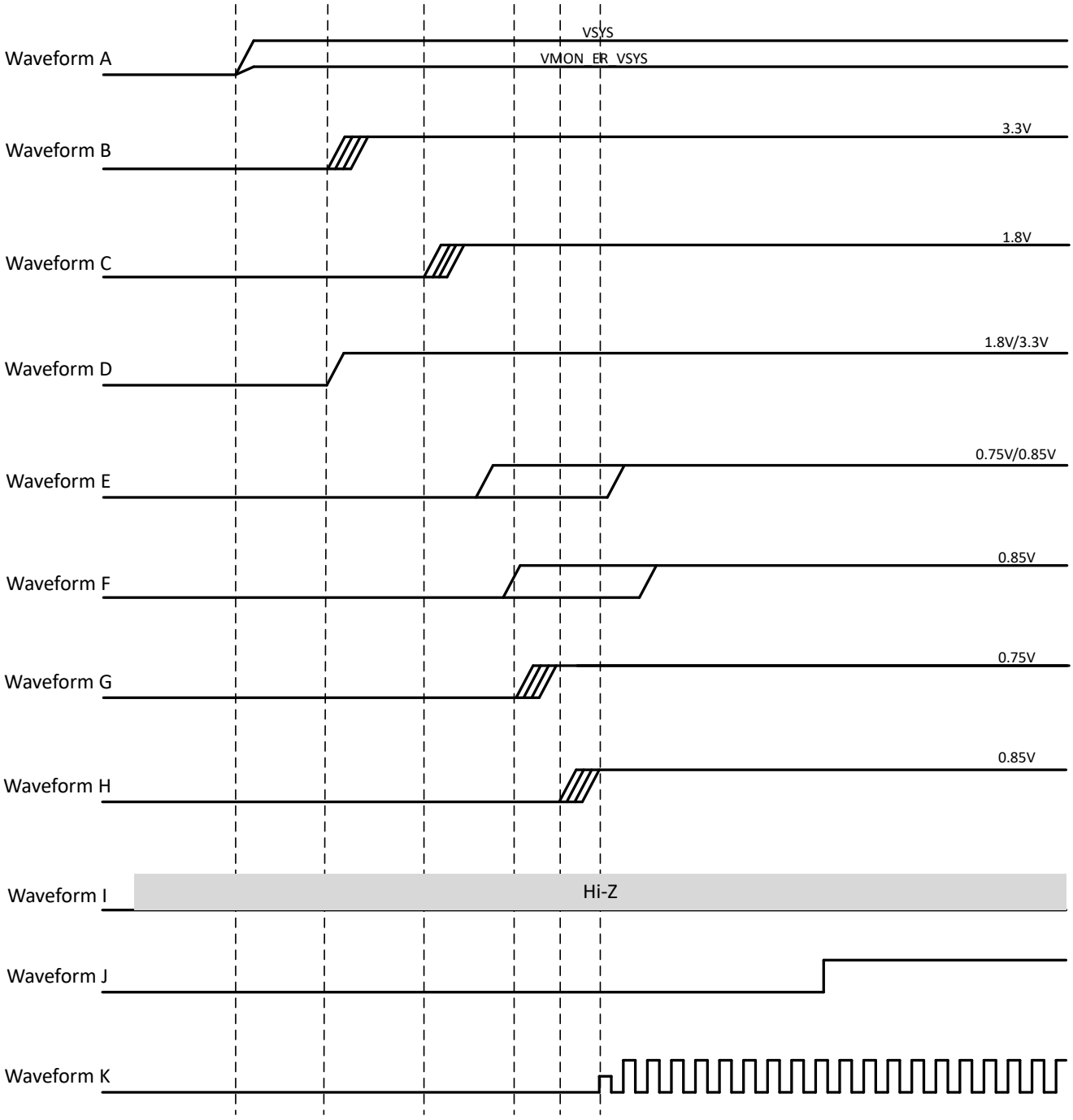


Figure 6-5. Power-Up Sequencing with IO Retention

6.12.2.2.3 Power-Up Sequencing - IO Retention Wakeup

Table 6-4 and Figure 6-6 describes the device power-up sequencing.

Table 6-4. Power-Up Sequencing - IO Retention Wakeup – Supply / Signal Assignments

See: Figure 6-6

WAVEFORM	SUPPLY / SIGNAL NAME
A	VSYS(1), VMON_ER_VSYS(2)
B	VDDA_3P3_USB, VDDSHV_MCU(3), VDDSHV0(3), VDDSHV1(3), VDDSHV2(3), VDDSHV3(3), VMON_3P3_SOC(4)
C	VDDA_MCU, VDDA_PLL0, VDDA_PLL1, VDDA_PLL2, VDDA_1P8_USB, VDDA_ADC0, VDDA_TEMP0, VDDA_TEMP1, VDDSHV_CANUART(5), VDDSHV_MCU(5), VDDSHV0(5), VDDSHV1(5), VDDSHV2(5), VDDSHV3(5), VDDS_OSC0, VMON_1P8_SOC(6)
D	VDDSHV_CANUART(7)
E	VDDSHV5(8)
F	VDD_CANUART(9)
G	VDD_CORE(10) (13), VDDA_CORE_USB0(10)
H	VDDR_CANUART(11)
I	VDD_CORE(12) (13), VDDA_CORE_USB0(12), VDDR_CORE(13)
J	VPP(14)
K	MCU_PORz
L	MCU_OSC0_XI, MCU_OSC0_XI

(1) VSYS represents the name of a supply which sources power to the entire system. This supply is expected to be a pre-regulated supply that sources power management devices which source all other supplies.

(2) VMON_ER_VSYS input is used to monitor VSYS via an external resistor divider circuit. For more information, see System Power Supply Monitor Design Guidelines.

(3) VDDSHV_MCU and VDDSHVx [x=0-3] are dual voltage IO supplies which can be operated at 1.8V or 3.3V depending on the application requirements.

When any of the VDDSHV_MCU and VDDSHVx [x=0-3] IO supplies are operating at 3.3V, they shall be ramped up with other 3.3V supplies during the 3.3V ramp period defined by this waveform.

(4) The VMON_3P3_SOC input is used to monitor supply voltage and shall be connected to the respective 3.3V supply source.

(5) VDDSHV_MCU and VDDSHVx [x=0-3] are dual voltage IO supplies which can be operated at 1.8V or 3.3V depending on the application requirements.

When any of the VDDSHV_MCU and VDDSHVx [x=0-3] IO supplies are operating at 1.8V, they shall be ramped up with other 1.8V supplies during the 1.8V ramp period defined by this waveform.

(6) The VMON_1P8_SOC input is used to monitor supply voltage and shall be connected to the respective 1.8V supply source.

(7) VDDSHV_CANUART can be operated at 1.8V or 3.3V. VDDSHV_CANUART shall be connected to an always-on power source when using Partial IO low power mode.

(8) VDDSHV5 is designed to support power-up, power-down, or dynamic voltage change without any dependency on other power rails. This capability is required to support UHS-I SD Cards.

(9) VDD_CANUART can be operated at 0.75V or 0.85V. VDD_CANUART shall be connected to an always-on power source when using Partial IO low power mode.

(10) VDD_CORE, and VDDA_CORE_USB can be operated at 0.75V or 0.85V. When these supplies are operating at 0.75V, they shall be ramped up prior to VDDR_CORE as defined by this waveform.

(11) VDDR_CANUART must be operated at 0.85V. VDD_CANUART shall be connected to an always-on power source when using Partial IO low power mode. VDDR_CANUART can be tied to the same 0.85V supply as VDD_CANUART at the board level when VDD_CANUART is operated at 0.85V.

(12) VDD_CORE, and VDDA_CORE_USB can be operated at 0.75V or 0.85V. When these supplies are operating at 0.85V, they shall be powered from the same source as VDDR_CORE and ramped during the 0.85V ramp period defined by this waveform.

(13) The potential applied to VDDR_CORE must never be greater than the potential applied to VDD_CORE + 0.18V during power-up or power-down. This requires VDD_CORE to ramp up before and ramp down after VDDR_CORE when VDD_CORE is operating at 0.75V. VDD_CORE does not have any ramp requirements beyond the one defined for VDDR_CORE.

VDD_CORE and VDDR_CORE are expected to be powered by the same source so they ramp together when VDD_CORE is operating at 0.85V.

(14) VPP is the 1.8V eFuse programming supply, which shall be left floating (HiZ) or grounded during power-up/down sequences and during normal device operation. This supply shall only be sourced while programming eFuse.

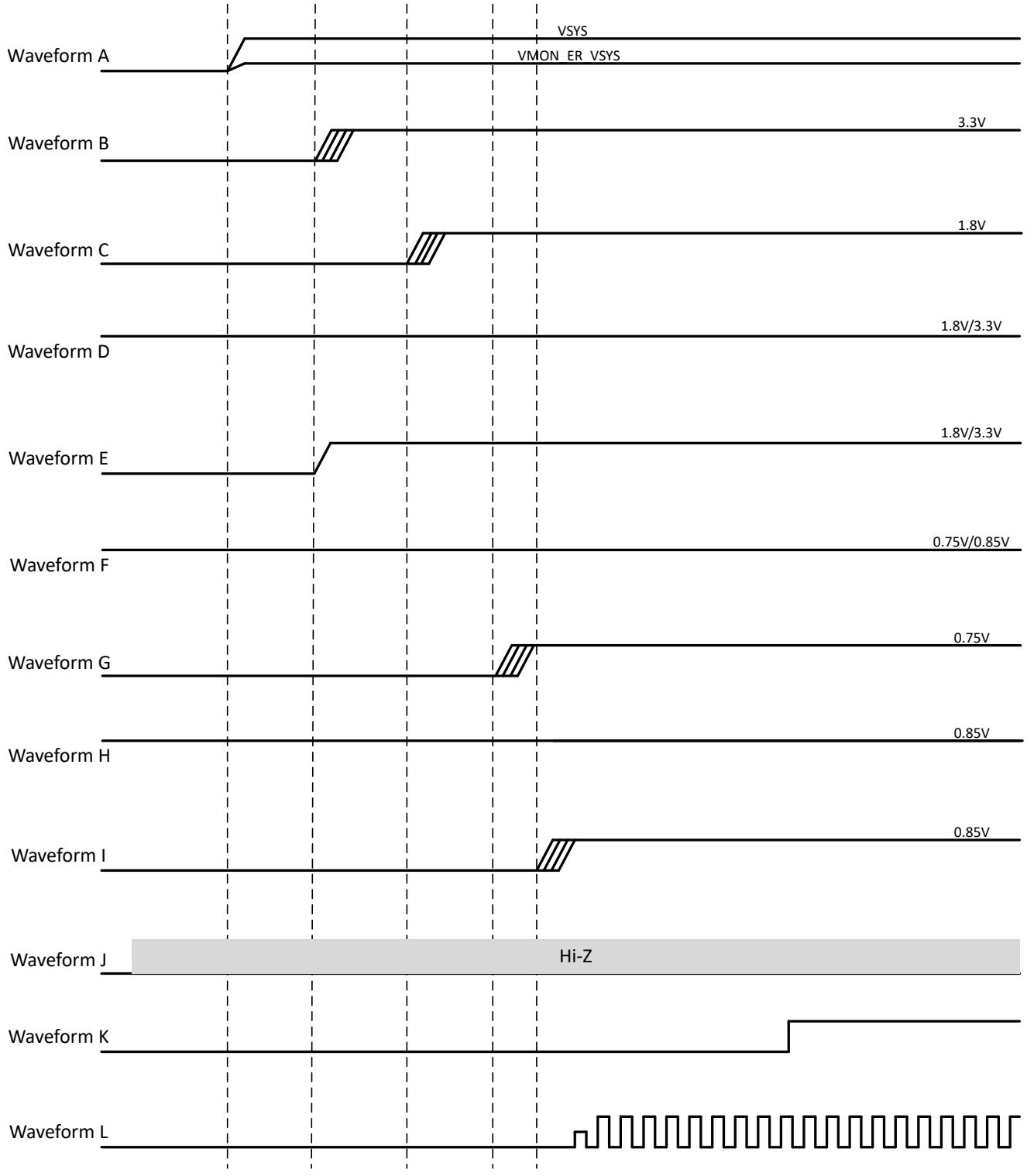


Figure 6-6. Power-Up Sequencing - IO Retention Wakeup

6.12.2.2.4 Power-Down Sequencing

Table 6-5 and Figure 6-7 describes the device power-down sequencing.

Note

The power supply sequencing requirements defined in this section does not include entry or exit from low power modes. See *Partial IO Power Sequencing* for more information on the requirements for entering or exiting from Partial IO low power mode.

Table 6-5. Power-Down Sequencing – Supply / Signal Assignments

See: Figure 6-7

WAVEFORM	SUPPLY / SIGNAL NAME
A	VSYS, VMON_VSYS
B	VDDSHV_CANUART(1), VDDSHV_MCU(1), VDDSHV0(1), VDDSHV1(1), VDDSHV2(1), VDDSHV3(1), VDDA_3P3_USB, VMON_3P3_SOC
C	VDDSHV_CANUART(2), VDDSHV_MCU(2), VDDSHV0(2), VDDSHV1(2), VDDSHV2(2), VDDSHV3(2), VDDS_MMC0, VDDA_MCU, VDDS_OSC0, VDDA_PLL0, VDDA_PLL1, VDDA_PLL2, VDDA_1P8_CSI_DSI, VDDA_1P8_OLDI0, VDDA_1P8_USB, VDDA_ADC0, VDDA_TEMP0, VDDA_TEMP1, VMON_1P8_SOC
D	VDDSHV5(3), VDDSHV6(3)
E	VDDS_DDR, VDDS_DDR_C
F	VDD_CANUART(4)
G	VDD_CANUART(5), VDD_CORE(5), VDDA_CORE_CSI_DSI(5), , VDDA_CORE_DSI_CLK(5), VDDA_CORE_USB0(5), VDDA_DDR_PLL0(5)
H	VDD_CANUART(6), VDD_CORE(6), VDDA_CORE_CSI_DSI(6), , VDDA_CORE_DSI_CLK(6), VDDA_CORE_USB0(6), VDDA_DDR_PLL0(6), VDDR_CORE, VDD_MMC0, VDDA_0P85_DLL_MMC0
I	VPP
J	MCU_PORz
K	MCU_OSC0_XI, MCU_OSC0_XI

(1) VDDSHV_CANUART, VDDSHV_MCU, and VDDSHVx [x=0-3] when operating at 3.3V.

(2) VDDSHV_CANUART, VDDSHV_MCU, and VDDSHVx [x=0-3] when operating at 1.8V.

(3) VDDSHV5, and VDDSHV6 were designed to support power-up, power-down, or dynamic voltage change without any dependency on other power rails. This capability is required to support UHS-I SD Cards.

(4) VDD_CANUART when connected to an always-on power source for Partial IO low power mode.

(5) VDD_CANUART, VDD_CORE, VDDA_CORE_CSI_DSI, VDDA_CORE_DSI_CLK, VDDA_CORE_USB0, and VDDA_DDR_PLL0 when operating at 0.75V

(6) VDD_CANUART, VDD_CORE, VDDA_CORE_CSI_DSI, VDDA_CORE_DSI_CLK, VDDA_CORE_USB0, and VDDA_DDR_PLL0 when operating at 0.85V

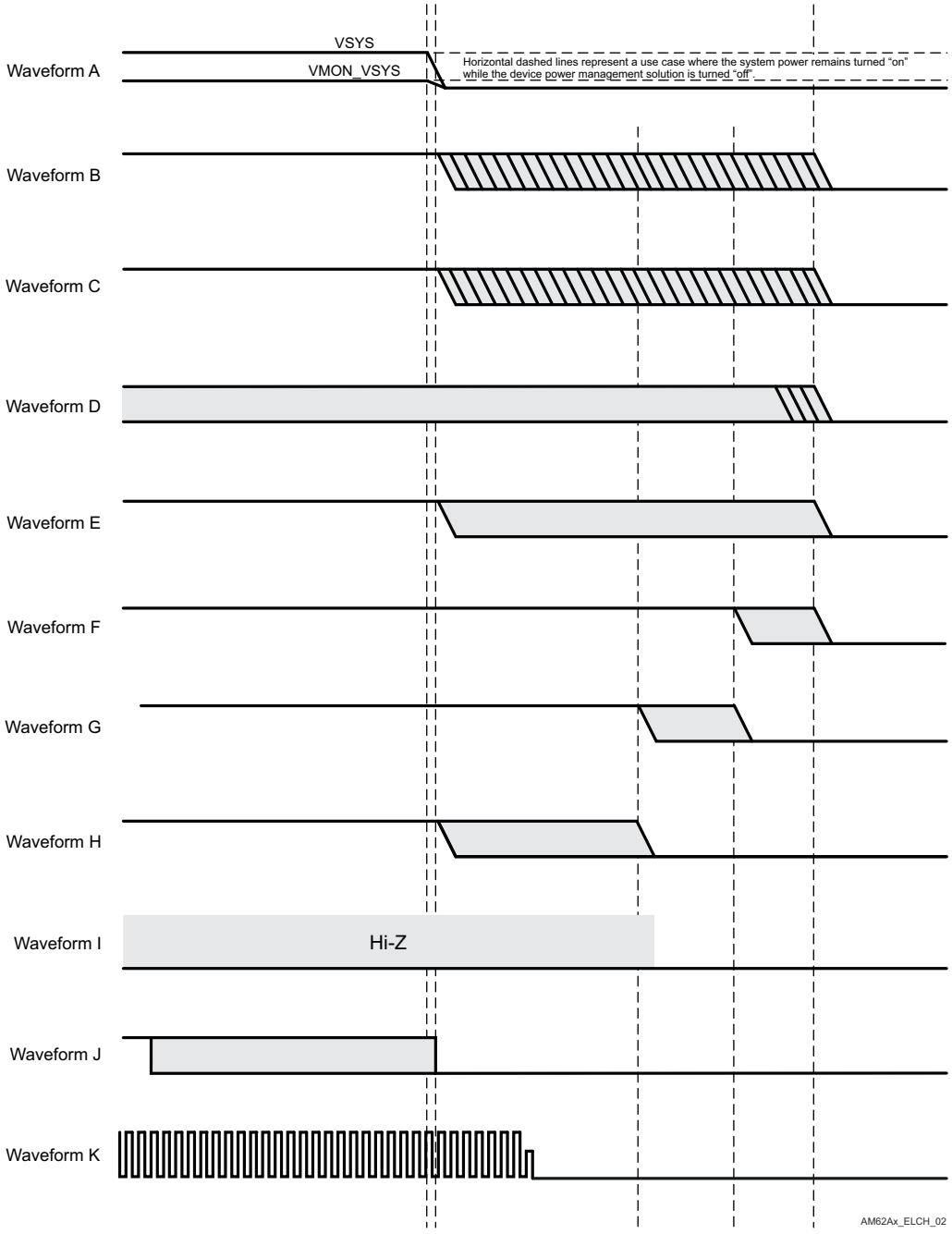


Figure 6-7. Power-Down Sequencing

6.12.3 System Timing

For more details about features and additional description information on the subsystem multiplexing signals, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

6.12.3.1 Reset Timing

Tables and figures provided in this section define timing conditions, timing requirements, and switching characteristics for reset related signals.

Reset Timing Conditions

PARAMETER			MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input Slew Rate	VDD(1) = 1.8V	0.0018		V/ns
		VDD(1) = 1.8V	0.0033		V/ns
OUTPUT CONDITIONS					
C_L	Output Load Capacitance		30		pF

(1) VDD stands for corresponding power supply. For more information on the power supply name and the corresponding ball(s), see POWER column of the *Pin Attributes* table.

MCU_PORz Timing Requirements

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
RST1	$t_{h(SUPPLIES\_VALID-MCU\_PORz)}$	Hold time, MCU_PORz active (low) at Power-up after supplies valid (using external crystal circuit)	9500000		ns
RST2		Hold time, MCU_PORz active (low) at Power-up after supplies valid (using external LVCMOS clock source)	1200		ns
RST3	$t_{w(PORzL)}$	Pulse Width, MCU_PORz low after Power-up (without removal of Power or system reference clock MCU_OSC0_XI/XO)	1200		ns

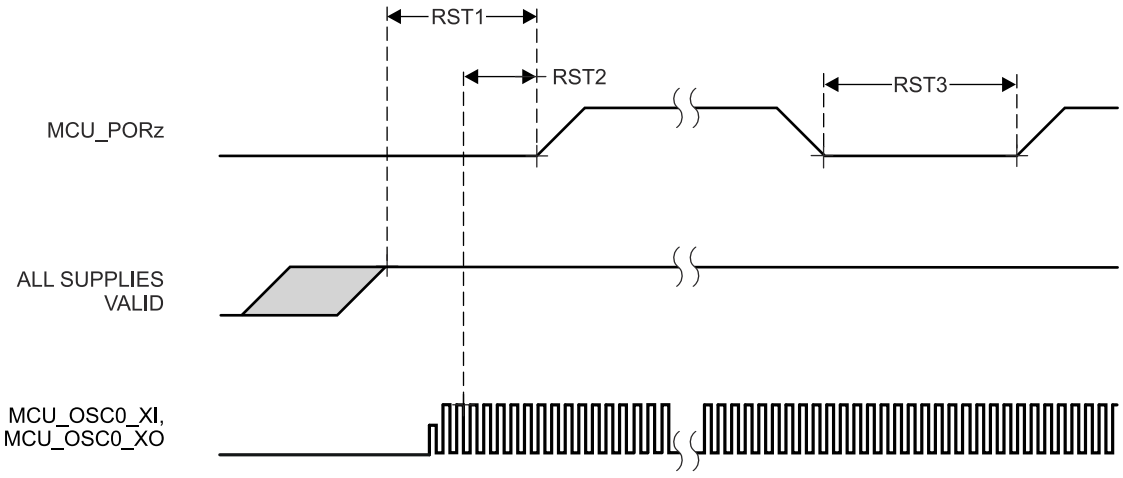


Figure 6-8. MCU_PORz Timing Requirements

RESETSTATz Switching Characteristics

NO.	PARAMETER		MIN	MAX	UNIT
RST6	$t_{d(MCU\_PORzL:-RESETSTATzL)}$	Delay time, MCU_PORz active (low) to RESETSTATz active (low)	0		ns

NO.	PARAMETER		MIN	MAX	UNIT
RST7	$t_{d(MCU\_PORzH-RESETSTATzH))}$	Delay time, MCU_PORz inactive (high) to RESETSTATz inactive (high)	9195 × S(1)		ns
RST9	$t_{w(RESETSTATzL)}$	Pulse Width, RESETSTATz low (SW_MCU_WARMRST, SW_MAIN_PORz, or SW_MAIN_WARMRST)	4040 × S(1)	6000000	ns

(1) S = MCU_OSC0_XI/XO clock period in ns.

MCU_RESETz Timing Requirements

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
RST10	$t_{w(MCU\_RESETzL)}$ (1)	Pulse Width minimum, MCU_RESETz active (low)	1200		ns

(1) This timing parameter is valid only after all supplies are valid and MCU_PORz has been asserted for the specified time.

RESETSTATz Switching Characteristics

NO.	PARAMETER		MIN	MAX	UNIT
RST13	$t_{d(MCU\_RESETzL:-RESETSTATzL)}$	Delay time, MCU_RESETz active (low) to RESETSTATz active (low)	960		ns
RST14	$t_{d(MCU\_RESETzH:-RESETSTATzH)}$	Delay time, MCU_RESETz inactive (high) to RESETSTATz inactive (high)	4040 × S(1)		ns

(1) S = MCU_OSC0_XI/XO clock period in ns.

EMUx Timing Requirements

NO.	PARAMETER		MIN	MAX	UNIT
RST18	$t_{su(EMUx-MCU\_PORz)}$	Setup time, EMU[1:0] before MCU_PORz inactive (high)	3 × S(1)		ns
RST19	$t_{h(MCU\_PORz-EMUx)}$	Hold time, EMU[1:0] after MCU_PORz inactive (high)	10		ns

(1) S = MCU_OSC0_XI/XO clock period in ns.

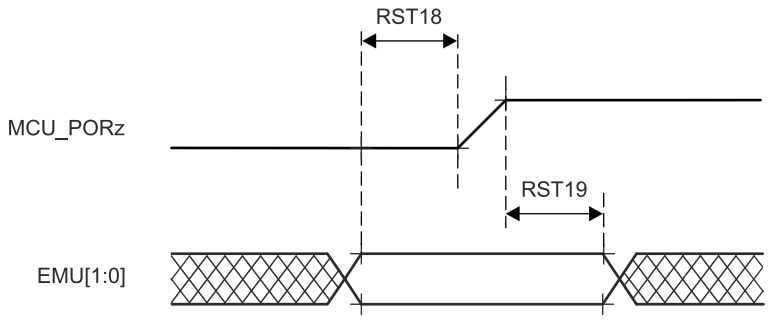


Figure 6-9. EMUx Timing Requirements

BOOTMODE Timing Requirements

NO.	PARAMETER		MIN	MAX	UNIT
RST23	$t_{sh(BOOTMODE-MCU\_PORz)}$	Setup time, BOOTMODE[15:0] before MCU_PORz high (Extneral MCU_PORz event or Software SW_MAIN_PORz)	3 × S(1)		ns

NO.	PARAMETER		MIN	MAX	UNIT
RST24	$t_{h(MCU\_PORz-BOOTMODE)}$	Hold time, BOOTMODE[15:0] after MCU_PORz high (Extneral MCU_PORz event or Software SW_MAIN_PORz)	0		ns

(1) S = MCU_OSC0_XI/XO clock period in ns.

6.12.3.2 Error Signal Timing

Tables and figures provided in this section define timing conditions and switching characteristics for MCU_ERRORn.

Error Signal Timing Conditions

PARAMETER		MIN	MAX	UNIT
OUTPUT CONDITIONS				
C_L	Output Load Capacitance		30	pF

MCU_ERRORn Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
ERR1	$t_{c(MCU\_ERRORn)}$	Cycle time minimum, MCU_ERRORn (PWM mode enabled)	$(P^{(1)} \times H^{(3)}) + (P^{(1)} \times L)^{(4)}$		ns
ERR2	$t_{w(MCU\_ERRORn)}$	Pulse width minimum, MCU_ERRORn active (PWM mode disabled)(5)	$P^{(1)} \times R^{(2)}$		ns
ERR3	$t_{d(ERROR\_CONDITION-MCU\_ERRORnL)}$	Delay time, ERROR_CONDITION to MCU_ERRORn active(5)	$50 \times P^{(1)}$		ns

(1) P = ESM functional clock
(2) R = Error Pin Counter Pre-Load Register count value
(3) H = Error Pin PWM High Pre-Load Register count value
(4) L = Error Pin PWM Low Pre-Load Register count value
(5) When PWM mode is enabled, SAFETY_ERRORn stops toggling after ERR3 and will maintain its value (either high or low) until the error is cleared. When PWM mode is disabled, MCU_ERRORn is active low.

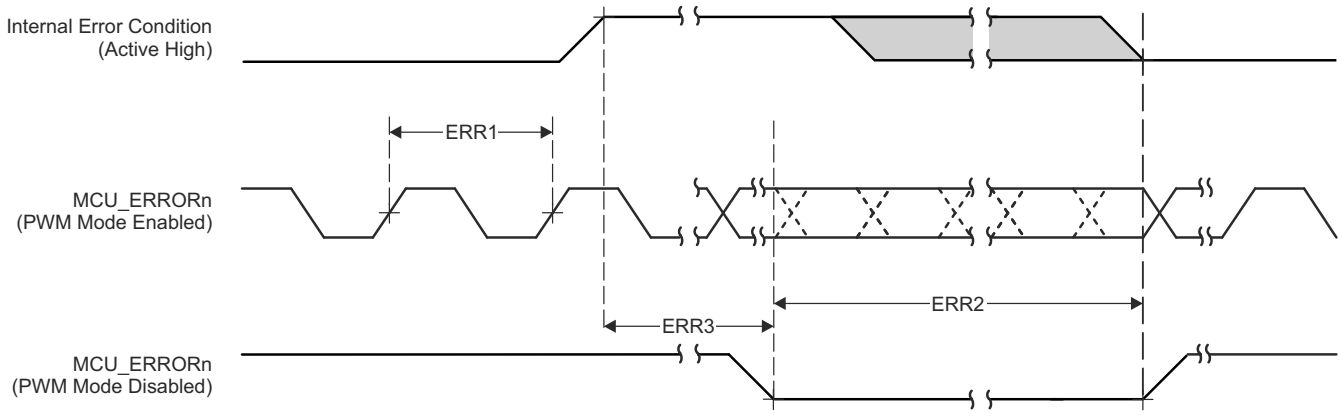


Figure 6-10. MCU_ERRORn Timing Requirements and Switching Characteristics

6.12.3.3 Clock Timing

Tables and figures provided in this section define timing conditions, timing requirements, and switching characteristics for clock signals.

Clock Timing Conditions

PARAMETER			MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input Slew Rate		0.5		V/ns
OUTPUT CONDITIONS					
C_L	Output Load Capacitance	5 ns ≤ t_c ≤ 8 ns		5	pF
		8 ns ≤ t_c ≤ 20 ns		10	pF
		20 ns ≤ t_c		30	pF

Clock Timing Requirements

NO.	PARAMETER		MIN	MAX	UNIT
CLK1	$t_{c(EXT\_REFCLK1)}$	Cycle time minimum, EXT_REFCLK1	10		ns
CLK2	$t_{w(EXT\_REFCLKH1)}$	Pulse Duration minimum, EXT_REFCLK1 high	E(1) × 0.45	E(1) × 0.55	ns
CLK3	$t_{w(EXT\_REFCLKL1)}$	Pulse Duration minimum, EXT_REFCLK1 low	E(1) × 0.45	E(1) × 0.55	ns
CLK1	$t_{c(MCU\_EXT\_REFCLK0)}$	Cycle time minimum, MCU_EXT_REFCLK0	10		ns
CLK2	$t_{w(MCU\_EXT\_REFCLK0H)}$	Pulse Duration minimum, MCU_EXT_REFCLK0 high	F(2) × 0.45	F(2) × 0.55	ns
CLK3	$t_{w(MCU\_EXT\_REFCLK0L)}$	Pulse Duration minimum, MCU_EXT_REFCLK0 low	F(2) × 0.45	F(2) × 0.55	ns
CLK1	$t_{c(AUDIO\_EXT\_REFCLK0)}$	Cycle time minimum, AUDIO_EXT_REFCLK0	20		ns
CLK2	$t_{w(AUDIO\_EXT\_REFCLK0H)}$	Pulse Duration minimum, AUDIO_EXT_REFCLK0 high	G(3) × 0.45	G(3) × 0.55	ns
CLK3	$t_{w(AUDIO\_EXT\_REFCLK0L)}$	Pulse Duration minimum, AUDIO_EXT_REFCLK0 low	G(3) × 0.45	G(3) × 0.55	ns
CLK1	$t_{c(AUDIO\_EXT\_REFCLK1)}$	Cycle time minimum, AUDIO_EXT_REFCLK1	20		ns
CLK2	$t_{w(AUDIO\_EXT\_REFCLK1H)}$	Pulse Duration minimum, AUDIO_EXT_REFCLK1 high	H(4) × 0.45	H(4) × 0.55	ns
CLK3	$t_{w(AUDIO\_EXT\_REFCLK1L)}$	Pulse Duration minimum, AUDIO_EXT_REFCLK1 low	H(4) × 0.45	H(4) × 0.55	ns
CLK1	$t_{c(AUDIO\_EXT\_REFCLK2)}$	Cycle time minimum, AUDIO_EXT_REFCLK2	20		ns
CLK2	$t_{w(AUDIO\_EXT\_REFCLK2H)}$	Pulse Duration minimum, AUDIO_EXT_REFCLK2 high	I(5) × 0.45	I(5) × 0.55	ns
CLK3	$t_{w(AUDIO\_EXT\_REFCLK2L)}$	Pulse Duration minimum, AUDIO_EXT_REFCLK2 low	I(5) × 0.45	I(5) × 0.55	ns

(1) E = EXT_REFCLK cycle time in ns.
(2) F = MCU_EXT_REFCLK0 cycle time in ns.
(3) G = AUDIO_EXT_REFCLK0 cycle time in ns.
(4) H = AUDIO_EXT_REFCLK1 cycle time in ns.
(5) I = AUDIO_EXT_REFCLK2 cycle time in ns.

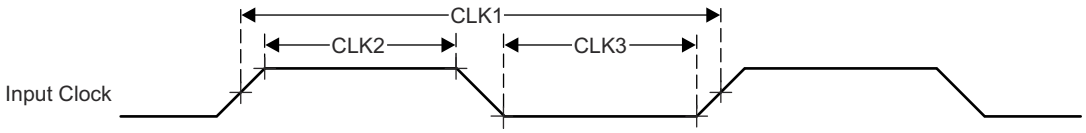


Figure 6-11. Clock Timing Requirements

Clock Switching Characteristics

NO.	PARAMETER		MIN	MAX	UNIT
CLK4	$t_{c(SYSCLKOUT0)}$	Cycle time minimum, SYSCLKOUT0	8		ns
CLK5	$t_{w(SYSCLKOUT0H)}$	Pulse Duration minimum, SYSCLKOUT0 high	A(1) × 0.4	A(1) × 0.6	ns
CLK6	$t_{w(SYSCLKOUT0L)}$	Pulse Duration minimum, SYSCLKOUT0 low	A(1) × 0.4	A(1) × 0.6	ns
CLK4	$t_{c(OBSCLK0)}$	Cycle time minimum, OBSCLK0	5		ns
CLK5	$t_{w(OBSCLK0H)}$	Pulse Duration minimum, OBSCLK0 high	B(2) × 0.45	B(2) × 0.55	ns
CLK6	$t_{w(OBSCLK0L)}$	Pulse Duration minimum, OBSCLK0 low	B(2) × 0.45	B(2) × 0.55	ns
CLK4	$t_{c(OBSCLK1)}$	Cycle time minimum, OBSCLK1	5		ns
CLK5	$t_{w(OBSCLK1H)}$	Pulse Duration minimum, OBSCLK1 high	F(3) × 0.45	F(3) × 0.55	ns
CLK6	$t_{w(OBSCLK1L)}$	Pulse Duration minimum, OBSCLK1 low	F(3) × 0.45	F(3) × 0.55	ns
CLK4	$t_{c(CLKOUT0)}$	Cycle time minimum, CLKOUT0	20		ns
CLK5	$t_{w(CLKOUT0H)}$	Pulse Duration minimum, CLKOUT0 high	C(4) × 0.4	C(4) × 0.6	ns
CLK6	$t_{w(CLKOUT0L)}$	Pulse Duration minimum, CLKOUT0 low	C(4) × 0.4	C(4) × 0.6	ns
CLK4	$t_{c(MCU\_SYSCLKOUT0)}$	Cycle time minimum, MCU_SYSCLKOUT0	10		ns
CLK5	$t_{w(MCU\_SYSCLKOUT0H)}$	Pulse Duration minimum, MCU_SYSCLKOUT0 high	E(5) × 0.4	E(5) × 0.6	ns
CLK6	$t_{w(MCU\_SYSCLKOUT0L)}$	Pulse Duration minimum, MCU_SYSCLKOUT0 low	E(5) × 0.4	E(5) × 0.6	ns
CLK4	$t_{c(MCU\_OBSCLK0)}$	Cycle time minimum, MCU_OBSCLK0	5		ns
CLK5	$t_{w(MCU\_OBSCLK0H)}$	Pulse Duration minimum, MCU_OBSCLK0 high	D(6) × 0.45	D(6) × 0.55	ns
CLK6	$t_{w(MCU\_OBSCLK0L)}$	Pulse Duration minimum, MCU_OBSCLK0 low	D(6) × 0.45	D(6) × 0.55	ns
CLK4	$t_{c(WKUP\_CLKOUT0)}$	Cycle time minimum, WKUP_CLKOUT0	5		ns
CLK5	$t_{w(WKUP\_CLKOUT0H)}$	Pulse Duration minimum, WKUP_CLKOUT0 high	W(7) × 0.4	W(7) × 0.6	ns
CLK6	$t_{w(WKUP\_CLKOUT0L)}$	Pulse Duration minimum, WKUP_CLKOUT0 low	W(7) × 0.4	W(7) × 0.6	ns
CLK4	$t_{c(AUDIO\_EXT\_REFCLK0)}$	Cycle time minimum, AUDIO_EXT_REFCLK0 (McASPClock Source)	20		ns
		Cycle time minimum, AUDIO_EXT_REFCLK0 (PLL Clock Source)	10		ns
CLK5	$t_{w(AUDIO\_EXT\_REFCLK0H)}$	Pulse Duration minimum, AUDIO_EXT_REFCLK0 high	G(8) × 0.4	G(8) × 0.6	ns
CLK6	$t_{w(AUDIO\_EXT\_REFCLK0L)}$	Pulse Duration minimum, AUDIO_EXT_REFCLK0 low	G(8) × 0.4	G(8) × 0.6	ns
CLK4	$t_{c(AUDIO\_EXT\_REFCLK1)}$	Cycle time minimum, AUDIO_EXT_REFCLK1 (McASPClock Source)	20		ns
		Cycle time minimum, AUDIO_EXT_REFCLK1 (PLL Clock Source)	10		ns
CLK5	$t_{w(AUDIO\_EXT\_REFCLK1H)}$	Pulse Duration minimum, AUDIO_EXT_REFCLK1 high	J(9) × 0.4	J(9) × 0.6	ns
CLK6	$t_{w(AUDIO\_EXT\_REFCLK1L)}$	Pulse Duration minimum, AUDIO_EXT_REFCLK1 low	J(9) × 0.4	J(9) × 0.6	ns

NO.	PARAMETER		MIN	MAX	UNIT
CLK4	$t_{c(AUDIO\_EXT\_REFCLK2)}$	Cycle time minimum, AUDIO_EXT_REFCLK2 (McASPClock Source)	20		ns
		Cycle time minimum, AUDIO_EXT_REFCLK2 (PLL Clock Source)	10		ns
CLK5	$t_{w(AUDIO\_EXT\_REFCLK2H)}$	Pulse Duration minimum, AUDIO_EXT_REFCLK2 high	K(10) × 0.4	K(10) × 0.6	ns
CLK6	$t_{w(AUDIO\_EXT\_REFCLK2L)}$	Pulse Duration minimum, AUDIO_EXT_REFCLK2 low	K(10) × 0.4	K(10) × 0.6	ns

(1) A = SYSCLKOUT0 cycle time in ns.
(2) B = OBSCLK0 cycle time in ns.
(3) F = OBSCLK1 cycle time in ns.
(4) C = CLKOUT0 cycle time in ns.
(5) E = MCU_SYSCLKOUT0 cycle time in ns.
(6) D = MCU_OBSCLK0 cycle time in ns.
(7) W = WKUP_CLKOUT0 cycle time in ns.
(8) G = AUDIO_EXT_REFCLK0 cycle time in ns.
(9) J = AUDIO_EXT_REFCLK1 cycle time in ns.
(10) K = AUDIO_EXT_REFCLK2 cycle time in ns.

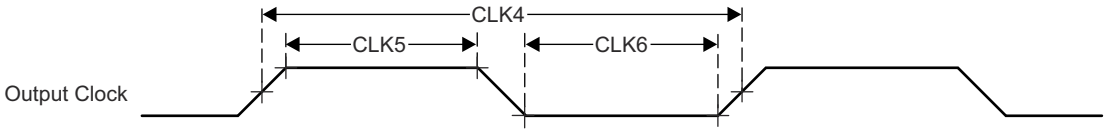


Figure 6-12. Clock Switching Characteristics

6.12.4 Clock Specifications

6.12.4.1 Input Clocks / Oscillators

Various external clock inputs/outputs are needed to drive the device. Summary of these input clock signals is as follows:

- MCU_OSC0_XO/MCU_OSC0_XI — external main crystal interface pins connected to the internal high-frequency oscillator (HFOSC0), which is the default clock source for internal reference clock HFOSC0_CLKOUT.
- OSC1_XO/OSC1_XI — external main crystal interface pins connected to the internal high-frequency oscillator (HFOSC1), which is the default clock source for internal reference clock HFOSC1_CLKOUT. OSC1 is used as the source for the audio bit clocks and should be 24.576MHz.
- WKUP_LFOSC0_XO/WKUP_LFOSC0_XI — external crystal interface pins connected to internal low-frequency oscillator (WKUP_LFOSC0), which sources optional 32768 Hz reference clock.
- General purpose clock inputs
  - MCU_EXT_REFCLK0 — optional external system clock.
  - EXT_REFCLK1 — optional external system clock, can be used as a McASP high-frequency input clock when configured to operate as an input.
- External audio reference clock inputs/outputs
  - AUDIO_EXT_REFCLK[2:0] — optional McASP high-frequency input clocks when configured to operate as an input.

For more information about Input clock interfaces, see *Clocking* section in *Device Configuration* chapter in the device TRM.

6.12.4.1.1 MCU_OSC0 and OSC1 Internal Oscillator Clock Source

Figure 6-13 shows the recommended crystal circuit. All discrete components used to implement the oscillator circuit must be placed as close as possible to the MCU_OSC0_XI and MCU_OSC0_XO pins.

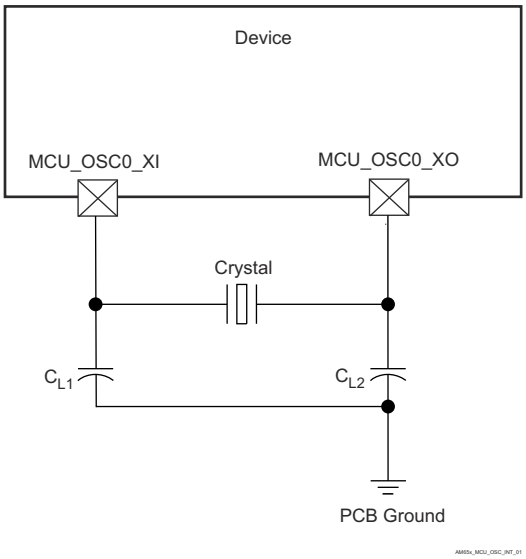


Figure 6-13. MCU_OSC0 Crystal Implementation

The crystal must be in the fundamental mode of operation and parallel resonant. HFOSC (MCU_OSC0 and OSC1) Crystal Circuit Requirements summarizes the required electrical constraints.

When selecting a crystal, the system design must consider temperature and aging characteristics of the crystal based on worst case environment and expected life expectancy of the system.

HFOSC (MCU_OSC0 and OSC1) Switching Characteristics - Crystal Mode details the switching characteristics of the oscillator.

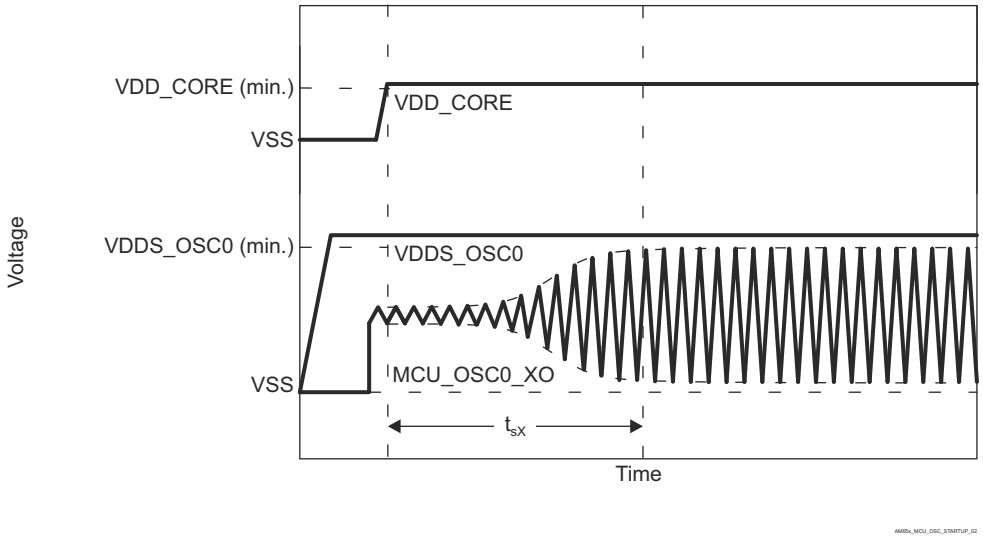


Figure 6-14. MCU_OSC0 Start-up Time

6.12.4.1.1.1 HFOSC (MCU_OSC0 and OSC1) Crystal Circuit Requirements

NAME	PARAMETER			MIN	TYP	MAX	UNIT
F_{xtal}	Crystal Parallel Resonance Frequency		MCU_OSC0		25		MHz
			OSC1		24.576		MHz
F_{xtal}	Crystal Frequency Stability and Tolerance		Ethernet RGMII and RMII not used			±100	ppm
			Ethernet RGMII and RMII using derived clock			±50	ppm
$C_{L1+PCBXI}$	Capacitance of C_{L1} + C_{PCBXI}			12		24	pF
$C_{L2+PCBXO}$	Capacitance of C_{L2} + C_{PCBXO}			12		24	pF
C_L	Crystal Load Capacitance			6		12	
C_{shunt}	Crystal Circuit Shunt Capacitance	ESR_{xtal} = 30 Ω	25 MHz			7	pF
		ESR_{xtal} = 40 Ω	25 MHz			5	pF
		ESR_{xtal} = 50 Ω	25 MHz			5	pF
ESR_{xtal}	Crystal Effective Series Resistance					(1)	Ω

(1) The maximum ESR of the crystal is a function of the crystal frequency and shunt capacitance. See the C_{shunt} parameter.

6.12.4.1.1.2 HFOSC (MCU_OSC0 and OSC1) Switching Characteristics - Crystal Mode

NAME	PARAMETER	MIN	TYP	MAX	UNIT
C_{XI}	XI Capacitance			1.58	pF
C_{XO}	XO Capacitance			1.49	pF
C_{XIXO}	XI to XO Mutual Capacitance			0.01	pF
t_s	Start-up Time		4		ms

6.12.4.1.1.3 Load Capacitance

The crystal circuit must be designed to apply the appropriate capacitive load to the crystal, as defined by the crystal manufacturer. The capacitive load, C_L, of this circuit is a combination of discrete capacitors C_{L1}, C_{L2}, and several parasitic contributions. PCB signal traces which connect crystal circuit components to MCU_OSC0_XI and MCU_OSC0_XO have parasitic capacitance to ground, C_{PCBXI} and C_{PCBXO}, where the PCB designer can extract parasitic capacitance for each signal trace. The MCU_OSC0 circuits and device package have combined parasitic capacitance to ground, C_{PCBXI} and C_{PCBXO}, where these parasitic capacitance values are defined in HFOSC (MCU_OSC0 and OSC1) Switching Characteristics - Crystal Mode.

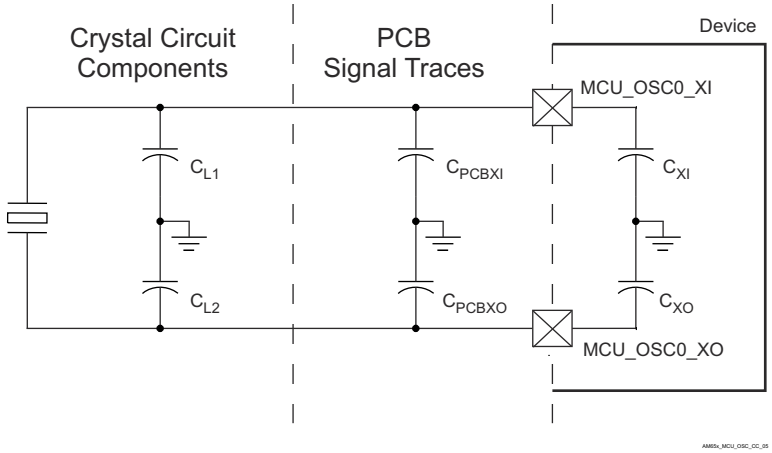


Figure 6-15. Load Capacitance

Load capacitors, C_{L1} and C_{L2} in Figure 6-13, can be chosen such that the below equation is satisfied. C_L in the equation is the load specified by the crystal manufacturer.

$C_L = [(C_{L1} + C_{PCBXI} + C_{XI}) \times (C_{L2} + C_{PCBXO} + C_{XO})] / [(C_{L1} + C_{PCBXI} + C_{XI}) + (C_{L2} + C_{PCBXO} + C_{XO})]$

To determine the value of C_{L1} and C_{L2}, multiply the capacitive load value C_L by 2. Using this result, subtract the combined values of C_{PCBXI} + C_{XI} to determine the value of C_{L1} and the combined values of C_{PCBXO} + C_{XO} to determine the value of C_{L2}. For example, if C_L = 10 pF, C_{PCBXI} = 2.9 pF, C_{XI} = 0.5 pF, C_{PCBXO} = 3.7 pF, C_{XO} = 0.5 pF, the value of $C_{L1} = [(2C_L) - (C_{PCBXI} + C_{XI})] = [(2 \times 10\text{ pF}) - 2.9\text{ pF} - 0.5\text{ pF})] = 16.6$ pF and $C_{L2} = [(2C_L) - (C_{PCBXO} + C_{XO})] = [(2 \times 10\text{ pF}) - 3.7\text{ pF} - 0.5\text{ pF})] = 15.8$ pF

6.12.4.1.1.4 Shunt Capacitance

The crystal circuit must also be designed such that it does not exceed the maximum shunt capacitance for MCU_OSC0 operating conditions defined in HFOSC (MCU_OSC0 and OSC1) Crystal Circuit Requirements. Shunt capacitance, C_{shunt}, of the crystal circuit is a combination of crystal shunt capacitance and parasitic contributions. PCB signal traces which connect crystal circuit components to MCU_OSC0 have mutual parasitic capacitance to each other, $C_{PCBXIXO}$, where the PCB designer should be able to extract mutual parasitic capacitance between these signal traces. The device package also has mutual parasitic capacitance, C_{XIXO}, where this mutual parasitic capacitance value is defined in HFOSC (MCU_OSC0 and OSC1) Switching Characteristics - Crystal Mode.

PCB routing should be designed to minimize mutual capacitance between XI and XO signal traces. This is typically done by keeping signal traces short and not routing them in close proximity. Mutual capacitance can also be minimized by placing a ground trace between these signals when the layout requires them to be routed in close proximity. It is important to minimize the mutual capacitance on the PCB to provide as much margin as possible when selecting a crystal.

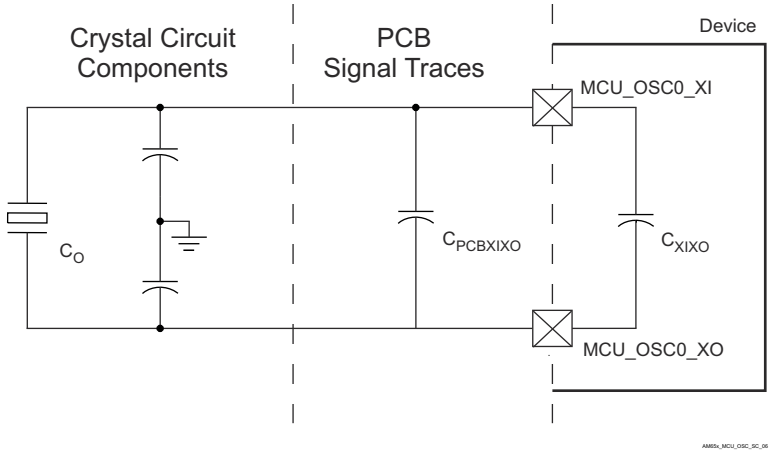


Figure 6-16. Shunt Capacitance

A crystal should be chosen such that the below equation is satisfied. C_O in the equation is the maximum shunt capacitance specified by the crystal manufacturer.

$C_{shunt} \geq C_O + C_{PCBXIXO} + C_{XIXO}$

For example, the equation would be satisfied when the crystal being used is 25 MHz with an ESR = 30 Ω, $C_{PCBXIXO}$ = 0.04 pF, C_{XIXO} = 0.01 pF, and shunt capacitance of the crystal is less than or equal to 6.95 pF.

6.12.4.1.2 MCU_OSC0 and OSC1 LVCMOS Digital Clock Source

Figure 6-17 shows the recommended oscillator connections when MCU_OSC0_XI or OSC1_XI is connected to a 1.8-V LVCMOS square-wave digital clock source.

Note

A DC steady-state condition is not allowed on MCU_OSC0_XI or OSC1_XI when the oscillator is powered up. This is not allowed because MCU_OSC0_XI and OSC1_XI are internally AC coupled to a comparator that can enter an unknown state when DC is applied to the input. Therefore, application software must power down MCU_OSC0 or OSC1 any time MCU_OSC0_XI or OSC1_XI is not toggling between logic states.

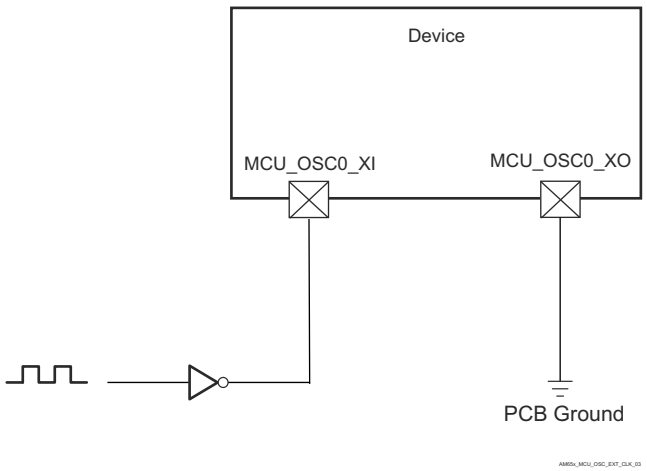


Figure 6-17. 1.8-V LVCMOS-Compatible Clock Input

6.12.4.1.3 WKUP_LFOSC0 Internal Oscillator Clock Source

Figure 6-18 shows the recommended crystal circuit. It is recommended that preproduction printed-circuit board (PCB) designs include the two optional resistors R_{bias} and R_d in case they are required for proper oscillator operation when combined with production crystal circuit components. In most cases, R_{bias} is not required and R_d is a 0-Ω resistor. These resistors may be removed from production PCB designs after evaluating oscillator performance with production crystal circuit components installed on preproduction PCBs.

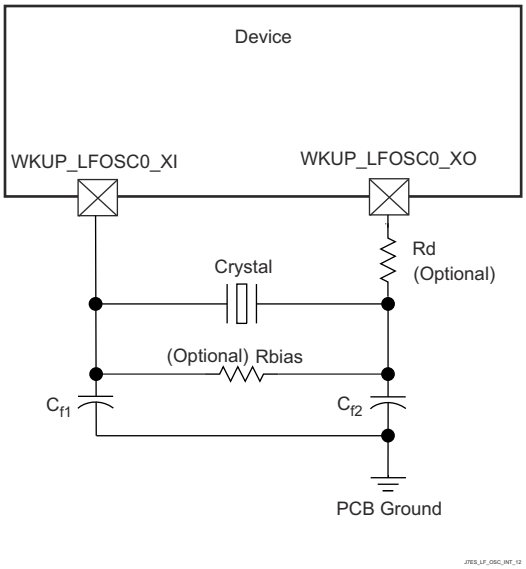


Figure 6-18. WKUP_LFOSC0 Crystal Implementation

Table 6-6 presents LFXOSC modes of operation.

Table 6-6. LFXOSC Modes of Operation

MODE	BP_C	PD_C	XI	XO	CLK_OUT	DESCRIPTION
ACTIVE	0	0	XTAL	XTAL	CLK_OUT	Active oscillator mode providing 32kHz
PWRDN	0	1	X	PD	LOW	Output will be pulled down to LOW. PAD to be tri-stated. Active mode disabled
BYPASS	1	0	CLK	PD	CLK	XI is driven by external clock source. XO is pulled down to LOW. Due to ESD diode to supply, XI should not be driven unless oscillator supply is present.

Note

User should set CTRLMMR_WKUP_LFXOSC_TRIM[18:16] i_mult = 3b'001 for CL in the range 6pf to 9.5pf. CTRLMMR_WKUP_LFXOSC_TRIM [18:16] i_mult = 3b'010 for CL in the range 8.5pf to 12pf. Default setting is 3b'010.

Note

The load capacitors, C_{f1} and C_{f2} in Figure 6-19, should be chosen such that the below equation is satisfied. C_L in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator WKUP_LFOSC0_XI, WKUP_LFOSC0_XO, and VSS pins.

$$C_L = \frac{C_{f1} C_{f2}}{(C_{f1} + C_{f2})}$$

Figure 6-19. Load Capacitance Equation

The crystal must be in the fundamental mode of operation and parallel resonant. LFOSC (WKUP_LFOSC0) Crystal Circuit Requirements summarizes the required electrical constraints.

When selecting a crystal, the system design must consider the temperature and aging characteristics of a based on the worst case environment and expected life expectancy of the system.

LFOSC (WKUP_LFOSC0) Switching Characteristics - Crystal Mode details the switching characteristics of the oscillator and the requirements of the input clock.

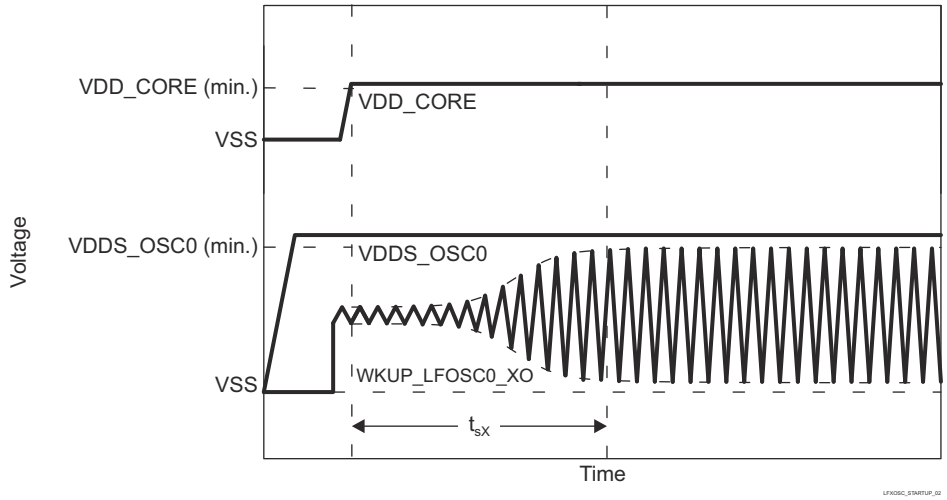


Figure 6-20. WKUP_LFOSC0 Start-up Time

6.12.4.1.3.1 LFOSC (WKUP_LFOSC0) Crystal Circuit Requirements

NAME	PARAMETER		MIN	TYP	MAX	UNIT
f_p	Parallel resonance crystal frequency			32768		Hz
	Crystal Frequency Stability and Tolerance				100	ppm
C_{f1}	C_{f1} load capacitance for crystal parallel resonance with $C_{f1} = C_{f2}$		12		24	pF
C_{f2}	C_{f2} load capacitance for crystal parallel resonance with $C_{f1} = C_{f2}$		12		24	pF
C_{shunt}	Crystal Circuit Shunt Capacitance	ESR_{xtal} = 40 Ω			4	pF
		ESR_{xtal} = 60 Ω			3	pF
		ESR_{xtal} = 80 Ω			2	pF
		ESR_{xtal} = 100 Ω			1	pF
ESR_{xtal}	Crystal Effective Series Resistance				(1)	Ω

(1) The maximum ESR of the crystal is a function of the crystal frequency and shunt capacitance. See the C_{shunt} parameter.

6.12.4.1.3.2 LFOSC (WKUP_LFOSC0) Switching Characteristics - Crystal Mode

NAME	PARAMETER	MIN	TYP	MAX	UNIT
f_{xtal}	Oscillation frequency		32768		Hz
t_{sX}	Start-up Time			96.5	ms

6.12.4.1.4 WKUP_LFOSC0 LVCMOS Digital Clock Source

Figure 6-21 shows the recommended oscillator connections when WKUP_LFOSC0_XI is connected to a 1.8-V LVCMOS square-wave digital clock source.

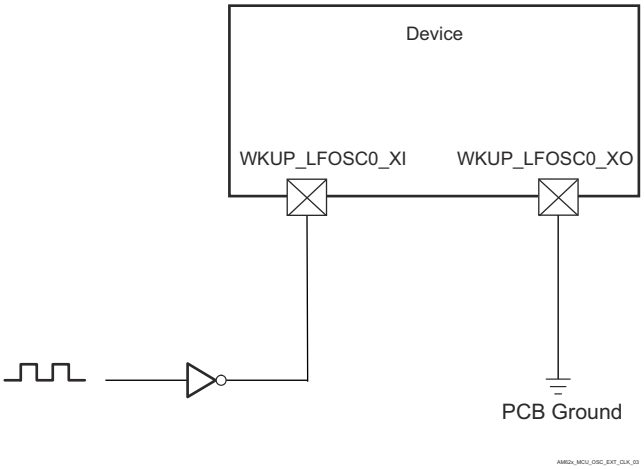


Figure 6-21. 1.8-V LVCMOS-Compatible Clock Input

6.12.4.1.5 WKUP_LFOSC0 Not Used

Figure 6-22 shows the recommended oscillator connections when WKUP_LFOSC0 is not used.

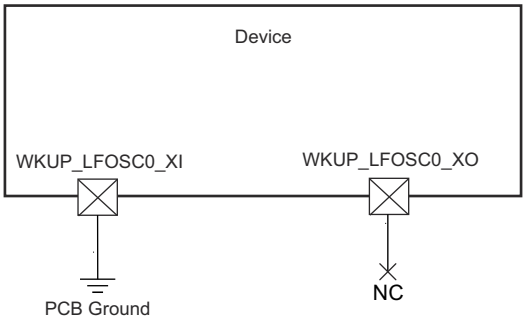


Figure 6-22. WKUP_LFOSC0 Not Used

6.12.4.2 Recommended System Precautions for Clock and Control Signal Transitions

All clock and strobe signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.

Monotonic transitions are more likely to occur with fast signal transitions. It is easy for noise to create non-monotonic events on a signal with slow transitions. Therefore, avoid slow signal transitions on all clock and control signals since they are more likely to generate glitches inside the device.

6.12.5 Peripherals

6.12.5.1 ATL

The device contains ATL module that can be used for asynchronous sample rate conversion of audio. The ATL calculates the error between two time bases, such as audio syncs, and optionally generates an averaged clock using cycle stealing via software.

Note

For more information about ATL, see *Audio Tracking Logic (ATL)* section in *Peripherals* chapter in the device TRM.

ATL Timing Conditions

PARAMETER		MODE	MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input Slew Rate	Internal or external reference CLK	0.5	5	V/ns
OUTPUT CONDITIONS					
C_L	Output Load Capacitance	Internal or external reference CLK	1	10	pF

ATL_AWS[x] Timing Requirements

NO.	PARAMETER		MODE	MIN	MAX	UNIT
D4	$t_{c(atl\_awsx)}$	Cycle time, ATL_AWS[x](3)	External reference CLK	2 × M(1)		ns
D5	$t_{w(atl\_awsLx)}$	Pulse Duration, ATL_AWS[x](3) low	Internal reference CLK	0.45 × A(2) + 2.5		ns
D6	$t_{w(atl\_awsHx)}$	Pulse Duration, ATL_AWS[x](3) high	Internal reference CLK	0.45 × A(2) + 2.5		ns

(1) M = ATL_CLK[x] period
(2) A = ATL_AWS[x] period
(3) x = 0 to 3

ATL_BWS[x] Timing Requirements

NO.	PARAMETER		MODE	MIN	MAX	UNIT
D7	$t_{c(atl\_bwsx)}$	Cycle time, ATL_BWS[x](3)	External reference CLK	2 × M(1)		ns
D8	$t_{w(atl\_bwsLx)}$	Pulse Duration, ATL_BWS[x](3) low	Internal reference CLK	0.45 × B(2) + 2.5		ns
D9	$t_{w(atl\_bwsHx)}$	Pulse Duration, ATL_BWS[x](3) high	Internal reference CLK	0.45 × B(2) + 2.5		ns

(1) M = ATL_CLK[x] period
(2) B = ATL_BWS[x] period
(3) x = 0 to 3

ATL_PCLK Timing Requirements

NO.	PARAMETER		MODE	MIN	MAX	UNIT
D1	$t_{c(pclk)}$	Cycle time, ATL_PCLK	External reference CLK	5		ns
D2	$t_{w(pclkL)}$	Pulse Duration, ATL_PCLK low	External reference CLK	0.45 × M(1) + 2.5		ns
D3	$t_{w(pclkH)}$	Pulse Duration, ATL_PCLK high	External reference CLK	0.45 × M(1) + 2.5		ns

(1) M = ATL_CLK[x] period

ATCLK[x] Switching Characteristics

NO.	PARAMETER		MODE	MIN	MAX	UNIT
D1	$t_{c(atclk)}$	Cycle time, ATCLK[x](3)	Internal reference CLK	20		ns
D2	$t_{w(atclkL)}$	Pulse Duration, ATCLK[x](3) low	Internal reference CLK	0.45 × P(2) – M(1) – 0.3		ns
DJ3	$t_{w(atclkH)}$	Pulse Duration, ATCLK[x](3) high	Internal reference CLK	0.45 × P(2) – M(1) – 0.3		ns

(1) M = ATL_CLK[x] period
(2) P = ATCLK[x] period
(3) x = 0 to 3

6.12.5.2 CPSW3G

For more details about features and additional description information on the device Gigabit Ethernet MAC, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

6.12.5.2.1 CPSW3G MDIO Timing

CPSW3G MDIO Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input Slew Rate	0.9	3.6	V/ns
OUTPUT CONDITIONS				
C_L	Output Load Capacitance	10	470	pF
PCB Connectivity Requirements				
t_d (Trace Delay)	Propagation delay of each trace	0	5	ns
t_d (Trace Mismatch Delay)	Propagation delay mismatch across all traces)		1	ns

CPSW3G MDIO Timing Requirements

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
MDIO1	$t_{su(MDIO-MDC)}$	Setup time, MDIO_DATA valid before MDIO_CLK high	45		ns
MDIO2	$t_{h(MDC-MDIO)}$	Hold time, MDIO_DATA valid after MDIO_CLK high	0		ns

CPSW3G MDIO Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
MDIO3	$t_{c(MDC)}$	Cycle time, MDIO_CLK	400		ns
MDIO4	$t_{w(MDCH)}$	Pulse duration, MDIO_CLK high	160		ns
MDIO5	$t_{w(MDCL)}$	Pulse duration, MDIO_CLK low	160		ns
MDIO7	$t_{d(MDC\_MDIO)}$	Delay time, MDIO_CLK low to MDIO_DATA valid	–10	10	ns

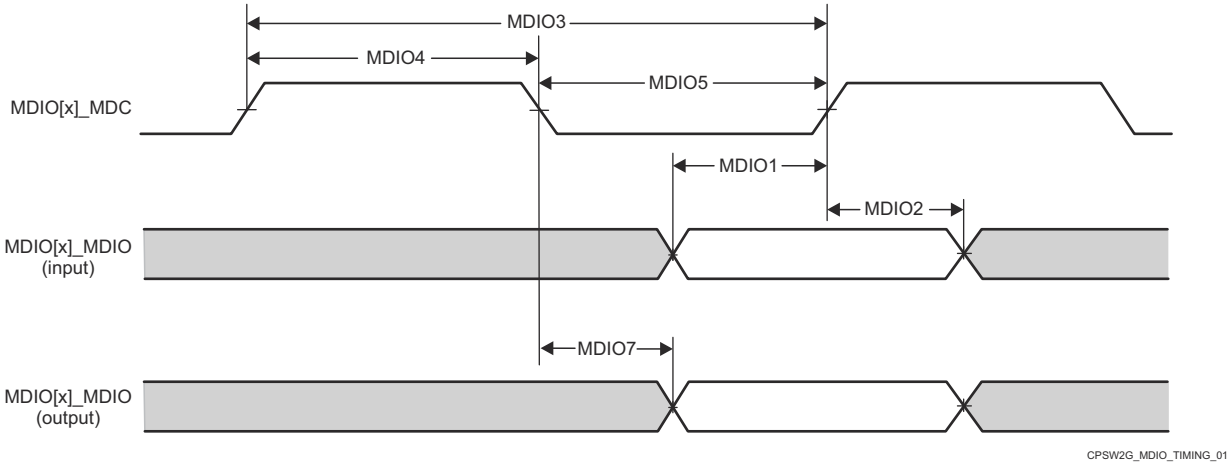


Figure 6-23. CPSW3G MDIO Timing Requirements and Switching Characteristics

6.12.5.2.2 CPSW3G RMII Timing

CPSW3G RMII Timing Conditions

PARAMETER			MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input Slew Rate	VDD = 1.8V	0.18	0.54	V/ns
		VDD = 3.3V	0.4	1.2	V/ns
OUTPUT CONDITIONS					
C_L	Output Load Capacitance		3	25	pF

CPSW3G RMII[x]_REFCLK Timing Requirements - RMII Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
RMII1	$t_{c(REF\_CLK)}$	Cycle time, REF_CLK	19.999	20.001	ns
RMII2	$t_{w(REF\_CLKH)}$	Pulse duration, REF_CLK High	7	13	ns
RMII3	$t_{w(REF\_CLKL)}$	Pulse duration, REF_CLK Low	7	13	ns

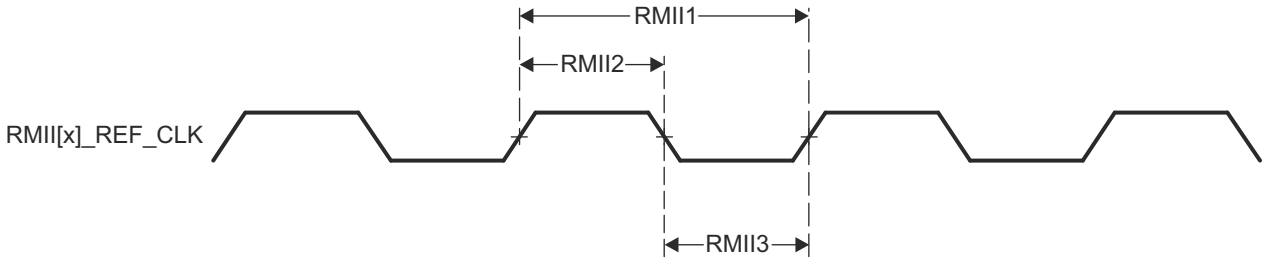


Figure 6-24. CPSW3G RMII[x]_REF_CLK Timing Requirements – RMII Mode

CPSW3G RMII[x]_RXD[1:0], RMII[x]_CRS_DV, and RMII[x]_RXER Timing Requirements - RMII Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
RMII4	$t_{su(RXD-REF\_CLK)}$	Setup time, RXD[1:0] valid before REF_CLK	4		ns
	$t_{su(CRS\_DV-REF\_CLK)}$	Setup time, CRS_DV valid before REF_CLK	4		ns
	$t_{su(RX\_ER-REF\_CLK)}$	Setup time, RX_ER valid before REF_CLK	4		ns

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
RMII5	$t_{h(REF\_CLK-RXD)}$	Hold time, RXD[1:0] valid after REF_CLK	2		ns
	$t_{h(REF\_CLK-CRS\_DV)}$	Hold time, CRS_DV valid after REF_CLK	2		ns
	$t_{h(REF\_CLK-RX\_ER)}$	Hold time, RX_ER valid after REF_CLK	2		ns

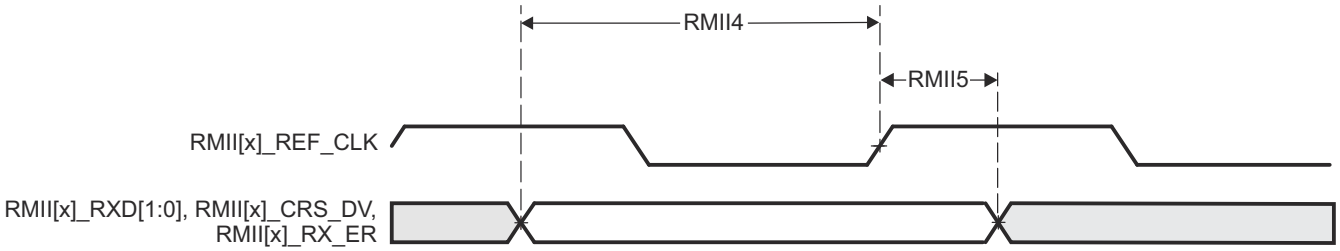


Figure 6-25. CPSW3G RMII[x]_RXD[1:0], RMII[x]_CRS_DV, RMII[x]_RX_ER Timing Requirements – RMII Mode

CPSW3G RMII[x]_TXD[1:0], and RMII[x]_TXEN Switching Characteristics - RMII Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
RMII6	$t_{d(REF\_CLK-TXD)}$	Delay time, REF_CLK High to TXD[1:0] valid	2	10	ns
	$t_{d(REF\_CLK-TXEN)}$	Delay time, REF_CLK to TXEN valid	2	10	ns

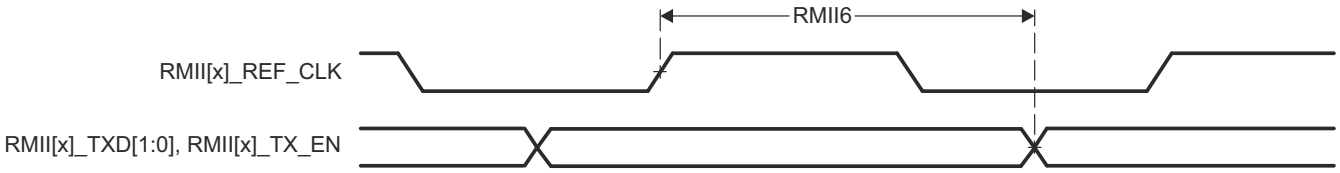


Figure 6-26. RMII[x]_TXD[1:0], and RMII[x]_TX_EN Switching Characteristics – RMII Mode

6.12.5.2.3 CPSW3G RGMII Timing

CPSW3G RGMII Timing Conditions

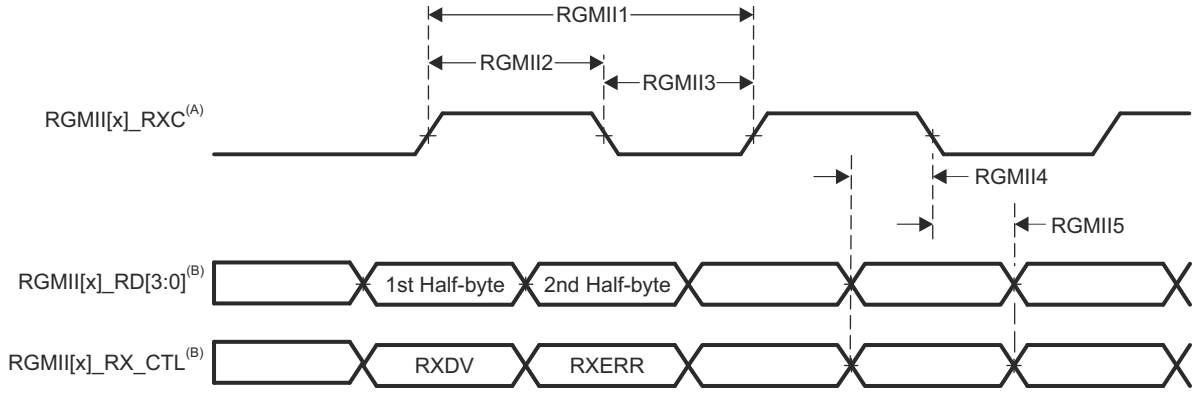
PARAMETER			MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input Slew Rate		2.64	5	V/ns
OUTPUT CONDITIONS					
C_L	Output Load Capacitance		2	20	pF
PCB Connectivity Requirements					
t_d (Trace Mismatch Delay)	Propagation Delay mismatch across all traces	RGMII[x]_RXC RGMII[x]_RD[3:0] RGMII[x]_RX_CTL		50	ps
		RGMII[x]_TXC RGMII[x]_TD[3:0] RGMII[x]_TX_CTL		50	ps

CPSW3G RGMII[x]_RCLK Timing Requirements - RGMII Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
RGMII1	$t_{c(RXC)}$	Cycle time, RXC	10Mbps	360	440	ns
			100Mbps	36	44	ns
			1000Mbps	7.2	8.8	ns
RGMII2	tw(RXCH)	Pulse duration, RXC high	10Mbps	160	240	ns
			100Mbps	16	24	ns
			1000Mbps	3.6	4.4	ns
RGMII3	tw(RXCL)	Pulse duration, RXC low	10Mbps	160	240	ns
			100Mbps	16	24	ns
			1000Mbps	3.6	4.4	ns

CPSW3G RGMII[x]_RD[3:0], and RGMII[x]_RCTL Timing Requirements - RGMII Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
RGMII4	$t_{su(RD-RXC)}$	Setup time, RD[3:0] valid before RXC high/low	10Mbps	1		ns
			100Mbps	1		ns
			1000Mbps	1		ns
	$t_{su(RX\_CTL-RXC)}$	Setup time, RX_CTL valid before RXC high/low	10Mbps	1		ns
			100Mbps	1		ns
			1000Mbps	1		ns
RGMII5	$t_{h(RXC-RD)}$	Hold time, RD[3:0] valid after RXC high/low	10Mbps	1		ns
			100Mbps	1		ns
			1000Mbps	1		ns
	$t_{h(RXC-RX\_CTL)}$	Hold time, RX_CTL valid after RXC high/low	10Mbps	1		ns
			100Mbps	1		ns
			1000Mbps	1		ns



A. RGMII[x]_RXC must be externally delayed relative to the data and control pins.

B. Data and control information is received using both edges of the clocks. RGMII[x]_RD[3:0] carries data bits 3-0 on the rising edge of RGMII[x]_RXC and data bits 7-4 on the falling edge of RGMII[x]_RXC. Similarly, RGMII[x]_RX_CTL carries RXDV on rising edge of RGMII[x]_RXC and RXERR on falling edge of RGMII[x]_RXC.

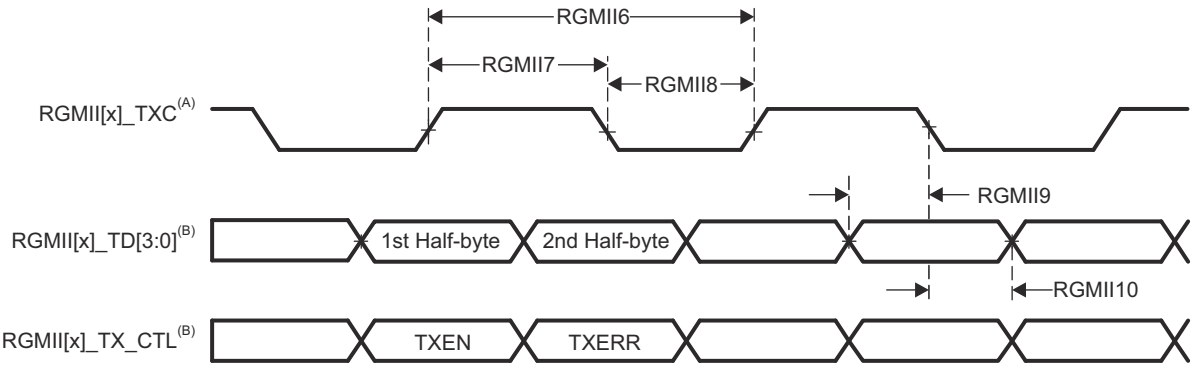
Figure 6-27. CPSW3G RGMII[x]_RXC, RGMII[x]_RD[3:0], RGMII[x]_RX_CTL Timing Requirements - RGMII Mode

CPSW3G RGMII[x]_TCLK Switching Characteristics - RGMII Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
RGMII6	$t_{c(TXC)}$	Cycle time, TXC	10Mbps	360	440	ns
			100Mbps	36	44	ns
			1000Mbps	7.2	8.8	ns
RGMII7	$t_{w(TXCH)}$	Pulse duration, TXC high	10Mbps	160	240	ns
			100Mbps	16	24	ns
			1000Mbps	3.6	4.4	ns
RGMII8	$t_{w(TXCL)}$	Pulse duration, TXC low	10Mbps	160	240	ns
			100Mbps	16	24	ns
			1000Mbps	3.6	4.4	ns

CPSW3G RGMII[x]_TD[3:0], and RGMII[x]_TCTL Switching Characteristics - RGMII Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
RGMII9	$t_{osu(TD-TXC)}$	Output setup time, RGMII[x]_TD[3:0] valid to RGMII[x]_TXC high/low	10Mbps	1.2		ns
			100Mbps	1.2		ns
			1000Mbps	1.2		ns
	$t_{osu(TX\_CTL-TXC)}$	Output setup time, RGMII[x]_TX_CTL valid to RGMII[x]_TXC high/low	10Mbps	1.2		ns
			100Mbps	1.2		ns
			1000Mbps	1.2		ns
RGMII10	$t_{oh(TXC-TD)}$	Output hold time, RGMII[x]_TD[3:0] valid after RGMII[x]_TXC high/low	10Mbps	1.2		ns
			100Mbps	1.2		ns
			1000Mbps	1.2		ns
	$t_{oh(TXC-TX\_CTL)}$	Output hold time, RGMII[x]_TX_CTL valid after RGMII[x]_TXC high/low	10Mbps	1.2		ns
			100Mbps	1.2		ns
			1000Mbps	1.2		ns



A. TXC is delayed internally before being driven to the RGMII[x]_TXC pin. This internal delay is always enabled.

B. Data and control information is received using both edges of the clocks. RGMII[x]_TD[3:0] carries data bits 3-0 on the rising edge of RGMII[x]_TXC and data bits 7-4 on the falling edge of RGMII[x]_TXC. Similarly, RGMII[x]_TX_CTL carries TXEN on rising edge of RGMII[x]_TXC and TXERR on falling edge of RGMII[x]_TXC.

Figure 6-28. CPSW3G RGMII[x]_TXC, RGMII[x]_TD[3:0], and RGMII[x]_TX_CTL Switching Characteristics - RGMII Mode

6.12.5.3 ECAP

For more information, see *Enhanced Capture (ECAP) Module* section in *Peripherals* chapter in the device TRM.

ECAP Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input Slew Rate	1	4	V/ns
OUTPUT CONDITIONS				
C_L	Output Load Capacitance	2	7	pF

ECAP Timing Requirements

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
CAP1	$t_{w(CAP)}$	Pulse duration, CAP (asynchronous)	2 × P[(1)] + 1		ns

(1) P = sysclk period in ns.

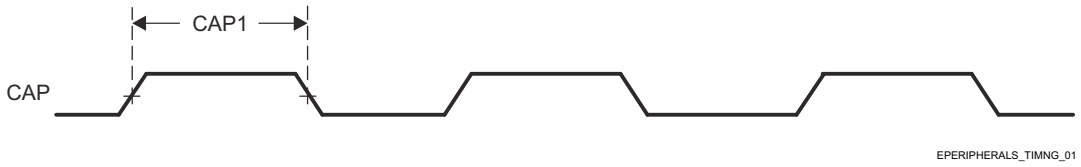


Figure 6-29. ECAP Timings Requirements

ECAP Switching Characteristics
(1)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
CAP2	$t_{w(APWM)}$	Pulse duration, APWMx high/low	2 × P[(1)] – 1		ns

(1) P = sysclk period in ns

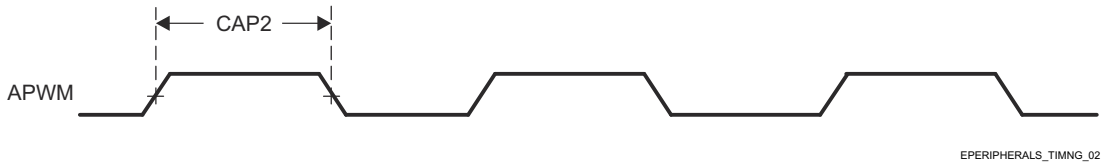


Figure 6-30. ECAP Switching Characteristics

6.12.5.4 Emulation and Debug

For more details about features and additional description information on the device Trace and JTAG interfaces, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

6.12.5.4.1 Trace

Trace Timing Conditions

PARAMETER		MIN	MAX	UNIT
OUTPUT CONDITIONS				
C_L	Output Load Capacitance	2	5	pF
OUTPUT CONDITIONS				
$t_{d(Trace\ Mismatch)}$	Propagation delay mismatch across all traces.		200	ps

Trace Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
DBTR1	$tc_{(TRC\_CLK)}$	Cycle time, TRC_CLK	1.8V	6.83		ns
			3.3V	8.78		
DBTR2	$t_{w(TRC\_CLKH)}$	Pulse width, TRC_CLK high	1.8V	2.66		ns
			3.3V	3.64		
DBTR3	$t_{w(TRC\_CLKL)}$	Pulse width, TRC_CLK low	1.8V	2.66		ns
			3.3V	3.64		
DBTR4	$t_{osu(TRC\_DATAV-TRC\_CLK)}$	Output setup time, TRC_DATA valid to TRC_CLK edge	1.8V	0.85		ns
			3.3V	1.1		
DBTR5	$t_{oh(TRC\_CLK-TRC-DATAI)}$	Output hold time, TRC_CLK edge to TRC_DATA invalid	1.8V	0.85		ns
			3.3V	1.1		
DBTR6	$t_{osu(TRC\_CTLV-TRC\_CLK)}$	Output setup time, TRC_CTL valid to TRC_CLK edge	1.8V	0.85		ns
			3.3V	1.1		
DBTR7	$t_{oh(TRC\_CLK-TRC\_CTLI)}$	Output hold time, TRC_CLK edge to TRC_CTL invalid	1.8V	0.85		ns
			3.3V	1.1		

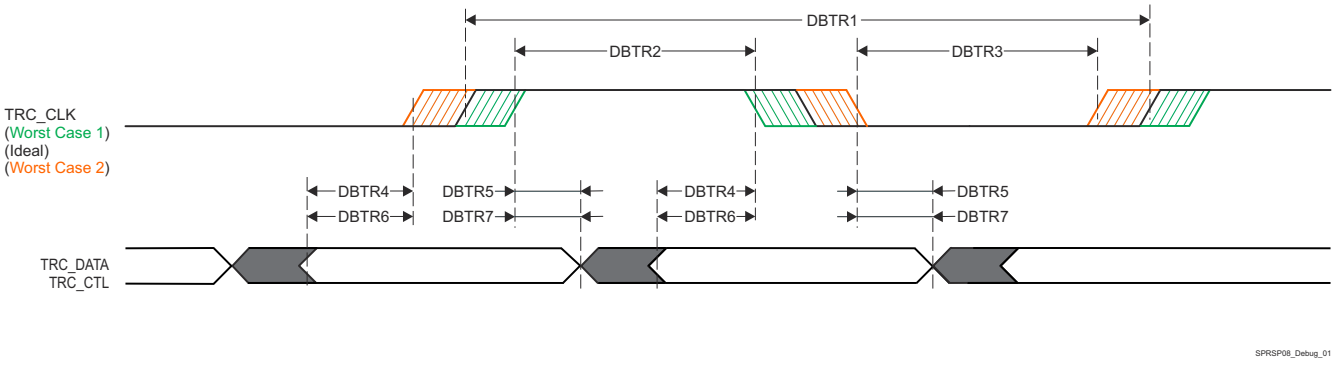


Figure 6-31. Trace Switching Characteristics

6.12.5.4.2 JTAG

JTAG Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input Slew Rate	0.5	2.00	V/ns
OUTPUT CONDITIONS				
C_L	Output Load Capacitance	5	15	pF
PCB CONNECTIVITY REQUIREMENTS				
$t_{d(Trace\ Delay)}$	Propagation delay of each trace	83.5	1000(1)	ps
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch across all traces		100	ps

(1) Maximum propagation delay associated with the JTAG signal traces has a significant impact on maximum TCK operating frequency. It may be possible to increase the trace delay beyond this value, but the operating frequency of TCK must be reduced to account for the additional trace delay.

JTAG Timing Requirements

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
J1	$t_{c(TCK)}$	Cycle time, TCK	40(1)		ns
J2	$t_{w(TCKH)}$	Pulse width, TCK high	0.4 × P(2)		ns
J3	$t_{w(TCKL)}$	Pulse width, TCK low	0.4 × P(2)		ns
J4	$t_{su(TDI-TCKH)}$	Input setup time, TDI valid to TCK high	2		ns
	$t_{su(TMS-TCKH)}$	Input setup time, TMS valid to TCK high	2		
J5	$t_{h(TCK-TDI)}$	Input hold time, TDI valid from TCK high	3		ns
	$t_{h(TCK-TMS)}$	Input hold time, TMS valid from TCK high	3		

(1) The maximum TCK operating frequency assumes the following timing requirements and switching characteristics for the attached debugger. The operating requency of TCK must be reduced to provide appropriate timing margin if the debugger exceeds any of these assumptions.
- Minimum TDO setup time of 2 ns relative to the rising edge of TCK
- TDI and TMS output delay in the range of -12.9 ns to 13.9 ns relative to the falling edge of TCK

(2) P = TCK cycle time in ns

JTAG Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
J6	$t_{d(TCKL-TDOI)}$	Delay time, TCK low to TDO invalid	0		ns
J7	$t_{d(TCKL-TDOV)}$	Delay time, TCK low to TDO valid		12	ns

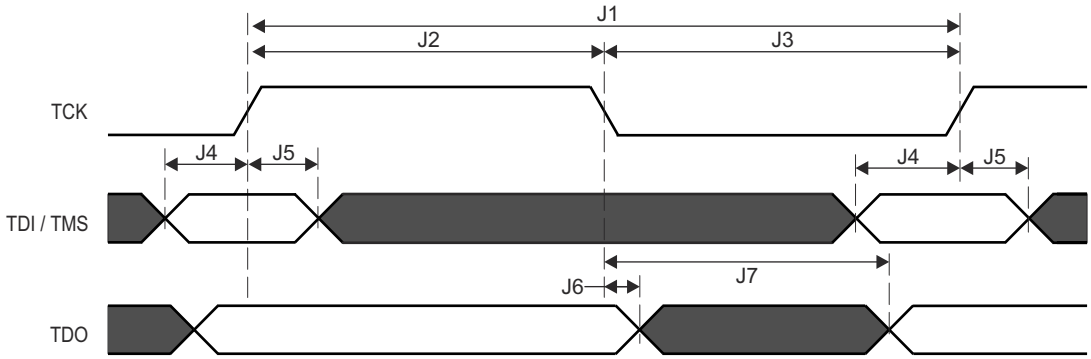


Figure 6-32. JTAG Timing Requirements and Switching Characteristics

6.12.5.5 EPWM

For more information, see *Enhanced Pulse Width Modulation (EPWM) Module* section in *Peripherals* chapter in the device TRM.

EPWM Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input Slew Rate	1	4	V/ns
OUTPUT CONDITIONS				
C_L	Output Load Capacitance	2	7	pF

EPWM Timing Requirements

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PWM6	$t_{w(SYNCIN)}$	Pulse duration, EHRPWM_SYNCI	2 × P(1) + 2		ns
PWM7	$t_{w(TZ)}$	Pulse duration, EHRPWM_TZn_IN low	3 × P(1) + 2		ns

(1) P = sysclk period in ns.

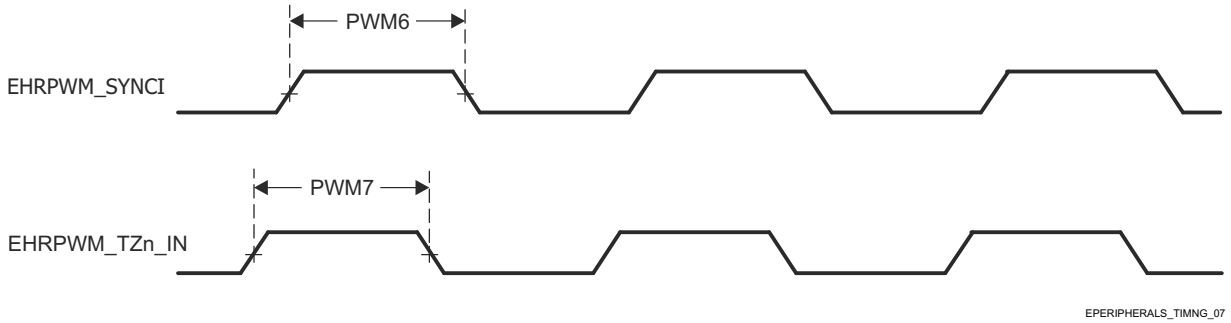


Figure 6-33. EPWM Timing Requirements

EPWM Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PWM1	$t_{w(PWM)}$	Pulse duration, EHRPWM_A/B high/low	P(1) – 3		ns
PWM2	$t_{w(SYNCOUT)}$	Pulse duration, EHRPWM_SYNCO	P(1) – 3		ns
PWM3	$t_{d(TZ-PWM)}$	Delay time, EHRPWM_TZn_IN active to EHRPWM_A/B forced high/low		11	ns
PWM4	$t_{d(TZ-PWMZ)}$	Delay time, EHRPWM_TZn_IN active to EHRPWM_A/B Hi-Z		11	ns
PWM5	$t_{w(SOC)}$	Pulse duration, EHRPWM_SOCA/B output	P(1) – 3		ns

(1) P = sysclk period in ns.

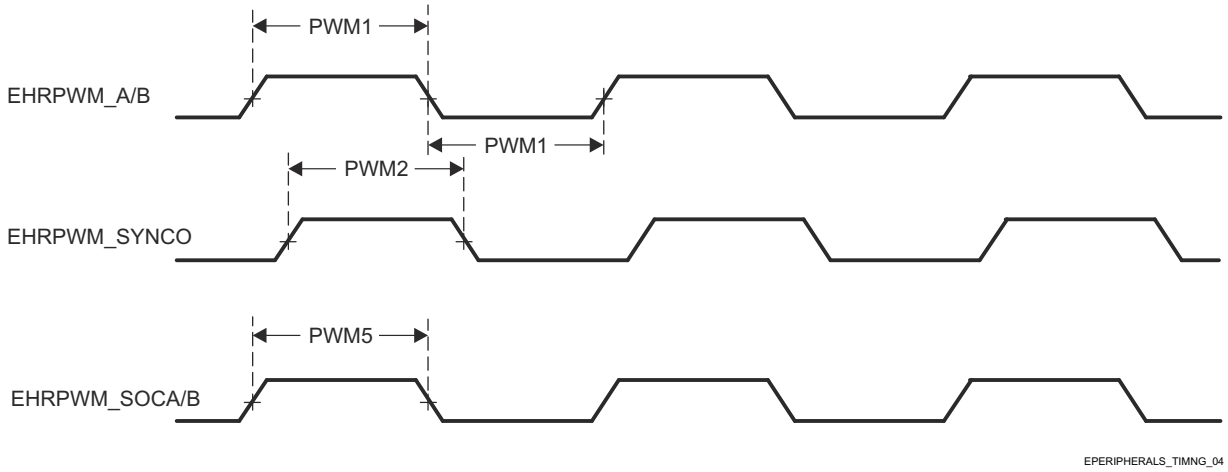


Figure 6-34. EHRPWM Switching Characteristics

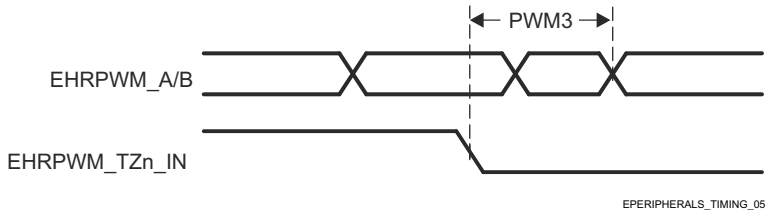


Figure 6-35. EHRPWM_TZn_IN to EHRPWM_A/B Forced Switching Characteristics

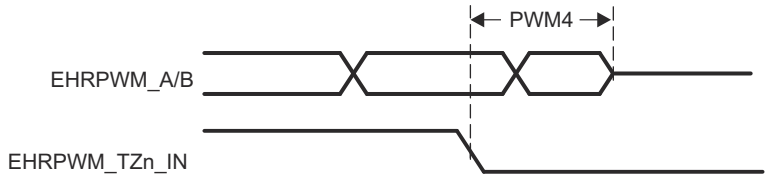


Figure 6-36. EHRPWM_TZn_IN to EHRPWM_A/B Hi-Z Switching Characteristics

For more information, see *Enhanced Pulse Width Modulation (EPWM) Module* section in *Peripherals* chapter in the device TRM.

6.12.5.6 GPIO

The device has three instances of the GPIO module.

- MCU_GPIO0
- GPIO0
- GPIO1

Note

GPIOn_x is generic name used to describe a GPIO signal, where n represents the specific GPIO module and x represents one of the input/output signals associated with the module.

For more information, see *General-Purpose Interface (GPIO)* section in *Peripherals* chapter in the device TRM.

GPIO Timing Conditions

PARAMETER		BUFFER TYPE	MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input Slew Rate	LVCMOS	0.2	6.6	V/ns
		I2C OD FS(1)	0.0033	0.08	V/ns
OUTPUT CONDITIONS					
C_L	Output Load Capacitance	LVCMOS	3	10	pF
		I2C OD FS(1)	3	100	pF

(1) A pull-up resistor is required for buffer type *I2C OD FS*.

GPIO Timing Requirements

NO.	PARAMETER	DESCRIPTION	BUFFER TYPE	MIN	MAX	UNIT
D3	$t_{w(GPIO\_IN)}$	Minimum Input Pulse Width	LVCMOS	2P(1) + 3		ns
D4			I2C OD FS(2)	2P(1) + 28		ns

(1) P = functional clock period in ns.
(2) A pull-up resistor is required for buffer type *I2C OD FS*.

GPIO Switching Characteristics

NO.	PARAMETER	DESCRIPTION	BUFFER TYPE	MIN	MAX	UNIT
D1	$t_{w(GPIO\_OUT)}$	Minimum Output Pulse Width	LVCMOS	0.975P(1) – 3.6		ns
D2	$t_{w(GPIO\_OUT)}$	Minimum Output Pulse Width Low	I2C OD FS(2)	160		ns
D3	$t_{w(GPIO\_OUT)}$	Minimum Output Pulse Width High	I2C OD FS(2)	160		ns

(1) P = functional clock period in ns.
(2) A pull-up resistor is required for buffer type *I2C OD FS*.

6.12.5.7 HyperBus

For more information, see *HyperBus Module* section in *Peripherals* chapter in the device TRM.

HyperBus Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input Slew Rate	2	5	V/ns
OUTPUT CONDITIONS				
C_L	Output Load Capacitance	1.5	8	pF

HyperBus Timing Requirements

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
D1	$t_{w(RESETn)}$	Pulse width, RESETn	200		ns
D2	$t_{w(csL)}$	Pulse width, Chip Select	1000		ns
D3	$t_{d(RESETnH-csL)}$	Delay time, RESETn inactive to CSn active	200.34		ns
D4	$t_{d(csL-RWDSL)}$	Delay time, CSn active to RWDS falling	186		ns

HyperBus 166MHz Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
D5	$t_{skn(rwdsX-dV)}$	Input skew, RWDS transitioning to D0:D7 valid	–0.46	0.46	ns
D6	$t_{c(clk/clkn)}$	CLK period, CLK/CLKn	6		ns
D7	$t_{w(clk/clkn)}$	Pulse width, CLK/CLKn	2.7		ns
D8	$t_{w(csIV)}$	Pulse width, CS0 invalid between operations	6		ns
D9	$t_{d(clkH-csL)}$	Delay time, CS0 active to CLK rising / CLKn falling		–3.28	
D10	$t_{d(clkL[LE]-csH)}$	Delay time, last falling CLK / rising CLKn edge to CS0 inactive	0.28		ns
D11	$t_{d(clkX-rwdsV)}$	Delay time, CLK transition to RWDS valid	0.88	2.14	
D12	$t_{d(clkX-d[0:7]V)}$	Delay time, CLK transitioning to D0:D7 valid	0.71	2.3	

HyperBus 100MHz Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
LFD5	$t_{skn(rwdsX-dV)}$	Input skew, RWDS transitioning to D0:D7 valid	–0.81	0.81	ns
LFD6	$t_{c(clk/clkn)}$	CLK period, CLK/CLKn	10		ns
LFD7	$t_{w(clk/clkn)}$	Pulse width, CLK/CLKn	4.75		ns
LFD8	$t_{w(csIV)}$	Pulse width, CS0 invalid between operations	10		ns
LFD9	$t_{d(clkH-csL)}$	Delay time, CS0 active to CLK rising / CLKn falling		–3.51	
LFD10	$t_{d(clkL[LE]-csH)}$	Delay time, last falling CLK / rising CLKn edge to CS0 inactive	0.51		ns
LFD11	$t_{d(clkX-rwdsV)}$	Delay time, CLK transition to RWDS valid	1.51	3.49	
LFD12	$t_{d(clkX-d[0:7]V)}$	Delay time, CLK transitioning to D0:D7 valid	1.34	3.66	

6.12.5.8 I2C

The device contains eight multicontroller Inter-Integrated Circuit (I2C) controllers. Each I2C controller was designed to be compliant to the Philips I²C-bus™ specification version 2.1. However, the device IOs are not fully compliant to the I2C electrical specification. The speeds supported and exceptions are described per port below:

- I2C0, I2C1, I2C2, I2C3, I2C4, I2C5, and I2C6
  - Speeds:
    - Standard-mode (up to 100Kbits/s)
      - 1.8V
      - 3.3V
    - Fast-mode (up to 400Kbits/s)
      - 1.8V
      - 3.3V
  - Exceptions:
    - The IOs associated with these ports are not compliant to the fall time requirements defined in the I2C specification because the IOs are implemented with higher performance LVCMOS push-pull IOs. These were designed to support other signal functions that can not be implemented with I2C compatible IOs. The LVCMOS IOs used on these ports are connected to emulate open-drain outputs. This emulation is achieved by forcing a constant low output and disabling the output buffer to enter the Hi-Z state.
    - The I2C specification defines a maximum input voltage V_{IH} of ($V_{DD_{max}}$ + 0.5 V), which exceeds the absolute maximum ratings for the device IOs. The system must be designed to provide the I2C signals never exceed the limits defined in the *Absolute Maximum Ratings* section of this data sheet.
- WKUP_I2C0
  - Speeds:
    - Standard-mode (up to 100Kbits/s)
      - 1.8V
      - 3.3V
    - Fast-mode (up to 400Kbits/s)
      - 1.8V
      - 3.3V
    - Hs-mode (up to 3.4Mbits/s)
      - 1.8V
  - Exceptions:
    - The IOs associated with these ports were not design to support Hs-mode while operating at 3.3V. So Hs-mode is limited to 1.8V operation.
    - The rise and fall times of the I2C signals connected to these ports must not exceed a slew rate of 0.08 V/ns (or 8E+7V/s). This limit is more restrictive than the minimum fall time limits defined in the I2C specification. Therefore, you can need to add additional capacitance to the I2C signals to slow the rise and fall times to not exceed a slew rate of 0.08V/ns.
    - The I2C specification defines a maximum input voltage V_{IH} of ($V_{DD_{max}}$ + 0.5 V), which exceeds the absolute maximum ratings for the device IOs. The system must be designed to provide the I2C signals never exceed the limits defined in the *Absolute Maximum Ratings* section of this data sheet.

Note

I2C3 has one or more signals which can be multiplexed to more than one pin. Timing is only valid for specific pin combinations known as IOSETs. Valid pin combinations or IOSETs for this interface are defined in the **SysConfig-PinMux Tool**.

Refer to the Philips I2C-bus specification version 2.1 for timing details.

For more details about features and additional description information on the device inter-integrated circuit, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

6.12.5.9 MCAN

For more details about features and additional description information on the device Controller Area Network Interface, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

Note

The device has multiple MCAN modules. MCANn is a generic prefix applied to MCAN signal names, where n represents the specific MCAN module.

For more information, see *Controller Area Network (MCAN)* section in *Peripherals* chapter in the device TRM.

MCAN Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input Slew Rate	0.33	15	V/ns
OUTPUT CONDITIONS				
C_L	Output Load Capacitance	5	20	pF

MCAN Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
M1	$t_{d(MCAN\_TX)}$	Delay time, transmit shift register to MCANn_TX pin		10	ns
M2	$t_{d(MCAN\_RX)}$	Delay time, MCANn_RX pin to receive shift register		10	ns

6.12.5.10 MCASP

Note

McASP has one or more signals which can be multiplexed to more than one pin. Timing requirements and switching characteristics defined in this section are only valid for specific pin combinations known as IOSETs. Valid pin combinations or IOSETs for this interface are defined in the **SysConfig-PinMux Tool**.

For more information, see *Multichannel Audio Serial Port (MCASP)* section in *Peripherals* chapter in the device TRM.

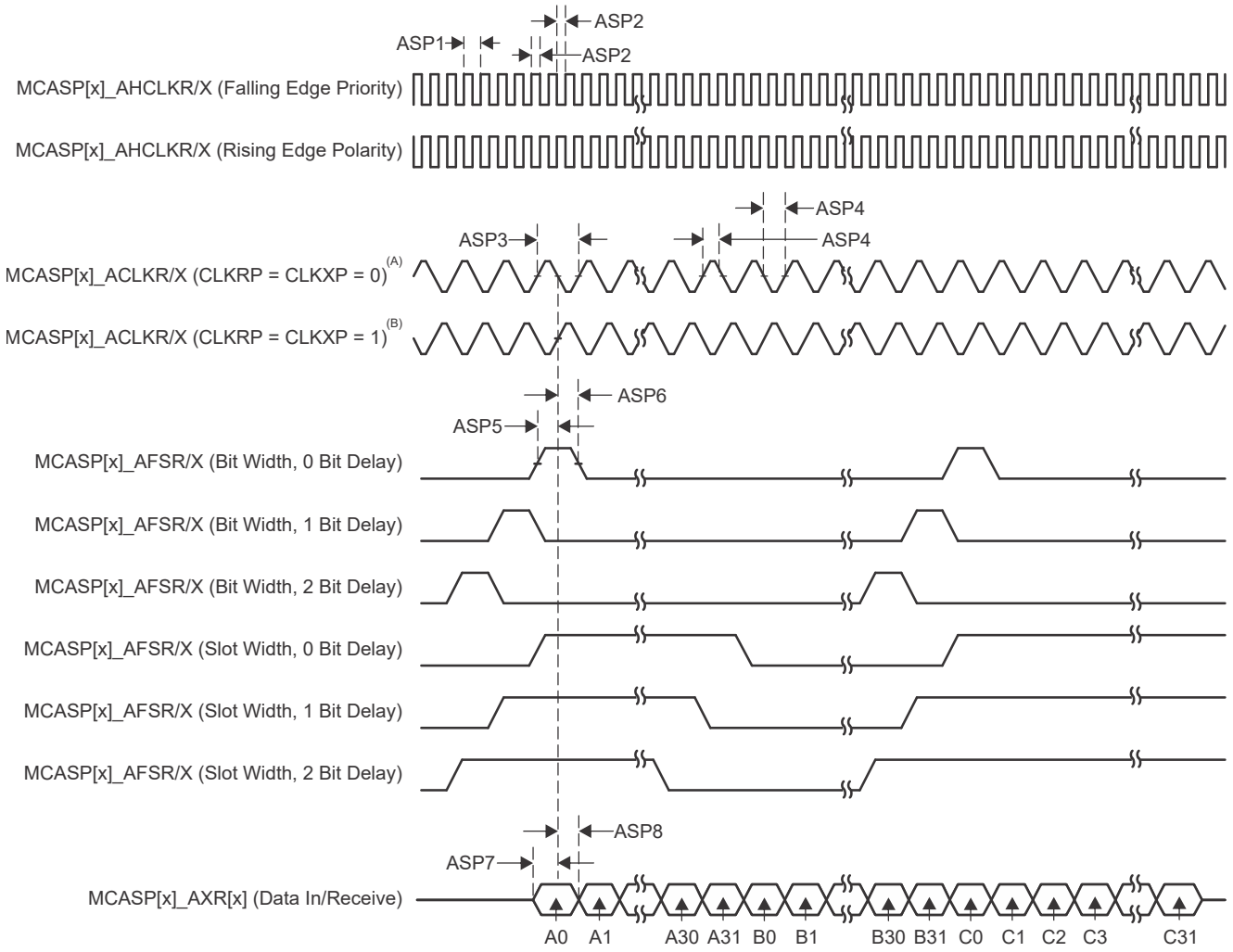
MCASP Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input Slew Rate	0.7	5	V/ns
OUTPUT CONDITIONS				
C_L	Output Load Capacitance	1	10	pF
PCB CONNECTIVITY REQUIREMENTS				
$t_{d(Trace\ Delay)}$	Propagation delay of each trace	100	1100	ps
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch across all traces		100	ps

MCASP Timing Requirements

NO.	PARAMETER	DESCRIPTION	MODE(1)	MIN	MAX	UNIT
ASP1	$t_{c(AHCLKRX)}$	Cycle time, MCASP[x]_AHCLKR/X(4)		20		ns
ASP2	$t_{w(AHCLKRX)}$	Pulse duration, MCASP[x]_AHCLKR/X(4) high or low		0.5P(2) – 1.53		ns
ASP3	$t_{c(ACLKRX)}$	Cycle time, MCASP[x]_ACLKR/X(4)		20		ns
ASP4	$t_{w(ACLKRX)}$	Pulse duration, MCASP[x]_ACLKR/X(4) high or low		0.5R(3) – 1.53		ns
ASP5	$t_{su(AFSRX-ACLKRX)}$	Setup time, MCASP[x]_AFSR/X(4) input valid before MCASP[x]_ACLKR/X(4)	ACLKR/X int	9.29		ns
			ACLKR/X ext in/out	4		ns
ASP6	$t_{h(ACLKRX-AFSRX)}$	Hold time, MCASP[x]_AFSR/X(4) input valid after MCASP[x]_ACLKR/X(4)	ACLKR/X int	–1		ns
			ACLKR/X ext in/out	1.6		ns
ASP7	$t_{su(AXR-ACLKRX)}$	Setup time, MCASP[x]_AXR(4) input valid before MCASP[x]_ACLKR/X(4)	ACLKR/X int	9.29		ns
			ACLKR/X ext in/out	4		ns
ASP8	$t_{h(ACLKRX-AXR)}$	Hold time, MCASP[x]_AXR(4) input valid after MCASP[x]_ACLKR/X(4)	ACLKR/X int	–1		ns
			ACLKR/X ext in/out	1.6		ns

(1) ACLKR internal: ACLKRCTL.CLKRM=1, PDIR.ACLKR = 1
ACLKR external input: ACLKRCTL.CLKRM=0, PDIR.ACLKR=0
ACLKR external output: ACLKRCTL.CLKRM=0, PDIR.ACLKR=1
ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1
ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0
ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1
(2) P = AHCLKR/X period in ns. For details on AHCLKR/X clock source options, see the McASP Clocks table in the Multichannel Audio Serial Port (MCASP) section of the Module Integration chapter found in the Technical Reference Manual.
(3) R = ACLKR/X period in ns.
(4) x in MCASP[x]_* is 0, 1, 2, 3, or 4



A. For CLKRP = CLKXP = 0, the MCASP transmitter is configured for rising edge (to shift data out) and the MCASP receiver is configured for falling edge (to shift data in).

B. For CLKRP = CLKXP = 1, the MCASP transmitter is configured for falling edge (to shift data out) and the MCASP receiver is configured for rising edge (to shift data in).

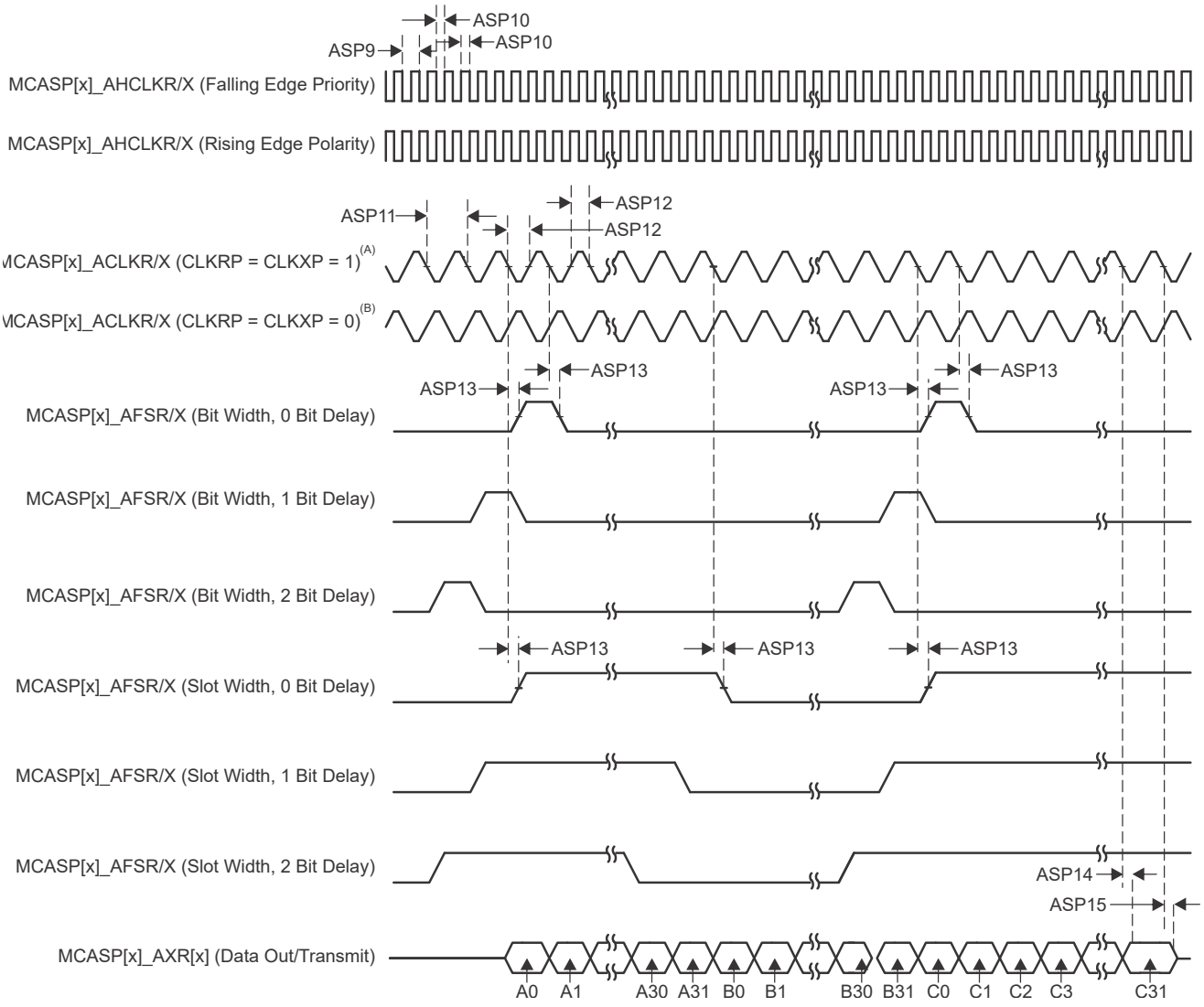
Figure 6-37. MCASP Timing Requirements

MCASP Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MODE(1)	MIN	MAX	UNIT
ASP9	$t_{c(AHCLKRX)}$	Cycle time, MCASP[x]_AHCLKR/X(4)		20		ns
ASP10	$t_{w(AHCLKRX)}$	Pulse duration, MCASP[x]_AHCLKR/X(4) high or low		0.5P(2) – 2		ns
ASP11	$t_{c(ACLKRX)}$	Cycle time, MCASP[x]_ACLKR/X(4)		20		ns
ASP12	$t_{w(ACLKRX)}$	Pulse duration, MCASP[x]_ACLKR/X(4) high or low		0.5R(3) – 2		ns
ASP13	$t_{d(ACLKRX-AFSRX)}$	Delay time, MCASP[x]_ACLKR/X(4) transmit edge to MCASP[x]_AFSR/X(4)	ACLKR/X int	–1	7.25	ns
			ACLKR/X ext in/out	–15.29	12.84	ns
ASP14	$t_{d(ACLKX-AXR)}$	Delay time, MCASP[x]_ACLKX(4) transmit edge to MCASP[x]_AXR(4)	ACLKR/X int	–1	7.25	ns
			ACLKR/X ext in/out	–15.29	12.84	ns

NO.	PARAMETER	DESCRIPTION	MODE(1)	MIN	MAX	UNIT
ASP15	$t_{dis(ACLKX-AXR)}$	Disable time, MCASP[x]_ACLKX(4) transmit edge to MCASP[x]_AXR(4) output high impedance	ACLKR/X int	–1	7.25	ns
			ACLKR/X ext in/out	–14.9	14	ns

(1) ACLKR internal: ACLKRCTL.CLKRM=1, PDIR.ACLKR = 1
ACLKR external input: ACLKRCTL.CLKRM=0, PDIR.ACLKR=0
ACLKR external output: ACLKRCTL.CLKRM=0, PDIR.ACLKR=1
ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1
ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0
ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1
(2) P = AHCLKR/X period in ns. For details on AHCLKR/X clock source options, see the McASP Clocks table in the Multichannel Audio Serial Port (MCASP) section of the Module Integration chapter found in the Technical Reference Manual.
(3) R = ACLKR/X period in ns.
(4) x in MCASP[x]_* is 0, 1, 2, 3, or 4



A. For CLKRP = CLKXP = 1, the MCASP transmitter is configured for falling edge (to shift data out) and the MCASP receiver is configured for rising edge (to shift data in).
B. For CLKRP = CLKXP = 0, the MCASP transmitter is configured for rising edge (to shift data out) and the MCASP receiver is configured for falling edge (to shift data in).

Figure 6-38. MCASP Switching Characteristics

6.12.5.11 MCSPI

Note

McSPI has one or more signals which can be multiplexed to more than one pin. Timing requirements and switching characteristics defined in this section are only valid for specific pin combinations known as IOSETs. Valid pin combinations or IOSETs for this interface are defined in the **SysConfig-PinMux Tool**.

For more details about features and additional description information on the device Serial Port Interface, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

For more information, see *Multichannel Serial Peripheral Interface (MCSPI)* section in *Peripherals* chapter in the device TRM.

MCSPI Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input Slew Rate	2	8.5	V/ns
OUTPUT CONDITIONS				
C_L	Output Load Capacitance	2	12	pF

MCSPI Timing Requirements - Controller Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SM4	$t_{su(POCI-SPICLK)}$	Setup time, SPIn_D[x] valid before SPIn_CLK active edge	2.8		ns
SM5	$t_{h(SPICLK-POCI)}$	Hold time, SPIn_D[x] valid after SPIn_CLK active edge	3		ns

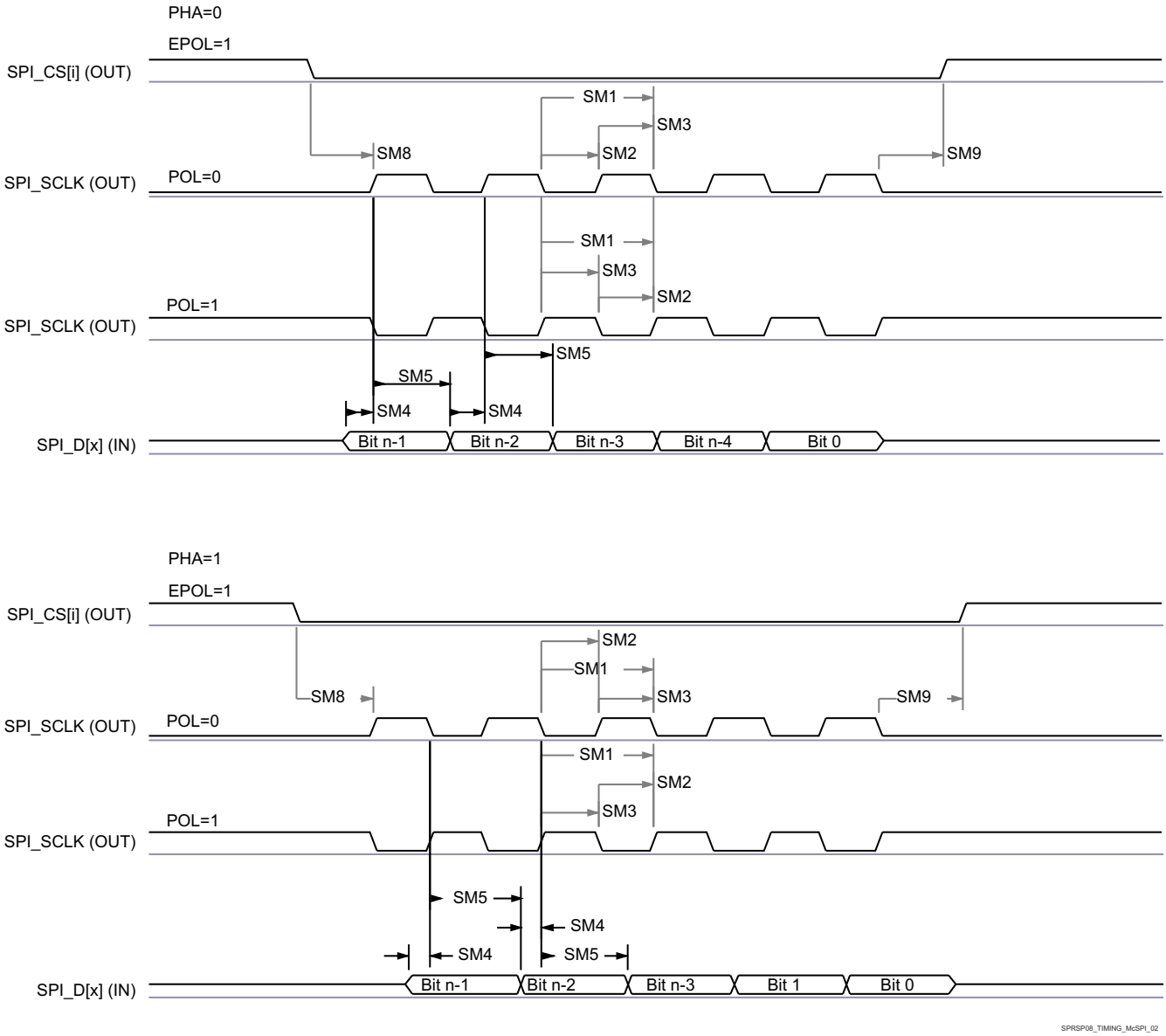


Figure 6-39. SPI Controller Mode Receive Timing

MCSPI Switching Characteristics - Controller Mode

NO.	PARAMETER	DESCRIPTION		MIN	MAX	UNIT
SM1	$t_{c(SPICLK)}$	Cycle time, SPIn_CLK		20		ns
SM2	$t_{w(SPICLKL)}$	Pulse duration, SPIn_CLK low		0.5P – 1[1]		ns
SM3	$t_{w(SPICLKH)}$	Pulse duration, SPIn_CLK high		0.5P – 1[1]		ns
SM6	$t_{d(SPICLK-PICO)}$	Delay time, SPIn_CLK active edge to SPIn_D[x]		–3	2.5	ns
SM7	$t_{d(CS-PICO)}$	Delay time, SPIn_CSi active edge to SPIn_D[x]		5		ns
SM8	$t_{d(CS-SPICLK)}$	Delay time, SPIn_CSi active to SPIn_CLK first edge	PHA = 0	B[2] – 4		ns
			PHA = 1	A[3] – 4		ns
SM9	$t_{d(SPICLK-CS)}$	Delay time, SPIn_CLK last edge to SPIn_CSi inactive	PHA = 0	A[3] – 4		ns
			PHA = 1	B[2] – 4		ns

(1) P = SPI Clock Period in ns

(2) T_ref is the period of the McSPI functional clock in ns. Fratio is the divide ratio of McSPI functional clock frequency to SPIn_CLK clock frequency, controlled by the CLKD and CLKG bit fields in the MSPI_CH(i)CONF register and the EXTCLK bit field in the MSPI_CH(i)CTRL register. TCS(i) is the value programmed into the chip select time control bit field of the MSPI_CH(i)CONF register.
- When Fratio = 1; B = (TCS(i) + 0.5) * T_ref.
- When Fratio ≥ 2 and even value; B = (TCS(i) + 0.5) * Fratio * T_ref.
- When Fratio ≥ 3 and odd value; B = ((TCS(i) * Fratio) + ((Fratio + 1) / 2)) * T_ref.

(3) T_ref is the period of the McSPI functional clock. Fratio is the divide ratio of McSPI functional clock frequency to SPIn_CLK clock frequency, controlled by the CLKD and CLKG bit fields in the MSPI_CH(i)CONF register and the EXTCLK bit field in the MSPI_CH(i)CTRL register. TCS(i) is the value programmed into the chip select time control bit field of the MSPI_CH(i)CONF register.
- When Fratio = 1; A = (TCS(i) + 1) * T_ref.
- When Fratio ≥ 2 and even value; A = (TCS(i) + 0.5) * Fratio * T_ref.
- When Fratio ≥ 3 and odd value; A = ((TCS(i) * Fratio) + ((Fratio - 1) / 2)) * T_ref.

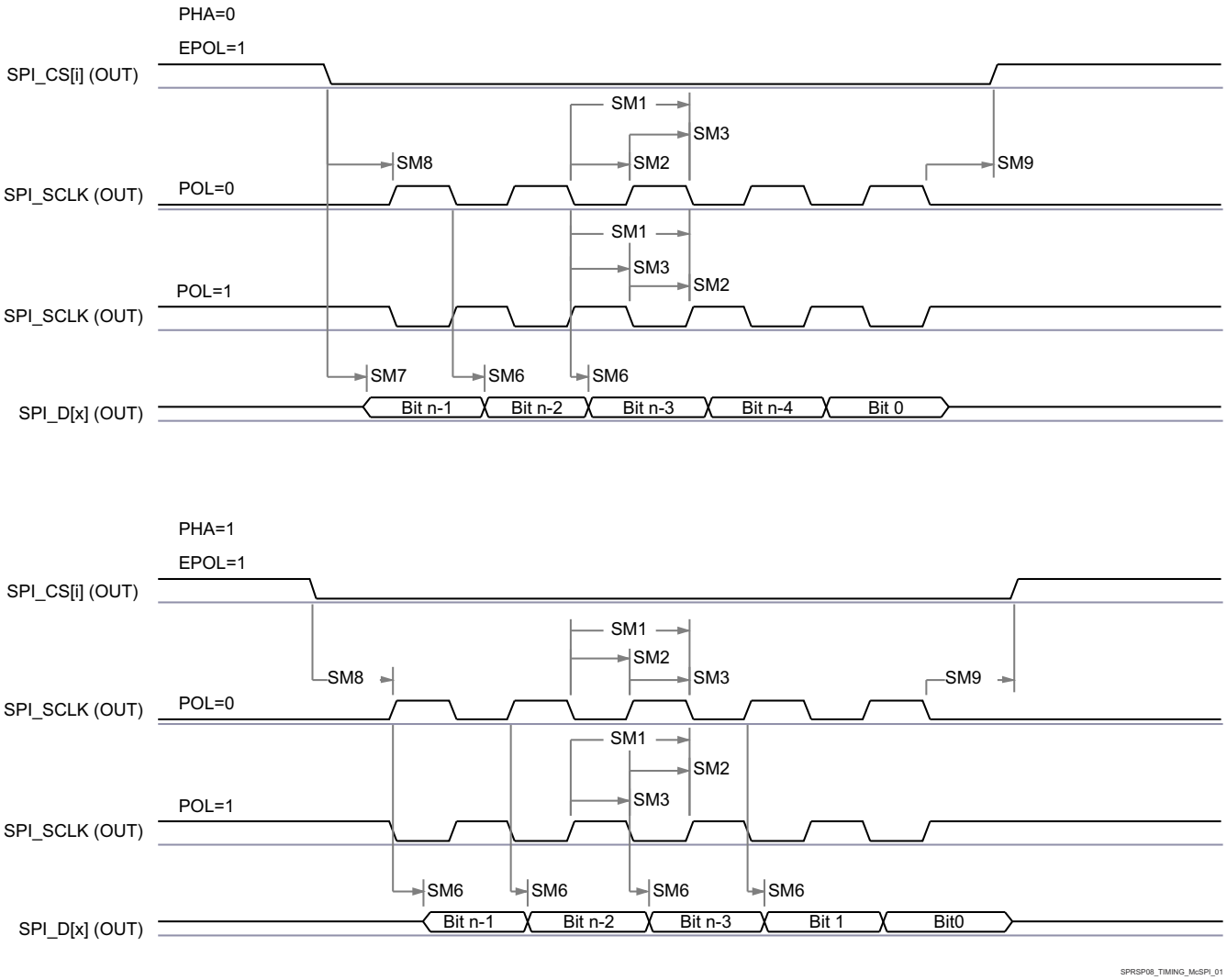


Figure 6-40. SPI Controller Mode Transmit Timing

MCSPI Timing Requirements - Peripheral Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SS1	$t_{c(SPICLK)}$	Cycle time, SPIn_CLK	20		ns
SS2	$t_{w(SPICLKL)}$	Pulse duration, SPIn_CLK low	0.45P(1)		ns
SS3	$t_{w(SPICLKH)}$	Pulse duration, SPIn_CLK high	0.45P(1)		ns
SS4	tsu(PICO-SPICLK)	Setup time, SPIn_D[x] valid before SPIn_CLK active edge	5		ns

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SS5	$t_{h(SPICLK-PICO)}$	Hold time, SPIn_D[x] valid after SPIn_CLK active edge	5		ns
SS8	$t_{su(CS-SPICLK)}$	Setup time, SPIn_CSi valid before SPIn_CLK first edge	5		ns
SS9	$t_{h(SPICLK-CS)}$	Hold time, SPIn_CSi valid after SPIn_CLK last edge	5		ns

(1) P = SPIn_CLK period in ns

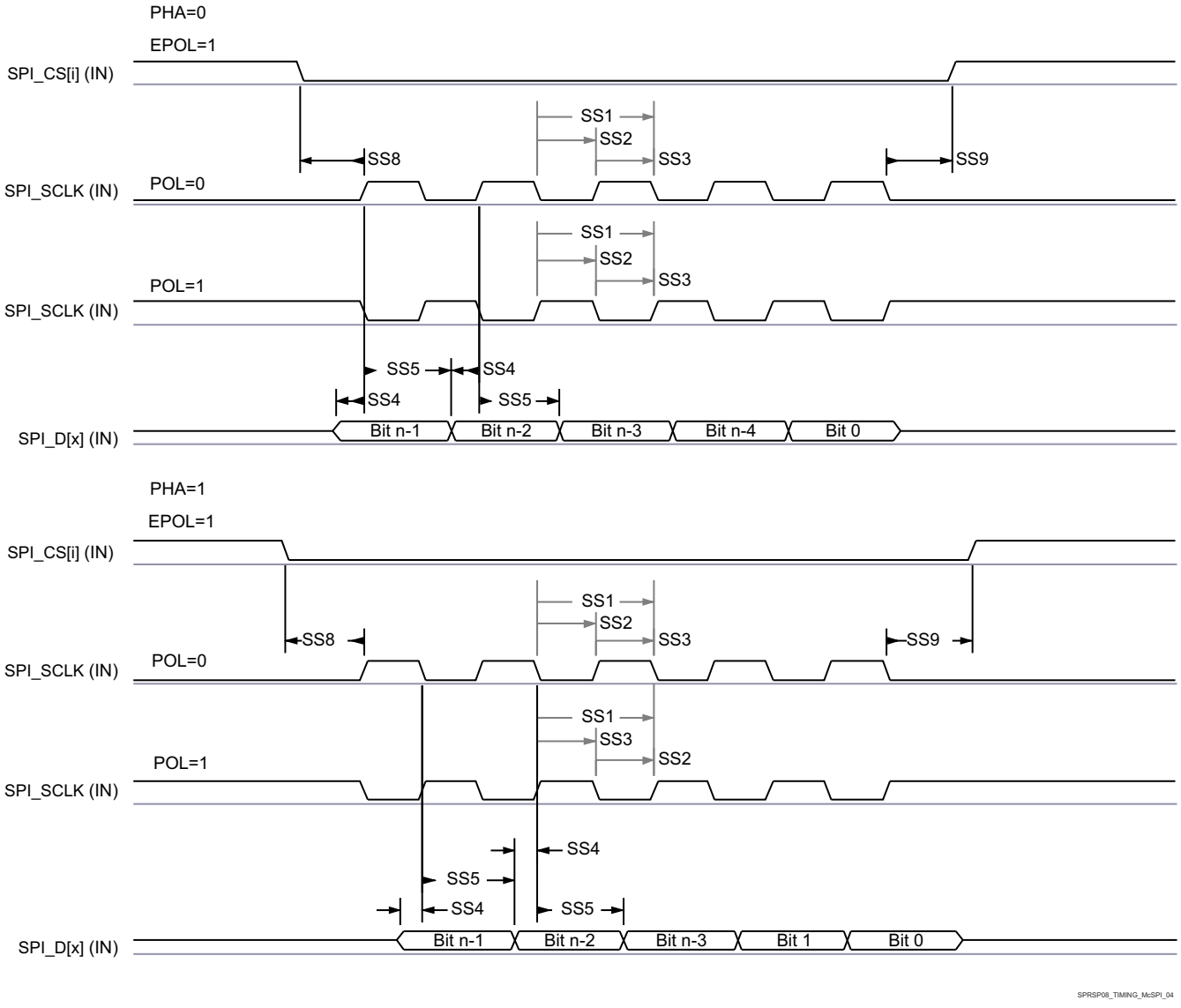


Figure 6-41. SPI Peripheral Mode Receive Timing

MCSPI Switching Characteristics - Peripheral Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SS6	$t_{d(SPICLK-POCI)}$	Delay time, SPIn_CLK active edge to SPIn_D[x]	2	13	ns
SS7	$t_{sk(CS-POCI)}$	Delay time, SPIn_CSi active edge to SPIn_D[x]		18	ns

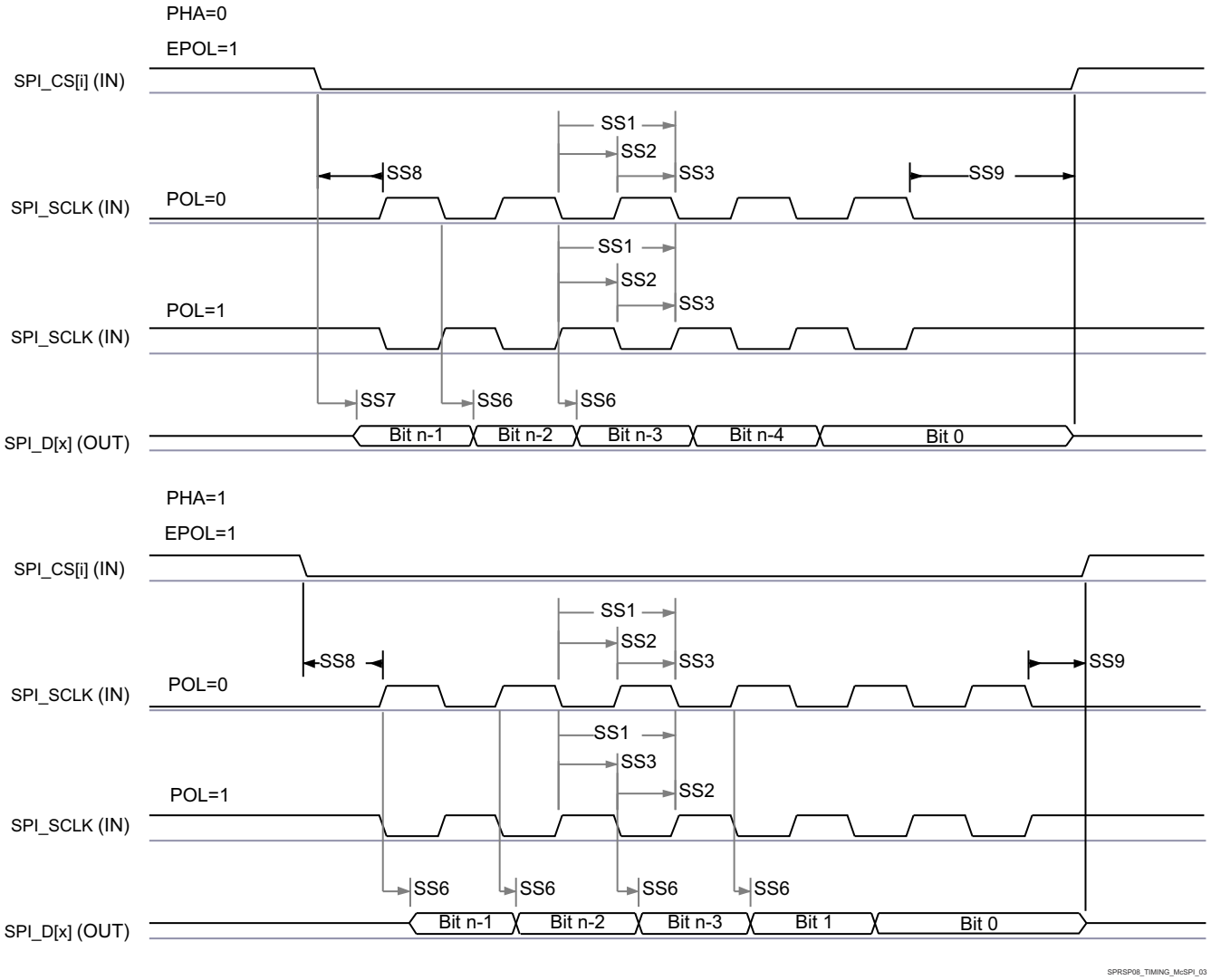


Figure 6-42. SPI Peripheral Mode Transmit Timing

6.12.5.12 MLB

For more information, see *Media Local Bus (MLB) Module* section in *Peripherals* chapter in the device TRM.

MLB Timing Conditions

PARAMETER		MODE	MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input Slew Rate	256FS	0.12	0.81	V/ns
		512FS	0.12	0.81	V/ns
		1024FS	0.12	0.81	V/ns
		2048FS, 3072FS, 4096FS - CLK	0.76	3.83	V/ns
		2048FS, 3072FS, 4096FS - SIG	0.7	3.93	V/ns
OUTPUT CONDITIONS					
C_L	Output Load Capacitance	256FS	1	60	pF
		512FS	1	60	pF
		1024FS	1	20	pF
		2048FS, 3072FS, 4096FS	1	5	pF

MLB Timing Requirements for MLBCLK - 3-pin
(1)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
1	$t_{c(MLBCLK)}$	Cycle time, MLB_CLK	256FS	78.1		ns
			512FS	39.1		ns
			1024FS	19.5		ns
2	$t_{w(MLBCLKH)}$	Pulse duration, MLB_CLK high	256FS	30		ns
			512FS	14		ns
			1024FS	6.1		ns
3	$t_{w(MLBCLKL)}$	Pulse duration, MLB_CLK low	256FS	30		ns
			512FS	14		ns
			1024FS	9.3		ns

(1) The reference points for the rise and fall transitions are measured at VIL MAX and VIH MIN.

MLB Timing Requirements for Receive Data - 3-pin

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
4	$t_{su(MLBDAT-MLBCLKL)}$	Setup time, MLB_DAT/MLB_SIG input valid before MLB_CLK low	256FS	1		ns
			512FS	1		ns
			1024FS	1		ns
5	$t_{h(MLBCLKL-MLBDAT)}$	Hold time, MLB_DAT/MLB_SIG input valid after MLB_CLK low	256FS	4		ns
			512FS	4		ns
			1024FS	2		ns

MLB Switching Characteristics - 3-Pin

NO.	PARAMETER	DESCRIPTION	BUFFER TYPE	MIN	MAX	UNIT
6	$t_{d(MLBCLKH-MLBDATV)}$	Delay time, MLBCLKH rising to MLB_DAT/MLB_SIG valid	256FS	0	20	ns
			512FS	0	10	ns
			1024FS	0	7	ns

NO.	PARAMETER	DESCRIPTION	BUFFER TYPE	MIN	MAX	UNIT
7	$t_{dis(MLBCLKL-MLBDATZ)}$	Disable time, MLBCLKH falling to MLB_DAT/MLB_SIG High-Z	256FS	0	30	ns
			512FS	0	14	ns
			1024FS	0	6.1	ns

MLB Timing Requirements for MLBCLK - 6-pin

(1)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
1	$t_{c(MLBCLK)}$	Cycle time, MLB_CLK	2048FS	9.77		ns
			4096FS	9.77		ns
2	$t_{w(MLBCLKH)}$	Pulse duration, MLB_CLK high	2048FS	4.64		ns
			4096FS	4.64		ns
3	$t_{w(MLBCLKL)}$	Pulse duration, MLB_CLK low	2048FS	4.64		ns
			4096FS	4.64		ns

(1) The reference points for the rise and fall transitions are measured at at 20%/80% of Vin+/-

MLB Timing Requirements for Receive Data - 6-pin

(1)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
10	tsu(DATx-CLKxH)	Setup time, MLBP_DATx/ MLBP_SIGx input valid before MLBP_CLKx rising	2048FS	1		ns
			4096FS	$0.5 – n^{(2)} \times P^{(1)} / 2$		ns
11	$t_{h(CLKxH-DATx)}$	Hold time, MLBP_DATx/MLBP_SIGx input valid after MLBP_CLKx rising	2048FS	0.6		ns
			4096FS	$0.6 + n^{(2)} \times P^{(1)} / 2$		ns

(1) P = MLBCLKx period
(2) n = 0 or 1, corresponding to two captures per clock cycle

MLB Switching Characteristics - 6-Pin

NO.	PARAMETER	DESCRIPTION	BUFFER TYPE	MIN	MAX	UNIT
13	$t_{d(CLKxH-DATxV)}$	Delay time, MLBPCLKxH rising to MLB_DATx/MLB_SIGx valid	2048FS	0.6	5	ns
			4096FS	$0.6 + n^{(2)} \times P^{(1)} / 2$	$2.5 + n^{(2)} \times P^{(1)} / 2$	ns
14	$t_{dis(CLKPH-DATPZ)}$	Disable time, MLBPCLKxH rising to MLBP_DATx/MLBPSIGx High-Z	2048FS	0.6	7	ns
			4096FS	$0.6 + n^{(2)} \times P^{(1)} / 2$	$3.5 + n^{(2)} \times P^{(1)} / 2$	ns

(1) P = MLBCLKx period
(2) n = 0 or 1, corresponding to two captures per clock cycle

6.12.5.13 MMCSD

The MMCSD Host Controller provides an interface to embedded Multi-Media Card (MMC), Secure Digital (SD), and Secure Digital IO (SDIO) devices. The MMCSD Host Controller deals with MMC/SD/SDIO protocol at transmission level, data packing, adding cyclic redundancy checks (CRCs), start/end bit insertion, and checking for syntactical correctness.

For more details about MMCSD interfaces, see the MMC0 subsection within *Signal Descriptions* and *Detailed Description* sections.

Note

Some operating modes require software configuration of the MMC DLL delay settings, as shown in table *MMC0 DLL Delay Mapping for SD/SDIO Timing Modes* and table *MMC0 DLL Delay Mapping for eMMC Timing Modes*.

The modes which show a value of "Tuning" in the ITAPDLYSEL column require a tuning algorithm to be used for optimizing input timing. Refer to the MMCSD Programming Guide in the device TRM for more information on the tuning algorithm and configuration of input delays required to optimize input timing.

For more information, see *Multi-Media Card/Secure Digital (MMCSD) Interface* section in *Peripherals* chapter in the device TRM.

6.12.5.13.1 MMC0 - eMMC/SDIO Interface

MMC0 interface is compliant with the SD Host Controller Standard Specification 4.10 and SD Physical Layer Specification v3.01 as well as SDIO Specification v3.00 and it supports the following SD Card applications:

- Default speed
- High Speed
- UHS-I SDR12
- UHS-I SDR25
- UHS-I SDR50
- UHS-I DDR50
- UHS-I SDR104

MMC0 interface is compliant with the JEDEC eMMC electrical standard v5.1 (JESD84-B51) and the interface supports the following eMMC applications:

- Legacy SDR
- High Speed SDR
- High Speed DDR
- HS200

MMC0 DLL Delay Mapping for SD/SDIO Timing Modes

Register Name		MMCSDn_PHY_CTRL_4_REG				MMCSDn_PHY_CTRL_5_REG	MMCSDn_HOST_CONTROL1
Bit Field		[20]	[16:12]	[8]	[4:0]	[2:0]	[2]
Bit Field Name		OTAPDLYENA	OTAPDLYSEL	ITAPDLYENA	ITAPDLYSEL	CLKBUFSEL	HIGH_SPEED_ENA
Mode	Description	Output Delay Enable	Delay Value	Input Delay Enable	Input Delay Value	Delay Buffer Duration	High Speed Enable
Default Speed	4-bit PHY operating in 3.3V, 25MHz	0x1	0x0	0x1	0x0	0x7	0x0
High Speed	4-bit PHY operating in 3.3V, 50MHz	0x1	0x0	0x1	0x0	0x7	0x0

Register Name		MMCSDn_PHY_CTRL_4_REG				MMCSDn_PHY_CTRL_5_REG	MMCSDn_HOST_CONTROL1
Bit Field		[20]	[16:12]	[8]	[4:0]	[2:0]	[2]
Bit Field Name		OTAPDLYENA	OTAPDLYSEL	ITAPDLYENA	ITAPDLYSEL	CLKBUFSEL	HIGH_SPEED_ENA
Mode	Description	Output Delay Enable	Delay Value	Input Delay Enable	Input Delay Value	Delay Buffer Duration	High Speed Enable
UHS-I SDR12	4-bit PHY operating in 1.8V, 25MHz	0x1	0xF	0x1	0x0	0x7	0x1
UHS-I SDR25	4-bit PHY operating in 1.8V, 50MHz	0x1	0xF	0x1	0x0	0x7	0x1
UHS-I SDR50	4-bit PHY operating in 1.8V, 100MHz	0x1	0xC	0x1	Tuning(1)	0x7	0x1
UHS-I DDR50	4-bit PHY operating in 1.8V, 50MHz	0x1	0x9	0x1	Tuning(1)	0x7	0x1
UHS-I SDR104	4-bit PHY operating in 1.8V, 200MHz	0x1	0x6	0x1	Tuning(1)	0x7	0x1

(1) Tuning means this mode requires a tuning algorithm to be used for optimal input timing

MMC0 DLL Delay Mapping for eMMC Timing Modes

Register Name		MMCSDn_PHY_CTRL_4_REG				MMCSDn_PHY_CTRL_5_REG	MMCSDn_HOST_CONTROL1
Bit Field		[20]	[16:12]	[8]	[4:0]	[2:0]	[2]
Bit Field Name		OTAPDLYENA	OTAPDLYSEL	ITAPDLYENA	ITAPDLYSEL	CLKBUFSEL	HIGH_SPEED_ENA
Mode	Description	Output Delay Enable	Delay Value	Input Delay Enable	Input Delay Value	Delay Buffer Duration	High Speed Enable
Legacy SDR	8-bit PHY operating in 1.8V, 3.3V 25MHz	0x1	0x0	0x0	NA(1)	0x7	0x0
High Speed SDR	8-bit PHY operating in 1.8V, 3.3V 50MHz	0x1	0x0	0x0	NA(1)	0x7	0x0
High Speed DDR	8-bit PHY operating in 1.8V, 3.3V 40MHz	0x1	0x15	0x1	0x2	0x7	0x1
HS200	8-bit PHY operating in 1.8V, 200MHz	0x1	0x6	0x1	Tuning(2)	0x7	0x1

(1) NA means Not Applicable
(2) Tuning means this mode requires a tuning algorithm to be used for optimal input timing

MMC Timing Conditions

PARAMETER	MODE	MIN	MAX	UNIT
INPUT CONDITIONS				

PARAMETER		MODE	MIN	MAX	UNIT
SR_I	Input Slew Rate	Legacy SDR 3.3 V, Default Speed High Speed SDR 3.3 V Default Speed andHigh Speed	0.69	2.06	V/ns
		Legacy SDR 1.8V UHS-I SDR12	0.14	1.44	V/ns
		High Speed SDR 1.8V UHS-I SDR25	0.3	1.34	V/ns
		UHS-I DDR50	1	2	V/ns
OUTPUT CONDITIONS					
C_L	Output Load Capacitance	HS200, UHS-I SDR104	1	10	pF
		All other modes	1	12	pF

MMC Timing Requirements - 3.3V Legacy SDR Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
LSDR1	$t_{su(cmdV-clkH)}$	Setup time, MMC0_CMD valid before MMC0_CLK rising edge	2.15		ns
LSDR2	$t_{h(clkH-cmdV)}$	Hold time, MMC0_CMD valid after MMC0_CLK rising edge	1.67		ns
LSDR3	$t_{su(dV-clkH)}$	Setup time, MMC0_DAT[7:0] valid before MMC0_CLK rising edge	2.15		ns
LSDR4	$t_{h(clkH-dV)}$	hold time, MMC0_DAT[7:0] valid after MMC0_CLK rising edge	1.67		ns

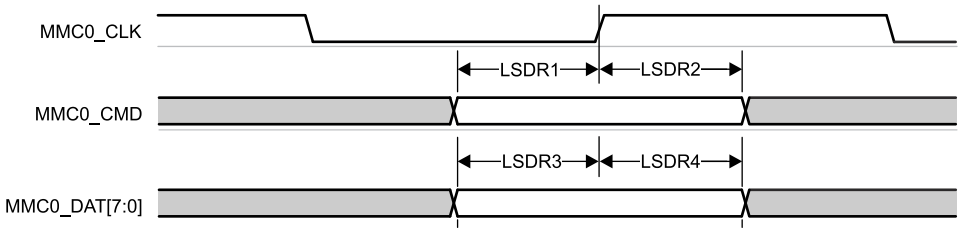


Figure 6-43. MMC0 – Legacy SDR – Receive Mode

MMC Switching Characteristics - 3.3V Legacy SDR Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC_CLK		25	MHz
LSDR5	$t_{c(clk)}$	Cycle time, MMC_CLK		40	ns
LSDR6	$t_{w(clkH)}$	Pulse duration, MMC_CLK high	18.7		ns
LSDR7	$t_{w(clkL)}$	Pulse duration, MMC_CLK low	18.7		ns
LSDR8	$t_{d(clkL-cmdV)}$	Delay time, MMC_CLK falling edge to MMC_CMD transition	–1.8	2.2	ns
LSDR9	$t_{d(clkL-dV)}$	Delay time, MMC_CLK falling edge to MMC_DAT[7:0] transition	–1.8	2.2	ns

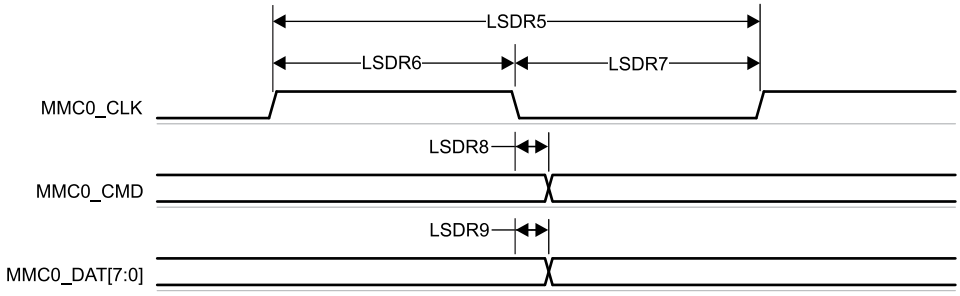


Figure 6-44. MMC0 – Legacy SDR – Transmit Mode

MMC Timing Requirements - 3.3V High Speed SDR Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
HSSDR1	$t_{su(cmdV-clkH)}$	Setup time, MMC_CMD valid before MMC_CLK rising edge	2.24		ns
HSSDR2	$t_{h(clkH-cmdV)}$	Hold time, MMC_CMD valid after MMC_CLK rising edge	1.66		ns
HSSDR3	$t_{su(dV-clkH)}$	Setup time, MMC_DAT[7:0] valid before MMC_CLK rising edge	2.24		ns
HSSDR4	$t_{h(clkH-dV)}$	Hold time, MMC_DAT[7:0] valid after MMC_CLK rising edge	1.66		ns

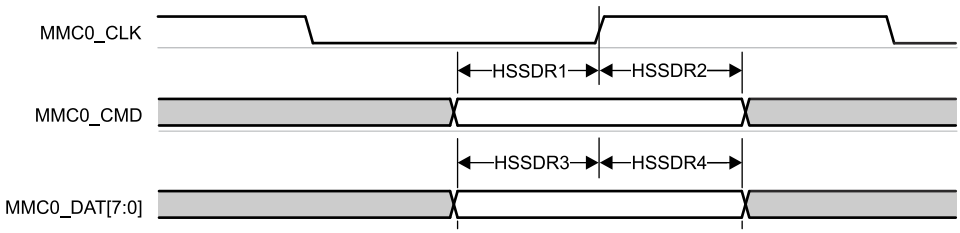


Figure 6-45. MMC0 – High Speed SDR Mode – Receive Mode

MMC Switching Characteristics - 3.3V High Speed SDR Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC_CLK		50	MHz
HSSDR5	$t_{c(clk)}$	Operating period, MMC_CLK	20		ns
HSSDR6	$t_{w(clkH)}$	Pulse duration, MMC_CLK high	9.2		ns
HSSDR7	$t_{w(clkL)}$	Pulse duration, MMC_CLK low	9.2		ns
HSSDR8	$t_{d(clkL-cmdV)}$	Delay time, MMC_CLK falling edge to MMC_CMD transition	–1.8	2.2	ns
HSSDR9	$t_{d(clkL-dV)}$	Delay time, MMC_CLK falling edge to MMC_DAT[7:0] transition	–1.8	2.2	ns

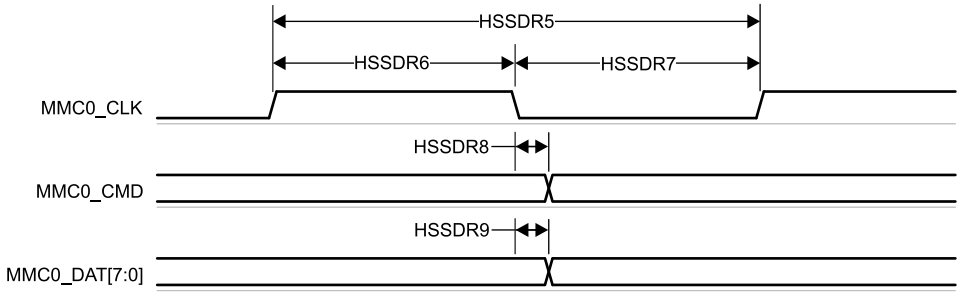


Figure 6-46. MMC0 – High Speed SDR Mode – Transmit Mode

MMC Timing Requirements - 1.8V Legacy SDR, UHS-I SDR12 Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
LSDR1	$t_{su(cmdV-clkH)}$	Setup time, MMC_CMD valid before MMC_CLK rising edge	4.2		ns
LSDR2	$t_{h(clkH-cmdV)}$	Hold time, MMC_CMD valid after MMC_CLK rising edge	0.87		ns
LSDR3	$t_{su(dV-clkH)}$	Setup time, MMC_DAT[7:0] valid before MMC_CLK rising edge	4.2		ns
LSDR4	$t_{h(clkH-dV)}$	Hold time, MMC_DAT[7:0] valid after MMC_CLK rising edge	0.87		ns

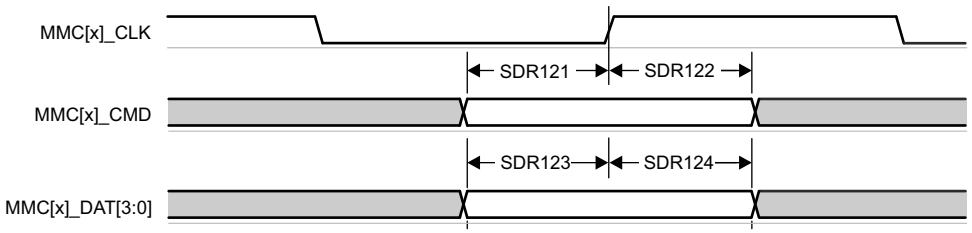


Figure 6-47. MMC0 – UHS-I SDR12 – Receive Mode

MMC Switching Characteristics - 1.8V Legacy SDR, UHS-I SDR12 Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC_CLK			25	MHz
LSDR5	$t_{c(clk)}$	Operating period, MMC_CLK		40		ns
LSDR6	$t_{w(clkH)}$	Pulse duration, MMC_CLK high		18.7		ns
LSDR7	$t_{w(clkL)}$	Pulse duration, MMC_CLK low		18.7		ns
LSDR8	$t_{d(clkL-cmdV)}$	Delay time, MMC_CLK falling edge to MMC_CMD transition	1.8V Legacy SDR	–2.1	2.1	ns
			SDR12	1.5	8.6	ns
LSDR9	$t_{d(clkL-dV)}$	Delay time, MMC_CLK falling edge to MMC_DAT[3:0] transition	1.8V Legacy SDR	–2.1	2.1	ns
			SDR12	1.5	8.6	ns

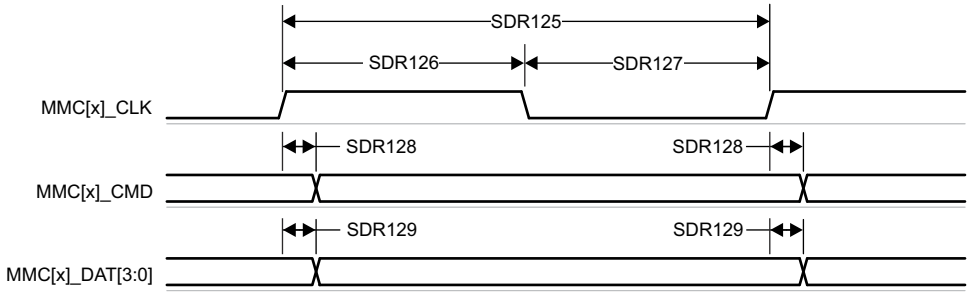


Figure 6-48. MMC0 – UHS-I SDR12 – Transmit Mode

MMC Timing Requirements - 1.8V High Speed SDR, UHS-I SDR25 Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
HSSDR1	$t_{su(cmdV-clkH)}$	Setup time, MMC_CMD valid before MMC_CLK rising edge	2.15		ns
HSSDR2	$t_{h(clkH-cmdV)}$	Hold time, MMC_CMD valid after MMC_CLK rising edge	1.27		ns
HSSDR3	$t_{su(dV-clkH)}$	Setup time, MMC_DAT[7:0] valid before MMC_CLK rising edge	2.15		ns
HSSDR4	$t_{h(clkH-dV)}$	Hold time, MMC_DAT[7:0] valid after MMC_CLK rising edge	1.27		ns

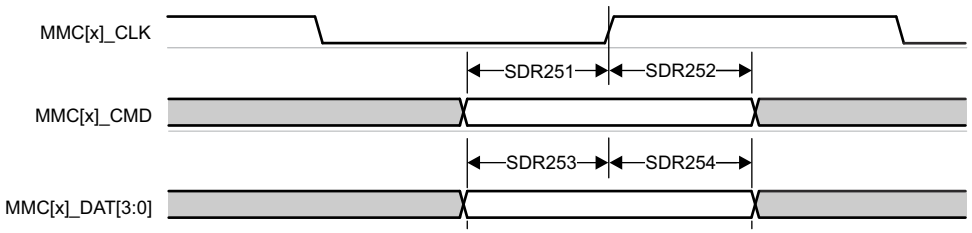


Figure 6-49. MMC0 – UHS-I SDR25 – Receive Mode

MMC Switching Characteristics - 1.8V High Speed SDR, UHS-I SDR25 Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC_CLK			50	MHz
HSSDR5	$t_{c(clk)}$	Operating period, MMC_CLK		20		ns
HSSDR6	$t_{w(clkH)}$	Pulse duration, MMC_CLK high		9.2		ns
HSSDR7	$t_{w(clkL)}$	Pulse duration, MMC_CLK low		9.2		ns
HSSDR8	$t_{d(clkL-cmdV)}$	Delay time, MMC_CLK falling edge to MMC_CMD transition	1.8V High Speed SDR	–1.55	3.05	ns
			SDR25	2.4	8.1	ns
HSSDR9	$t_{d(clkL-dV)}$	Delay time, MMC_CLK falling edge to MMC_DAT[3:0] transition	1.8V High Speed SDR	–1.55	3.05	ns
			SDR25	2.4	8.1	ns

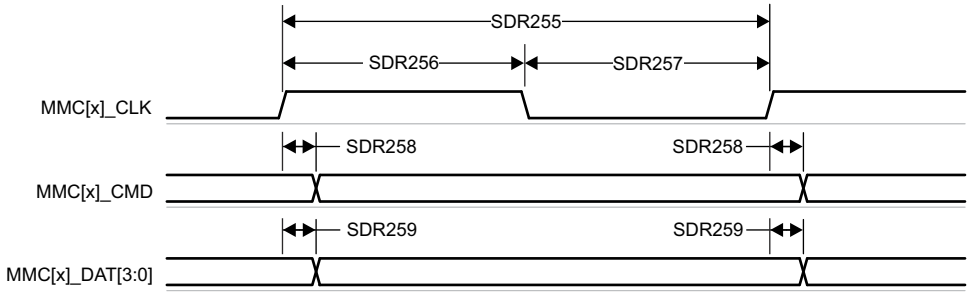


Figure 6-50. MMC0 – UHS-I SDR25 – Transmit Mode

MMC Switching Characteristics - UHS-I SDR50 Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC_CLK		100	MHz
SDR505	$t_{c(clk)}$	Operating period, MMC_CLK	10		ns
SDR506	$t_{w(clkH)}$	Pulse duration, MMC_CLK high	4.45		ns
SDR507	$t_{w(clkL)}$	Pulse duration, MMC_CLK low	4.45		ns
SDR508	$t_{d(clkL-cmdV)}$	Delay time, MMC_CLK falling edge to MMC_CMD transition	1.2	6.35	ns
SDR509	$t_{d(clkL-dV)}$	Delay time, MMC_CLK falling edge to MMC_DAT[7:0] transition	1.2	6.35	ns

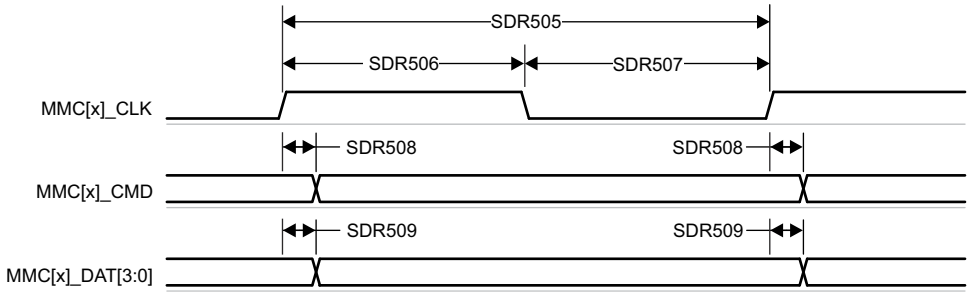


Figure 6-51. MMC0 – UHS-I SDR50 – Transmit Mode

MMC Switching Characteristics - UHS-I DDR50 Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC_CLK		50	MHz
HSSDR5	$t_{c(clk)}$	Operating period, MMC_CLK	20		ns
HSSDR6	$t_{w(clkH)}$	Pulse duration, MMC_CLK high	9.2		ns
HSSDR7	$t_{w(clkL)}$	Pulse duration, MMC_CLK low	9.2		ns
HSSDR8	$t_{d(clkL-cmdV)}$	Delay time, MMC_CLK falling edge to MMC_CMD transition	1.12	6.43	ns
HSSDR9	$t_{d(clkL-dV)}$	Delay time, MMC_CLK falling edge to MMC_DAT[7:0] transition	1.12	6.43	ns

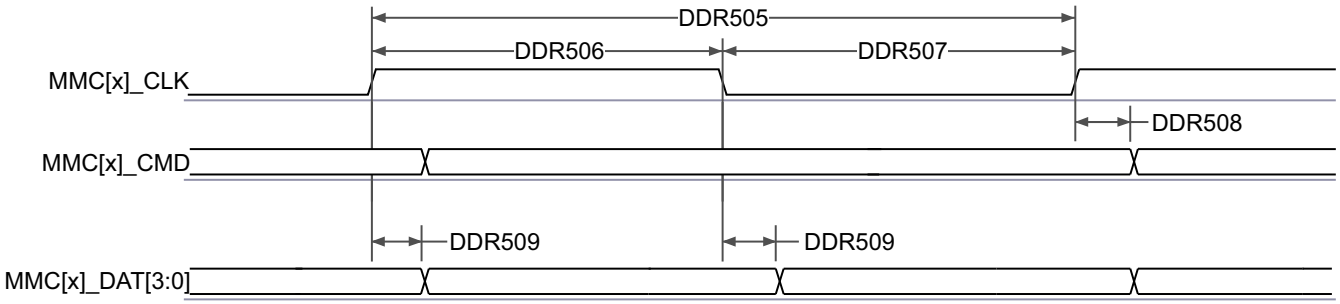


Figure 6-52. MMC0 – UHS-I DDR50 – Transmit Mode

MMC Switching Characteristics - HS200 Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC_CLK		200	MHz
HS2005	$t_{c(clk)}$	Operating period, MMC_CLK	5		ns
HS2006	$t_{w(clkH)}$	Pulse duration, MMC_CLK high	2.12		ns
HS2007	$t_{w(clkL)}$	Pulse duration, MMC_CLK low	2.12		ns
HS2008	$t_{d(clkL-cmdV)}$	Delay time, MMC_CLK falling edge to MMC_CMD transition	1.07	3.21	ns
HS2009	$t_{d(clkL-dV)}$	Delay time, MMC_CLK falling edge to MMC_DAT[7:0] transition	1.07	3.21	ns

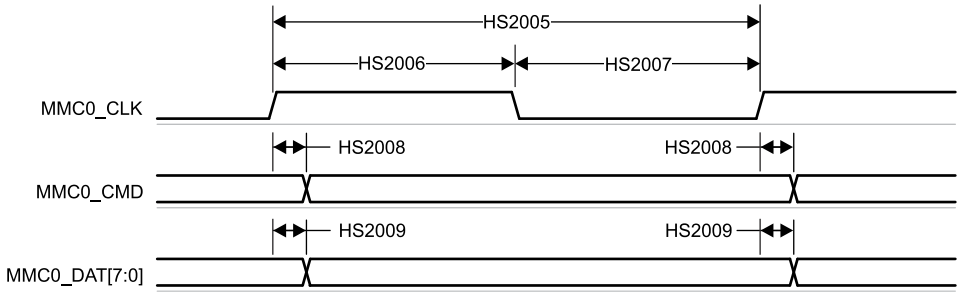


Figure 6-53. MMC0 – HS200 Mode – Transmit Mode

6.12.5.14 OSPI

OSPI0 offers two data capture modes, PHY mode and Tap mode.

PHY mode uses an internal reference clock to transmit and receive data via a DLL based PHY, where each reference clock cycle produces a single cycle of OSPI0_CLK for Single Data Rate (SDR) transfers or a half cycle of OSPI0_CLK for Double Data Rate (DDR) transfers. PHY mode supports four clocking topologies for the receive data capture clock. Internal PHY Loopback - uses the internal reference clock as the PHY receive data capture clock. Internal Pad Loopback - uses OSPI0_LBCLKO looped back into the PHY from the OSPI0_LBCLKO pin as the PHY receive data capture clock. External Board Loopback - uses OSPI0_LBCLKO looped back into the PHY from the OSPI0_DQS pin as the PHY receive data capture clock. DQS - uses the DQS output from the attached device as the PHY receive data capture clock. SDR transfers are not supported when using the Internal Pad Loopback and DQS clocking topologies. DDR transfers are not supported when using the Internal PHY Loopback or Internal Pad Loopback clocking topologies.

Tap mode uses an internal reference clock with selectable taps to adjusted data transmit and receive capture delays relative to OSPI0_CLK, which is a divide by 4 of the internal reference clock for SDR transfers or a divide by 8 of the internal reference clock for DDR transfers. Tap mode only supports one clocking topology for the receive data capture clock. No Loopback - uses the internal reference clock as the Tap receive data capture clock. This clocking topology supports a maximum internal reference clock rate of 200 MHz, which produces an OSPI0_CLK rate up to 50 MHz for SDR mode or 25 MHz for DDR mode.

For more information, see *Octal Serial Peripheral Interface (OSPI)* section in *Peripherals* chapter in the device TRM.

For more details about features and additional description information on the device Octal Serial Peripheral Interface, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

OSPI Timing Conditions

PARAMETER		MODE	MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate		3	6	V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance		3	10	pF
PCB CONNECTIVITY REQUIREMENTS					
$t_{d(Trace\ Delay)}$	Propagation delay of OSPI0_CLK trace	No Loopback Internal PHY Loopback Internal Pad Loopback		450	ps
	Propagation delay of OSPI0_DQS trace	DQS	L(1) - 30	L(1) + 30	ps
	Propagation delay of OSPI0_LBCLKO trace	External Board Loopback	2L(1) - 30	2L(1) + 30	ps
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch of OSPI0_D[7:0] and OSPI0_CSn[1:0] relative to OSPI0_CLK	All modes		60	ps

(1) L = Propagation delay of OSPI0_CLK trace

6.12.5.14.1 OSPI0 PHY Mode

6.12.5.14.1.1 OSPI0 With PHY Data Training

Read and write data valid windows shift due to variation in process, voltage, temperature, and operating frequency. A data training method can be implemented to dynamically configure read and write timing. Implementing data training enables proper operation across temperature with a specific process, voltage, and frequency operating condition, while achieving a higher operating frequency.

Data transmit and receive timing parameters are not defined for the data training use case since the parameters are dynamically adjusted based on the operating condition.

OSPI DLL Delay Mapping for PHY Data Training

MODE	OSPI_PHY_CONFIGURATION_REG BIT FIELD	DELAY VALUE
Transmit		
All modes	PHY_CONFIG_TX_DLL_DELAY_FLD	(1)
Receive		
All modes	PHY_CONFIG_RX_DLL_DELAY_FLD	(2)

(1) Transmit DLL delay value determined by training software
(2) Receive DLL delay value determined by training software

OSPI Timing Requirements - PHY Data Training

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
O15	$t_{su(D-DQS)}$	Setup time, OSPI0_D[7:0] valid before active OSPI0_DQS edge	DDR with DQS	(1)		ns
O16	$t_{h(DQS-D)}$	Hold time, OSPI0_D[7:0] valid after active OSPI0_DQS edge	DDR with DQS	(1)		ns
O21	$t_{su(D-DQS)}$	Setup time, OSPI0_D[7:0] valid before active OSPI0_DQS edge	SDR with External Board Loopback	(1)		ns
O22	$t_{h(DQS-D)}$	Hold time, OSPI0_D[7:0] valid after active OSPI0_DQS edge	SDR with External Board Loopback	(1)		ns
	t_{DVW}	Data valid window (O15 + O16)	1.8V, DDR with DQS	1.6		ns
			3.3V DDR with DQS	2.2		ns
		Data valid window (O21 + O22)	1.8V, SDR with External Board Loopback	2.3		ns
			3.3V SDR with External Board Loopback	2.9		ns

(1) Minimum setup and hold time requirements for OSPI0_D[7:0] inputs are not defined when Data Training is used to find the optimum data valid window.

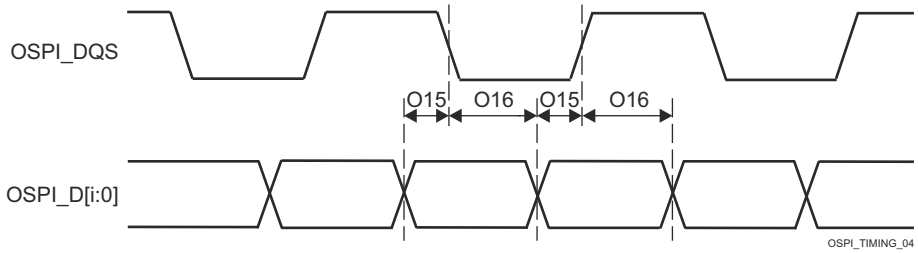


Figure 6-54. OSPI0 Timing Requirements – PHY Data Training, DDR with DQS

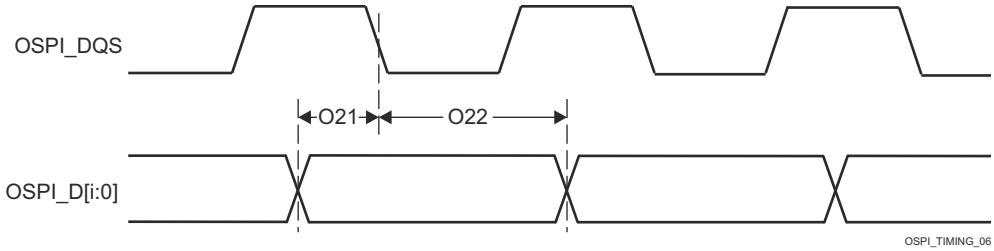


Figure 6-55. OSPI0 Timing Requirements – PHY Data Training, SDR with External Board Loopback

OSPI Switching Characteristics - PHY Data Training

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
O1	$t_{c(CLK)}$	Cycle time, OSPI0_CLK	1.8V, SDR, DDR	6	10	ns
			3.3V, SDR, DDR	7.5	10	ns
O2	$t_{w(CLKL)}$	Pulse duration, OSPI0_CLK low	SDR, DDR	0.475P(1) – 0.3		ns
O3	$t_{w(CLKH)}$	Pulse duration, OSPI0_CLK high	SDR, DDR	0.475P(1) – 0.3		ns
O4	$t_{d(CSn-CLK)}$	Delay time, OSPI0_CSn[1:0] active edge to OSPI0_CLK rising edge	SDR, DDR	0.475P(1) + (0.975 × M(2) × R(4)) + 0.04TD(5) – 1	0.525P(1) + (1.025 × M(2) × R(4)) + 0.11TD(5) + 1	ns
O5	$t_{d(CLK-CSn)}$	Delay time, OSPI0_CLK rising edge to OSPI0_CSn[1:0] inactive edge	SDR, DDR	0.475P(1) + (0.975 × N(3) × R(4)) + 0.04TD(5) – 1	0.525P(1) + (1.025 × N(3) × R(4)) + 0.11TD(5) + 1	ns
O6	$t_{d(CLK-D)}$	Delay time, OSPI0_CLK active edge to OSPI0_D[7:0] transition	SDR, DDR	(6)	(6)	ns
	t_{DIVW}	Data Invalid Window (O6 Max – Min)	SDR, DDR		1.6	ns

(1) P = OSPI0_CLK cycle time = SCLK period in ns
(2) M = OSPI_DEV_DELAY_REG[D_INIT_FLD]
(3) N = OSPI_DEV_DELAY_REG[D_AFTER_FLD]
(4) R = REFCLK cycle time in ns
(5) TD = PHY_CONFIG_TX_DLL_DELAY_FLD
(6) Minimum and maximum delay times for OSPI0_D[7:0] outputs are not defined when Data Training is used to find the optimum data valid window.

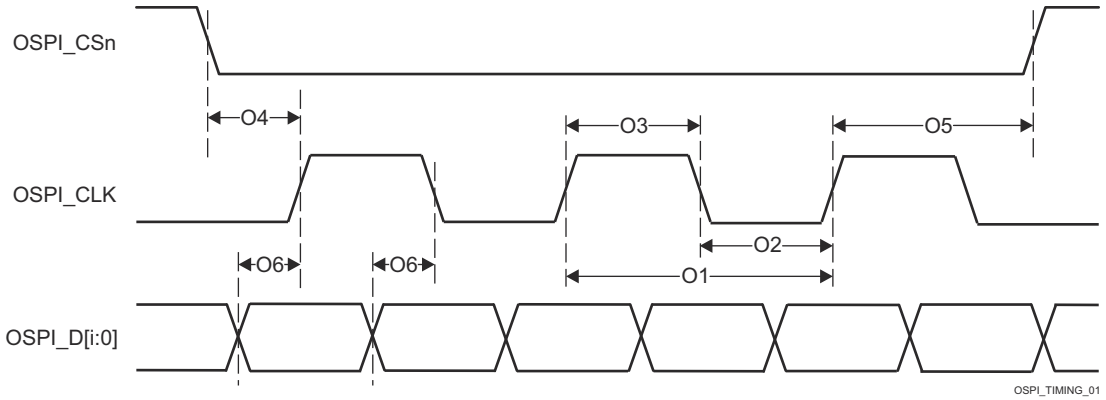


Figure 6-56. OSPI0 Switching Characteristics – PHY DDR Data Training

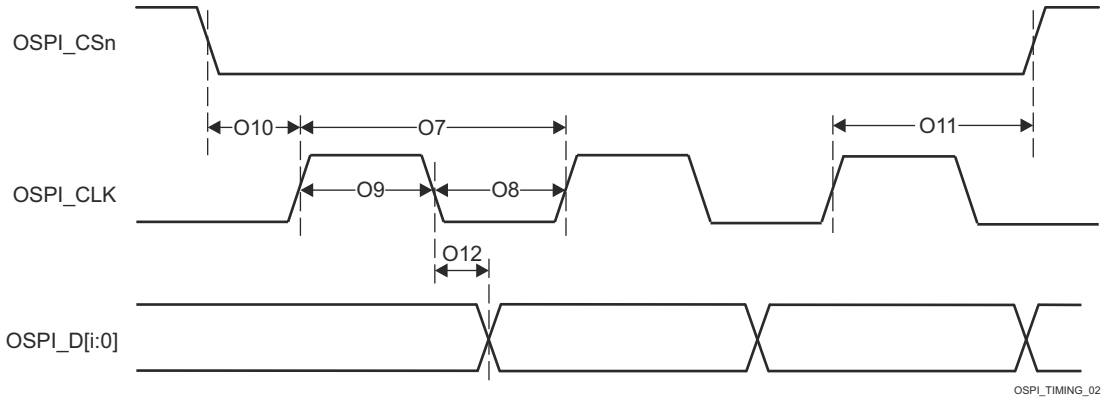


Figure 6-57. OSPI0 Switching Characteristics – PHY SDR Data Training

6.12.5.14.1.2 OSPI0 Without Data Training

Note

Timing parameters defined in this section are only applicable when data training is not implemented and DLL delays are configured as described in OSPI0 PHY SDR Timing.

6.12.5.14.1.2.1 OSPI0 PHY SDR Timing

OSPI DLL Delay Mapping for PHY SDR Timing Modes

MODE	OSPI_PHY_CONFIGURATION_REG BIT FIELD	DELAY VALUE
Transmit		
All modes	PHY_CONFIG_TX_DLL_DELAY_FLD	0x0
Receive		
All modes	PHY_CONFIG_RX_DLL_DELAY_FLD	0x0

OSPI Timing Requirements - PHY SDR Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
O19	$t_{su(D-CLK)}$	Setup time, OSPI0_D[7:0] valid before active OSPI0_CLK edge	1.8V, SDR with Internal PHY Loopback	4.8		ns
			3.3V, SDR with Internal PHY Loopback	5.19		ns
O20	$t_{h(CLK-D)}$	Hold time, OSPI0_D[7:0] valid after active OSPI0_CLK edge	1.8V, SDR with Internal PHY Loopback	–0.5		ns
			3.3V, SDR with Internal PHY Loopback	–0.5		ns
O21	$t_{su(D-LBCLK)}$	Setup time, OSPI0_D[7:0] valid before active OSPI0_DQS edge	1.8V, SDR with External Board Loopback	0.6		ns
			3.3V, SDR with External Board Loopback	0.9		ns
O22	$t_{h(LBCLK-D)}$	Hold time, OSPI0_D[7:0] valid after active OSPI0_DQS edge	1.8V, SDR with External Board Loopback	1.7		ns
			3.3V, SDR with External Board Loopback	2.0		ns

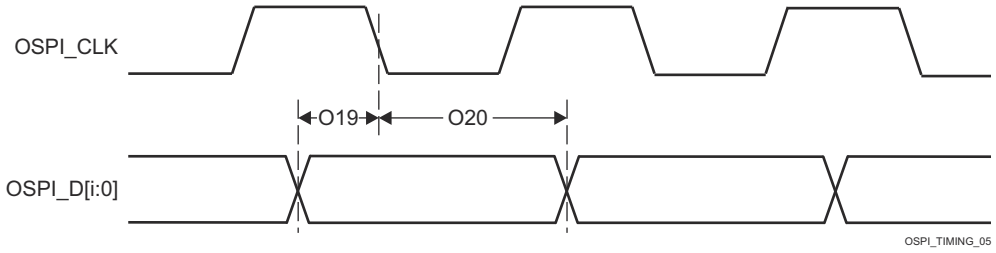


Figure 6-58. OSPI0 Timing Requirements – PHY SDR with Internal PHY Loopback

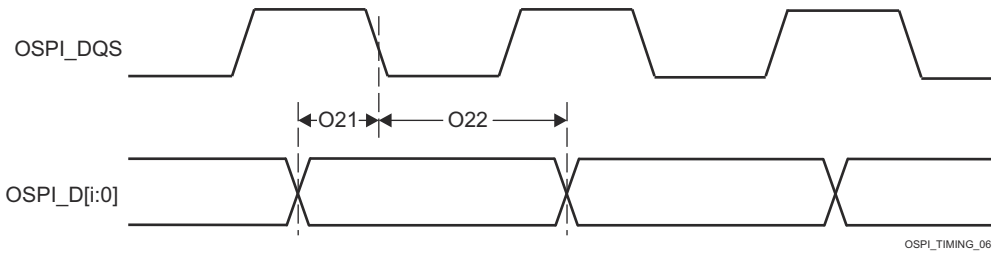


Figure 6-59. OSPI0 Timing Requirements – PHY SDR with External Board Loopback

OSPI Switching Characteristics - PHY SDR Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
O7	$t_{c(CLK)}$	Cycle time, OSPI0_CLK	1.8V	7		ns
			3.3V	6.03		ns
O8	$t_{w(CLKL)}$	Pulse duration, OSPI0_CLK low		0.475P(1) – 0.3		ns
O9	$t_{w(CLKH)}$	Pulse duration, OSPI0_CLK high		0.475P(1) – 0.3		ns
O10	$t_{d(CSn-CLK)}$	Delay time, OSPI0_CSn[1:0] active edge to OSPI0_CLK rising edge		0.475P(1) + 0.975 × M(2) × R(4) – 1	0.525P(1) + 1.025 × M(2) × R(4) + 1	ns
O11	$t_{d(CLK-CSn)}$	Delay time, OSPI0_CLK rising edge to OSPI0_CSn[1:0] inactive edge		0.475P(1) + 0.975 × N(3) × R(4) – 1	0.525P(1) + 1.025 × N(3) × R(4) + 1	ns
O12	$t_{d(CLK-D)}$	Delay time, OSPI0_CLK active edge to OSPI0_D[7:0] transition	1.8V	–1.16	1.25	ns
			3.3V	–1.33	1.51	ns

(1) P = CLK cycle time = SCLK period in ns
(2) M = OSPI_DEV_DELAY_REG[D_INIT_FLD]
(3) N = OSPI_DEV_DELAY_REG[D_AFTER_FLD]
(4) R = REFCLK cycle time in ns

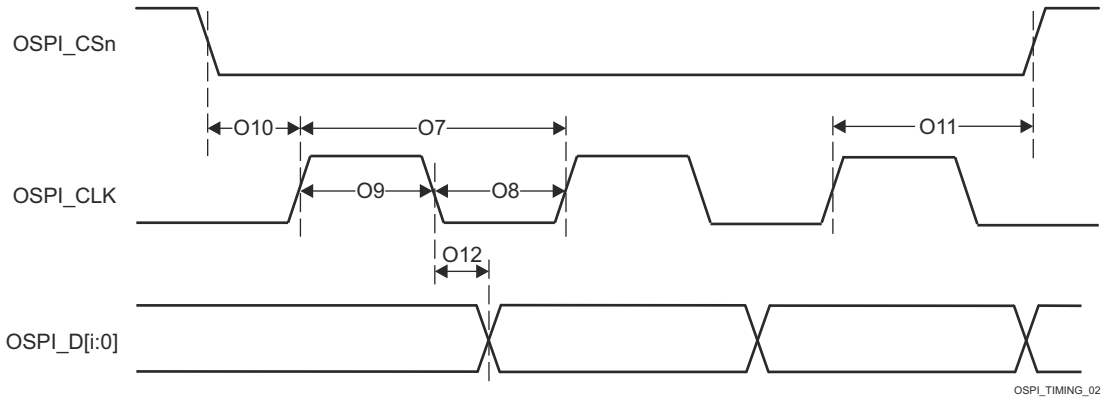


Figure 6-60. OSPI0 Switching Characteristics – PHY SDR

6.12.5.14.2 OSPI0 Tap Mode

6.12.5.14.2.1 OSPI0 Tap SDR Timing

OSPI Timing Requirements - Tap SDR Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
O19	$t_{su(D-CLK)}$	Setup time, OSPI0_D[7:0] valid before active OSPI0_CLK edge	No Loopback	15.4 – (0.975 × T(1) × R(2))		ns
O20	$t_{h(CLK-D)}$	Hold time, OSPI0_D[7:0] valid after active OSPI0_CLK edge	No Loopback	–4.3 + (0.975 × T(1) × R(2))		ns

(1) T = OSPI_RD_DATA_CAPTURE_REG[DELAY_FLD]

(2) R = REFCLK cycle time in ns

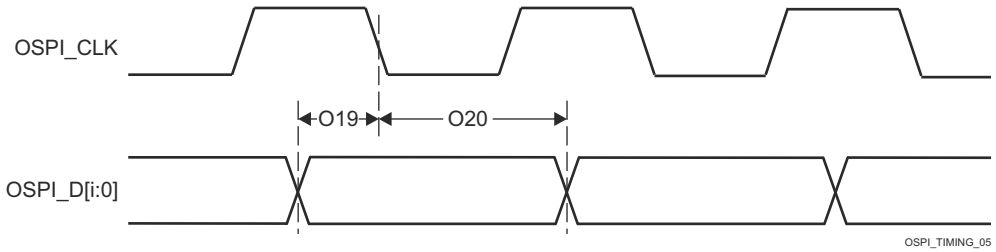


Figure 6-61. OSPI0 Timing Requirements – Tap SDR, No Loopback

OSPI Switching Characteristics - Tap SDR Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
O7	$t_{c(CLK)}$	Cycle time, OSPI0_CLK		20		ns
O8	$t_{w(CLKL)}$	Pulse duration, OSPI0_CLK low		0.475P(1) – 0.3		ns
O9	$t_{w(CLKH)}$	Pulse duration, OSPI0_CLK high		0.475P(1) – 0.3		ns
O10	$t_{d(CSn-CLK)}$	Delay time, OSPI0_CSn[1:0] active edge to OSPI0_CLK rising edge		0.475P(1) + (0.975 × M(2) × R(4)) – 1	0.525P(1) + (1.025 × M(2) × R(4)) + 1	ns
O11	$t_{d(CLK-CSn)}$	Delay time, OSPI0_CLK rising edge to OSPI0_CSn[1:0] inactive edge		0.475P(1) + (0.975 × N(3) × R(4)) – 1	0.525P(1) + (1.025 × N(3) × R(4)) + 1	ns
O12	$t_{d(CLK-D)}$	Delay time, OSPI0_CLK active edge to OSPI0_D[7:0] transition		–4.25	7.25	ns

(1) P = CLK cycle time = SCLK period in ns
(2) M = OSPI_DEV_DELAY_REG[D_INIT_FLD]
(3) N = OSPI_DEV_DELAY_REG[D_AFTER_FLD]
(4) R = REFCLK cycle time in ns

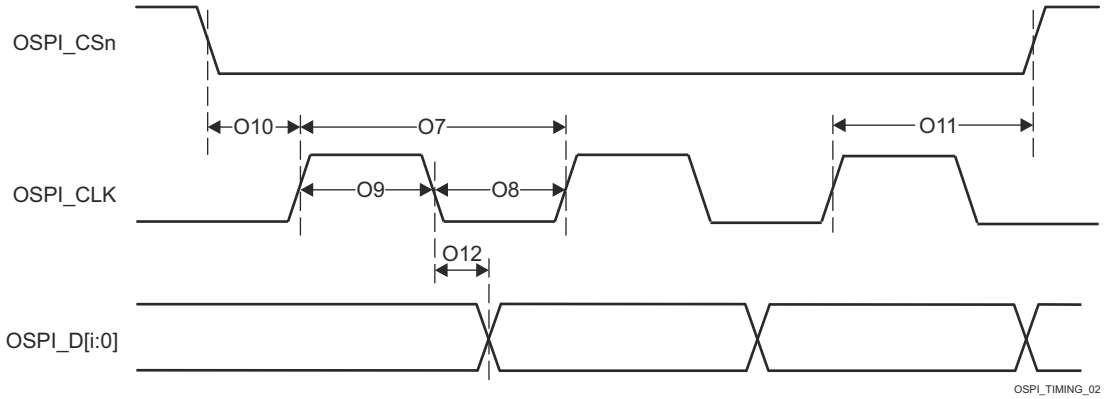


Figure 6-62. OSPI0 Switching Characteristics – Tap SDR, No Loopback

6.12.5.14.2.2 OSPI0 Tap DDR Timing

OSPI Timing Requirements - Tap DDR Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
O13	$t_{su(D-CLK)}$	Setup time, OSPI0_D[7:0] valid before active OSPI0_CLK edge	No Loopback	17.04 – (0.975 × T[1] × R[2])		ns
O14	$t_{h(CLK-D)}$	Hold time, OSPI0_D[7:0] valid after active OSPI0_CLK edge	No Loopback	–3.16 + (0.975 × T[1] × R[2])		ns

(1) T = OSPI_RD_DATA_CAPTURE_REG[DELAY_FLD]
(2) R = REFCLK cycle time in ns

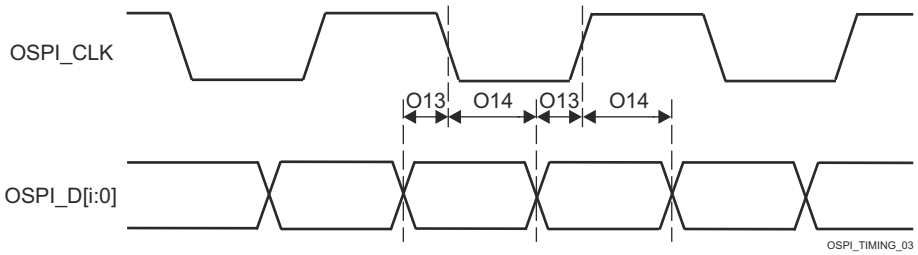


Figure 6-63. OSPI0 Timing Requirements – Tap DDR, No Loopback

OSPI Switching Characteristics - Tap DDR Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
O1	$t_{c(CLK)}$	Cycle time, OSPI0_CLK		40		ns
O2	$t_{w(CLKL)}$	Pulse duration, OSPI0_CLK low		0.475P[1] – 0.3		ns
O3	$t_{w(CLKH)}$	Pulse duration, OSPI0_CLK high		0.475P[1] – 0.3		ns
O4	$t_{d(CSn-CLK)}$	Delay time, OSPI0_CSn[1:0] active edge to OSPI0_CLK rising edge		0.475P[1] + (0.975 × M[2] × R[4]) – 1	0.525P[1] + (1.025 × M[2] × R[4]) + 1	ns
O5	$t_{d(CLK-CSn)}$	Delay time, OSPI0_CLK rising edge to OSPI0_CSn[1:0] inactive edge		0.475P[1] + (0.975 × N[3] × R[4]) – 1	0.525P[1] + (1.025 × N[3] × R[4]) + 1	ns
O6	$t_{d(CLK-D)}$	Delay time, OSPI0_CLK active edge to OSPI0_D[7:0] transition		–5.04 + (0.975 × T[5] × R[4]) – 0.525P[1]	3.64 + (1.025 × (T[5] + 1) × R[4]) – 0.475P[1]	ns

(1) P = CLK cycle time = SCLK period in ns
(2) M = OSPI_DEV_DELAY_REG[D_INIT_FLD]
(3) N = OSPI_DEV_DELAY_REG[D_AFTER_FLD]
(4) R = REFCLK cycle time in ns
(5) T = OSPI_RD_DATA_CAPTURE_REG[DDR_READ_DELAY_FLD]

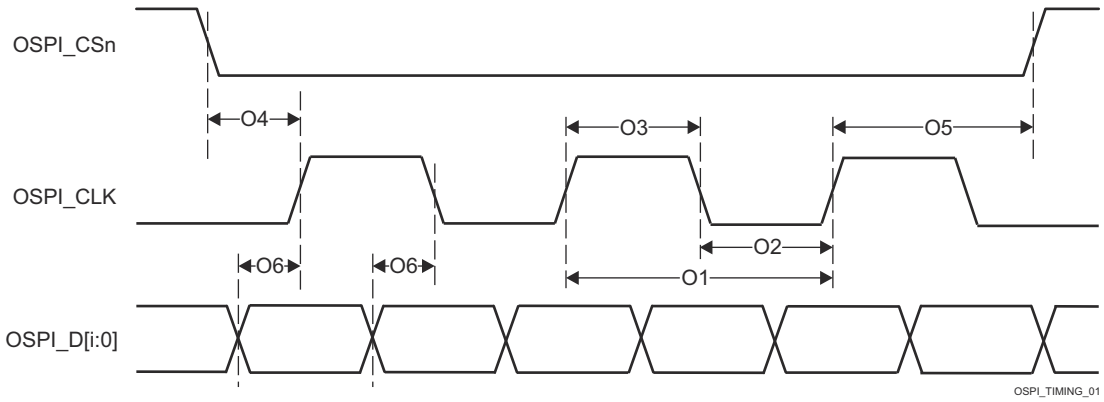


Figure 6-64. OSPI0 Switching Characteristics – Tap DDR, No Loopback

6.12.5.15 Timers

For more details about features and additional description information on the device Timers, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

For more information, see *Timers* section in *Peripherals* chapter in the device TRM.

Timer Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input Slew Rate	0.5	5	V/ns
OUTPUT CONDITIONS				
C_L	Output Load Capacitance	2	10	pF

Timer Timing Requirements

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
1	$t_{w(TINPH)}$	Pulse duration, high	2 + 4 × P(1)		ns
2	$t_{w(TINPL)}$	Pulse duration, low	2 + 4 × P(1)		ns

(1) P = functional clock period in ns.

Timer Switching Characteristics
(1)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
3	$t_{w(TOUTH)}$	Pulse duration, high	–2 + 4 × P(1)		ns
4	$t_{w(TOUTL)}$	Pulse duration, low	–2 + 4 × P(1)		ns

(1) P = functional clock period in ns

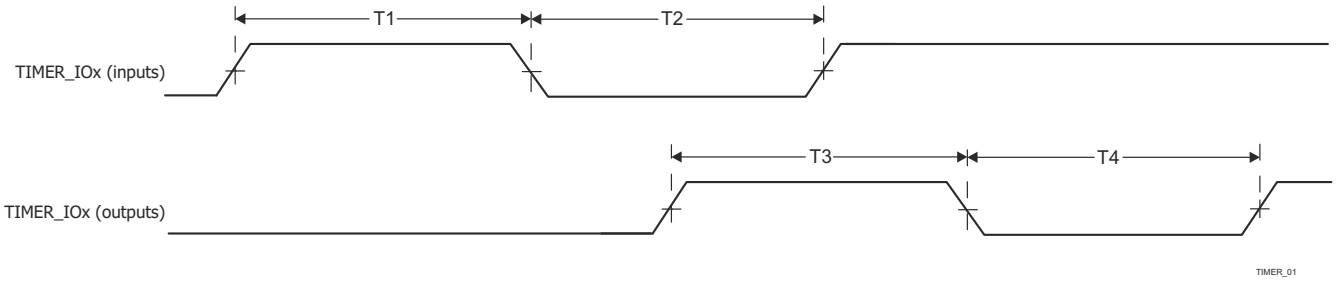


Figure 6-65. Timer Timing Requirements and Switching Characteristics

6.12.5.16 UART

For more details about features and additional description information on the device Universal Asynchronous Receiver Transmitter, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

For more information, see *Universal Asynchronous Receiver/Transmitter (UART)* section in *Peripherals* chapter in the device TRM.

UART Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input Slew Rate	0.5	5	V/ns
OUTPUT CONDITIONS				
C_L	Output Load Capacitance	1	30(1)	pF

(1) This value represents an absolute maximum load capacitance. As the UART baud rate increases, it may be necessary to reduce the load capacitance to a value less than this maximum limit to provide enough timing margin for the attached device. The output rise/fall times increase as capacitive load increases, which decreases the time data is valid for the receiver of the attached devices. Therefore, it is important to understand the minimum data valid time required by the attached device at the operating baud rate. Then use the device IBIS models to verify the actual load capacitance on the UART signals does not increase the rise/fall times beyond the point where the minimum data valid time of the attached device is violated.

UART Timing Requirements

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
4	$t_{w(RX)}$	Pulse width, receive data bit, high or low	0.95U(1) (2)	1.05U(1) (2)	ns
5	$t_{w(CTS)}$	Pulse width, receive start bit, high or low	0.95U(1) (2)		ns

(1) U = UART baud time = 1 / Programmed baud rate.
(2) This value defines the data valid time, where the input voltage is required to be above V_{IH} or below V_{IL}.

UART Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
	$f_{(baud)}$	Programmable baud rate for MAIN domain UARTs		12	Mbps
		Programmable baud rate for WKUP domain UARTs		3.7	
2	$t_{w(TX)}$	Pulse width, transmit data bit, high or low	U(1) – 2	U(1) + 2	ns
3	$t_{w(RTS)}$	Pulse width, transmit start bit, high or low	U(1) – 2		ns

(1) U = UART baud time = 1 / Programmed baud rate.

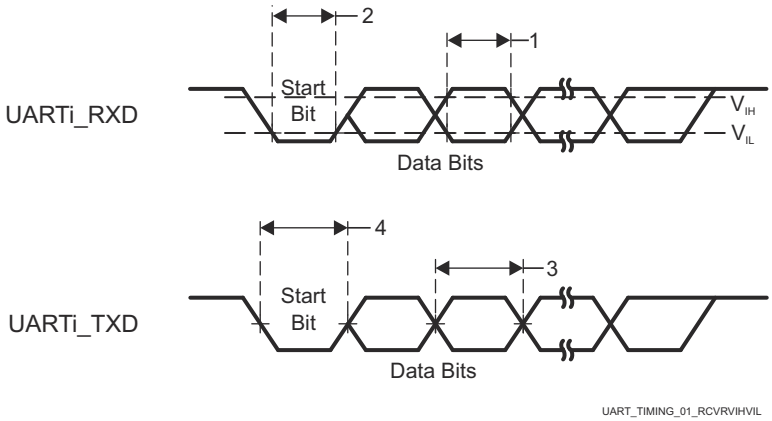


Figure 6-66. UART Timing Requirements and Switching Characteristics

6.12.5.17 USB

The USB 2.0 subsystem is compliant with the Universal Serial Bus (USB) Specification, revision 2.0. Refer to the specification for timing details.

For more details about features and additional description information on the device Universal Serial Bus Subsystem (USB), see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

7 Detailed Description

7.1 Overview

The AM275x processor from the Signal Processing Microcontroller family is targeted for audio applications needing high-performance Digital Signal Processing.

Key cores on the device include the ARM® Cortex®-R5F and C7000™ (“C7x”) scalar and vector DSP core from Texas Instruments, a dedicated Matrix Multiplication Accelerator (MMA), and Asynchronous Audio Sample Rate Converters (ASRC). All are protected by automotive grade safety and security hardware accelerators.

DSP Core Overview: the C7x core provides up to 40GFLOPS of DSP compute. The core achieves 4x to 8x or more performance compared to the previous generation C66x DSP core. Some of the key features includes:

- 256-bit fixed- and floating-point DSP vector core
- Single-cycle latency to access L2 memory via Streaming Engine
- Improved control code efficiency
- True 64-bit machine with 64-bit memory addressing and single-cycle 64-bit base arithmetic operations

Integration Overview: along with dual C7x DSP cores, the AM275 SoC integrates up to Quad Arm® Cortex®-R5F cores capable of running in dual lockstep mode or all independently. Integrated diagnostics and safety features support operations up to ASIL-B levels while the integrated security features protect data against modern day attacks. The AM275 device also offers a 2-port Gigabit Ethernet switch with Time-Sensitive Networking (TSN) to enable audio networking features such as Ethernet Audio Video Bridging (eAVB), while peripherals like the McASP enable multi-channel I2S and TDM Audio inputs and outputs. The device also includes two hardware Asynchronous Audio Sample Rate Converters (ASRCs) to convert audio sample rates on digital audio streams.

Note

For more information on features, subsystems, and architecture of superset device System on Chip (SoC), see the device TRM.

7.2 Processor Subsystems

7.2.1 Arm Cortex-R5F Subsystem

The R5FSS is a dual-core implementation of the ARM® Cortex®-R5F processor configured for dual-core (split) or lockstep modes of operation. R5FSS also includes accompanying memories (L1 caches and tightly-coupled memories), standard Arm® CoreSight™ debug and trace architecture, integrated Vectored Interrupt Manager (VIM), ECC Aggregators, and various wrappers for protocol conversion and address translation for easy integration into the SoC. The device supports up to two R5FSS modules for a total possible 4x functional cores (dual-core mode) or 2x functional cores (lockstep mode).

Note

The Arm® Cortex®-R5F processor is a Cortex-R5 processor that includes the optional Floating-Point Unit (FPU) extension.

For more information, see *Arm Cortex-R5F Subsystem* section in *Processors and Accelerators* chapter in the device TRM.

7.2.2 Device/Power Manager

The WKUP_R5FSS is a single-core implementation of the ARM® Cortex®-R5F processor that acts as the Device Manager responsible for boot, resource management, and power management functions. WKUP_R5FSS also includes accompanying memories (L1 caches and tightly-coupled memories), standard Arm® CoreSight™ debug and trace architecture, integrated Vectored Interrupt Manager (VIM), ECC aggregators, and various other modules for protocol conversion and address translation for easy integration into the SoC.

For more information, see the *Cortex-R5F Subsystem* section in *Processors and Accelerators* chapter in the device TRM.

8 Applications, Implementation, and Layout

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Device Connection and Layout Fundamentals

8.1.1 Power Supply

8.1.2 External Oscillator

For more information about External Oscillators, see the Clock Specifications section.

8.1.3 JTAG, EMU, and TRACE

Texas Instruments supports a variety of eXtended Development System (XDS) JTAG controllers with various debug capabilities beyond only JTAG support. A summary of this information is available in the XDS Target Connection Guide.

For recommendations on JTAG, EMU, and TRACE routing, see the Emulation and Trace Headers Technical Reference Manual

8.1.4 Unused Pins

For more information about Unused Pins, see Pin Connectivity Requirements.

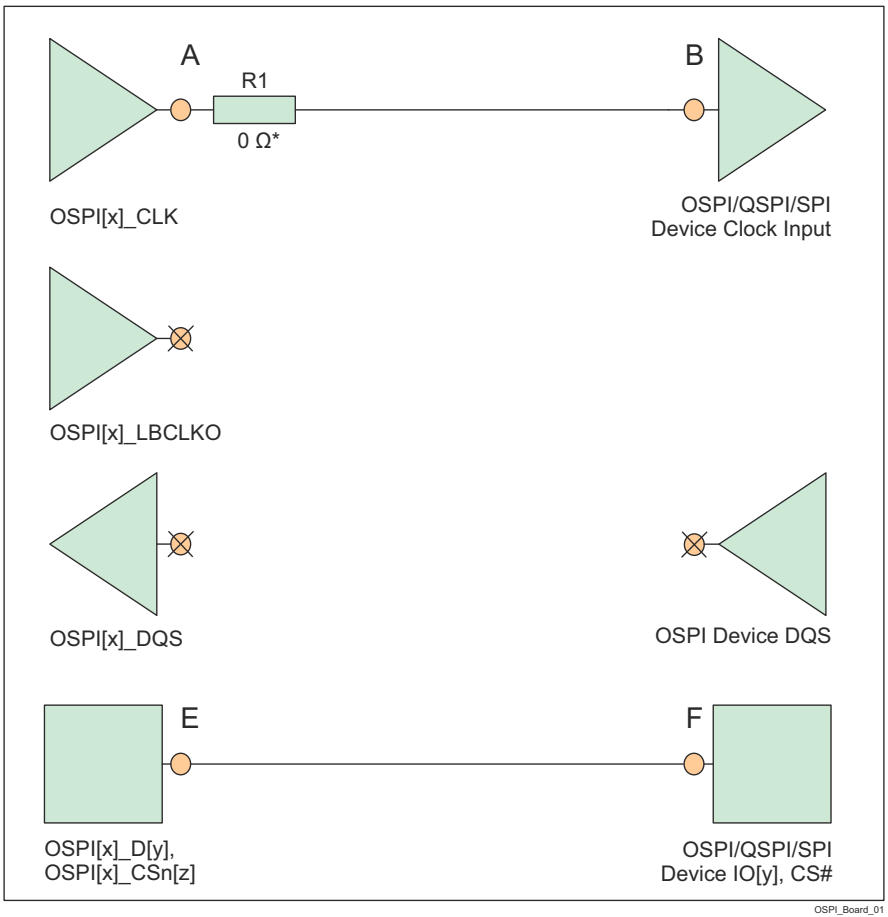
8.2 Peripheral- and Interface-Specific Design Information

8.2.1 OSPI/QSPI/SPI Board Design and Layout Guidelines

The following section details the PCB routing guidelines that must be observed when connecting OSPI, QSPI, or SPI devices.

8.2.1.1 No Loopback, Internal PHY Loopback, and Internal Pad Loopback

- The OSPI[x]_CLK output pin must be connected to the CLK input pin of the attached OSPI/QSPI/SPI device
- The signal propagation delay from the OSPI[x]_CLK pin to the attached OSPI/QSPI/SPI device CLK pin (A to B) must be ≤ 450ps (~7cm as stripline or ~8cm as microstrip)
- The signal propagation delay of each OSPI[x]_D[y] and OSPI[x]_CSn[z] pin to the corresponding attached OSPI/QSPI/SPI device data and control pin (E to F, or F to E) must be approximately equal to the signal propagation delay from the OSPI[x]_CLK pin to the attached OSPI/QSPI/SPI device CLK pin (A to B)
- 50 Ω PCB routing is recommended along with series terminations, as shown in Figure 8-1
- Propagation delays and matching:
  - (A to B) ≤ 450ps
  - (E to F, or F to E) = ((A to B) ± 60ps)



* 0 Ω resistor (R1), located as close as possible to the OSPI[x]_CLK pin, is placeholder for fine tuning, if needed.

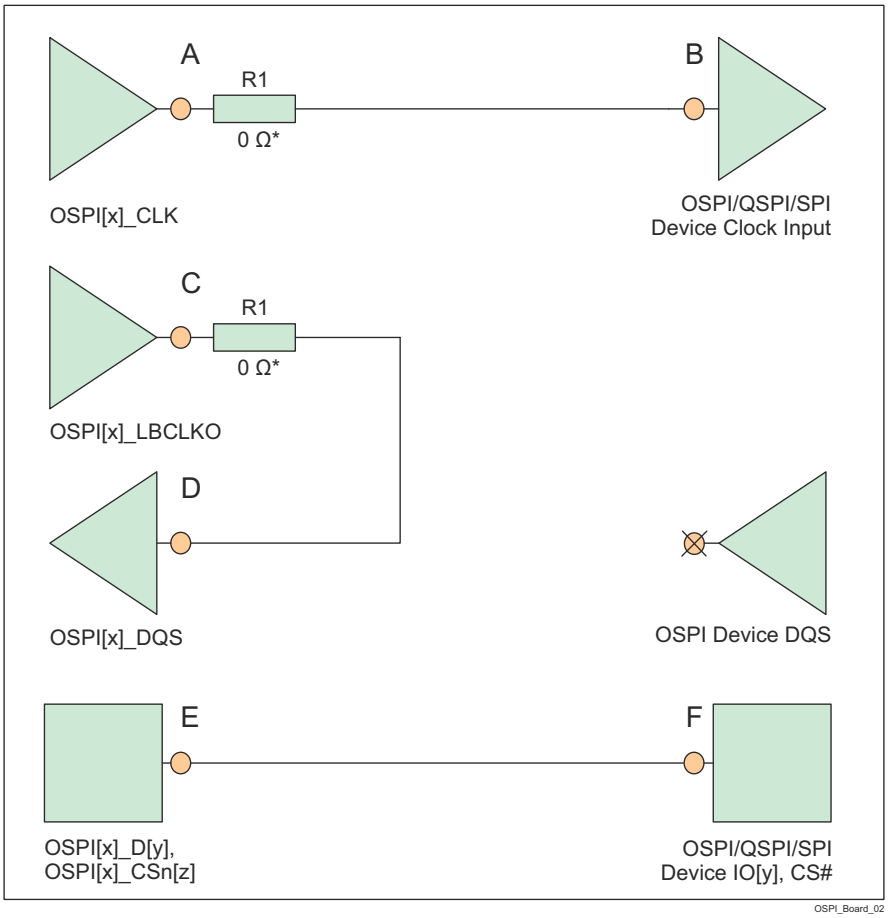
Figure 8-1. OSPI Connectivity Schematic for No Loopback, Internal PHY Loopback, and Internal Pad Loopback

8.2.1.2 External Board Loopback

- The OSPI[x]_CLK output pin must be connected to the CLK input pin of the attached OSPI/QSPI/SPI device
- The OSPI[x]_LBCLKO output pin must be looped back to the OSPI[x]_DQS input pin
- The signal propagation delay of the OSPI[x]_LBCLKO pin to the OSPI[x]_DQS pin (C to D) must be approximately twice the propagation delay of the OSPI[x]_CLK pin to the attached OSPI/QSPI/SPI device CLK pin (A to B)
- The signal propagation delay of each OSPI[x]_D[y] and OSPI[x]_CSn[z] pin to the corresponding attached OSPI/QSPI/SPI device data and control pin (E to F, or F to E) must be approximately equal to the signal propagation delay from the OSPI[x]_CLK pin to the attached OSPI/QSPI/SPI device CLK pin (A to B)
- 50 Ω PCB routing is recommended along with series terminations, as shown in Figure 8-2
- Propagation delays and matching:
  - (C to D) = 2 x ((A to B) ± 30 ps), see the exception note below.
  - (E to F, or F to E) = ((A to B) ± 60 ps)

Note

The External Board Loopback hold time requirement (defined by parameter number O16 in the *OSPI0 Timing Requirements - PHY DDR Mode* section) may be larger than the hold time provided by a typical OSPI/QSPI/SPI device. In this case, the propagation delay of OPSI[x]_LBCLKO pin to the OSPI[x]_DQS pin (C to D) can be reduced to provide additional hold time.

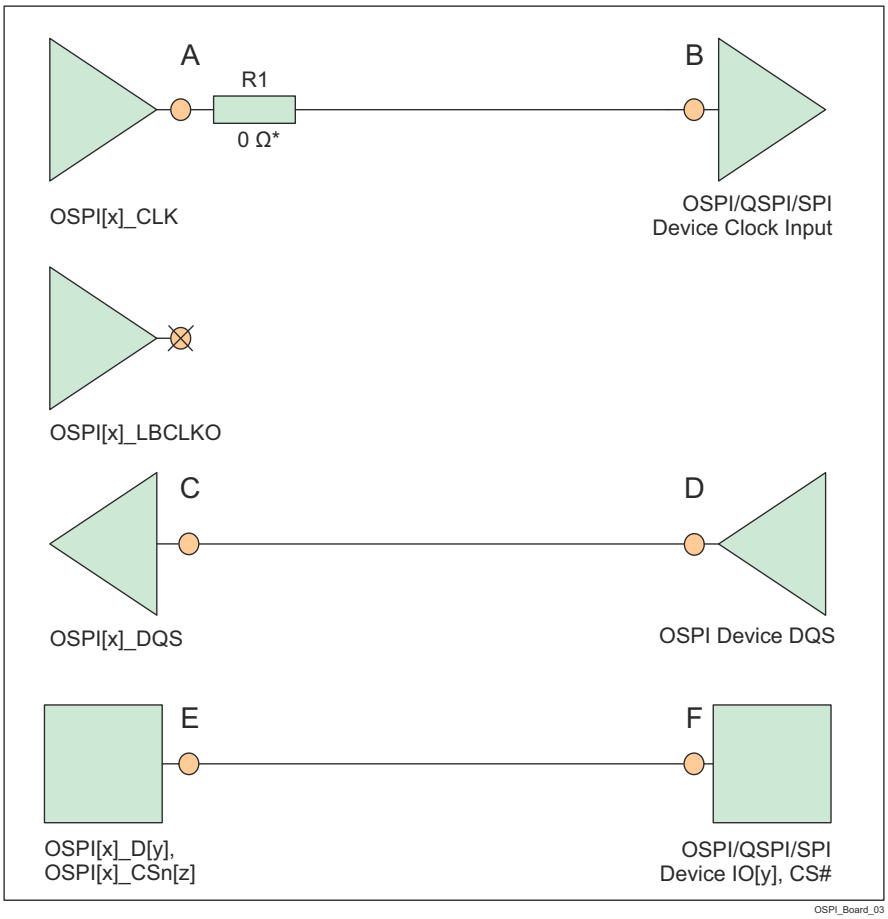


* 0 Ω resistor (R1), located as close as possible to the OSPI[x]_CLK and OSPI[x]_LBCLKO pins, is a placeholder for fine tuning, if needed.

Figure 8-2. OSPI Connectivity Schematic for External Board Loopback

8.2.1.3 DQS (only available in Octal SPI devices)

- The OSPI[x]_CLK output pin must be connected to the CLK input pin of the attached OSPI/QSPI/SPI device
- The DQS pin of the attached OSPI/QSPI/SPI device must be connected to OSPI[x]_DQS pin
- The signal propagation delay from the attached OSPI/QSPI/SPI device DQS pin to the OSPI[x]_DQS pin (D to C) must be approximately equal to the signal propagation delay from the OSPI[x]_CLK pin to the attached OSPI/QSPI/SPI device CLK pin (A to B)
- The signal propagation delay of each OSPI[x]_D[y] and OSPI[x]_CSn[z] pin to the corresponding attached OSPI/QSPI/SPI device data and control pin (E to F, or F to E) must be approximately equal to the signal propagation delay from the OSPI[x]_CLK pin to the attached OSPI/QSPI/SPI device CLK pin (A to B)
- 50 Ω PCB routing is recommended along with series terminations, as shown in Figure 8-3
- Propagation delays and matching:
  - (D to C) = ((A to B) ± 30 ps)
  - (E to F, or F to E) = ((A to B) ± 60 ps)



* 0 Ω resistor (R1), located as close as possible to the OSPI[x]_CLK pin, is a placeholder for fine tuning, if needed.

Figure 8-3. OSPI Connectivity Schematic for DQS

8.2.2 USB VBUS Design Guidelines

The USB 3.1 specification allows the VBUS voltage to be as high as 5.5V for normal operation, and as high as 20V when the Power Delivery addendum is supported. Some automotive applications require a max voltage to be 30V.

The device requires the VBUS signal voltage be scaled down using an external resistor divider (as shown in the Figure 8-4), which limits the voltage applied to the actual device pin (USB0_VBUS). The tolerance of these external resistors should be equal to or less than 1%, and the leakage current of Zener diode at 5V should be less than 100nA.

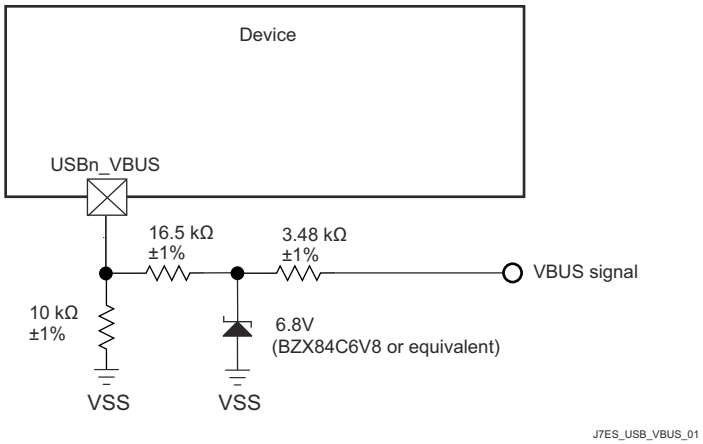


Figure 8-4. USB VBUS Detect Voltage Divider / Clamp Circuit

The USB0_VBUS pin can be considered to be fail-safe because the external circuit in Figure 8-4 limits the input current to the actual device pin in a case where VBUS is applied while the device is powered off.

8.2.3 System Power Supply Monitor Design Guidelines

The VMON_ER_VSYS pin provides a way to monitor a system power supply. This system power supply is typically a single pre-regulated power source for the entire system and can be connected to the VMON_ER_VSYS pin via and external resistor divider circuit. This system supply is monitored by comparing the external voltage divider output voltage to an internal voltage reference, where a power fail event is triggered when the voltage applied to VMON_ER_VSYS drops below the internal reference voltage. The actual system power supply voltage trip point is determined by the system designer when selecting component values used to implement the external resistor voltage divider circuit.

When designing the resistor divider circuit the designer must understand various factors which contribute to variability in the system power supply monitor trip point. The first thing to consider is the initial accuracy of the VMON_ER_VSYS input threshold which has a nominal value of 0.45V, with a variation of ±3%. Precision 1% resistors with similar thermal coefficient are recommended for implementing the resistor voltage divider. This minimizes variability contributed by resistor value tolerances. Input leakage current associated with VMON_ER_VSYS must also be considered since any current flowing into the pin creates a loading error on the voltage divider output. The VMON_ER_VSYS input leakage current can be in the range of 10nA to 2.5µA when applying 0.45V.

Note

The resistor voltage divider shall be designed such that the output voltage never exceeds the maximum value defined in the *Recommended Operating Conditions* section, during normal operating conditions.

Figure 8-5 presents an example, where the system power supply is nominally 5 V and the maximum trigger threshold is 5V - 10%, or 4.5V.

For this example, the designer must understand which variables effect the maximum trigger threshold when selecting resistor values. A device which has a VMON_ER_VSYS input threshold of 0.45V + 3% needs to be considered when trying to design a voltage divider that doesn't trip until the system supply drops 10%. The effect of resistor tolerance and input leakage also needs to be considered, but the contribution to the maximum trigger point is not obvious. When selecting component values which produce a maximum trigger voltage, the system designer must consider a condition where the value of R1 is 1% low and the value of R2 is 1% high combined with a condition where input leakage current for the VMON_ER_VSYS pin is 2.5µA. When implementing a resistor divider where R1 = 4.81KΩ and R2 = 40.2KΩ, the result is a maximum trigger threshold of 4.517V.

Once component values have been selected to satisfy the maximum trigger voltage as described above, the system designer can determine the minimum trigger voltage by calculating the applied voltage that produces an output voltage of 0.45V - 3% when the value of R1 is 1% high and the value of R2 is 1% low, and the input leakage current is 10nA, or zero. Using an input leakage of zero with the resistor values given above, the result is a minimum trigger threshold of 4.013 V.

This example demonstrates a system power supply voltage trip point that ranges from 4.013V to 4.517V. Approximately 250mV of this range is introduced by VMON_VSYS input threshold accuracy of ±3%, approximately 150mV of this range is introduced by resistor tolerance of ±1%, and approximately 100mV of this range is introduced by loading error when VMON_ER_VSYS input leakage current is 2.5µA.

The resistor values selected in this example produces approximately 100 µA of bias current through the resistor divider when the system supply is 4.5 V. The 100 mV of loading error mentioned above can be reduced to about 10 mV by increasing the bias current through the resistor divider to approximately 1 mA. So resistor divider bias current vs loading error is something the system designer needs to consider when selecting component values.

The system designer must also consider implementing a noise filter on the voltage divider output since VMON_ER_VSYS has minimum hysteresis and a high-bandwidth response to transients. This can be done by installing a capacitor across R1 as shown in Figure 8-5. However, the system designer must determine the response time of this filter based on system supply noise and expected response to transient events.

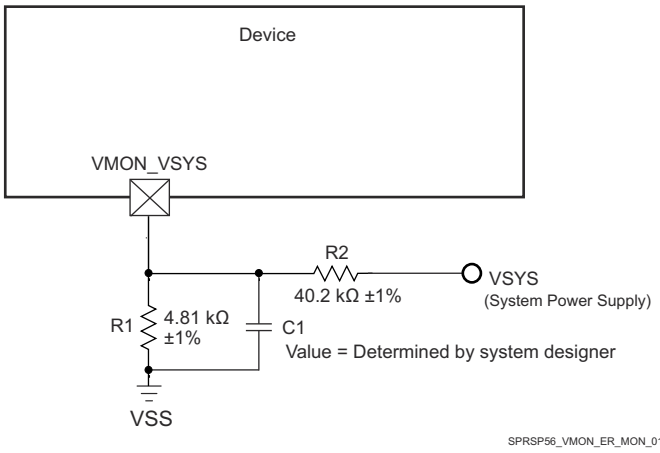


Figure 8-5. System Supply Monitor Voltage Divider Circuit

VMON_1P8_SOC pin provides a way to monitor external 1.8V power supplies. This pin must be connected directly to their respective power source. An internal resistor divider with software control is implemented inside the SoC for each of these pins. Software can program each internal resistor divider to create appropriate under voltage and over voltage interrupts.

VMON_3P3_SOC pin provides a way to monitor external 3.3V power supplies. This pin must be connected directly to their respective power source. An internal resistor divider with software control is implemented inside the SoC for each of these pins. Software can program each internal resistor divider to create appropriate under voltage and over voltage interrupts.

8.2.4 High Speed Differential Signal Routing Guidance

The High Speed Interface Layout Guidelines provides guidance for successful routing of the high speed differential signals. This includes PCB stackup and materials guidance as well as routing skew, length and spacing limits. TI supports *only* designs that follow the board design guidelines contained in the application note.

8.2.5 Thermal Solution Guidance

The Thermal Design Guide for DSP and ARM Application Processors provides guidance for successful implementation of a thermal solution for system designs containing this device. This document provides background information on common terms and methods related to thermal solutions. TI only supports designs that follow system design guidelines contained in the application note.

8.3 Clock Routing Guidelines

8.3.1 Oscillator Routing

When designing the printed-circuit board:

- Place all crystal circuit components as close as possible to the respective device pins.
- Route the crystal circuit traces on the outer layer of the PCB and minimize trace lengths to reduce parasitic capacitance and minimize crosstalk from other signals.
- Place a continuous ground plane on the adjacent layer of the PCB such that it is under all crystal circuit components and crystal circuit traces.
- Route a ground guard around the crystal circuit components to shield it from any adjacent signals routed on the same layer as the crystal circuit traces. Insert multiple vias to stitch down the ground guard such that it does not have any unterminated stubs.
- Route a ground guard between the MCU_OSC0_XI/OSC1_XI/WKUP_LFOSC0_XI and MCU_OSC0_XO/OSC1_XO/WKUP_LFOSC0_XO signals to shield the _XI signal from the _X0 signal. Insert multiple vias to stitch down the ground guard such that it does not have any unterminated stubs.
- Connect all crystal circuit ground connections and ground guard connections directly to the adjacent layer ground plane, and the device VSS ground plane if they are implemented separately on different layers of the PCB.

Note

Implementing a ground guard between the MCU_OSC0_XI/OSC1_XI/WKUP_LFOSC0_XI and MCU_OSC0_XO/OSC1_XO/WKUP_LFOSC0_XO signals is critical to minimize shunt capacitance between the two signals. Routing these two signals adjacent to each other without a ground guard between them will effectively reduce the gain of the oscillator amplifier, which reduces its ability to start oscillation.

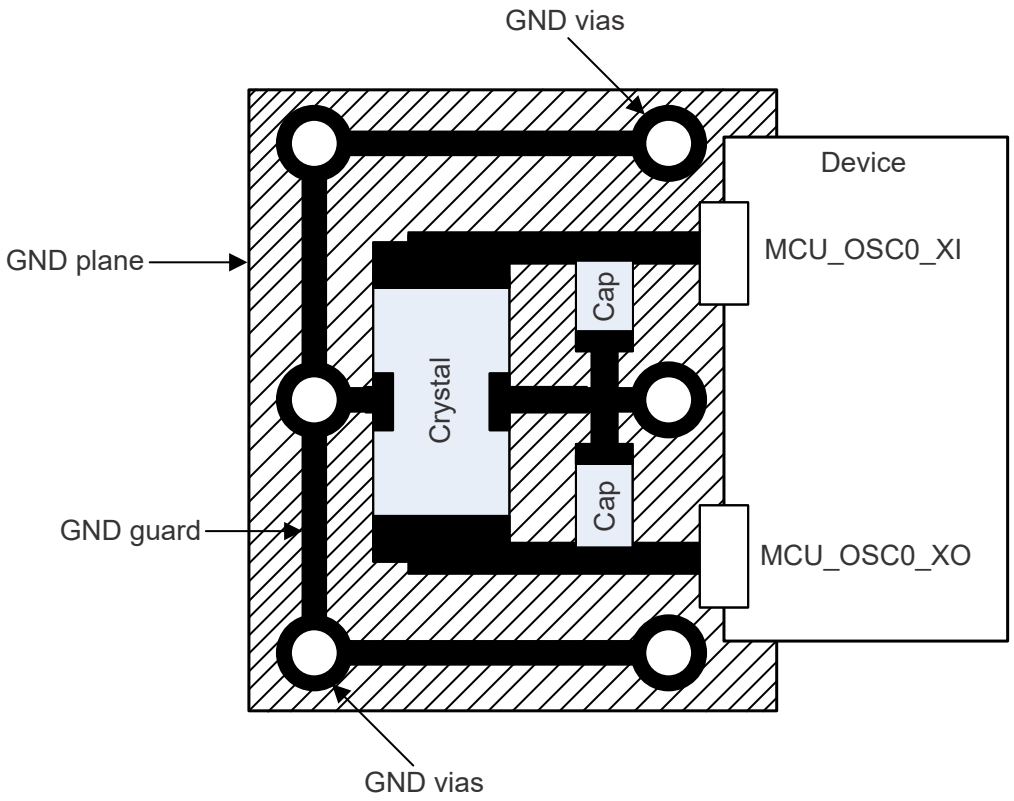


Figure 8-6. MCU_OSC0/OSC1/WKUP_LFOSC0 PCB requirements

9 Device and Documentation Support

9.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microprocessors (MPUs) and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, AM27542AFZIANJRQ1). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices and tools (TMDS).

Device development evolutionary flow:

X Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

P Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

null Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

For orderable part numbers of AM275 devices in the ANJ package type, see the Package Option Addendum of this document, the TI website (ti.com), or contact your TI sales representative.

9.1.1 Standard Package Symbolization

Note

Some devices may have a cosmetic circular marking visible on the top of the device package which results from the production test process. In addition, some devices may also show a color variation in the package substrate which results from the substrate manufacturer. These differences are cosmetic only with no reliability impact.

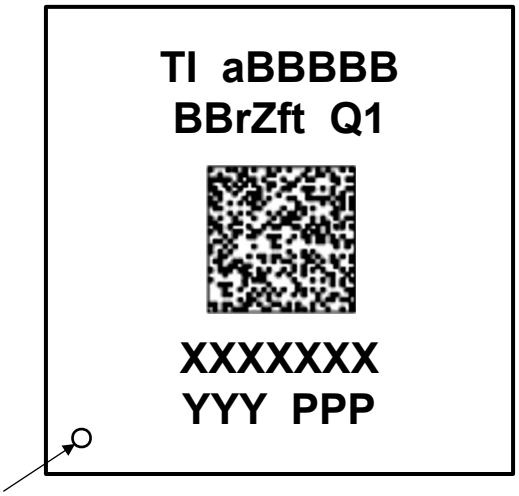


Figure 9-1. Printed Device Reference

9.1.2 Device Naming Convention

FIELD PARAMETER	FIELD DESCRIPTION	VALUE	DESCRIPTION
a	Device evolution stage(1)	X	Prototype
		P	Preproduction (production test flow, no reliability data)
		BLANK (null)	Production
BBBBBBB	Base production part number	AM27542	For more P/N details, see Device Comparison
		AM27522	
		AM27521	
r	Device Revision	A	SR 1.0
Z	Device Speed and Memory Grade	A	See Device Speed Grades
		B	
		C	
		D	
		E	
		F	
f	Software Bundle	Z, F	No software bundle
t	Temperature(2)	A	–40°C to 105°C - Industrial
		I	–40°C to 125°C - Automotive
Q1	Automotive Designator	BLANK	Standard
		Q1	Meet AEC-Q100 qualification requirements, with exceptions as specified in this document (data sheet). Supports T_J = –40°C to 125°C
	2D Barcode	Varies	Optional 2D barcode
		BLANK	
XXXXXXX			Lot Trace Code (LTC)
YYY			Production Code, For TI use only
PPP	Package Designator	ANJ	ANJ FCCSP (15.8 mm × 15.8 mm)
O			Pin one designator

(1) To designate the stages in the product development cycle, TI assigns prefixes to the part numbers. These prefixes represent evolutionary stages of product development from engineering prototypes through fully qualified production devices.
Prototype devices are shipped against the following disclaimer:
“This product is still in development and is intended for internal evaluation purposes.”
Notwithstanding any provision to the contrary, TI makes no warranty expressed, implied, or statutory, including any implied warranty of merchantability of fitness for a specific purpose, of this device.
(2) Applies to device max junction temperature.

Note

BLANK in the symbol or part number is collapsed so there are no gaps between characters.

9.2 Tools and Software

The following Development Tools support development for TI's Embedded Processing platforms:

Development Tools

Code Composer Studio™ Integrated Development Environment Code Composer Studio (CCS) Integrated Development Environment (IDE) is a development environment that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio comprises a suite of tools used to develop and debug embedded applications. The tool includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking you through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers.

SysConfig-PinMux Tool The SysConfig-PinMux Tool is a software tool which provides a Graphical User Interface for configuring pin multiplexing settings, resolving conflicts and specifying I/O cell characteristics for TI Embedded Processor devices. The tool can be used to automatically calculate the optimal pinmux configuration to satisfy entered system requirements. The tool generates output C header/code files that can be imported into software development kits (SDKs) and used to configure customer's software to meet custom hardware requirements. The **Cloud-based SysConfig-PinMux Tool** is also available.

For a complete listing of development-support tools for the processor platform, visit the Texas Instruments website at ti.com. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

9.3 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The following documents describe the AM275 devices.

Technical Reference Manual

AM275 Processors Silicon Revision 1.0 Technical Reference Manual: Details the integration, the environment, the functional description, and the programming models for each peripheral and subsystem in the AM275 family of devices.

Errata

AM275 Processors Silicon Revision 1.0 Silicon Errata: Describes the known exceptions to the functional specifications for the device.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

Changes from July 31, 2025 to April 21, 2026 (from Revision A (July 2025) to Revision B (April 2026)) — Page

11 Mechanical, Packaging, and Orderable Information

11.1 Packaging Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AM27521AAZIANJRQ1	Active	Production	FCCSP (ANJ) | 361	1000 | LARGE T&R	Yes	Call TI	Level-3-250C-168 HR	-40 to 125	21AAZI Q1
AM27521ABZIANJRQ1	Active	Production	FCCSP (ANJ) | 361	1000 | LARGE T&R	Yes	Call TI	Level-3-250C-168 HR	-40 to 125	21ABZI Q1
AM27522ACZIANJRQ1	Active	Production	FCCSP (ANJ) | 361	1000 | LARGE T&R	Yes	Call TI	Level-3-250C-168 HR	-40 to 125	22ACZI Q1
AM27542ADZIANJRQ1	Active	Production	FCCSP (ANJ) | 361	1000 | LARGE T&R	Yes	Call TI	Level-3-250C-168 HR	-40 to 125	42ADZI Q1
AM27542AEZIANJRQ1	Active	Production	FCCSP (ANJ) | 361	1000 | LARGE T&R	Yes	Call TI	Level-3-250C-168 HR	-40 to 125	42AEZI Q1
AM27542AFZIANJRQ1	Active	Production	FCCSP (ANJ) | 361	1000 | LARGE T&R	Yes	Call TI	Level-3-250C-168 HR	-40 to 125	42AFZI Q1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

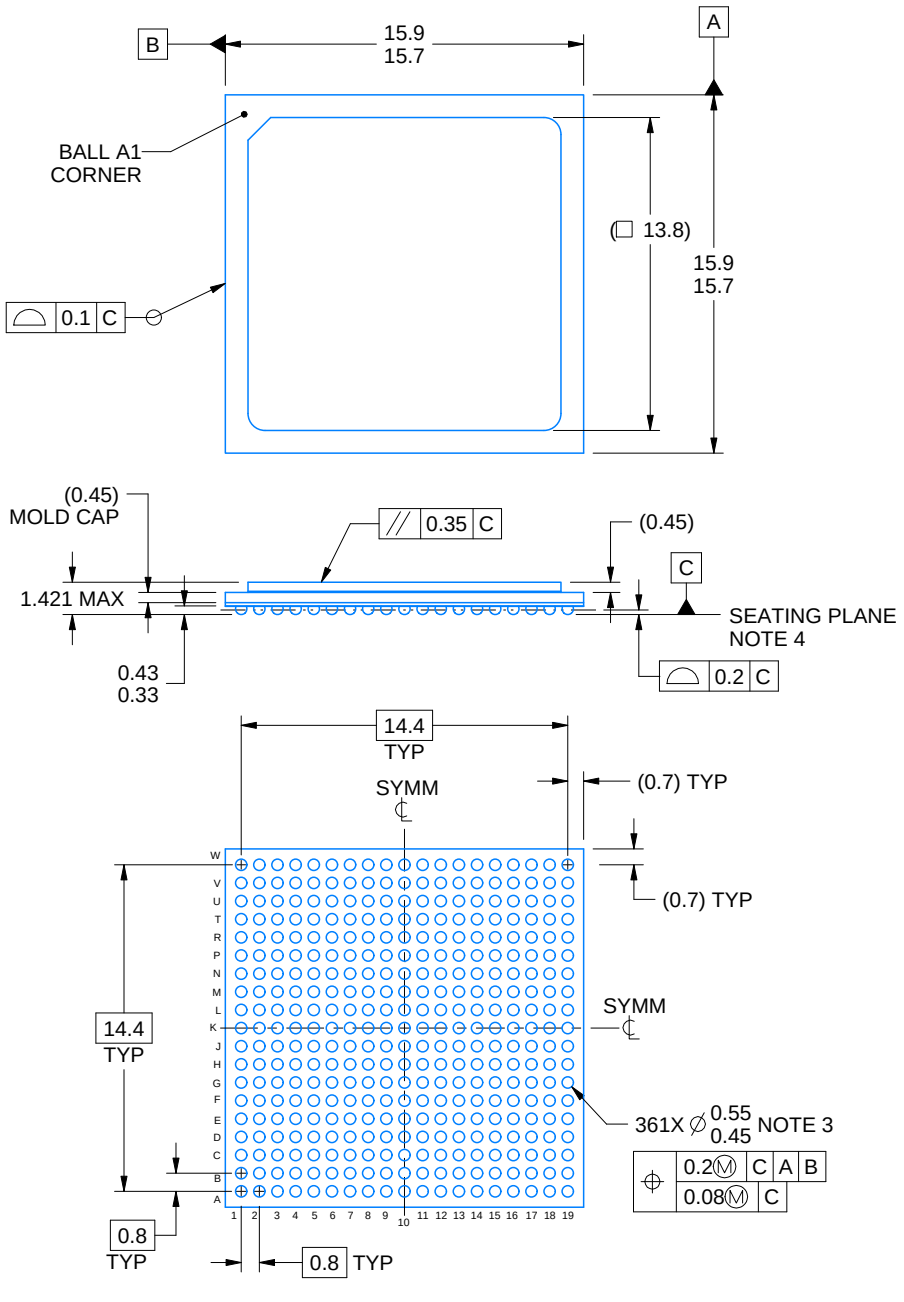
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

PACKAGE OUTLINE

ANJ0361A

FCCSP - 1.421 mm max height

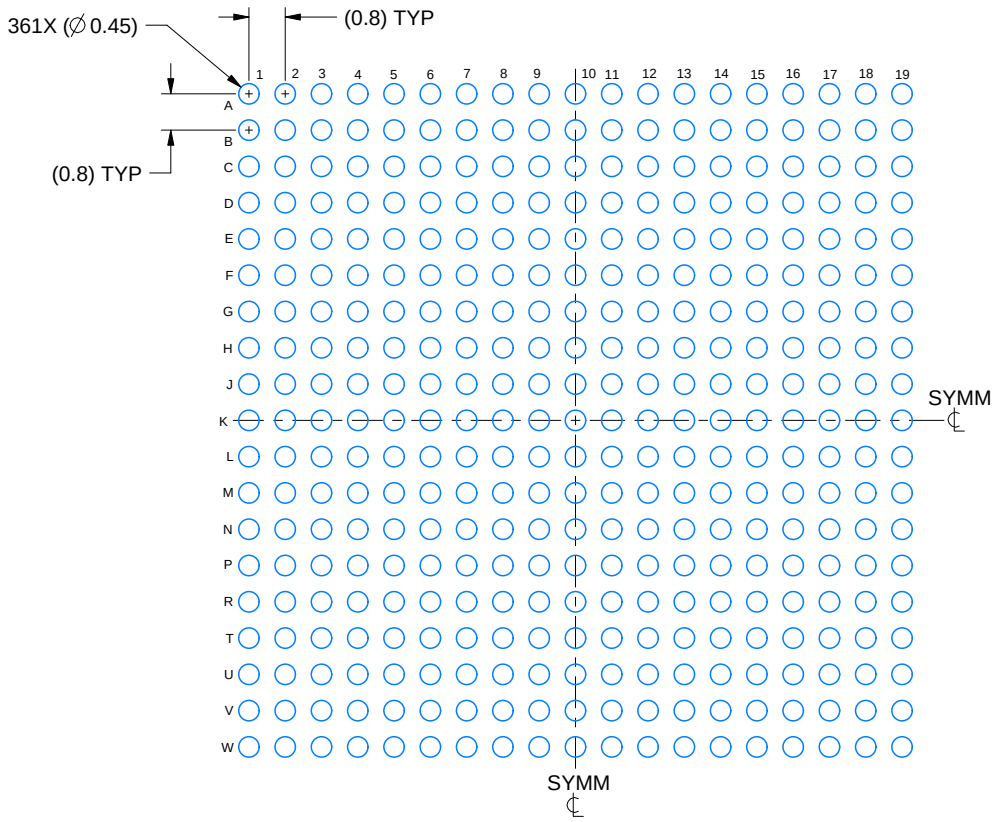
BALL GRID ARRAY



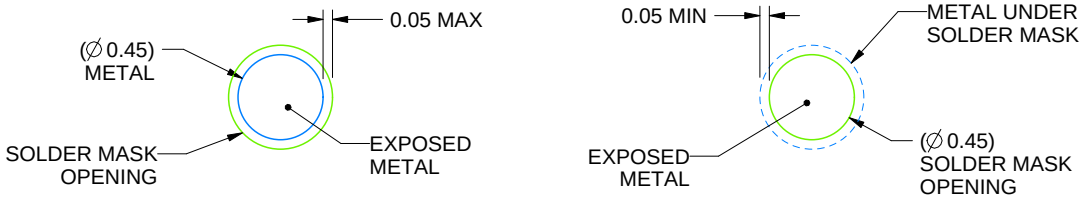
4230660/A 04/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension is measured at the maximum solder ball diameter, post reflow, parallel to primary datum C.
4. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 6X



NON-SOLDER MASK DEFINED (PREFERRED)

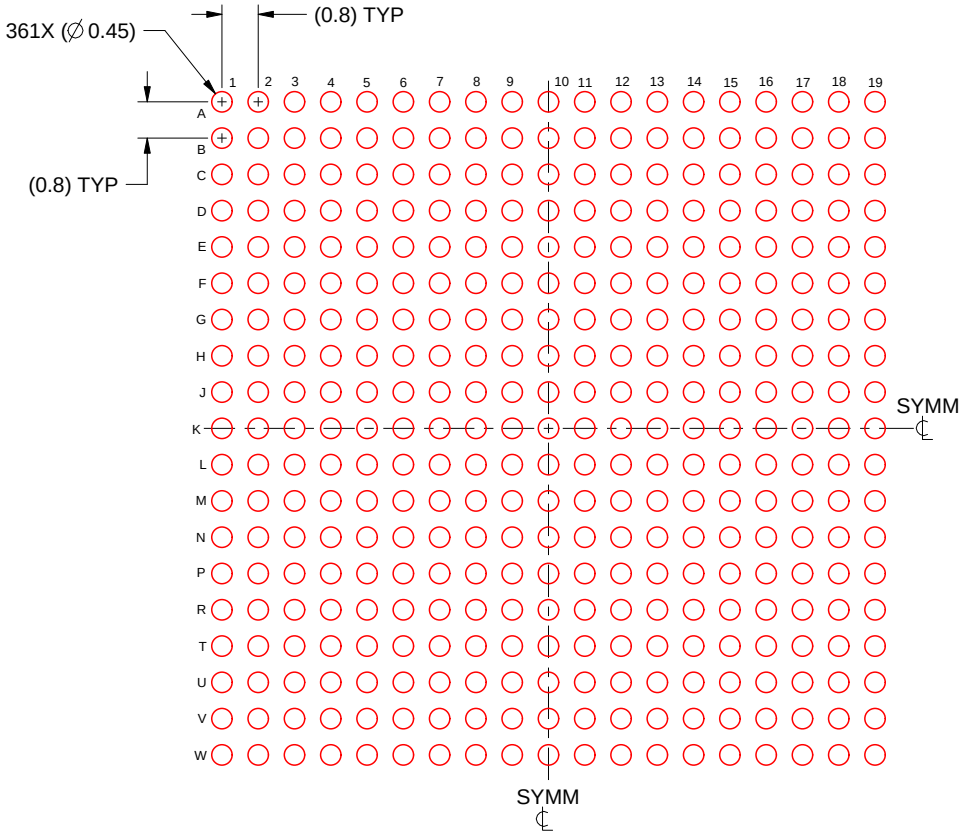
SOLDER MASK DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4230660/A 04/2024

NOTES: (continued)

5. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SPRU811 (www.ti.com/lit/spru811).



SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE: 6X

4230660/A 04/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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Last updated 10/2025