AMC1306x Small, High-Precision, Reinforced Isolated Delta-Sigma Modulators With High CMTI

1 Features

- Pin-compatible family optimized for shunt-resistor-based current measurements:
  - ±50mV or ±250mV input voltage ranges
  - Manchester coded or uncoded bitstream options
- Excellent DC performance:
  - Offset error: ±50µV or ±100µV (max)
  - Offset drift: 1µV/°C (max)
  - Gain error: ±0.2% (max)
  - Gain drift: ±40ppm/°C (max)
- Transient immunity: 100kV/µs (typ)
- System-level diagnostic features
- Safety-related certifications:
  - $7000V_{PEAK}$ reinforced isolation per DIN EN IEC 60747-17 (VDE 0884-17)
  - $5000V_{RMS}$ isolation for 1 minute per UL1577
  - CAN/CSA no. 5A-component acceptance service notice and IEC 62368-1 end equipment standard
- Fully specified over the extended industrial temperature range: –40°C to +125°C

2 Applications

- Shunt-resistor-based current sensing and isolated voltage measurements in:
  - Industrial motor drives
  - Photovoltaic inverters
  - Uninterruptable power supplies

3 Description

The AMC1306 is a precision, delta-sigma (ΔΣ) modulator with the output separated from the input circuitry by a capacitive double isolation barrier that is highly resistant to magnetic interference. This barrier is certified to provide reinforced isolation of up to $7000V_{PEAK}$ according to the DIN EN IEC 60747-17 (VDE 0884-17) and UL1577 standards. Used in conjunction with isolated power supplies, this isolated modulator separates parts of the system that operate on different common-mode voltage levels and protects lower-voltage parts from damage.

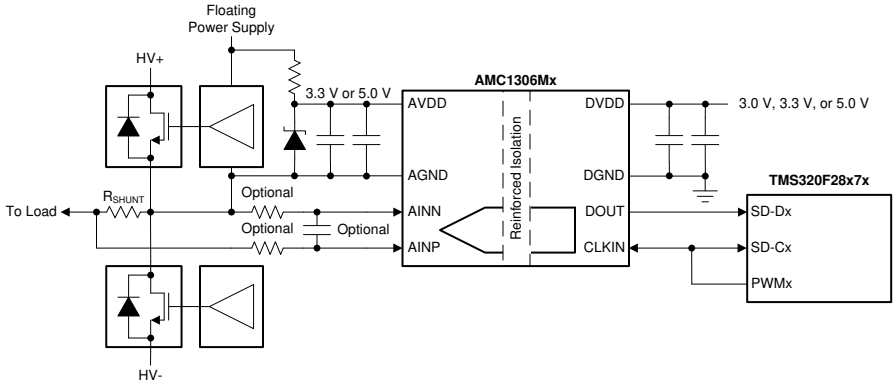
The input of the AMC1306 is optimized for direct connection to shunt resistors or other low voltage-level signal sources. The output bitstream of the AMC1306 is Manchester coded (AMC1306Ex) or uncoded (AMC1306Mx), depending on the derivate. Combined with a digital filter (such as those in the TMS320F2807x or TMS320F2837x microcontroller families), the device achieves 16 bits of resolution with a dynamic range of 85dB at a data rate of 78 kSPS.

The bitstream output of the Manchester coded AMC1306Ex versions support single-wire data and clock transfer without having to consider the setup and hold time requirements of the receiving device.

Device Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
AMC1306x	DWV (SOIC, 8)	5.85mm × 11.5mm

(1) For more information, see Mechanical, Packaging, and Orderable Information.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

Table of Contents

4 Device Comparison Table

PART NUMBER	INPUT VOLTAGE RANGE	DIFFERENTIAL INPUT RESISTANCE	DIGITAL OUTPUT INTERFACE
AMC1306E05	±50mV	4.9kΩ	Manchester coded CMOS
AMC1306E25	±250mV	22kΩ	Manchester coded CMOS
AMC1306M05	±50mV	4.9kΩ	Uncoded CMOS
AMC1306M25	±250mV	22kΩ	Uncoded CMOS

5 Pin Configuration and Functions

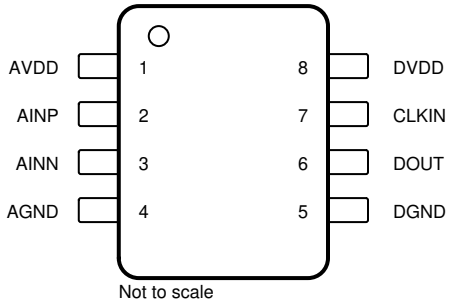


Figure 5-1. DWV Package, 8-Pin SOIC (Top View)

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	AVDD	—	Analog (high-side) power supply, 3.0V to 5.5V. See the *Power Supply Recommendations* section for decoupling recommendations.
2	AINP	Input	Noninverting analog input
3	AINN	Input	Inverting analog input
4	AGND	—	Analog (high-side) ground reference
5	DGND	—	Digital (controller-side) ground reference
6	DOUT	Output	Modulator data output. This pin is a Manchester coded output for AMC1306Ex derivates.
7	CLKIN	Input	Modulator clock input: 5MHz to 21MHz (5V operation) with internal pulldown resistor (typical value: 1.5MΩ)
8	DVDD	—	Digital (controller-side) power supply, 2.7V to 5.5V. See the *Power Supply Recommendations* section for decoupling recommendations.

6 Specifications

6.1 Absolute Maximum Ratings

see(1)

PARAMETER		MIN	MAX	UNIT
Power-supply voltage	AVDD to AGND	–0.3	6.5	V
	DVDD to DGND	–0.3	6.5	
Analog input voltage	INP, INN	AGND – 6	AVDD + 0.5V	V
Digital input voltage	CLKIN	DGND – 0.5	DVDD + 0.5	V
Digital output voltage	DOUT	DGND – 0.5	DVDD + 0.5	V
Input current	Continuous, any pin except power-supply pins	–10	10	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–65	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions* . If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001	±2000	V
		Charged-device model (CDM), per per ANSI/ESDA/JEDEC JS-002	±1000	

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
AVDD	Hgh-side power supply	AVDD to AGND	3	5.0	5.5	V
DVDD	Low-side power supply	DVDD to DGND	2.7	3.3	5.5	V
ANALOG INPUT (AMC1306x05)						
$V_{Clipping}$	Differential input voltage before clipping output	$V_{IN} = V_{INP} – V_{INN}$		±64		mV
V_{FSR}	Specified linear differential full-scale voltage	$V_{IN} = V_{INP} – V_{INN}$	–50		50	mV
V_{CM}	Operating common-mode input voltage	$(V_{INP} + V_{INN}) / 2$ to AGND	–0.1		AVDD – 2.1	V
ANALOG INPUT (AMC1306x25)						
$V_{Clipping}$	Differential input voltage before clipping output	$V_{IN} = V_{INP} – V_{INN}$		±320		mV
V_{FSR}	Specified linear differential full-scale voltage	$V_{IN} = V_{INP} – V_{INN}$	–250		250	mV
V_{CM}	Operating common-mode input voltage	$(V_{INP} + V_{INN}) / 2$ to AGND	–0.5		AVDD – 2.1	V
DIGITAL I/O						
V_{IO}	Digital input / output voltage		0		VDD	V
f_{CLKIN}	Input clock frequency	4.5V ≤ AVDD ≤ 5.5V	5	20	21	MHz
		3.0V ≤ AVDD ≤ 5.5V	5	20	20	
TEMPERATURE RANGE						
T_A	Specified ambient temperature		–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		DWV (SOIC)	UNIT
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	112.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	47.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	23.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	60.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
P_D	Maximum power dissipation (both sides)	AMC1306Ex, AVDD = DVDD = 5.5V	91.85	mW
		AMC1306Mx, AVDD = DVDD = 5.5V	86.90	
P_{D1}	Maximum power dissipation (high-side supply)	AVDD = 5.5V	53.90	mW
P_{D2}	Maximum power dissipation (low-side supply)	AMC1306Ex, DVDD = 5.5V	37.95	mW
		AMC1306Mx, DVDD = 5.5V	33.00	

6.6 Insulation Specifications

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest pin-to-pin distance through air	≥ 8.5	mm
CPG	External creepage(1)	Shortest pin-to-pin distance across the package surface	≥ 8.5	mm
DTI	Distance through insulation	Minimum internal gap (internal clearance) of the double insulation	≥ 21	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300V_{RMS}	I-IV	
		Rated mains voltage ≤ 6000V_{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17)(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	At AC voltage	2120	V_{PK}
V_{IOWM}	Maximum-rated isolation working voltage	At AC voltage (sine wave)	1500	V_{RMS}
		At DC voltage	2120	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60s (qualification test), $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1s (100% production test)	7000	V_{PK}
V_{IMP}	Maximum impulse voltage(3)	Tested in air, 1.2/50µs waveform per IEC 62368-1	9800	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(4)	Tested in oil (qualification test), 1.2/50µs waveform per IEC 62368-1	12800	V_{PK}
q_{pd}	Apparent charge(5)	Method a, after input/output safety test subgroups 2 and 3, $V_{pd(ini)} = V_{IOTM}$, t_{ini} = 60s, $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10s	≤ 5	pC
		Method a, after environmental tests subgroup 1, $V_{pd(ini)} = V_{IOTM}$, t_{ini} = 60s, $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10s	≤ 5	
		Method b1, at preconditioning (type test) and routine test, $V_{pd(ini)} = 1.2 \times V_{IOTM}$, t_{ini} = 1s, $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1s	≤ 5	
		Method b2, at routine test (100% production)(7) $V_{pd(ini)} = V_{pd(m)} = 1.2 \times V_{IOTM}$, $t_{ini} = t_m$ = 1s	≤ 5	
C_{IO}	Barrier capacitance, input to output(6)	V_{IO} = 0.5V_{PP} at 1MHz	≅1	pF
R_{IO}	Insulation resistance, input to output(6)	V_{IO} = 500V at T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500V at 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500V at T_S = 150°C	> 10^9	
	Pollution degree		2	
	Climatic category		55/125/21	
UL1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$, t = 60s (qualification test), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1s (100% production test)	5000	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Maintain the creepage and clearance distance of a board design to make sure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air to determine the surge immunity of the package.
(4) Testing is carried in oil to determine the intrinsic surge immunity of the isolation barrier.
(5) Apparent charge is electrical discharge caused by a partial discharge (pd).
(6) All pins on each side of the barrier are tied together, creating a two-pin device.
(7) Either method b1 or b2 is used in production.

6.7 Safety-Related Certifications

VDE	UL
DIN EN IEC 60747-17 (VDE 0884-17), EN IEC 60747-17, DIN EN IEC 62368-1 (VDE 0868-1), EN IEC 62368-1, IEC 62368-1 Clause : 5.4.3 ; 5.4.4.4 ; 5.4.9	Recognized under 1577 component recognition and CSA component acceptance NO 5 programs
Reinforced insulation	Single protection
Certificate number: 40040142	File number: E181974

6.8 Safety Limiting Values

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 112.2°C/W, AVDD = DVDD = 5.5V, T_J = 150°C, T_A = 25°C			202.5	mA
		$R_{\theta JA}$ = 112.2°C/W, AVDD = DVDD = 3.6V, T_J = 150°C, T_A = 25°C			309.4	mA
P_S	Safety input, output, or total power(1)	$R_{\theta JA}$ = 112.2°C/W, T_J = 150°C, T_A = 25°C			1114	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I_S and P_S. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the *Thermal Information* table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum junction temperature.
$P_S = I_S \times AVDD_{max} + I_S \times DVDD_{max}$, where $AVDD_{max}$ is the maximum high-side voltage and $DVDD_{max}$ is the maximum controller-side supply voltage.

6.9 Electrical Characteristics (AMC1306x05)

minimum and maximum specifications are at T_A = –40°C to 125°C, AVDD = 3.0V to 5.5V, DVDD = 2.7V to 5.5V, AINP = –50mV to 50mV, AINN = AGND, and sinc^3 filter with OSR = 256 (unless otherwise noted); typical specifications are at T_A = 25°C, CLKIN = 20MHz, AVDD = 5V, and DVDD = 3.3V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
V_{CMov}	Commonmode overvoltage detection level	(INP + INN) / 2 to AGND	AVDD – 2			V
C_{IN}	Single-ended input capacitance	INN = AGND		4		pF
C_{IND}	Differential input capacitance			2		pF
R_{IN}	Single-ended input resistance	INN = AGND		4.75		kΩ
R_{IND}	Differential input resistance			4.9		kΩ
I_{IB}	Input bias current	INP = INN = AGND, $I_{IB} = I_{BP} + I_{BN}$	–97	–72	–57	µA
I_{IO}	Input offset current			±10		nA
CMTI	Common-mode transient immunity		50	100		kV/µs
CMRR	Common-mode rejection ratio	INP = INN, f_{IN} = 0Hz, $V_{CM\ min} \le V_{IN} \le V_{CM\ max}$		–99		dB
		INP = INN, f_{IN} from 0.1Hz to 50kHz, $V_{CM\ min} \le V_{IN} \le V_{CM\ max}$		–98		
BW	Input bandwidth			800		kHz
DC ACCURACY						
DNL	Differential nonlinearity	Resolution: 16 bits	–0.99		0.99	LSB
INL	Integral nonlinearity(3)	Resolution: 16 bits, 4.5V ≤ AVDD ≤ 5.5V	–4	±1	4	LSB
		Resolution: 16 bits, 3.0V ≤ AVDD ≤ 3.6V	–5	±1.5	5	LSB
E_O	Offset error(1)	T_A = 25°C, INP = INN = GND1	–50	±2.5	50	µV
TCE_O	Offset error temperature drift(4)		–1	±0.25	1	µV/°C
E_G	Gain error	T_A = 25°C	–0.2%	±0.005%	0.2%	
TCE_G	Gain error temperature drift(5)		–40	±20	40	ppm/°C
PSRR	Power-supply rejection ratio	INP = INN = AGND, AVDD from 3.0V to 5.5V, at DC		–108		dB
		INP = INN = AGND, AVDD from 3. 0V to 5.5V, 10kHz / 100mV ripple		–107		
AC ACCURACY						
SNR	Signal-to-noise ratio	f_{IN} = 1kHz	78	82.5		dB
SINAD	Signal-to-noise + distortion	f_{IN} = 1kHz	77.5	82.3		dB
THD	Total harmonic distortion(6)	4.5V ≤ AVDD ≤ 5.5V, f_{IN} = 1kHz, 5MHz ≤ f_{CLKIN} ≤ 21MHz		–98	–84	dB
		3.0V ≤ AVDD ≤ 3.6V, f_{IN} = 1kHz, 5MHz ≤ f_{CLKIN} ≤ 20MHz		–93	–83	
SFDR	Spurious-free dynamic range	f_{IN} = 1kHz	83	100		dB

minimum and maximum specifications are at T_A = –40°C to 125°C, AVDD = 3.0V to 5.5V, DVDD = 2.7V to 5.5V, AINP = –50mV to 50mV, AINN = AGND, and sinc^3 filter with OSR = 256 (unless otherwise noted); typical specifications are at T_A = 25°C, CLKIN = 20MHz, AVDD = 5V, and DVDD = 3.3V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CMOS LOGIC WITH SCHMITT-TRIGGER						
I_{IN}	Input current	DGND ≤ V_{IN} ≤ DVDD	0		7	µA
C_{IN}	Input capacitance			4		pF
V_{IH}	High-level input voltage		0.7 × DVDD		DVDD + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.3 × DVDD	V
C_{LOAD}	Output load capacitance			30		pF
V_{OH}	High-level output voltage	I_{OH} = –20µA	DVDD – 0.1			V
		I_{OH} = –4mA	DVDD – 0.4			
V_{OL}	Low-level output voltage	I_{OL} = 20µA			0.1	V
		I_{OL} = 4mA			0.4	
POWER SUPPLY						
I_{AVDD}	High-side supply current	3.0V ≤ AVDD ≤ 3.6V		6.3	8.5	mA
		4.5V ≤ AVDD ≤ 5.5V		7.2	9.8	
I_{DVDD}	Low-side supply current	AMC1306Ex, 2.7V ≤ DVDD ≤ 3.6V, C_{LOAD} = 15pF		4.1	5.5	mA
		AMC1306Mx, 2.7V ≤ DVDD ≤ 3.6V, C_{LOAD} = 15pF		3.3	4.8	
		AMC1306Ex, 4.5V ≤ DVDD ≤ 5.5V, C_{LOAD} = 15pF		5.0	6.9	
		AMC1306Mx, 4.5V ≤ DVDD ≤ 5.5V, C_{LOAD} = 15pF		3.9	6.0	

(1) This parameter is input referred.
(2) Integral nonlinearity is defined as the maximum deviation from a straight line passing through the end-points of the ideal ADC transfer function expressed as number of LSBs or as a percent of the specified linear full-scale range FSR.
(3) Offset error temperature drift is calculated using the box method, as described by the following equation: $TCE_O = (E_{O,MAX} – E_{O,MIN}) / TempRange$ where $E_{O,MAX}$ and $E_{O,MIN}$ refer to the maximum and minimum E_O values measured within the temperature range (–40 to 125°C).
(4) Gain error temperature drift is calculated using the box method, as described by the following equation: $TCE_G\ (ppm) = ((E_{G,MAX} - E_{G,MIN}) / TempRange) \times 10^4$ where $E_{G,MAX}$ and $E_{G,MIN}$ refer to the maximum and minimum E_G values (in %) measured within the temperature range (–40 to 125°C).
(5) THD is the ratio of the rms sum of the amplitudes of first five higher harmonics to the amplitude of the fundamental.

6.10 Electrical Characteristics (AMC1306x25)

minimum and maximum specifications are at T_A = –40°C to 125°C, AVDD = 3.0V to 5.5V, DVDD = 2.7V to 5.5V, AINP = –250mV to 250mV, AINN = AGND, and sinc^3 filter with OSR = 256 (unless otherwise noted); typical specifications are at T_A = 25°C, CLKIN = 20MHz, AVDD = 5V, and DVDD = 3.3V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
V_{CMov}	Common-mode overvoltage detection level	(INP + INN) / 2 to AGND	AVDD – 2			V
C_{IN}	Single-ended input capacitance	INN = AGND		2		pF
C_{IND}	Differential input capacitance			1		pF
I_{IB}	Input bias current	INP = INN = AGND, $I_{IB} = I_{BP} + I_{BN}$	–82	–60	–48	µA
R_{IN}	Single-ended input resistance	INN = AGND		19		kΩ
R_{IND}	Differential input resistance			22		kΩ
I_{IO}	Input offset current			±5		nA
CMTI	Common-mode transient immunity		50	100		kV/µs
CMRR	Common-mode rejection ratio	INP = INN, f_{IN} = 0Hz, $V_{CM\ min} \le V_{IN} \le V_{CM\ max}$		–95		dB
		INP = INN, f_{IN} from 0.1Hz to 50kHz, $V_{CM\ min} \le V_{IN} \le V_{CM\ max}$		–95		
BW	Input bandwidth			900		kHz
DC ACCURACY						
DNL	Differential nonlinearity	Resolution: 16 bits	–0.99		0.99	LSB
INL	Integral nonlinearity(3)	Resolution: 16 bits	–4	±1	4	LSB
E_O	Offset error(1)	INP = INN = AGND, T_A = 25°C	–100	±4.5	100	µV
TCE_O	Offset error temperature drift(4)		–1		1	µV/°C
E_G	Gain error	T_A = 25°C	–0.2%	±0.005%	0.2%	
TCE_G	Gain error temperature drift(5)		–40	±20	40	ppm/°C
PSRR	Power-supply rejection ratio	INP = INN = AGND, AVDD from 3.0V to 5.5V, at DC		–103		dB
		INP = INN = AGND, AVDD from 3.0V to 5.5V, 10kHz / 100mV ripple		–92		
AC ACCURACY						
SNR	Signal-to-noise ratio	f_{IN} = 1kHz	82	86		dB
SINAD	Signal-to-noise + distortion	f_{IN} = 1kHz	81.9	85.7		dB
THD	Total harmonic distortion(6)	4.5V ≤ AVDD ≤ 5.5V, f_{IN} = 1kHz, 5MHz ≤ f_{CLKIN} ≤ 21MHz		–98	–86	dB
		3.0V ≤ AVDD ≤ 3.6V, f_{IN} = 1kHz, 5MHz ≤ f_{CLKIN} ≤ 20MHz		–93	–85	
SFDR	Spurious-free dynamic range	f_{IN} = 1kHz	83	100		dB
CMOS LOGIC WITH SCHMITT-TRIGGER						
I_{IN}	Input current	DGND ≤ V_{IN} ≤ DVDD	0		7	µA
C_{IN}	Input capacitance			4		pF
V_{IH}	High-level input voltage		0.7 × DVDD		DVDD + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.3 × DVDD	V
C_{LOAD}	Output load capacitance			30		pF
V_{OH}	High-level output voltage	I_{OH} = –20µA	DVDD – 0.1			V

minimum and maximum specifications are at T_A = –40°C to 125°C, AVDD = 3.0V to 5.5V, DVDD = 2.7V to 5.5V, AINP = –250mV to 250mV, AINN = AGND, and $sinc^3$ filter with OSR = 256 (unless otherwise noted); typical specifications are at T_A = 25°C, CLKIN = 20MHz, AVDD = 5V, and DVDD = 3.3V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4mA	DVDD – 0.4			V
V_{OL}	Low-level output voltage	I_{OL} = 20µA			0.1	V
V_{OL}	Low-level output voltage	I_{OL} = 4mA			0.4	V
POWER SUPPLY						
I_{AVDD}	High-side supply current	3.0V ≤ AVDD ≤ 3.6V		6.3	8.5	mA
		4.5V ≤ AVDD ≤ 5.5V		7.2	9.8	
I_{DVDD}	Low-side supply current	AMC1306Ex, 2.7V ≤ DVDD ≤ 3.6V, C_{LOAD} = 15pF		4.1	5.5	mA
	Low-side supply current	AMC1306Mx, 2.7V ≤ DVDD ≤ 3.6V, C_{LOAD} = 15pF		3.3	4.8	mA
	Low-side supply current	AMC1306Ex, 4.5V ≤ DVDD ≤ 5.5V, C_{LOAD} = 15pF		5.0	6.9	mA
	Low-side supply current	AMC1306Mx, 4.5V ≤ DVDD ≤ 5.5V, C_{LOAD} = 15pF		3.9	6.0	mA

(1) This parameter is input referred.
(2) Integral nonlinearity is defined as the maximum deviation from a straight line passing through the end-points of the ideal ADC transfer function expressed as number of LSBs or as a percent of the specified linear full-scale range FSR.
(3) Offset error temperature drift is calculated using the box method, as described by the following equation: $TCE_O = (E_{O,MAX} – E_{O,MIN}) / TempRange$ where $E_{O,MAX}$ and $E_{O,MIN}$ refer to the maximum and minimum E_O values measured within the temperature range (–40 to 125°C).
(4) Gain error temperature drift is calculated using the box method, as described by the following equation: $TCE_G\ (ppm) = ((E_{G,MAX} - E_{G,MIN}) / TempRange) \times 10^4$ where $E_{G,MAX}$ and $E_{G,MIN}$ refer to the maximum and minimum E_G values (in %) measured within the temperature range (–40 to 125°C).
(5) THD is the ratio of the rms sum of the amplitudes of first five higher harmonics to the amplitude of the fundamental.

6.11 Switching Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_H	DOUT hold time after rising edge of CLKIN	C_{LOAD} = 15pF	3.5			ns
t_D	Rising edge of CLKIN to DOUT valid delay	C_{LOAD} = 15 pF			15	ns
t_r	DOUT rise time	10% to 90%, 2.7V ≤ DVDD ≤ 3.6V, C_{LOAD} = 15pF		0.8	3.5	ns
		10% to 90%, 4.5V ≤ DVDD ≤ 5.5V, C_{LOAD} = 15pF		1.8	3.9	
t_f	DOUT fall time	10% to 90%, 2.7V ≤ DVDD ≤ 3.6V, C_{LOAD} = 15pF		0.8	3.5	ns
		10% to 90%, 4.5V ≤ DVDD ≤ 5.5V, C_{LOAD} = 15pF		1.8	3.9	
t_{ISTART}	Interface startup time	DVDD at 2.7V (min) to DOUT valid with AVDD ≥ 3.0V	32		32	CLKIN cycles
t_{START}	Analog start-up time	AVDD step from 0 to 3.0V with DVDD ≥ 2.7V to bitstream valid, 0.1% settling		0.5		ms

6.12 Timing Diagrams

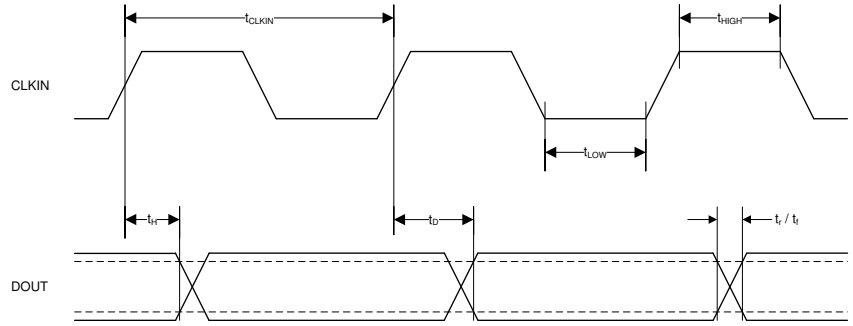


Figure 6-1. Digital Interface Timing

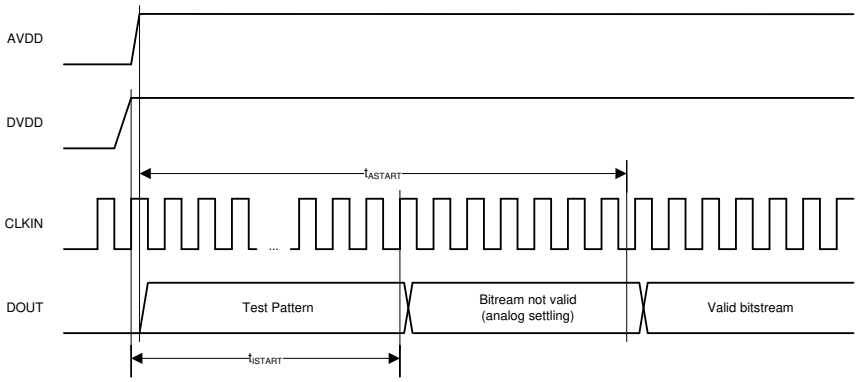


Figure 6-2. Device Startup Timing

6.13 Insulation Characteristics Curves

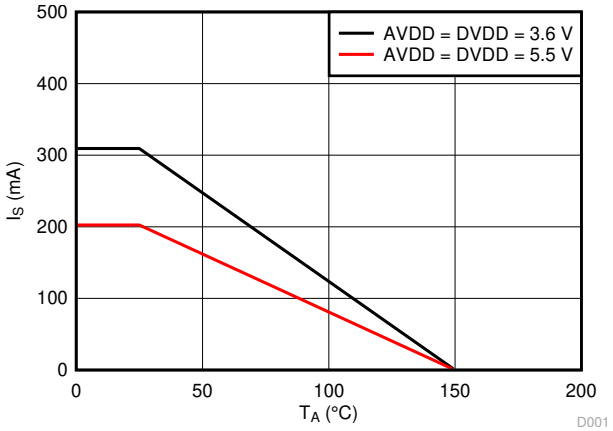


Figure 6-3. Thermal Derating Curve for Safety-Limiting Current per VDE

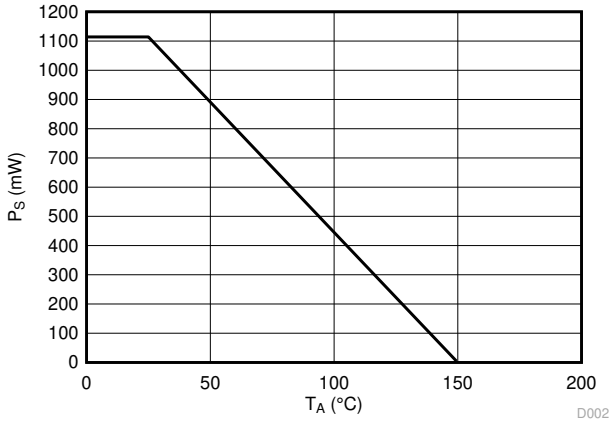
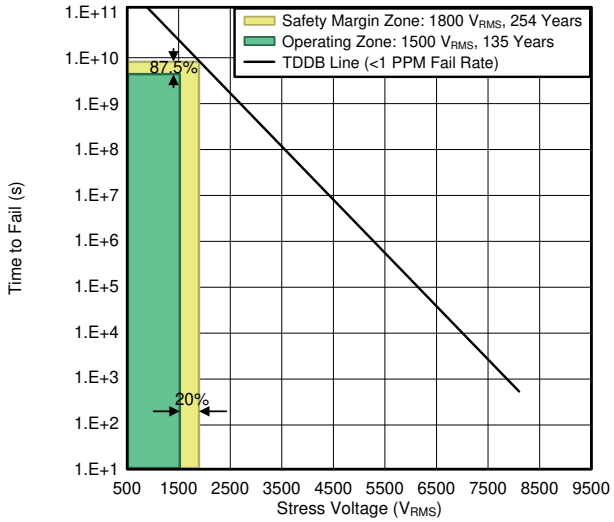


Figure 6-4. Thermal Derating Curve for Safety-Limiting Power per VDE



T_A up to 150°C, stress-voltage frequency = 60Hz, isolation working voltage = 1500V_{RMS}, operating lifetime = 135 years

Figure 6-5. Reinforced Isolation Capacitor Lifetime Projection

6.14 Typical Characteristics

at AVDD = 5V, DVDD = 3.3V, AINP = –50mV to 50mV (AMC1306x05) or –250mV to 250mV (AMC1306x25), AINN = AGND, f_{CLKIN} = 20MHz, and $sinc^3$ filter with OSR = 256 (unless otherwise noted)

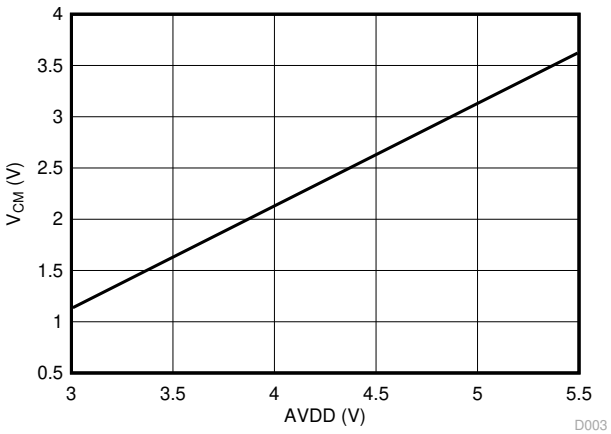


Figure 6-6. Maximum Operating Common-Mode Input Voltage vs High-Side Supply Voltage

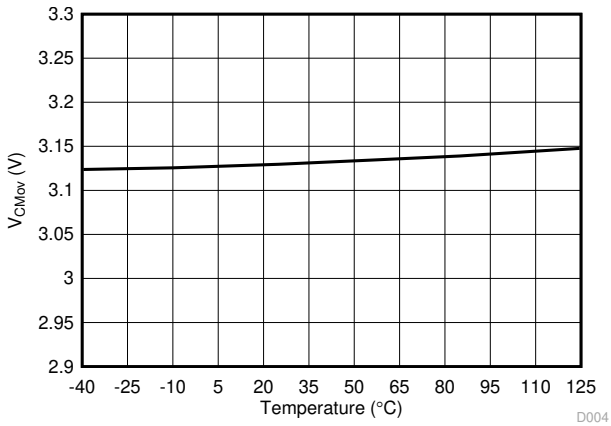


Figure 6-7. Common-Mode Overvoltage Detection Level vs Temperature

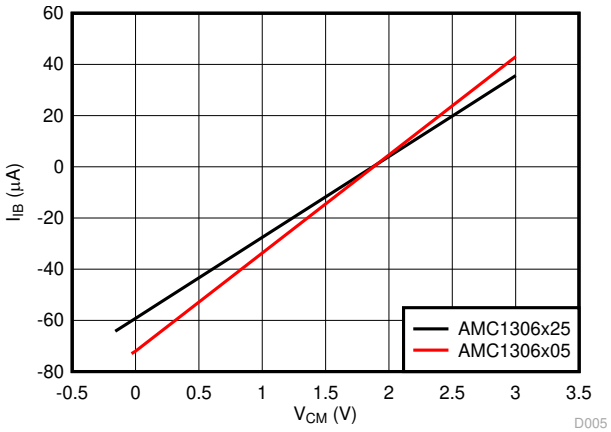


Figure 6-8. Input Bias Current vs Common-Mode Input Voltage

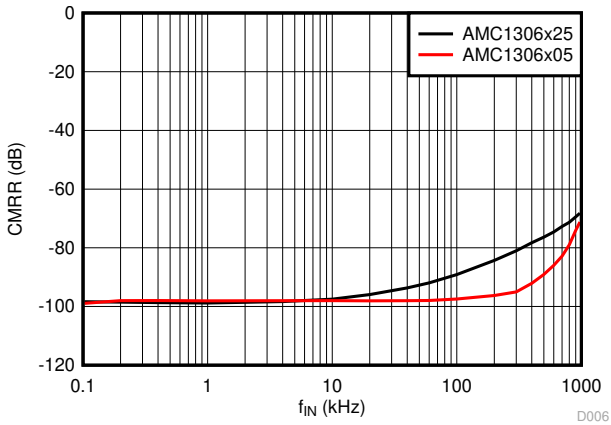


Figure 6-9. Common-Mode Rejection Ratio vs Input Signal Frequency

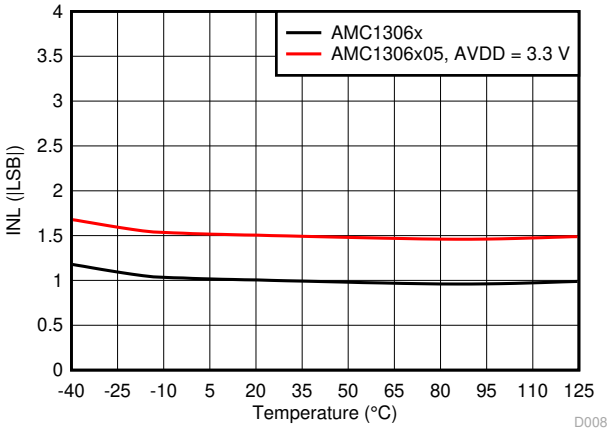


Figure 6-10. Integral Nonlinearity vs Temperature

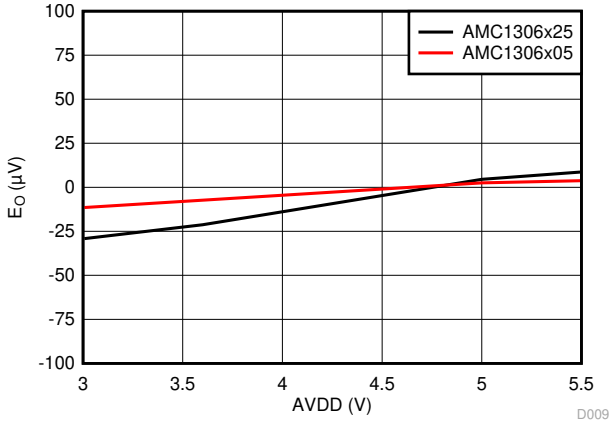


Figure 6-11. Offset Error vs High-Side Supply Voltage

6.14 Typical Characteristics (continued)

at AVDD = 5V, DVDD = 3.3V, AINP = –50mV to 50mV (AMC1306x05) or –250mV to 250mV (AMC1306x25), AINN = AGND, f_{CLKIN} = 20MHz, and sinc^3 filter with OSR = 256 (unless otherwise noted)

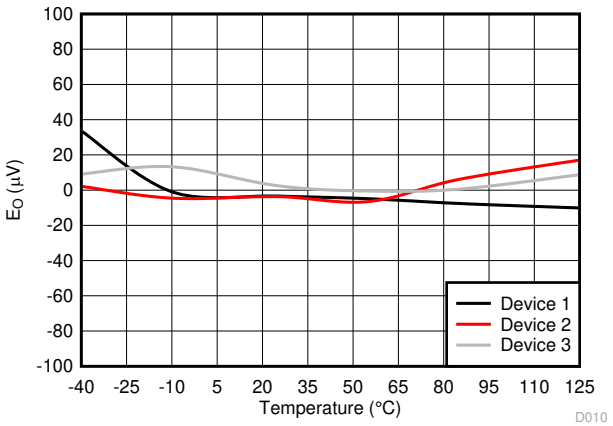


Figure 6-12. Offset Error vs Temperature

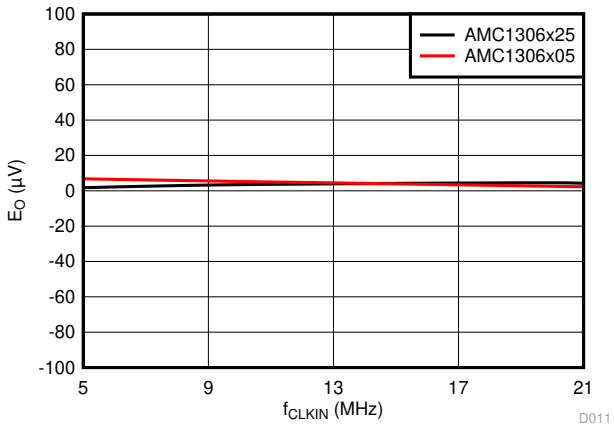


Figure 6-13. Offset Error vs Clock Frequency

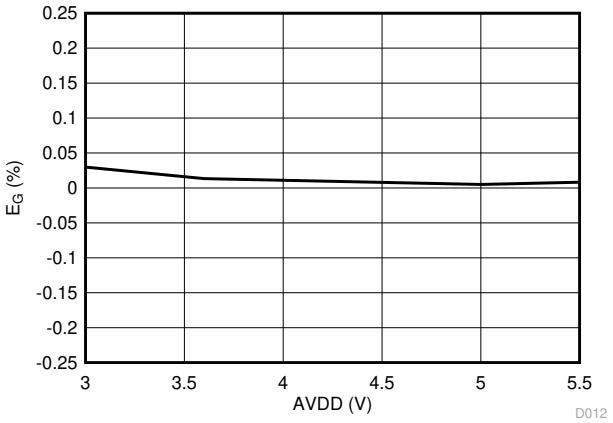


Figure 6-14. Gain Error vs High-Side Supply Voltage

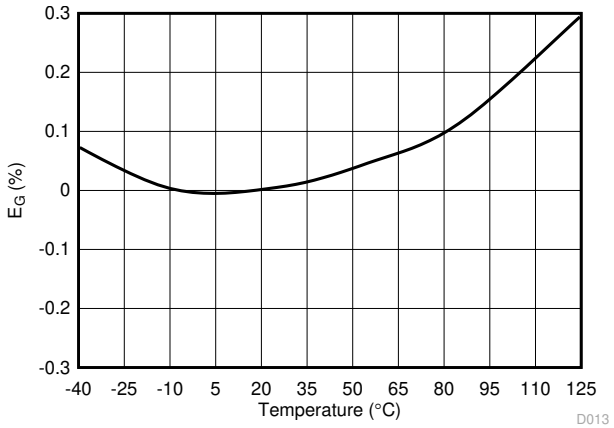


Figure 6-15. Gain Error vs Temperature

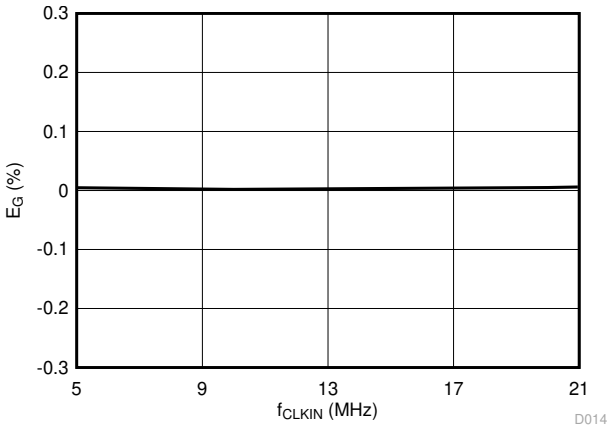


Figure 6-16. Gain Error vs Clock Frequency

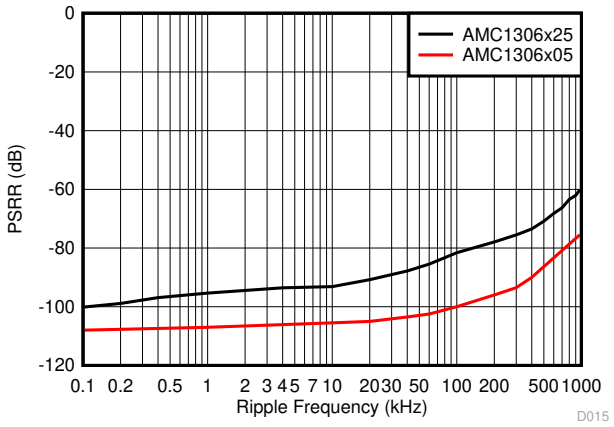


Figure 6-17. Power-Supply Rejection Ratio vs Ripple Frequency

6.14 Typical Characteristics (continued)

at AVDD = 5V, DVDD = 3.3V, AINP = –50mV to 50mV (AMC1306x05) or –250mV to 250mV (AMC1306x25), AINN = AGND, f_{CLKIN} = 20MHz, and $sinc^3$ filter with OSR = 256 (unless otherwise noted)

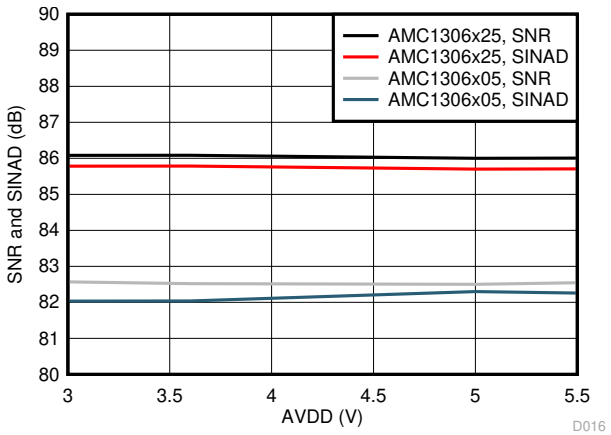


Figure 6-18. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs High-Side Supply Voltage

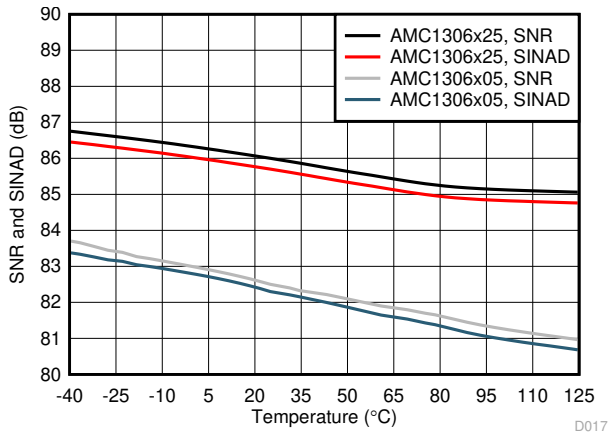


Figure 6-19. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Temperature

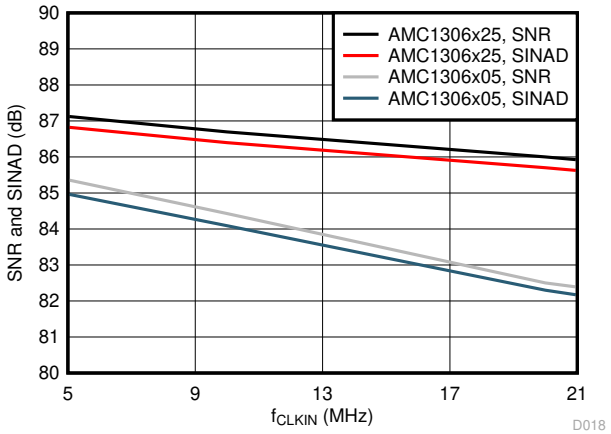


Figure 6-20. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Clock Frequency

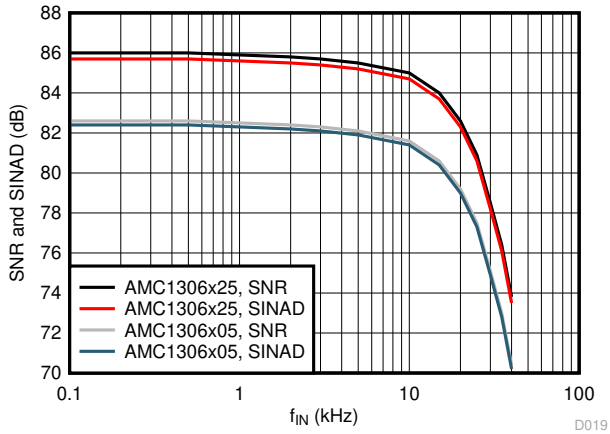


Figure 6-21. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Input Signal Frequency

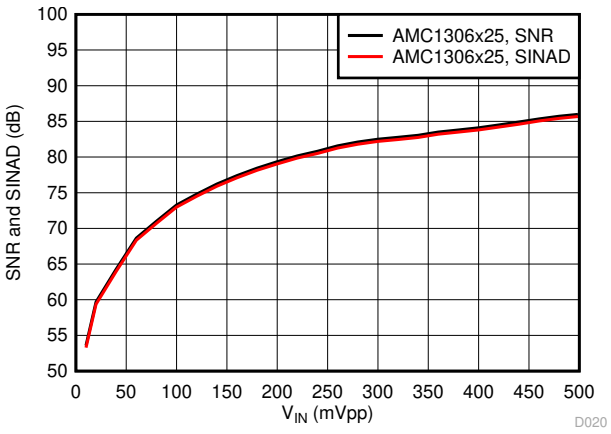


Figure 6-22. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Input Signal Amplitude

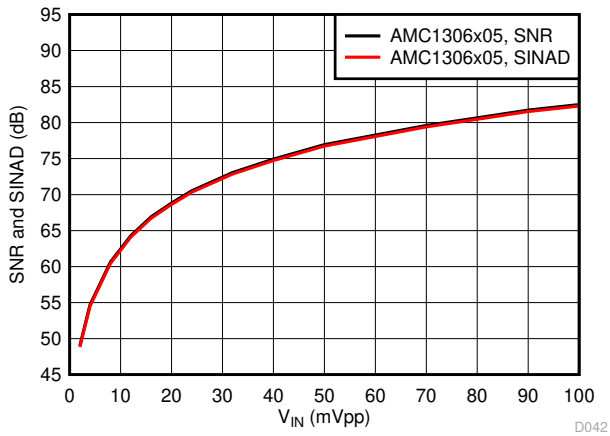
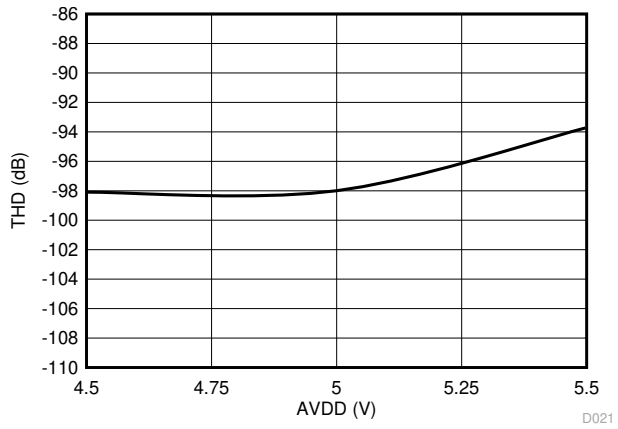


Figure 6-23. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Input Signal Amplitude

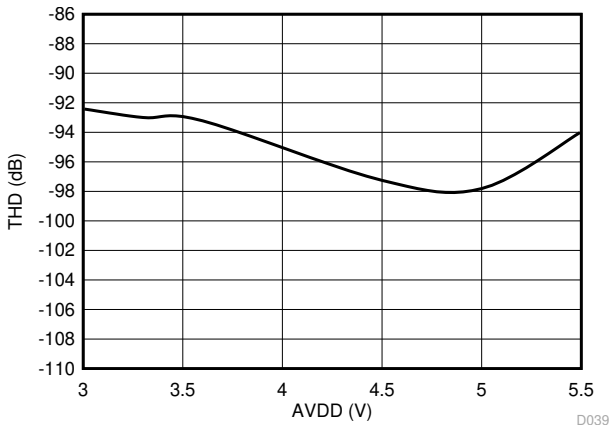
6.14 Typical Characteristics (continued)

at AVDD = 5V, DVDD = 3.3V, AINP = –50mV to 50mV (AMC1306x05) or –250mV to 250mV (AMC1306x25), AINN = AGND, f_{CLKIN} = 20MHz, and sinc^3 filter with OSR = 256 (unless otherwise noted)



f_{CLKIN} = 21MHz

Figure 6-24. Total Harmonic Distortion vs High-Side Supply Voltage (5V, nom)



f_{CLKIN} = 20MHz

Figure 6-25. Total Harmonic Distortion vs High-Side Supply Voltage (3.3V, nom)

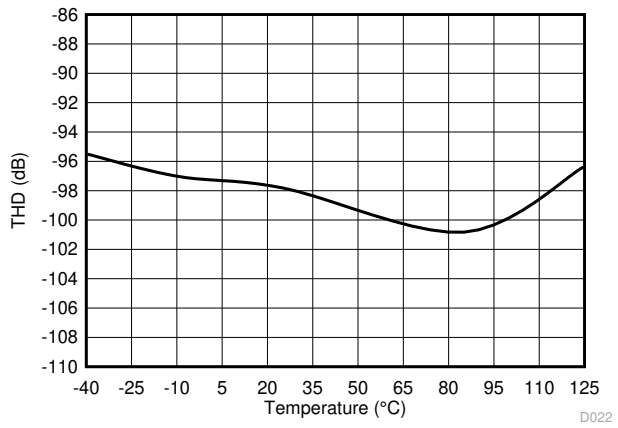


Figure 6-26. Total Harmonic Distortion vs Temperature

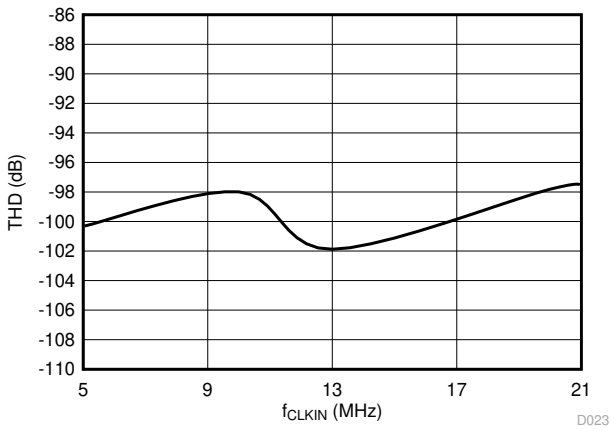


Figure 6-27. Total Harmonic Distortion vs Clock Frequency

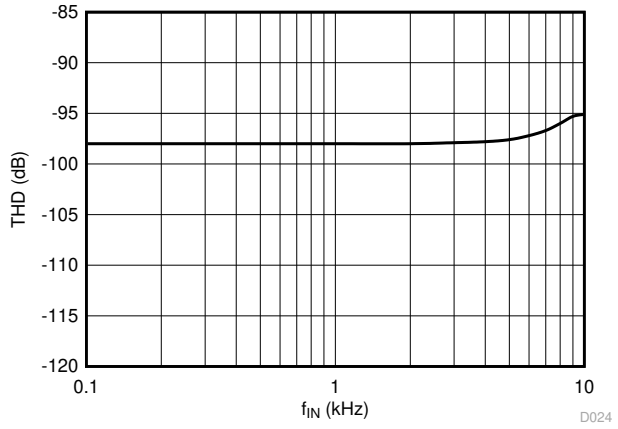
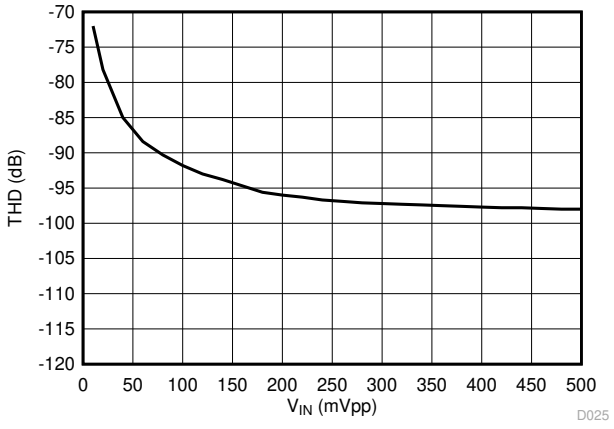


Figure 6-28. Total Harmonic Distortion vs Input Signal Frequency

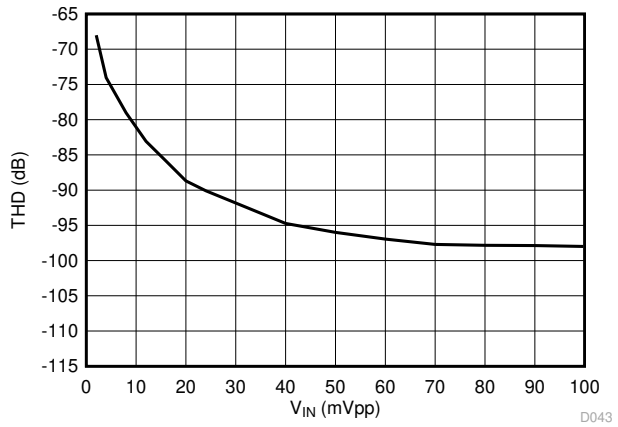


AMC1306x25

Figure 6-29. Total Harmonic Distortion vs Input Signal Amplitude

6.14 Typical Characteristics (continued)

at AVDD = 5V, DVDD = 3.3V, AINP = –50mV to 50mV (AMC1306x05) or –250mV to 250mV (AMC1306x25), AINN = AGND, f_{CLKIN} = 20MHz, and sinc^3 filter with OSR = 256 (unless otherwise noted)



AMC1306x05

Figure 6-30. Total Harmonic Distortion vs Input Signal Amplitude

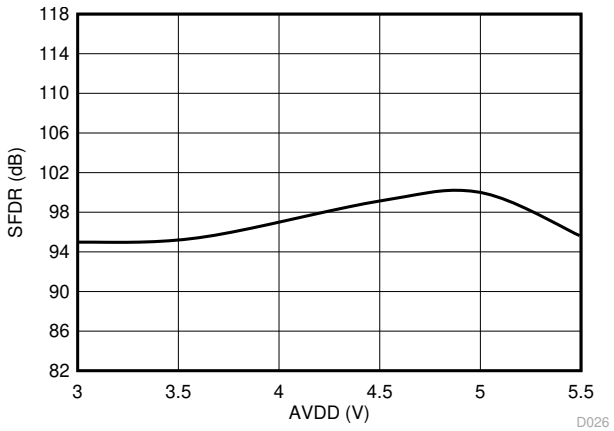


Figure 6-31. Spurious-Free Dynamic Range vs High-Side Supply Voltage

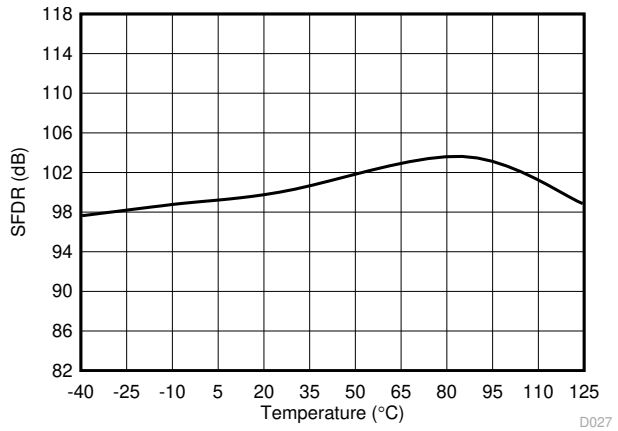


Figure 6-32. Spurious-Free Dynamic Range vs Temperature

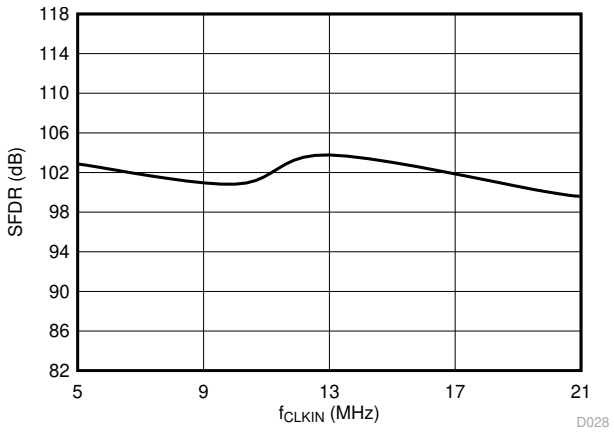


Figure 6-33. Spurious-Free Dynamic Range vs Clock Frequency

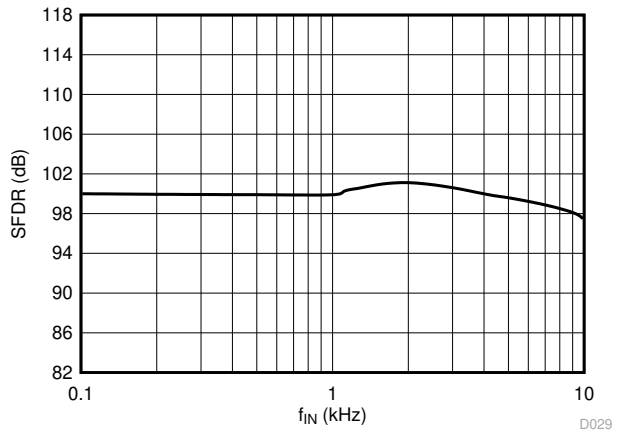
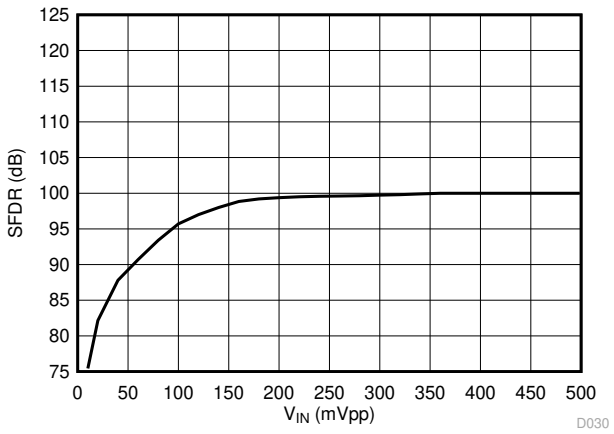


Figure 6-34. Spurious-Free Dynamic Range vs Input Signal Frequency

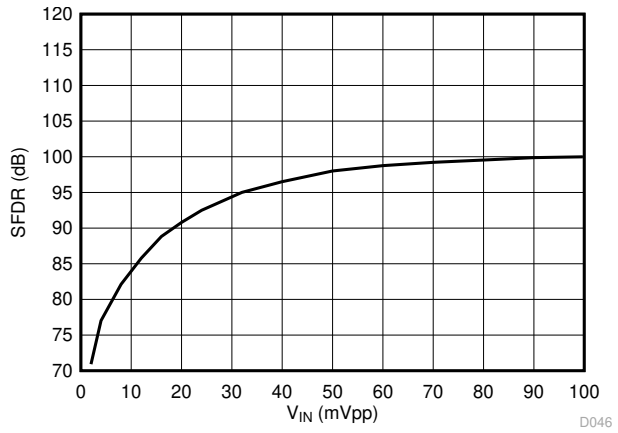


AMC1306x25

Figure 6-35. Spurious-Free Dynamic Range vs Input Signal Amplitude

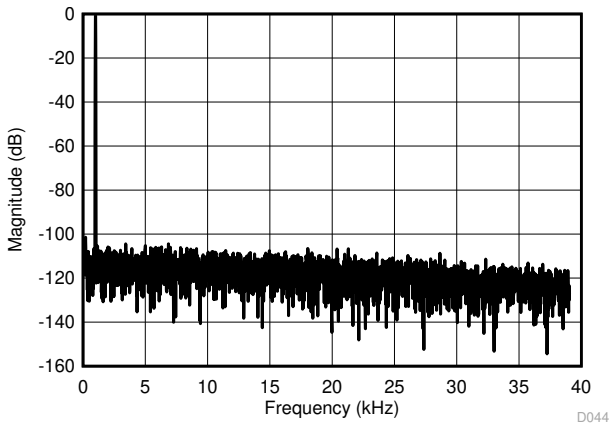
6.14 Typical Characteristics (continued)

at AVDD = 5V, DVDD = 3.3V, AINP = –50mV to 50mV (AMC1306x05) or –250mV to 250mV (AMC1306x25), AINN = AGND, f_{CLKIN} = 20MHz, and sinc^3 filter with OSR = 256 (unless otherwise noted)



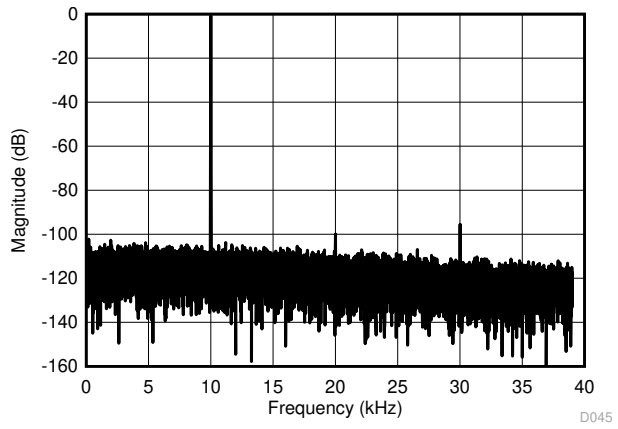
AMC1306x05

Figure 6-36. Spurious-Free Dynamic Range vs Input Signal Amplitude



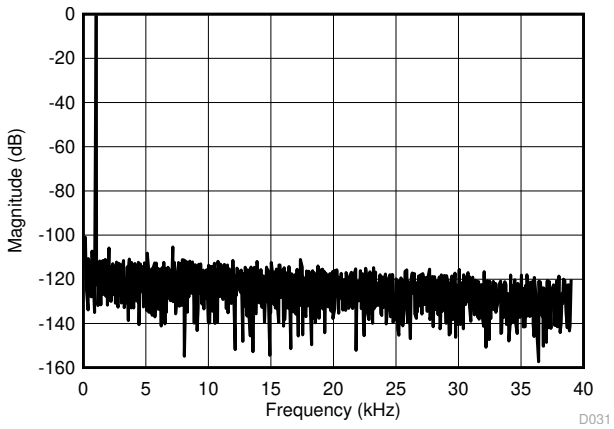
AMC1306x05, 4096-point FFT, V_{IN} = 100mV$_{PP}$

Figure 6-37. Frequency Spectrum with 1kHz Input Signal



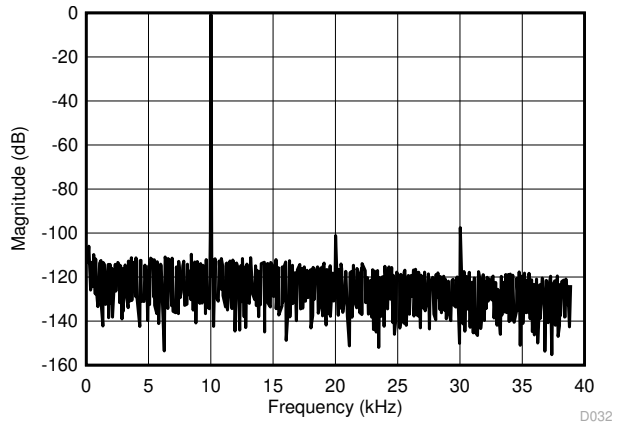
AMC1306x05, 4096-point FFT, V_{IN} = 100mV$_{PP}$

Figure 6-38. Frequency Spectrum with 10kHz Input Signal



AMC1306x25, 4096-point FFT, V_{IN} = 500mV$_{PP}$

Figure 6-39. Frequency Spectrum with 1kHz Input Signal



AMC1306x25, 4096-point FFT, V_{IN} = 500mV$_{PP}$

Figure 6-40. Frequency Spectrum with 10kHz Input Signal

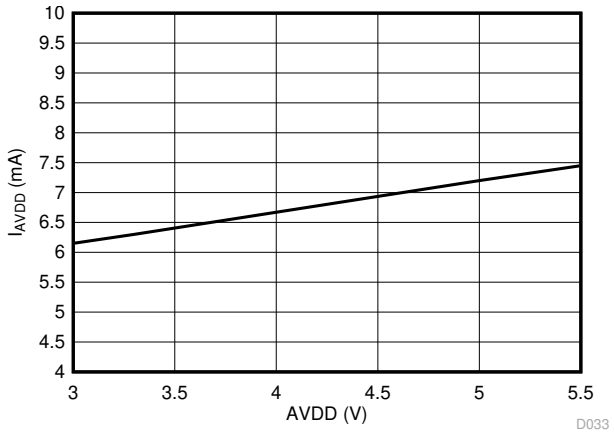


Figure 6-41. High-Side Supply Current vs High-Side Supply Voltage

6.14 Typical Characteristics (continued)

at AVDD = 5V, DVDD = 3.3V, AINP = –50mV to 50mV (AMC1306x05) or –250mV to 250mV (AMC1306x25), AINN = AGND, f_{CLKIN} = 20MHz, and $sinc^3$ filter with OSR = 256 (unless otherwise noted)

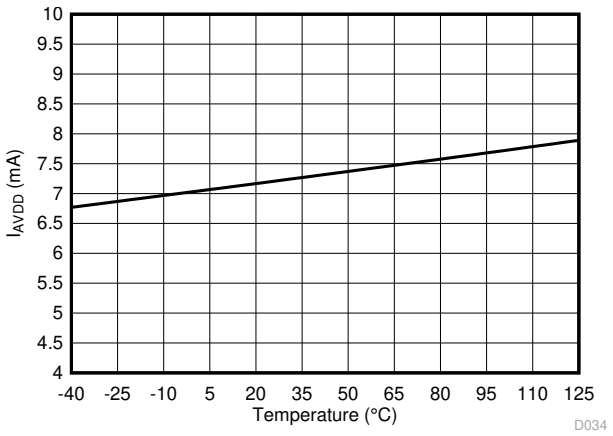


Figure 6-42. High-Side Supply Current vs Temperature

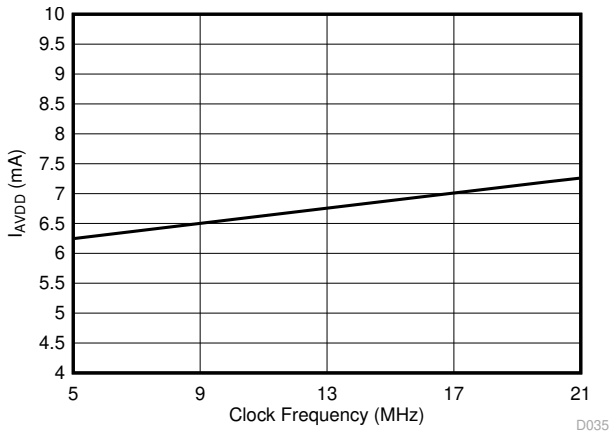


Figure 6-43. High-Side Supply Current vs Clock Frequency

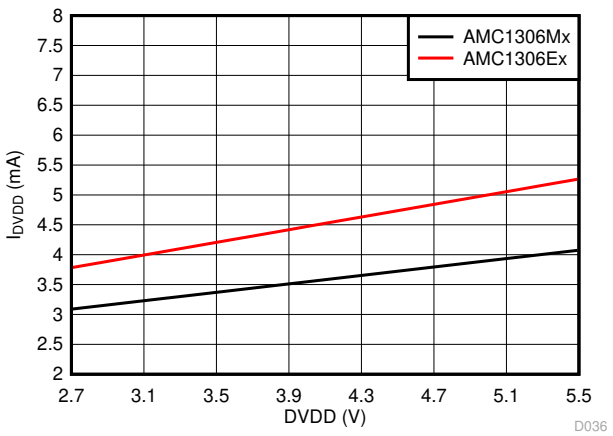


Figure 6-44. Controller-Side Supply Current vs Controller-Side Supply Voltage

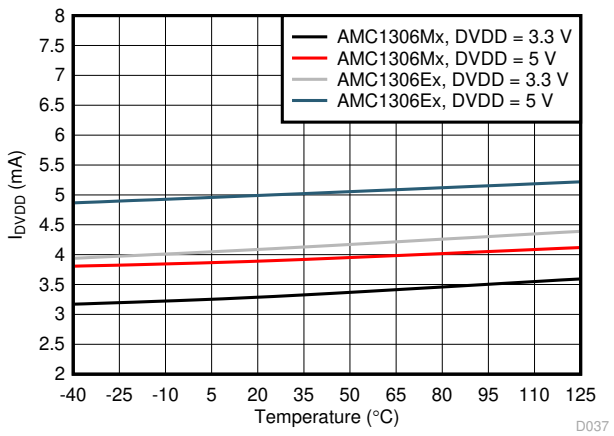


Figure 6-45. Controller-Side Supply Current vs Temperature

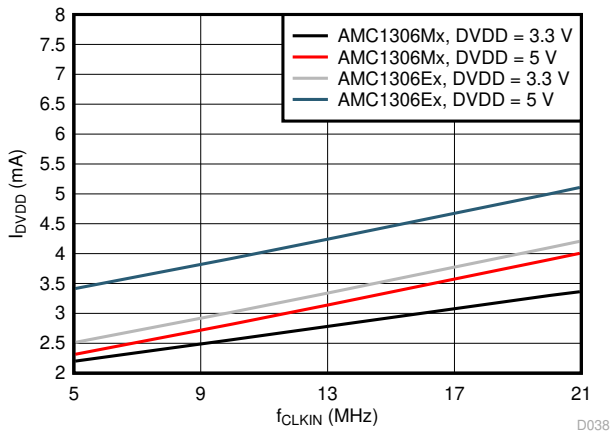


Figure 6-46. Controller-Side Supply Current vs Clock Frequency

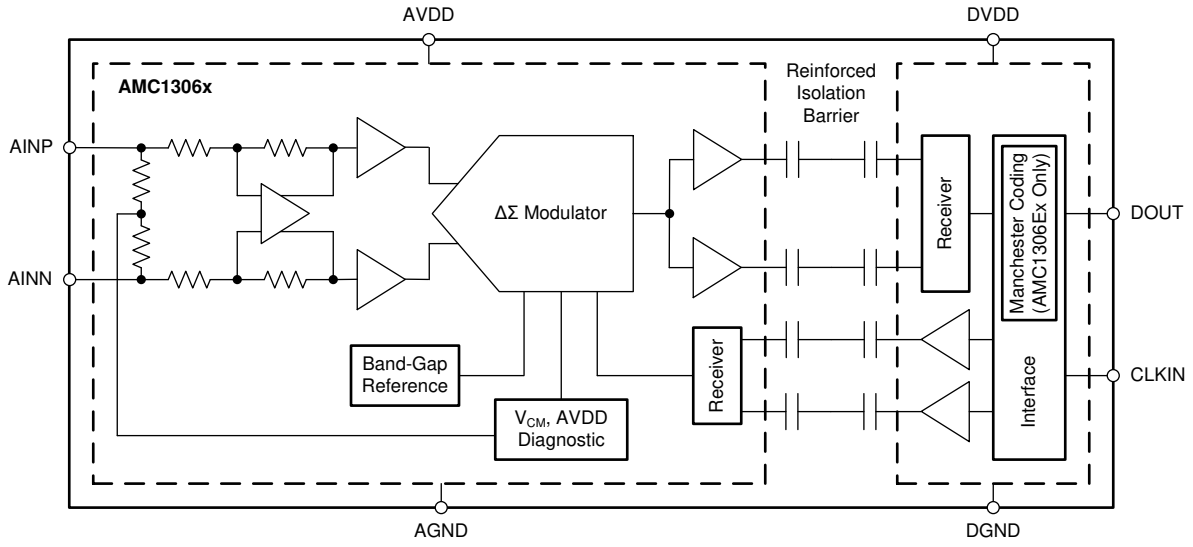
7 Detailed Description

7.1 Overview

The differential analog input (comprised of input signals AINP and AINN) of the AMC1306 is a fully-differential amplifier feeding the switched-capacitor input of a second-order, delta-sigma (ΔΣ) modulator stage that digitizes the input signal into a 1-bit output stream. The isolated data output DOUT of the converter provides a stream of digital ones and zeros that is synchronous to the externally-provided clock source at the CLKIN pin with a frequency in the range of 5MHz to 21MHz. The time average of this serial bitstream output is proportional to the analog input voltage.

The *Functional Block Diagram* shows a detailed block diagram of the AMC1306. The analog input range is tailored to directly accommodate a voltage drop across a shunt resistor used for current sensing. The silicon-dioxide (SiO_2) based capacitive isolation barrier supports a high level of magnetic field immunity as described in the *ISO72x Digital Isolator Magnetic-Field Immunity* application report, available for download at www.ti.com. The external clock input simplifies the synchronization of multiple current-sensing channels on the system level. The extended frequency range of up to 21MHz supports higher performance levels compared to the other designs available on the market.

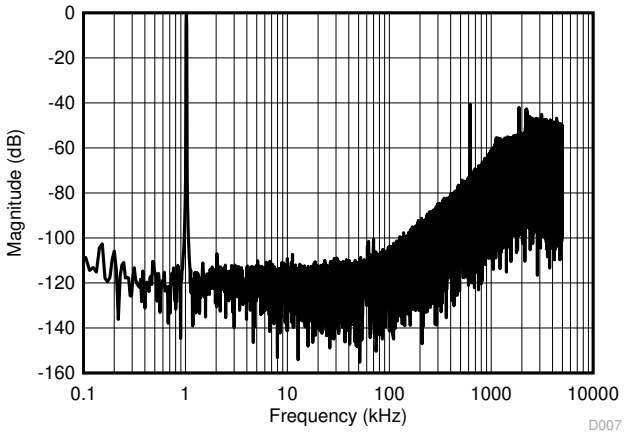
7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Analog Input

The AMC1306 incorporates front-end circuitry that contains a differential amplifier and a sampling stage, followed by a ΔΣ modulator. The gain of the differential amplifier is set by internal precision resistors to a factor of 4 for devices with a specified input voltage range of ±250mV (this value is for the AMC1306x25), or to a factor of 20 in devices with a ±50mV input voltage range (for the AMC1306x05), resulting in a differential input impedance of 4.9kΩ (for the AMC1306x05) or 22kΩ (for the AMC1306x25). For reduced offset and offset drift, the differential amplifier is chopper-stabilized with the switching frequency set at f_{CLKIN} / 32. The switching frequency generates a spur as shown in Figure 7-1.



sinc^3 filter, OSR = 2, f_{CLKIN} = 20MHz, f_{IN} = 1kHz

Figure 7-1. Quantization Noise Shaping

Consider the input impedance of the AMC1306 in designs with high-impedance signal sources that can cause degradation of gain and offset specifications. The importance of this effect, however, depends on the desired system performance. Additionally, the input bias current caused by the internal common-mode voltage at the output of the differential amplifier is dependent on the actual amplitude of the input signal; see the *Section 8.2.2* section for more details on reducing these effects.

There are two restrictions on the analog input signals (AINP and AINN). First, if the input voltage exceeds the range AGND – 6V to AVDD + 0.5V, the input current must be limited to 10mA because the device input electrostatic discharge (ESD) diodes turn on. In addition, the linearity and noise performance of the device are ensured only when the differential analog input voltage remains within the specified linear full-scale range (FSR), that is ±250mV (for the AMC1306x25) or ±50mV (for the AMC1306x05), and within the specified input common-mode range.

7.3.2 Modulator

The modulator implemented in the AMC1306 is a second-order, switched-capacitor, feed-forward ΔΣ modulator, such as the one conceptualized in Figure 7-2. The analog input voltage V_{IN} and the output V_5 of the 1-bit digital-to-analog converter (DAC) are differentiated, providing an analog voltage V_1 at the input of the first integrator stage. The output of the first integrator feeds the input of the second integrator stage, resulting in output voltage V_3 that is differentiated with the input signal V_{IN} and the output of the first integrator V_2. Depending on the polarity of the resulting voltage V_4, the output of the comparator is changed. In this case, the 1-bit DAC responds on the next clock pulse by changing the associated analog output voltage V_5, causing the integrators to progress in the opposite direction and forcing the value of the integrator output to track the average value of the input.

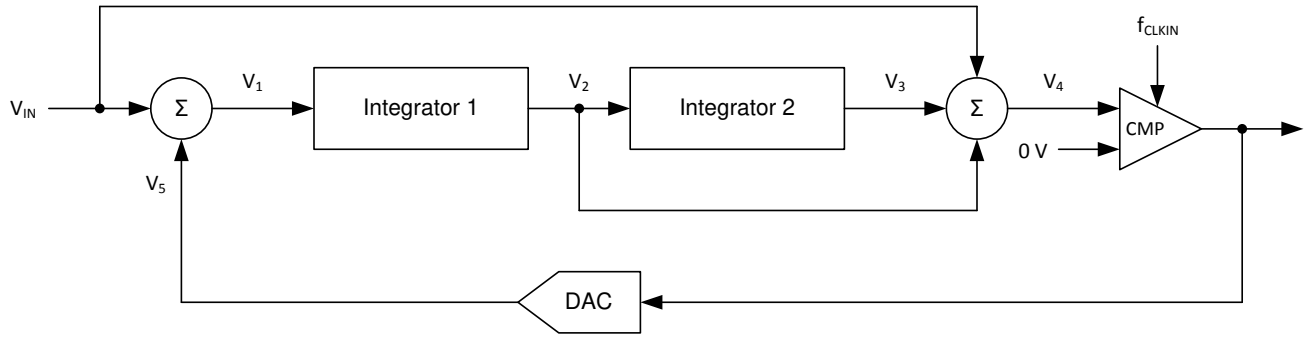


Figure 7-2. Block Diagram of a Second-Order Modulator

The modulator shifts the quantization noise to high frequencies, as shown in Figure 7-2. Therefore, use a low-pass digital filter at the output of the device to increase the overall performance. This filter is also used to convert from the 1-bit data stream at a high sampling rate into a higher-bit data word at a lower rate (decimation). TI's microcontroller families TMS320F2807x and TMS320F2837x offer a good programmable, hardwired filter structure termed a *sigma-delta filter module* (SDFM) designed for usage with the AMC1306 family. Also, SD24_B converters on the MSP430F677x microcontrollers offer a path to directly access the integrated sinc-filters for a simple system-level design for multichannel, isolated current sensing. An additional option is to use an appropriate application-specific device, such as the AMC1210 (a four-channel digital sinc-filter). Alternatively, a field-programmable gate array (FPGA) can be used to implement the filter.

7.3.3 Isolation Channel Signal Transmission

The AMC1306 device uses an on-off keying (OOK) modulation scheme to transmit the modulator output bitstream across the capacitive SiO_2-based isolation barrier. The transmitter modulates the bitstream at TX IN in Figure 7-3 with an internally-generated, 480MHz carrier across the isolation barrier to represent a digital *one* and sends a *no signal* to represent the digital *zero*. The receiver demodulates the signal after advanced signal conditioning and produces the output. The symmetrical design of each isolation channel improves the CMTI performance and reduces the radiated emissions caused by the high-frequency carrier. The block diagram of an isolation channel integrated in the AMC1306 is shown in Figure 7-3.

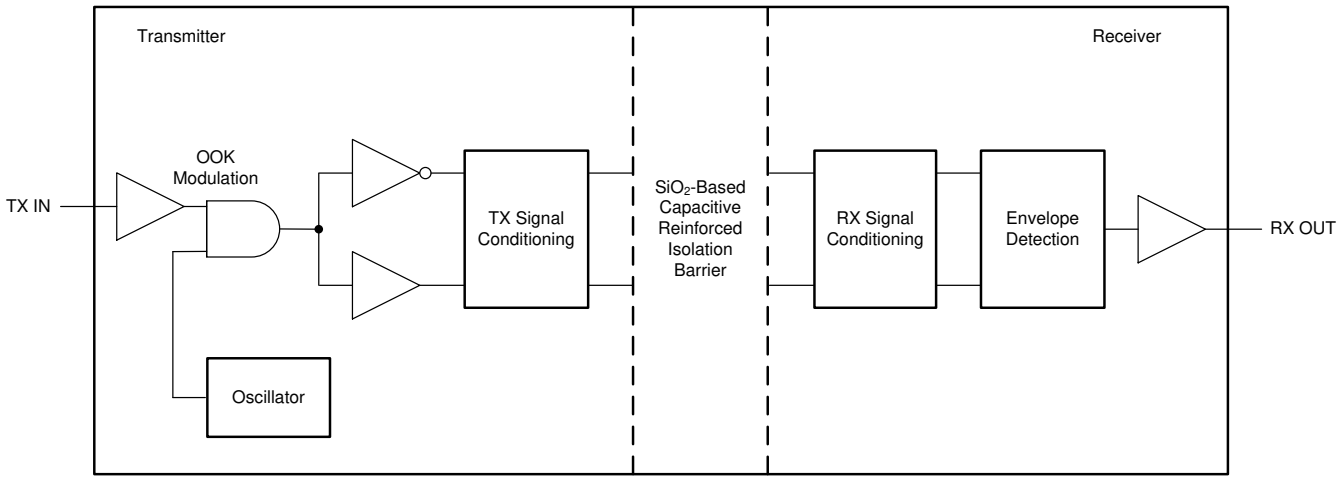


Figure 7-3. Block Diagram of an Isolation Channel

Figure 7-4 shows the concept of the on-off keying scheme.

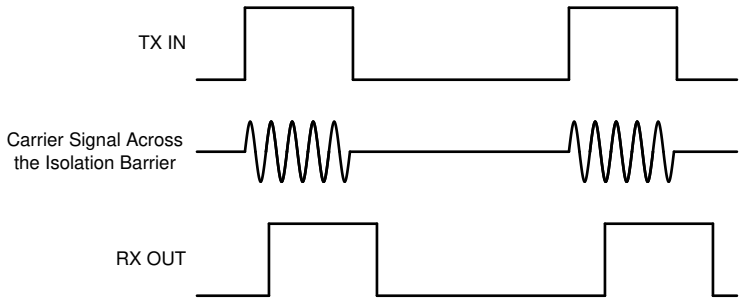


Figure 7-4. OOK-Based Modulation Scheme

7.3.4 Digital Output

A differential input signal of 0V ideally produces a stream of ones and zeros that are high 50% of the time. A differential input of 250mV (for the AMC1306x25) or 50mV (for the AMC1306x05) produces a stream of ones and zeros that are high 89.06% of the time. With 16 bits of resolution, that percentage ideally corresponds to the code 58368. A differential input of –250mV (–50mV for the AMC1306x05) produces a stream of ones and zeros that are high 10.94% of the time and ideally results in code 7168 with 16-bit resolution. These input voltages are also the specified linear ranges of the different AMC1306 versions with performance as specified in this document. If the input voltage value exceeds these ranges, the output of the modulator shows nonlinear behavior when the quantization noise increases. The output of the modulator clips with a stream of only zeros with an input less than or equal to –320mV (–64mV for the AMC1306x05) or with a stream of only ones with an input greater than or equal to 320mV (64mV for the AMC1306x05). In this case, however, the AMC1306 generates a single 1 (if the input is at negative full-scale) or 0 every 128 clock cycles to indicate proper device function (see the *Section 7.4.1* section for more details). The input voltage versus the output modulator signal is shown in Analog Input Versus the AMC1306 Modulator Output.

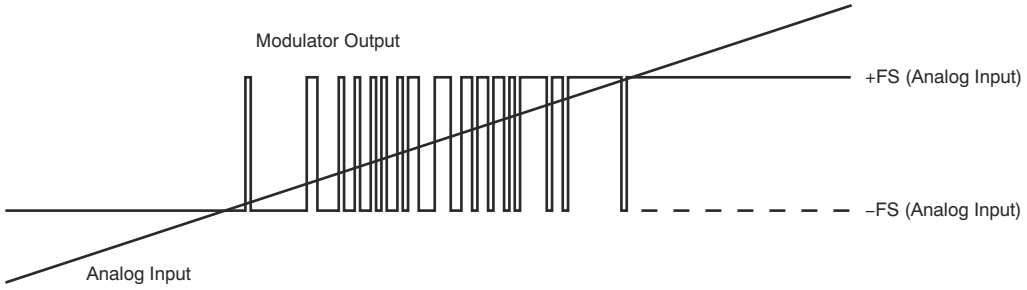


Figure 7-5. Analog Input Versus the AMC1306 Modulator Output

The density of ones in the output bitstream for any input voltage value (with the exception of a full-scale input signal, as described in the *Section 7.4.2* section) can be calculated using Equation 1:

$$\frac{V_{IN} + V_{Clipping}}{2 \times V_{Clipping}} \quad (1)$$

The AMC1306 system clock is provided externally at the CLKIN pin. For more details, see the *Switching Characteristics* table and the *Section 7.3.5* section.

7.3.5 Manchester Coding Feature

The AMC1306Ex offers the IEEE 802.3-compliant Manchester coding feature that generates at least one transition per bit to support clock signal recovery from the bitstream. A Manchester coded bitstream is free of dc components. The Manchester coding combines the clock and data information using exclusive or (XOR) logical operation and results in a bitstream as shown in Figure 7-6. The duty cycle of the Manchester encoded bitstream depends on the duty cycle of the input clock CLKIN.

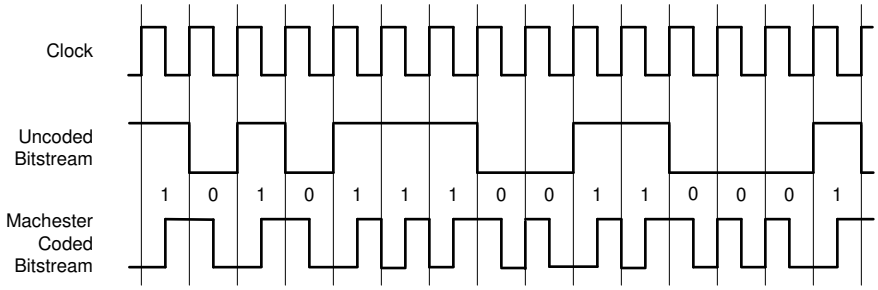


Figure 7-6. Manchester Coded Output of the AMC1306Ex

7.4 Device Functional Modes

7.4.1 Fail-Safe Output

In the case of a missing high-side supply voltage AVDD, the output of a ΔΣ modulator is not defined and can cause a system malfunction. In systems with high safety requirements, this behavior is not acceptable. Therefore, the AMC1306 implements a fail-safe output function that verifies that the output DOUT of the device offers a steady-state bitstream of logic 0s in case of a missing AVDD, as shown in Figure 7-7.

Additionally, if the common-mode voltage of the input reaches or exceeds the specified common-mode overvoltage detection level V_{CMov} as defined in the *Electrical Characteristics* table, the AMC1306 offers a steady-state bitstream of logic 1s at the output DOUT, as also shown in Figure 7-7.

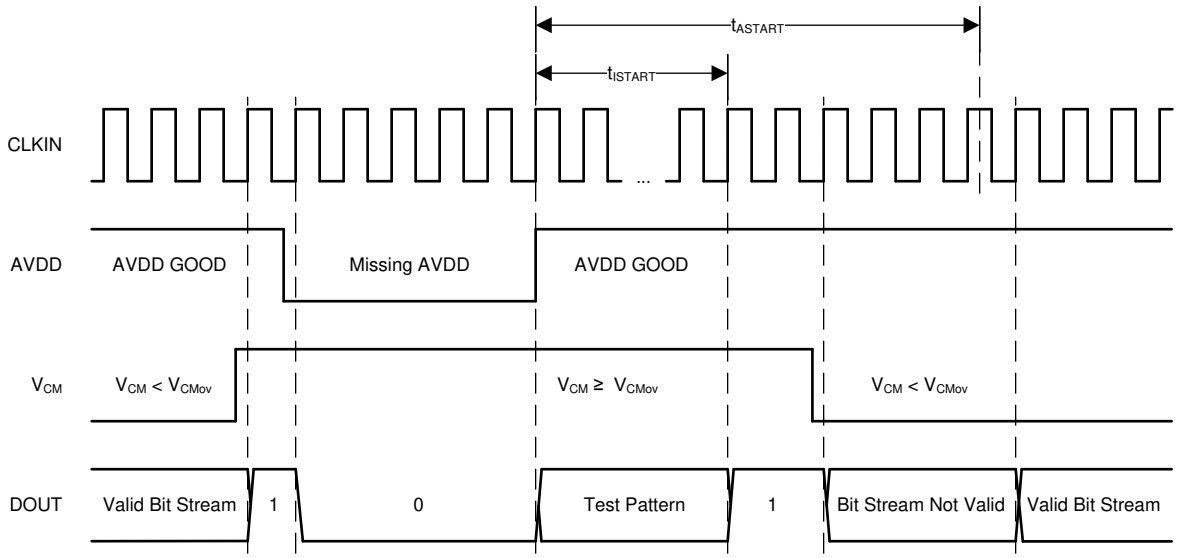


Figure 7-7. Fail-Safe Output of the AMC1306

7.4.2 Output Behavior in Case of a Full-Scale Input

If a full-scale input signal is applied to the AMC1306 (that is, $V_{IN} \geq V_{Clipping}$), the device generates a single one or zero every 128 bits at DOUT, depending on the actual polarity of the signal being sensed, as shown in Figure 7-8. In this way, differentiating between a missing AVDD and a full-scale input signal is possible on the system level.

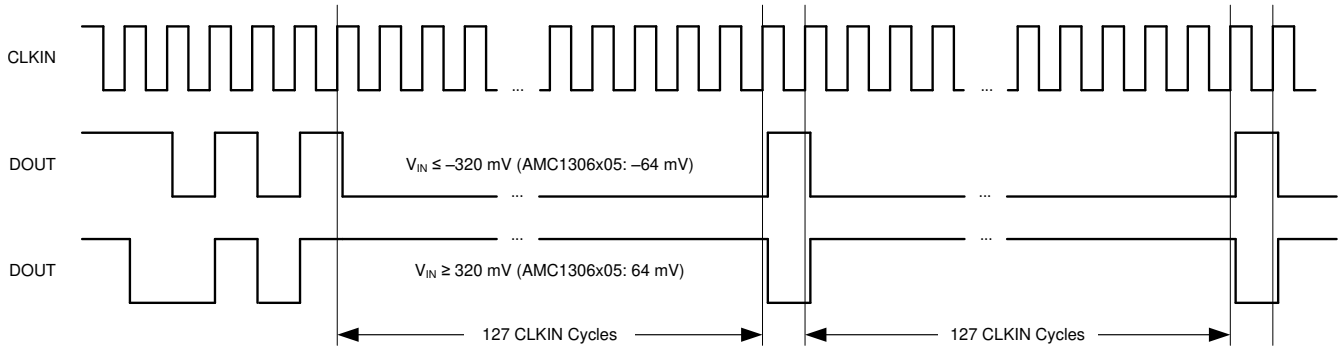


Figure 7-8. Overrange Output of the AMC1306

8 Application and Implementation

8.1 Application Information

8.1.1 Digital Filter Usage

The modulator generates a bitstream that is processed by a digital filter to obtain a digital word similar to a conversion result of a conventional analog-to-digital converter (ADC). A very simple filter, built with minimal effort and hardware, is a sinc^3-type filter, as shown in Equation 2:

$$H(z) = \left(\frac{1 - z^{-OSR}}{1 - z^{-1}} \right)^3 \quad (2)$$

This filter provides the best output performance at the lowest hardware size (count of digital gates) for a second-order modulator. All the characterization in this document is also done with a sinc^3 filter with an oversampling ratio (OSR) of 256 and an output word width of 16 bits.

The effective number of bits (ENOB) is often used to compare the performance of ADCs and ΔΣ modulators. Figure 8-1 shows the ENOB of the AMC1306 with different oversampling ratios. In this document, this number is calculated from the SINAD by using Equation 3:

$$SINAD = 1.76dB + 6.02dB \times ENOB \quad (3)$$

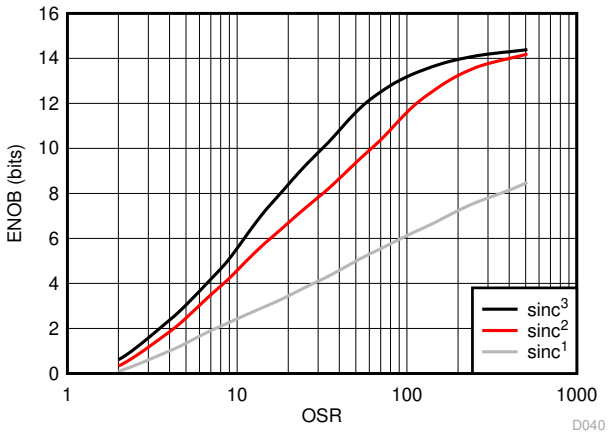


Figure 8-1. Measured Effective Number of Bits versus Oversampling Ratio

An example code for implementing a sinc^3 filter in an FPGA is discussed in the *Combining the ADS1202 with an FPGA Digital Filter for Current Measurement in Motor Control Applications* application note, available for download at www.ti.com.

8.2 Typical Applications

8.2.1 Frequency Inverter Application

Isolated ΔΣ modulators are being widely used in frequency inverter designs because of the high ac and dc performance. Frequency inverters are critical parts of industrial motor drives, photovoltaic inverters (string and central inverters), uninterruptible power supplies (UPS), electrical and hybrid electrical vehicles, and other industrial applications.

Figure 8-2 shows a simplified schematics of the AMC1306Mx in a typical frequency inverter application as used in industrial motor drives with shunt resistors (R_{SHUNT}) used for current sensing. Depending on the system design, either all three or only two motor phase currents are sensed. The Manchester coded bitstream output of the AMC1306Ex minimizes the wiring efforts of the connection between the power board and the control board; see Figure 8-3. This bitstream output also allows the clock to be generated locally on the power board without the having to adjust the propagation delay time of each DOUT connection to fulfill the setup and hold time requirements of the microcontroller.

In both examples, an additional fourth AMC1306 is used to support isolated voltage sensing of the dc link. This high voltage is reduced using a high-impedance resistive divider and is sensed by the device across a smaller resistor. The value of this resistor can degrade the performance of the measurement, as described in the *Section 8.2.2* section.

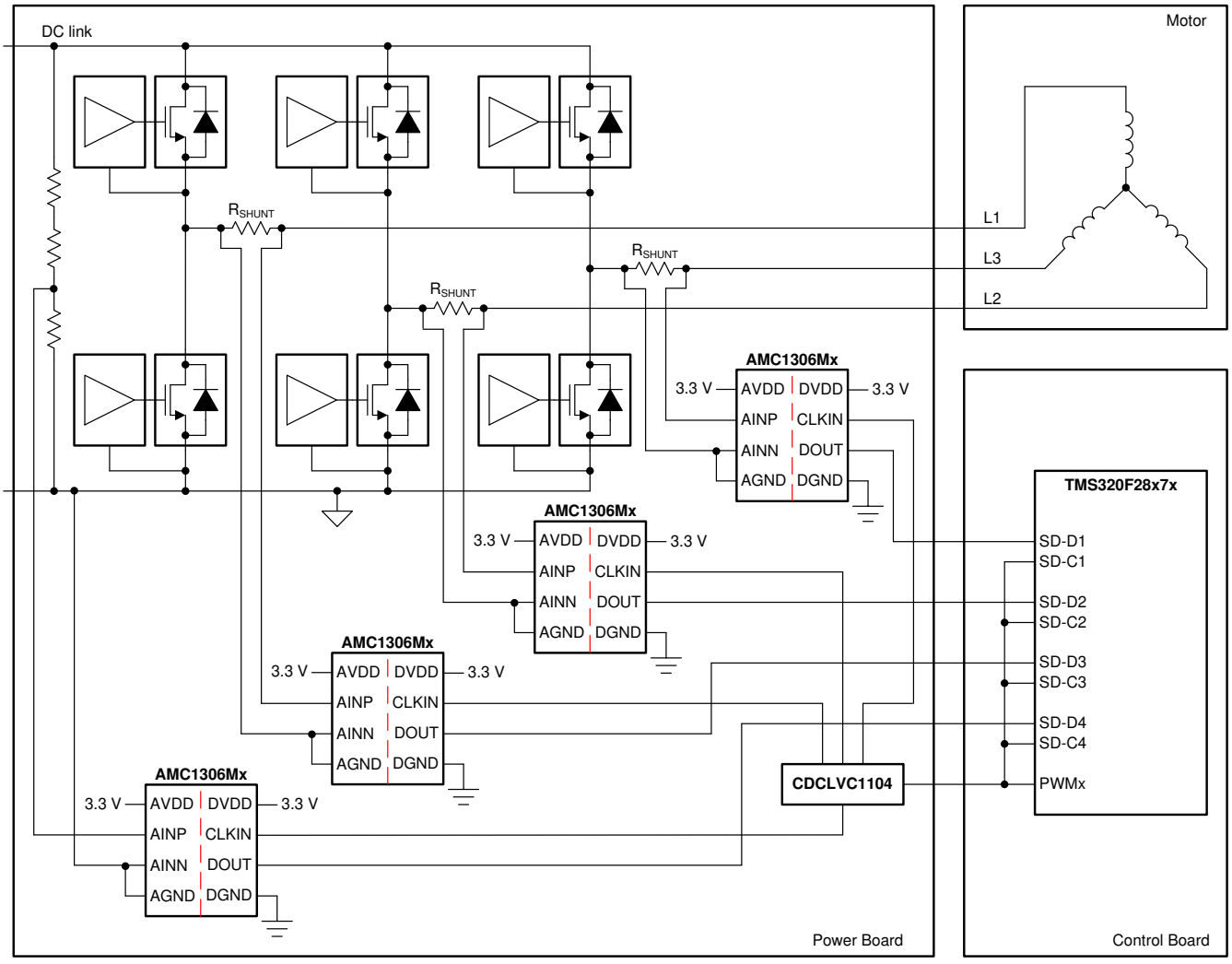


Figure 8-2. The AMC1306Mx in a Frequency Inverter Application

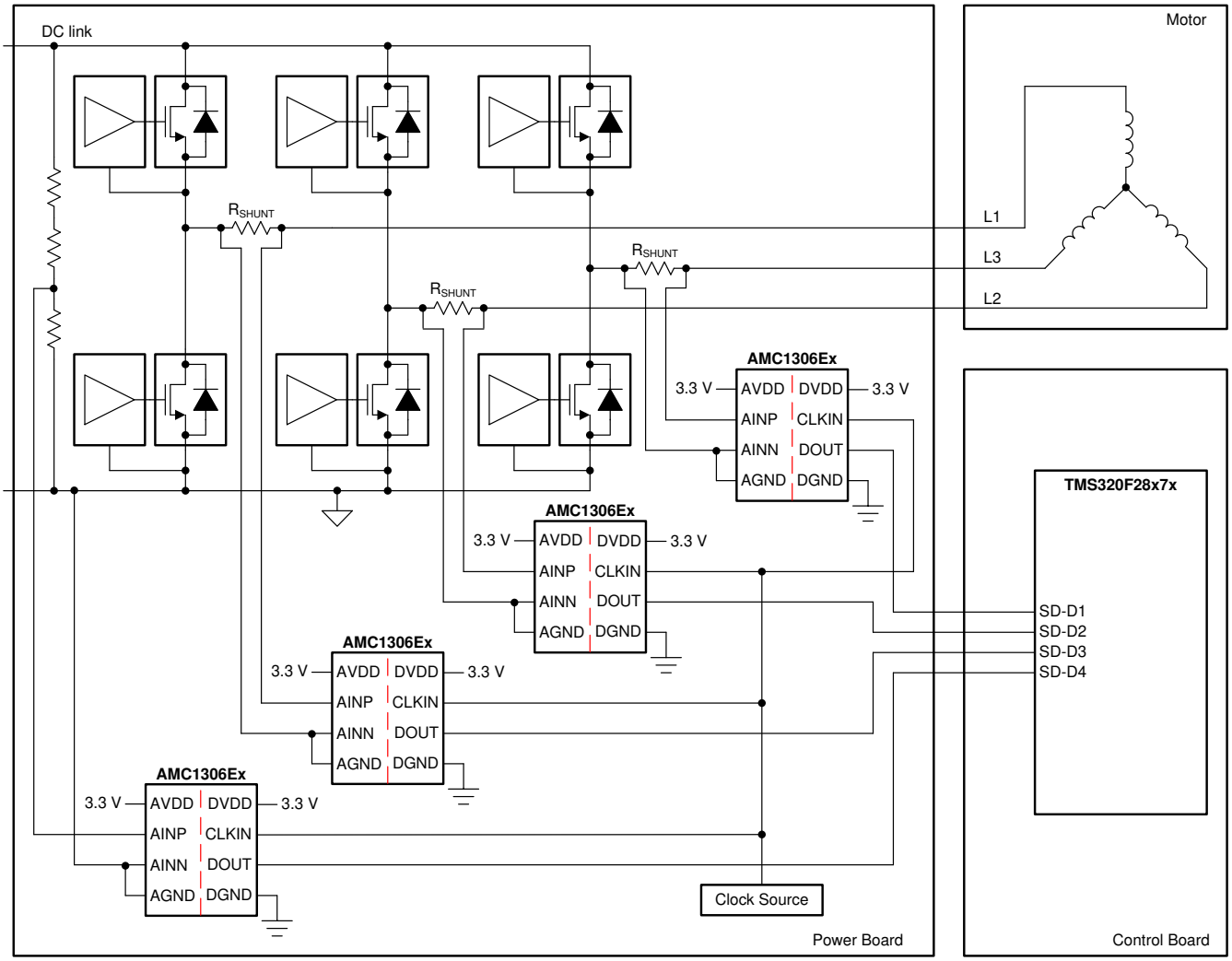


Figure 8-3. The AMC1306Ex in a Frequency Inverter Application

8.2.1.1 Design Requirements

Table 8-1 lists the parameters for the typical application in the *Section 8.2.1* section.

Table 8-1. Design Requirements

PARAMETER	VALUE
High-side supply voltage	3.3V or 5V
Low-side supply voltage	3.3V or 5V
Voltage drop across the shunt for a linear response	±250mV (maximum)

8.2.1.2 Detailed Design Procedure

The high-side power supply (AVDD) for the AMC1306 device is derived from the power supply of the upper gate driver. Further details are provided in the *Power Supply Recommendations* section.

The floating ground reference (AGND) is derived from one of the ends of the shunt resistor that is connected to the negative input of the AMC1306 (AINN). If a four-pin shunt is used, the inputs of the device are connected to the inner leads and AGND is connected to one of the outer shunt leads.

Use Ohm's Law to calculate the voltage drop across the shunt resistor (V_{SHUNT}) for the desired measured current: $V_{SHUNT} = I \times R_{SHUNT}$.

Consider the following two restrictions to choose the proper value of the shunt resistor R_{SHUNT}:

- The voltage drop caused by the nominal current range must not exceed the recommended differential input voltage range: $V_{SHUNT} \leq \pm 250mV$
- The voltage drop caused by the maximum allowed overcurrent must not exceed the input voltage that causes a clipping output: $|V_{SHUNT}| \leq |V_{Clipping}|$

The typically recommended RC filter in front of a ΔΣ modulator to improve signal-to-noise performance of the signal path is not required for the AMC1306. By design, the input bandwidth of the analog front-end of the device is limited as specified in the *Electrical Characteristics (AMC1306x05)* table.

For modulator output bitstream filtering, a device from TI's TMS320F2807x family of low-cost microcontrollers (MCUs) or TMS320F2837x family of dual-core MCUs is recommended. These families support up to eight channels of dedicated hardwired filter structures that significantly simplify system level design by offering two filtering paths per channel: one providing high accuracy results for the control loop and one fast response path for overcurrent detection.

8.2.1.3 Application Curve

In motor control applications, a very fast response time for overcurrent detection is required. The time for fully settling the filter in case of a step-signal at the input of the modulator depends on the filter order; that is, a $sinc^3$ filter requires three data updates for full settling (with $f_{DATA} = f_{CLK} / OSR$). Therefore, for overcurrent protection, filter types other than $sinc^3$ can be a better choice; an alternative is the $sinc^2$ filter. Figure 8-4 compares the settling times of different filter orders.

The delay time of the sinc filter with a continuous signal is half of the settling time.

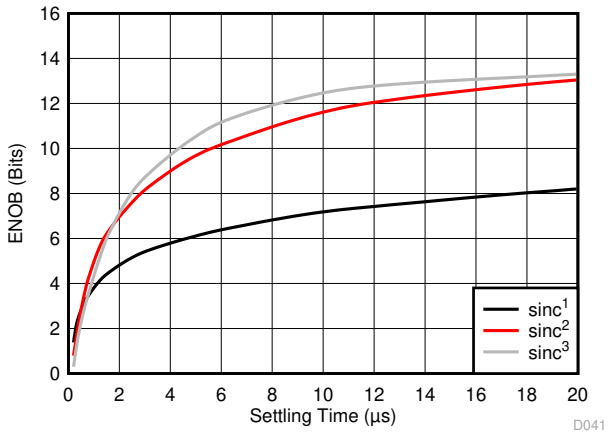


Figure 8-4. Measured Effective Number of Bits versus Settling Time

8.2.2 Isolated Voltage Sensing

The AMC1306 is designed to be used in current-sensing applications using low-impedance shunts. However, the device can also be used in isolated voltage-sensing applications if the affect of the (typically higher) impedance of the resistor used in this case is considered.

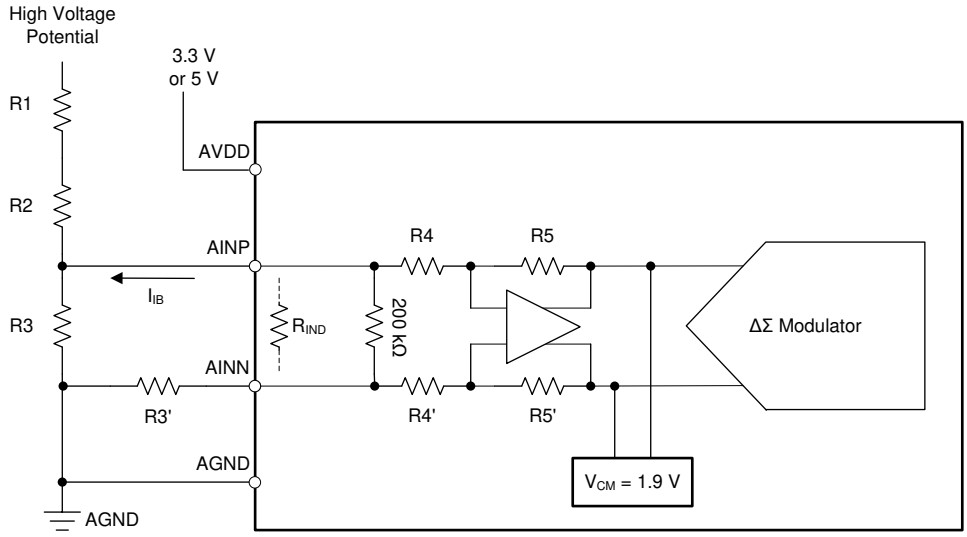


Figure 8-5. Using the AMC1306 for Isolated Voltage Sensing

8.2.2.1 Design Requirements

Figure 8-5 shows a simplified circuit typically used in high-voltage-sensing applications. The high impedance resistors (R1 and R2) are used as voltage dividers and dominate the current value definition. The resistance of the sensing resistor R3 is selected to meet the input voltage range of the AMC1306. This resistor and the differential input impedance of the device (the AMC1306x25 is 22kΩ, the AMC1306x05 is 4.9kΩ) also create a voltage divider that results in an additional gain error. With the assumption of R1, R2, and R_{IN} having a considerably higher value than R3, the resulting total gain error can be estimated using Equation 4, with E_G being the gain error of the AMC1306.

$$|E_{Gtot}| = |E_G| + \frac{R3}{R_{IN}} \tag{4}$$

This gain error can be easily minimized during the initial system-level gain calibration procedure.

8.2.2.2 Detailed Design Procedure

As indicated in Figure 8-5, the output of the integrated differential amplifier is internally biased to a common-mode voltage of 1.9V. This voltage results in a bias current I_{IB} through the resistive network R4 and R5 (or R4' and R5') used for setting the gain of the amplifier. The value range of this current is specified in the *Electrical Characteristics (AMC1306x05)* table. This bias current generates additional offset error that depends on the value of the resistor R3. The initial system offset calibration does not minimize this effect because the value of the bias current depends on the actual common-mode amplitude of the input signal (as illustrated in Figure 8-6). Therefore, in systems with high accuracy requirements, a series resistor is recommended to be used at the negative input (AINN) of the AMC1306 with a value equal to the shunt resistor R3 (that is, R3' = R3 in Figure 8-5) to eliminate the effect of the bias current.

This additional series resistor (R3') influences the gain error of the circuit. The effect can be calculated using Equation 5 with R5 = R5' = 50kΩ and R4 = R4' = 2.5kΩ (for the AMC1306x05) or 12.5kΩ (for the AMC1306x25).

$$E_G(\%) = \left(1 - \frac{R4}{R4' + R3'}\right) \times 100\% \quad (5)$$

8.2.2.3 Application Curve

Figure 8-6 shows the dependency of the input bias current on the common-mode voltage at the input of the AMC1306.

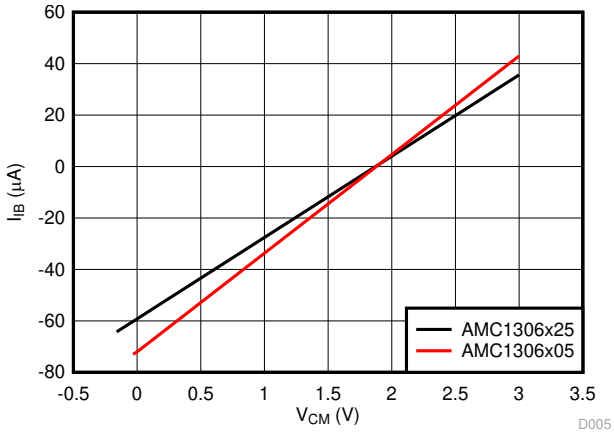


Figure 8-6. Input Bias Current vs Common-Mode Input Voltage

8.2.3 What To Do and What Not To Do

Do not leave the inputs of the AMC1306 unconnected (floating) when the device is powered up. If both modulator inputs are left floating, the input bias current drives these inputs to the output common-mode of the analog front-end of approximately 1.9V. If that voltage is above the specified input common-mode range, the front gain diminishes and the modulator outputs a bitstream resembling a zero input differential voltage.

8.3 Power Supply Recommendations

In a typical frequency-inverter application, the high-side power supply (AVDD) for the device is directly derived from the floating power supply of the upper gate driver. For lowest system-level cost, a Zener diode can be used to limit the voltage to 5V or 3.3V (±10%). Alternatively a low-cost low-drop regulator (LDO), for example the LM317N, can be used to adjust the supply voltage level and minimize noise on the power-supply node. A low-ESR decoupling capacitor of 0.1 µF is recommended for filtering this power-supply path. Place this capacitor (C2 in Figure 8-7) as close as possible to the AVDD pin of the AMC1306 for best performance. If better filtering is required, an additional 10µF capacitor can be used.

The floating ground reference (AGND) is derived from the end of the shunt resistor that is connected to the negative input (AINN) of the device. If a four-pin shunt is used, the device inputs are connected to the inner leads and AGND is connected to one of the outer leads of the shunt.

For decoupling of the digital power supply on the controller side, a 0.1µF capacitor is recommended to be placed as close to the DVDD pin of the AMC1306 as possible, followed by an additional capacitor in the range from 1µF to 10µF.

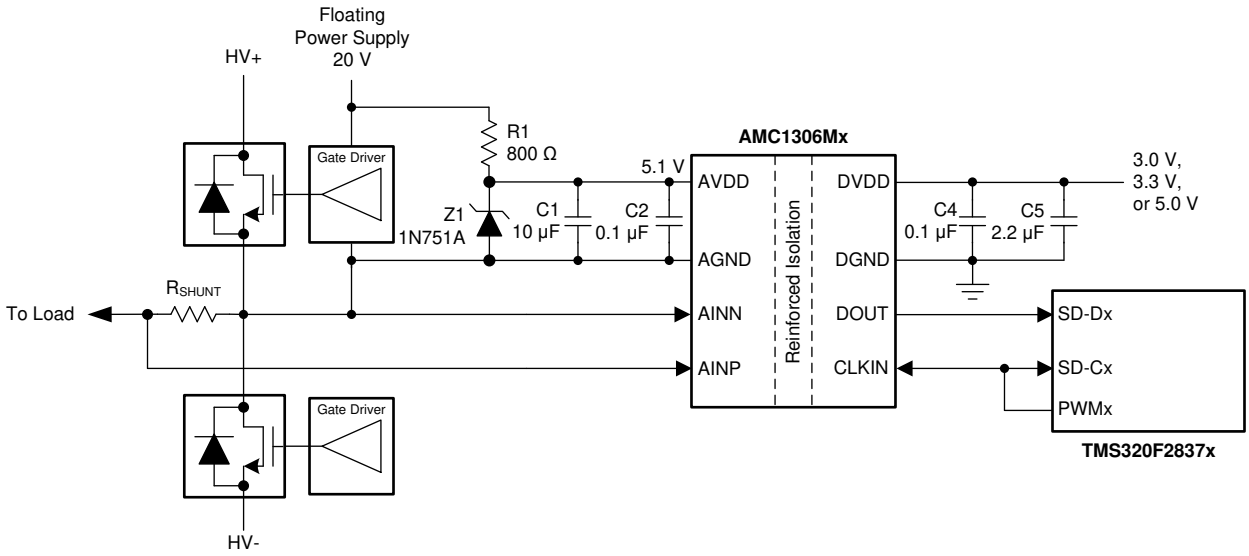


Figure 8-7. Decoupling the AMC1306

8.4 Layout

8.4.1 Layout Guidelines

A layout recommendation showing the critical placement of the decoupling capacitors (as close as possible to the AMC1306) and placement of the other components required by the device is shown in Figure 8-8. For best performance, place the shunt resistor close to the AINP and AINN inputs of the AMC1306 and keep the layout of both connections symmetrical.

8.4.2 Layout Example

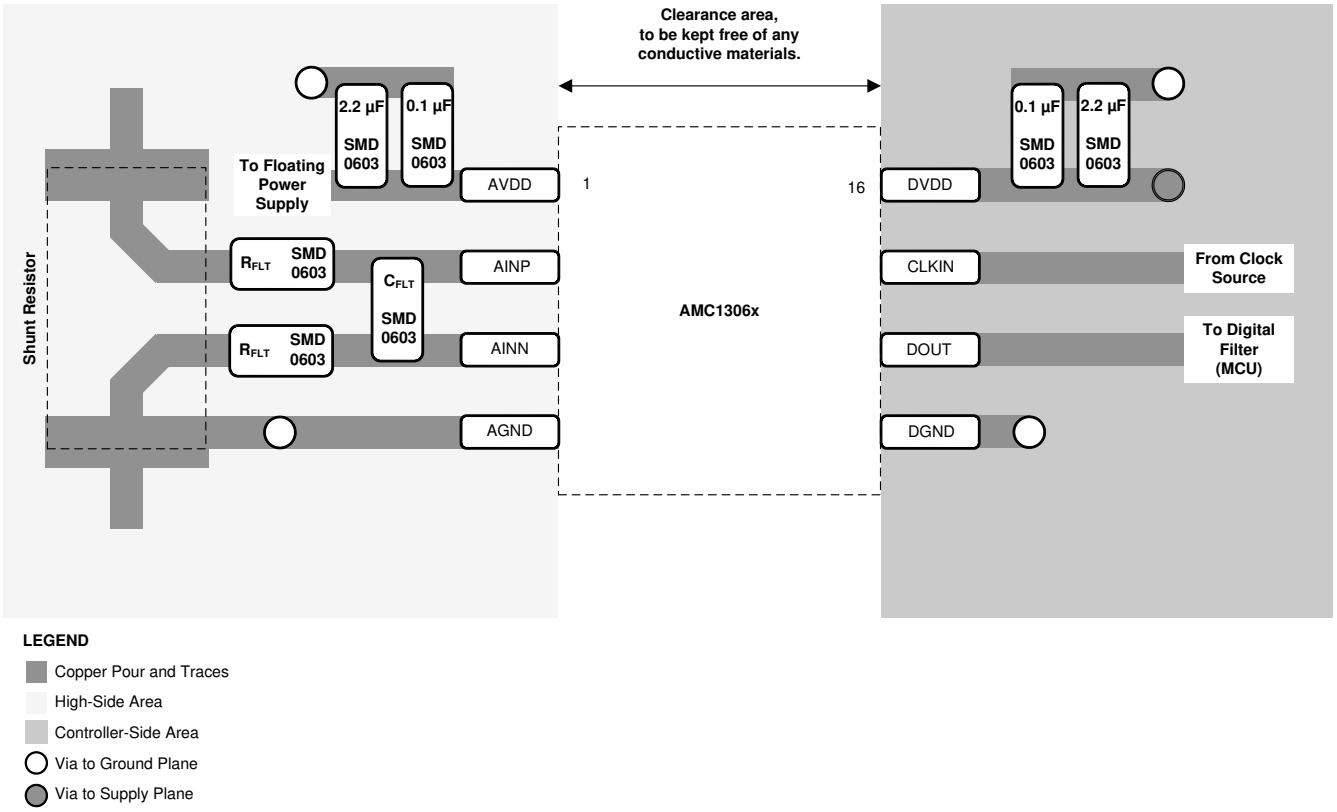


Figure 8-8. Recommended Layout of the AMC1306x

9 Device and Documentation Support

9.1 Device Support

9.1.1 Device Nomenclature

9.1.1.1 Isolation Glossary

See the *Isolation Glossary*

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *AMC1210 Quad Digital Filter for 2nd-Order Delta-Sigma Modulator* datasheet
- Texas Instruments, *MSP430F677x Polyphase Metering SoCs* datasheet
- Texas Instruments, *TMS320F2807x Piccolo™ Microcontrollers* datasheet
- Texas Instruments, *TMS320F2837xD Dual-Core Delfino™ Microcontrollers* datasheet
- Texas Instruments, *ISO72x Digital Isolator Magnetic-Field Immunity* application note
- Texas Instruments, *Combining the ADS1202 with an FPGA Digital Filter for Current Measurement in Motor Control Applications* application note
- Texas Instruments, *CDCLVC11xx 3.3V and 2.5V LVCMOS High-Performance Clock Buffer Family* datasheet

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (January 2020) to Revision D (August 2026)	Page
• Changed isolation standard from DIN VDE V 0884-11 (VDE V 0884-11) to DIN EN IEC 60747-17 (VDE 0884-17) and updated the *Insulation Specifications and Safety-Related Certifications* tables accordingly	1
• Changed $V_{CM, MIN}$ for AMC1306x05 from –32mV to –100mV	4

- Changed $V_{CM, MIN}$ for AMC1305x25 from –160mV to –500mV 4

Changes from Revision B (June 2018) to Revision C (January 2020) **Page**

- Changed *Safety-related certifications* bullet in *Features* section: changed *VDE certification* revision from *DIN V VDE V 0884-10 (VDE V 0884-11)* to *DIN VDE V 0884-11* and changed *IEC 60950-1, and IEC 60065* to *IEC 62368-1* 1
- Changed *DIN V VDE V* to *DIN VDE V* in *Description* section 1
- Changed 6.05dB to 6.02dB in Equation 3 27
- Changed input common-mode voltage from 2V to 1.9V for consistency with *Input Bias Current vs Common-Mode Input Voltage* figure in *What To Do and What Not To Do* section 32
- Changed *VINx* to *AINx* in *Layout Guidelines* section 33
- Changed *Recommended Layout of the AMC1306x* figure to include connection to the shunt resistor and input filter components 33

Changes from Revision A (July 2017) to Revision B (June 2018) **Page**

- Changed *Reinforced Isolation Capacitor Lifetime Projection* figure 13

Changes from Revision * (March 2017) to Revision A (July 2017) **Page**

- Released AMC1306E05 and AMC1306M05 to production 1
- Added ±50 µV to first *DC Performance* sub-bullet to reflect the AMC1306x05 devices 1
- Changed standard deviation from 0884-10 to 0884-11 in first *Safety-Related Certifications* sub-bullet 1
- Changed V_{PEAK} from 8000 to 7000 and standard deviation from 0884-10 to 0884-11 in first paragraph of *Description* section 1
- Deleted Status column from *Device Comparison Table* 3
- Added AMC1306x05 devices to *Typical Characteristics* section 14

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this datasheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AMC1306E05DWV	Active	Production	SOIC (DWV) | 8	64 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1306E05
AMC1306E05DWV.A	Active	Production	SOIC (DWV) | 8	64 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1306E05
AMC1306E05DWVR	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1306E05
AMC1306E05DWVR.A	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1306E05
AMC1306E25DWV	Active	Production	SOIC (DWV) | 8	64 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1306E25
AMC1306E25DWV.A	Active	Production	SOIC (DWV) | 8	64 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1306E25
AMC1306E25DWVR	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1306E25
AMC1306E25DWVR.A	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1306E25
AMC1306E25DWVRG4	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1306E25
AMC1306E25DWVRG4.A	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1306E25
AMC1306M05DWV	Active	Production	SOIC (DWV) | 8	64 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1306M05
AMC1306M05DWV.A	Active	Production	SOIC (DWV) | 8	64 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1306M05
AMC1306M05DWVG4	Active	Production	SOIC (DWV) | 8	64 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1306M05
AMC1306M05DWVG4.A	Active	Production	SOIC (DWV) | 8	64 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1306M05
AMC1306M05DWVR	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1306M05
AMC1306M05DWVR.A	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1306M05
AMC1306M25DWV	Active	Production	SOIC (DWV) | 8	64 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1306M25
AMC1306M25DWV.A	Active	Production	SOIC (DWV) | 8	64 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1306M25
AMC1306M25DWVR	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1306M25
AMC1306M25DWVR.A	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1306M25

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF AMC1306M05, AMC1306M25 :

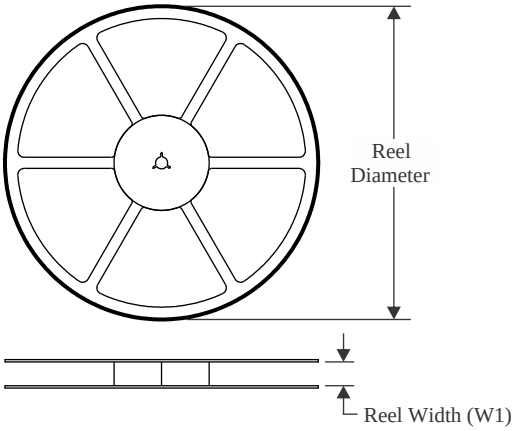
- Automotive : AMC1306M05-Q1, AMC1306M25-Q1

NOTE: Qualified Version Definitions:

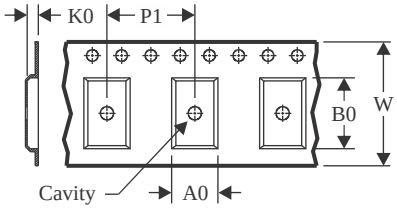
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

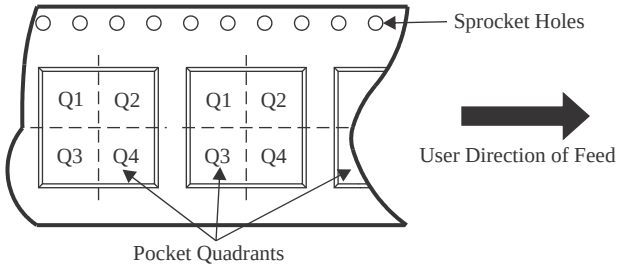


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

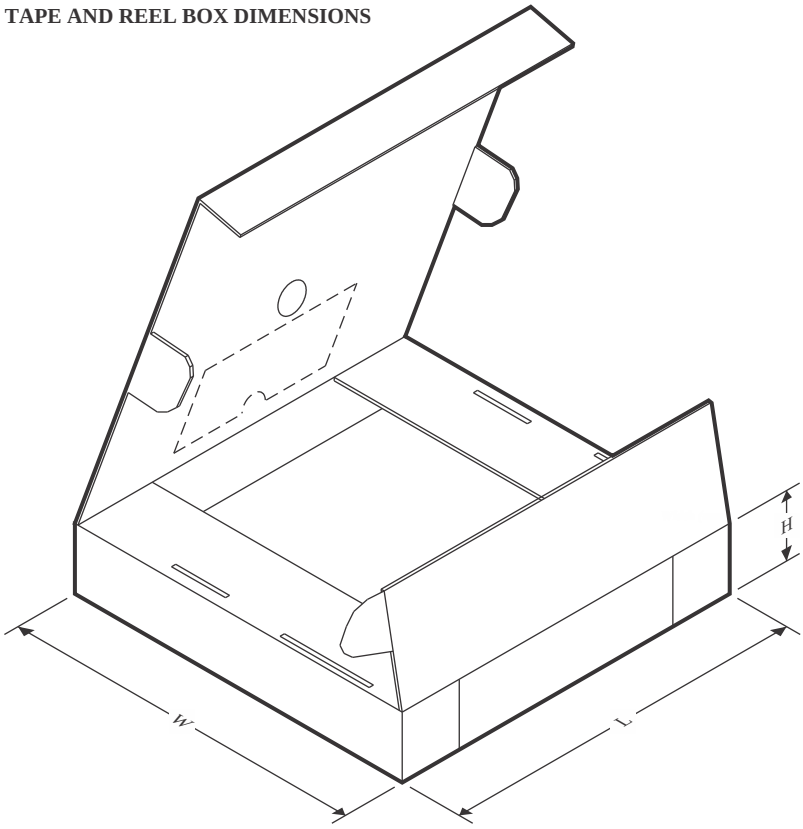
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC1306E05DWVR	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
AMC1306E05DWVR	SOIC	DWV	8	1000	330.0	16.4	12.15	6.2	3.05	16.0	16.0	Q1
AMC1306E25DWVR	SOIC	DWV	8	1000	330.0	16.4	12.15	6.2	3.05	16.0	16.0	Q1
AMC1306E25DWVR	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
AMC1306E25DWVRG4	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
AMC1306M05DWVR	SOIC	DWV	8	1000	330.0	16.4	12.15	6.2	3.05	16.0	16.0	Q1
AMC1306M05DWVR	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
AMC1306M25DWVR	SOIC	DWV	8	1000	330.0	16.4	12.15	6.2	3.05	16.0	16.0	Q1

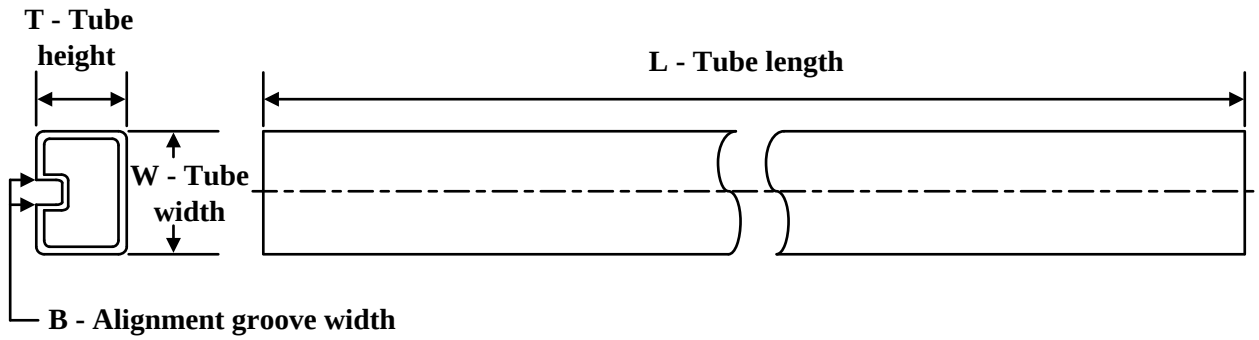
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

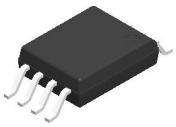
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC1306E05DWVR	SOIC	DWV	8	1000	350.0	350.0	43.0
AMC1306E05DWVR	SOIC	DWV	8	1000	353.0	353.0	32.0
AMC1306E25DWVR	SOIC	DWV	8	1000	353.0	353.0	32.0
AMC1306E25DWVR	SOIC	DWV	8	1000	350.0	350.0	43.0
AMC1306E25DWVRG4	SOIC	DWV	8	1000	350.0	350.0	43.0
AMC1306M05DWVR	SOIC	DWV	8	1000	353.0	353.0	32.0
AMC1306M05DWVR	SOIC	DWV	8	1000	350.0	350.0	43.0
AMC1306M25DWVR	SOIC	DWV	8	1000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

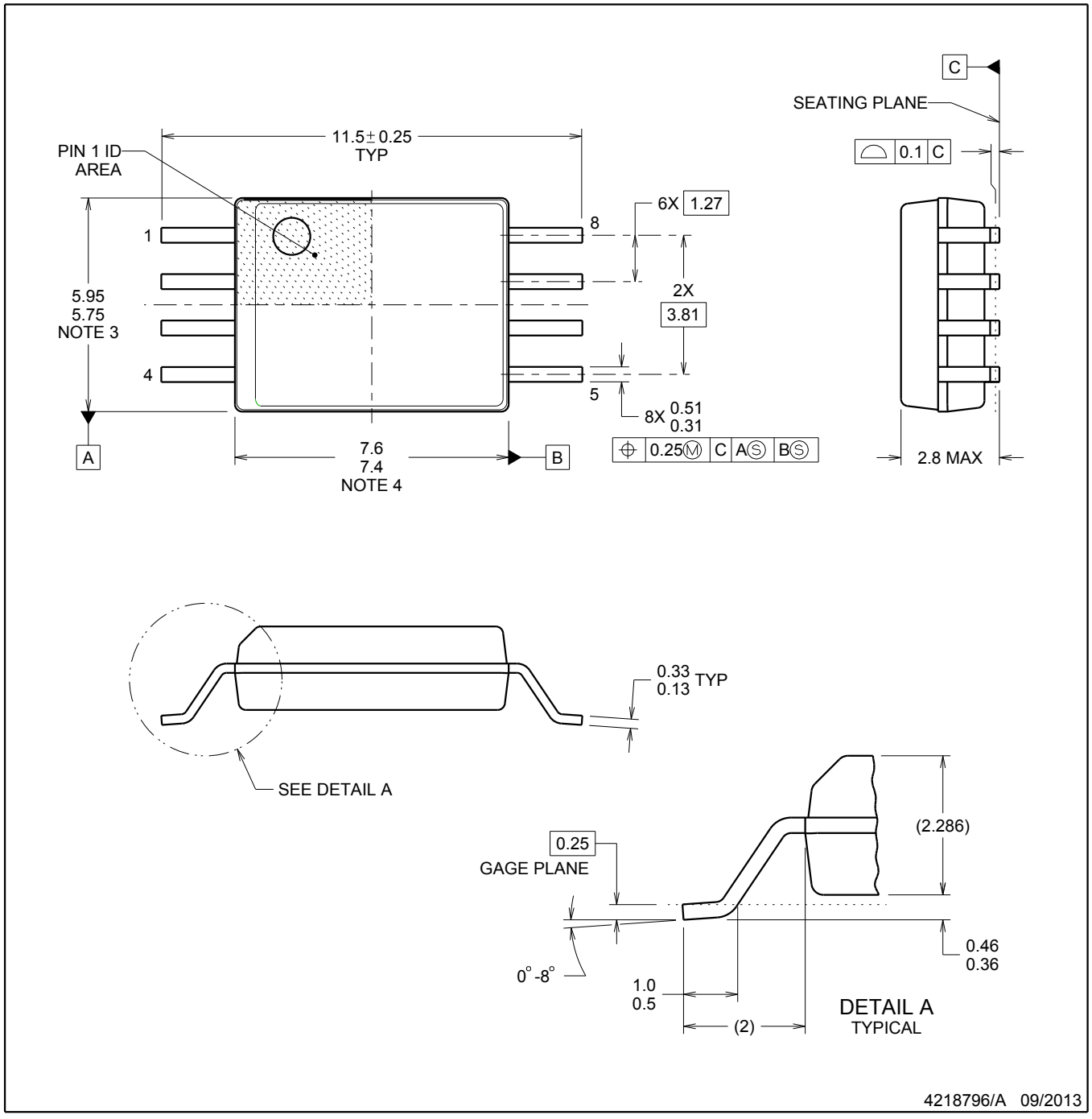
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
AMC1306E05DWV	DWV	SOIC	8	64	505.46	13.94	4826	6.6
AMC1306E05DWV.A	DWV	SOIC	8	64	505.46	13.94	4826	6.6
AMC1306E25DWV	DWV	SOIC	8	64	505.46	13.94	4826	6.6
AMC1306E25DWV.A	DWV	SOIC	8	64	505.46	13.94	4826	6.6
AMC1306M05DWV	DWV	SOIC	8	64	505.46	13.94	4826	6.6
AMC1306M05DWV.A	DWV	SOIC	8	64	505.46	13.94	4826	6.6
AMC1306M05DWVG4	DWV	SOIC	8	64	505.46	13.94	4826	6.6
AMC1306M05DWVG4.A	DWV	SOIC	8	64	505.46	13.94	4826	6.6
AMC1306M25DWV	DWV	SOIC	8	64	505.46	13.94	4826	6.6
AMC1306M25DWV.A	DWV	SOIC	8	64	505.46	13.94	4826	6.6



DWV0008A

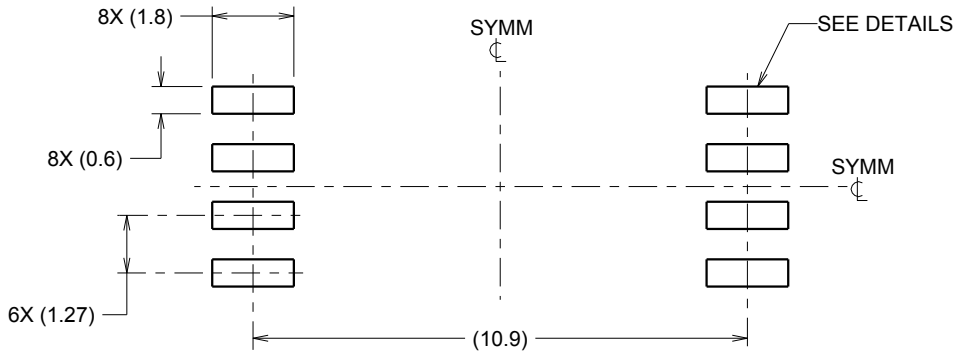
SOIC - 2.8 mm max height

SOIC

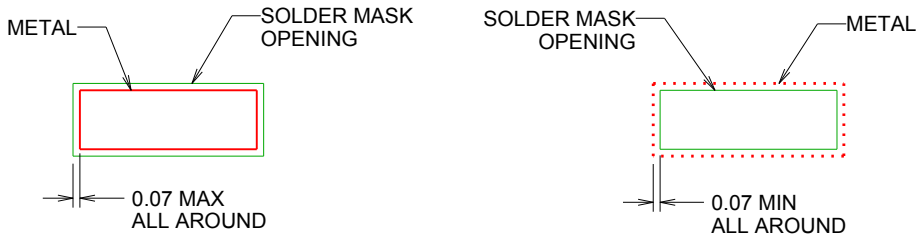


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
9.1 mm NOMINAL CLEARANCE/CREEPAGE
SCALE:6X



SOLDER MASK DETAILS

4218796/A 09/2013

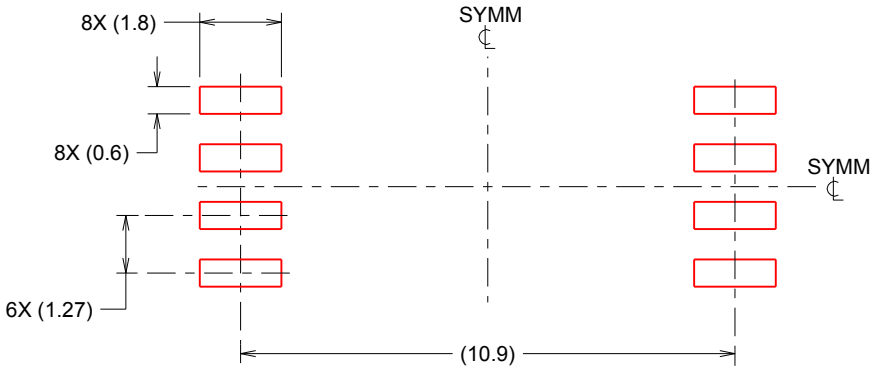
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

DWV0008A

SOIC - 2.8 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4218796/A 09/2013

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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