

BQ21088 I²C Controlled, 1-Cell, 1A Linear Battery Charger with Power Path, Ship Mode, Shutdown Mode, and Battery Tracking VINDPM

1 Features

- 1A linear battery charger
 - 3.0V to 5.5V input voltage operating range for battery-to-battery charging and USB adapters
 - Configurable battery regulation voltage with 0.5% accuracy from 3.6V to 4.65V in 10mV steps
 - Li-ion, Li-Poly, and LiFePO₄ chemistries support
 - 5mA to 1A configurable fast charge current
 - 55mΩ battery FET ON resistance
 - Up to 3A discharge current to support high system loads
 - Configurable NTC charging profile thresholds including JEITA support
- Power path management for powering the system and charging the battery
 - Regulated system voltage (SYS) ranging from 4.4V to 4.9V addition to battery voltage tracking and input pass-through options
 - Battery Tracking input voltage dynamic power management (VINDPM) for high impedance input sources
- Ultra low quiescent current
 - 4μA in Battery Only mode
 - 30μA Input adapter I_q in sleep mode
- One push-button wake-up and reset input
- Integrated fault protection
 - Input overvoltage protection (VIN_OVP)
 - Battery short protection (BATSC)
 - Battery overcurrent protection (BATOCP)
 - Input current limit protection (ILIM)
 - Thermal regulation (TREG) and thermal shutdown (TSHUT)
 - Battery thermal fault protection (TS)
 - Watchdog and safety timer fault

2 Applications

- [TWS headset and charging case](#)
- [Smart glasses, AR and VR](#)
- [Smart watches and other wearable devices](#)
- [Retail automation and payment](#)
- [Building automation](#)

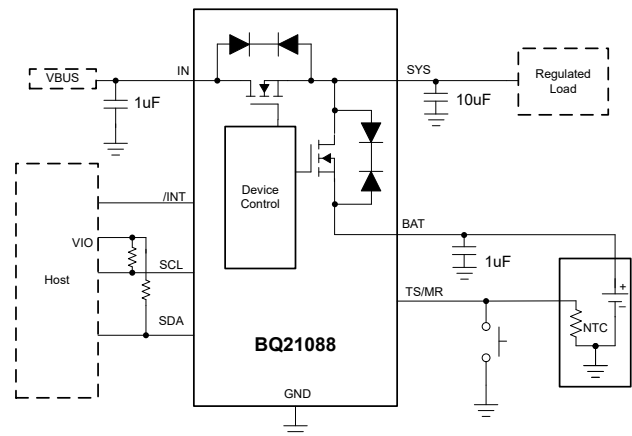
3 Description

The BQ21088 is a linear battery charger IC focusing on small solution size and low quiescent current for extending battery life. The device is available in an 8-ball chipscale package which does not need HDI PCB process for fabrication thereby reducing the PCB cost. The device can support up to 1A charging and system loads of up to 3A.

Package Information

| PART NUMBER | PACKAGE ⁽¹⁾ | PACKAGE SIZE ⁽²⁾ | BODY SIZE (NOM) |
|-------------|------------------------|-----------------------------|-----------------|
| BQ21088 | YBG (DSBGA 8) | 1.6mm x 1.1mm | 1.6mm x 1.1mm |

- (1) For all available packages, see [Section 13](#).
 (2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

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4 Description (continued)

The battery is charged using a standard Li-ion or LiFePO4 charge profile with three phases: precharge, constant current and constant voltage. Thermal regulation provides the maximum charge current while managing the device temperature. The charger is also optimized for battery to battery charging with 3V minimum input voltage operation and can withstand 25V absolute maximum line transients. The device integrates a single push-button input to reduce the total solution footprint.

5 Pin Configuration and Functions

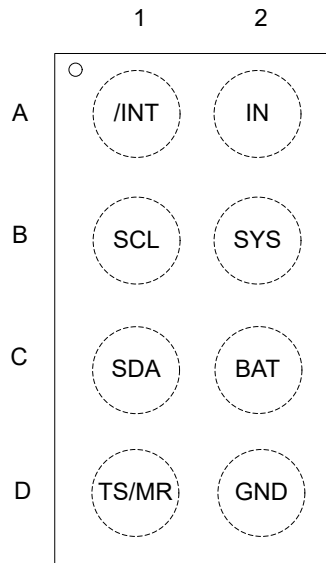


Figure 5-1. YBG Package WCSP 8 Pin (Top View)

Table 5-1. Pin Functions

| PIN | | I/O ⁽¹⁾ | DESCRIPTION |
|-------|-----|--------------------|--|
| NAME | NO. | | |
| IN | A2 | P | DC Input Power Supply. IN is connected to the external DC supply. Bypass IN to GND with at least 1 μ F of effective capacitance using a ceramic capacitor. |
| SYS | B2 | P | Regulated System Output. Connect at least 10- μ F ceramic capacitor (at least 1 μ F of ceramic capacitance with DC bias de-rating) from SYS to GND as close to the SYS and GND pins as possible. |
| BAT | C2 | P | Battery Connection. Connect to the positive terminal of the battery. Bypass BAT to GND with at least 1 μ F of ceramic capacitance. |
| GND | D2 | - | Ground connection. Connect to the ground plane of the circuit. |
| SCL | B1 | I/O | I ² C Interface Clock. Connect SCL to the logic rail through a 10-k Ω resistor. |
| SDA | C1 | I/O | I ² C Interface Data. Connect SDA to the logic rail through a 10-k Ω resistor. |
| /INT | A1 | O | INT is an open-drain output that signals fault interrupts. When a fault occurs, a 128- μ s active low pulse is sent out as an interrupt for the host. INT is enabled/disabled using the MASK_INT bit in the control register. Can be pulled up to a 1- to 20-k Ω resistor. Typical pull-up voltage = 1.8 V, max pull-up voltage = 5 V. |
| TS/MR | D1 | I/O | Manual Reset Input/ NTC thermistor pin. TSMR is a general purpose input that must be held low for greater than t_{LPRESS} to go into Shipmode or perform a hardware reset. It can also be used to detect shorter button press durations such as t_{wake1} and t_{wake2} TSMR may be driven by a momentary push-button or a MOS switch. The TSMR pin will also have an NTC thermistor connected on to it. |

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|---------------------|----------------------|------|-----|------|
| Input Voltage | IN | -0.3 | 25 | V |
| Voltage | All other pins | -0.3 | 5.5 | V |
| Input Current (DC) | IN | | 1.1 | A |
| Output Sink Current | /INT | | 20 | mA |
| T _J | Junction temperature | -40 | 150 | °C |
| T _{stg} | Storage temperature | -65 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

| | | | VALUE | UNIT |
|--------------------|-------------------------|--|-------|------|
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins ⁽¹⁾ | ±2500 | V |
| | | Charged device model (CDM), per ANSI/ESDA/ JEDEC JS-002, all pins ⁽²⁾ | ±1500 | |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | BQ25185 | UNIT |
|-------------------------------|--|---------|------|
| | | DLH | |
| | | 10 | |
| R _{θJA} | Junction-to-ambient thermal resistance (JEDEC ⁽¹⁾) | 107.1 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 0.9 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 30.3 | °C/W |
| Ψ _{JT} | Junction-to-top characterization parameter | 0.3 | °C/W |
| Ψ _{JB} | Junction-to-board characterization parameter | 30.3 | °C/W |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | N/A | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|-------------|--|-----|-----|-----|------|
| VBAT | Battery Voltage Range | 2.2 | | 4.6 | V |
| VIN | Input Voltage Range | 2.7 | | 5.5 | V |
| IIN | Input Current Range (IN to SYS) | | | 1.1 | A |
| ISYS (DC) | SYS Discharge Current (DC) | | | 2 | A |
| ISYS (Peak) | SYS Discharge Current (tpulse < 20mS) | | | 3 | A |
| IBAT | Battery Discharge Current (BAT to SYS) | | | 3 | A |

6.4 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|----------------|--------------------------------------|-----|-----|-----|------|
| T _J | Operating Junction Temperature Range | -40 | | 125 | °C |

6.5 Electrical Characteristics

V_{IN} = 5V, V_{BAT} = 3.6V. T_J = 25°C unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|---|------|-------|------|------|
| INPUT CURRENTS | | | | | | |
| I _{Q_IN} | Input supply quiescent current | V _{BAT} = 3.6V, V _{IN} = 5V, Charge enabled, I _{CHG} = 0mA, SYSREG = 4.5V | | 0.75 | 1 | mA |
| I _{Q_IN} | Input supply quiescent current | V _{BAT} = 3.6V, V _{IN} = 5V, Charge enabled, I _{CHG} = 0mA, SYSREG = Passthrough | | 0.660 | 1.5 | mA |
| I _{SLEEP_IN} | SLEEP input current | V _{IN} = 3.6V, V _{BAT} = 3.7V | | 30 | | µA |
| I _{Q_BAT} | Battery quiescent current | V _{IN} < V _{UVLO} or floating, Watchdog disabled, Push button disabled, I _{2C} functional. V _{BAT} = 3.6V T _J = 25°C | | 3 | 3.5 | µA |
| I _{Q_BAT} | Battery quiescent current | V _{IN} < V _{UVLO} , V _{BAT} = 3.6V, Push-button function enabled, 0°C < T _J < 85°C | | 4 | 5 | µA |
| I _{BAT_SHUTDOWN} | Battery discharge current in Shutdown Mode | V _{IN} = 0V, Shutdown Mode, V _{BAT} = 3.6V, Adapter Sense wake enabled. | | 30 | | nA |
| I _{BAT_SHIP} | Battery discharge current in Ship Mode | V _{BAT} = 3.6V, Push button function enabled (average current), 0°C < T _J < 85°C | | 3.2 | 5 | µA |
| POWER-PATH MANAGEMENT AND INPUT | | | | | | |
| V _{IN_OP} | Input voltage operating range | | 3.6 | | 5.5 | V |
| V _{IN_UVLOZ} | Exit IN undervoltage lock-out | IN rising | | | 3 | V |
| V _{IN_UVLO} | Enter IN undervoltage lock-out | IN falling | | | 2.7 | V |
| V _{IN_LOVW} | IN voltage to start charging | IN rising | | 3 | 3.15 | V |
| V _{IN_LOVWZ} | IN voltage to stop charging | IN falling | | 2.95 | 3.1 | V |
| V _{IN_PORZ} | IN voltage threshold to enter shipmode | IN falling | 1.09 | 1.3 | 1.66 | V |
| V _{SLEEP} | Enter sleep mode threshold | IN falling, V _{IN} - V _{BAT} , V _{BAT} = 4V | | 82 | | mV |
| V _{SLEEPZ} | Exit sleep mode threshold | IN rising, V _{IN} - V _{BAT} , V _{BAT} = 4V | 168 | 208 | 262 | mV |
| V _{IN_OVP} | V _{IN} overvoltage rising threshold | IN rising | 5.5 | 5.7 | 5.9 | V |
| V _{IN_OVP_HYS} | IN overvoltage hysteresis | IN falling | | 125 | | mV |
| I _{BAT_OCP} | BATOCP(Reverse OCP only) | V _{BAT} = 4V, I _{BAT_OCP} = 00 | | 0.5 | | A |
| | | V _{BAT} = 4V, I _{BAT_OCP} = 01 | | 1.05 | | A |
| | | V _{BAT} = 4V, I _{BAT_OCP} = 10 | | 1.65 | | A |
| | | V _{BAT} = 4V, I _{BAT_OCP} = 11 | | 3 | | A |
| I _{BAT_OCPACC} | Battery OCP Accuracy | I _{BAT} = 3 A, T _J = 27C | | | 18 | % |
| VBSUP1 | Enter supplement mode threshold | V _{BAT} = 3.6V, V _{BAT} > V _{BUVLO} , V _{SYS} < V _{BAT} -VBSUP1 | | 40 | | mV |
| VBSUP2 | Exit supplement mode threshold | V _{BAT} > V _{BUVLO} , V _{SYS} > V _{BAT} -VBSUP2 | | 20 | | mV |

6.5 Electrical Characteristics (continued)

VIN = 5V, VBAT = 3.6V. TJ = 25°C unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------|--|--|------|---------------------|------|------|
| ILIM | Input Current Limit | VIN = 5V, ILIM =50mA | 40 | 50 | 60 | mA |
| | | VIN = 5V, ILIM =100mA | 80 | 90 | 98 | mA |
| | | VIN = 5V, ILIM= 200mA | 180 | 200 | 220 | mA |
| | | VIN = 5V, ILIM= 300mA | 270 | 300 | 330 | mA |
| | | VIN = 5V, ILIM= 380mA | 360 | 380 | 400 | mA |
| | | VIN = 5V, ILIM= 500mA | 450 | 475 | 498 | mA |
| | | VIN = 5V, ILIM=665mA | 630 | 665 | 700 | mA |
| | | VIN = 5V, ILIM= 1050mA | 995 | 1050 | 1100 | mA |
| VINDPM_ACC | VINDPM accuracy | VINDPM target is not disabled | -3 | | 3 | % |
| VINDPM | Input voltage threshold when input current is reduced | VINDPM target = VBAT + VINDPM_TRACK | | VBAT + VINDPM_TRACK | | V |
| | Input voltage threshold when input current is reduced | VINDPM target =4.5V | | 4.5 | | V |
| | Input voltage threshold when input current is reduced | VINDPM target =4.7V | | 4.7 | | V |
| VINDPM_TRACK | Input voltage threshold offset for when input current is reduced and when VBAT > 3.5 V | VINDPM target = VBAT + VINDPM_TRACK | | 330 | | mV |
| VDPPM | SYS voltage threshold when charge current is reduced | VBAT = 3.6V, VSYS = VDPPM + VBAT before charge current is reduced. | | 0.1 | | V |
| VSYS_REG_ACCURACY | Programmable SYS voltage regulation accuracy | VIN = 5V, VBAT = 3.6V, RSYS = 100ohm, SYS regulation target = 4.4V to 4.9V | -2 | | 2 | % |
| VMINSYS | Minimum SYS voltage when in battery tracking mode | VBAT < 3.6V | | 3.8 | | V |
| VSYS_TRACK | Voltage regulation threshold for SYS when VBAT >3.6V in battery tracking mode | VBAT = 4V, VSYS = VBAT + VSYS_TRACK | | 225 | | mV |
| RSYS_PD | SYS pull down resistance | VSYS = 3.6V | | 20 | | Ω |
| VSYS_SHORT | Voltage threshold for detecting SYS_SHORT condition has occurred | falling voltage | | 0.86 | | V |
| VSYS_SHORT_HYS | Voltage threshold for exiting SYS_SHORT condition has occurred | rising voltage | | 1.1 | | V |
| BATTERY CHARGER | | | | | | |
| RON_BAT | Battery FET on-resistance | VBAT = 4.5V, IBAT =500mA | | 55 | 90 | mΩ |
| RON_IN | Input FET on-resistance | IN = 5V, IIN = 0.8A | | 330 | 470 | mΩ |
| VREG_RANGE | Typical BAT charge voltage regulation range | 10mV steps, programmable through I ² C | 3.5 | | 4.65 | V |
| VREG_ACC | BAT charge voltage accuracy, summary for all settings | All VBATREG settings, typical measurement at VBATREG = 4.2V | -0.5 | | 0.5 | % |
| ICHG_RANGE | Typical charge current regulation range | VBAT > VLOWV | 5 | | 1000 | mA |
| ICHG_ACC | Charge current accuracy | VIN = 5V, Fastcharge >=40mA | -10 | | 10 | % |
| ICHG_ACC | Charge current accuracy | Fastcharge current = 5mA | 4.1 | 5 | 5.5 | mA |
| ICHG_ACC | Charge current accuracy | Fastcharge current = 40mA | 36 | 40 | 44 | mA |
| ICHG_ACC | Charge current accuracy | Fastcharge current = 630mA | 567 | 630 | 693 | mA |
| IPRECHG | Typical pre-charge current, as percentage of ICHG | VOUT < VLOWV | | 20 | | % |
| IPRECHG_ACC | Precharge current accuracy | Fastcharge current >=40mA | -10 | | 10 | % |

6.5 Electrical Characteristics (continued)

VIN = 5V, VBAT = 3.6V. TJ = 25°C unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|---|--------|----------|--------|------|
| I _{TERM} | Typical termination current, as percentage of ICHG | V _{OUT} = VBATREG | | 10 | | % |
| I _{TERM_ACC} | Termination current accuracy | IBAT = 3mA (ICHG= 30mA) Tj = 25°C | -10 | | 10 | % |
| I _{TERM_ACC} | Termination current accuracy | IBAT = 3mA (ICHG= 30mA) Tj = 25°C | 2.7 | | 3.3 | mA |
| V _{LOWV} | Pre-charge to fast-charge transition threshold | VLOWVSEL = 3.0V, VBAT rising | 2.9 | 3 | 3.1 | V |
| V _{LOWV} | Pre-charge to fast-charge transition threshold | VLOWVSEL = 2.8V, VBAT rising | 2.7 | 2.8 | 2.9 | V |
| V _{LOWV_HYS} | Battery LOWV hysteresis | All settings | | 100 | | mV |
| V _{BUVLO} | Battery UVLO, VBAT falling | BUVLO setting = b000 | | 3 | | V |
| | Battery UVLO, VBAT falling | BUVLO setting = b011 | | 2.8 | | V |
| | Battery UVLO, VBAT falling | BUVLO setting = b100 | | 2.6 | | V |
| | Battery UVLO, VBAT falling | BUVLO setting = b101 | | 2.4 | | V |
| | Battery UVLO, VBAT falling | BUVLO setting = b110 | | 2.2 | | V |
| | Battery UVLO, VBAT falling | BUVLO setting = b111 | | 2.0 | | V |
| V _{BUVLO_HYS} | Battery UVLO hysteresis, VBAT rising | Any BUVLO Setting, value above VBAT, VIN = 5V | 110 | 150 | 190 | mV |
| V _{BUVLO_HYS} | Battery UVLO hysteresis, VBAT rising | Any BUVLO Setting, value above VBAT, VIN = 0V | 90 | 150 | 210 | mV |
| V _{BATPOR} | Battery only power up voltage, VBAT rising | -40C < Tj < 125C | 3.08 | 3.21 | 3.46 | V |
| V _{RCH} | Battery Recharge Threshold | BAT falling, VRCH bit = 0 | 75 | 100 | 130 | mV |
| | | BAT falling, VRCH bit = 1 | 175 | 200 | 230 | mV |
| V _{BATSC} | Short on battery threshold for trickle charge, VBAT rising | | 1.6 | 1.8 | 2.0 | V |
| V _{BATSC_HYS} | Battery short circuit voltage hysteresis | | | 200 | | mV |
| I _{BATSC} | Trickle Charge Current | VBAT < V _{BATSC} | | 1 | | mA |
| TEMPERATURE REGULATION AND TEMPERATURE SHUTDOWN | | | | | | |
| T _{REG} | Typical junction temperature regulation | THERM_REG = 00 | | 100 | | °C |
| T _{REG} | Typical junction temperature regulation | THERM_REG = 01 | | 80 | | °C |
| T _{REG} | Typical junction temperature regulation | THERM_REG = 10 | | 60 | | °C |
| T _{REG} | Typical junction temperature regulation | THERM_REG = 11 | | Disabled | | |
| T _{SHUT_RISING} | Thermal shutdown rising threshold | Temperature increasing | | 150 | | °C |
| T _{SHUT_FALLING} | Thermal shutdown falling threshold | Temperature decreasing | | 135 | | °C |
| BATTERY NTC MONITOR | | | | | | |
| I _{TS_BIAS} | TS nominal bias current | | 36.5 | 38 | 39.5 | μA |
| V _{T1_Entry} | Cold - 00 @ Approx. 0°C, default | VIN = 5V | 0.9575 | 1.0075 | 1.0575 | V |
| V _{T2_Entry} | Cold - 01 @ Approx. 3°C | VIN = 5V | 0.8450 | 0.8900 | 0.9325 | V |
| V _{T3_Entry} | Cold - 10 @ Approx. 5°C | VIN = 5V | 0.7775 | 0.8200 | 0.8600 | V |
| V _{T4_Entry} | Cold - 11 @ Approx. -3°C | VIN = 5V | 1.0850 | 1.1425 | 1.2000 | V |
| V _{T5_Entry} | Cool - 00 @ Approx. 10°C, default | VIN = 5V | 0.6350 | 0.6700 | 0.7025 | V |
| V _{T6_Entry} | Warm - 00 @ Approx. 45°C, default | VIN = 5V | 0.1730 | 0.1850 | 0.198 | V |
| V _{T7_Entry} | Hot - 00 @ Approx. 60°C, default | VIN = 5V | 0.1050 | 0.1150 | 0.1250 | V |
| V _{T8_Entry} | Hot - 01 @ Approx. 65°C | VIN = 5V | 0.0875 | 0.0975 | 0.1075 | V |
| V _{T9_Entry} | Hot - 10 @ Approx. 50°C | VIN = 5V | 0.1475 | 0.1575 | 0.1675 | V |
| V _{T10_Entry} | Hot - 11 @ Approx. 45°C | VIN = 5V | 0.1750 | 0.1850 | 0.1950 | V |

6.5 Electrical Characteristics (continued)

VIN = 5V, VBAT = 3.6V. TJ = 25°C unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---|--|----------------------------|--------|--------|------|
| V _{T1_Exit} | Cold - 00 @ Approx. 5°C, default | VIN = 5V | 0.7775 | 0.8200 | 0.8600 | V |
| V _{T2_Exit} | Cold - 01 @ Approx. 8°C | VIN = 5V | 0.6875 | 0.7250 | 0.7600 | V |
| V _{T3_Exit} | Cold - 10 @ Approx. 10°C | VIN = 5V | 0.6350 | 0.6700 | 0.7025 | V |
| V _{T4_Exit} | Cold - 11 @ Approx. 2°C | VIN = 5V | 0.8800 | 0.9275 | 0.9725 | V |
| V _{T5_Exit} | Cool - 00 @ Approx. 15°C, default | VIN = 5V | 0.5225 | 0.5500 | 0.5775 | V |
| V _{T6_Exit} | Warm - 00 @ Approx. 41°C, default | VIN = 5V | 0.2080 | 0.2200 | 0.235 | V |
| V _{T7_Exit} | Hot - 00 @ Approx. 55°C, default | VIN = 5V | 0.1250 | 0.1350 | 0.1450 | V |
| V _{T8_Exit} | Hot - 01 @ Approx. 60°C | VIN = 5V | 0.1050 | 0.1150 | 0.1250 | V |
| V _{T9_Exit} | Hot - 10 @ Approx. 45°C | VIN = 5V | 0.1750 | 0.1850 | 0.1950 | V |
| V _{T10_Exit} | Hot - 11 @ Approx. 40°C | VIN = 5V | 0.2100 | 0.2200 | 0.23 | V |
| V _{TS_ENZ} | TS monitoring enable threshold VTSMR < VTS_ENZ for TS function to be enabled | TS Rising, VIN = 5V | 1.8 | 2.1 | 2.8 | V |
| V _{TS_CLAMP} | TS maximum voltage clamp | TS open-circuit (float), VIN = 5V | 2.2 | 2.8 | 3.3 | V |
| PUSH BUTTON TIMERS AND THRESHOLDS | | | | | | |
| I _{TSMR} | Adapter present | | 36.5 | 38 | 39.5 | μA |
| I _{TSMR} | Battery only mode | | | 60 | | μA |
| V _{TSMR} | TSMR voltage to detect a button press event, battery only mode | | | | 90 | mV |
| V _{TSMR} | TSMR voltage to detect a button press event, adapter present | | | | 90 | mV |
| t _{WAKE1} | WAKE1 Timer. Time from TSMR low detection | MR_WAKE1_TIMER = 0 | | 300 | | ms |
| | | MR_WAKE1_TIMER = 1 | | 1 | | s |
| t _{WAKE2} | WAKE2 Timer. Time from TSMR low detection | MR_WAKE2_TIMER = 0 | | 2 | | s |
| | | MR_WAKE2_TIMER = 1 | | 3 | | s |
| t _{RESET_WARN} | RESET_WARN Timer. Time prior to HW RESET | MR_RESET_WARN = 0 | 0.9 | 1 | 1.1 | s |
| t _{LPRESS} | Long Press timer. Time from button press detection to long press action. | MR_LPRESS = 00 | 4.5 | 5 | 5.5 | s |
| | | MR_LPRESS = 01 | 9 | 10 | 11 | s |
| | | MR_LPRESS = 10 | 13.5 | 15 | 16.5 | s |
| | | MR_LPRESS = 11 | 18 | 20 | 22 | s |
| t _{RESTART(AUTOWAKE)} | RESTART Timer. Time from HW Reset to SYS power up | AUTOWAKE = 00 | | 0.5 | | s |
| | | AUTOWAKE = 01 | | 1 | | s |
| | | AUTOWAKE = 10 | | 2 | | s |
| | | AUTOWAKE = 11 | | 4 | | s |
| BATTERY CHARGING TIMERS | | | | | | |
| t _{MAXCHG} | Charge safety timer | Programmable range | 180 | | 720 | min |
| t _{PRECHG} | Precharge safety timer | | 0.25 * t _{MAXCHG} | | | |
| I2C INTERFACE | | | | | | |
| I _{sink} | /PG pin current sink capability (QFN) | VBAT = 4V | | | 20 | mA |
| V _{IL} | Input low threshold level | VPULLUP = 1.8V, SDA and SCL | | | 0.4 | V |
| V _{IH} | Input high threshold level | VPULLUP = 1.8V, SDA and SCL | 1.3 | | | V |
| V _{OL} | Output low threshold level | IL = 5mA, sink current, VPULLUP = 1.8V | | | 0.4 | V |
| I _{LKG} | High-Level leakage current | VPULLUP = 1.8V | | | 1 | μA |
| LOGIC PINS | | | | | | |

6.5 Electrical Characteristics (continued)

VIN = 5V, VBAT = 3.6V. TJ = 25°C unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------|----------------------------|--|-----|-----|-----|------|
| V _{OL} | Output low threshold level | IL = 5mA, sink current, V _{PULLUP} = 3.3V, /INT pin | | | 0.4 | V |

6.6 Timing Requirements

| | | MIN | NOM | MAX | UNIT |
|---|---|-----|-----|----------|------|
| INPUT | | | | | |
| t _{VIN_OVPZ_DGL} | VIN_OVP deglitch, VIN falling | | 30 | | ms |
| t _{SLEEP_DGL} | Deglitch time to enter SLEEP, VIN falling | | 64 | | μs |
| t _{VIN_WAKE} | V _{IN} Required for Shipmode or Shutdown Exit | 10 | | | ms |
| BATTERY CHARGER | | | | | |
| t _{REC_SC} | Recovery time, BATOCP during Discharge Mode | | 250 | | ms |
| t _{RETRY_SC} | Retry window for SYS or BAT short circuit recovery(BATOCP) | | 2 | | s |
| t _{BUVLO} | Deglitch time to disconnect the BATFET when VBAT < V _{BUVLO} setting | | 60 | | μs |
| t _{TS_DUTY_ON} | TS turnon-time (battery only mode) | | 4 | | ms |
| t _{TS_DUTY_OFF} | TS turnoff time (battery only mode) | | 196 | | ms |
| DIGITAL CLOCK, WATCHDOG and PUSHBUTTON | | | | | |
| t _{WDOG} | I2C interface reset timer, adjustable | 40 | 160 | Disabled | s |
| t _{I2CRESET} | I2C interface inactive reset timer | | 500 | | ms |
| t _{HW_RESET} | Hardware Reset | 4 | | 14 | s |
| t _{SHIPWAKE} | Wake timer to count for ship mode (WAKE2 DefaultTimer) | | 2 | | s |

6.7 Typical Characteristics

VIN = 5 V, CIN = 2.2 μF, COUT = 10 μF, CBAT = 1 μF (unless otherwise specified)

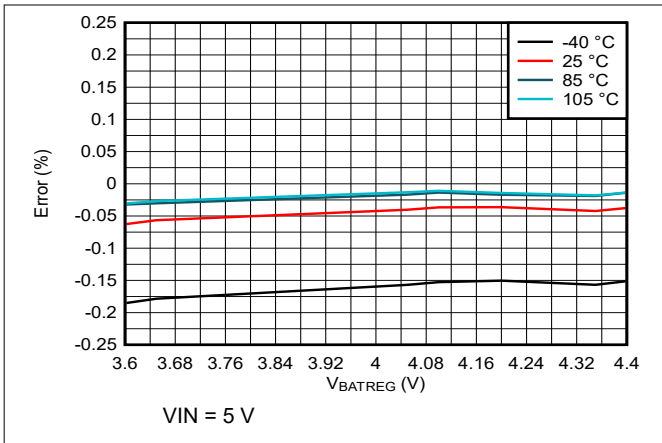


Figure 6-1. Battery Regulation Voltage Accuracy vs VBATREG Setting

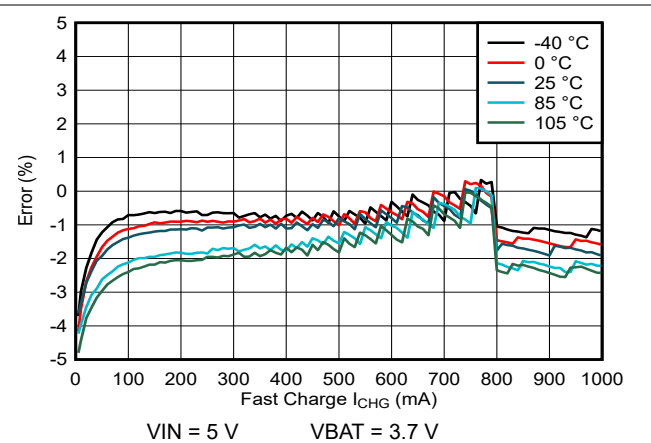


Figure 6-2. Charge Current Accuracy vs ICHARGE Setting

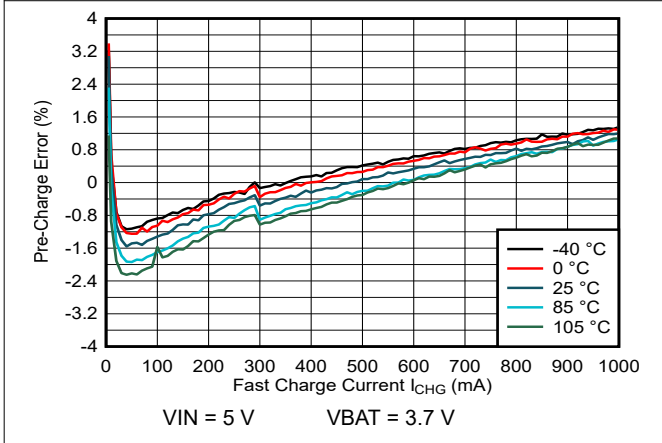


Figure 6-3. Precharge Accuracy vs Battery Voltage

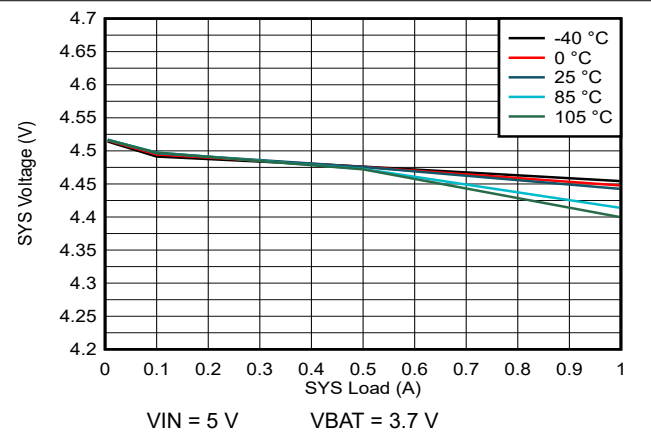


Figure 6-4. SYS Load Regulation

7 Detailed Description

7.1 Overview

The BQ21088 integrates a linear charger that allows the battery to be charged with a programmable charge current of up to 1 A. In addition to the charge current, other charging parameters can be programmed through I²C such as the precharge, termination, and input current limit.

The power path allows the system to be powered from a regulated output, SYS, even when the battery is empty or charging, by drawing power from IN pin. It also prioritizes the system load in SYS, reducing the charging current, if necessary, in order support the load when input power is limited. If the input supply is removed and the battery voltage level is above V_{BUVLO} , SYS will automatically and seamlessly switch to battery power.

Charging is done through the internal battery MOSFET. There are several loops that influence the charge current: constant current loop (CC), constant voltage loop (CV), input current limit, thermal regulation, VDPPM, and VINDPM. During the charging process, all loops are enabled and the one that is dominant takes control.

The device supports multiple battery chemistries for single-cell applications, through adjustable battery regulation voltage regulation (V_{BATREG}) and charge current (I_{CHG}) options.

7.1.1 Battery Charging Process

When a valid input source is connected ($V_{\text{IN}} > V_{\text{INDPM}}$ and $V_{\text{BAT}} + V_{\text{SLEEP}} < V_{\text{IN}} < V_{\text{IN_OVP}}$), the state of the CHARGE_DISABLE bit and the TS/MR pin determine whether a charge cycle is initiated. When the CHARGE_DISABLE bit is set to disable charging, $V_{\text{HOT}} < V_{\text{TS/MR}} < V_{\text{COLD}}$ and a valid input source is connected, the battery FET is turned off, preventing any kind of charging of the battery. Note that supplement behavior is independent of the CHARGE_DISABLE bit. The device will be able to charge a battery as long as VIN voltage is higher than the $V_{\text{IN_LOWV}}$ threshold. This threshold is present as the VIN can be considered "powergood" with a very low battery voltage or a 0-V battery.

The following figure illustrates a typical charge cycle.

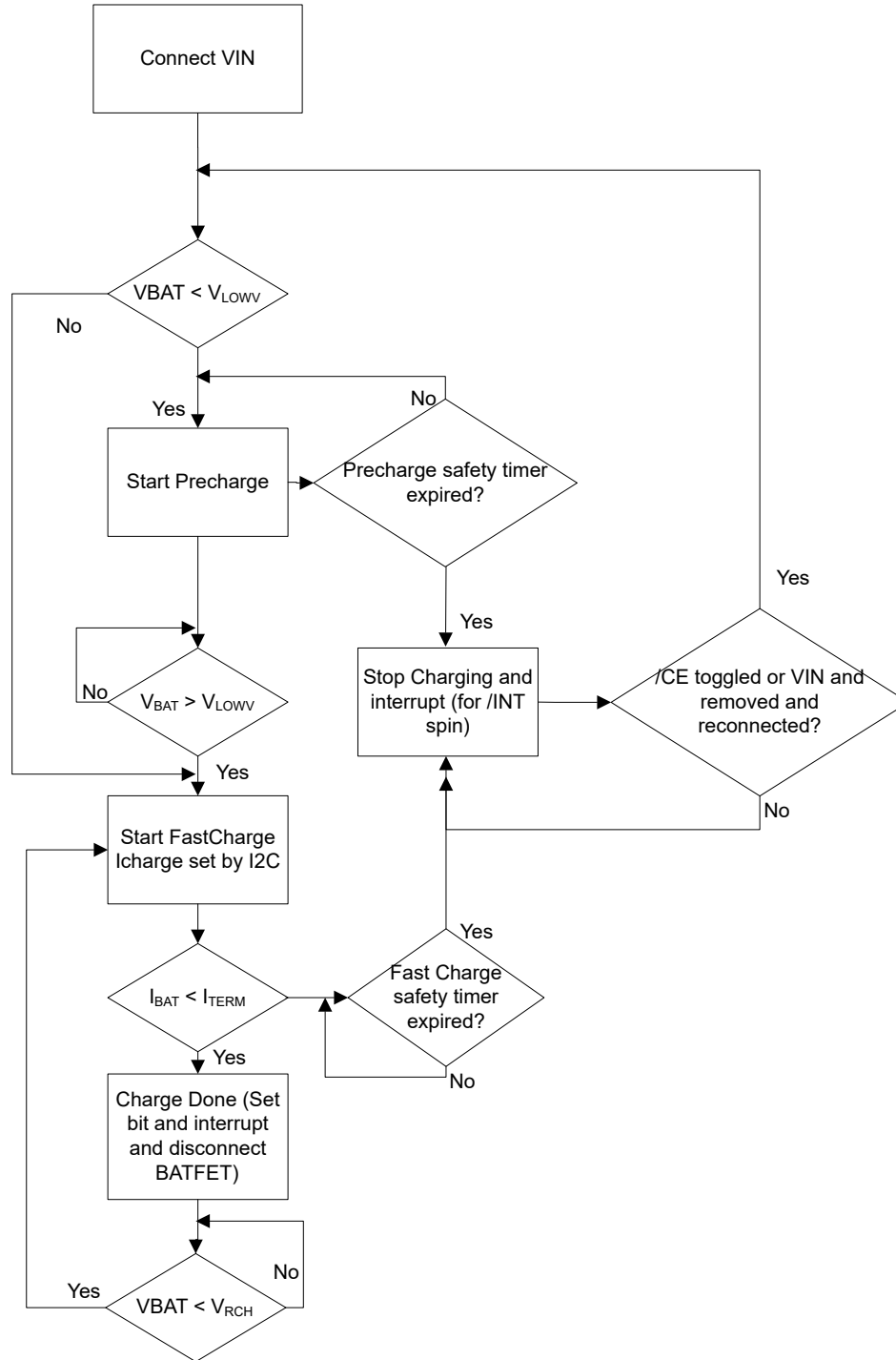


Figure 7-1. Charger Flow Diagram

7.1.1.1 Trickle Charge

In order to prevent damage to the battery, the device will charge the battery at a much lower current level known as trickle charge (I_{BATSC}) when the battery voltage (V_{BAT}) is below the V_{BATSC} threshold. During trickle charge, the device still counts against the precharge safety timer. Rather trickle charge and precharge are counting against the same duration of 25% of the fast charge timer.

7.1.1.2 Pre-Charge

When battery voltage is above the V_{BATSC} but lower than V_{LOWV} threshold, the battery is charged with the pre-charge current (I_{PRECHG}). Pre-charge current is a multiplier of the termination current (Section 8.1.1.5 Termination). As a result, the pre-charge current is a percentage of the fast charge current (I_{CHG}).

When the battery voltage reaches the precharge to fast charge transition threshold (V_{LOWV}), the device charges the battery at the fast charge current. If the device does not exit pre-charge within 25% of the fast charge safety timer, the device will stop charging. For more information on safety timers, see Section 8.3.7.7. Safety Timer.

7.1.1.3 Fast Charge

The charger has two main control loops that control charging when $V_{BAT} > V_{LOWV}$: the Constant Current (CC) and Constant Voltage (CV) loops. When the CC loop is dominant, typically when $V_{BAT} < V_{BATREG} - V_{RCH}$, the battery is charged at the maximum charge current level I_{CHG} , unless there is a TS fault condition, (JEITA operation), VINDPM is active, thermal regulation or DPPM is active. (See respective sections for details on these modes of operation). Once the battery voltage approaches the V_{BATREG} level, the CV loops becomes more dominant and the charging current starts tapering off as shown in Typical Charging Profile of a Battery. Once the charging current reaches the termination current (I_{TERM}) the charge is done, then Charge_done status is set. If the I²C of VBATREG is set higher than 4.65 V, the battery regulation voltage is still maintained at 4.65 V. The device will switch to fast charge based on VLOWV setting.

7.1.1.4 Termination

As the device CV loop becomes more dominate than the CC loop in fast charge operation, the charge current will taper and approach the I_{TERM} threshold. can be configured by I²C transactions writing to the ITERM_0 bits.

Table 7-1. Termination Based on ITERM_0 Bits

| ITERM_0 | TERMINATION THRESHOLD |
|---------|-----------------------|
| 0b00 | Disabled |
| 0b01 | 5 % of I_{CHG} |
| 0b10 | 10 % of I_{CHG} |
| 0b11 | 20 % of I_{CHG} |

Once the I_{TERM} threshold is met during the CV phase, the device automatically terminates charge current by disabling the BATFET (disconnects the battery from SYS) to enter high impedance mode. If there is a regulation loop such as VINDPM, DPPM, or a thermal regulation loop that affects the charge current while the CV loop is tapering the charge current, termination will not occur. Charge current will continue to taper due to the active current affecting regulation loops and CV but the device will not terminate the charge current.

Termination only occurs when the CV loop is operating without any other regulation loops in effect that could reduce the charge current further. Post termination, the battery FET is disabled and the device monitors the BAT pin voltage. If the BAT pin voltage has dropped lower than the battery regulation voltage (V_{BATREG}) by the recharge threshold (V_{RCH}), a new charge cycle is started and safety timers are reset.

During charging or even when charge done, a higher SYS load will be supported through the supplement operation.

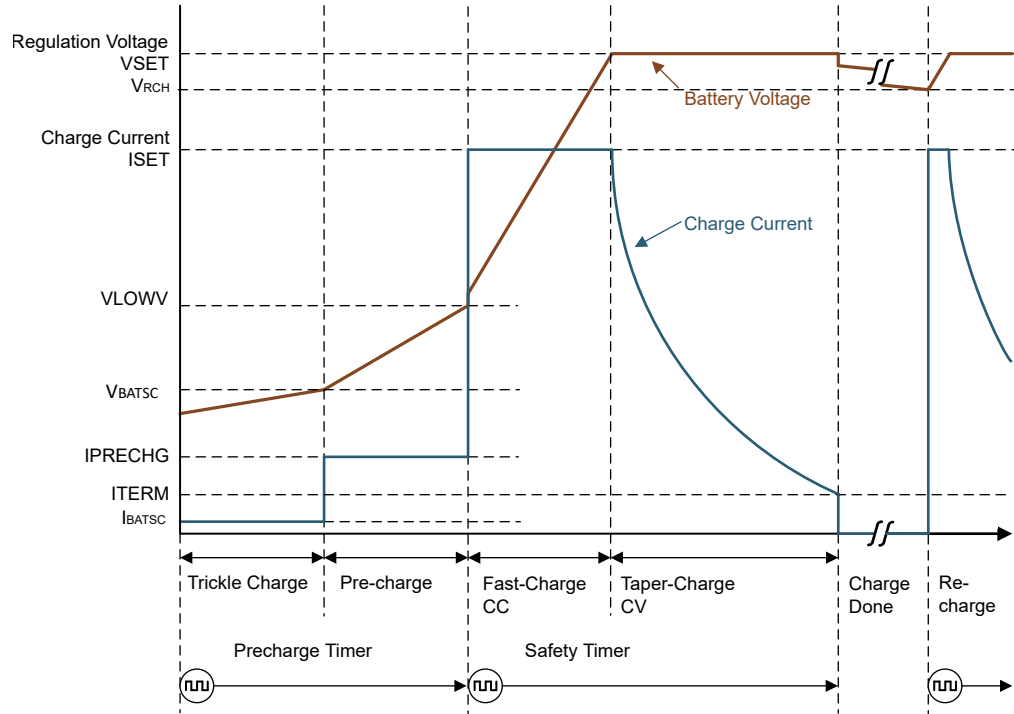


Figure 7-2. Typical Charging Profile of a Battery

7.2 Functional Block Diagram

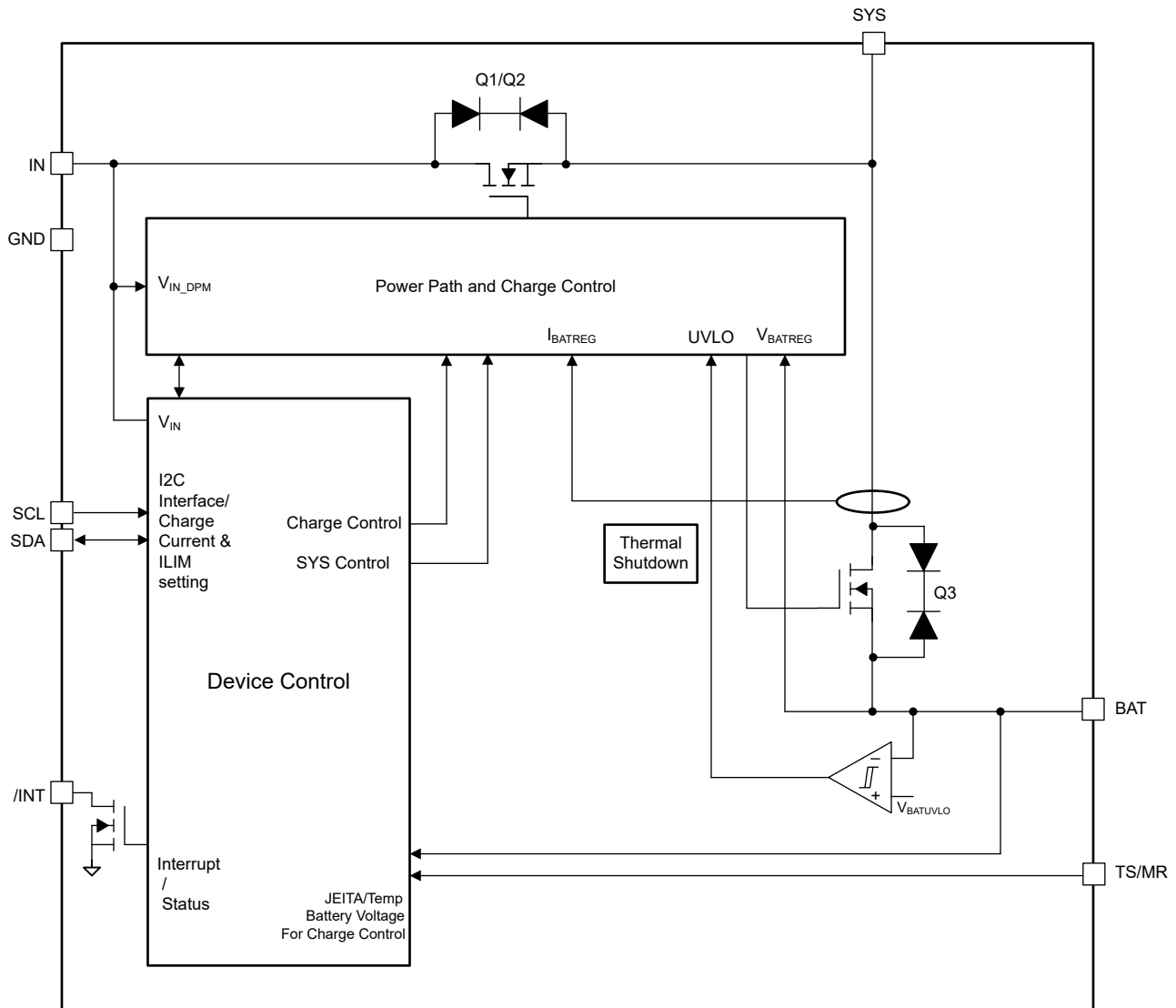


Figure 7-3. Functional Block Diagram

7.3 Feature Description

7.3.1 Input Voltage Based Dynamic Power Management (VINDPM)

The VINDPM loop prevents the input voltage from collapsing to a point where charging would be interrupted. This is done by reducing the current drawn by charger enough to keep the input voltage above the VINDPM threshold (V_{INDPM}).

During the normal charging process, if the input power source is not able to support the programmed or default charging current and System load, the supply voltage decreases. Once the supply drops to the V_{INDPM} threshold, the input DPM current and voltage loops will reduce the input current through the blocking FETs to prevent the further drop of the supply.

The VINDPM threshold is programmable through the I²C register and can be completely disabled. This is set through the VINDPM_0 and VINDPM_1 selection bits. When the device enters this mode, the charge current may be lower than the set value and the VINDPM_ACTIVE_STAT bit is set. If the 2x timer is set through

2XTMR_EN bit, the safety timer is extended while VINDPM is active. The VINDPM threshold can be configured to track battery voltage. In BATTRACK mode, the VINDPM threshold 330 mV above VBAT or 3.6V, whichever is greater. Additionally, termination is disabled when VINDPM is active.

7.3.2 Dynamic Power Path Management Mode (DPPM)

With a valid input source connected, the power-path management circuitry monitors the input voltage and current continuously. The current into IN is shared at SYS between charging the battery and powering the system load at SYS. If the sum of the charging and load currents exceeds the preset maximum input current, the input DPM loop reduces input current. If SYS drops below the DPPM voltage threshold, the charging current is reduced by the DPPM loop through the BATFET. If SYS falls below the supplement mode threshold after BATFET charging current is reduced to zero, the part will enter supplement mode. SYS voltage is maintained above battery voltage when the DPPM loop is in control. Battery termination is disabled when the DPPM loop is active.

The VDPPM threshold is typically 100 mV above VBAT. The VDPPM disable bit (VDPPM_DIS = b1) will allow the charger to operate with lower headroom on VSYS. No current reduction occurs when the voltage between SYS and BAT is less than the VDPPM threshold. In VBAT tracking mode where VSYS is VBAT+225 mV, disabling this bit will have no effect.

7.3.3 Battery Supplement Mode

While in DPPM mode, if the charging current falls to zero and the system load current increases beyond the programmed input current limit, the voltage at SYS reduces further. When the SYS voltage drops below the battery voltage to V_{BSUP1} , the battery supplements the system load. The battery stops supplementing the system load when the voltage on the SYS pin rises within the battery voltage to V_{BSUP2} . During supplement mode, the battery supplement current is not regulated, however, the BATOCP protection circuit is active if enabled. Battery termination is disabled while in supplement mode. Battery voltage has to be higher than battery undervoltage lockout threshold (V_{BUVLO}) to be able to supplement the system.

7.3.4 Sleep Mode

The device enters the low-power sleep mode if V_{IN} falls below the sleep-mode entry threshold and V_{IN} is higher than the undervoltage lockout threshold. In sleep mode, the input is isolated from the battery. This feature prevents draining the battery during the absence of V_{IN} . When $V_{IN} < V_{BAT} + V_{SLEEP}$, the device turns the battery discharge FET on, sends a pulse on the INT output, and the VIN_PGOOD_STAT bits of the register is updated over I²C. Once $V_{IN} > V_{BAT} + V_{SLEEP}$ and V_{IN} exceeds the VINDPM threshold, the device initiates a new charge cycle.

7.3.5 SYS Power Control (SYS_MODE bit control)

The device also offers the option to control SYS through the I²C SYS_MODE bits. These bits can force SYS to be supplied by BAT instead of IN (even if $V_{IN} > V_{BAT} + V_{SLEEP}$), disconnect SYS from either supply, pull SYS down or leave it floating. The table below shows the device behavior based on SYS_MODE setting:

Table 7-2. Settings

| SYS_MODE | DESCRIPTION | SYS SUPPLY | SYS PULL-DOWN |
|----------|-------------------------------|------------|----------------------------|
| 00 | Normal Operation | IN or BAT | Off except during HW reset |
| 01 | Force BAT power (USB Suspend) | BAT | Off except during HW reset |
| 10 | SYS Off – Floating | None | Off |
| 11 | SYS Off – Pulled Down | None | On |

SYS_MODE = 00

This is the default state / normal operation of the device. SYS will be powered from IN if $V_{IN} > V_{UVLO}$, $V_{IN} > V_{BAT} + V_{SLEEP}$, and $V_{IN} < V_{IN_OVP}$. SYS will be powered by BAT if these conditions are not met. SYS will only be disconnected from IN or BAT and pulled down when a HW Reset occurs or the device goes into Ship mode.

SYS_MODE = 01

When this configuration is set, SYS will be powered by BAT if $V_{BAT} > V_{BUVLO}$ regardless of V_{IN} state. This allows the host to minimize the current draw from the adapter while it is still connected as needed in the system. If $SYS_MODE = 01$ is set while $V_{BAT} < V_{BUVLO}$, the $SYS_MODE = 01$ setting will be ignored and the device will go to $SYS_MODE = 00$. In the same manner, if the adapter (V_{IN}) is removed and then connected the device will also switch to $SYS_MODE=00$. This prevents the device from needing a POR in order to restore power to the system thereby allowing battery charging and providing a true USB suspend mode. If $SYS_MODE = 01$ is set during charging, charging will be stopped and the battery will start to provide power to SYS as needed. The behavior is similar to that when the input adapter is disconnected.

SYS_MODE = 10

When this configuration is set, SYS will be disconnected and left floating. The digital remains on and active. When floating, SYS can only be forced to a voltage up to V_{BAT} level. Toggling V_{IN} ($V_{IN} < V_{INUVLO}$) will reset the SYS_MODE to 00.

SYS_MODE = 11

When this configuration is set, SYS will be disconnected and pulled down to ground. Toggling V_{IN} will reset the SYS_MODE to 00.

7.3.5.1 SYS Pulldown Control

The device has an internal pulldown on the SYS pin which is enabled in the following cases:

Table 7-3. States

| STATE | NOTES |
|--------------------------------------|---|
| Shipmode | Pulldown on SYS is enabled once the device enters the shipmode and after disconnecting the BATFET |
| HW_RESET | Pulldown on SYS is enabled after the BATFET and ILIM FET are disconnected and retained until the autowake timer expires |
| $SYS_MODE = 11$ (SYS pulldown mode) | Pulldown on SYS is enabled after the BATFET and ILIM FET are disconnected and retained till either an I2C transaction – changing SYS_MODE or a hardware reset – is given or V_{IN} is toggled. |

7.3.6 SYS Regulation

The BQ21088 includes a SYS voltage regulation loop. By regulating the SYS voltage the device prevents downstream devices connected to SYS from being exposed to voltages as high as V_{IN_OVP} . SYS regulation is only active when $V_{IN} > V_{UVLO}$, $V_{IN} > V_{BAT} + V_{SLEEP}$ and $V_{IN} < V_{IN_OVP}$ rather meeting the $V_{IN_Powergood}$ condition.

SYS voltage regulation target can be controlled through the $SYS_REG_CTRL_2:0$ bits on the SYS_REG Register to either track the battery, set to a fixed voltage, or enable pass through modes.

In battery tracking mode, the minimum voltage is at V_{MINSYS} value for battery < 3.6 V. As battery voltage increases- V_{SYS} is regulated to 225 mV above battery. If $V_{IN} < V_{MINSYS}$ and $V_{IN_Powergood}$ is still active, then the SYS will be in dropout.

In the fixed voltage mode, the SYS voltage is regulated to a target set by the host ranging from 4.4 V to 4.9 V . If V_{IN} voltage is less than the SYS target voltage, then the device will be in dropout mode.

Table 7-4. Regulation

| SYS_REG_CTRL | V_{SYS} TARGET |
|------------------|------------------------------------|
| 000 | $V_{BAT} + 225$ mV (3.8 V minimum) |

Table 7-4. Regulation (continued)

| SYS_REG_CTRL | VSYS TARGET |
|---------------|-------------|
| 001 | 4.4 |
| 010 (default) | 4.5 |
| 011 | 4.6 |
| 100 | 4.7 |
| 101 | 4.8 |
| 110 | 4.9 |
| 111 | Passthrough |

7.3.7 ILIM Control

The input current limit can be controlled through I²C by selecting the ILIM bits.

If the ILIM clamp is active, ILIM_ACTIVE_STAT bit is set.

The MASK_ILIM will prevent interrupt from being issued but does not override the ILIM behavior itself. ILIM value can be programmed dynamically through the I²C by the host.

7.3.8 Protection Mechanisms

7.3.8.1 Input Overvoltage Protection

The input overvoltage protection protects the device and downstream components connected to SYS, and BAT against damage from overvoltage on the input supply. When $V_{IN} > V_{IN_OVP}$, a VIN overvoltage condition is determined to exist. During the VIN overvoltage condition, the device turns the battery discharge FET on, sends a single 128- μ s pulse on INT, and the fault bit (VIN_OVP_FAULT_FLAG) is updated over I²C. The VIN_PGOOD_STAT bit also is affected by VIN overvoltage condition as the VIN powergood condition will fail. For a persisting OVP fault- even after clear on read- the OVP bit will be set right away. Once the VIN overvoltage condition is removed, the VIN_OVP_FAULT_FLAG fault bit is cleared and the device returns to normal operation. Thereafter VIN powergood condition is determined if $V_{IN} > V_{BAT} + V_{SLEEP}$.

7.3.8.2 Battery Undervoltage Lockout

To prevent deep discharge of the battery, the device integrates a battery undervoltage lockout feature that disengages the BAT to SYS path when voltage at the battery drops below the programmed BUVLO voltagesetting present in the CHARGERCTRL1 register. BUVLO status can also be read when a valid voltage on VIN is present.

7.3.8.3 Battery Overcurrent Protection

In order to protect the device from overcurrent and prevent excessive battery discharge current, the device detects if the current on the battery FET exceeds IBAT_OCP. If the BATOCP limit is reached, the battery discharge FET is turned off and the device starts operating in hiccup mode, re-enabling the BATFET t_{REC_SC} (250 ms) after being turned OFF by the over current condition. If the overcurrent condition is triggered upon retry for 4 to 7 consecutive times in a 2-s window, the BATFET shall then remain off until valid VIN is connected ($V_{IN} = V_{IN_POWERGOOD}$). If the overcurrent condition and hiccup operation occurs while in supplement mode where VIN is already present, VIN must be toggled in order for BATFET to be enabled and start another detection cycle.

7.3.8.4 System Overvoltage Protection

The system overvoltage protection is to prevent the SYS from overshooting to a high voltage due to the input supply. The SYS_OVP will momentarily disconnect the blocking FETs and re-engage when the thresholds have dropped to less than SYS_OVP_FALLING threshold.

The SYS_OVP_RISING threshold is typically 120% of the target SYS voltage and the SYS_OVP_FALLING threshold is 117% of the target SYS voltage.

7.3.8.5 System Short Protection

System short protection kicks in when the following conditions are met - the adapter connected the device turns ON the input FET for 5 ms and it detects the SYS pin to be shorted (voltage on SYS $< V_{\text{SYS_SHORT}}$). In this scenario, the device will turn OFF the input FET for 200 μs and turn it back ON for 5 ms for SYS to rise above the V_{SYSSHORT} threshold. If after 10 tries, the voltage at SYS does not rise above the V_{SYSSHORT} threshold, the device will disable both the input and BATFET paths and wait on adapter insertion before turning the paths ON again. A 2s timer is implemented to refresh the retry counter. After 2s, the device will check for system short again repeating the 10 attempts if there is a system short. The device should allow BATFET to supplement SYS during the 10 attempts to identify a short.

7.3.8.6 Thermal Protection and Thermal Regulation

During operation, to protect the device from damage due to overheating, the junction temperature of the die, T_J , is monitored. When T_J reaches $T_{\text{SHUT_RISING}}$ the device stops charging operation and V_{SYS} is shutdown. In the case where $T_J > T_{\text{SHUT_RISING}}$ prior to power being applied to the device (either battery or adapter), the input FET or BATFET will not turn ON, regardless of TSMR pin. Thereafter if temperature falls below $T_{\text{SHUT_FALLING}}$ the device will automatically power up if VIN is present or if in Battery Only mode.

Thermal considerations such as input voltage, charge current, and system load should be taken into account when designing the charging system. It should not be designed such that the device not regularly reaches T_{SHUT} . Rather, device junction temperature should be limited to the [Recommended Operating Temperature conditions](#).

During the charging process, to prevent overheating in the device, the device monitors the junction temperature of the die and reduces the charging current once T_J reaches the thermal regulation threshold (T_{REG}) based on bits set by THERM_REG setting. If the charge current is reduced to 0, the battery supplies the current needed to supply the SYS output.

To ensure that the system power dissipation is under the limit of the device. The power dissipated by the device can be calculated using the following equation:

$P_{\text{DISS}} = P_{\text{SYS}} + P_{\text{BAT}}$ Where:

$$P_{\text{SYS}} = (V_{\text{IN}} - V_{\text{SYS}}) * I_{\text{IN}}$$

$$P_{\text{BAT}} = (V_{\text{SYS}} - V_{\text{BAT}}) * I_{\text{BAT}}$$

The die junction temperature, T_J , can be estimated based on the expected board performance using the following equation:

$$T_J = T_A + \theta_{\text{JA}} * P_{\text{DISS}}$$

The θ_{JA} is largely driven by the board layout, board layers, copper thickness and the layout. For more information about traditional and new thermal metrics, see the [IC Package Thermal Metrics Application Report](#). Under typical conditions, the time spent in this state is very short.

7.3.8.7 Safety Timer and Watchdog Timer

At the beginning of each charge cycle mode (Precharge or Fast Charge), the device starts the respective mode safety timer. If charging has not terminated before the programmed safety time, t_{MAXCHG} expires or the device does not exit the precharge mode before t_{PRECHG} expires, charging is disabled. The precharge safety timer, t_{PRECHG} , is 25% of t_{MAXCHG} . When a safety timer fault occurs, a single 128- μs pulse is sent to the /INT pin and the STAT and FAULT bits of the status registers are updated. The charge enable bit or the input power must be toggled in order to clear the safety timer.

If the safety timer has expired, the device will produce an interrupt and update the SAFETY_TMR_FAULT_FLAG bit on the register map. The safety timer duration is programmable using the SAFETY_TIMER_1:0 bits. When the safety timer is active, changing the safety timer duration resets the safety timer. The device also contains

a 2XTMR_EN bit that doubles the safety timer duration to prevent premature safety timer expiration when the charge current is reduced by a high load on SYS (DPM operation- causing VDPPM to be enabled), VINDPM, thermal regulation, or a NTC (JEITA) condition. When 2XTMR_EN bit is set, the timer is allowed to run at half speed when any loop is active other than CC or CV. If the charge current is reduced by pre-charge or TS_Cool then 2XTMR_EN has no effect and the safety timer runs at normal speed. Input sources that can't provide sufficient current even at a significantly lowered charge current may not be operating properly so it is safest to not double safety timer duration. In the event where during CC mode the battery voltage drops to push the charger into precharge mode, (due to a large load on battery, thermal events, and so forth) the safety timer will reset counting through precharge and then resetting the fast charge safety timer. If the device entered battery supplement mode while in precharge, CC or CV mode, while the charger is not disabled, the device will suspend the safety timer till the charging can resume back again. This prevents the safety timer from resetting when a supplement condition is caused.

In addition to the safety timer, the device contains a watchdog timer that monitors the host through the I²C interface. The watchdog timer is enabled by default and may be disabled by the host through an I²C transaction. Once the initial transaction is received, the watchdog timer is started. The watchdog timer is reset by any transaction by the host using the I²C interface. If the watchdog timer expires without a reset from the I²C interface, all R/W registers are reset to the default values. Watchdog timer can be set through the WATCHDOG_SEL_1:0 bits either on battery only mode or when adapter is present.

7.3.9 Pushbutton Wake and Reset Input

The pushbutton function implemented through TS/MR pin has three main functions. First, it serves as a means to wake the device from ultra-low power modes like Factory mode. Second, it serves as a short button press detector, sending an interrupt to the host when the button driving the TSMR pin has been pressed for a Wake1, Wake2 or long press durations. This allows the implementation of different functions in the end application such as menu selection and control. Finally it serves as a mean to get device into , Shutdown mode, or reset the system by performing a power cycle (shut down SYS and automatically powering it back on) after detecting a long button press. The timing for the short and long button press duration is programmable through I²C for added flexibility and allows system designers to customize the end user experience of a specific application. Note that if a specific timer duration is changed through I²C while that timer is active and has not expired, the new programmed value will be ignored until the timer expires and/or is reset by /MR.

7.3.9.1 Pushbutton Wake or Short Button Press Functions

There are two programmable wake or short button press timers, Wake1 and Wake2. There are no specific actions taken by the t_{wake1} or t_{wake2} durations other than issuing an interrupt and updating the MR_WAKE registers. For a wake from ship mode event , the push button has to be low for $t_{shipwake}$ before it can turn ON the SYS rail. This only applies to ship mode; a button press that pulls the TS/MR pin low for a duration $t_{shipwake}$ will not turn on the SYS rail when the device is in shutdown mode.

In the case where a valid V_{IN} ($V_{IN} > V_{UVLO}$) is connected prior to $t_{shipwake}$ timer expiring, the device will exit the shipmode immediately regardless of the TS/MR or wake timer state. V_{IN} should remain valid for t_{VIN_WAKE} to allow for a proper shipmode exit. Refer to [Section 7.5](#) for more details.

The EN_PUSH bit will enable the button checking event through the periodic wake up of the current source on the TSMR pin. The timing will be similar to when in shipmode. When this bit is enabled all button events such as Wake1, Wake2 and MR_LPRESS events are valid. When this function is disabled, the button events are ignored. When the adapter is present and charging is actively in progress, this bit status is ignored as the current source is ON/ OFF when the NTC is being checked.

7.3.9.2 Pushbutton Reset or Long Button Press Functions

Depending on the configuration set on pushbutton long press action register bits, the device will perform a ship mode entry, shutdown mode entry, or hardware reset or completely ignore the long button press action. Toggling the /CE pin will restart the timer for the long press button when VIN is present.

To wake up the device from ship mode , there are two methods: a valid VIN power up or holding the TS/MR button for a time $t_{SHIPWAKE}$.

7.3.10 15-Second Timeout for HW Reset

Based on the I²C register bit WATCHDOG_15S_ENABLE the device can perform HW reset/power cycle in the same manner a long button press or HW_RESET would. This 15-second watchdog or timeout is gated upon $V_{IN} > V_{VBAT} + V_{SLEEP}$ so that the HW reset would only occur if the host does not respond after a charger is connected and the

If the charger is connected and the host responds before the 15-second watchdog expires, the part continues in normal operation and starts the normal 50-second watchdog timer if enabled. The 15-second watchdog may be enabled/ disabled through I²C through the WATCHDOG_15S_ENABLE bit.

7.3.11 Hardware Reset

The device is capable of hardware reset to completely powercycle the system. This is particularly useful when a soft reset on the MCU or host fails to work. A hardware reset needs to be possible in all SYS MODES.

There are a few ways a hardware reset occurs. A hardware reset will occur when:

1. The HW_RESET clock expires when the WATCHDOG_SEL is set to 0b01 or 0b10
2. No I2C transaction occurs when VIN is plugged in when the WATCHDOG_15_SENABLE is set to 0b1 within 15s
3. EN_RST_SHIP is set to 2b11
4. PB_LPRESS_ACTION is set to 2b11 and the button has been pressed for a duration set by MR_LP_LPRESS

Below is a sequence of events during a hardware reset:

1. Turn OFF (if adapter is present) input FET
2. Turn OFF battery FET
3. Engage pulldown on SYS
4. Start the Autowake timer
5. Once the Autowake timer expires, disconnect the pulldown on SYS
6. Reset all registers to default (as in new power up)
7. Turn ON battery FET and input FET (if applicable).

At a time t_{RESET_WARN} before the reset pulldown on SYS occurs, an interrupt occurs to signify a hardware reset is about to occur.

7.3.12 Software Reset

When a software reset is issued either through the watchdog action configurable through WATCHDOG_SEL bits or register reset configurable through REG_RST bit, the device will reset all the registers to defaults.

7.3.13 Interrupt Indicator (/INT) Pin

The device contains an open-drain output that signals its status and is valid only after the device has completed start-up into a valid state. If the part starts into a fault, interrupts will not be sent.

The /INT pin is normally in high impedance and is pulled low for 128 μ s when an interrupt condition occurs. When a fault or status change occurs or any other condition that generates an interrupt, a 128- μ s pulse (/INT pin pulled down) is sent on /INT to notify the host.

Interrupts can be masked through I²C. If the interrupt condition occurs while the interrupt is masked an interrupt pulse will not be sent. If the interrupt is unmasked while the fault condition is still present, an interrupt pulse will not be sent until the /INT trigger condition occurs while unmasked. Below are a list of interrupts that can be masked through I²C.

Table 7-5. Mask Bit

| MASK BIT | ACTION |
|---------------|---|
| ILIM_INT_MASK | Do not issue an /INT pulse when ILIM limiting occurs |
| DPM_INT_MASK | Do not issue an /INT pulse when VINDPM is active or VDPPM |

Table 7-5. Mask Bit (continued)

| MASK BIT | ACTION |
|---------------------|---|
| TS_INT_MASK | Do not issue an /INT pulse when any of the TS events have occurred. |
| TREG_INT_MASK | Do not issue an /INT pulse when TREG is actively reducing the current |
| BAT_INT_MASK | Do not issue an /INT pulse when BATOCP or BUVLO event is triggered |
| CHG_STATUS_INT_MASK | Do not send an interrupt anytime there is a charging status change. |

7.3.14 External NTC Monitoring (TS)

7.3.14.1 TS Biasing and Function

The device is configured to meet JEITA requirements ora simpler HOT/COLD function only. Additionally, the TS charger control function can be disabled through the TS_EN bit. This will only disable the TS charge action but the faults are still reported based on the TS voltage. To satisfy the JEITA requirements, four temperature thresholds are monitored: the cold battery threshold, the cool battery threshold, the warm battery threshold, and the hot battery threshold. These temperatures correspond to the V_{COLD} , V_{COOL} , V_{WARM} , and V_{HOT} thresholds in the Electrical Characteristics table. Charging and safety timers are suspended when $V_{TS} < V_{HOT}$ or $V_{TS} > V_{COLD}$. When $V_{COOL} < V_{TS} < V_{COLD}$, the charging current is reduced to the value programmed in the TS_Setting register/ bit TS_ICHG_0. When $V_{HOT} < V_{TS} < V_{WARM}$, the battery regulation voltage is reduced by 100 mV or 200 mV based on the value programmed in TS_VRCG_0 bit within the TS_Setting register.

For devices where the TS function is not needed, tie a 10-kΩ resistor to the TS/MR pin.

There is an active voltage clamp present on this device which will prevent the voltage on TS/MR pin from rising above the V_{TS_CLAMP} threshold. This will particularly be ON when the TS/MR pin is floating. The bit TS_OPEN_STAT is set when this clamp is active. This will also be ON regardless of the TS_EN bit. The interrupt is asserted as long as the TS_INT mask is not written.

The bits TS_HOT, TS_COLD, TS_WARM and TS_COOL will allow these thresholds to be adjusted slightly. The hysteresis will also move along with these thresholds. When the TS_WARM condition occurs, the device will lower the battery target regulation voltage by TS_VRCG but will not modify the VBAT_CTRL register.

The TS_ICHG bit will reduce charging current based on the factor described in the register map when the TSMR pin hits a TS_COOL condition. The TREG function will still be based on this reduced threshold.

The TS_VRCG_0 bit will reduce the charging voltage when the TS/MR pin hits the TS_WARM threshold. The factor will be based on the register map.

When the button is detected as a “press” during the charging process, charging will be momentarily suspended until the button is high again. When charging is disabled in any of the TS faults, the trickle charging is also disabled. In a TS fault where the current is reduced (COOL), the trickle charging current is not altered.

7.3.15 I²C Interface

The device uses an I²C compatible interface to program and read control parameters, status bits, etc. I²C™ is a 2-wire serial interface developed by Philips Semiconductor (see I²C-Bus Specification, Version 2.1, January 2000). The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I²C compatible devices connect to the I²C bus through open drain I/O pins, SDA and SCL. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and/or transmits data on the bus under control of the master device.

The device works as a peripheral and supports the following data transfer modes, as defined in the I²C Bus™ Specification: standard mode (100 kbps) and fast mode (400 kbps). The interface adds flexibility to the battery

charge solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements.

Register contents remain intact as long as V_{BAT} or V_{IN} voltages remains above their respective undervoltage lockout thresholds and the device is not in shutdown mode.

The data transfer protocol for standard and fast modes is exactly the same; therefore, they are referred to as the F/S-mode in this document. The device only supports 7-bit addressing. The device 7-bit address is 0x6A (8-bit shifted address is 0xD4).

7.3.15.1 F/S Mode Protocol

The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 7-4. All I²C-compatible devices should recognize a start condition.

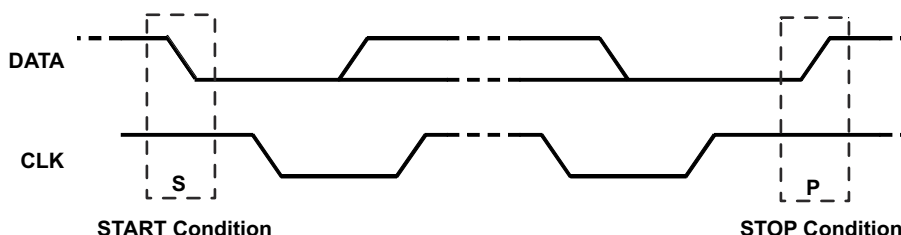


Figure 7-4. START and STOP Condition

The master then generates the SCL pulses, and transmits the 8-bit address and the read/write direction bit R/W on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 7-5). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an acknowledge (see Figure 7-6) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master knows that communication link with a slave has been established.

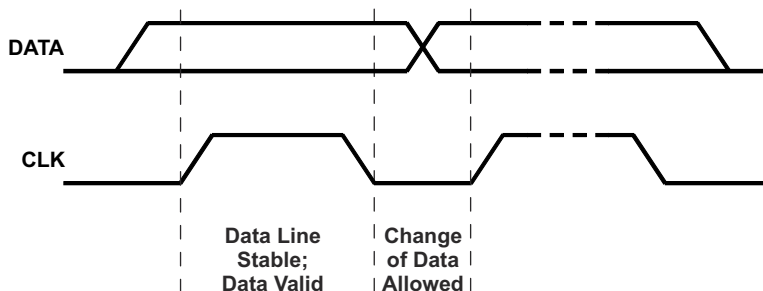


Figure 7-5. Bit Transfer on the Serial Interface

The master generates further SCL cycles to either transmit data to the slave (R/W bit 1) or receive data from the slave (R/W bit 0). In either case, the receiver needs to acknowledge the data sent by the transmitter. So an acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. The 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary. To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see Figure 7-4). This releases the bus and stops the communication link with the addressed slave. All I²C compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and wait for a start condition followed by a matching address. If a transaction is terminated prematurely, the master needs sending a STOP condition to prevent the slave I²C logic from remaining in an incorrect state. Attempting to read data from register addresses not listed in this section will result in FFh being read out.

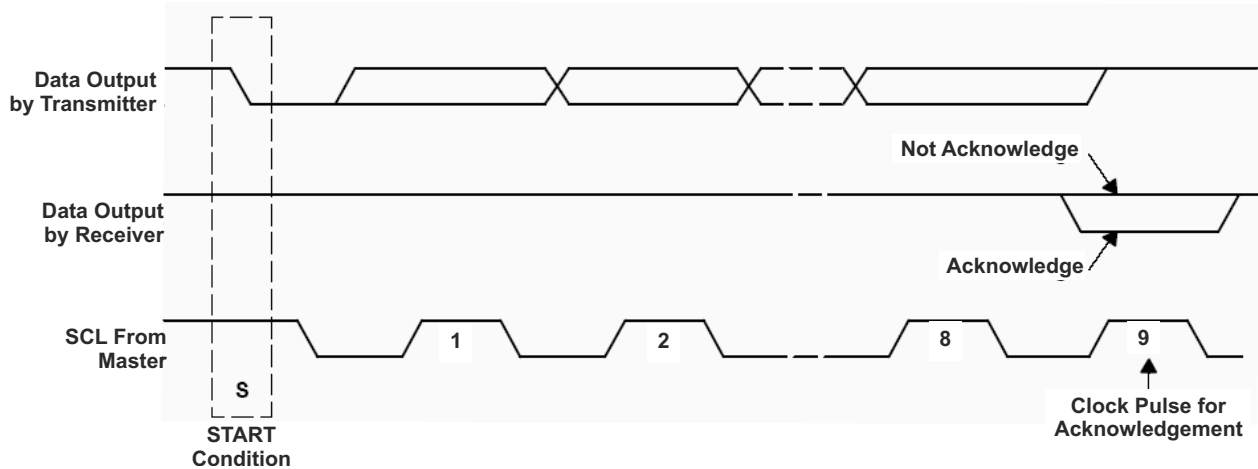


Figure 7-6. Acknowledge on the I²C Bus

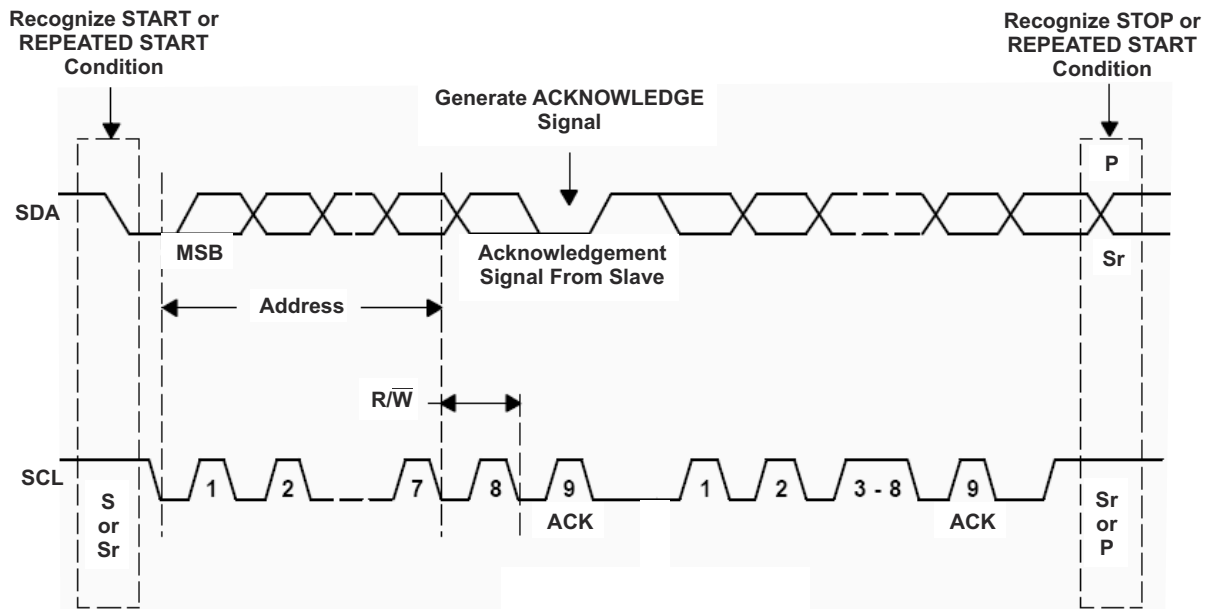


Figure 7-7. Bus Protocol

7.4 Device Functional Modes

The BQ21088 has four main modes of operation: Charger/Adapter Mode (when a supply is connected to IN), Battery Mode (when only battery is connected), Ship Mode, and Shutdown Mode. The table below summarizes the functions that are active for each operation mode.

Table 7-6. Device Functional Modes

| FUNCTION | CHARGER/ADAPTER MODE | BATTERY MODE | SHIP MODE | SHUTDOWN MODE |
|-------------------------------|----------------------|--------------|-----------|---------------|
| Input Overvoltage | Yes | Yes | No | No |
| Input Undervoltage | Yes | Yes | Yes | Yes |
| Battery Overcurrent | Yes | Yes | Yes | No |
| Input DPM | Yes | No | Yes | No |
| Dynamic Power Path Management | Yes | No | No | No |

Table 7-6. Device Functional Modes (continued)

| FUNCTION | CHARGER/ADAPTER MODE | BATTERY MODE | SHIP MODE | SHUTDOWN MODE |
|---------------------|---------------------------------|---------------------|------------------|----------------------|
| BATFET | Yes | Yes | No | No |
| TS Measurement | Yes | No | No | No |
| Battery Charging | Yes | No | No | No |
| Input Current Limit | Yes | No | No | No |
| Pushbutton Input | Yes | No | No | No |

7.5 Register Maps

7.5.1 I²C Registers

Table 7-7 lists the I²C registers. All register offset addresses not listed in Table 7-7 should be considered as reserved locations and the register contents should not be modified.

Table 7-7. I²C Registers

| Offset | Acronym | Register Name | Section |
|--------|-------------|--|--------------------|
| 0x0 | STAT0 | Charger Status | Go |
| 0x1 | STAT1 | Charger Status and Faults | Go |
| 0x2 | FLAG0 | Charger Flag Registers | Go |
| 0x3 | VBAT_CTRL | Battery Voltage Control | Go |
| 0x4 | ICHG_CTRL | Fast Charge Current Control | Go |
| 0x5 | CHARGECTRL0 | Charger Control 0 | Go |
| 0x6 | CHARGECTRL1 | Charger Control 1 | Go |
| 0x7 | IC_CTRL | IC Control | Go |
| 0x8 | TMR_ILIM | Timer and Input Current Limit Control | Go |
| 0x9 | SHIP_RST | Shipmode, Reset and Pushbutton Control | Go |
| 0xA | SYS_REG | SYS Regulation Voltage Control | Go |
| 0xB | TS_CONTROL | TS Control | Go |
| 0xC | MASK_ID | MASK and Device ID | Go |

Complex bit access types are encoded to fit into small table cells. Table 7-8 shows the codes that are used for access types in this section.

Table 7-8. I²C Access Type Codes

| Access Type | Code | Description |
|------------------------|------|--|
| Read Type | | |
| R | R | Read |
| RC | RC | Read to Clear |
| Write Type | | |
| W | W | Write |
| Reset or Default Value | | |
| - n | | Value after reset or the default value |

7.5.1.1 STAT0 Register (Offset = 0x0) [Reset = X]

STAT0 is shown in [Figure 7-8](#) and described in [Table 7-9](#).

Return to the [Summary Table](#).

Figure 7-8. STAT0 Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|--------------|---|------------------|-------------------|--------------------|----------------------|----------------|
| TS_OPEN_STAT | CHG_STAT_1:0 | | ILIM_ACTIVE_STAT | VDPPM_ACTIVE_STAT | VINDPM_ACTIVE_STAT | THERMREG_ACTIVE_STAT | VIN_PGOOD_STAT |
| R-X | R-X | | R-X | R-X | R-X | R-X | R-X |

Table 7-9. STAT0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------------|------|-------|--|
| 7 | TS_OPEN_STAT | R | X | TS Open Status (Clamp is active) 1b0 = TSMR pin is not Open 1b1 = TSMR pin is Open or $V_{BAT} < V_{BAT_HALT}$. |
| 6-5 | CHG_STAT_1:0 | R | X | Charging Status Indicator 2b00 = Not Charging while charging is enabled. 2b01 = Constant Current Charging (Trickle Charge/ Pre Charge or in Fast Charge Mode) 2b10 = Constant Voltage Charging 2b11 = Charge Done or charging is disabled by the host. |
| 4 | ILIM_ACTIVE_STAT | R | X | Input Current Limit Active 1b0 = Not Active 1b1 = Active |
| 3 | VDPPM_ACTIVE_STAT | R | X | VDPPM Mode Active 1b0 = Not Active 1b1 = Active |
| 2 | VINDPM_ACTIVE_STAT | R | X | VINDPM Mode Active 1b0 = Not Active 1b1 = Active |
| 1 | THERMREG_ACTIVE_STAT | R | X | Thermal Regulation Active 1b0 = Not Active 1b1 = Active |
| 0 | VIN_PGOOD_STAT | R | X | VIN Power Good 1b0 = VIN Power Not Good 1b1 = VIN Power Good |

7.5.1.2 STAT1 Register (Offset = 0x1) [Reset = X]

STAT1 is shown in [Figure 7-9](#) and described in [Table 7-10](#).

Return to the [Summary Table](#).

Figure 7-9. STAT1 Register

| 7 | | 6 | | 5 | | 4 | | 3 | | 2 | | 1 | | 0 | |
|--------------|--|------------|--|----------|--|-------------|--|-----------------------|--|------------|--|------------|--|---|--|
| VIN_OVP_STAT | | BUVLO_STAT | | RESERVED | | TS_STAT_1:0 | | SAFETY_TMR_FAULT_FLAG | | WAKE1_FLAG | | WAKE2_FLAG | | | |
| R-1b0 | | R-X | | R-X | | R-2b00 | | RC-1b0 | | RC-1b0 | | RC-1b0 | | | |

Table 7-10. STAT1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------------|------|-------|---|
| 7 | VIN_OVP_STAT | R | 1b0 | VIN_OVP Status 1b0 = Not Active 1b1 = Active |
| 6 | BUVLO_STAT | R | X | Battery UVLO Status 1b0 = Not Active 1b1 = Active |
| 4-3 | TS_STAT_1:0 | R | 2b00 | TS Status 2b00 = Normal 2b01 = VTS < VHOT or VTS > VCOLD(charging suspended) 2b10 = VCOOL < VTS < VCOLD (Charging current reduced by value set by TS_Registers) 2b11 = VWARM > VTS > VHOT (Charging voltage reduced by value set by TS_Registers) |
| 2 | SAFETY_TMR_FAULT_FLAG | RC | 1b0 | Safety Timer Expired Fault Cleared only after CE is toggled. 1b0 = Not Active 1b1 = Active |
| 1 | WAKE1_FLAG | RC | 1b0 | Wake 1 Timer Flag 1b0 = Does not meet Wake 1 Condition 1b1 = Met Wake 1 Condition |
| 0 | WAKE2_FLAG | RC | 1b0 | Wake 2 Timer Flag 1b0 = Does not meet Wake 2 Condition 1b1 = Met Wake2 Condition |

7.5.1.3 FLAG0 Register (Offset = 0x2) [Reset = X]

FLAG0 is shown in [Figure 7-10](#) and described in [Table 7-11](#).

Return to the [Summary Table](#).

Figure 7-10. FLAG0 Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|------------------|-------------------|--------------------|----------------------|--------------------|------------------|---------------|
| TS_FAULT | ILIM_ACTIVE_FLAG | VDPPM_ACTIVE_FLAG | VINDPM_ACTIVE_FLAG | THERMREG_ACTIVE_FLAG | VIN_OVP_FAULT_FLAG | BUVLO_FAULT_FLAG | BAT_OCP_FAULT |
| RC-X | RC-X | RC-X | RC-X | RC-X | RC-X | RC-X | RC-X |

Table 7-11. FLAG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------------|------|-------|--|
| 7 | TS_FAULT | RC | X | TS_Fault 1b0 = No TS Fault detected 1b1 = TS Fault detected |
| 6 | ILIM_ACTIVE_FLAG | RC | X | ILIM Active 1b0 = NO ILIM Fault detected 1b1 = ILIM Fault detected |
| 5 | VDPPM_ACTIVE_FLAG | RC | X | VDPPM FLAG 1b0 = VDPPM fault not detected 1b1 = VDPPM fault detected |
| 4 | VINDPM_ACTIVE_FLAG | RC | X | VINDPM FLAG 1b0 = VINDPM fault not detected 1b1 = VINDPM fault detected |
| 3 | THERMREG_ACTIVE_FLAG | RC | X | Thermal Regulation FLAG 1b0 = No thermal regulation detected 1b1 = Thermal regulation has occurred |
| 2 | VIN_OVP_FAULT_FLAG | RC | X | VIN_OVP FLAG 1b0 = VIN_OVP fault not detected 1b1 = VIN_OVP fault detected |
| 1 | BUVLO_FAULT_FLAG | RC | X | Battery undervoltage FLAG 1b0 = Battery undervoltage fault not detected 1b1 = Battery undervoltage fault detected |
| 0 | BAT_OCP_FAULT | RC | X | Battery overcurrent protection 1b0 = Battery overcurrent condition not detected 1b1 = Battery overcurrent condition detected |

7.5.1.4 VBAT_CTRL Register (Offset = 0x3) [Reset = 0x46]

VBAT_CTRL is shown in [Figure 7-11](#) and described in [Table 7-12](#).

Return to the [Summary Table](#).

Figure 7-11. VBAT_CTRL Register

| | | | | | | | |
|----------|-------------|---------------|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | VBATREG_6:0 | | | | | | |
| R/W-1b0 | | R/W-7b1000110 | | | | | |

Table 7-12. VBAT_CTRL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------|------|-----------|---|
| 7 | PG_MODE | R/W | 1b0 | PG_GPO pin as GPO 1b0 = PG_GPO as a status of VIN (Power Good) 1b1 = PG_GPO as a general-purpose output pin (GPO) |
| 6-0 | VBATREG_6:0 | R/W | 7b1000110 | Battery Regulation Voltage VBATREG= 3.5V + VBATREG_CODE * 10mV. Maximum programmable voltage = 4.65V |

7.5.1.5 ICHG_CTRL Register (Offset = 0x4) [Reset = 0x5]

ICHG_CTRL is shown in [Figure 7-12](#) and described in [Table 7-13](#).

Return to the [Summary Table](#).

Figure 7-12. ICHG_CTRL Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------------|---|---|---|---|---|---|
| CHG_DIS | ICHG_6:0 | | | | | | |
| R/W-1b0 | R/W-7b0000101 | | | | | | |

Table 7-13. ICHG_CTRL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-----------|---|
| 7 | CHG_DIS | R/W | 1b0 | Charge Disable 1b0 = Battery Charging Enabled 1b1 = Battery Charging Disabled |
| 6-0 | ICHG_6:0 | R/W | 7b0000101 | For ICHG ≤ 35mA = ICHGCODE +5mA For ICHG > 35mA = 40+ ((ICHGCODE-31)*10)mA. Maximum programmable current = 1000mA |

7.5.1.6 CHARGECTRL0 Register (Offset = 0x5) [Reset = 0x24]

CHARGECTRL0 is shown in [Figure 7-13](#) and described in [Table 7-14](#).

Return to the [Summary Table](#).

Figure 7-13. CHARGECTRL0 Register

| | | | | | | | |
|----------|---------|-----------|---|------------|---|---------------|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | IPRECHG | ITERM_1:0 | | VINDPM_1:0 | | THERM_REG_1:0 | |
| R/W-1b0 | R/W-1b0 | R/W-2b10 | | R/W-2b01 | | R/W-2b00 | |

Table 7-14. CHARGECTRL0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------|------|-------|---|
| 7 | EN_FC_MODE | R/W | 1b0 | Enable or disable Flash Charging mode 1b0 = Disable 1b1 = Enable |
| 6 | IPRECHG | R/W | 1b0 | Precharge current = x times of term 1b0 = Precharge is 2x Term 1b1 = Precharge is Term |
| 5-4 | ITERM_1:0 | R/W | 2b10 | Termination current = % of Icharge 2b00 = Disable 2b01 = 5% of ICHG 2b10 = 10% of ICHG 2b11 = 20% of ICHG |
| 3-2 | VINDPM_1:0 | R/W | 2b11 | VINDPM Level Selection 2b00 = VBAT + 300 mV. 2b01 = 4.5 V 2b10 = 4.7 V 2b11 = Disabled |
| 1-0 | THERM_REG_1:0 | R/W | 2b00 | Thermal Regulation Threshold 2b00 = 100C 2b01 = 80C 2b10 = 60C 2b11 = Disabled |

7.5.1.7 CHARGECTRL1 Register (Offset = 0x6) [Reset = 0x56]

CHARGECTRL1 is shown in [Figure 7-14](#) and described in [Table 7-15](#).

Return to the [Summary Table](#).

Figure 7-14. CHARGECTRL1 Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|---|-----------|---|---|---------------------|---------------|-----------------|
| IBAT_OCP_1:0 | | BUVLO_2:0 | | | CHG_STATUS_INT_MASK | ILIM_INT_MASK | VINDPM_INT_MASK |
| R/W-2b01 | | R/W-3b010 | | | R/W-1b1 | R/W-1b1 | R/W-1b0 |

Table 7-15. CHARGECTRL1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------------|------|-------|--|
| 7-6 | IBAT_OCP_1:0 | R/W | 2b01 | Battery Discharge Current Limit 2b00 = 500mA 2b01 = 1000mA 2b10 = 1500mA 2b11 = 3000mA |
| 5-3 | BUVLO_2:0 | R/W | 3b010 | Battery Undervoltage LockOut Threshold Falling (150mV Hist). 3b000 = 3.0V 3b001 = 3.0V 3b010 = 3.0V 3b011 = 2.8V 3b100 = 2.6V 3b101 = 2.4V 3b110 = 2.2V 3b111 = 2.0V |
| 2 | CHG_STATUS_INT_MASK | R/W | 1b1 | Mask Charging Status Interrupt 1b0 = Enable Charging Status Interrupt anytime there is a charging status change. 1b1 = Mask Charging Status Interrupt |
| 1 | ILIM_INT_MASK | R/W | 1b1 | Mask ILIM Fault Interrupt 1b0 = Enable ILIM Interrupt 1b1 = Mask ILIM Interrupt |
| 0 | VINDPM_INT_MASK | R/W | 1b0 | Mask VINDPM Interrupt 1b0 = Enable VINDPM and DPPM Interrupt 1b1 = Mask VINDPM and DPPM Interrupt |

7.5.1.8 IC_CTRL Register (Offset = 0x7) [Reset = 0x84]

IC_CTRL is shown in [Figure 7-15](#) and described in [Table 7-16](#).

Return to the [Summary Table](#).

Figure 7-15. IC_CTRL Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-----------|---------|----------|------------------|---|------------------|---|
| TS_EN | VLOWV_SEL | VRCH_0 | 2XTMR_EN | SAFETY_TIMER_1:0 | | WATCHDOG_SEL_1:0 | |
| R/W-1b1 | R/W-1b0 | R/W-1b0 | R/W-1b0 | R/W-2b01 | | R/W-2b00 | |

Table 7-16. IC_CTRL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------------|------|-------|---|
| 7 | TS_EN | R/W | 1b1 | TS Auto Function 1b0 = TS auto function disabled (Only charge control is disabled. TS monitoring is enabled) 1b1 = TS auto function enabled |
| 6 | VLOWV_SEL | R/W | 1b0 | Precharge Voltage Threshold (VLOWV) 1b0 = 3V 1b1 = 2.8V |
| 5 | VRCH_0 | R/W | 1b0 | Recharge Voltage Threshold 1b0 = 100mV 1b1 = 200 mV |
| 4 | 2XTMR_EN | R/W | 1b0 | Timer Slow 1b0 = The timer is not slowed at any time 1b1 = The timer is slowed by 2x when in any control other than CC or CV |
| 3-2 | SAFETY_TIMER_1:0 | R/W | 2b01 | Fast Charge Timer 2b00 = 3 hour fast charge 2b01 = 6 hour fast charge 2b10 = 12 hour fast charge 2b11 = Disable safety timer |
| 1-0 | WATCHDOG_SEL_1:0 | R/W | 2b00 | Watchdog Selection 2b00 = 160s default register values 2b01 = 160s HW_RESET 2b10 = 40s HW_RESET 2b11 = Disable watchdog function |

7.5.1.9 TMR_ILIM Register (Offset = 0x8) [Reset = 0x4D]

TMR_ILIM is shown in [Figure 7-16](#) and described in [Table 7-17](#).

Return to the [Summary Table](#).

Figure 7-16. TMR_ILIM Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|---|------------------|--------------|---|-----------|---|---|
| MR_LPRESS_1:0 | | MR_RESET_VI N | AUTOWAKE_1:0 | | ILIM_2:0 | | |
| R/W-2b01 | | R/W-1b0 | R/W-2b01 | | R/W-3b101 | | |

Table 7-17. TMR_ILIM Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------|------|-------|---|
| 7-6 | MR_LPRESS_1:0 | R/W | 2b01 | Push button Long Press duration timer 2b00 = 5s 2b01 = 10s 2b10 = 15s 2b11 = 20s |
| 5 | MR_RESET_VIN | R/W | 1b0 | Hardware reset condition 1b0 = HW Resets are not gated by VIN_PowerGood 1b1 = HW Resets require VIN_PowerGood |
| 4-3 | AUTOWAKE_1:0 | R/W | 2b01 | Auto Wake Up Timer Restart 2b00 = 0.5s 2b01 = 1s 2b10 = 2s 2b11 = 4s |
| 2-0 | ILIM_2:0 | R/W | 3b101 | Input Current Limit Setting (max) 3b000 = 50mA 3b001 = 100mA 3b010 = 200mA 3b011 = 300mA 3b100 = 400mA 3b101 = 500mA 3b110 = 665mA 3b111 = 1050mA |

7.5.1.10 SHIP_RST Register (Offset = 0x9) [Reset = 0x11]

SHIP_RST is shown in [Figure 7-17](#) and described in [Table 7-18](#).

Return to the [Summary Table](#).

Figure 7-17. SHIP_RST Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-----------------|---|----------------------|---|-----------|-----------|---------|
| REG_RST | EN_RST_SHIP_1:0 | | PB_LPRESS_ACTION_1:0 | | WAKE1_TMR | WAKE2_TMR | EN_PUSH |
| R/W-1b0 | R/W-2b00 | | R/W-2b10 | | R/W-1b0 | R/W-1b0 | R/W-1b1 |

Table 7-18. SHIP_RST Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------------|------|-------|--|
| 7 | REG_RST | R/W | 1b0 | Software Reset 1b0 = Do nothing 1b1 = Software Reset |
| 6-5 | EN_RST_SHIP_1:0 | R/W | 2b00 | Ship mode Enable and Hardware Reset 2b00 = Do nothing 2b01 = Enable shutdown mode 2b10 = Enable ship mode 2b11 = Hardware Reset |
| 4-3 | PB_LPRESS_ACTION_1:0 | R/W | 2b10 | Pushbutton long press action 2b00 = Do nothing 2b01 = Hardware Reset 2b10 = Enable Ship mode. Ship mode can be exited by waking the device with a TSMR button press or adapter insertion 2b11 = Enable Shutdown Mode. Shutdown mode can be exited by an adapter insertion. |
| 2 | WAKE1_TMR | R/W | 1b0 | Wake 1 Timer Set 1b0 = 300ms 1b1 = 1s |
| 1 | WAKE2_TMR | R/W | 1b0 | Wake 2 Timer Set 1b0 = 2s 1b1 = 3s |
| 0 | EN_PUSH | R/W | 1b1 | Enable Push Button and Reset Functionality when in Active Battery 1b0 = Disable 1b1 = Enable |

7.5.1.11 SYS_REG Register (Offset = 0xA) [Reset = 0x42]

SYS_REG is shown in [Figure 7-18](#) and described in [Table 7-19](#).

Return to the [Summary Table](#).

Figure 7-18. SYS_REG Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------------|---|---|----------|--------------|---|-------------------------|-----------|
| SYS_REG_CTRL_2:0 | | | RESERVED | SYS_MODE_1:0 | | WATCHDOG_1 5S_ENABLE | VDPPM_DIS |
| R/W-3b010 | | | R/W-1b0 | R/W-2b00 | | R/W-1b0 | R/W-1b0 |

Table 7-19. SYS_REG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------------|------|-------|---|
| 7-5 | SYS_REG_CTRL_2:0 | R/W | 3b010 | SYS Regulation Voltage 3b000 = Battery Tracking Mode 3b001 = 4.4V 3b010 = 4.5V 3b011 = 4.6V 3b100 = 4.7V 3b101 = 4.8V 3b110 = 4.9V 3b111 = Pass-Through (if OVP is 5.7 V) or 5.5 V (if OVP is 18.5 V) |
| 4 | PG_GPO | R/W | 1b0 | Power Good Logic Level 1b0 = PG_GPO is high impedance 1b1 = PG_GPO is low |
| 3-2 | SYS_MODE_1:0 | R/W | 2b00 | Sets how SYS is powered in any state, except SHIPMODE 2b00 = SYS powered from VIN if present or VBAT (current def) 2b01 = SYS powered from VBAT only, even if VIN present 2b10 = SYS disconnected and left floating (VDD and digital are all still running. TSMR/ VIN would have to wake SYS) 2b11 = SYS disconnected with pulldown(VDD and digital are all still running. TSMR/VIN would have to wake SYS) |
| 1 | WATCHDOG_15S_ENABLE | R/W | 1b0 | I2C Watchdog 1b0 = Mode Disabled 1b1 = Do a HW reset after 15s if no I2C transaction after VIN plugged |
| 0 | VDPPM_DIS | R/W | 1b0 | Disable DPPM 1b0 = Enable DPPM 1b1 = Disable DPPM |

7.5.1.12 TS_CONTROL Register (Offset = 0xB) [Reset = 0x0]

TS_CONTROL is shown in [Figure 7-19](#) and described in [Table 7-20](#).

Return to the [Summary Table](#).

Figure 7-19. TS_CONTROL Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---|----------|---|---------|---------|---------|---------|
| TS_HOT | | TS_COLD | | TS_WARM | TS_COOL | TS_ICHG | TS_VRCG |
| R/W-2b00 | | R/W-2b00 | | R/W-1b0 | R/W-1b0 | R/W-1b0 | R/W-1b0 |

Table 7-20. TS_CONTROL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------|------|-------|--|
| 7-6 | TS_HOT | R/W | 2b00 | TS Hot threshold register 2b00 = Default 60C 2b01 = 65C 2b10 = 50C 2b11 = 45C |
| 5-4 | TS_COLD | R/W | 2b00 | TS Cold threshold register 2b00 = Default 0C 2b01 = 3C 2b10 = 5C 2b11 = -3C |
| 3 | TS_WARM | R/W | 1b0 | TS Warm threshold register TS Warm threshold (Easy to push with Rs, favor low) 1b0 = Default 45C 1b1 = Disabled |
| 2 | TS_COOL | R/W | 1b0 | TS Cool threshold register (Easy to push with Rp, favor high) 1b0 = Default 10C 1b1 = Disabled |
| 1 | TS_ICHG | R/W | 1b0 | Fast charge current when decreased by TS function 1b0 = 0.5*ICHG 1b1 = 0.2*ICHG |
| 0 | TS_VRCG | R/W | 1b0 | Reduced target battery voltage during Warm 1b0 = VBATREG -100mV 1b1 = VBATREG -200mV |

7.5.1.13 MASK_ID Register (Offset = 0xC) [Reset = 0x40]

MASK_ID is shown in [Figure 7-20](#) and described in [Table 7-21](#).

Return to the [Summary Table](#).

Figure 7-20. MASK_ID Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------|--------------|-------------|-----------|---|---|---|
| TS_INT_MASK | TREG_INT_MASK | BAT_INT_MASK | PG_INT_MASK | Device_ID | | | |
| R/W-1b0 | R/W-1b1 | R/W-1b0 | R/W-1b0 | R-4b0000 | | | |

Table 7-21. MASK_ID Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------|------|--------|---|
| 7 | TS_INT_MASK | R/W | 1b0 | MASK_TS 1b0 = Enable TS Interrupt 1b1 = Mask TS Interrupt |
| 6 | TREG_INT_MASK | R/W | 1b1 | MASK_TREG 1b0 = Enable TREG Interrupt 1b1 = Mask TREG Interrupt |
| 5 | BAT_INT_MASK | R/W | 1b0 | MASK_BATOCP_BUVLO 1b0 = Enable BOCP or BUVLO Interrupt 1b1 = Mask BOCP or BUVLO Interrupt |
| 4 | PG_INT_MASK | R/W | 1b0 | MASK_PG 1b0 = Enable PG and VINOVP Interrupt 1b1 = Mask PG and VINOVP Interrupt |
| 3-0 | Device_ID | R | 4b0100 | Device ID |

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

A typical application of the BQ21088 consists of the device configured as an I²C controlled single cell Li-ion battery charger and power path manager or battery applications such as smart-watches and wireless headsets. A battery thermistor may be connected to the TS pin to allow the device to monitor the battery temperature and control charging as desired.

The system designer may connect the TS/MR pin input to a push-button to send interrupts to the host as a button is pressed or to allow the application end user to reset the system.

8.2 Typical Application

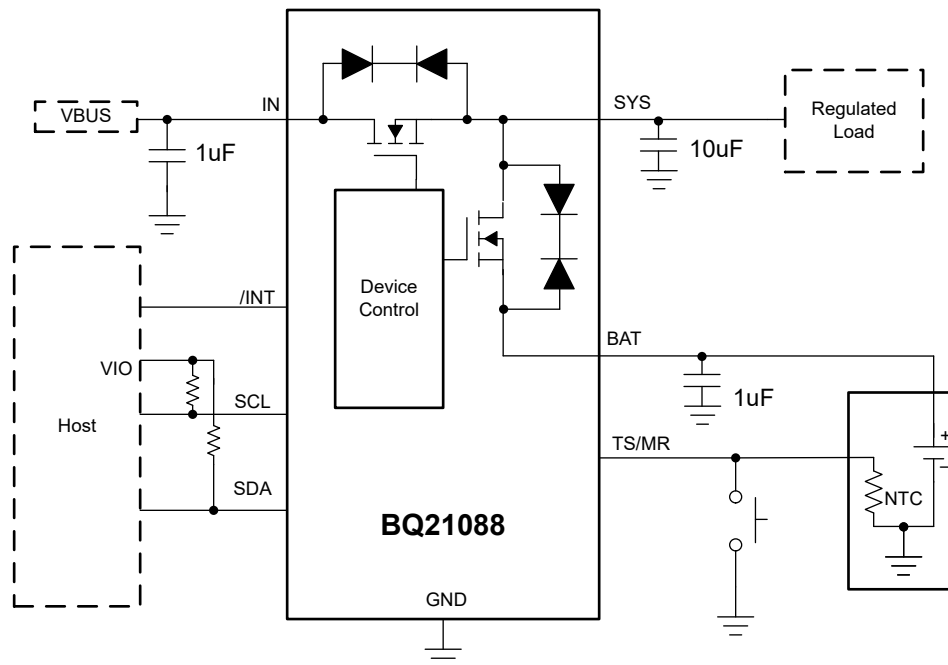


Figure 8-1. Typical Application

8.2.1 Application

8.2.2 Design Requirements

The design requirements for the following design example are shown in [Table 8-1](#).

Table 8-1. Design Parameters

| PARAMETER | VALUE |
|----------------------------|-------|
| IN Supply Voltage | 5 V |
| Battery Regulation Voltage | 4.2 V |

8.2.3 Detailed Design Procedure

Input (IN/SYS) Capacitors

Low ESR ceramic capacitors such as X7R or X5R are preferred for input decoupling capacitors and should be placed as close as possible to the supply and ground pins for the IC. Due to the voltage derating of the capacitors, it is recommended that 35-V rated capacitors are used for the IN pin. Higher IN voltages can cause significant decrease in effective capacitance due to DC Bias derating. For output stability, it is important that the minimum capacitance after derating be higher than 1 μF for the operating input voltage.

TS

The ground connection for the NTC must be made as close as possible to the GND pin of the device or kelvin connected to it to minimize any error in TS measurement due to IR drops on the ground board lines.

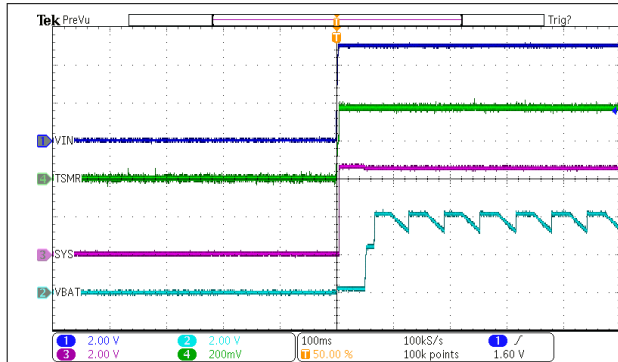
If the system designer does not wish to use the TS function for charging control, a 10-k Ω resistor must be connected from TS to ground.

Recommended Passive Components

| PARAMETER | | MIN | NOM | MAX | UNIT |
|------------------|--|-----|-----|-----|---------------|
| C _{SYS} | Capacitance on SYS pin | 1 | 10 | 100 | μF |
| C _{BAT} | Capacitance on BAT pin | 1 | 1 | - | μF |
| C _{IN} | IN input bypass capacitance (After DC Bias Derating) | 1 | 1 | 10 | μF |

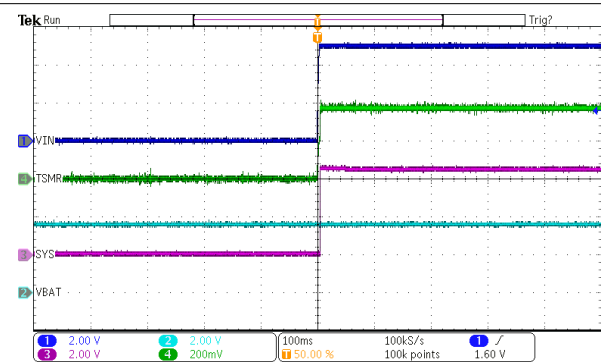
8.2.4 Application Curves

$C_{IN} = 1 \mu\text{F}$, $C_{OUT} = 10 \mu\text{F}$, $V_{IN} = 5 \text{ V}$, $V_{OUT} = 3.8 \text{ V}$, $I_{CHG} = 10 \text{ mA}$ (unless otherwise specified)



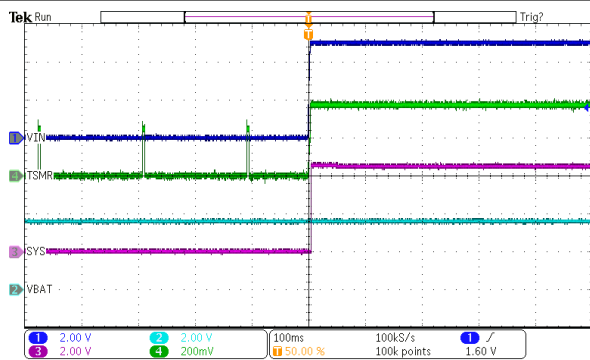
VIN = 5 V VBAT = Floating

Figure 8-2. Power Up with IN Supply Insertion with No Battery



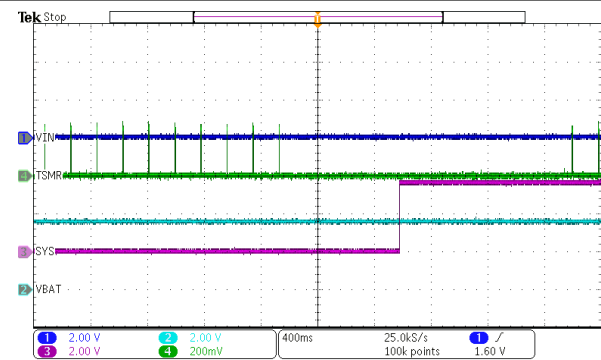
VIN = 5 V VBAT = 3.6 V

Figure 8-3. Power Up from Shutdown Mode with VIN Supply Insertion



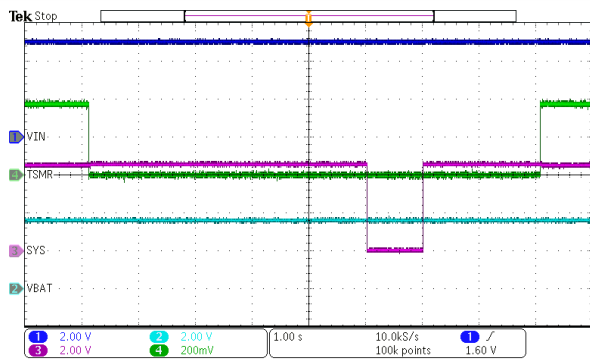
VIN = 0 V → 5 V VBAT = 3.8 V

Figure 8-4. Power Up from Shipmode with VIN Insertion



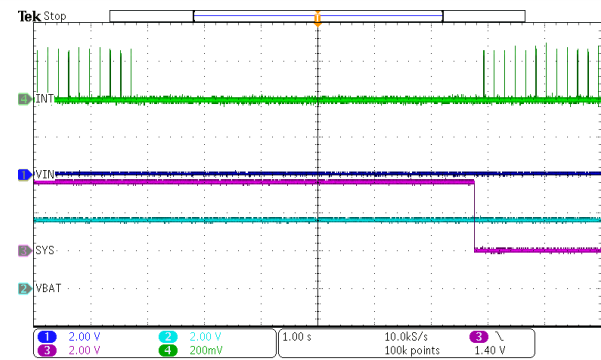
MR_LPRESS = 00 (5s Long Press Timer)

Figure 8-5. Power Up from Shipmode with /TSMR Button Press



MR_LPRESS = 00 (5s Long Press Timer)
 PB_LPRESS_ACTION = 01 (Hardware Reset)

Figure 8-6. Hardware Reset with /TSMR Press



MR_LPRESS = 00 (5s Long Press Timer)
 PB_LPRESS_ACTION = 10

Figure 8-7. Enter Shipmode with Push Button Long Press

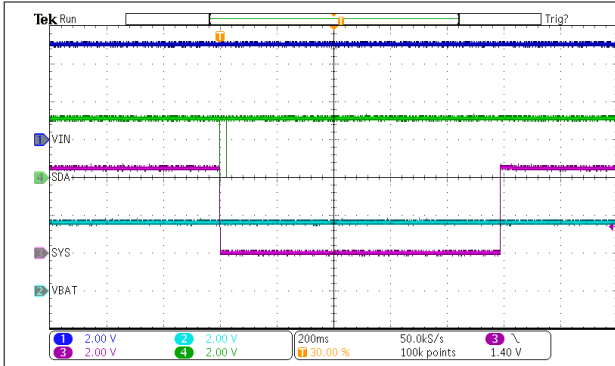
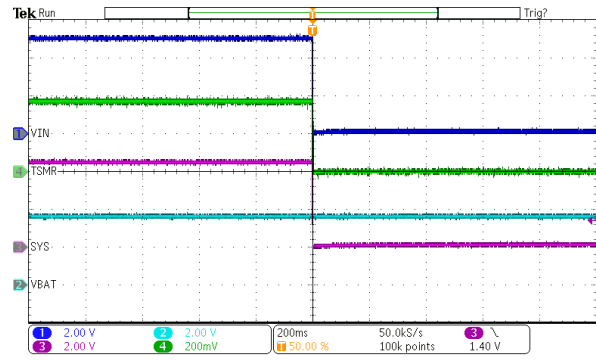
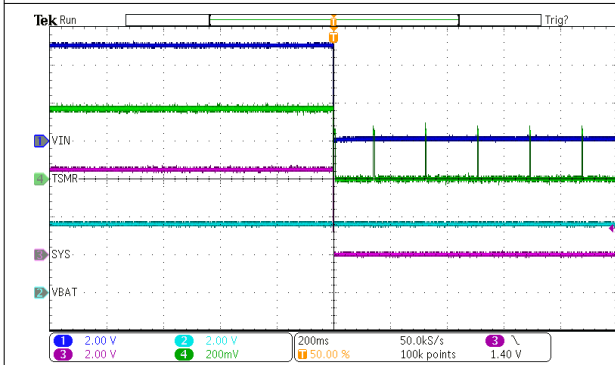


Figure 8-8. Hardware Reset Through I²C



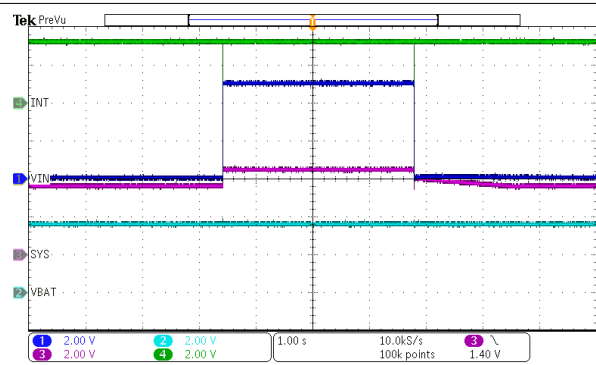
EN_RST_SHIP = 01 (enable shutdown with wake on adapter insert only)

Figure 8-9. Shutdown Entry on VIN Removal



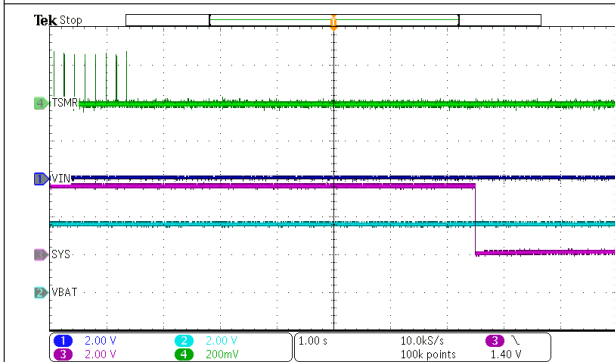
EN_RST_SHIP = 10 (enable shutdown with wake on adapter insert only)

Figure 8-10. Shipmode Entry on VIN Removal



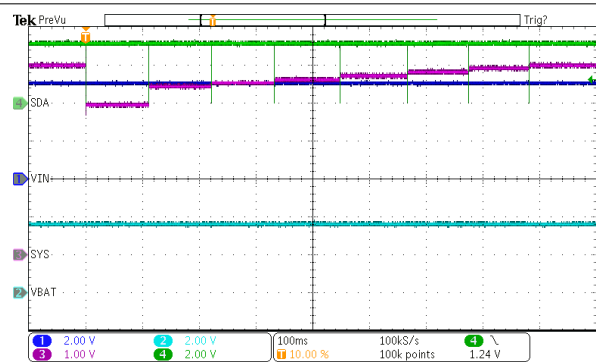
V_{IN} = 0 V → 5 V → 0 V

Figure 8-11. Power Good Interrupt on /INT



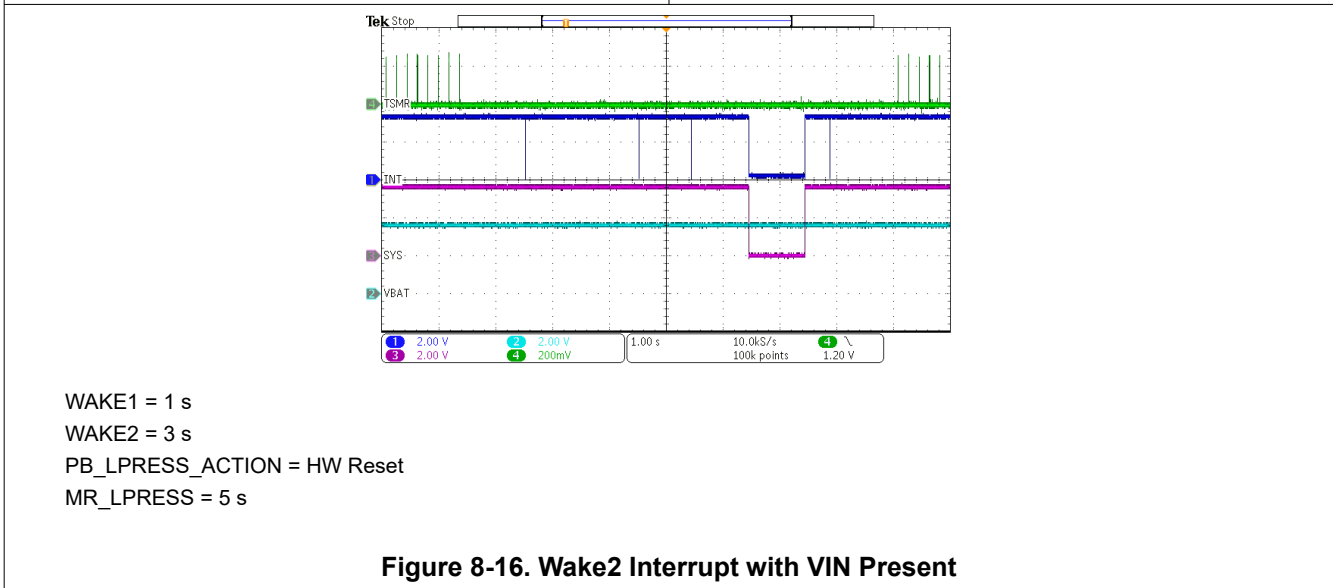
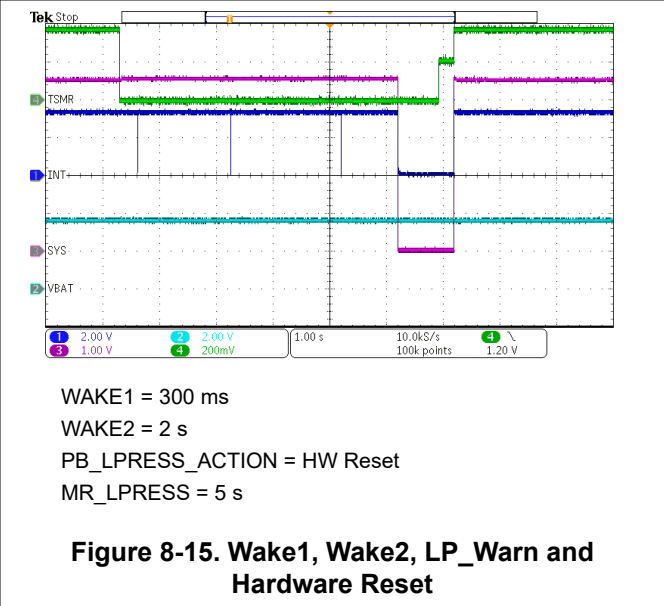
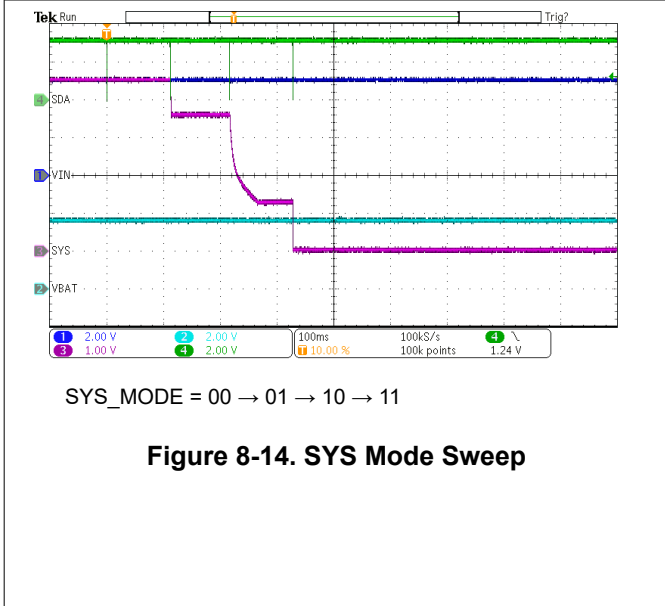
V_{IN} = 0 V
PB_LPRESS_ACTION = 11 (enable shutown mode)
MR_LPRESS = 00 (5 seconds)

Figure 8-12. Shutdown Mode Entry with Push Button Long Press



SYS_REG_CTRL = 000 → 111 in steps

Figure 8-13. SYS Regulation Sweep



9 Power Supply Recommendations

The BQ21088 requires the adapter or IN supply to be between 3.3 V and 5.5 V. The battery voltage must be higher than 3.15 V or $V_{BATUVLO}$ to ensure proper operation. Higher input voltages result in higher input dissipation.

10 Layout

10.1 Layout Guidelines

- To obtain optimal performance, the decoupling capacitor from IN to GND, the capacitor from SYS to GND, and the BAT to GND capacitor should be placed as close as possible to the device.
- A solid ground plane should be used that is tied to the GND pin and thermal pad
- The pushbutton GND should be connected as close to the device as possible
- The high current charge paths into IN, SYS, and BAT must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces

10.2 Layout Example

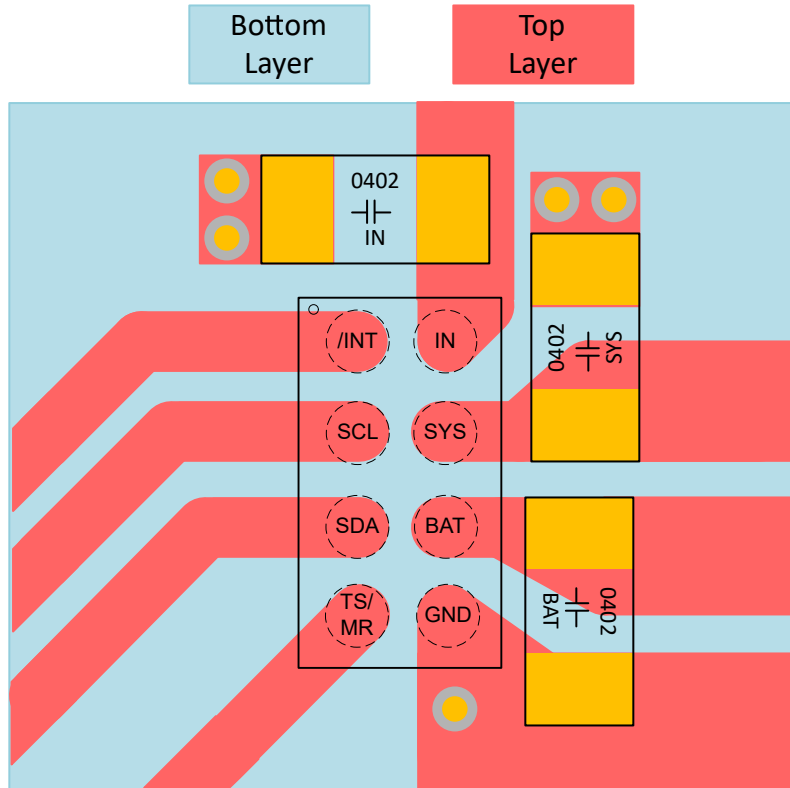


Figure 10-1. Board Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Documentation Support

11.2.1 Related Documentation

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

12 Revision History

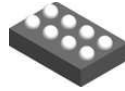
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE | REVISION | NOTES |
|---------------|----------|-----------------|
| November 2024 | * | Initial Release |

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

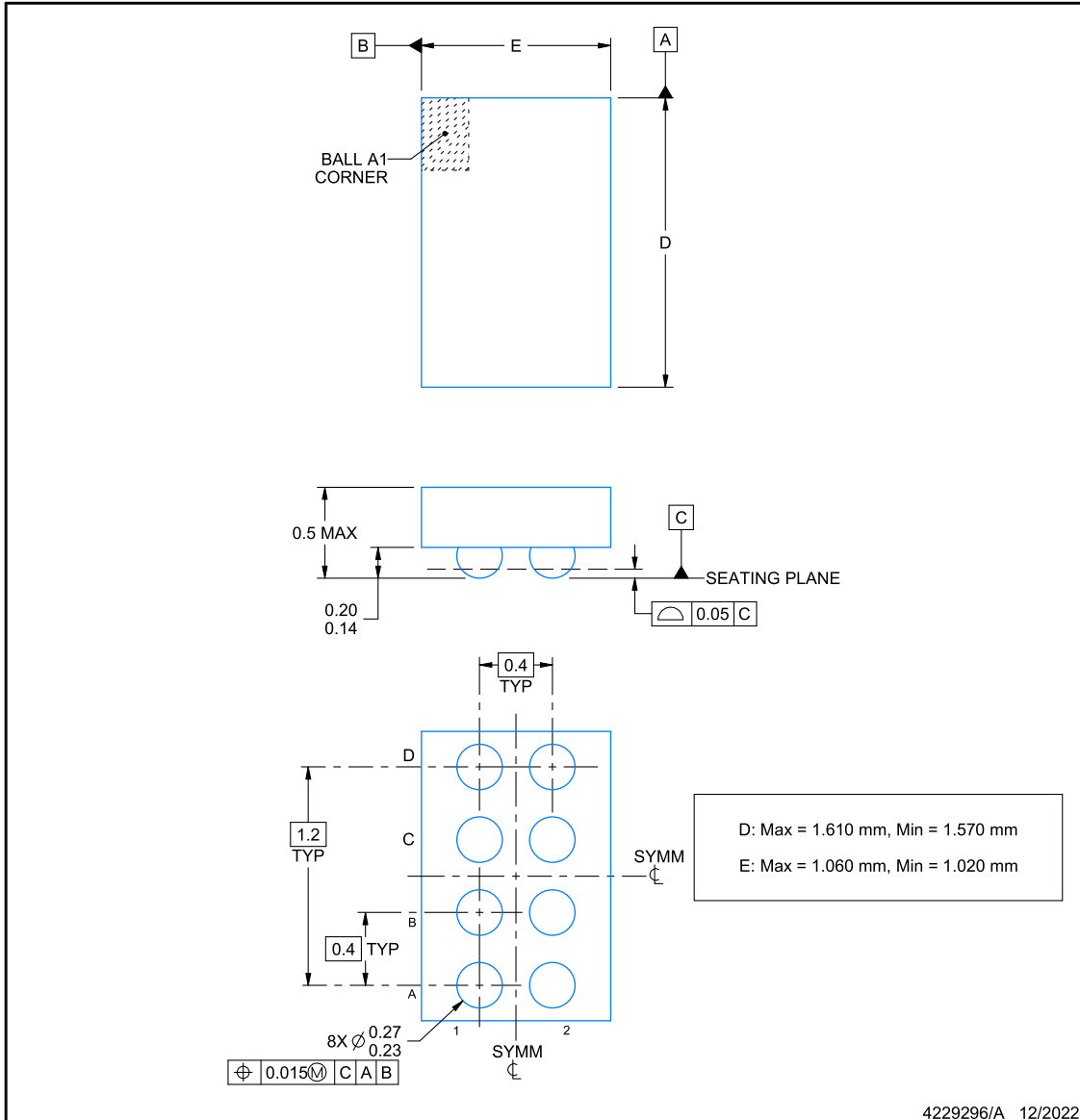
13.1 Mechanical Data



YBG0008-C01

PACKAGE OUTLINE
DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

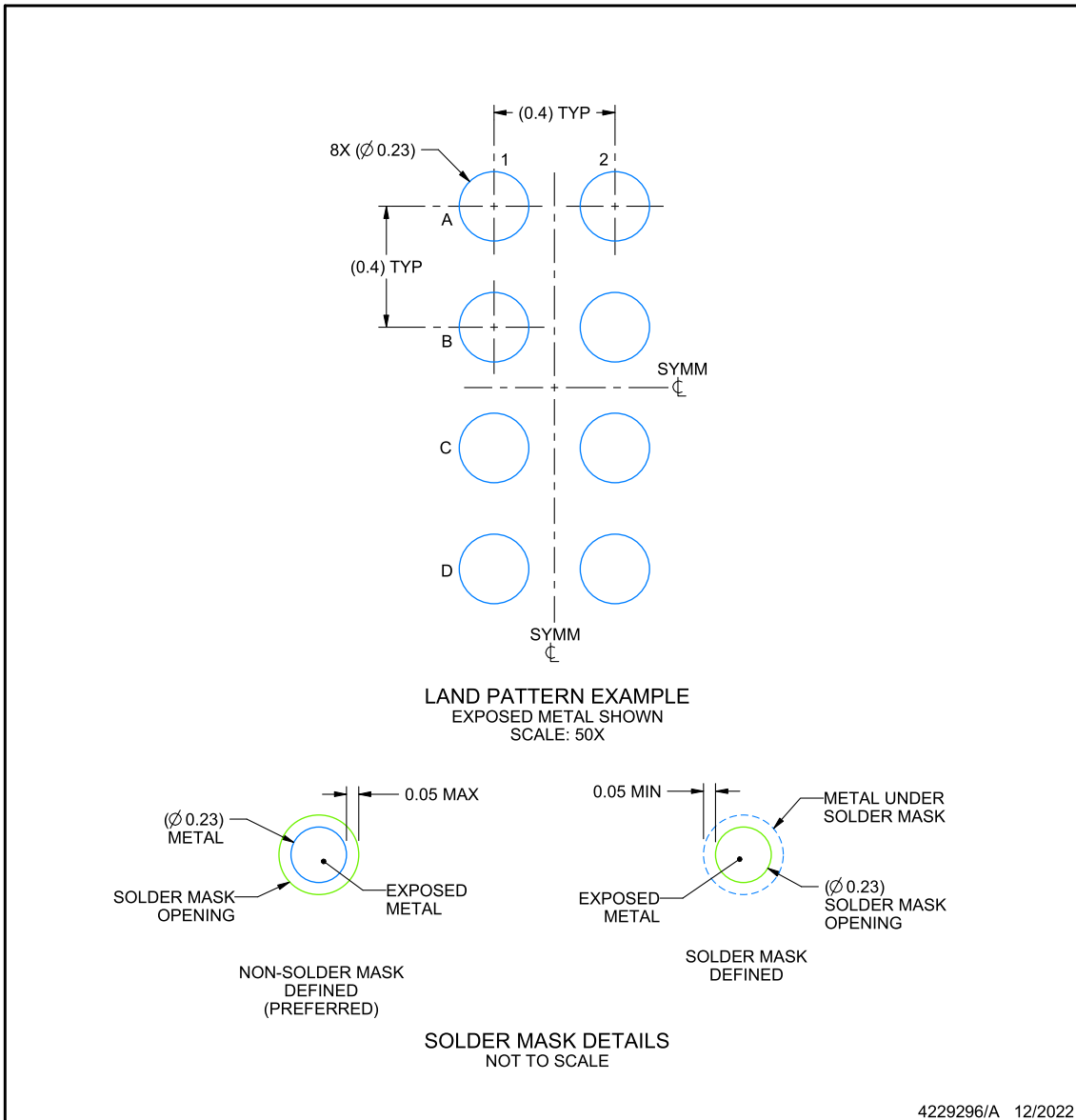
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

YBG0008-C01

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES: (continued)

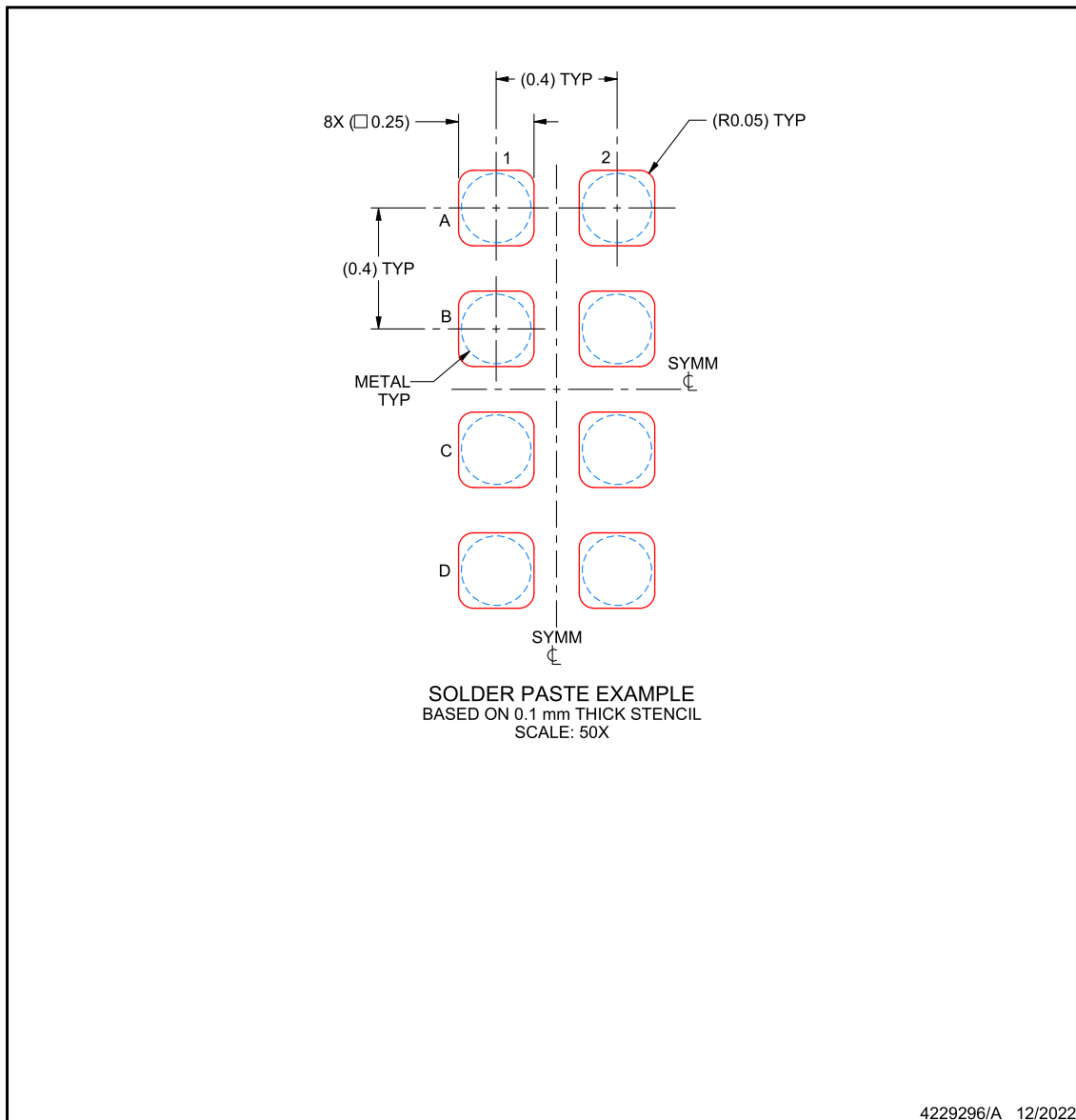
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YBG0008-C01

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-----------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| BQ21088YBGR | Active | Production | DSBGA (YBG) 8 | 3000 LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | B088 |
| BQ21088YBGR.A | Active | Production | DSBGA (YBG) 8 | 3000 LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | B088 |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

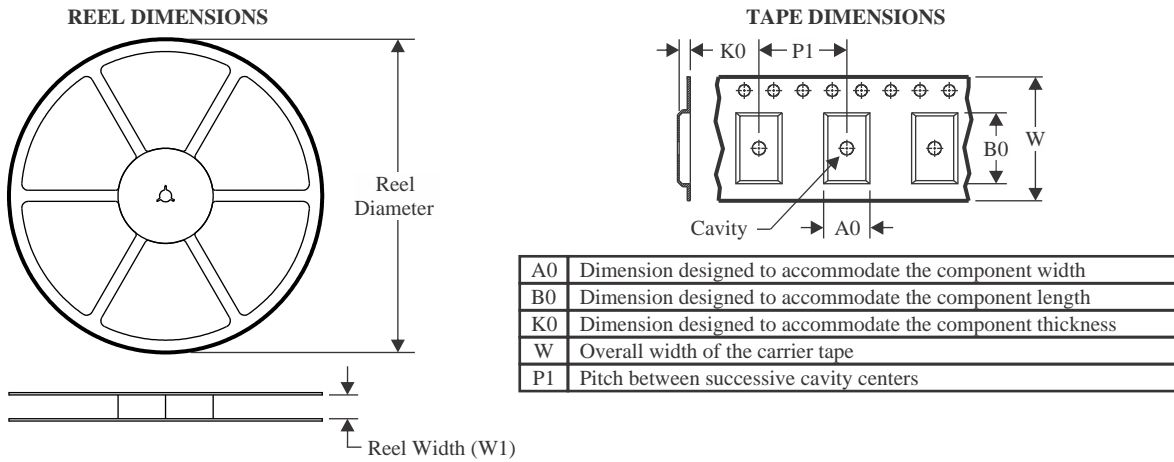
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| BQ21088YBGR | DSBGA | YBG | 8 | 3000 | 180.0 | 8.4 | 1.15 | 1.75 | 0.65 | 4.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| BQ21088YBGR | DSBGA | YBG | 8 | 3000 | 182.0 | 182.0 | 20.0 |

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Last updated 10/2025