bq25100B 250-mA Single Cell Li-Ion Battery Chargers, 1-mA Termination, 75-nA Battery Leakage

1 Features

- Charging
  - 1% Charge Voltage Accuracy
  - 10% Charge Current Accuracy
  - Supports Applications for Very Low Charge Currents - 10 mA to 250 mA
  - Supports Minimum 1-mA Charge Termination Current
  - Ultra Low Battery Output Leakage Current - Maximum 75 nA
  - Adjustable Termination and Precharge Threshold
  - High voltage Chemistry Support: 4.30 V
- Protection
  - 30-V Input Rating; with 6.5-V Input Overvoltage Protection
  - Input Voltage Dynamic Power Management
  - 125°C Thermal Regulation; 150°C Thermal Shutdown Protection
  - OUT Short-Circuit Protection and ISET Short Detection
  - Fixed 10 Hour Safety Timer
- System
  - Automatic Termination and Timer Disable Mode (TTDM) for Absent Battery Pack
  - Available in Small 1.60 mm × 0.90 mm DSBGA Package

2 Applications

- Fitness Accessories
- Smart Watches
- Bluetooth® Headsets
- Low-Power Handheld Devices

3 Description

The bq25100B device is a highly integrated Li-Ion and Li-Pol linear charger targeted at space-limited portable applications. The high input voltage range with input overvoltage protection supports low-cost unregulated adapters.

The bq25100B has a single power output that charges the battery. A system load can be placed in parallel with the battery as long as the average system load does not keep the battery from charging fully during the 10 hour safety timer.

The battery is charged in three phases: conditioning, constant current and constant voltage. In all charge phases, an internal control loop monitors the IC junction temperature and reduces the charge current if an internal temperature threshold is exceeded.

The charger power stage and charge current sense functions are fully integrated. The charger function has high accuracy current and voltage regulation loops and charge termination. The pre-charge current and termination current threshold are programmed via an external resistor on the bq25100B. The fast charge current value is also programmable via an external resistor.

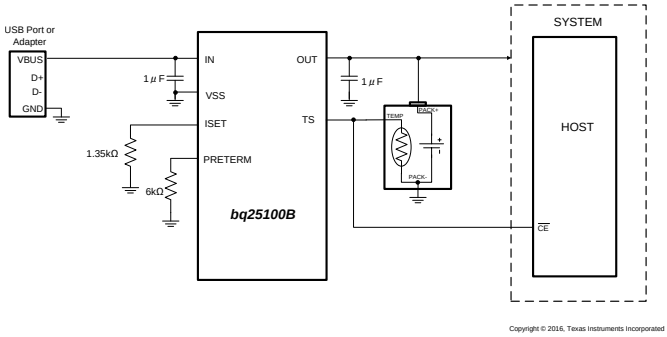
References to other devices in the bq25100B family are included in this document. For more information on those devices, please see their respective datasheets. This includes references to the $\overline{CHG}$ pin and the JEITA temperature functionality.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
bq25100B	DSBGA (6)	1.60 mm × 0.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Diagram



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4 Revision History

Changes from Original (May 2016) to Revision A **Page**

- Changed $I_{OUT(SC)}$ values From: 9, 11, 13 To: 10, 12, 14 in the *Electrical Characteristics* table ... 5
- Changed $I_{PRE-TERM}$ values From: 23, 25, 27 To: 24.25, 26.25, 28.25 in the *Electrical Characteristics* table ... 6
- Changed the $I_{NTC-10k}$ values From: 48.5, 50.5, 52.5 To: 50.5, 52.5, 54.5 in the *Electrical Characteristics* table ... 7
- Changed the $I_{NTC-DIS-10k}$ values From: 27, 30, 33 To: 28, 31, 34 in the *Electrical Characteristics* table ... 7
- Changed the $V_{TS-0°C}$ values From: 1230, 1255, 1280 To: 1225, 1250, 1275 in the *Electrical Characteristics* table ... 7
- Changed the $V_{TS-45°C}$ values From: 253, 268, 283 To: 255, 267, 279 in the *Electrical Characteristics* table ... 7
- Changed the $V_{TS-EN-10k}$ values From: 84, 92, 100 To: 83, 91, 99 in the *Electrical Characteristics* table ... 8

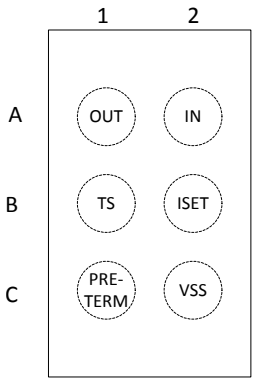
5 Device Comparison Table

PART NUMBER	$V_{O(REG)}$	V_{OVP}	PreTerm $\overline{CHG}$	TS
bq25100	4.20 V	6.5 V	PreTerm	TS (JEITA)
bq25101	4.20 V	6.5 V	$\overline{CHG}$	TS (JEITA)
bq25100A	4.30 V	6.5 V	PreTerm	TS
bq25100B (1)	4.284 V	6.5 V	PreTerm	TS
bq25100H	4.35 V	6.5 V	PreTerm	TS (JEITA)
bq25101H	4.35 V	6.5 V	$\overline{CHG}$	TS (JEITA)
bq25100L (2)	4.06 V	6.5 V	PreTerm	TS

(1) The bq25100B is part of the bq25100 family of devices. Please see *Device Support* for viewing other devices.
(2) Product preview. Contact the local TI representative for device details.

6 Pin Configuration and Functions

YFP Package
6-Pin DSBGA
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NUMBER		
IN	A2	I	Input power, connected to external DC supply (AC adapter or USB port). Expected range of bypass capacitors 1 μF to 10 μF, connect from IN to V_{SS}.
ISET	B2	I	Programs the fast-charge current setting. External resistor from ISET to VSS defines fast charge current value. Recommended range is 13.5 kΩ (10 mA) to 0.54 kΩ (250 mA).
OUT	A1	O	Battery Connection. System Load may be connected. Expected range of bypass capacitors 1 μF to 10 μF.
PRE-TERM	C1	I	Programs the current termination threshold (1% to 50% of I_{OUT}, 1 mA minimum). The pre-charge current is twice the termination current level. Expected range of programming resistor is 600 Ω to 30 kΩ (6k: I_{CHG}/10 for term; I_{CHG}/5 for precharge)
TS	B1	I	Temperature sense pin connected to 10k at 25°C NTC thermistor, in the battery pack. Floating TS pin or pulling high puts part in TTDM *Charger* mode and disables TS monitoring, Timers and Termination. Pulling pin low disables the IC. If NTC sensing is not needed, connect this pin to VSS through an external 10-kΩ resistor. A 250-kΩ resistor from TS to ground will prevent IC entering TTDM mode when battery with thermistor is removed.
VSS	C2	–	Ground pin

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
	Input voltage	IN (with respect to VSS)	–0.3	30	V
		OUT (with respect to VSS)	–0.3	7	V
		PRE-TERM, ISET, TS, $\overline{CHG}$ (with respect to VSS)	–0.3	7	V
	Input current	IN		300	mA
	Output current (continuous)	OUT		300	mA
	Output sink current	$\overline{CHG}$		15	mA
T_J	Junction temperature		–40	150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC61000-4-2 contact discharge(1)	Pins A1, A2, B1(2)	±8000	V
		IEC61000-4-2 air-gap discharge(1)	Pins A1, A2, B1(2)	±15000	

(1) The test was performed on IC pins that may potentially be exposed to the customer at the product level. The bq2510x IC requires a minimum of the listed capacitance, external to the IC, to pass the ESD test.
(2) 1 µF between IN (pin A2) and GND,
1 µF between TS (pin B1) and GND,
2 µF between OUT (pin A1) and GND,
x5R ceramic or equivalent

7.3 Recommended Operating Conditions

see (1)

		MIN	NOM	UNIT
V_{IN}	IN voltage	3.5	28	V
	IN operating voltage, restricted by V_{DPM} and V_{OVP}	4.45	6.45	V
I_{IN}	Input current, IN pin		250	mA
I_{OUT}	Current, OUT pin		250	mA
$R_{PRE-TERM}$	Programs precharge and termination current thresholds	0.6	30	kΩ
R_{ISET}	Fast-charge current programming resistor	0.54	13.5	kΩ
R_{TS}	10k NTC thermistor range without entering $\overline{BAT\_EN}$ or TTDM	1.66	258	kΩ
T_J	Junction temperature	–5	125	°C

(1) Operation with V_{IN} less than 4.5V or in drop-out may result in reduced performance.

7.4 Thermal Information

THERMAL METRIC[1]		bq25100B YFP (DSBGA) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	132.9	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	1.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	21.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	21.8	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

Over junction temperature range –5°C ≤ T_J ≤ 125°C and recommended supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
UVLO	Undervoltage lockout exit	V_{IN}: 0 V → 4 V	3.15	3.3	3.45	V
V_{HYS_UVLO}	Hysteresis on V_{UVLO_RISE} falling	V_{IN}: 4 V→0 V; $V_{UVLO\_FALL} = V_{UVLO\_RISE} – V_{HYS-UVLO}$		263		mV
V_{IN-DT}	Input power good detection threshold is $V_{OUT} + V_{IN-DT}$	Input power good if $V_{IN} > V_{OUT} + V_{IN-DT}$; V_{OUT} = 3.6 V; V_{IN}: 3.5 V → 4 V	15	60	130	mV
$V_{HYS-INDT}$	Hysteresis on V_{IN-DT} falling	V_{OUT} = 3.6 V; V_{IN}: 4 V → 3.5 V		31		mV
$t_{DGL(PG\_PWR)}$	Deglitch time on exiting sleep	Time measured from V_{IN}: 0 V → 5 V 1-µs rise-time to charge enables; V_{OUT} = 3.6 V		29		ms
$t_{DGL(PG\_NO-PWR)}$	Deglitch time on $V_{HYS-INDT}$ power down. Same as entering sleep.	Time measured from V_{IN}: 5 V → 3.2 V 1-µs fall-time to charge disables; V_{OUT} = 3.6 V		29		ms
V_{OVP}	Input over-voltage protection threshold	V_{IN}: 5 V → 12 V	6.50	6.65	6.84	V
$t_{DGL(OVP-SET)}$	Input over-voltage blanking time	V_{IN}: 5 V → 12 V		113		µs
$V_{HYS-OVP}$	Hysteresis on OVP	V_{IN}: 11 V → 5 V		110		mV
$t_{DGL(OVP-REC)}$	Deglitch time exiting OVP	Time measured from V_{IN}: 12 V → 5 V 1-µs fall-time to charge enables		450		µs
V_{IN-DPM}	Low input voltage protection. Restricts Iout at V_{IN-DPM}	Limit input source current to 50 mA; V_{OUT} = 3.5 V; R_{ISET} = 1.35 kΩ	4.25	4.31	4.37	V
ISET SHORT CIRCUIT TEST						
R_{ISET_SHORT}	Highest resistor value considered a fault (short).	R_{ISET}: 540 Ω → 250 Ω, Iout latches off; Cycle power to reset		426	470	Ω
t_{DGL_SHORT}	Deglitch time transition from ISET short to Iout disable	Clear fault by disconnecting IN or cycling (high / low) TS/$\overline{BAT\_EN}$		1		ms
I_{OUT_CL}	Maximum OUT current limit regulation (Clamp)	V_{IN} = 5 V; V_{OUT} = 3.6 V; R_{ISET}: 540 Ω → 250 Ω; I_{OUT} latches off after $t_{DGL-SHORT}$	550	600	650	mA
BATTERY SHORT PROTECTION						
$V_{OUT(SC)}$	OUT pin short-circuit detection threshold/ precharge threshold	V_{OUT}:3 V → 0.5 V; No deglitch	0.75	0.8	0.85	V
$V_{OUT(SC-HYS)}$	OUT pin Short hysteresis	Recovery ≥ $V_{OUT(SC)} + V_{OUT(SC-HYS)}$; Rising; No deglitch		77		mV
$I_{OUT(SC)}$	Source current to OUT pin during short-circuit detection		10	12	14	mA
QUIESCENT CURRENT						
$I_{OUT(PDWN)}$	Battery current into OUT pin	V_{IN} = 0 V; 0°C to 125°C			80	nA
		V_{IN} = 0 V; 0°C to 85°C			50	
$I_{OUT(DONE)}$	OUT pin current, charging terminated	V_{IN} = 6 V; $V_{OUT} > V_{OUT(REG)}$			6	µA
$I_{IN(STDBY)}$	Standby current into IN pin	TS = GND; V_{IN} ≤ 6 V			125	µA
I_{CC}	Active supply current, IN pin	TS = open, V_{IN} = 6 V; TTDM – no load on OUT pin; $V_{OUT} > V_{OUT(REG)}$; IC enabled		0.75	1	mA

Electrical Characteristics (continued)

Over junction temperature range –5°C ≤ T_J ≤ 125°C and recommended supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BATTERY CHARGER FAST-CHARGE						
$V_{OUT(REG)}$	Output voltage	T_J = -5°C to 125°C; I_{OUT} = 0 mA to 250 mA; V_{IN} = 5.0 V; $V_{TS-45°C} \le V_{TS} \le V_{TS-0°C}$ (bq25100B)	4.25	4.284	4.305	V
		T_J = -5°C to 55°C; I_{OUT} = 10mA to 75 mA; V_{IN} = 5.0 V; $V_{TS-45°C} \le V_{TS} \le V_{TS-0°C}$ (bq25100B)	4.266	4.284	4.305	
$I_{OUT(RANGE)}$	Programmed output “fast charge” current range	$V_{OUT(REG)} > V_{OUT} > V_{LOWV}$; V_{IN} = 5 V; R_{ISET} = 0.54 kΩ to 13.5 kΩ	10		250	mA
$V_{DO(IN-OUT)}$	Drop-Out, VIN – VOUT	Adjust V_{IN} down until I_{OUT} = 0.2 A; V_{OUT} = 4.15 V; R_{ISET} = 680 Ω; T_J ≤ 100°C		240	400	mV
I_{OUT}	Output “fast charge” formula	$V_{OUT(REG)} > V_{OUT} > V_{LOWV}$; V_{IN} = 5 V		K_{ISET}/R_{ISET}		A
K_{ISET}	Fast charge current factor	$R_{ISET} = K_{ISET} / I_{OUT}$; 20 < I_{OUT} < 250 mA	129	135	145	AΩ
		$R_{ISET} = K_{ISET} / I_{OUT}$; 5 < I_{OUT} < 20 mA	125	135	145	
PRECHARGE – SET BY PRETERM PIN						
V_{LOWV}	Pre-charge to fast-charge transition threshold		2.4	2.5	2.6	V
$t_{DGL1(LOWV)}$	Deglitch time on pre-charge to fast-charge transition			57		µs
$t_{DGL2(LOWV)}$	Deglitch time on fast-charge to pre-charge transition			32		ms
$I_{PRE-TERM}$	Refer to the Termination Section					
$\%_{PRECHG}$	Pre-charge current, default setting	$V_{OUT} < V_{LOWV}$; R_{ISET} = 2.7 kΩ; $R_{PRE-TERM}$= High Z or for bq25101/101H	18	20	22	$\%I_{OUT-CC}$
	Pre-charge current formula	$R_{PRE-TERM} = K_{PRE-CHG}$ (Ω/%) × $\%_{PRE-CHG}$ (%)		$R_{PRE-TERM}/K_{PRE-CHG\%}$		
$K_{PRE-CHG}$	% Pre-charge Factor	$V_{OUT} < V_{LOWV}$; V_{IN} = 5 V; $R_{PRE-TERM}$ = 6 kΩ to 30 kΩ; R_{ISET} = 1.8 kΩ; $R_{PRE-TERM} = K_{PRE-CHG} \times \%I_{PRE-CHG}$, where $\%I_{PRE-CHG}$ is 20 to 100%	280	300	320	Ω/%
		$V_{OUT} < V_{LOWV}$; V_{IN} = 5 V; $R_{PRE-TERM}$ = 3 kΩ to 6 kΩ; R_{ISET} = 1.8 kΩ; $R_{PRE-TERM} = K_{PRE-CHG} \times \%I_{PRE-CHG}$, where $\%I_{PRE-CHG}$ is 10% to 20%	265	305	347	Ω/%
TERMINATION – SET BY PRE-TERM PIN						
$\%_{TERM}$	Termination threshold current, default setting	$V_{OUT} > V_{RCH}$; R_{ISET} = 2.7 kΩ; $R_{PRE-TERM}$ = High Z or for bq25101/101H	9	10	11	$\%I_{OUT-CC}$
	Termination current threshold formula	$R_{PRE-TERM} = K_{TERM}$ (Ω/%) × %TERM (%)		$R_{PRE-TERM}/ K_{TERM}$		
K_{TERM}	% Term factor	$V_{OUT} > V_{RCH}$; V_{IN} = 5 V; $R_{PRE-TERM}$ = 6 kΩ to 30 kΩ; R_{ISET} = 1.8 kΩ, $R_{PRE-TERM} = K_{TERM} \times \%I_{TERM}$, where $\%I_{TERM}$ is 10 to 50%	575	600	640	Ω/%
		$V_{OUT} > V_{RCH}$; V_{IN} = 5 V; $R_{PRE-TERM}$ = 3 kΩ to 6 kΩ ; R_{ISET} = 1.8 kΩ, $R_{PRE-TERM} = K_{TERM} \times \%I_{TERM}$, where $\%I_{TERM}$ is 5 to 10%	555	620	685	
		$V_{OUT} > V_{RCH}$; V_{IN} = 5 V; $R_{PRE-TERM}$ = 750 Ω to 3 kΩ; R_{ISET} = 1.8 kΩ, $R_{PRE-TERM} = K_{TERM} \times \%I_{TERM}$, where $\%I_{TERM}$ is 1.25% to 5%	352	680	1001	
$I_{PRE-TERM}$	Current for programming the term. and pre-chg with resistor, $I_{Term-Start}$ is the initial PRE-TERM current	$R_{PRE-TERM}$ = 6 kΩ; V_{OUT} = 4.15 V	24.25	26.25	28.25	µA
ITERM	Termination current range	Minimum absolute termination current	1			mA
%TERM	Termination current formula			R_{TERM}/ K_{TERM}		%
$t_{DGL(TERM)}$	Deglitch time, termination detected			29		ms

Electrical Characteristics (continued)

Over junction temperature range –5°C ≤ T_J ≤ 125°C and recommended supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RECHARGE OR REFRESH						
V_{RCH}	Recharge detection threshold – normal temp	V_{IN} = 5 V; V_{TS} = 0.5 V; V_{OUT}: 4.35 V → V_{RCH}	$V_{O(REG)}$ –0.125	$V_{O(REG)}$ –0.101	$V_{O(REG)}$ –0.075	V
$t_{DGL1(RCH)}$	Deglitch time, recharge threshold detected	V_{IN} = 5 V; V_{TS} = 0.5 V; V_{OUT}: 4.25 V → 3.5V in 1 µs; $t_{DGL(RCH)}$ is time to ISET ramp		29		ms
$t_{DGL2(RCH)}$	Deglitch time, recharge threshold detected in OUT-Detect Mode	V_{IN} = 5 V; V_{TS} = 0.5 V; V_{OUT} = 3.5 V inserted; $t_{DGL(RCH)}$ is time to ISET ramp		29		ms
BATTERY DETECT ROUTINE – (NOTE: In Hot mode $V_{O(REG)}$ becomes $V_{O\_HT(REG)}$)						
V_{REG-BD}	VOUT reduced regulation during battery detect	V_{IN} = 5 V; V_{TS} = 0.5 V; Battery absent	$V_{O(REG)}$- 0.550	$V_{O(REG)}$- 0.500	$V_{O(REG)}$- 0.450	V
$I_{BD-SINK}$	Sink current during V_{REG-BD}	V_{IN} = 5 V; V_{TS} = 0.5 V; Battery absent		2		mA
$t_{DGL(HI/LOW\ REG)}$	Regulation time at V_{REG} or V_{REG-BD}	V_{IN} = 5 V; V_{TS} = 0.5 V; Battery absent		25		ms
V_{BD-HI}	High battery detection threshold	V_{IN} = 5 V; V_{TS} = 0.5 V; Battery absent	$V_{O(REG)}$ - 0.150	$V_{O(REG)}$- 0.100	$V_{O(REG)}$- 0.050	V
V_{BD-LO}	Low battery detection threshold	V_{IN} = 5 V; V_{TS} = 0.5 V; Battery absent	V_{REG-BD} +0.05	V_{REG-BD} +0.1	V_{REG-BD} +0.15	V
BATTERY CHARGING TIMERS AND FAULT TIMERS						
t_{PRECHG}	Pre-charge safety timer value	Restarts when entering pre-charge; Always enabled when in pre-charge.	1700	1940	2250	s
t_{MAXCH}	Charge safety timer value	Clears fault or resets at UVLO, TS disable, OUT Short, exiting LOWV and Refresh	34000	38800	45000	s
BATTERY-PACK NTC MONITOR (see (1)); TS pin: 10k NTC						
$I_{NTC-10k}$	NTC bias current	V_{TS} = 0.3 V	50.5	52.5	54.5	µA
$I_{NTC-DIS-10k}$	10k NTC bias current when charging is disabled	V_{TS} = 0 V	28	31	34	µA
$I_{NTC-FLDBK-10k}$	INTC is reduced prior to entering TTDM to keep cold thermistor from entering TTDM	V_{TS}: Set to 1.525 V	4	5	6.5	µA
$V_{TTDM(TS)}$	Termination and timer disable mode Threshold – Enter	V_{TS}: 0.5 V → 1.7 V; Timer held in reset	1550	1600	1650	mV
$V_{HYS-TTDM(TS)}$	Hysteresis exiting TTDM	V_{TS}: 1.7 V → 0.5 V; Timer enabled		100		mV
$V_{CLAMP(TS)}$	TS maximum voltage clamp	V_{TS} = Open (float)	1900	1950	2000	mV
$t_{DGL(TTDM)}$	Deglitch exit TTDM between states			57		ms
	Deglitch enter TTDM between states			8		µs
$V_{TS\_I-FLDBK}$	TS voltage where INTC is reduce to keep thermistor from entering TTDM	INTC adjustment (90 to 10%; 45 to 6.6 uA) takes place near this spec threshold; V_{TS}: 1.425 V → 1.525 V		1475		mV
C_{TS}	Optional capacitance – ESD			0.22		µF
$V_{TS-0°C}$	Low temperature, charge pending	Low temperature charging to pending; V_{TS}: 1 V → 1.5 V	1225	1250	1275	mV
$V_{HYS-0°C}$	Hysteresis	At 0°C; Charge pending to low temperature charging; V_{TS}: 1.5 V → 1 V		100		mV
$V_{TS-10°C}$	Low temperature, half charge	Normal charging to low temperature charging; V_{TS}: 0.5 V → 1 V	775	800	830	mV
$V_{HYS-10°C}$	Hysteresis	At 10°C; Low temperature charging to normal charging; V_{TS}: 1 V → 0.5 V		55		mV
$V_{TS-45°C}$	High temperature	At 4.1V (bq25100/101) or 4.2V (bq25100H/101H); Normal charging to high temperature charging; V_{TS}: 0.5 V → 0.2 V	255	267	279	mV

(1) In Hot mode $V_{O(REG)}$ becomes $V_{O\_HT(REG)}$

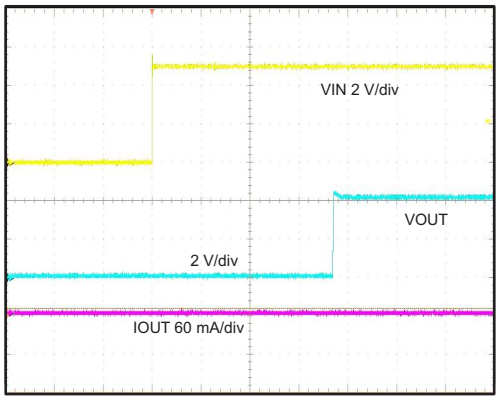
Electrical Characteristics (continued)

Over junction temperature range –5°C ≤ T_J ≤ 125°C and recommended supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{HYS-45°C}$	Hysteresis	At 45°C; High tempemperature charging to normal charging; V_{TS}: 0.2 V → 0.5 V		20		mV
$V_{TS-60°C}$	High temperature disable	bq25100/01/100H/101H/100L; High temperature charge to pending; V_{TS}: 0.2 V → 0.1 V	160	170	180	mV
$V_{HYS-60°C}$	Hysteresis	At 60°C (bq25100/01/100H/101H/100L); Charge pending to high temperature charging; V_{TS}: 0.1 V → 0.2 V		20		mV
$t_{DGL(TS\_10C)}$	Deglitch for TS thresholds: 10C	Normal to cold operation; V_{TS}: 0.6 V → 1 V		50		ms
		Cold to normal operation; V_{TS}: 1 V → 0.6 V		12		
$t_{DGL(TS)}$	Deglitch for TS thresholds: 0/45/60C	Battery charging		30		ms
$V_{TS-EN-10k}$	Charge enable threshold, (10k NTC)	V_{TS}: 0 V → 0.175 V	83	91	99	mV
$V_{TS-DIS\_HYS-10k}$	HYS below $V_{TS-EN-10k}$ to disable, (10k NTC)	V_{TS}: 0.125 V → 0 V		12		mV
THERMAL REGULATION						
$T_{J(REG)}$	Temperature regulation limit			125		°C
$T_{J(OFF)}$	Thermal shutdown temperature			155		°C
$T_{J(OFF-HYS)}$	Thermal shutdown hysteresis			20		°C
LOGIC LEVELS ON /CHG						
V_{OL}	Output low voltage	I_{SINK} = 5 mA			0.4	V
I_{LEAK}	Leakage current into IC	$V_{\overline{CHG}}$ = 5 V			1	μA

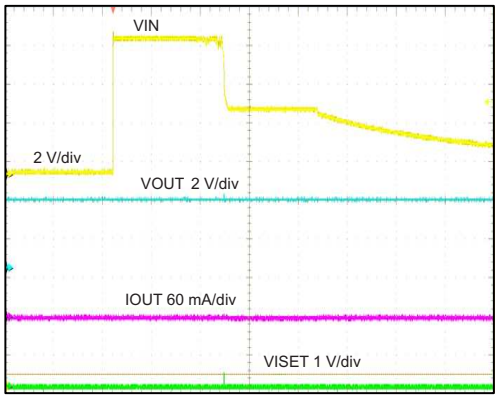
7.6 Typical Characteristics

Setup: Typical Applications Schematic; V_{IN} = 5 V, V_{BAT} = 3.6 V (unless otherwise noted)



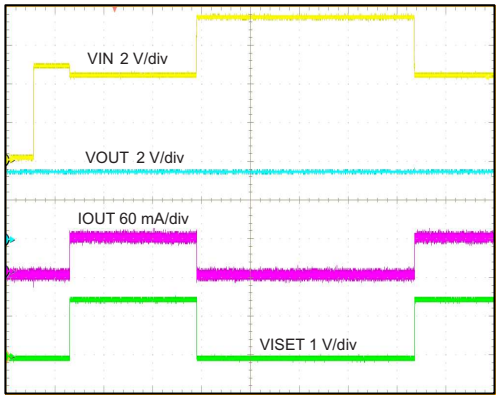
No Battery, No Load

Figure 1. Power Up Timing



Hot Plug

Figure 2. OVP 7-V Adaptor



V_{IN} 0 V -5 V-7 V-5 V

Figure 3. OVP from Normal Power-Up Operation

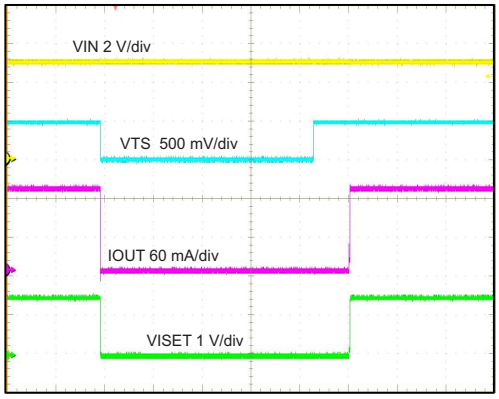
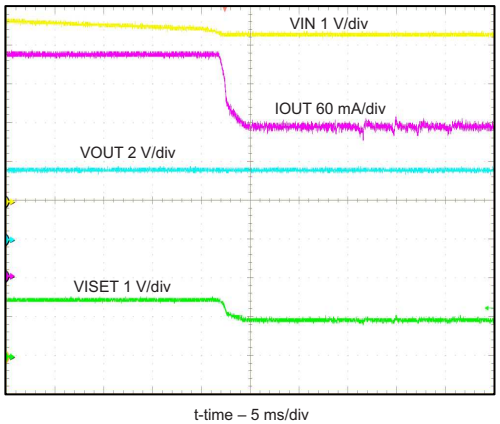


Figure 4. TS Enable and Disable



V_{IN} Regulated

Figure 5. DPM-Adaptor Current Limits

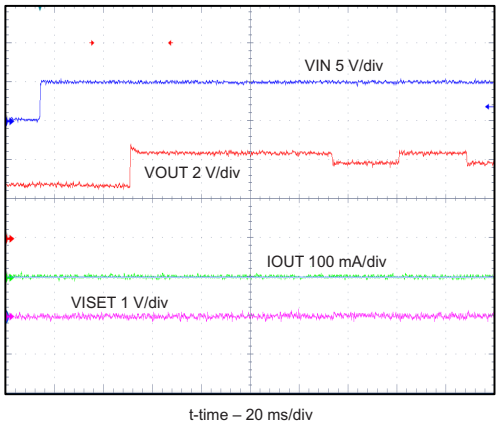
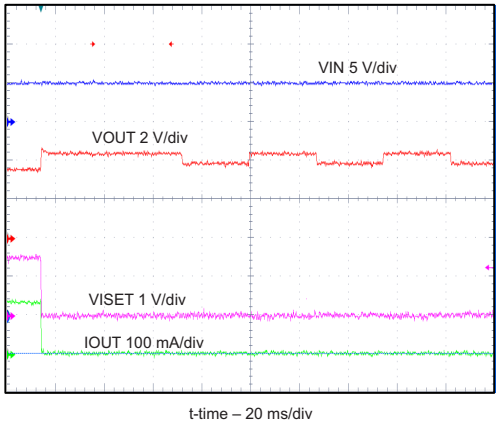


Figure 6. Hot Plug Source with No Battery - Battery Detection

Typical Characteristics (continued)

Setup: Typical Applications Schematic; V_{IN} = 5 V, V_{BAT} = 3.6 V (unless otherwise noted)



No Load

Figure 7. Battery Removal

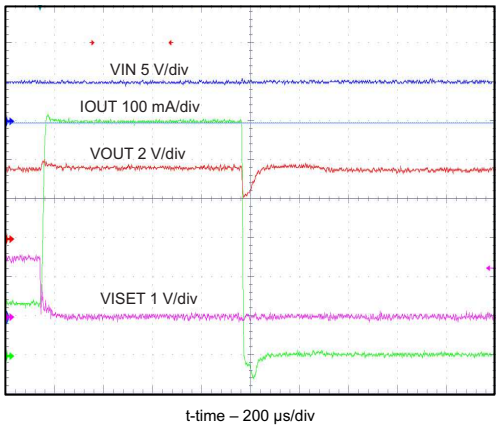
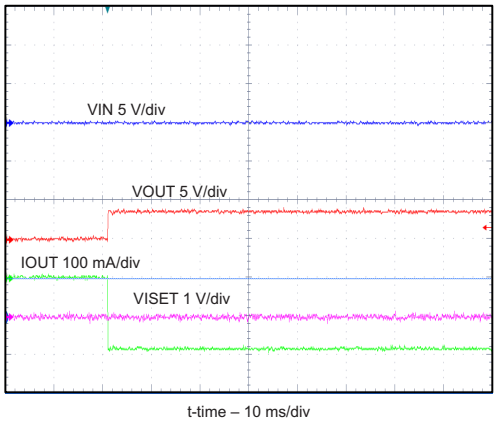
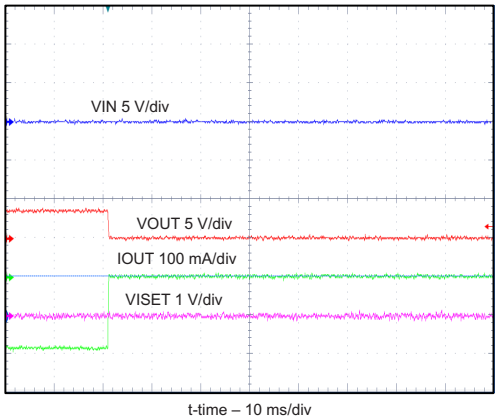


Figure 8. ISET Shorted During Normal Operation



20-Ω resistor at OUT, No input, VBAT = 3.7 V

Figure 9. Battery Plug In



20-Ω resistor at OUT, No input, VBAT = 3.7 V

Figure 10. Battery Removal

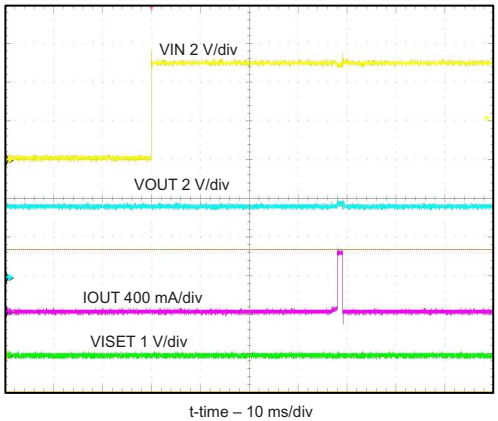
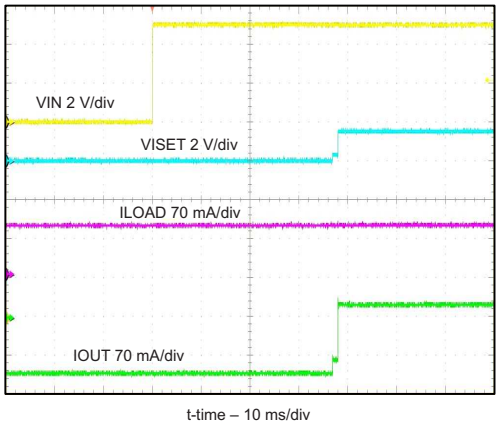


Figure 11. ISET Short Prior to Power Up



90-mA Load, 120-mA ICHG

Figure 12. Power Up

Typical Characteristics (continued)

Setup: Typical Applications Schematic; V_{IN} = 5 V, V_{BAT} = 3.6 V (unless otherwise noted)

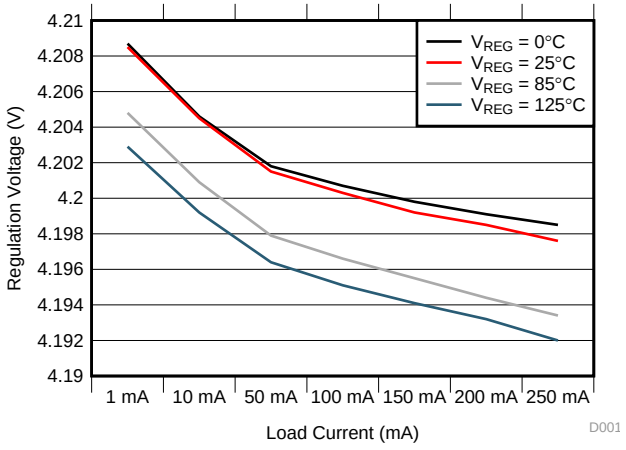


Figure 13. Load Regulation Over Temperature

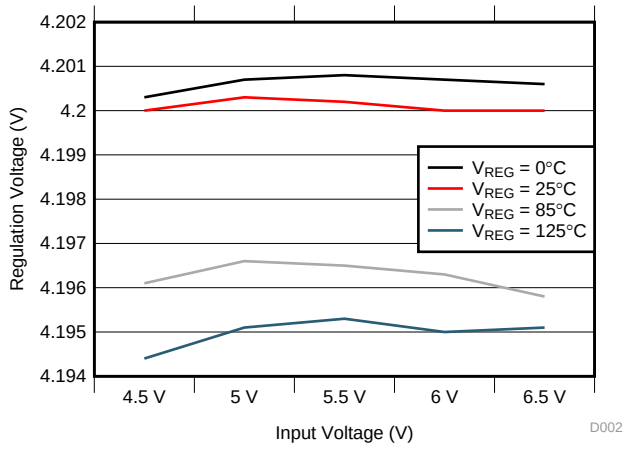


Figure 14. Line Regulation Over Temperature

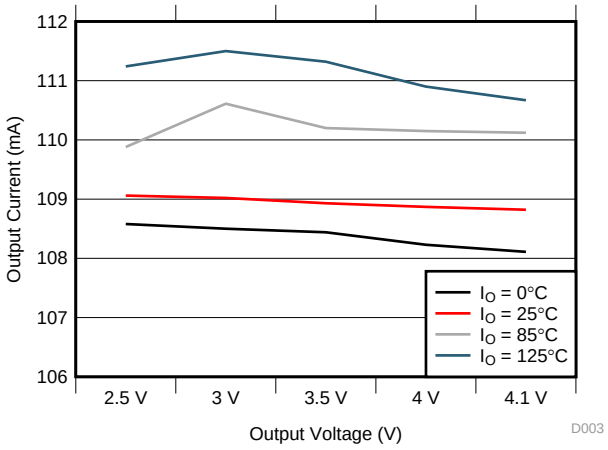
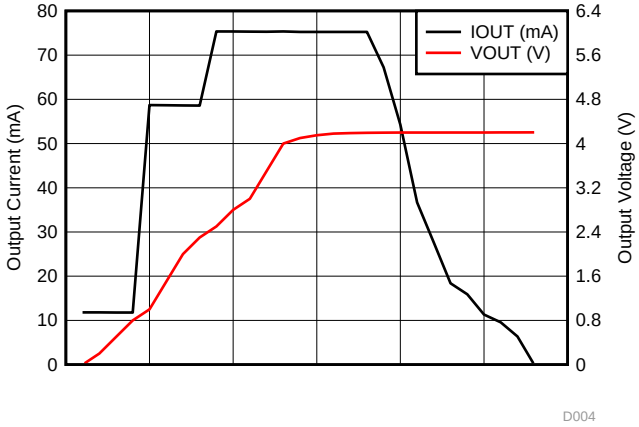


Figure 15. Current Regulation Over Temperature



bq25100 charge cycle, ICHG = 75 mA, VBAT_REG = 4.2 V

Figure 16. Battery Voltage vs Charge Current

8 Detailed Description

8.1 Overview

The bq25100B is a highly integrated family of single cell Li-Ion and Li-Pol chargers. The charger can be used to charge a battery, power a system or both. The charger has three phases of charging: pre-charge to recover a fully discharged battery, fast-charge constant current to supply the charge safely and voltage regulation to safely reach full capacity. The charger is very flexible, allowing programming of the fast-charge current and Pre-charge/Termination Current. This charger is designed to work with a USB connection (100-mA limit) or Adaptor (DC output). The charger also checks to see if a battery is present. The following discussion reviews all products in the bq25100B family. Not all features apply to the bq25100B.

The charger also comes with a full set of safety features: JEITA Temperature Standard (bq25100/01/100H/101H), Over-Voltage Protection, DPM-IN, Safety Timers, and ISET short protection. All of these features and more are described in detail below.

The charger is designed for a single power path from the input to the output to charge a single cell Li-Ion or Li-Pol battery pack. Upon application of a 5-V DC power source the ISET and OUT short checks are performed to assure a proper charge cycle.

If the battery voltage is below the LOWV threshold, the battery is considered discharged and a preconditioning cycle begins. The amount of precharge current can be programmed using the PRE-TERM pin which programs a percent of fast charge current (10 to 100%) as the precharge current. This feature is useful when the system load is connected across the battery “stealing” the battery current. The precharge current can be set higher to account for the system loading while allowing the battery to be properly conditioned. The PRE-TERM pin is a dual function pin which sets the precharge current level and the termination threshold level. The termination "current threshold" is always half of the precharge programmed current level.

Once the battery voltage has charged to the VLOWV threshold, fast charge is initiated and the fast charge current is applied. The fast charge constant current is programmed using the ISET pin. The constant current provides the bulk of the charge. Power dissipation in the IC is greatest in fast charge with a lower battery voltage. If the IC reaches 125°C, the IC enters thermal regulation, slows the timer clock by half, and reduces the charge current as needed to keep the temperature from rising any further. Figure 17 shows the charging profile with thermal regulation. Typically under normal operating conditions, the IC’s junction temperature is less than 125°C and thermal regulation is not entered.

Once the cell has charged to the regulation voltage the voltage loop takes control and holds the battery at the regulation voltage until the current tapers to the termination threshold. The termination can be disabled if desired.

Further details are described in the Operating Modes section.

Overview (continued)

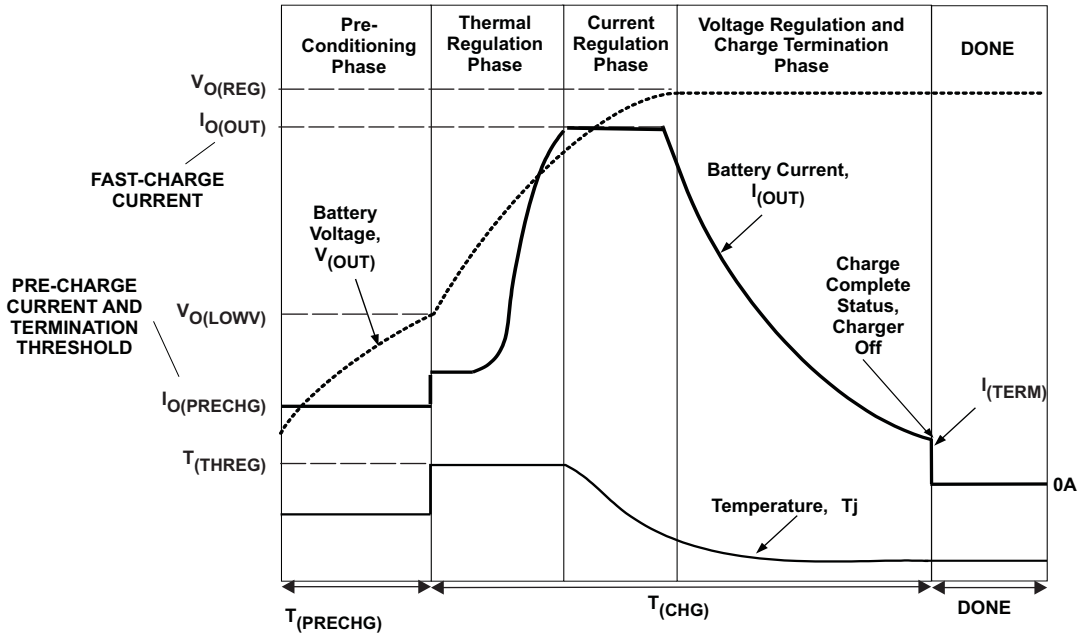
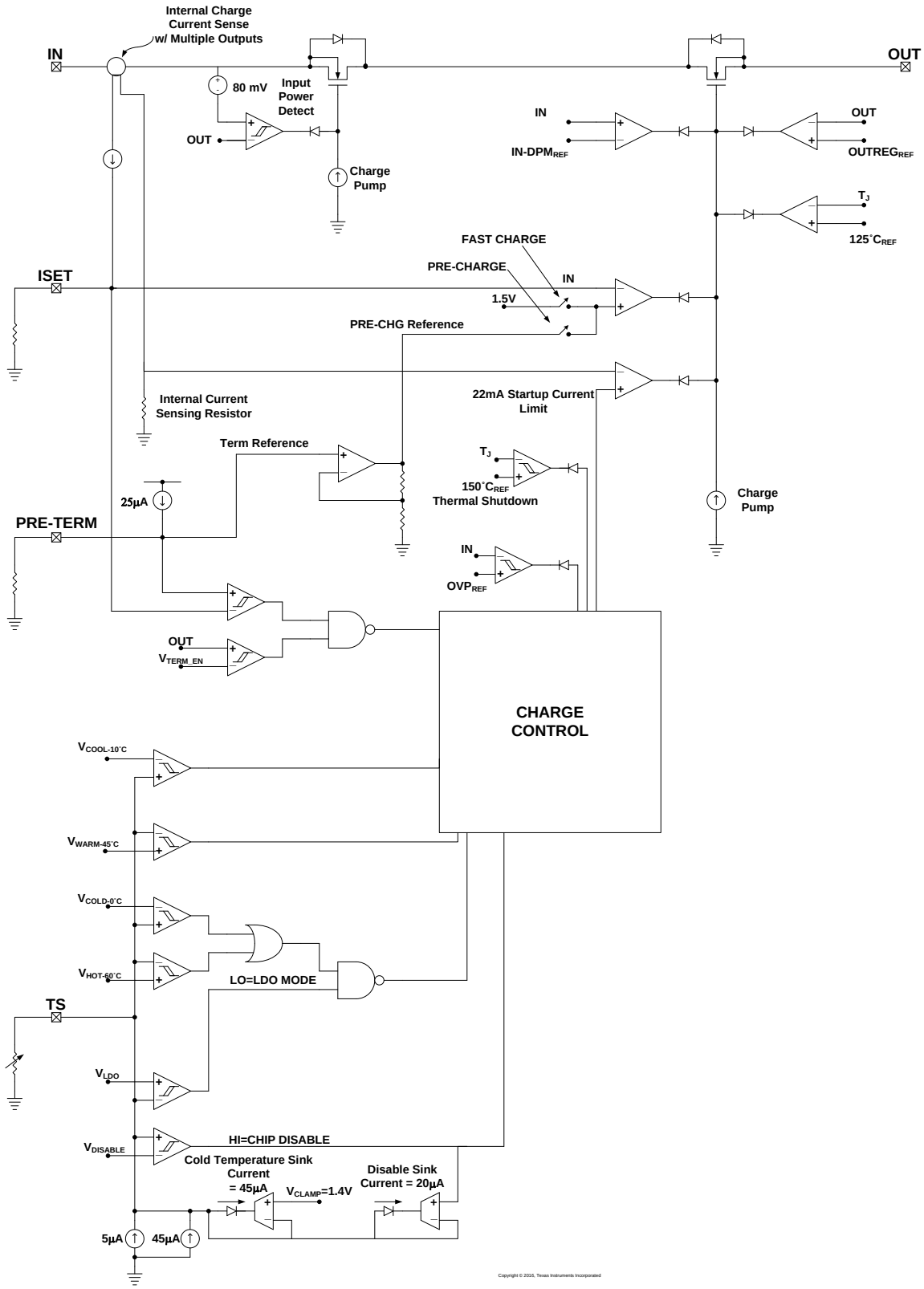


Figure 17. Charging Profile With Thermal Regulation

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Overvoltage-Protection (OVP) – Continuously Monitored

If the input source applies an overvoltage, the pass FET, if previously on, turns off after a deglitch, $t_{BLK(OVP)}$. The timer stops counting. Once the overvoltage returns to a normal voltage, the timer and charge continues.

8.3.2 $\overline{\text{CHG}}$ Pin Indication (bq25101, bq25101H)

The charge pin has an internal open drain FET which is on (pulls down to VSS) during the first charge only (independent of TTDM) and is turned off once the battery reaches voltage regulation and the charge current tapers to the termination threshold set by the PRE-TERM resistor. The bq25101/01H terminates at 10% of the programmed charge current. The charge pin is high impedance in sleep mode and OVP and returns to its previous state once the condition is removed. Cycling input power, removing and replacing the battery, pulling the TS pin low and releasing or entering pre-charge mode causes the $\overline{\text{CHG}}$ pin to go reset (go low if power is good and a discharged battery is attached) and is considered the start of a first charge.

8.3.3 $\overline{\text{CHG}}$ Pin LED Pull-up Source (bq25101, bq25101H)

For host monitoring, a pull-up resistor is used between the $\overline{\text{CHG}}$ pin and the VCC of the host and for a visual indication a resistor in series with an LED is connected between the /CHG pin and a power source. If the CHG source is capable of exceeding 7 V, a 6.2-V zener should be used to clamp the voltage. If the source is the OUT pin, note that as the battery changes voltage, and the brightness of the LEDs vary.

8.3.4 IN-DPM (V_{IN}-DPM or IN-DPM)

The IN-DPM feature is used to detect an input source voltage that is folding back (voltage dropping), reaching its current limit due to excessive load. When the input voltage drops to the $V_{IN\text{-}DPM}$ threshold the internal pass FET starts to reduce the current until there is no further drop in voltage at the input. This would prevent a source with voltage less than $V_{IN\text{-}DPM}$ to power the out pin. This is an added safety feature that helps protect the source from excessive loads. This feature is not applicable for bq25100B.

8.3.5 OUT

The Charger's OUT pin provides current to the battery and to the system, if present. This IC can be used to charge the battery plus power the system, charge just the battery or just power the system (TTDM) assuming the loads do not exceed the available current. The OUT pin is a current limited source and is inherently protected against shorts. If the system load ever exceeds the output programmed current threshold, the output will be discharged unless there is sufficient capacitance or a charged battery present to supplement the excessive load.

8.3.6 ISET

An external resistor is used to Program the Output Current (10 to 250 mA) and can be used as a current monitor.

$$R_{ISET} = K_{ISET} \div I_{OUT} \quad (1)$$

Where:

I_{OUT} is the desired fast charge current;
K_{ISET} is a gain factor found in the electrical specification

For greater accuracy at lower currents, part of the sense FET is disabled to give better resolution. Going from higher currents to low currents, there is hysteresis and the transition occurs around 50 mA.

The ISET resistor is short protected and will detect a resistance lower than ≠420 Ω. The detection requires at least 50 mA of output current. If a "short" is detected, then the IC will latch off and can be reset by cycling the power or cycling TS pin. The OUT current is internally clamped to a maximum current of 600 mA typical and is independent of the ISET short detection circuitry.

For charge current that is below 50 mA, an extra RC circuit is recommended on ISET to acheive more stable current signal. More detail is available in 9.1 Application Information.

Feature Description (continued)

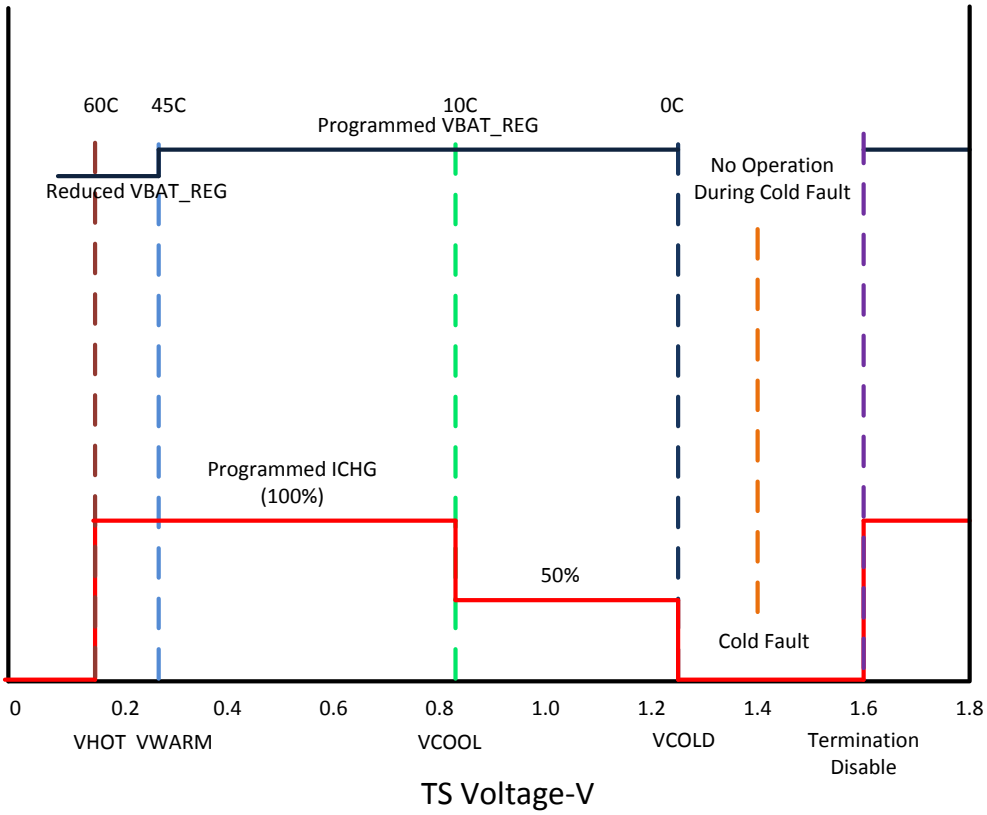


Figure 18. JEITA Operation Over TS Bias Voltage - bq25100, bq25100H, bq25101, bq25101H

Feature Description (continued)

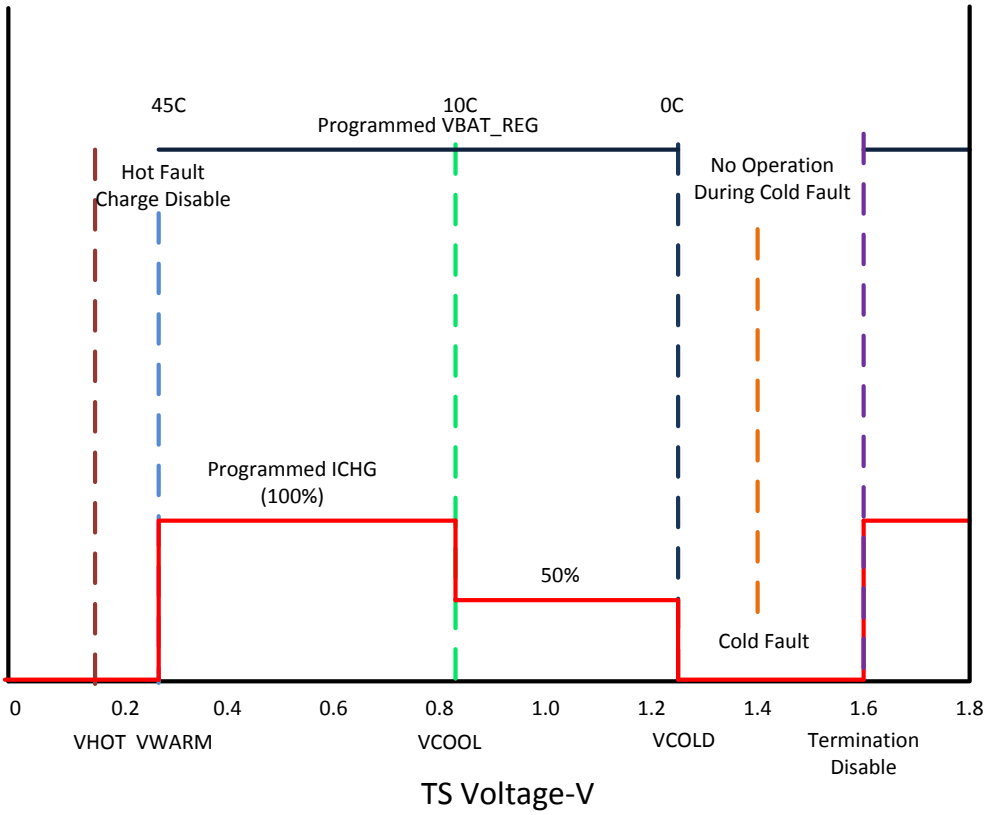


Figure 19. Standard Operation Over TS Bias Voltage – bq25100B, bq25100A, bq25100L

8.3.7 PRE_TERM – Pre-Charge and Termination Programmable Threshold

Pre-Term is used to program both the pre-charge current and the termination current threshold. The pre-charge current level is a factor of two higher than the termination current level. The termination can be set between 5 and 50% (recommended range) of the programmed output current level set by ISET. If left floating the termination and pre-charge are set internally at 10/20% respectively. The $R_{PRE-TERM}$ is ranged from 600 Ω to 30 kΩ and the minimum termination current can be programmed to 1 mA. The pre-charge-to-fast-charge, V_{lowv} threshold is set to 2.5 V.

$$R_{PRE-TERM} = \%Term \times K_{TERM} = \%Pre\text{-}CHG \times K_{PRE-CHG} \quad (2)$$

Where:

%Term is the percent of fast charge current where termination occurs;
%Pre-CHG is the percent of fast charge current that is desired during precharge;
K_{TERM} and $K_{PRE-CHG}$ are gain factors found in the electrical specifications.

8.3.8 TS

The TS function for the bq25100B/bq25100A cuts the charge current level in half between 0°C and 10°C and disables charging when the NTC temperature is above 45°C. The TS function for the bq25100/bq25100H/bq25101/bq25101H is designed to follow the new JEITA temperature standard for Li-Ion and Li-Pol batteries. There are now four thresholds, 60°C, 45°C, 10°C, and 0°C. Normal operation occurs between 10°C and 45°C. If between 0°C and 10°C the charge current level is cut in half and if between 45°C and 60°C the regulation voltage is reduced to 4.1 V max for bq25100 and 4.2 V max for bq25100H, see Figure 18.

Feature Description (continued)

The TS feature is implemented using an internal 50μA current source to bias the thermistor (designed for use with a 10-k NTC β = 3370 (SEMITEC 103AT-2 or Mitsubishi TH05-3H103F) connected from the TS pin to V_{SS}. If this feature is not needed, a fixed 10-k can be placed between TS and V_{SS} to allow normal operation. This may be done if the host is monitoring the thermistor and then the host would determine when to pull the TS pin low to disable charge.

The TS pin has two additional features, when the TS pin is pulled low or floated/driven high. A low disables charge and a high puts the charger in TTDM.

Above 45°C (60°C for bq25100/bq25100H/bq25101/bq25101H) or below 0°C the charge is disabled. Once the thermistor reaches ≠–10°C the TS current folds back to keep a cold thermistor (between –10°C and –50°C) from placing the IC in the TTDM mode. If the TS pin is pulled low into disable mode, the current is reduce to ≠30 μA. Since the I_{TS} curent is fixed along with the temperature thresholds, it is not possible to use thermistor values other than the 10-k NTC (at 25°C).

8.3.9 Timers

The pre-charge timer is set to 30 minutes. The pre-charge current, can be programmed to off-set any system load, making sure that the 30 minutes is adequate.

The fast charge timer is fixed at 10 hours and can be increased real time by going into thermal regulation or IN-DPM. The timer clock slows by a factor of 2, resulting in a clock than counts half as fast when in these modes. If either the 30 minute or ten hour timer times out, the charging is terminated and for bq25101/1H the $\overline{CHG}$ pin goes high impedance if not already in that state. The timer is reset by disabling the IC, cycling power or going into and out of TTDM.

8.3.10 Termination

Once the OUT pin goes above VRCH, (reaches voltage regulation) and the current tapers down to the termination threshold, a battery detect route is run to determine if the battery was removed or the battery is full. If the battery is present, the charge current will terminate. If the battery was removed along with the thermistor, then the TS pin is driven high and the charge enters TTDM. If the battery was removed and the TS pin is held in the active region, then the battery detect routine will continue until a battery is inserted. The termination current can be programmed down to 625 uA, however, the accuracy will reduce acoordingly when the termination current is below 1 mA.

8.4 Device Functional Modes

8.4.1 Power-Down or Undervoltage Lockout (UVLO)

The bq25100B family is in power down mode if the IN pin voltage is less than UVLO. The part is considered “dead” and all the pins are high impedance. Once the IN voltage rises above the UVLO threshold the IC will enter Sleep Mode or Active mode depending on the OUT pin (battery) voltage.

8.4.2 Power-up

The IC is alive after the IN voltage ramps above UVLO (see sleep mode), resets all logic and timers, and starts to perform many of the continuous monitoring routines. Typically the input voltage quickly rises through the UVLO and sleep states where the IC declares power good, starts the qualification charge at 22 mA, sets the charge current base on the ISET pin, and starts the safety timer.

8.4.3 Sleep Mode

If the IN pin voltage is between V_{OUT}+V_{DT} and UVLO, the charge current is disabled, the safety timer counting stops (not reset). As the input voltage rises and the charger exits sleep mode, the safety timer continues to count and the charge is enabled. See Figure 20.

8.4.4 New Charge Cycle

A new charge cycle is started when a good power source is applied, performing a chip disable/enable (TS pin), exiting Termination and Timer Disable Mode (TTDM), detecting a battery insertion or the OUT voltage dropping below the VRCH threshold.

Device Functional Modes (continued)

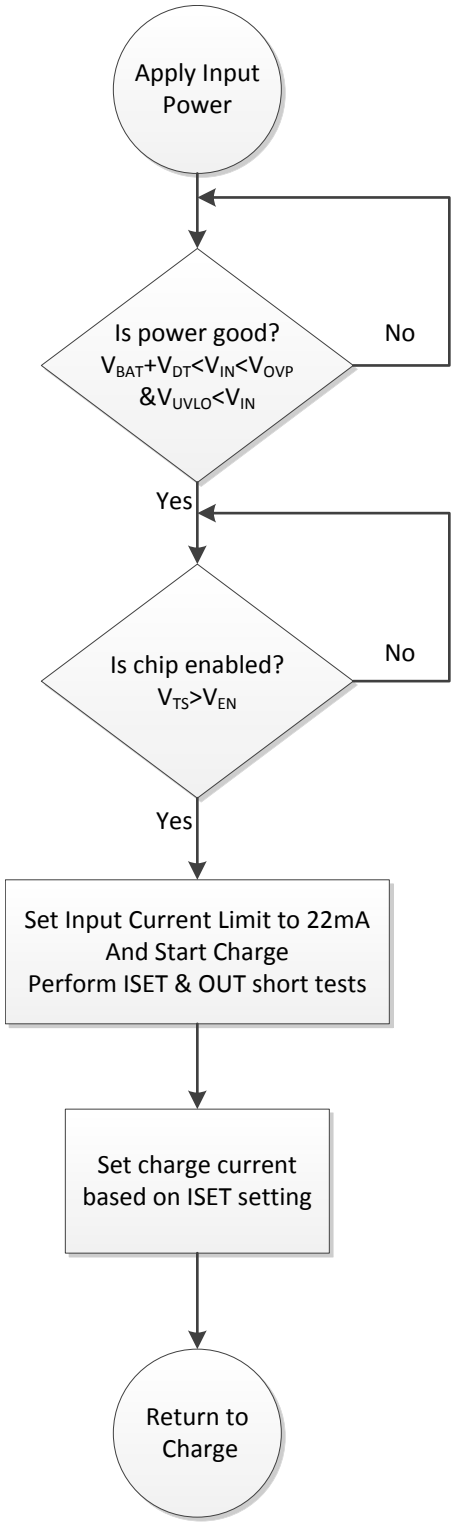


Figure 20. bq25100B Power-Up Flow Diagram

Device Functional Modes (continued)

8.4.5 Termination and Timer Disable Mode (TTDM) - TS Pin High

The battery charger is in TTDM when the TS pin goes high from removing the thermistor (removing battery pack/floating the TS pin) or by pulling the TS pin up to the TTDM threshold.

When entering TTDM, the 10 hour safety timer is held in reset and termination is disabled. A battery detect routine is run to see if the battery was removed or not. For bq25101/1H, if the battery was removed then the $\overline{CHG}$ pin will go to its high impedance state if not already there. If a battery is detected the $\overline{CHG}$ pin does not change states until the current tapers to the termination threshold, where the $\overline{CHG}$ pin goes to its high impedance state if not already there (the regulated output will remain on).

The charging profile does not change (still has pre-charge, fast-charge constant current and constant voltage modes). This implies the battery is still charged safely and the current is allowed to taper to zero.

When coming out of TTDM, the battery detect routine is run and if a battery is detected, then a new charge cycle begins.

If TTDM is not desired upon removing the battery with the thermistor, one can add a 237-kΩ resistor between TS and V_{SS} to disable TTDM. This keeps the current source from driving the TS pin into TTDM. This creates ≠0.1°C error at hot and a ≠3°C error at cold.

8.4.6 Battery Detect Routine

The battery detect routine should check for a missing battery while keeping the OUT pin at a useable voltage.

The battery detect routine is run when entering and exiting TTDM to verify if battery is present, or run all the time if battery is missing and not in TTDM. On power-up, if battery voltage is greater than V_{RCH} thereshold, a battery detect routine is run to determine if a battery is present.

The battery detect routine is disabled while the IC is in TTDM, or has a TS fault. See Figure 21 for the Battery Detect Flow Diagram.

8.4.7 Refresh Threshold

After termination, if the OUT pin voltage drops to V_{RCH} (100mV below regulation) then a new charge is initiated.

8.4.8 Starting a Charge on a Full Battery

The termination threshold is raised by ≠14% for the first minute of a charge cycle so if a full battery is removed and reinserted or a new charge cycle is initiated, that the new charge terminates (less than 1 minute). Batteries that have relaxed many hours may take several minutes to taper to the termination threshold and terminate charge.

Device Functional Modes (continued)

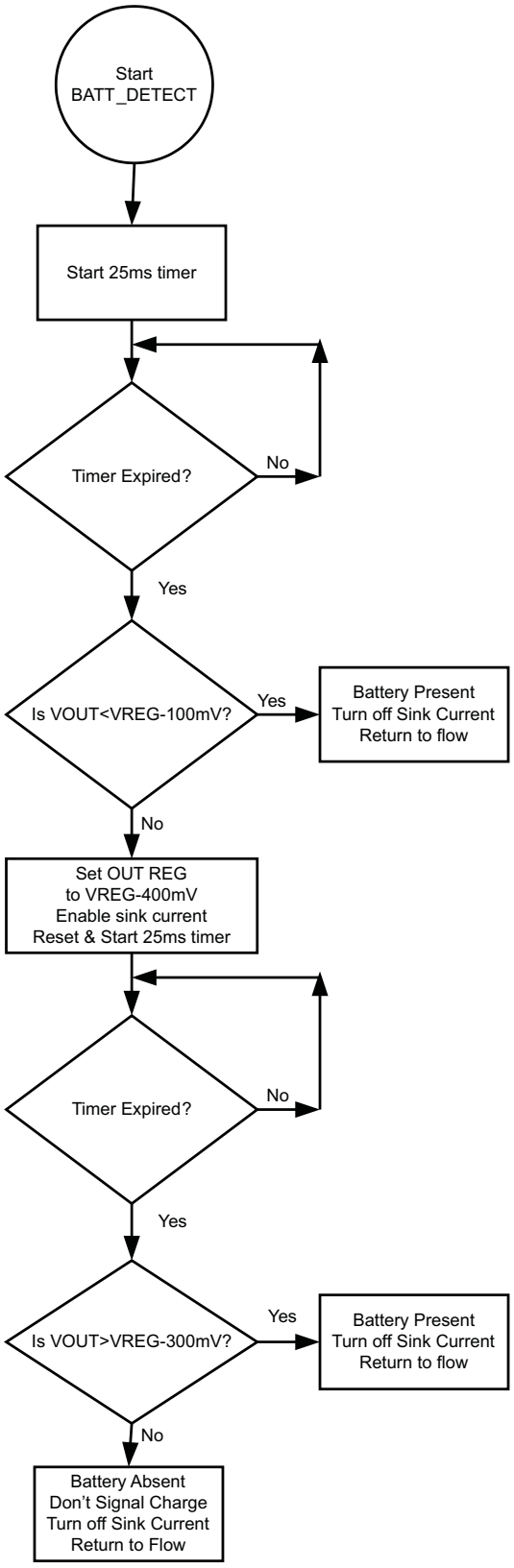


Figure 21. Battery Detect Routine

9 Application and Implementation

NOTE

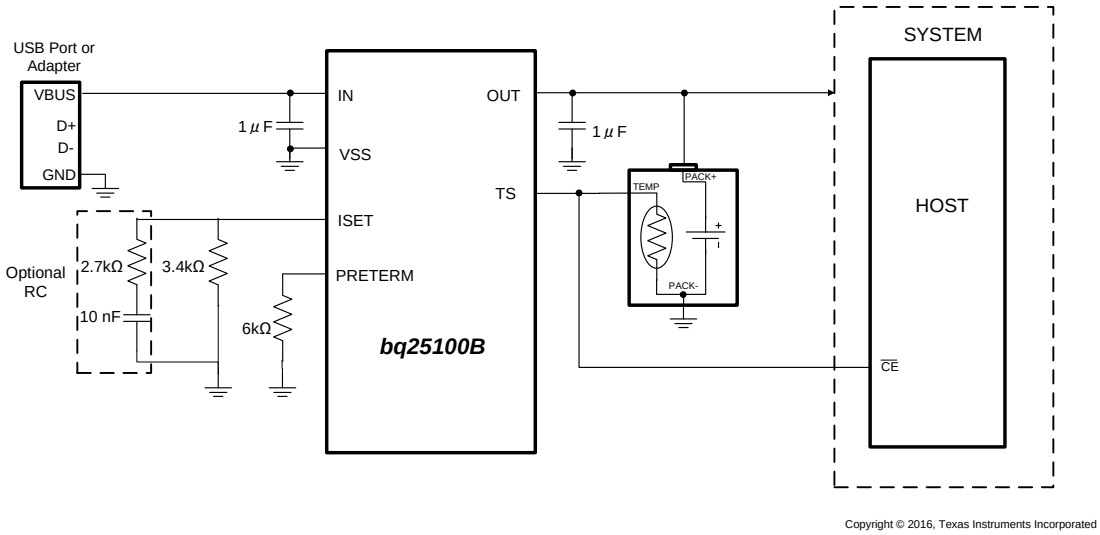
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The bq25100B series of devices are highly integrated Li-Ion and Li-Pol linear chargers targeted at space-limited portable applications. The fast charge current can be programmed from 10 mA to 250 mA through an external resistor on ISET pin. The pre_charge and termination current can also be programmed through the resistor connected on PRETERM pin. The device has complete system-level protection such as input under-voltage lockout (UVLO), input over-voltage protection (OVP), sleep mode, thermal regulation, safety timers, and NTC monitoring input.

9.2 Typical Application

This typical application shows a charger application design example.



9.2.1 Design Requirements

- Supply voltage = 5 V
- Fast charge current: I_{OUT-FC} = 40 mA;
- Termination Current Threshold: $\%_{IOUT-FC}$ = 10% of Fast Charge or ~4 mA
- Pre-Charge Current by default is twice the termination Current or ~8 mA
- TS – Battery Temperature Sense = 10-k NTC (103AT)
- $\overline{CE}$ is an open drain control pin

Typical Application (continued)

9.2.2 Detailed Design Procedures

- The regulation voltage is set to 4.2 V, the input voltage is 5 V and the charge current is programmed to 40 mA.
- For charge current that is below 50 mA, an extra RC circuit is recommended on ISET to acheive more stable current signal. For applications that need higher charge current, the RC circuit is not needed.
- For applications that use more than 200-mA current, there could be a very low level ~1% of charge current ringing in the output. The ringing can be removed by increasing the input capacitance.

9.2.2.1 Calculations

9.2.2.1.1 Program the Fast Charge Current, ISET:

$R_{ISET} = [K_{(ISET)} / I_{(OUT)}]$
from electrical characteristics table. . . $K_{(SET)} = 135$ AΩ
$R_{ISET} = [135$ AΩ/0.04 A] = 3.4 kΩ
Selecting the closest standard value, use a 3.4-kΩ resistor between ISET and Vss.

9.2.2.1.2 Program the Termination Current Threshold, ITERM:

$R_{PRE\text{-}TERM} = K_{(TERM)} \times \%_{IOUT\text{-}FC}$
$R_{PRE\text{-}TERM} = 600$ Ω/% × 10% = 6 kΩ
Selecting the closest standard value, use a 6-kΩ resistor between PRETERM and Vss.
One can arrive at the same value by using 20% for a pre-charge value (factor of 2 difference).
$R_{PRE\text{-}TERM} = K_{(PRE\text{-}CHG)} \times \%_{IOUT\text{-}FC}$
$R_{PRE\text{-}TERM} = 300$ Ω/% × 20%= 6 kΩ

9.2.2.1.3 TS Function

Use a 10-k NTC thermistor in the battery pack (103AT).

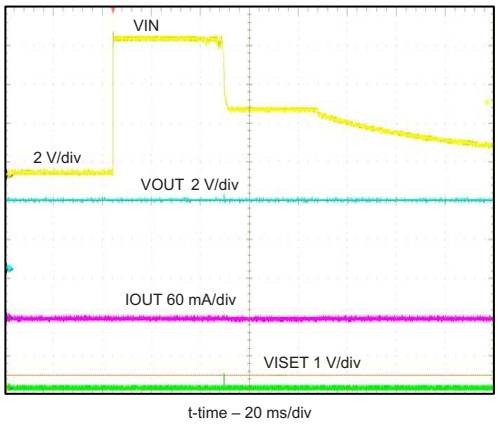
To Disable the temp sense function, use a fixed 10-kΩ resistor between the TS and VSS.

9.2.2.1.4 Selecting IN and OUT Pin Capacitors

In most applications, all that is needed is a high-frequency decoupling capacitor (ceramic) on the power pin, input and output pins. Using the values shown on the application diagram is recommended. After evaluation of these voltage signals with real system operational conditions, one can determine if capacitance values can be adjusted toward the minimum recommended values (DC load application) or higher values for fast, high amplitude, pulsed load applications. Note if designed for high input voltage sources (bad adaptors or wrong adaptors), the capacitor needs to be rated appropriately. Ceramic capacitors are tested to 2x their rated values so a 16-V capacitor may be adequate for a 30-V transient (verify tested rating with capacitor manufacturer).

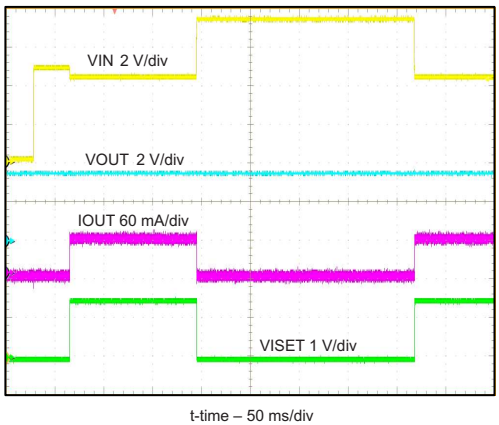
Typical Application (continued)

9.2.3 Application Performance Plots



Hot Plug

Figure 22. OVP 7-V Adaptor



V_{IN} 0 V -5 V-7 V-5 V

Figure 23. OVP from Normal Power-Up Operation

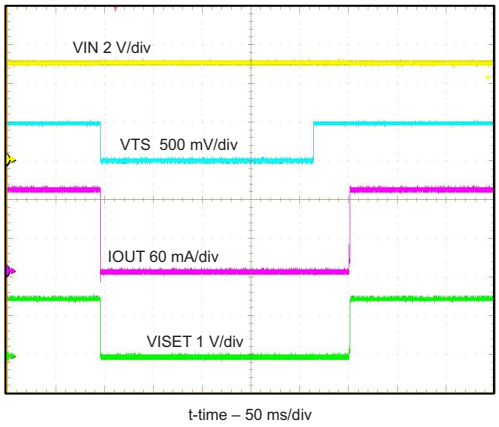
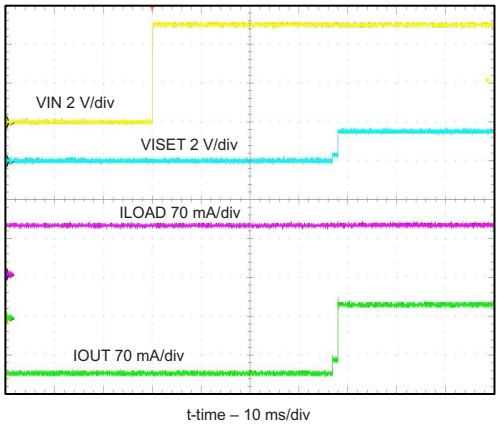


Figure 24. TS Enable and Disable



90-mA Load, 120-mA IOUT

Figure 25. Power Up

10 Power Supply Recommendations

10.1 Leakage Current Effects on Battery Capacity

To determine how fast a leakage current on the battery will discharge the battery is an easy calculation. The time from full to discharge can be calculated by dividing the Amp-Hour Capacity of the battery by the leakage current. For a 0.1-AHr battery and a 75-nA leakage current (100 mAHr/75 nA = 250000 Hours), it would take 1333k hours or 152 years to discharge. In reality the self discharge of the cell would be much faster so the 75-nA leakage would be considered negligible.

11 Layout

11.1 Layout Guidelines

To obtain optimal performance, the decoupling capacitor from IN to GND and the output filter capacitors from OUT to GND should be placed as close as possible to the bq25100B, with short trace runs to both IN, OUT and GND.

- All low-current GND connections should be kept separate from the high-current charge or discharge paths from the battery. Use a single-point ground technique incorporating both the small signal ground path and the power ground path.
- The high current charge paths into IN pin and from the OUT pin must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces

11.2 Layout Example

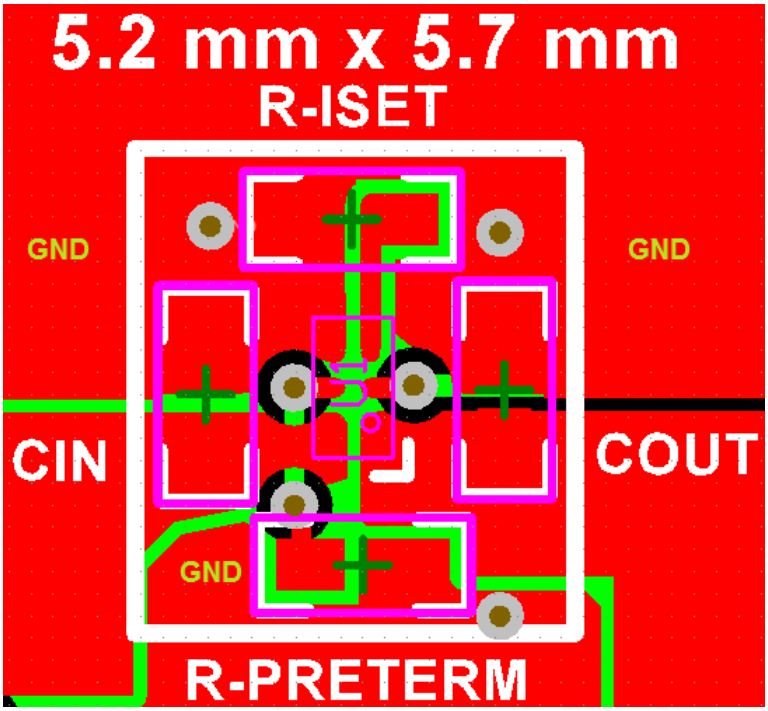


Figure 26. Board Layout

11.3 Thermal Considerations

The most common measure of package thermal performance is thermal impedance (θ_{JA}) measured (or modeled) from the chip junction to the air surrounding the package surface (ambient). The mathematical expression for θ_{JA} is:

$$R_{\theta JA} = (T_J – T_A) / P$$

where

- T_J = chip junction temperature
- T_A = Ambient temperature
- P = device power dissipation (3)

Factors that can influence the measurement and calculation of $R_{\theta JA}$ include:

1. Whether or not the device is board mounted
2. Trace size, composition, thickness, and geometry
3. Orientation of the device (horizontal or vertical)
4. Volume of the ambient air surrounding the device under test and airflow
5. Whether other surfaces are in close proximity to the device being tested

Due to the charge profile of Li-Ion and Li-Pol batteries the maximum power dissipation is typically seen at the beginning of the charge cycle when the battery voltage is at its lowest. Typically after fast charge begins the pack voltage increases to ≠3.4 V within the first 2 minutes. The thermal time constant of the assembly typically takes a few minutes to heat up so when doing maximum power dissipation calculations, 3.4 V is a good minimum voltage to use.

The device power dissipation, P, is a function of the charge rate and the voltage drop across the internal PowerFET. It can be calculated from the following equation when a battery pack is being charged :

$$P = [V_{(IN)} – V_{(OUT)}] × I_{(OUT)} \quad (4)$$

The thermal loop feature reduces the charge current to limit excessive IC junction temperature. It is recommended that the design not run in thermal regulation for typical operating conditions (nominal input voltage and nominal ambient temperatures) and use the feature for non typical situations such as hot environments or higher than normal input source voltage. With that said, the IC will still perform as described, if the thermal loop is always active.

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
bq25100	Click here	Click here	Click here	Click here	Click here
bq25101	Click here	Click here	Click here	Click here	Click here
bq25100A	Click here	Click here	Click here	Click here	Click here
bq25100H	Click here	Click here	Click here	Click here	Click here
bq25101H	Click here	Click here	Click here	Click here	Click here
bq25100L	Click here	Click here	Click here	Click here	Click here

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
Bluetooth is a registered trademark of Bluetooth SIG, Inc..

12.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ25100BYFPR	Active	Production	DSBGA (YFP) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-5 to 125	25100B
BQ25100BYFPR.A	Active	Production	DSBGA (YFP) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-5 to 125	25100B
BQ25100BYFPT	Active	Production	DSBGA (YFP) | 6	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-5 to 125	25100B
BQ25100BYFPT.A	Active	Production	DSBGA (YFP) | 6	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-5 to 125	25100B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

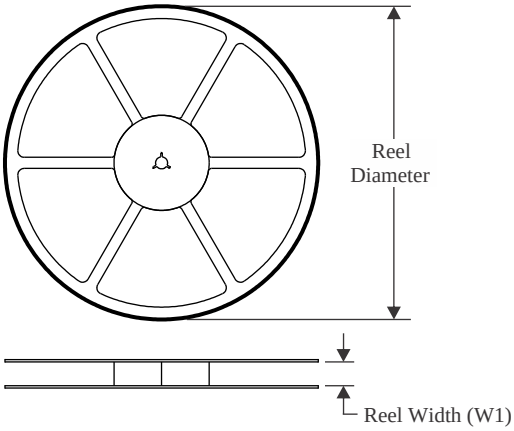
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

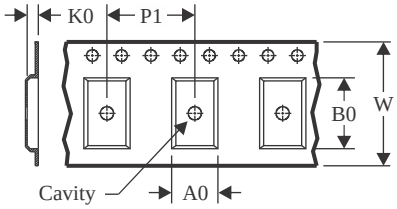
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

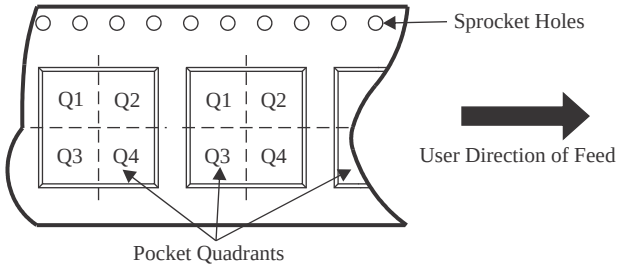


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

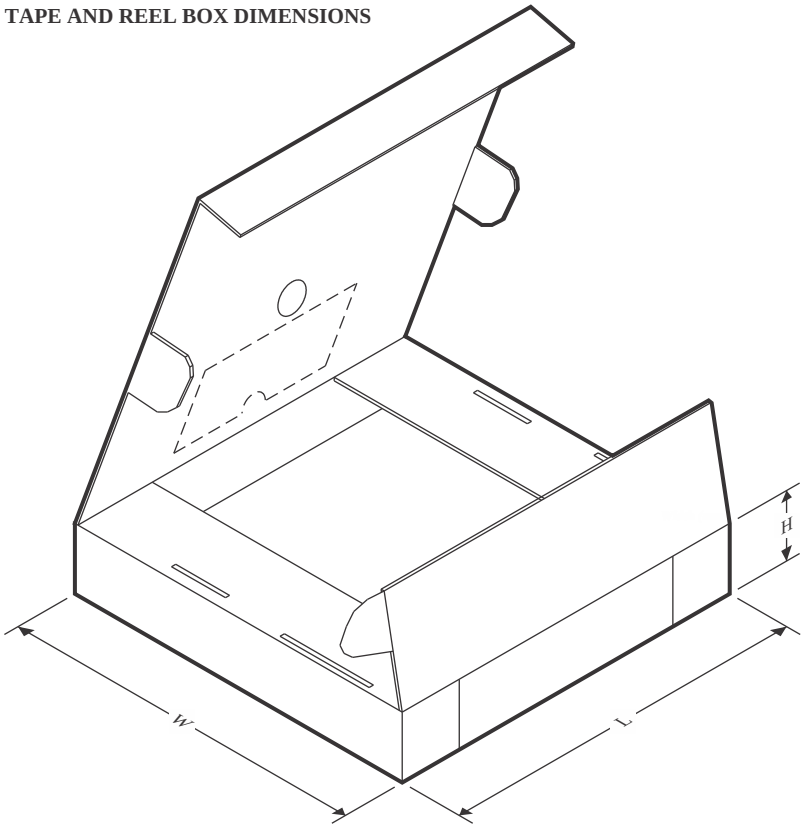
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ25100BYFPR	DSBGA	YFP	6	3000	180.0	8.4	0.98	1.68	0.59	4.0	8.0	Q1
BQ25100BYFPT	DSBGA	YFP	6	250	180.0	8.4	0.98	1.68	0.59	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

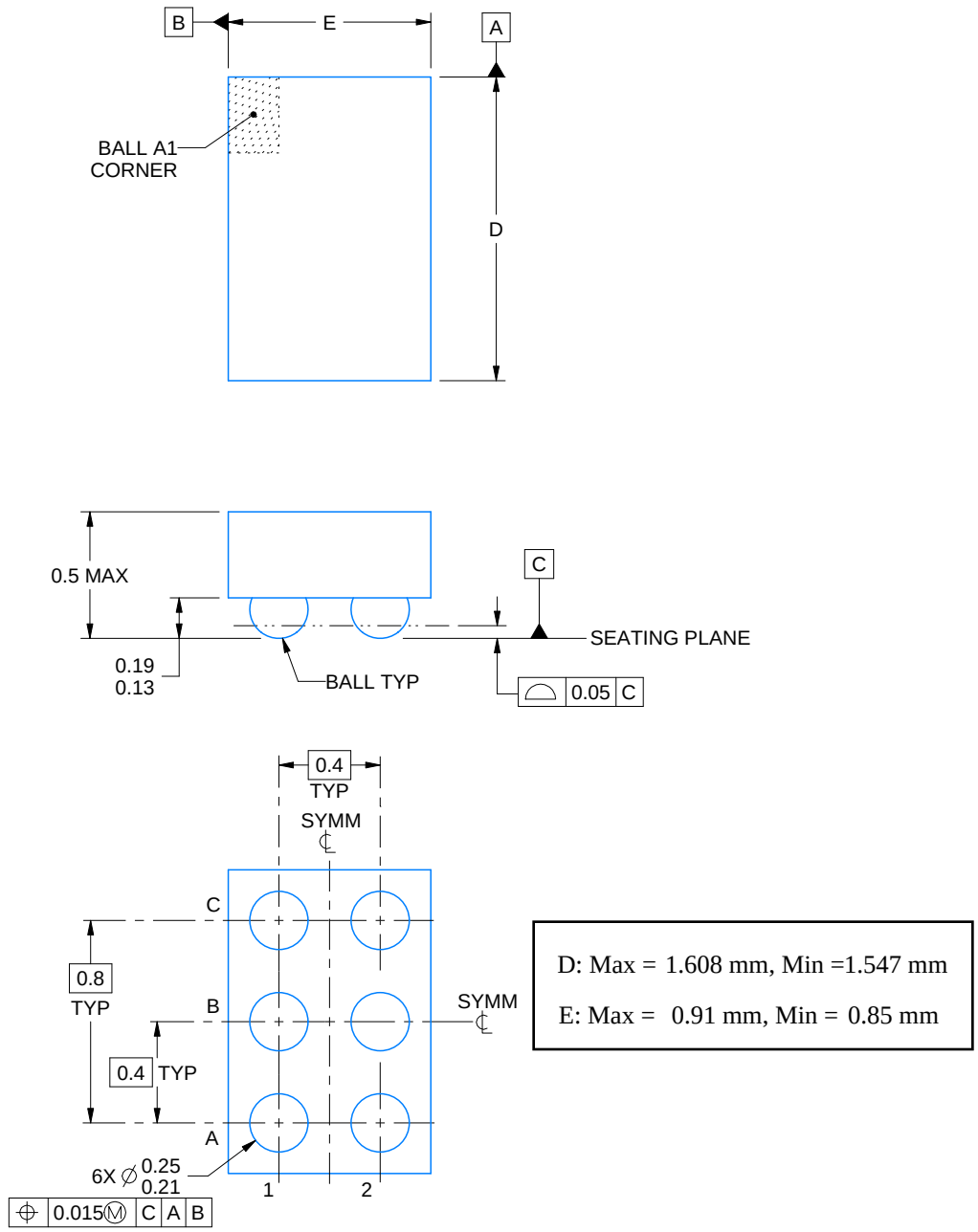
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ25100BYFPR	DSBGA	YFP	6	3000	182.0	182.0	20.0
BQ25100BYFPT	DSBGA	YFP	6	250	182.0	182.0	20.0

PACKAGE OUTLINE

YFP0006

DSBGA - 0.5 mm max height

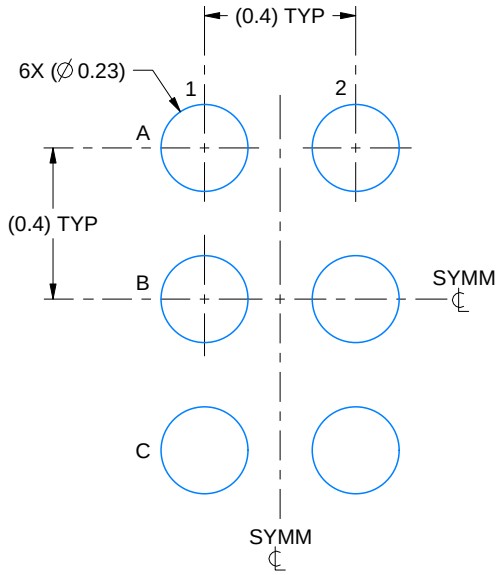
DIE SIZE BALL GRID ARRAY



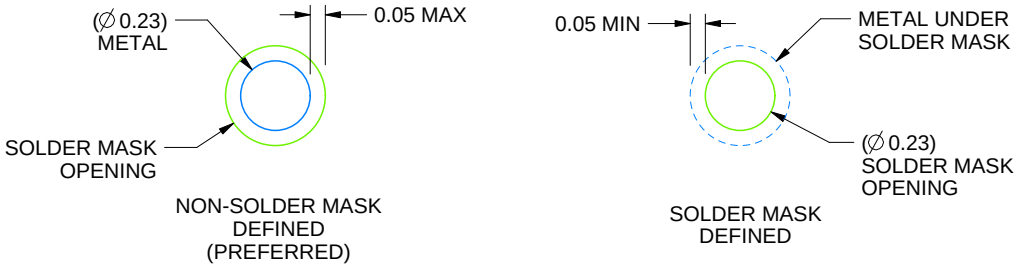
4223410/A 11/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:50X



SOLDER MASK DETAILS
NOT TO SCALE

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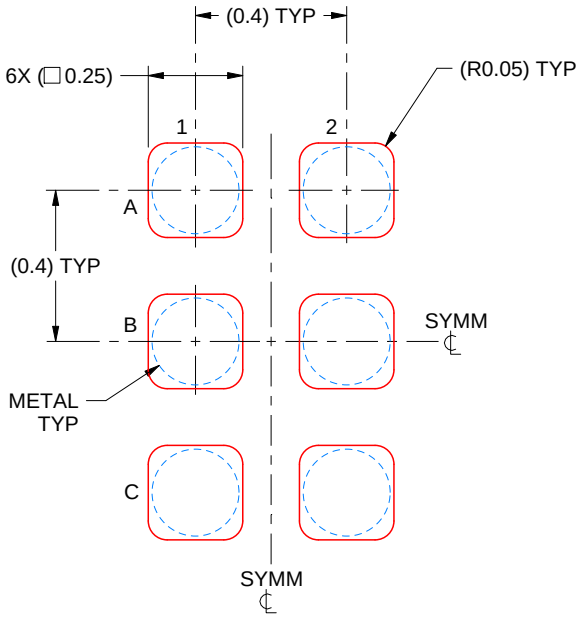
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

4223410/A 11/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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