

## bq3060 SBS 1.1-Compliant Gas Gauge and Protection With CEDV

### 1 Features

- Advanced CEDV (Compensated End-of-Discharge Voltage) Gauging
- Fully Integrated 2, 3, and 4 Series Li-Ion or Li-Polymer Cell Battery Pack Manager
- 8-Bit RISC CPU With Ultra-Low Power Modes
- Full Array of Programmable Protection Features
  - Voltage, Current, and Temperature
- SHA-1 Authentication
- Flexible Memory Architecture With Integrated Flash Memory
- Supports Two-Wire SMBus v1.1 Interface With High-speed 400kHz Programming Option
- P-CH High Side Protection FET Drive
- Low Power Consumption Sleep Mode: < 69  $\mu$ A
- High-Accuracy Analog Front End With Two Independent ADCs
  - High-Resolution, 15~22-bit Integrator for Coulomb Counting
  - 16-Bit Delta-Sigma ADC With a 16-Channel Multiplexer for Voltage, Current, and Temperature
- Ultra Compact Package: 24-Pin TSSOP PW

### 2 Applications

- Netbook and Notebook PCs
- Medical and Test Equipment
- Portable Instruments

### 3 Description

The Texas Instruments bq3060 Battery Manager is a fully integrated, single-chip, pack-based solution that provides a rich array of features for gas gauging, protection, and authentication for 2, 3, or 4 series cell Li-Ion battery packs. With a footprint of merely 7.8 mm  $\times$  6.4 mm in a compact 24-pin TSSOP package, the bq3060 maximizes functionality and safety while dramatically cutting the solution cost and size for smart batteries.

Using its integrated high-performance analog peripherals, the bq3060 measures and maintains an accurate record of available capacity, voltage, current, temperature, and other critical parameters in Li-Ion or Li-Polymer batteries, and reports the information to the system host controller over an SMBus 1.1-compatible interface.

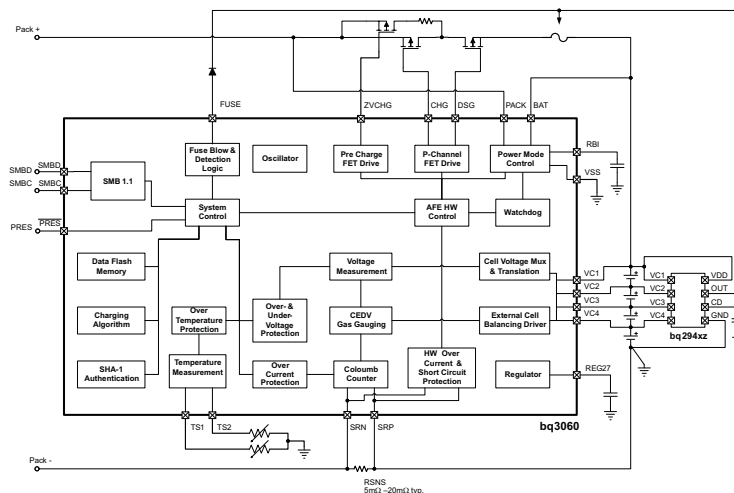
The bq3060 provides software-first level and second level safety protection on overvoltage, undervoltage, overtemperature, and overcharge, as well as hardware-overcurrent in discharge, short circuit in charge, and discharge protection.

#### Device Information<sup>(1)</sup>

| PART NUMBER | PACKAGE    | BODY SIZE (NOM)        |
|-------------|------------|------------------------|
| bq3060      | TSSOP (24) | 4.4 mm $\times$ 7.8 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### System Partitioning Diagram



## Table of Contents

|                                                |          |                                                                 |           |
|------------------------------------------------|----------|-----------------------------------------------------------------|-----------|
| <b>1 Features</b> .....                        | <b>1</b> | <b>7 Detailed Description</b> .....                             | <b>11</b> |
| <b>2 Applications</b> .....                    | <b>1</b> | 7.1 Feature Description.....                                    | 11        |
| <b>3 Description</b> .....                     | <b>1</b> | 7.2 Device Functional Modes.....                                | 13        |
| <b>4 Revision History</b> .....                | <b>2</b> | <b>8 Device and Documentation Support</b> .....                 | <b>14</b> |
| <b>5 Pin Configuration and Functions</b> ..... | <b>3</b> | 8.1 Documentation Support .....                                 | 14        |
| <b>6 Specifications</b> .....                  | <b>4</b> | 8.2 Receiving Notification of Documentation Updates..           | 14        |
| 6.1 Absolute Maximum Ratings .....             | 4        | 8.3 Community Resources.....                                    | 14        |
| 6.2 ESD Ratings.....                           | 4        | 8.4 Trademarks .....                                            | 14        |
| 6.3 Recommended Operating Conditions.....      | 4        | 8.5 Electrostatic Discharge Caution .....                       | 14        |
| 6.4 Thermal Information .....                  | 5        | 8.6 Glossary .....                                              | 14        |
| 6.5 Electrical Characteristics.....            | 5        | <b>9 Mechanical, Packaging, and Orderable Information</b> ..... | <b>14</b> |

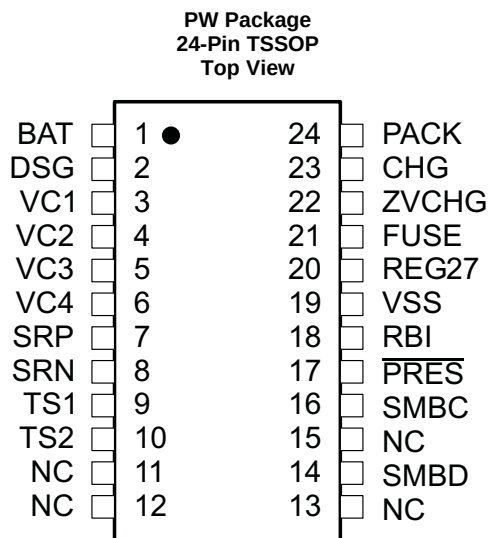
## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision A (November 2009) to Revision B                                                                                                                                                                                     | Page |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| • Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section..... | 1    |
| • Changed Device From: Production To: NRND.....                                                                                                                                                                                           | 1    |

| Changes from Original (March 2009) to Revision A           | Page |
|------------------------------------------------------------|------|
| • Changed Device From: Product Preview To: Production..... | 1    |

## 5 Pin Configuration and Functions



**Pin Functions**

| PIN                      |     | I/O    | DESCRIPTION                                                                                                                                                              |
|--------------------------|-----|--------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME                     | NO. |        |                                                                                                                                                                          |
| BAT                      | 1   | P      | Power input from battery                                                                                                                                                 |
| DSG                      | 2   | O      | P-CH FET Drive controlling discharge                                                                                                                                     |
| VC1                      | 3   | IA     | Sense voltage input terminal and external cell balancing drive output for most positive cell, and battery stack measurement input.                                       |
| VC2                      | 4   | IA     | Sense voltage input terminal and external cell balancing drive output for second most positive cell.                                                                     |
| VC3                      | 5   | IA     | Sense voltage input terminal and external cell balancing drive output for third most positive cell.                                                                      |
| VC4                      | 6   | IA     | Sense voltage input terminal and external cell balancing drive output for least positive cell.                                                                           |
| SRP                      | 7   | IA     | Analog input pin connected to the internal coulomb-counter peripheral for integrating a small voltage between SRP and SRN where SRP is the top of the sense resistor.    |
| SRN                      | 8   | IA     | Analog input pin connected to the internal coulomb-counter peripheral for integrating a small voltage between SRP and SRN where SRN is the bottom of the sense resistor. |
| TS1                      | 9   | I/O,IA | Thermistor input TS1                                                                                                                                                     |
| TS2                      | 10  | I/O,IA | Thermistor input TS2                                                                                                                                                     |
| NC                       | 11  | —      | Keep this pin floating                                                                                                                                                   |
| NC                       | 12  | —      | Keep this pin floating                                                                                                                                                   |
| NC                       | 13  | —      | Keep this pin floating                                                                                                                                                   |
| SMBD                     | 14  | I/OD   | SMBus data pin                                                                                                                                                           |
| NC                       | 15  | —      | Keep this pin floating                                                                                                                                                   |
| SMBC                     | 16  | I/OD   | SMBus clock pin                                                                                                                                                          |
| $\overline{\text{PRES}}$ | 17  | I/OD   | Active low input to sense system insertion and typically requires additional ESD protection                                                                              |
| RBI                      | 18  | P      | RAM backup pin to provide backup potential to the internal DATA RAM if power is momentarily lost by using a capacitor attached between RBI and VSS                       |
| VSS                      | 19  | P      | Device ground                                                                                                                                                            |
| REG27                    | 20  | P      | Internal power supply 2.7V bias output                                                                                                                                   |
| FUSE                     | 21  | I/OD   | Push-pull fuse drive and secondary protector activation input sensing                                                                                                    |
| ZVCHG                    | 22  | O      | P-CH precharge FET Drive controlling pre-charge and zero-volt charge                                                                                                     |
| CHG                      | 23  | O      | P-CH FET Drive controlling charge                                                                                                                                        |
| PACK                     | 24  | P      | PACK positive terminal and alternative power source                                                                                                                      |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                   |                                              |                             | MIN                   | MAX                                             | UNIT |
|-------------------|----------------------------------------------|-----------------------------|-----------------------|-------------------------------------------------|------|
| V <sub>MAX</sub>  | Supply voltage range                         | PACK w.r.t. V <sub>SS</sub> | −0.3                  | 34                                              | V    |
| V <sub>IN</sub>   | Input voltage range                          | VC1, BAT                    | V <sub>VC2</sub> −0.3 | V <sub>VC2</sub> +8.5 or 34, whichever is lower | V    |
|                   |                                              | VC2                         | V <sub>VC3</sub> −0.3 | V <sub>VC3</sub> +8.5                           | V    |
|                   |                                              | VC3                         | V <sub>VC4</sub> −0.3 | V <sub>VC4</sub> +8.5                           | V    |
|                   |                                              | VC4                         | V <sub>SRP</sub> −0.3 | V <sub>SRP</sub> +8.5                           | V    |
|                   |                                              | SRP, SRN                    | −0.3                  | V <sub>REG27</sub>                              | V    |
|                   |                                              | SMBD, SMBC                  | −0.3                  | 6                                               | V    |
|                   |                                              | TS1, TS2, /PRES             | −0.3                  | V <sub>REG27</sub> + 0.3                        | V    |
| V <sub>O</sub>    | Output voltage range                         | CHG, DSG, ZVCHG, FUSE       | −0.3                  | BAT                                             | V    |
|                   |                                              | RBI, REG27                  | −0.3                  | 2.75                                            | V    |
| I <sub>SS</sub>   | Maximum combined sink current for input pins |                             |                       | 50                                              | mA   |
| T <sub>FUNC</sub> | Functional temperature                       |                             | −40                   | 110                                             | °C   |
| T <sub>STG</sub>  | Storage temperature                          |                             | −65                   | 150                                             | °C   |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

|                    |                         | VALUE                                                                          | UNIT  |
|--------------------|-------------------------|--------------------------------------------------------------------------------|-------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±2000 |
|                    |                         | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±500  |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±500 V may actually have higher performance.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                       |                                                             | MIN                                                     | TYP              | MAX                 | UNIT |
|-----------------------|-------------------------------------------------------------|---------------------------------------------------------|------------------|---------------------|------|
| Supply voltage        | PACK                                                        |                                                         |                  | 25                  | V    |
|                       | BAT                                                         | 3.8                                                     |                  | V <sub>VC2</sub> +5 |      |
| V <sub>STARTUP</sub>  | Start up voltage at PACK                                    |                                                         | 5.2              | 5.5                 | V    |
| V <sub>shutdown</sub> | V <sub>PACK</sub> or V <sub>BAT</sub> , whichever is higher | 3                                                       | 3.2              | 3.3                 | V    |
| V <sub>IN</sub>       | Input voltage range                                         | VC1, BAT                                                | V <sub>VC2</sub> | V <sub>VC2</sub> +5 | V    |
|                       |                                                             | VC2                                                     | V <sub>VC3</sub> | V <sub>VC3</sub> +5 |      |
|                       |                                                             | VC3                                                     | V <sub>VC4</sub> | V <sub>VC4</sub> +5 |      |
|                       |                                                             | VC4                                                     | V <sub>SRP</sub> | V <sub>SRP</sub> +5 |      |
|                       |                                                             | VC <sub>n</sub> – VC <sub>(n+1)</sub> , (n=1, 2, 3, 4 ) | 0                | 5                   |      |
|                       |                                                             | PACK                                                    |                  | 25                  |      |
|                       |                                                             | SRP to SRN                                              | −0.3             | 1                   | V    |
| C <sub>REG27</sub>    | External 2.7V REG capacitor                                 | 1                                                       |                  |                     | μF   |
| T <sub>OPR</sub>      | Operating temperature                                       | −40                                                     |                  | 85                  | °C   |

## 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | bq3060     | UNIT |
|-------------------------------|----------------------------------------------|------------|------|
|                               |                                              | PW (TSSOP) |      |
|                               |                                              | 24 PINS    |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 83.6       | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 16.5       | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 39.4       | °C/W |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 0.4        | °C/W |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 38.8       | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | –          | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

Typical values stated where T<sub>A</sub> = 25°C and V<sub>BAT</sub> = V<sub>PACK</sub> = 14.4 V, Minimum/Maximum values stated where T<sub>A</sub> = –40°C to 85°C and V<sub>BAT</sub> = V<sub>PACK</sub> = 3.8 V to 25 V (unless otherwise noted)

| PARAMETER                   | TEST CONDITION                           | MIN                                                               | TYP                     | MAX                   | UNIT |
|-----------------------------|------------------------------------------|-------------------------------------------------------------------|-------------------------|-----------------------|------|
| <b>GENERAL PURPOSE I/O</b>  |                                          |                                                                   |                         |                       |      |
| V <sub>IH</sub>             | High-level input voltage                 | /PRES, SMBD, SMBC, TS1, TS2                                       | 2                       |                       | V    |
| V <sub>IL</sub>             | Low-level input voltage                  | /PRES, SMBD, SMBC, TS1, TS2                                       |                         | 0.8                   | V    |
| V <sub>OH</sub>             | Output voltage high                      | /PRES, SMBD, SMBC, TS1, TS2, I <sub>L</sub> = –0.5 mA             | V <sub>REG27</sub> –0.5 |                       | V    |
| V <sub>OH(FUSE)</sub>       | High level fuse output                   | V <sub>BAT</sub> = 3.8 V to 9 V, C <sub>L</sub> = 1 nF            | 3                       | V <sub>BAT</sub> –0.3 | 8.6  |
|                             |                                          | V <sub>BAT</sub> = 9 V to 25 V, C <sub>L</sub> = 1nF              | 7.5                     | 8                     | 9    |
| t <sub>R(FUSE)</sub>        | FUSE output rise time                    | C <sub>L</sub> = 1 nF,<br>V <sub>OH(FUSE)</sub> = 0 V to 5 V      |                         | 10                    | μs   |
| Z <sub>O(FUSE)</sub>        | FUSE output impedance                    |                                                                   | 2                       | 6                     | kΩ   |
| V <sub>FUSE_DET</sub>       | FUSE detect input voltage                |                                                                   | 0.8                     | 2                     | 3.2  |
| V <sub>OL</sub>             | Low-level output voltage                 | /PRES, SMBD, SMBC, TS1, TS2, I <sub>L</sub> = 7 mA                |                         | 0.4                   | V    |
| C <sub>IN</sub>             | Input capacitance                        |                                                                   | 5                       |                       | pF   |
| I <sub>lkg</sub>            | Input leakage current                    | /PRES, SMBD, SMBC, TS1, TS2<br>SMBD and SMBC pull-down disabled   |                         | 1                     | μA   |
| R <sub>PD(SMBx)</sub>       | SMBD and SMBC pull-down                  | T <sub>A</sub> = –40°C to 100°C                                   | 600                     | 950                   | 1300 |
| R <sub>PAD</sub>            | Pad resistance                           | TS1, TS2                                                          | 87                      | 110                   | Ω    |
| <b>SUPPLY CURRENT</b>       |                                          |                                                                   |                         |                       |      |
| I <sub>CC</sub>             | Normal mode                              | Firmware running, no flash writes                                 | 441                     |                       | μA   |
| I <sub>SLEEP</sub>          | Sleep mode                               | Discharge FET ON, Charge FET ON<br>([NR]=1, [NRCHG]=1)            | 69                      |                       | μA   |
|                             |                                          | Discharge FET ON, Charge FET OFF<br>([NR]=1, [NRCHG]=0)           | 66                      |                       |      |
|                             |                                          | Discharge FET OFF, Charge FET OFF<br>([NR]=0, System not present) | 61                      |                       |      |
| I <sub>SHUTDOWN</sub>       | Shutdown mode                            | T <sub>A</sub> = –40°C to 110°C                                   | 0.5                     | 1                     | μA   |
| <b>REG27 POWER ON RESET</b> |                                          |                                                                   |                         |                       |      |
| V <sub>REG27IT–</sub>       | Negative-going voltage input             | At REG27                                                          | 2.22                    | 2.35                  | 2.34 |
| V <sub>REG27IT+</sub>       | Positive-going voltage input             | At REG27                                                          | 2.25                    | 2.5                   | 2.6  |
| <b>INTERNAL LDO</b>         |                                          |                                                                   |                         |                       |      |
| V <sub>REG</sub>            | Regulator output voltage                 | I <sub>REG27</sub> = 10 mA; T <sub>A</sub> = –40°C to 85°C        | 2.5                     | 2.7                   | 2.75 |
| ΔV <sub>(REGTEMP)</sub>     | Regulator output change with temperature | I <sub>REG</sub> = 10 mA; T <sub>A</sub> = –40°C to 85°C          | ±0.5%                   |                       |      |
| ΔV <sub>(REGLINE)</sub>     | Line regulation                          | I <sub>REG</sub> = 10 mA                                          | ±2                      | ±4                    | mV   |
| ΔV <sub>(REGLOAD)</sub>     | Load regulation                          | I <sub>REG</sub> = 0.2 to 10 mA                                   | ±20                     | ±40                   | mV   |

## Electrical Characteristics (continued)

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{BAT} = V_{PACK} = 14.4\text{ V}$ , Minimum/Maximum values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{BAT} = V_{PACK} = 3.8\text{ V}$  to  $25\text{ V}$  (unless otherwise noted)

| PARAMETER                   |                                                         | TEST CONDITION                                                                      | MIN   | TYP    | MAX                                | UNIT   |
|-----------------------------|---------------------------------------------------------|-------------------------------------------------------------------------------------|-------|--------|------------------------------------|--------|
| I <sub>(REGMAX)</sub>       | Current limit                                           |                                                                                     | 25    |        | 50                                 | mA     |
| SRx WAKE FROM SLEEP         |                                                         |                                                                                     |       |        |                                    |        |
| V <sub>WAKE_ACR</sub>       | Accuracy of V <sub>WAKE</sub>                           | V <sub>WAKE</sub> = 1.2 mV                                                          | 0.2   | 1.2    | 2                                  | mV     |
|                             |                                                         | V <sub>WAKE</sub> = 2.4 mV                                                          | 0.4   | 2.4    | 3.6                                |        |
|                             |                                                         | V <sub>WAKE</sub> = 5 mV                                                            | 2     | 5      | 6.8                                |        |
|                             |                                                         | V <sub>WAKE</sub> = 10 mV                                                           | 5.3   | 10     | 13                                 |        |
| V <sub>WAKE_TCO</sub>       | Temperature drift of V <sub>WAKE</sub> accuracy         |                                                                                     |       | 0.5    |                                    | %/°C   |
| t <sub>WAKE</sub>           | Time from application of current and wake of bq3060     |                                                                                     |       | 0.2    | 1                                  | ms     |
| COULOMB COUNTER             |                                                         |                                                                                     |       |        |                                    |        |
|                             | Input voltage range                                     |                                                                                     | −0.20 |        | 0.25                               | V      |
|                             | Conversion time                                         | Single conversion                                                                   |       | 250    |                                    | ms     |
|                             | Effective resolution                                    | Single conversion                                                                   | 15    |        |                                    | Bits   |
|                             | Integral nonlinearity                                   | T <sub>A</sub> = −25°C to 85°C                                                      |       | ±0.007 | ±0.034                             | %FSR   |
|                             | Offset error <sup>(1)</sup>                             | T <sub>A</sub> = −25°C to 85°C                                                      |       | 10     |                                    | μV     |
|                             | Offset error drift                                      |                                                                                     |       | 0.3    | 0.5                                | μV/°C  |
|                             | Full-scale error <sup>(2)</sup>                         |                                                                                     | −0.8% | 0.2%   | 0.8%                               |        |
|                             | Full-scale error drift                                  |                                                                                     |       |        | 150                                | PPM/°C |
|                             | Effective input resistance                              |                                                                                     | 2.5   |        |                                    | MΩ     |
| ADC                         |                                                         |                                                                                     |       |        |                                    |        |
|                             | Input voltage range                                     |                                                                                     | −0.2  |        | 0.8×V <sub>RE</sub> <sub>G27</sub> | V      |
|                             | Conversion time                                         |                                                                                     |       | 31.5   |                                    | ms     |
|                             | Resolution (no missing codes)                           |                                                                                     | 16    |        |                                    | Bits   |
|                             | Effective resolution                                    |                                                                                     | 14    | 15     |                                    | Bits   |
|                             | Integral nonlinearity                                   |                                                                                     |       |        | ±0.020                             | %FSR   |
|                             | Offset error <sup>(3)</sup>                             |                                                                                     |       | 70     | 160                                | M μV   |
|                             | Offset error drift                                      |                                                                                     |       | 1      |                                    | μV/°C  |
|                             | Full-scale error                                        | V <sub>IN</sub> = 1 V                                                               | −0.8% | ±0.2%  | 0.4%                               |        |
|                             | Full −scale error drift                                 |                                                                                     |       |        | 150                                | PPM/°C |
|                             | Effective input resistance                              |                                                                                     | 8     |        |                                    | MΩ     |
| EXTERNAL CELL BALANCE DRIVE |                                                         |                                                                                     |       |        |                                    |        |
| R <sub>BAL_drive</sub>      | Internal pull-down resistance for external cell balance | Cell balance ON for VC1, V <sub>CI</sub> -V <sub>CI</sub> +1 = 4 V, where i = 1~4   |       | 5.7    |                                    | kΩ     |
|                             |                                                         | Cell balance ON for VC2, V <sub>CI</sub> -V <sub>CI</sub> +1 = 4 V, where = i = 1~4 |       | 3.7    |                                    |        |
|                             |                                                         | Cell balance ON for VC3, V <sub>CI</sub> -V <sub>CI</sub> +1 = 4 V, where = i = 1~4 |       | 1.75   |                                    |        |
|                             |                                                         | Cell balance ON for VC4, V <sub>CI</sub> -V <sub>CI</sub> +1 = 4 V, where = i = 1~4 |       | 0.85   |                                    |        |
| CELL VOLTAGE MONITOR        |                                                         |                                                                                     |       |        |                                    |        |
|                             | CELL Voltage Measurement Accuracy <sup>(4)</sup>        | T <sub>A</sub> = −10°C to 60°C                                                      |       | ±10    | ±20                                | mV     |
|                             |                                                         | T <sub>A</sub> = −40°C to 85°C                                                      |       | ±10    | ±35                                |        |

(1) Post Calibration Performance

(2) Uncalibrated performance. This gain error can be eliminated with external calibration.

(3) Channel to channel offset

(4) This is the performance expected for non-calibrated device.

## Electrical Characteristics (continued)

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{BAT} = V_{PACK} = 14.4\text{ V}$ , Minimum/Maximum values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{BAT} = V_{PACK} = 3.8\text{ V}$  to  $25\text{ V}$  (unless otherwise noted)

| PARAMETER                                |                                                | TEST CONDITION                                                                                                         | MIN   | TYP    | MAX  | UNIT   |
|------------------------------------------|------------------------------------------------|------------------------------------------------------------------------------------------------------------------------|-------|--------|------|--------|
| INTERNAL TEMPERATURE SENSOR              |                                                |                                                                                                                        |       |        |      |        |
| T <sub>(TEMP)</sub>                      | Temperature sensor accuracy                    |                                                                                                                        |       | ±3%    |      | °C     |
| THERMISTOR MEASUREMENT SUPPORT           |                                                |                                                                                                                        |       |        |      |        |
| R <sub>ERR</sub>                         | Internal resistor drift                        |                                                                                                                        |       | −230   |      | ppm/°C |
| R                                        | Internal resistor                              | TS1, TS2                                                                                                               |       | 17     | 20   | kΩ     |
| INTERNAL THERMAL SHUTDOWN <sup>(5)</sup> |                                                |                                                                                                                        |       |        |      |        |
| T <sub>MAX</sub>                         | Maximum REG27 temperature                      |                                                                                                                        | 125   |        | 175  | °C     |
| T <sub>RECOVER</sub>                     | Recovery hysteresis temperature                |                                                                                                                        |       | 10     |      | °C     |
| HIGH FREQUENCY OSCILLATOR                |                                                |                                                                                                                        |       |        |      |        |
| f <sub>(OSC)</sub>                       | Operating frequency of CPU clock               |                                                                                                                        |       | 2.097  |      | MHz    |
| f <sub>(EIO)</sub>                       | Frequency error <sup>(6)</sup>                 | T <sub>A</sub> = −20°C to 70°C                                                                                         | −2%   | ±0.25% | 2%   |        |
|                                          |                                                | T <sub>A</sub> = −40°C to 85°C                                                                                         | −3%   | ±0.25% | 3%   |        |
| t <sub>(SXO)</sub>                       | Start-up time <sup>(7)</sup>                   | T <sub>A</sub> = −25°C to 85°C                                                                                         |       | 3      | 6    | ms     |
| LOW FREQUENCY OSCILLATOR                 |                                                |                                                                                                                        |       |        |      |        |
| f <sub>(LOSC)</sub>                      | Operating frequency                            |                                                                                                                        |       | 32.768 |      | MHz    |
| f <sub>(LEIO)</sub>                      | Frequency error <sup>(6)</sup>                 | T <sub>A</sub> = −20°C to 70°C                                                                                         | −1.5% | ±0.25% | 1.5% |        |
|                                          |                                                | T <sub>A</sub> = −40°C to 85°C                                                                                         | −2.5% | ±0.25% | 2.5% |        |
| t <sub>(LSXO)</sub>                      | Start-up time <sup>(8)</sup>                   | T <sub>A</sub> = −25°C to 85°C                                                                                         |       |        | 100  | ms     |
| FLASH <sup>(9)</sup>                     |                                                |                                                                                                                        |       |        |      |        |
|                                          | Data retention                                 |                                                                                                                        | 10    |        |      | Years  |
|                                          | Flash programming write-cycles                 |                                                                                                                        | 20k   |        |      | Cycles |
| t <sub>(ROWPROG)</sub>                   | Row programming time                           |                                                                                                                        |       |        | 2    | ms     |
| t <sub>(MASSERASE)</sub>                 | Mass-erase time                                |                                                                                                                        |       |        | 250  | ms     |
| t <sub>(PAGEERASE)</sub>                 | Page-erase time                                |                                                                                                                        |       |        | 25   | ms     |
| I <sub>CC(PROG)</sub>                    | Flash-write supply current                     |                                                                                                                        |       | 4      | 6    | mA     |
| I <sub>CC(ERASE)</sub>                   | Flash-erase supply current                     | T <sub>A</sub> = −40°C to 0°C                                                                                          |       | 8      | 22   | mA     |
|                                          |                                                | T <sub>A</sub> = 0°C to 85°C                                                                                           |       | 3      | 15   |        |
| RAM BACKUP                               |                                                |                                                                                                                        |       |        |      |        |
| I <sub>(RBI)</sub>                       | RBI data-retention input current               | V <sub>RBI</sub> > V <sub>(RBI)MIN</sub> , V <sub>REG27</sub> < V <sub>REG27IT-</sub> , T <sub>A</sub> = 70°C to 110°C |       | 20     | 1500 | nA     |
|                                          |                                                | V <sub>RBI</sub> > V <sub>(RBI)MIN</sub> , V <sub>REG27</sub> < V <sub>REG27IT-</sub> , T <sub>A</sub> = −40°C to 70°C |       |        | 500  |        |
| V <sub>(RBI)</sub>                       | RBI data-retention voltage <sup>(9)</sup>      |                                                                                                                        | 1     |        |      | V      |
| CURRENT PROTECTION THRESHOLDS            |                                                |                                                                                                                        |       |        |      |        |
| V <sub>(OCD)</sub>                       | OCD detection threshold voltage range, typical | RSNS = 0; RSNS is set in STATE_CTL register                                                                            | 50    |        | 200  | mV     |
|                                          |                                                | RSNS = 1; RSNS is set in STATE_CTL register                                                                            | 25    |        | 100  |        |

(5) Parameters assured by design. Not production tested.

(6) The frequency drift is included and measured from the trimmed frequency at  $V_{BAT} = V_{PACK} = 14.4\text{ V}$ ,  $T_A = 25^\circ\text{C}$

(7) The startup time is defined as the time it takes for the oscillator output frequency to be  $\pm 3\%$  when the device is already powered.

(8) The startup time is defined as the time it takes for the oscillator output frequency to be  $\pm 3\%$ .

(9) Specified by design. Not production tested

## Electrical Characteristics (continued)

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{BAT} = V_{PACK} = 14.4\text{ V}$ , Minimum/Maximum values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{BAT} = V_{PACK} = 3.8\text{ V}$  to  $25\text{ V}$  (unless otherwise noted)

| PARAMETER                 |                                                   | TEST CONDITION                                                                                                                                                 | MIN      | TYP | MAX | UNIT    |
|---------------------------|---------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|-----|-----|---------|
| $\Delta V_{(OCDT)}$       | OCD detection threshold voltage program step      | RSNS = 0; RSNS is set in STATE_CTL register                                                                                                                    | 10       |     |     | mV      |
|                           |                                                   | RSNS = 1; RSNS is set in STATE_CTL register                                                                                                                    | 5        |     |     |         |
| $V_{(SCCT)}$              | SCC detection threshold voltage range, typical    | RSNS = 0; RSNS is set in STATE_CTL register                                                                                                                    | −100−300 |     |     | mV      |
|                           |                                                   | RSNS = 1; RSNS is set in STATE_CTL register                                                                                                                    | −50−225  |     |     |         |
| $\Delta V_{(SCCT)}$       | SCC detection threshold voltage program step      | RSNS = 0; RSNS is set in STATE_CTL register                                                                                                                    | −50      |     |     | mV      |
|                           |                                                   | RSNS = 1; RSNS is set in STATE_CTL register                                                                                                                    | −25      |     |     |         |
| $V_{(SCDT)}$              | SCD detection threshold voltage range, typical    | RSNS = 0; RSNS is set in STATE_CTL register                                                                                                                    | 100450   |     |     | mV      |
|                           |                                                   | RSNS = 1; RSNS is set in STATE_CTL register                                                                                                                    | 50225    |     |     |         |
| $\Delta V_{(SCDT)}$       | SCD detection threshold voltage program step      | RSNS = 0; RSNS is set in STATE_CTL register                                                                                                                    | 50       |     |     | mV      |
|                           |                                                   | RSNS = 1; RSNS is set in STATE_CTL register                                                                                                                    | 25       |     |     |         |
| $V_{(OFFSET)}$            | SCD, SCC and OCD offset                           |                                                                                                                                                                | −1010    |     |     | mV      |
| $V_{(Scale\_Err)}$        | SCD, SCC and OCD scale error                      |                                                                                                                                                                | −10%10%  |     |     |         |
| CURRENT PROTECTION TIMING |                                                   |                                                                                                                                                                |          |     |     |         |
| $t_{(OCDD)}$              | Overcurrent in discharge delay                    |                                                                                                                                                                | 131      |     |     | ms      |
| $t_{(OCDD\_STEP)}$        | OCDD step options                                 |                                                                                                                                                                | 2        |     |     | ms      |
| $t_{(SCDD)}$              | Short circuit in discharge delay                  | AFE.STATE_CNTL[SCDDx2] = 0                                                                                                                                     | 0915     |     |     | $\mu$ s |
|                           |                                                   | AFE.STATE_CNTL[SCDDx2] = 1                                                                                                                                     | 01830    |     |     |         |
| $t_{(SCDD\_STEP)}$        | SCDD step options                                 | AFE.STATE_CNTL[SCDDx2] = 0                                                                                                                                     | 61       |     |     | $\mu$ s |
|                           |                                                   | AFE.STATE_CNTL[SCDDx2] = 1                                                                                                                                     | 122      |     |     |         |
| $t_{(SCCD)}$              | Short circuit in charge delay                     |                                                                                                                                                                | 0915     |     |     | $\mu$ s |
| $t_{(SCCD\_STEP)}$        | SCCD step options                                 |                                                                                                                                                                | 61       |     |     | $\mu$ s |
| $t_{(DETECT)}$            | Current fault detect time                         | $V_{SRP-SRN} = V_{THRESH} + 12.5\text{ mV}$ ,<br>$T_A = -40^{\circ}\text{C}$ to $85^{\circ}\text{C}$                                                           | 35160    |     |     | $\mu$ s |
| $t_{ACC}$                 | Overcurrent and short circuit delay time accuracy | Accuracy of typical delay time with WDI active                                                                                                                 | −20%20%  |     |     |         |
|                           |                                                   | Accuracy of typical delay time with no WDI input                                                                                                               | −50%50%  |     |     |         |
| P-CH FET DRIVE            |                                                   |                                                                                                                                                                |          |     |     |         |
| $V_{(FETON)}$             | Output voltage, charge and discharge FETs on      | $V_{(FETONDSG)} = V_{(BAT)} - V_{(DSG)}$ , $R_{GS} = 1\text{M}\Omega$ ,<br>$T_A = -40^{\circ}\text{C}$ to $110^{\circ}\text{C}$ , $BAT = 20\text{ V}^{(10)}$   | 12       | 15  | 18  | V       |
|                           |                                                   | $V_{(FETONCHG)} = V_{(PACK)} - V_{(CHG)}$ , $R_{GS} = 1\text{M}\Omega$ ,<br>$T_A = -40^{\circ}\text{C}$ to $110^{\circ}\text{C}$ , $PACK = 20\text{ V}^{(10)}$ | 12       | 15  | 18  |         |
| $V_{(FETOFF)}$            | Output voltage, charge and discharge FETs off     | $V_{(FETOFFDSG)} = V_{(BAT)} - V_{(DSG)}$ ,<br>$T_A = -40^{\circ}\text{C}$ to $110^{\circ}\text{C}$ , $BAT = 16\text{ V}$                                      | 0.2      |     |     | V       |
|                           |                                                   | $V_{(FETOFFCHG)} = V_{(PACK)} - V_{(CHG)}$ ,<br>$T_A = -40^{\circ}\text{C}$ to $110^{\circ}\text{C}$ , $PACK = 16\text{ V}$                                    | 0.2      |     |     |         |
| $t_r$                     | Rise time                                         | $C_L = 4700\text{ pF}$ ; $V_{DSG}$ : 10% to 90%                                                                                                                | 70200    |     |     | $\mu$ s |
|                           |                                                   | $C_L = 4700\text{ pF}$ ; $V_{CHG}$ : 10% to 90%                                                                                                                | 70200    |     |     |         |

(10) For a  $V_{BAT}$  or  $V_{PACK}$  input range of 3.8 V to 25 V, MIN  $V_{(FETON)}$  voltage is 12 V or  $V_{(BAT)} - 1\text{ V}$ , whichever is less.



## Electrical Characteristics (continued)

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{BAT} = V_{PACK} = 14.4\text{ V}$ , Minimum/Maximum values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{BAT} = V_{PACK} = 3.8\text{ V}$  to  $25\text{ V}$  (unless otherwise noted)

| PARAMETER                  |                                                                                                           | TEST CONDITION                                                                     | MIN | TYP  | MAX      | UNIT |
|----------------------------|-----------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------|-----|------|----------|------|
| t <sub>f</sub>             | Fall time                                                                                                 | C <sub>L</sub> = 4700 pF; V <sub>DSG</sub> : 10% to 90%                            |     | 70   | 200      | μs   |
|                            |                                                                                                           | C <sub>L</sub> = 4700 pF; V <sub>CHG</sub> : 10% to 90%                            |     | 70   | 200      |      |
| PRE-CHARGE/ZVCHG FET DRIVE |                                                                                                           |                                                                                    |     |      |          |      |
| V <sub>(PreCHGON)</sub>    | V <sub>O(PreCHGON)</sub> = V <sub>(PACK)</sub> − V <sub>(ZVCHG)</sub> , pre-charge FET on <sup>(11)</sup> | R <sub>GS</sub> =1 MΩ, T <sub>A</sub> = −40°C to 110°C                             | 12  | 15   | 18       | V    |
| V <sub>(PreCHGOFF)</sub>   | Output voltage, pre-charge FET off <sup>(11)</sup>                                                        | R <sub>GS</sub> =1 MΩ, T <sub>A</sub> = −40°C to 110°C                             |     |      | VBAT−0.5 | V    |
| t <sub>r</sub>             | Rise time                                                                                                 | C <sub>L</sub> = 4700 pF, R <sub>G</sub> = 5.1 kΩ, V <sub>ZVCHG</sub> : 10% to 90% |     | 80   | 200      | μs   |
| t <sub>f</sub>             | Fall time                                                                                                 | C <sub>L</sub> = 4700 pF, R <sub>G</sub> = 5.1 kΩ, V <sub>ZVCHG</sub> : 90% to 10% |     | 1.7  |          | ms   |
| SMBus                      |                                                                                                           |                                                                                    |     |      |          |      |
| f <sub>SMB</sub>           | SMBus operating frequency                                                                                 | Slave mode, SMBC 50% duty cycle                                                    | 10  |      | 100      | kHz  |
| f <sub>MAS</sub>           | SMBus master clock frequency                                                                              | Master mode, no clock low slave extend                                             |     | 51.2 |          | kHz  |
| t <sub>BUF</sub>           | Bus free time between start and stop                                                                      |                                                                                    | 4.7 |      |          | μs   |
| t <sub>HD:STA</sub>        | Hold time after (repeated) start                                                                          |                                                                                    | 4   |      |          | μs   |
| t <sub>SU:STA</sub>        | Repeated start setup time                                                                                 |                                                                                    | 4.7 |      |          | μs   |
| t <sub>SU:STO</sub>        | Stop setup time                                                                                           |                                                                                    | 4   |      |          | μs   |
| t <sub>HD:DAT</sub>        | Data hold time                                                                                            | Receive mode                                                                       | 0   |      |          | ns   |
|                            |                                                                                                           | Transmit mode                                                                      | 300 |      |          |      |
| t <sub>SU:DAT</sub>        | Data setup time                                                                                           |                                                                                    | 250 |      |          | ns   |
| t <sub>TIMEOUT</sub>       | Error signal/detect                                                                                       | See <sup>(12)</sup>                                                                | 25  |      | 35       | ms   |
| t <sub>LOW</sub>           | Clock low period                                                                                          |                                                                                    | 4.7 |      |          | μs   |
| t <sub>HIGH</sub>          | Clock high period                                                                                         | See <sup>(13)</sup>                                                                | 4   |      | 50       | μs   |
| t <sub>LOW:SEXT</sub>      | Cumulative clock low slave extend time                                                                    | See <sup>(14)</sup>                                                                |     |      | 10       | ms   |
| t <sub>LOW:MEXT</sub>      | Cumulative clock low master extend time                                                                   | See <sup>(15)</sup>                                                                |     |      | 300      | ns   |
| t <sub>F</sub>             | Clock/data fall time                                                                                      | See <sup>(16)</sup>                                                                |     |      | 300      | ns   |
| t <sub>R</sub>             | Clock/data rise time                                                                                      | See <sup>(17)</sup>                                                                |     |      | 1000     | ns   |
| SMBus XL                   |                                                                                                           |                                                                                    |     |      |          |      |
| f <sub>SMBXL</sub>         | SMBus XL operating frequency                                                                              | Slave mode                                                                         | 40  |      | 400      | kHz  |
| t <sub>BUF</sub>           | Bus free time between start and stop                                                                      |                                                                                    | 4.7 |      |          | μs   |
| t <sub>HD:STA</sub>        | Hold time after (repeated) start                                                                          |                                                                                    | 4   |      |          | μs   |
| t <sub>SU:STA</sub>        | Repeated start setup time                                                                                 |                                                                                    | 4.7 |      |          | μs   |
| t <sub>SU:STO</sub>        | Stop setup time                                                                                           |                                                                                    | 4   |      |          | μs   |

(11) For a  $V_{BAT}$  or  $V_{PACK}$  input range of 3.8 V to 25 V, MIN  $V_{(\text{PreCHGON})}$  voltage is 12 V or  $V_{(\text{BAT})} - 1\text{V}$ , whichever is less.

(12) The bq3060 times out when any clock low exceeds  $t_{\text{TIMEOUT}}$

(13)  $t_{\text{HIGH}}$ , Max, is the minimum bus idle time. SMBC = SMBD = 1 for  $t > 50\text{ }\mu\text{s}$  causes reset of any transaction involving bq3060 that is in progress. This specification is valid when the NC\_SMB control bit remains in the default cleared state (CLK[0]=0). If NC\_SMB is set then the timeout is disabled.

(14)  $t_{\text{LOW:SEXT}}$  is the cumulative time a slave device is allowed to extend the clock cycles in one message from initial start to the stop.

(15)  $t_{\text{LOW:MEXT}}$  is the cumulative time a master device is allowed to extend the clock cycles in one message from initial start to the stop.

(16) Rise time  $t_R = V_{\text{ILMAX}} - 0.15$  to  $(V_{\text{IHMIN}} + 0.15)$

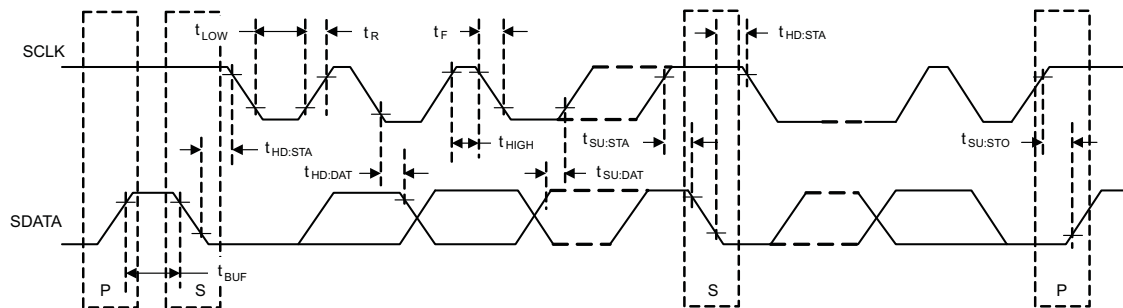
(17) Fall time  $t_F = 0.9V_{\text{DD}}$  to  $(V_{\text{ILMAX}} - 0.15)$

## Electrical Characteristics (continued)

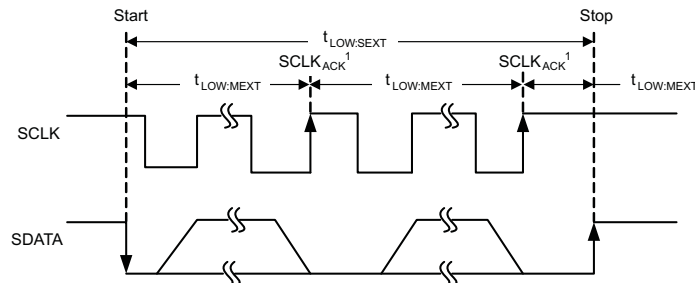
Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{BAT} = V_{PACK} = 14.4\text{ V}$ , Minimum/Maximum values stated where  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{BAT} = V_{PACK} = 3.8\text{ V}$  to  $25\text{ V}$  (unless otherwise noted)

| PARAMETER            | TEST CONDITION      | MIN      | TYP | MAX | UNIT          |
|----------------------|---------------------|----------|-----|-----|---------------|
| $t_{\text{TIMEOUT}}$ | Error signal/detect | See (12) |     | 35  | ms            |
| $t_{\text{LOW}}$     | Clock low period    | 1        |     | 1   | $\mu\text{s}$ |
| $t_{\text{HIGH}}$    | Clock high period   | 1        |     | 2   | $\mu\text{s}$ |

**Timing Measurement Intervals**



**$t_{\text{TIMEOUT}}$  Measurement Intervals**



(1)  $\text{SCLK}_{\text{ACK}}$  is the acknowledge-related clock pulse generated by the master.

## 7 Detailed Description

### 7.1 Feature Description

#### 7.1.1 Battery Parameter Measurements

The bq3060 uses an integrating delta-sigma analog-to-digital converter (ADC) for current measurement, and a second delta-sigma ADC for individual cell and battery voltage, and temperature measurement.

##### 7.1.1.1 Charge and Discharge Counting

The integrating delta-sigma ADC measures the charge/discharge flow of the battery by measuring the voltage drop across a small-value sense resistor between the SR1 and SR2 pins. The integrating ADC measures bipolar signals from -0.20 V to 0.25 V. The bq3060 detects charge activity when  $V_{SR} = V_{(SRP)} - V_{(SRN)}$  is positive, and discharge activity when  $V_{SR} = V_{(SRP)} - V_{(SRN)}$  is negative. The bq3060 continuously integrates the signal over time, using an internal counter. The fundamental rate of the counter is 0.65 nVh.

##### 7.1.1.2 Voltage

The bq3060 updates the individual series cell voltages at one second intervals. The internal ADC of the bq3060 measures the voltage, scales, and offsets, and calibrates it appropriately. To ensure an accurate differential voltage sensing, the IC ground should be connected directly to the most negative terminal of the battery stack, not to the positive side of the sense resistor. This minimizes the voltage drop across the PCB trace.

##### 7.1.1.3 Voltage Calibration and Accuracy

The bq3060 is calibrated for voltage prior to shipping from TI. The bq3060 voltage measurement signal chain (ADC, high voltage translation, circuit interconnect) will be calibrated for each cell. The external filter resistors, connected from each cell to the VCx input of the bq3060, are required to be 1kΩ. The accuracy of the factory-calibrated devices is +/- 10mV per cell at room temperature at 4V cell voltage. Without any customer voltage calibration, this is the level of accuracy expected as long as the filter resistor value is 1kΩ. If better voltage accuracy is desired, customer voltage calibration is required. An application note on calibrating and programming the bq3060 is available in the product web folder. See *Data Flash Programming and Calibrating the bq3060 Gas Gauge* (SLUA502) for more details.

##### 7.1.1.4 Current

The bq3060 uses the SRP and SRN inputs to measure and calculate the battery charge and discharge current using a 5 mΩ to 20 mΩ typ. sense resistor.

##### 7.1.1.5 Auto Calibration

The bq3060 can automatically calibrate its offset between the A to D converter and the output of the high voltage translation circuit. Also, the bq3060 provides an auto-calibration for the coulomb counter to cancel the voltage offset error across SRN and SRP for maximum charge measurement accuracy. The bq3060 performs auto-calibration when the SMBus lines stay low continuously for a minimum of 5 s.

##### 7.1.1.6 Temperature

The bq3060 has an internal temperature sensor and inputs for 2 external temperature sensor inputs TS1 and TS2 used in conjunction with two identical NTC thermistors (default is Semitec 103AT) to sense the battery cell temperature. The bq3060 can be configured to use internal or up to 2 external temperature sensors.

### 7.1.2 Primary (1st Level) Safety Features

The bq3060 supports a wide range of battery and system protection features that can easily be configured. The primary safety features include:

- Cell over/undervoltage protection
- Charge and discharge overcurrent
- Short circuit
- Charge and discharge overtemperature
- AFE Watchdog

## Feature Description (continued)

### 7.1.3 Secondary (2nd Level) Safety Features

The secondary safety features of the bq3060 can be used to indicate more serious faults via the FUSE (pin 21). This pin can be used to blow an in-line fuse to permanently disable the battery pack from charging and discharging. This pin is also used as an input to sense the state of the fuse. The secondary safety protection features include:

- Safety overvoltage
- Safety overcurrent in charge and discharge
- Safety overtemperature in charge and discharge
- Charge FET and Zero-Volt Charge FET fault
- Discharge FET fault
- Cell imbalance detection
- Fuse blow by a secondary voltage protection IC
- AFE register integrity fault (AFE\_P)
- AFE communication fault (AFE\_C)

### 7.1.4 Charge Control Features

The bq3060 charge control features include:

- Supports JEITA temperature ranges. Reports charging voltage and charging current according to the active temperature range.
- Handles more complex charging profiles. Allows for splitting the standard temperature range into 2 sub-ranges and allows for varying the charging current according to the cell voltage.
- Reports the appropriate charging current needed for constant current charging and the appropriate charging voltage needed for constant voltage charging to a smart charger using SMBus broadcasts.
- Reduce the charge difference of the battery cells in fully charged state of the battery pack gradually using a voltage-based cell balancing algorithm during charging. A voltage threshold can be set up for cell balancing to be active. This prevents fully charged cells from overcharging and causing excessive degradation and also increases the usable pack energy by preventing premature charge termination
- Supports pre-charging/zero-volt charging
- Supports charge inhibit and charge suspend if battery pack temperature is out of temperature range
- Reports charging fault and also indicate charge status via charge and discharge alarms.

### 7.1.5 Gas Gauging

The bq3060 uses advanced CEDV (Compensated End-of-Discharge Voltage) technology to measure and calculate the available capacity in battery cells. The bq3060 accumulates a measure of charge and discharge currents and compensates the charge current measurement for temperature and state-of-charge of the battery. The bq3060 estimates self-discharge of the battery and also adjusts the self-discharge estimation based on temperature.

See *bq3060 Technical Reference* ([SLUU319](#)) for further details.

### 7.1.6 Lifetime Data Logging Features

The bq3060 offers limited lifetime data logging for the following critical battery parameters for analysis purposes:

- Lifetime maximum temperature
- Lifetime minimum temperature
- Lifetime maximum battery cell voltage
- Lifetime minimum battery cell voltage

### 7.1.7 Authentication

The bq3060 supports authentication by the host using SHA-1.

## Feature Description (continued)

### 7.1.8 Configuration

#### 7.1.8.1 System Present Operation

The bq3060 checks the  $\overline{\text{PRES}}$  pin periodically (1 second). If  $\overline{\text{PRES}}$  input is pulled to ground by external system, the bq3060 detects the presence of the system.

#### 7.1.8.2 2-, 3-, or 4-Cell Configuration

In a 2-cell configuration, VC1 is shorted to VC2 and VC3. In a 3-cell configuration, VC1 is shorted to VC2.

#### 7.1.8.3 Cell Balance Control

If cell balancing is required, the bq3060 cell balance control allows a weak, internal pull-down for each VCx pin. The purpose of this weak pull-down is to enable an external FET for current bypass. Series resistors placed between the input VCx pins and the positive battery cell terminals control the VGS of the external FET. See *bq3060 Cell balancing using external MOSFET* (SLUA509) or *bq3060 Gas Gauge Circuit Design* (SLUA507) for more details.

### 7.1.9 Communications

The bq3060 uses SMBus v1.1 with Master Mode and package error checking (PEC) options per the SBS specification.

#### 7.1.9.1 SMBus On and Off State

The bq3060 detects an SMBus off state when SMBC and SMBD are logic-low for  $\geq 2$  seconds. Clearing this state requires either SMBC or SMBD to transition high. Within 1 ms, the communication bus is available.

#### 7.1.10 SBS Commands

See *bq3060 Technical Reference* (SLUU319) for further details.

## 7.2 Device Functional Modes

### 7.2.1 Power Modes

The bq3060 supports 3 different power modes to reduce power consumption:

- In Normal Mode, the bq3060 performs measurements, calculations, protection decisions and data updates in 1 second intervals. Between these intervals, the bq3060 is in a reduced power stage.
- In Sleep Mode, the bq3060 performs measurements, calculations, protection decisions and data update in adjustable time intervals. Between these intervals, the bq3060 is in a reduced power stage. The bq3060 has a wake function that enables exit from Sleep mode, when current flow or failure is detected.
- In Shutdown Mode the bq3060 is completely disabled.

## 8 Device and Documentation Support

### 8.1 Documentation Support

#### 8.1.1 Related Documentation

- [bq3060 Technical Reference](#) (SLUU319)
- [bq3060 Cell balancing using external MOSFET](#) (SLUA509)
- [bq3060 Gas Gauge Circuit Design](#) (SLUA507)
- [Data Flash Programming and Calibrating the bq3060 Gas Gauge](#) (SLUA502)

### 8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 8.3 Community Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 8.4 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

### 8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 8.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number     | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|---------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">BQ3060PW</a>  | Active        | Production           | TSSOP (PW)   24 | 60   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | 3060                |
| BQ3060PW.A                | Active        | Production           | TSSOP (PW)   24 | 60   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | 3060                |
| <a href="#">BQ3060PWR</a> | Active        | Production           | TSSOP (PW)   24 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | 3060                |
| BQ3060PWR.A               | Active        | Production           | TSSOP (PW)   24 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | 3060                |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device    | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| BQ3060PWR | TSSOP        | PW              | 24   | 2000 | 330.0              | 16.4               | 6.95    | 8.3     | 1.6     | 8.0     | 16.0   | Q1            |



## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

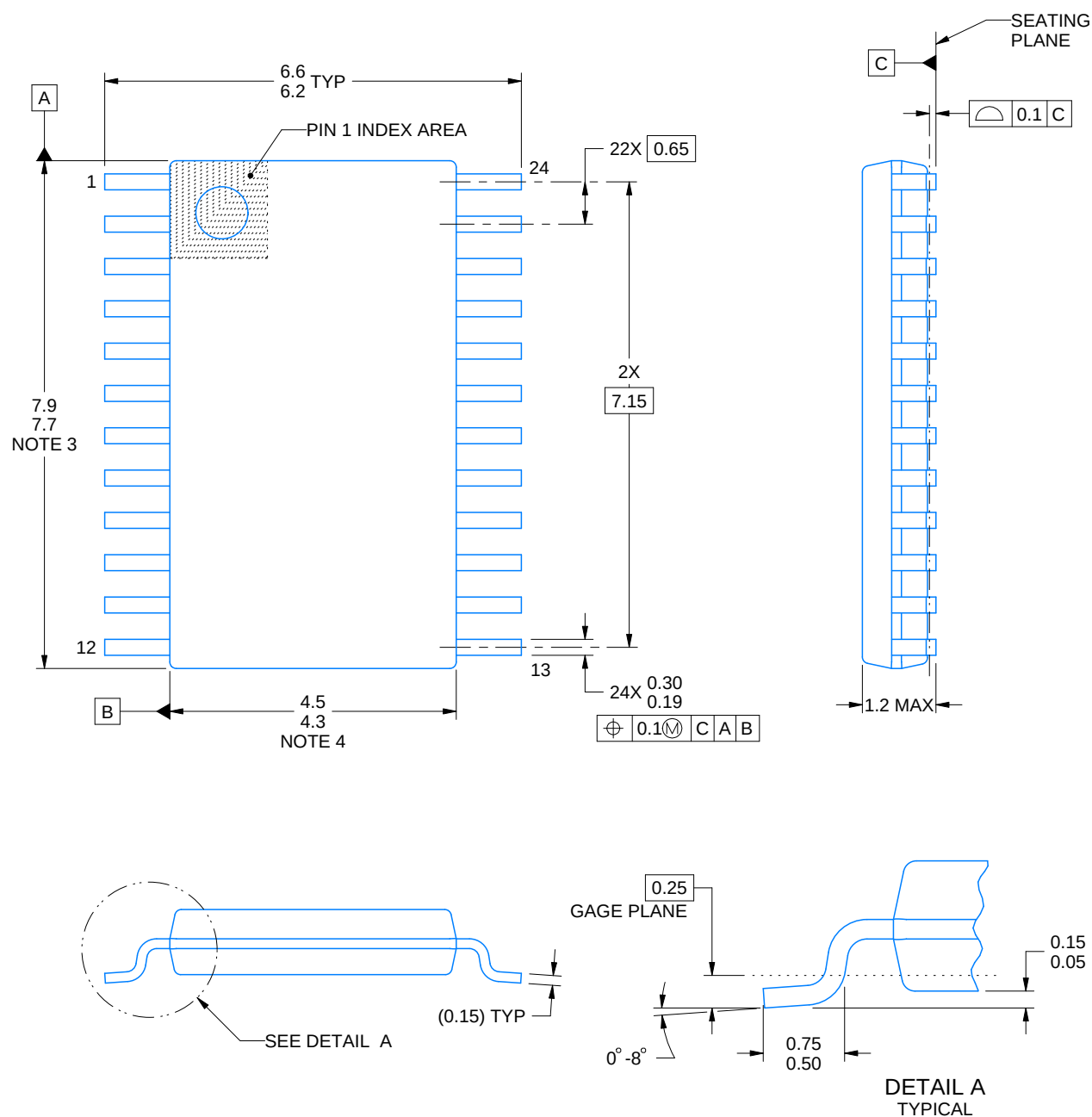
| Device    | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------|--------------|-----------------|------|------|-------------|------------|-------------|
| BQ3060PWR | TSSOP        | PW              | 24   | 2000 | 353.0       | 353.0      | 32.0        |



**PW0024A**

**TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



4220208/A 02/2017

NOTES:

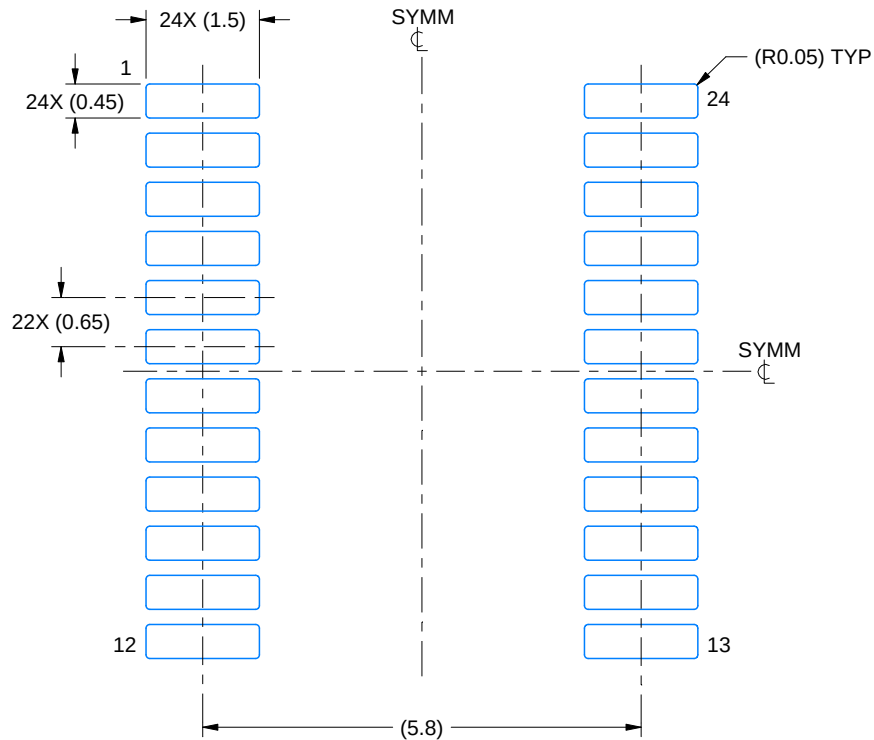
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

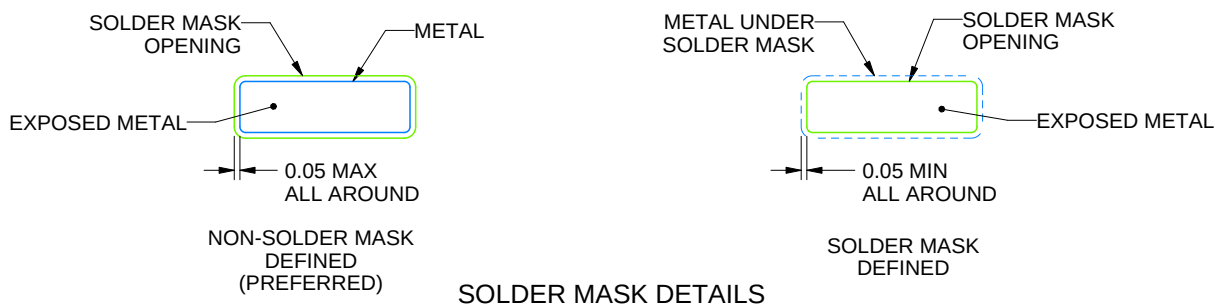
PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

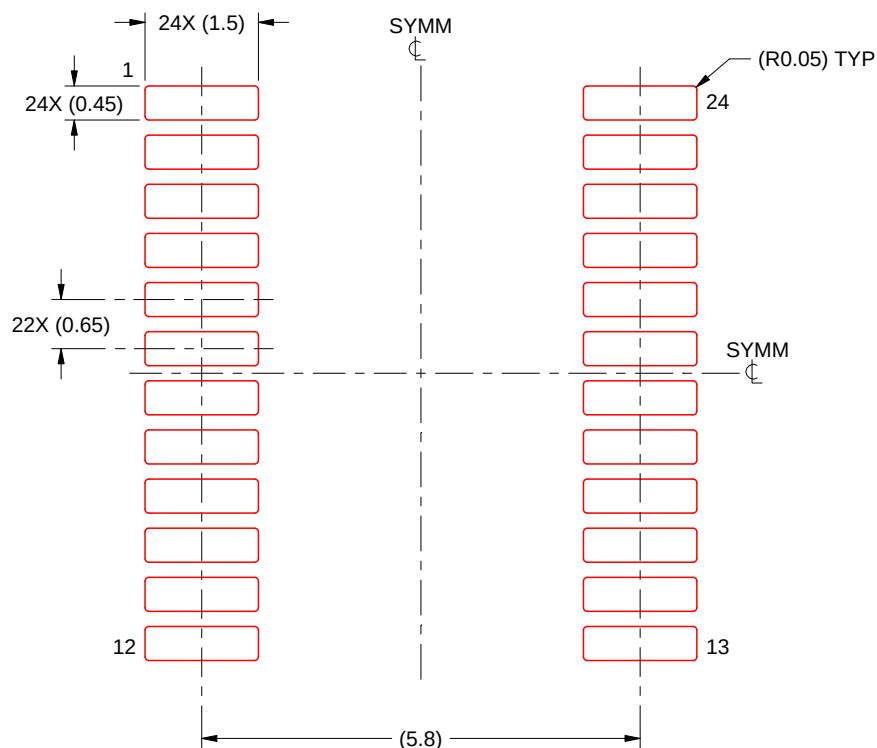
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025