



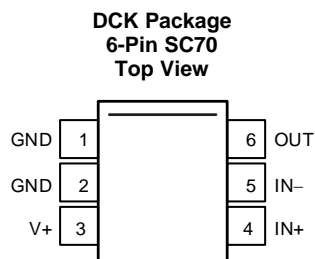
## Table of Contents

<b>1 Features</b> .....	<b>1</b>	7.4 Device Functional Modes.....	<b>8</b>
<b>2 Applications</b> .....	<b>1</b>	<b>8 Application and Implementation</b> .....	<b>9</b>
<b>3 Description</b> .....	<b>1</b>	8.1 Application Information.....	<b>9</b>
<b>4 Revision History</b> .....	<b>2</b>	8.2 Typical Application .....	<b>9</b>
<b>5 Pin Configuration and Functions</b> .....	<b>3</b>	<b>9 Power Supply Recommendations</b> .....	<b>11</b>
<b>6 Specifications</b> .....	<b>4</b>	<b>10 Layout</b> .....	<b>12</b>
6.1 Absolute Maximum Ratings .....	4	10.1 Layout Guidelines .....	12
6.2 ESD Ratings.....	4	10.2 Layout Example .....	12
6.3 Recommended Operating Conditions.....	4	<b>11 Device and Documentation Support</b> .....	<b>13</b>
6.4 Thermal Information .....	4	11.1 Documentation Support .....	13
6.5 Electrical Characteristics.....	5	11.2 Community Resources.....	13
6.6 Typical Characteristics .....	6	11.3 Trademarks .....	13
<b>7 Detailed Description</b> .....	<b>7</b>	11.4 Electrostatic Discharge Caution.....	13
7.1 Overview .....	7	11.5 Glossary .....	13
7.2 Functional Block Diagram .....	7	<b>12 Mechanical, Packaging, and Orderable</b>	
7.3 Feature Description.....	7	<b>Information</b> .....	<b>13</b>

## 4 Revision History

DATE	REVISION	NOTES
January 2016	*	Initial release.

## 5 Pin Configuration and Functions



### Pin Functions

PIN		I/O	DESCRIPTION
NAME	SC70		
GND	1, 2	Analog	Ground for the power-supply voltage rail
IN–	5	Analog input	Connect to load side of shunt resistor
IN+	4	Analog input	Connect to supply side of shunt resistor
OUT	6	Analog output	Output voltage
V+	3	Analog	Power supply, 2.7 V to 6 V

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Supply voltage			7	V
Analog inputs, $V_{IN+}$ , $V_{IN-}$ <sup>(2)</sup>	Differential ( $V_{IN+} - V_{IN-}$ )	-26	26	V
	Common-mode <sup>(3)</sup>	GND – 0.3	26	
Output <sup>(3)</sup>		GND – 0.3	(V+) + 0.3	V
Input current Into all pins <sup>(3)</sup>			5	mA
Temperature	Operating, $T_A$	-40	125	°C
	Junction, $T_J$		150	
	Storage, $T_{stg}$	-65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2)  $V_{IN+}$  and  $V_{IN-}$  are the voltages at the IN+ and IN– pins, respectively.
- (3) Input voltage at any pin can exceed the voltage shown if the current at that pin is limited to 5 mA.

### 6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000	
	Machine model (MM)	±200	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{CM}$	Common-mode input voltage		12		V
$V_S$	Operating supply voltage (applied to V+)		3.3		V
$T_A$	Operating free-air temperature	-40		105	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		bq500100	UNIT
		DCK (SC70)	
		6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	227.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	79.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	72.1	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	3.6	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	70.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

at  $T_A = 25^\circ\text{C}$ ,  $V_+ = 5\text{ V}$ ,  $V_{IN+} = 12\text{ V}$ , and  $V_{SENSE} = V_{IN+} - V_{IN-}$  (unless otherwise noted)

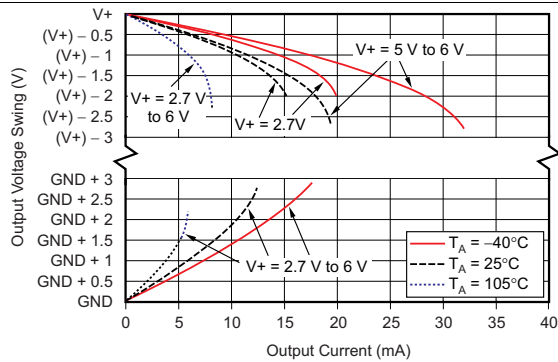
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
V <sub>CM</sub>	Common-mode input range	T <sub>A</sub> = −40°C to +105°C	0		20	V
CMR	Common-mode rejection	V <sub>IN+</sub> = 0 V to 20 V, T <sub>A</sub> = −40°C to +105°C	100	120		dB
V <sub>OS</sub>	Offset voltage, RTI <sup>(1)</sup>			±5	±150	μV
dV <sub>OS</sub> /dT	Offset voltage, RTI vs temperature	T <sub>A</sub> = −40°C to +105°C		0.1	0.5	μV/°C
PSR	Power-supply rejection	V+ = 2.7 V to 6 V, V <sub>IN+</sub> = 18 V		±0.1		μV/V
I <sub>B</sub>	Input bias current			28		μA
I <sub>OS</sub>	Input offset current			±0.02		μA
OUTPUT						
G	Gain		49	50	51	V/V
	Maximum capacitive load	No sustained oscillation		1		nF
VOLTAGE OUTPUT <sup>(2)</sup>						
	Swing to V+ power-supply rail	R <sub>L</sub> = 10 kΩ to GND, T <sub>A</sub> = −40°C to +105°C		(V+) − 0.05	(V+) − 0.2	V
	Swing to GND	R <sub>L</sub> = 10 kΩ to GND, T <sub>A</sub> = −40°C to +105°C		(V <sub>GND</sub> ) + 0.005	(V <sub>GND</sub> ) + 0.05	V
FREQUENCY RESPONSE						
GBW	Bandwidth	C <sub>LOAD</sub> = 10 pF		80		kHz
SR	Slew rate			0.4		V/μs
NOISE, RTI <sup>(1)</sup>						
	Voltage noise density			25		nV/√Hz
POWER SUPPLY						
V <sub>S</sub>	Operating voltage range (applied to V+)	T <sub>A</sub> = −40°C to +105°C	2.7		6	V
I <sub>Q</sub>	Quiescent current	V <sub>SENSE</sub> = 0 mV		65	100	μA
		T <sub>A</sub> = −40°C to +105°C			115	
TEMPERATURE RANGE						
	Specified range		−40		105	°C
	Operating range		−40		125	°C

(1) RTI = Referred-to-input.

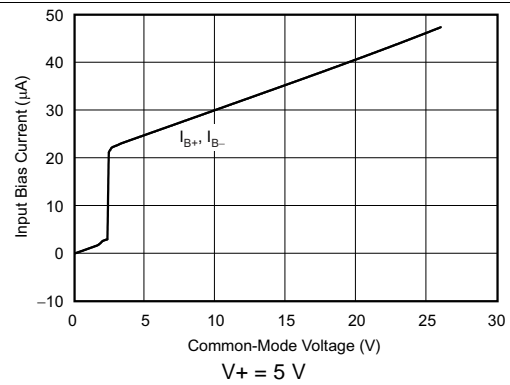
(2) See typical characteristic curve, *Output Voltage Swing vs Output Current* (Figure 1).

## 6.6 Typical Characteristics

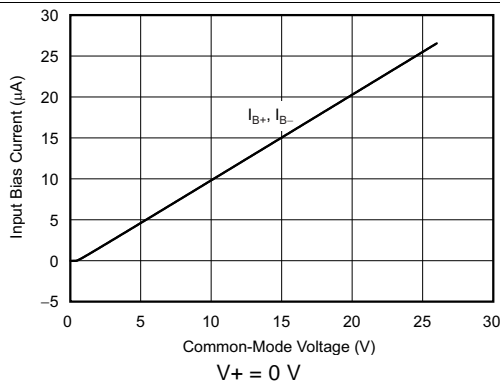
performance measured at  $T_A = 25^\circ\text{C}$ ,  $V_+ = 5\text{ V}$ , and  $V_{IN+} = 12\text{ V}$  (unless otherwise noted)



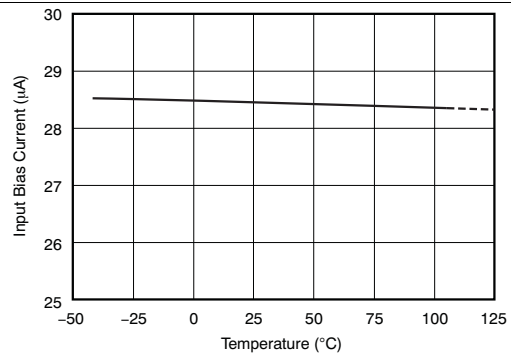
**Figure 1. Output Voltage Swing vs Output Current**



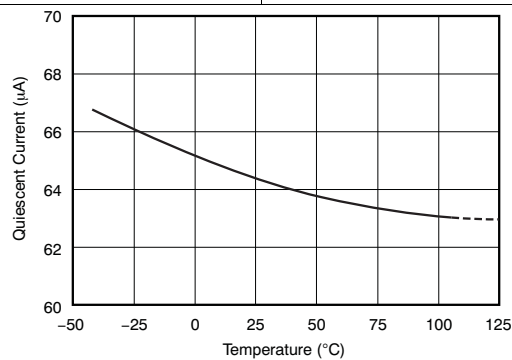
**Figure 2. Input Bias Current vs Common-Mode Voltage**



**Figure 3. Input Bias Current vs Common-Mode Voltage (Shutdown)**



**Figure 4. Input Bias Current vs Temperature**



**Figure 5. Quiescent Current vs Temperature**

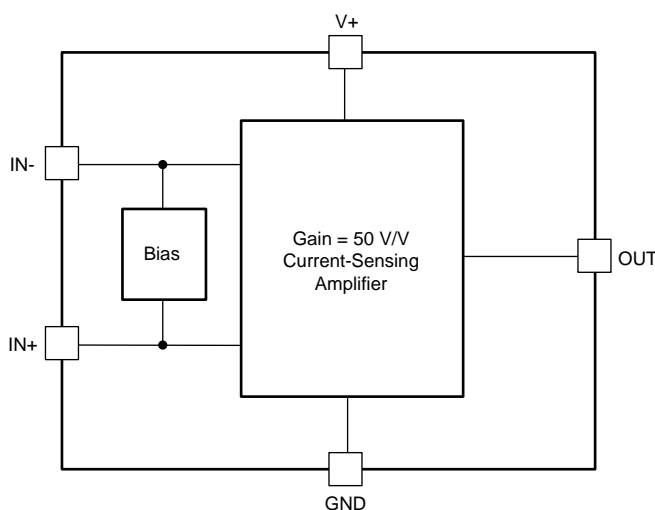
## 7 Detailed Description

### 7.1 Overview

The bq500100 is specially-designed to facilitate foreign object detection (FOD) in wireless charging applications by monitoring the coil supply current. The current-sensing amplifier is able to accurately measure voltages developed across a current-sensing resistor on common-mode voltages that far exceed the supply voltage powering the device. Current can be measured on input voltage rails as high as 20 V when the device is powered off a lower supply voltage.

Low drift characteristics enables high-precision measurements with maximum input offset voltages as low as 200  $\mu\text{V}$  with a maximum temperature contribution of 0.5  $\mu\text{V}/^\circ\text{C}$  over the full temperature range of  $-40^\circ\text{C}$  to  $+105^\circ\text{C}$ .

### 7.2 Functional Block Diagram



### 7.3 Feature Description

#### 7.3.1 High Input Common-Mode Range

The bq500100 can support input common-mode voltages up to 20 V. Because of the internal topology, the common-mode range is not restricted by the supply voltage as long as the input supply stays within the operational range of 2.7 V to 6 V. The ability to operate with supply voltages lower than the input voltage common-mode signal makes the device well-suited for monitoring the current in wireless charging applications where the common-mode voltage varies to obtain a desired amount of power transfer.

When the dc common-mode voltage varies, the effect on the output voltage is very small as a result of the high common-mode rejection. The dc common-mode rejection for the bq500100 is expressed in decibels and is typically as high as 120 dB. In wireless charging applications, the current-sensed rail commonly varies in voltage to adjust for the amount of power transferred by the coil.

#### 7.3.2 High Current-Sense Accuracy Over a Wide Dynamic Range

The offset voltage, gain error, and shunt resistor are the three primary contributors that determine the current measurement accuracy over a specified current range. The offset voltage dominates the error when operating at low current values and the gain error dominates when operating at high current values. The low offset voltage allows use of smaller shunt resistors values. Both the low offset and gain error allow the bq500100 to accurately measure current over a wide dynamic range and still maintain a high level of accuracy.

## 7.4 Device Functional Modes

### 7.4.1 Normal Operation

The bq500100 is in normal operation when the following conditions are met:

- $V_+$  is between 2.7 V and 6.0 V
- The common-mode input voltage is less than 20 V
- The differential input signal times gain is less than the supply voltage minus the output voltage swing to  $V_+$
- The differential input signal times gain is greater than the swing to GND
- Current flows into the shunt resistor from  $IN_+$  to  $IN_-$  connection points (unidirectional)

When in the normal operating region, the device operates as expected and produces an output voltage that is the gained-up representation of the difference voltage from  $IN_+$  to  $IN_-$ .

#### 7.4.1.1 Device Power-Up

The topology of the bq500100 allows voltages to be present on the inputs before power is applied; therefore, there is no sequencing requirement in regards to the input voltages and the power supply rail for  $V_+$ . There is a small delay of approximately 50  $\mu$ s from when power is applied to when the output voltage of the bq500100 settles to the correct voltage level.

#### 7.4.1.2 Input Differential Overload

If the differential input voltage ( $V_{IN_+} - V_{IN_-}$ ) multiplied by gain exceeds the voltage swing specification, the device drives the output as close as possible to the positive supply and does not provide accurate measurement of the differential input voltage. If this behavior occurs during normal circuit operation, then reduce the value of the shunt resistor to avoid this mode of operation. If a differential overload occurs in a fault event, then the output of the bq500100 returns to the expected value approximately 250  $\mu$ s after the fault condition is removed.



## 8 Application and Implementation

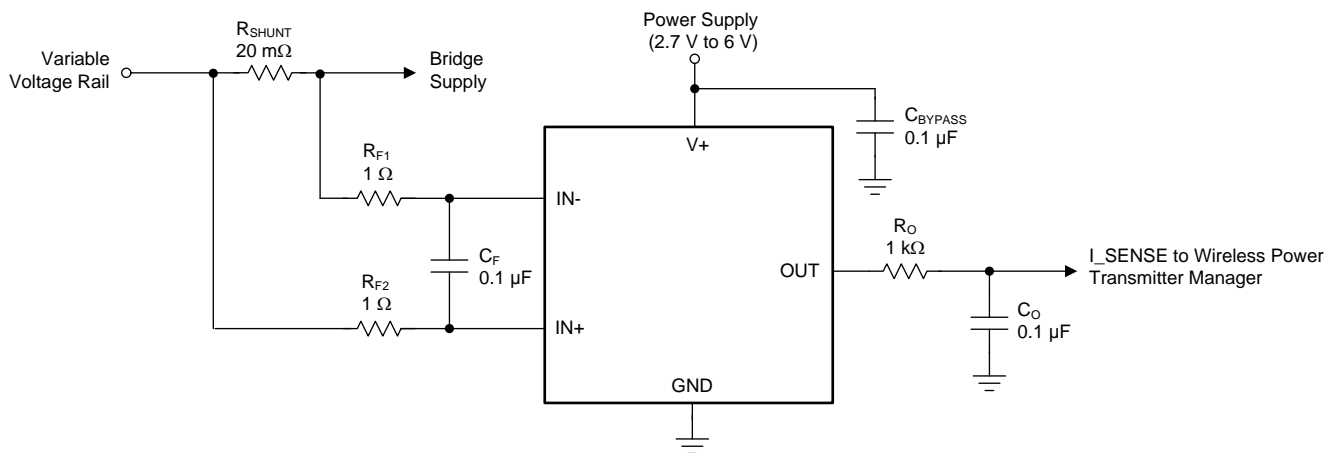
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The bq500100 is tailored to monitor current in wireless charging applications. This section focuses on the current-sense requirements for wireless charging. A typical application schematic and design procedure are provided in this section as reference.

### 8.2 Typical Application



NOTE:  $R_{F1} = R_{F2} = R_F$

**Figure 6. Typical Application for Wireless Charging**

#### 8.2.1 Design Requirements

The design requirements for a typical wireless charging application is shown in [Table 1](#). These requirements use the schematic shown in [Figure 6](#).

**Table 1. Design Parameters**

PARAMETER	DESIGN REQUIREMENT
Supply voltage range for V+	3.3 V $\pm$ 3% provided by a dc-dc converter
Common-mode voltage range	9 V to 19 V provided by a dc-dc converter
Power loss in the shunt resistor	20 mW or less at 1 A
Current-monitoring accuracy (gain error + offset error)	Better than 2.3% at 1 A, $V_{CM} = 12$ V, $T_A = 25^\circ\text{C}$
I_SENSE peak-to-peak ripple	Less than 15 mV

#### 8.2.2 Detailed Design Procedure

The first step in designing a solution is to make sure that the supply voltage and common-mode voltage are within the specified operational range of the device. For the supply and common-mode voltage requirements specified in [Table 1](#), the bq500100 reliably operates and is an ideal fit for this application.

The next step is to select the desired value for the shunt resistor. In this application example, the maximum power dissipation in the shunt resistor is specified to be 20 mW or less with a 1-A current-sense signal. The maximum power dissipation requirement limits the maximum value of the shunt resistor to  $20 \text{ mW} / (1 \text{ A})^2$ , or 20 mΩ. To meet this application requirement and still maximize the current-sense accuracy, the maximum allowable resistance of 20 mΩ is selected.

Additional input filtering (see [Figure 6](#)) is required to mitigate the affects of differential noise and switching ripple because the device is sensing the voltage rail of the dc-dc supply. When adding series resistance to the input, keeping the resistance as small as possible is recommended because any added resistance adds to the gain error of the device. For the bq500100, the amount of additional gain error resulting from the filter resistance  $R_S$  can be calculated using [Equation 1](#):

$$\text{Gain Error (\%)} = 100 - \left( 100 \times \frac{20,000}{(17 \times R_F) + 20,000} \right) \quad (1)$$

Applying [Equation 1](#) for the case where  $R_F$  is equal to 1 Ω results in an additional gain error of 0.085%. Applying this result to the total gain error is calculated to be approximately 2.085%.

The total offset voltage can be calculated by adding the effects of drift, change in supply voltage, and change in the common-mode input voltage to the specified offset voltage. In this example, no additional errors need to be added to the common-mode voltage and temperature because the conditions specified in [Table 1](#) match the  $V_{OS}$  conditions specified in the [Electrical Characteristics](#) table. The only additional error that needs to be added to the offset voltage is the effect of changes to the supply voltage. This document specifies a supply voltage of 5 V; however, this application calls for a supply voltage of 3.3 V. The change in offset voltage resulting from the difference in supply voltage can be calculated by using the PSR specification in this document; see the [Electrical Characteristics](#) table. The PSRR of the device is typically  $\pm 0.1 \text{ } \mu\text{V/V}$ ; therefore, the change in offset voltage can be calculated by taking the difference in supply voltage and multiplying by this value. In this case, the supply voltage difference is 1.7 V (5 V – 3.3 V), so the change in offset voltage is 0.17 μV. Therefore the total offset voltage error is 150.17 μV. Because the offset voltage error is a fixed value, the percentage influence on the accuracy is a function of the load current and can be calculated by applying [Equation 2](#).

$$\text{Total Offset Error (\%)} = \frac{\text{Total Offset Error (V)}}{I_{\text{SHUNT}}(\text{A}) \times R_{\text{SHUNT}}(\Omega)} \times 100\% \quad (2)$$

Applying [Equation 2](#) with an offset value of 150.15 μV, an  $R_{\text{SHUNT}}$  value of 20 mΩ, and a shunt current of 1 A results in a percentage error of 0.751%.

Now that the total gain error and offset error of the device are known, the accuracy of the current-shunt monitor can be calculated with [Equation 3](#):

$$\text{Total Error (\%)} = \sqrt{\text{Total Gain Error (\%)}^2 + \text{Total Offset Error (\%)}^2} \quad (3)$$

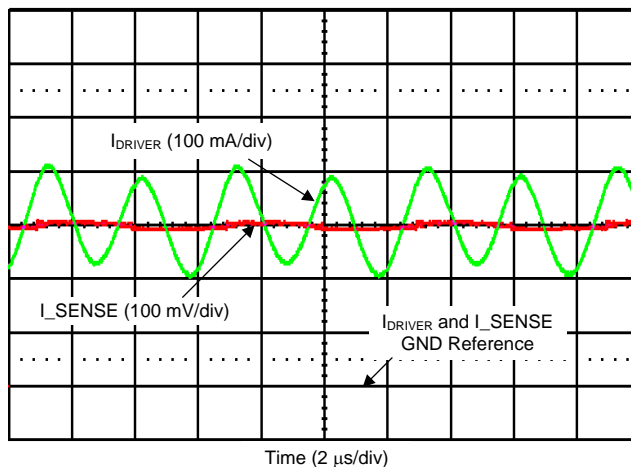
Applying [Equation 3](#) with a total gain error of 2.085% and a total offset error of 0.751% results in a total accuracy of 2.22% at 1 A, which is within the design target of 2.3%. Using a resistor tolerance of 0.5% to minimize errors introduced by  $R_{\text{SHUNT}}$  is recommended.

Additional output filtering consisting of  $R_O$  and  $C_O$  (see [Figure 6](#)) is required to further reduce the ripple at the bq500100 current-sense output. For best performance, keeping the ripple on the current monitor output below 15 mV is recommended. The values provided in [Figure 6](#) are sufficient for most use cases.

### 8.2.3 Application Curve

An example output response of the wireless charging application is shown in [Figure 7](#).

The coil driver current is shown in green and has both ac and dc components. The I\_SENSE signal is shown in red and is filtered to generate a signal representative of the dc current for foreign object detection.



**Figure 7. Current-Sense Output in a Wireless Charging Application**

## 9 Power Supply Recommendations

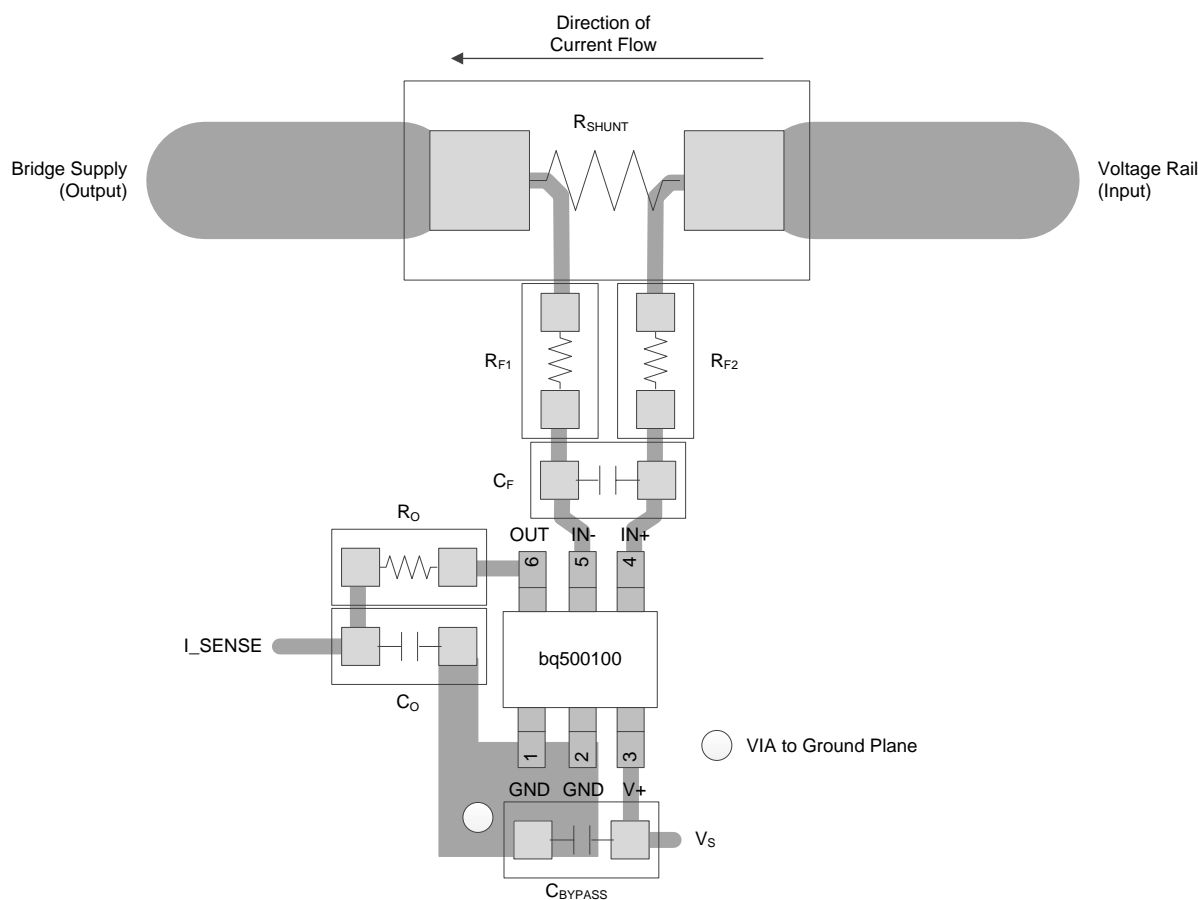
The input circuitry of the bq500100 can accurately measure beyond its power-supply voltage, V+. For example, the V+ power supply can be 5 V, whereas the load power-supply voltage can be as high as 20 V. However, the output voltage range of the OUT pin is limited by the voltages on the power-supply pin. Also, the bq500100 can withstand the full input signal range up to the 20-V range in the input pins, regardless of whether the device has power applied or not.

## 10 Layout

### 10.1 Layout Guidelines

- Make connections to the shunt resistor with a Kelvin or 4-wire connection. This connection technique ensures that only the current-sensing resistor impedance is detected between the input pins. Poor routing of the current-sensing resistor commonly results in additional resistance present between the input pins. Given the very low ohmic value of the current resistor, any additional high-current carrying impedance can cause significant measurement errors.
- Place the power-supply bypass capacitor as closely as possible to the supply and ground pins. The recommended value of this bypass capacitor is 0.1  $\mu\text{F}$ . Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies.
- Place the input filter capacitor,  $C_F$ , as close as possible to the input pins of the device. Place the input filter resistors as close as possible to each other to minimize the enclosed loop area between the device and the shunt resistor.
- The output of the current-sense circuit must be located as close as possible to the wireless power transmitter manager device. If the distance to the wireless power transmitter is greater than 1 cm, the output filter capacitor ( $C_O$ ) shown in Figure 8 must be placed next to the I\_SENSE pin of the wireless power transmitter manger. Placing the capacitor at the I\_SENSE pin of the wireless power transmitter manger provides the best filtering of the current-sense signal.

### 10.2 Layout Example



**Figure 8. Recommended Layout**

## 11 Device and Documentation Support

### 11.1 Documentation Support

#### 11.1.1 Related Documentation

bq501210 Data Sheet, [SLUSCF5](#)

bq500101 Data Sheet, [SLPS585](#)

*Transient Robustness for Current Shunt Monitor*, [TIDU473](#)

### 11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.3 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

### 11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 11.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">BQ500100DCKR</a>	Active	Production	SC70 (DCK)   6	3000   LARGE T&R	Yes	NIPDAU   SN	Level-2-260C-1 YEAR	-	12Y
BQ500100DCKR.B	Active	Production	SC70 (DCK)   6	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	See BQ500100DCKR	12Y
<a href="#">BQ500100DCKT</a>	Active	Production	SC70 (DCK)   6	250   SMALL T&R	Yes	NIPDAU   SN	Level-2-260C-1 YEAR	-	12Y
BQ500100DCKT.B	Active	Production	SC70 (DCK)   6	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	See BQ500100DCKT	12Y

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

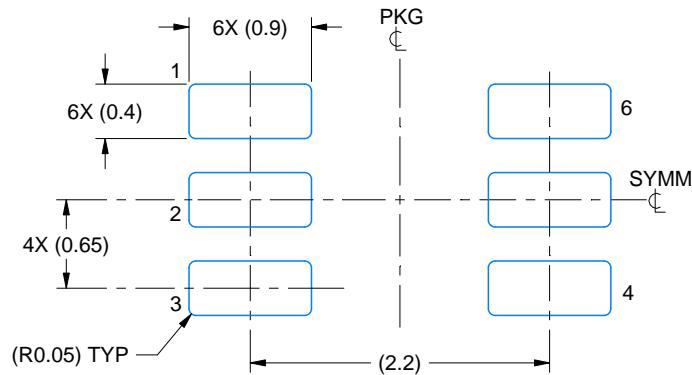
<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

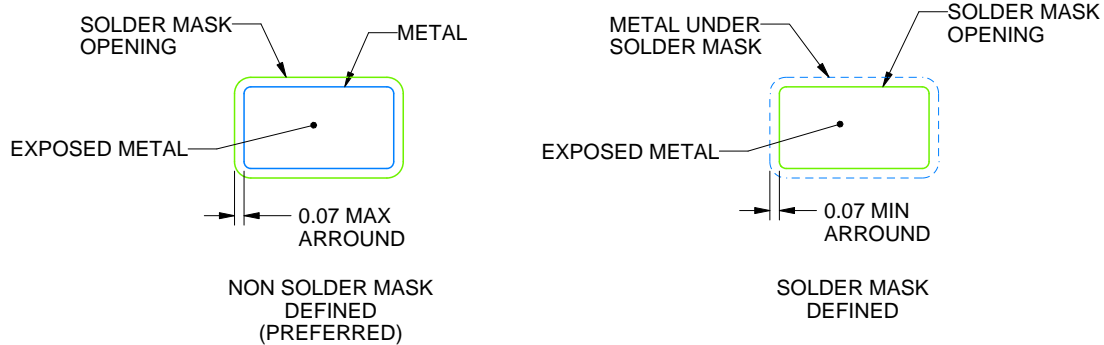
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LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X



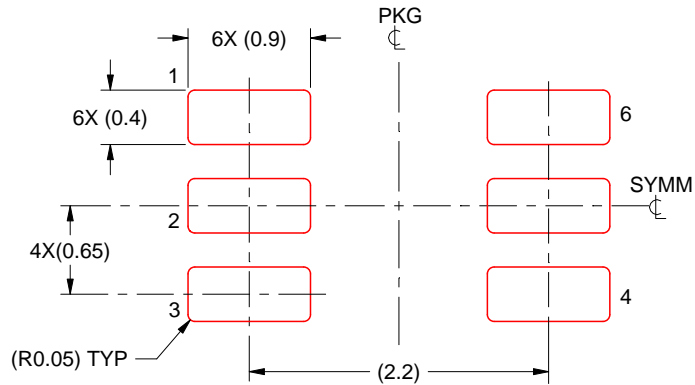
## SOLDER MASK DETAILS

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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.  
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





SOLDER PASTE EXAMPLE  
 BASED ON 0.125 THICK STENCIL  
 SCALE:18X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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