



## 4-Channel, Rail-to-Rail, CMOS BUFFER AMPLIFIER

### FEATURES

- UNITY GAIN BUFFER
- RAIL-TO-RAIL INPUT/OUTPUT
- WIDE BANDWIDTH: 8MHz
- HIGH SLEW RATE: 10V/ $\mu$ s
- LOW QUIESCENT CURRENT: 1.1mA
- TINY PACKAGE: MSOP-10, TSSOP-14

### APPLICATIONS

- TFT-LCD REFERENCE DRIVERS
- NOTEBOOKS
- ELECTRONIC GAMES
- ELECTRONIC BOOKS
- PERSONAL COMMUNICATION DEVICES
- PDA
- ACTIVE FILTERS
- ADC/DAC BUFFER

### DESCRIPTION

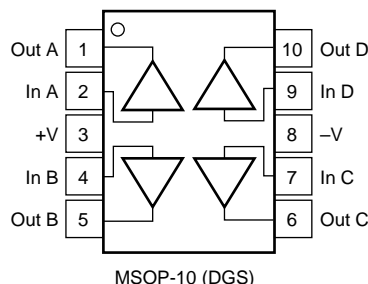
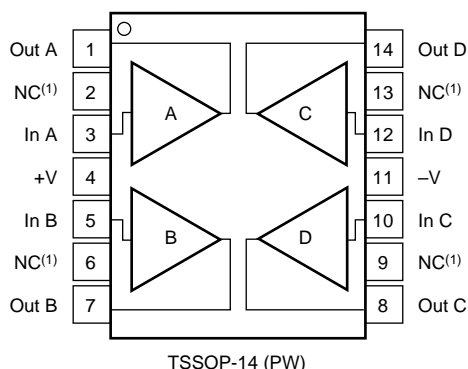
The BUF04701 is a 4-channel, low-power, high-voltage rail-to-rail input/output buffer. Operating on supplies ranging from 3.5V to 12V ( $\pm 1.75$ V to  $\pm 6$ V), the BUF04701 has a 3dB bandwidth of 8MHz with a slew rate of 10V/ $\mu$ s, and requires only 1.1mA quiescent current. The BUF04701 features rail-to-rail input and output capability, giving maximum dynamic range at any supply voltage.

Featuring fast slewing and settling times, as well as a high output drive, the BUF04701 is ideal for use as a voltage reference buffer in Thin Film Transistor Liquid Crystal Displays (TFT-LCDs).

The BUF04701 is available in an MSOP-10 package, providing the smallest footprint and thinnest package option available, as well as the TSSOP-14 package with a pinout that corresponds to standard quad op amps. This makes it easy to replace quad op amps in existing LCD displays with the low cost BUF04701, without changing the layout. The BUF04701 operates over a temperature range of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

### BUF04701 RELATED PRODUCTS

FEATURES	PRODUCT
1.2 MHz BW, 3.3mA $I_Q$	BUF11702
7MHz GBW, 1.5mA $I_Q$ , $V_S$ 3.5 - 12	OPA4743
5.9MHz GBW, 4.5mA $I_Q$ , $V_S$ = 4V - 44V	TLE2144/2
10MHz GBW, 2.5mA $I_Q$ , 16V/ $\mu$ s SR	TLC084



NOTE: (1) NC Means No Internal Connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Supply Voltage, V+ to V–	13.2V
Signal Input Terminals, Voltage <sup>(2)</sup>	(V–) –0.5V to (V+) + 0.5V
Current <sup>(2)</sup>	10mA
Output Short-Circuit <sup>(3)</sup>	Continuous
Operating Temperature	–40°C to +125°C
Storage Temperature	–65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current-limited to 10mA or less. (3) Short-circuit to ground, one amplifier per package.



## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION<sup>(1)</sup>

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
<b>Quad</b>						
BUF04701	MSOP-10	DGS	–40°C to +125°C	BUF04701	BUF04701AIDGSR	Tape and Reel, 2500
BUF04701	TSSOP-14	PW	–40°C to +125°C	04701A	BUF04701AIPWR	Tape and Reel, 2500

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet.

# ELECTRICAL CHARACTERISTICS: $V_S = +3.5V$ to $+12V$

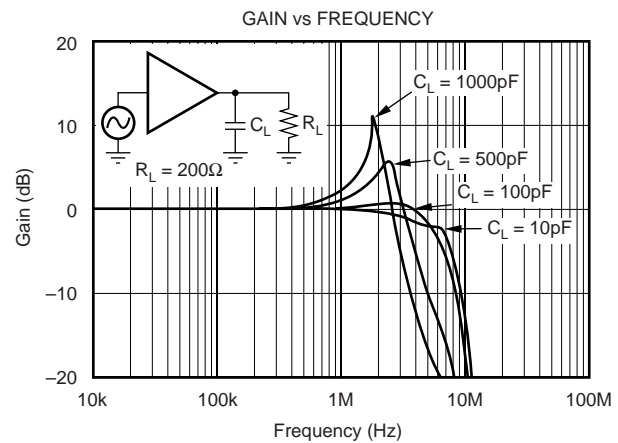
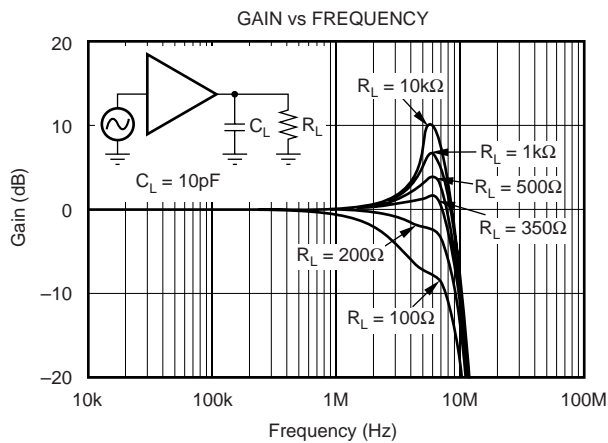
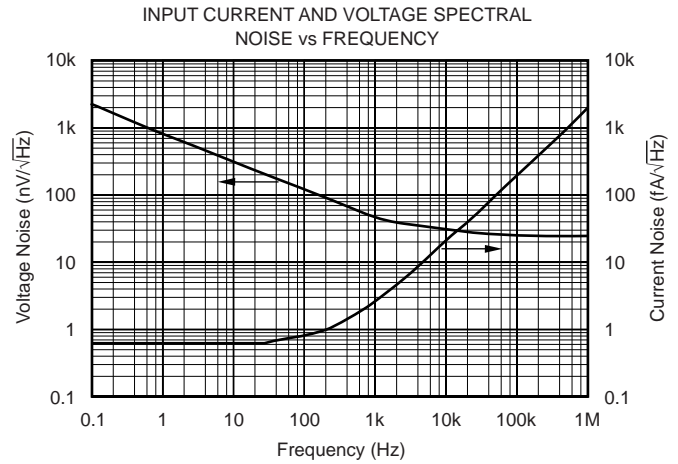
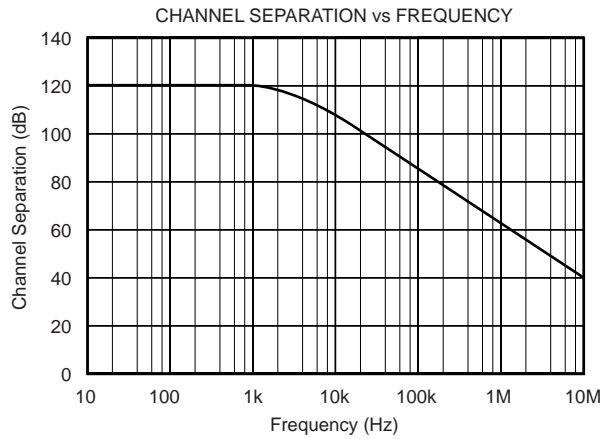
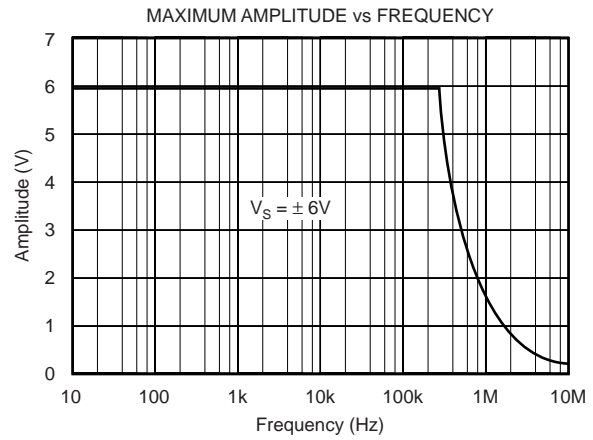
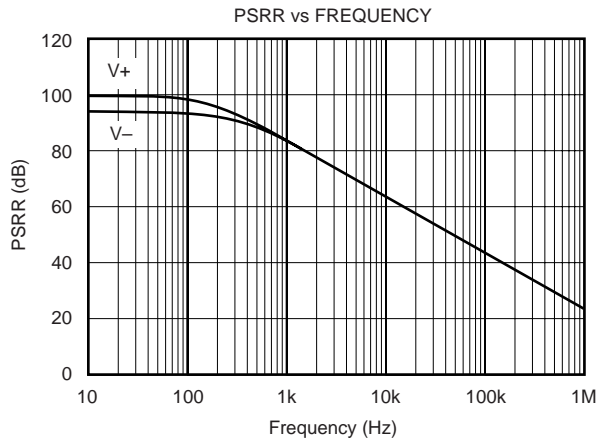
**Boldface** limits apply over the specified temperature range,  $T_A = -40^{\circ}C$  to  $+125^{\circ}C$

At  $T_A = +25^{\circ}C$ ,  $R_L = 10k\Omega$  connected to  $V_S/2$  and  $V_{OUT} = V_S/2$ , unless otherwise noted.

PARAMETER	CONDITION	BUF04701			UNITS
		MIN	TYP	MAX	
<b>OFFSET VOLTAGE</b> Input Offset Voltage $V_{OS}$ <b>Drift</b> $dV_{OS}/dT$ vs Power Supply PSRR <b>Over Temperature</b> Channel Separation, DC $f = 10kHz$	$V_S = \pm 5, V_{CM} = 0$  $V_S = 3.5V$ to $12V$ , $V_{CM} = V_S/2 - 0.5V$ <b><math>V_S = 3.5V</math> to <math>12V</math>, <math>V_{CM} = V_S/2 - 0.5V</math></b>		$\pm 1.5$ <b><math>\pm 8</math></b> 20  1 110	$\pm 7$  100 <b>200</b>	mV $\mu V/^{\circ}C$ $\mu V/V$ $\mu V/V$ dB
<b>INPUT VOLTAGE RANGE</b> Common-Mode Voltage Range $V_{CM}$		Limited by Output Range			
<b>INPUT BIAS CURRENT</b> Input Bias Current $I_B$	$V_{CM} = V_S/2$		1	$\pm 10$	pA
<b>INPUT IMPEDANCE</b> Common-Mode			$5 \cdot 10^{12} \parallel 4$		$\Omega \parallel pF$
<b>NOISE</b> Input Voltage Noise, $f = 0.1Hz$ to $10Hz$ Input Voltage Noise Density, $f = 10kHz$ $e_n$ Input Current Noise Density, $f = 1kHz$ $i_n$	$V_S = \pm 6V, V_{CM} = 0$ $V_S = \pm 6V, V_{CM} = 0$ $V_S = \pm 6V, V_{CM} = 0$		11 30 2.5		$\mu V_{rms}$ $nV/\sqrt{Hz}$ $fA/\sqrt{Hz}$
<b>TRANSFER CHARACTERISTIC</b> Gain <b>over Temperature</b>		0.9975 <b>0.995</b>	1.000 <b>1.000</b>	1.0025 <b>1.005</b>	
<b>OUTPUT</b> Voltage Output Swing from Rail  <b>over Temperature</b> Short-Circuit Current $I_{SC}$	$R_L = 10k\Omega$ $R_L = 2k\Omega$ <b><math>R_L = 2k\Omega</math></b>		75 150 $\pm 32$	200 <b>250</b>	mV mV <b>mV</b> mA
<b>FREQUENCY RESPONSE</b> Bandwidth $-3dB$ BW Slew Rate SR Settling Time, 0.1% $t_s$ Overload Recovery Time Total Harmonic Distortion + Noise THD+N	$C_L = 10pF$  $V_S = \pm 6V$ $V_S = \pm 6V, 5V$ Step $V_{IN} = V_S$ $V_S = \pm 6V, V_O = 1V_{rms}, G = 1,$ $f = 6kHz, V_{CM} = V_S/2$		8 10 9 0.2 0.001		MHz $V/\mu s$ $\mu s$ $\mu s$ %
<b>POWER SUPPLY</b> Specified Voltage Range, Single Supply $V_S$ Specified Voltage Range, Dual Supplies Operating Voltage Range Quiescent Current (per amplifier) $I_Q$ <b>over Temperature</b>	$I_Q = 0$	3.5 $\pm 1.75$	$+3.5$ to $+12$ 1.1	12 $\pm 6$ 1.5 <b>1.7</b>	V V V <b>mA</b> <b>mA</b>
<b>TEMPERATURE RANGE</b> Specified Range Operating Range Storage Range Thermal Resistance $\theta_{JA}$ TSSOP Surface Mount MSOP Surface Mount		$-40$ $-40$ $-65$	100 200	$+125$ $+125$ $+150$	$^{\circ}C$ $^{\circ}C$ $^{\circ}C$ $^{\circ}C/W$ $^{\circ}C/W$

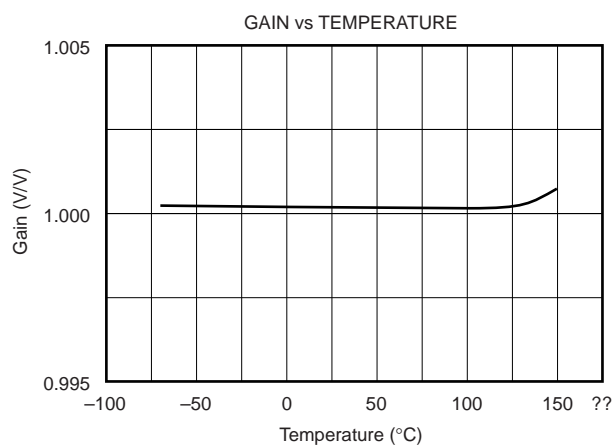
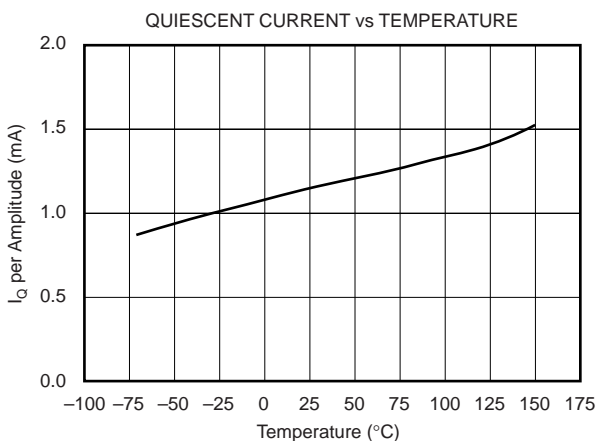
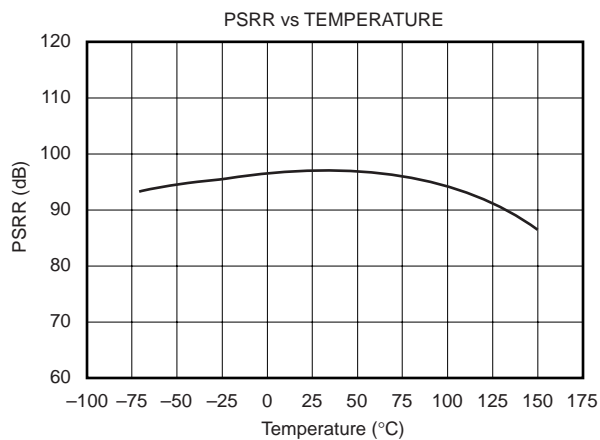
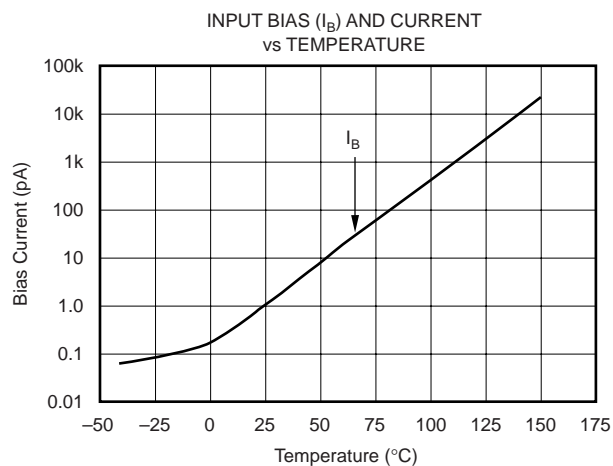
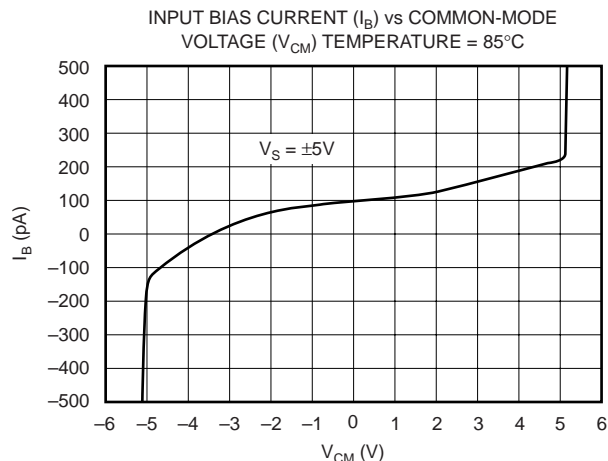
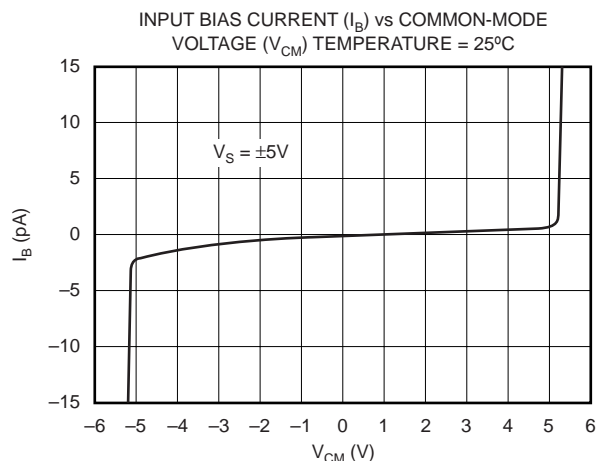
# TYPICAL CHARACTERISTICS

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 6\text{V}$ , and  $R_L = 10\text{k}\Omega$ , unless otherwise noted.



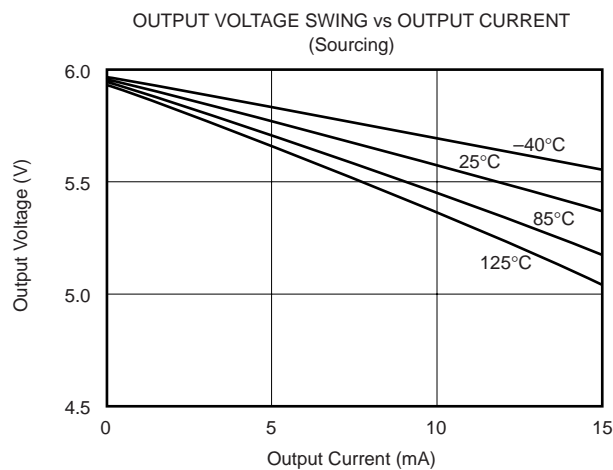
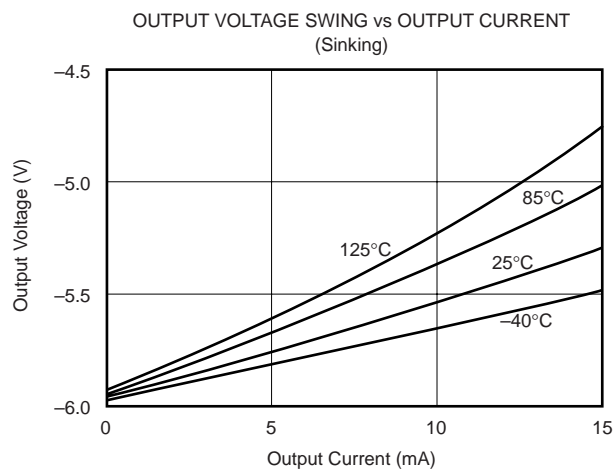
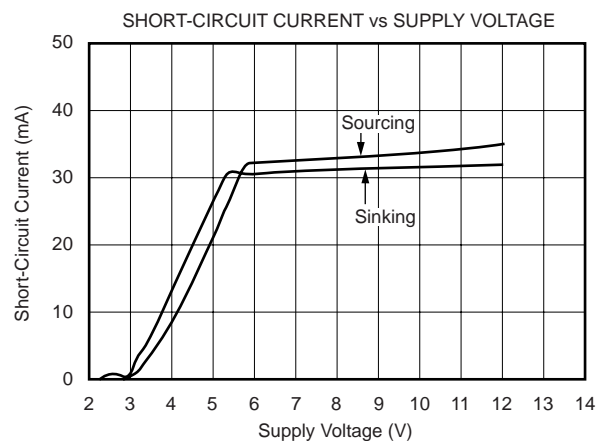
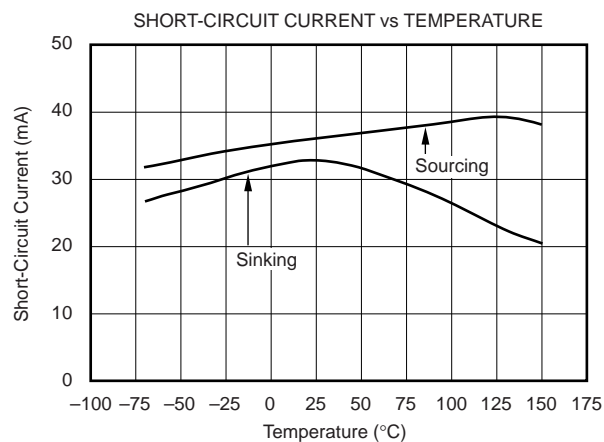
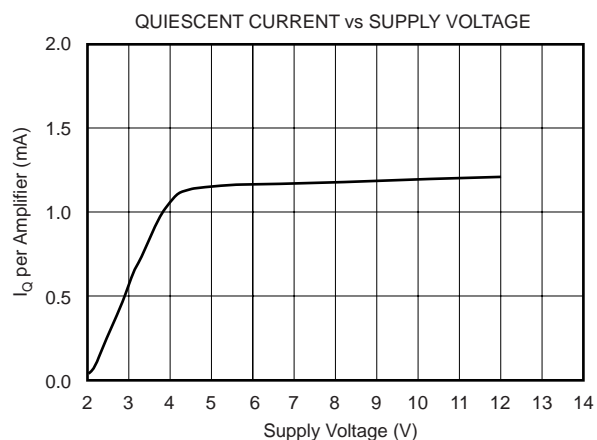
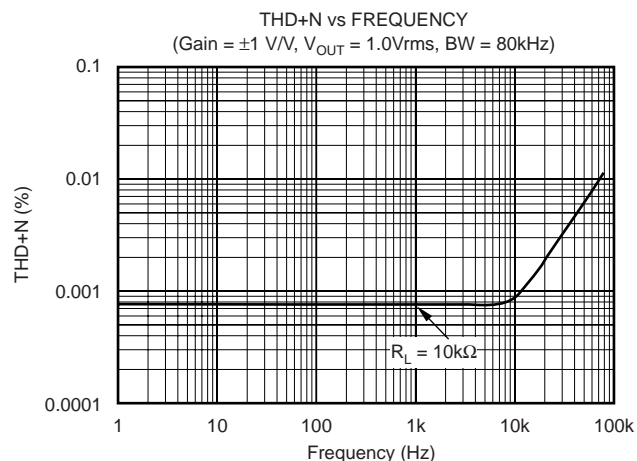
# TYPICAL CHARACTERISTICS (Cont.)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 6\text{V}$ , and  $R_L = 10\text{k}\Omega$ , unless otherwise noted.



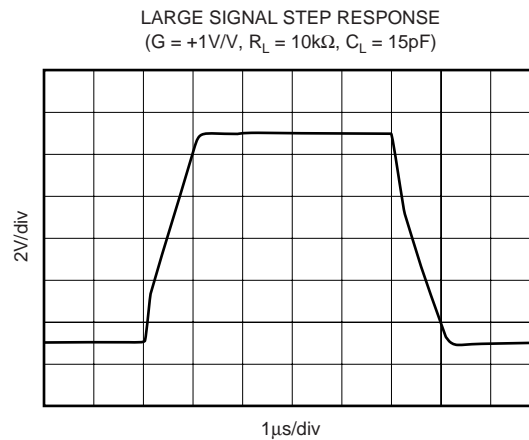
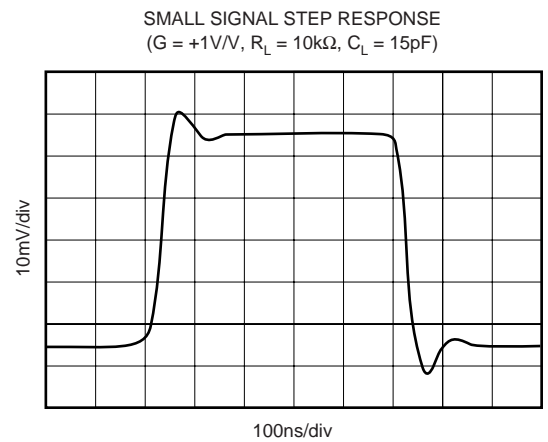
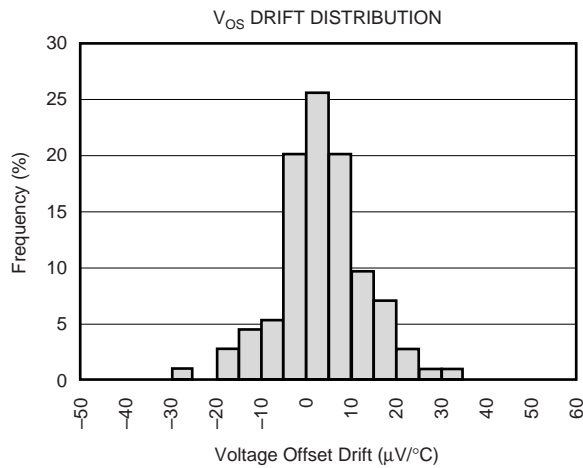
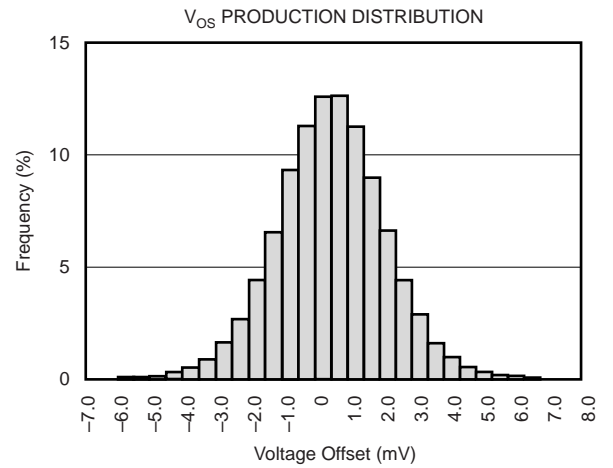
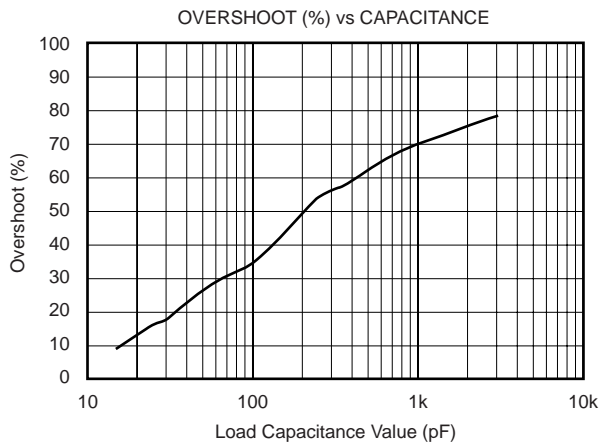
# TYPICAL CHARACTERISTICS (Cont.)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 6\text{V}$ , and  $R_L = 10\text{k}\Omega$ , unless otherwise noted.



# TYPICAL CHARACTERISTICS (Cont.)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 6\text{V}$ , and  $R_L = 10\text{k}\Omega$ , unless otherwise noted.



# APPLICATIONS INFORMATION

Figure 1 shows the BUF04701 connected as a buffer. Power supplies should be bypassed with capacitors connected close to the device pins. Capacitor values as low as  $0.1\mu\text{F}$  will assure stable operation in most applications, but high output current and fast output slewing can demand large current transients from the power supplies.

Rail-to-rail input and output swing helps maintain dynamic range, especially in low supply applications. Figure 2 shows the input and output waveforms for the BUF04701. On a  $\pm 6\text{V}$  supply with a  $100\text{k}\Omega$  load connected to  $V_S/2$ , the output is tested to swing within  $50\text{mV}$  to the rail.

## OPERATING VOLTAGE

The BUF04701 is fully specified and tested from  $3.5\text{V}$  to  $12\text{V}$  over a temperature range of  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ . Parameters that vary significantly with operating voltages or temperature are shown in the Typical Characteristic Curves.

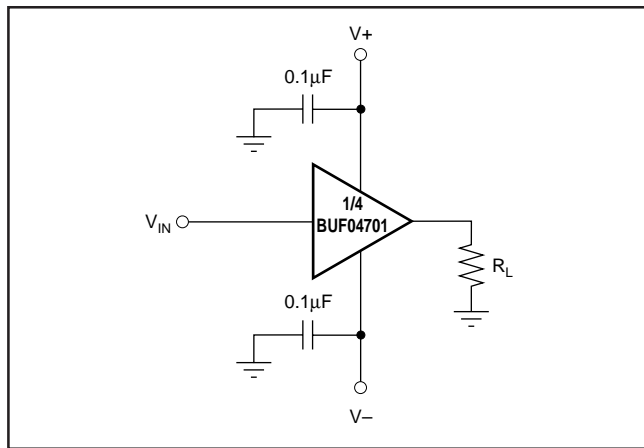


FIGURE 1. Basic Connections.

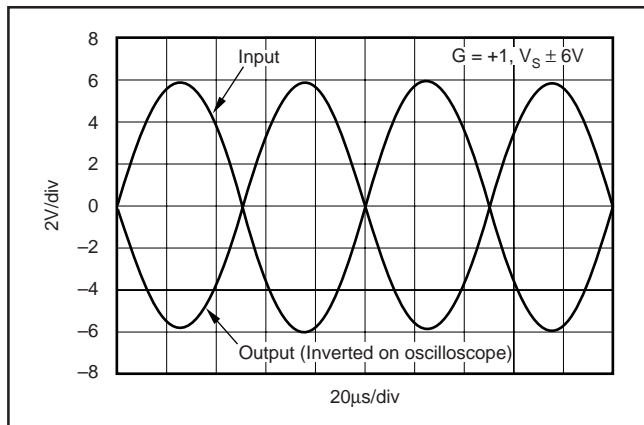


FIGURE 2. Rail-to-Rail Input and Output.

## RAIL-TO-RAIL INPUT

The input common-mode voltage range of the BUF04701 extends  $100\text{mV}$  beyond the supply rails at room temperature; however, due to the fixed gain at  $G = 1$ , the output will limit the useable input range. This wide swing is achieved with a complementary input stage—an N-channel input differential pair in parallel with a P-channel differential pair. The N-channel pair is active for input voltages close to the positive rail, typically  $(V+) - 2.0\text{V}$  to  $100\text{mV}$  above the positive supply, while the P-channel pair is on for inputs from  $100\text{mV}$  below the negative supply to approximately  $(V+) - 1.5\text{V}$ . There is a small transition region, typically  $(V+) - 2.0\text{V}$  to  $(V+) - 1.5\text{V}$ , in which both pairs are on. This  $500\text{mV}$  transition region can vary  $\pm 100\text{mV}$  with process variation. Thus, the transition region (both stages on) can range from  $(V+) - 2.1\text{V}$  to  $(V+) - 1.4\text{V}$  on the low end, up to  $(V+) - 1.9\text{V}$  to  $(V+) - 1.6\text{V}$  on the high end.

## INPUT PROTECTION

Device inputs are protected by ESD diodes that will conduct if the input voltages exceed the power supplies by more than approximately  $300\text{mV}$ . Momentary voltages greater than  $300\text{mV}$  beyond the power supply can be tolerated if the current is limited to  $10\text{mA}$ . This is easily accomplished with an input resistor, in series with the buffer input shown in Figure 3. Many input signals are inherently current-limited to less than  $10\text{mA}$ ; therefore, a limiting resistor is not always required. The BUF04701 features no phase inversion when the inputs extend beyond supplies if the input current is limited, as shown in Figure 4.

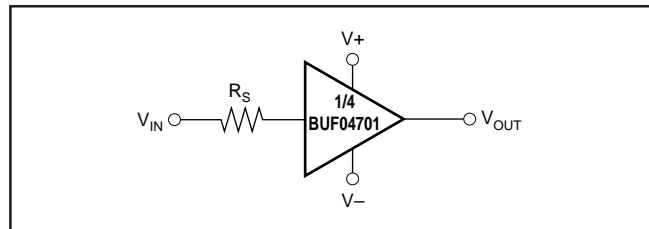


FIGURE 3. Limiting Input Current on the BUF04701.

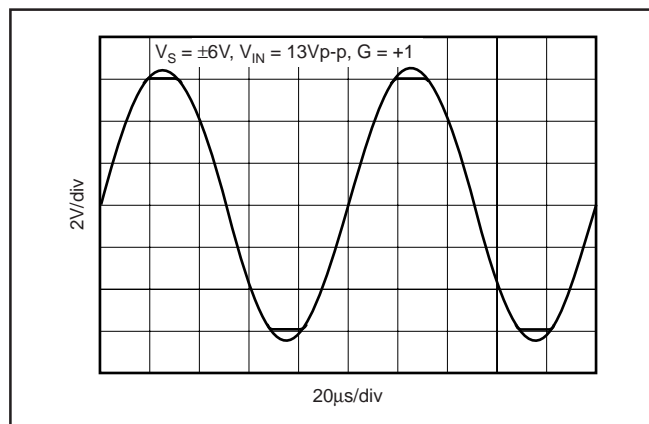


FIGURE 4. BUF04701—No Phase Inversion with Inputs Greater than the Power-Supply Voltage.



## RAIL-TO-RAIL OUTPUT

A class AB output stage with common-source transistors is used to achieve rail-to-rail output. This output stage is capable of driving  $1\text{k}\Omega$  loads connected to any point between  $V_+$  and  $V_-$ . For light resistive loads ( $> 100\text{k}\Omega$ ), the output voltage can swing to  $100\text{mV}$  from the supply rail. With  $2\text{k}\Omega$  resistive loads, the output is specified to swing to within  $200\text{mV}$  of the supply rails while maintaining high open-loop gain (see the typical characteristic curve *Output Voltage Swing vs Output Current*).

## CAPACITIVE LOAD AND STABILITY

The BUF04701 can drive up to  $1000\text{pF}$  pure capacitive load. One method of improving capacitive load drive is to insert a  $10$  to  $20\Omega$  resistor in series with the output, as shown in Figure 5. This reduces ringing with large capacitive loads while maintaining DC accuracy.

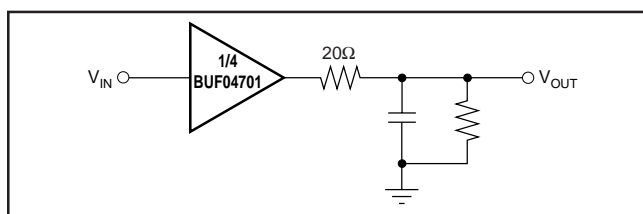


FIGURE 5. Improving Capacitive Load Drive.

## APPLICATION CIRCUITS

### REFERENCE BUFFER FOR LCD SOURCE DRIVERS

In modern high-resolution TFT-LCD displays, gamma correction must be performed to correct for nonlinearities in the glass transmission characteristics of the LCD panel. The typical LCD source driver for 64 bits of grayscale uses internal Digital-to-Analog Converters (DACs) to convert the 6-bit data into analog voltages applied to the LCD. These DACs typically require external voltage references for proper operation. Normally these external reference voltages are generated using a simple resistive ladder, like the one shown in Figure 6.

Typical laptop or desktop LCD panels require 6 to 8 of the source driver circuits in parallel to drive all columns of the panel. Although the resistive load of one internal string of a DAC is only around  $10\text{k}\Omega$  to  $16\text{k}\Omega$ , 6 to 8 strings in parallel represent a very substantial load. The power supply used for the LCD source drivers for laptops is typically in the order of  $10\text{V}$ . To maximize the dynamic range of the DAC, rail-to-rail

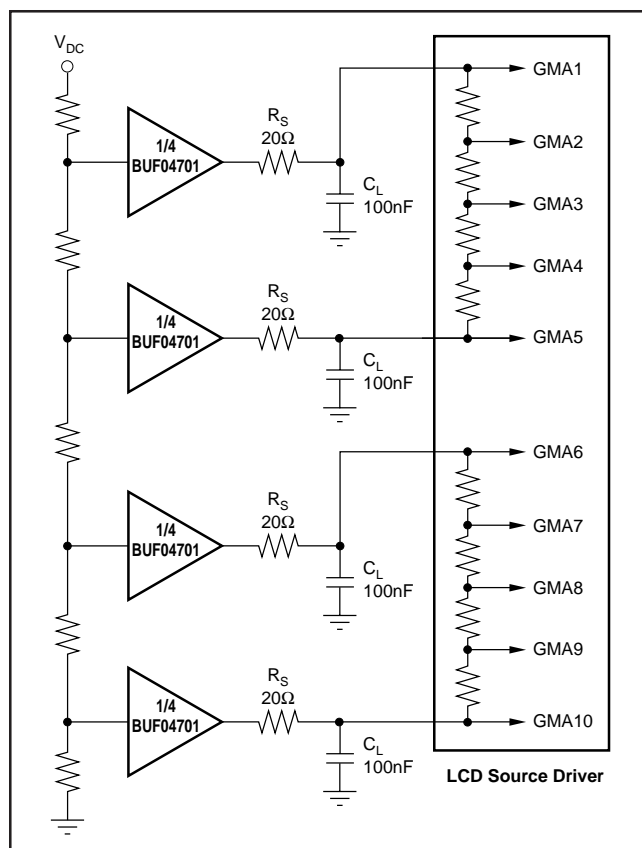


FIGURE 6. BUF04701 as LCD Display Buffer.

output performance is required for the upper and lower buffer. The ability of the BUF04701 to operate on  $12\text{V}$  supplies, to drive heavy resistive loads (as low as  $2\text{k}\Omega$ ), and to swing to within  $200\text{mV}$  of the supply rails, makes it very well suited as a buffer for the reference voltage inputs of LCD source drivers.

During conversion of the DAC, internal switches create current glitches on the output of the reference buffer. The capacitor  $C_L$  (typically  $100\text{nF}$ ) functions as a charge reservoir that provides/absorbs most of the glitch energy. The series resistor  $R_S$  isolates the outputs of the BUF04701 from the heavy capacitive load and helps to improve settling time.

### 4-POLE LOW-PASS Sallen-Key FILTER

The high open-loop gain and wide bandwidth of the BUF04701 make it optimal for active filtering applications. Figure 7 shows the BUF04701 in a 4-pole Butterworth low-pass active filter configuration of  $20\text{kHz}$  bandwidth.

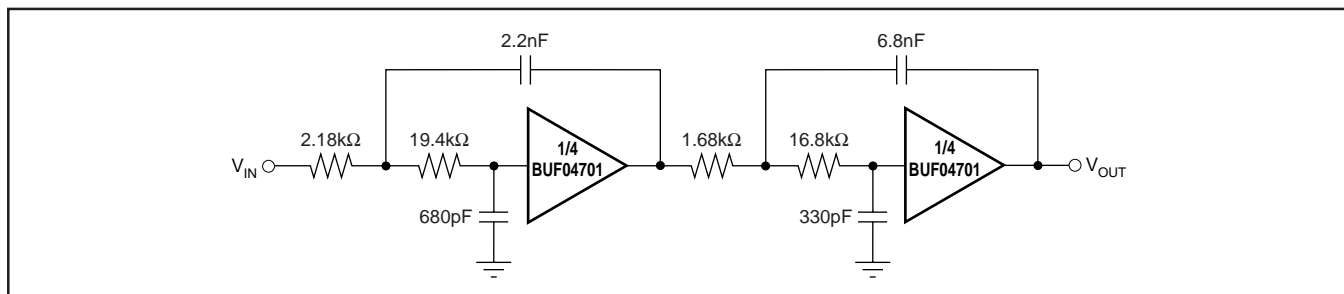


FIGURE 7. BUF04701 Configured as a 4-Pole Sallen-Key Butterworth Low-Pass Filter.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BUF04701AIDGSR	NRND	Production	VSSOP (DGS)   10	2500   LARGE T&R	Yes	Call TI   Nipdauag	Level-2-260C-1 YEAR	-40 to 125	B01
BUF04701AIDGSR.B	NRND	Production	VSSOP (DGS)   10	2500   LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	B01

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

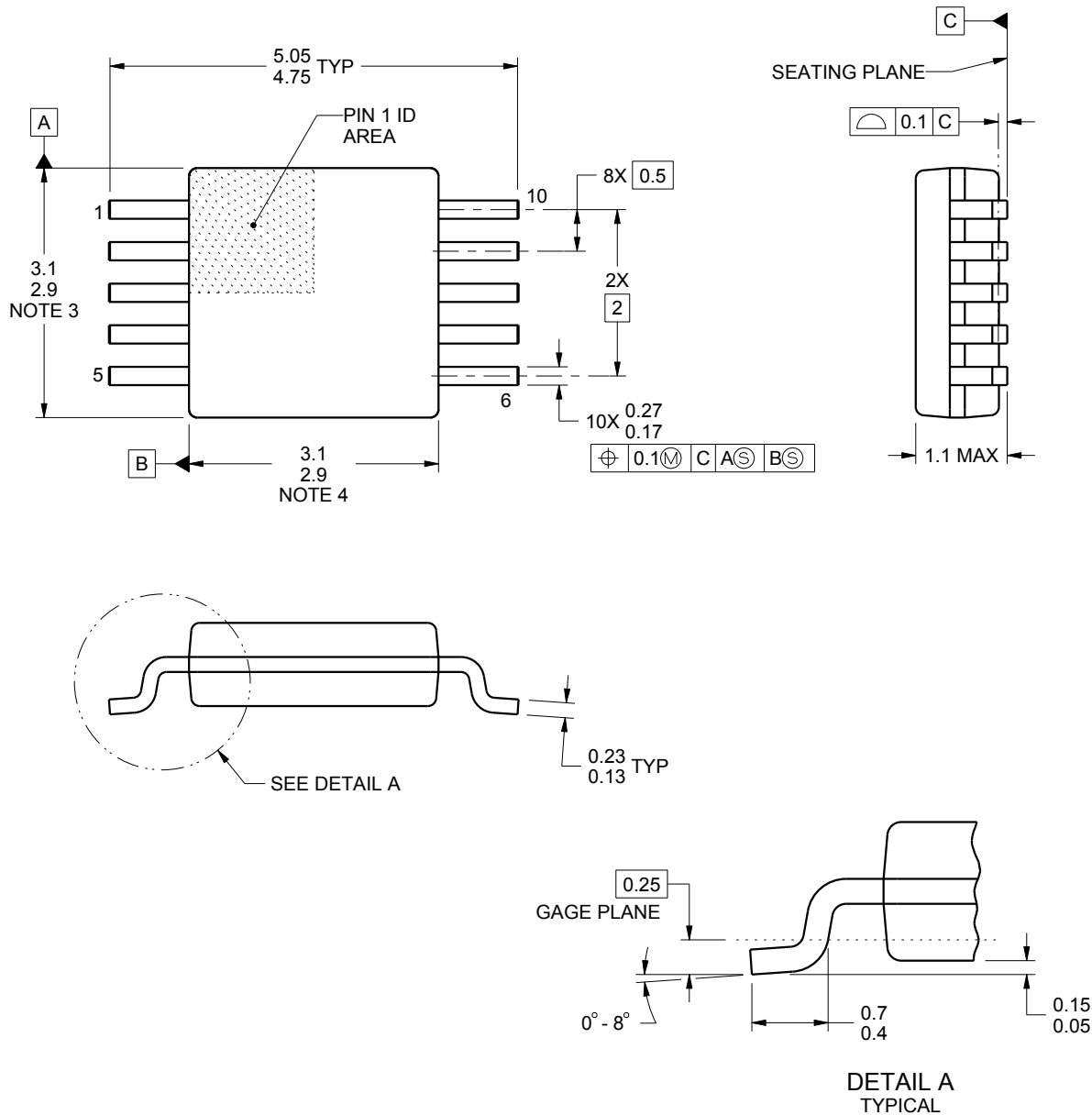
<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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NOTES:

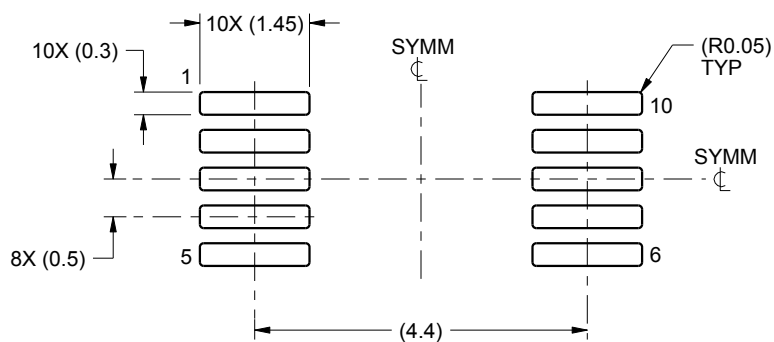
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.

# EXAMPLE BOARD LAYOUT

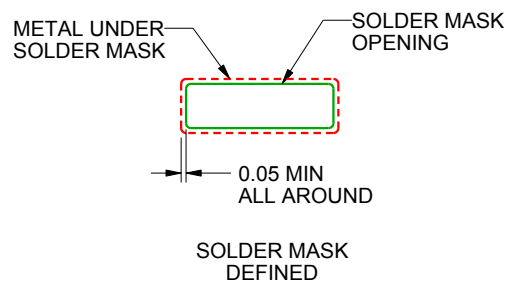
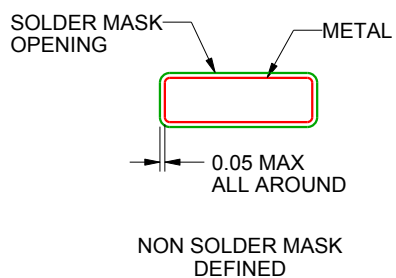
DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

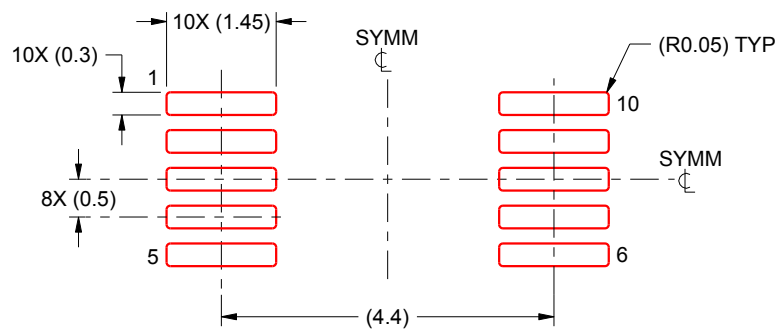
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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