# BUF634 250mA High-Speed Buffer

## 1 Features

- A newer version of this device is now available: BUF634A
- High output current: 250mA
- Slew rate: 2000V/µs
- Pin-selected bandwidth: 30MHz to 180MHz
- Low quiescent current: 1.5mA (30MHz BW)
- Wide supply range: ±2.25V to ±18V
- Internal current limit
- Thermal shutdown protection
- Packages:
  - 5-pin SOIC
  - 5-pin TO-220
  - 5-pin TO-263 surface-mount

## 2 Applications

- Valve driver
- Solenoid driver
- Op amp current booster
- Line driver
- Headphone driver
- Video driver
- Motor driver
- Test equipment
- ATE pin driver

## 3 Description

The BUF634 is a high-speed, unity-gain, open-loop buffer recommended for a wide range of applications. The BUF634 can be used inside the feedback loop of op amps to increase output current, eliminate thermal feedback, and improve capacitive load drive.

For low-power applications, the BUF634 operates on 1.5mA quiescent current with 250mA output, 2000V/µs slew rate, and 30MHz bandwidth. Bandwidth can be adjusted from 30MHz to 180MHz by connecting a resistor between V– and the BW pin.

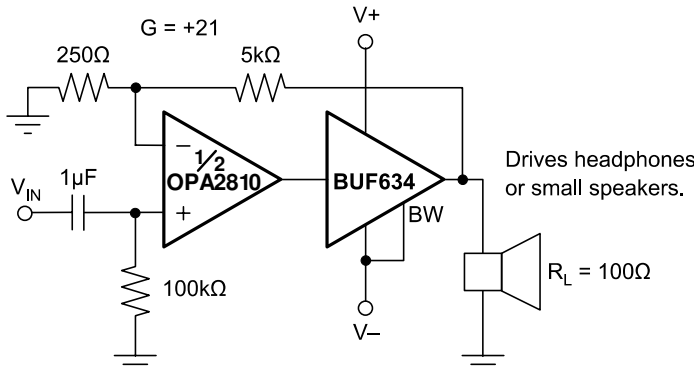
Output circuitry is fully protected by internal current limit and thermal shutdown, making the device rugged and easy to use.

The BUF634 is available in a variety of packages to meet mechanical and power-dissipation requirements. Types include SOIC-8 surface-mount, 5-lead TO-220, and a 5-lead TO-263 (DDPAK) surface-mount plastic power packages.

**Package Information**

| PART NUMBER | PACKAGE(1) | PACKAGE SIZE(2) |
|---|---|---|
| BUF634 | D (SOIC, 8) | 4.9mm × 6mm |
| | KC (TO-220, 5) | 10.16mm × 4.45mm |
| | KTT (TO-263, 5) | 10.16mm × 15.24mm |

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.




**Boost the Output Current of any Operational Amplifier**

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## 4 Device Comparison Table

| DEVICE | $V_{S\pm}$ (V) | $I_Q$/CHANNEL (mA) | BW (MHz) | SLEW RATE (V/µs) | VOLTAGE NOISE (nV/√HZ) | AMPLIFIER DESCRIPTION |
|---|---|---|---|---|---|---|
| BUF634A | ±18 | 1.5 to 8.5 | 35 to 210 | 3750 | 3.4 | Unity-gain, open-loop buffer |
| BUF634 | ±18 | 1.5 to 15 | 30 to 180 | 2000 | 4 | Unity-gain, open-loop buffer |
| LMH6321 | ±18 | 11 | 110 | 1800 | 2.8 | Unity-gain, open-loop buffer with adjustable current limit |

## 5 Pin Configuration and Functions

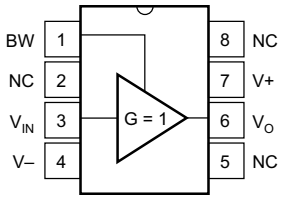



**Figure 5-1. D Package, 8-Pin SOIC (Top View)**

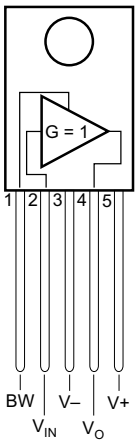



**Figure 5-2. KC Package, 5-Pin TO-220 (Top View)**

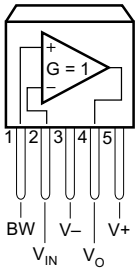



**Figure 5-3. KTT Package, 5-Pin TO-263 (Top View)**

**Table 5-1. Pin Functions**

| PIN | | | TYPE | DESCRIPTION |
|---|---|---|---|---|
| NAME | NO. | | | |
| | D (SOIC) | KC (TO-220)<br>KTT (TO-263) | | |
| BW | 1 | 1 | Input | Bandwidth adjust pin |
| NC | 2, 5, 8 | — | — | No internal connection |
| V+ | 7 | 5 | Input | Positive power supply |
| $V_{IN}$ | 3 | 2 | Input | Input |
| $V_O$ | 6 | 4 | Output | Output |
| V– | 4 | 3 | Input | Negative power supply |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| | Supply voltage | | ±18 | V |
| | Input voltage | | $\pm V_S$ | |
| | Output short-circuit (to ground) | | Continuous | |
| | Operating temperature | –40 | 125 | °C |
| | Junction temperature | | 150 | °C |
| | Lead temperature (soldering, 10 s) | | 300 | °C |
| $T_{stg}$ | Storage temperature | –55 | 125 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| **BUF634U in D (SOIC) Package** | | | | |
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2500 | V |
| **BUF634U in D (SOIC) Package** | | | | |
| $V_{(ESD)}$ | Electrostatic discharge, | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±1000 | V |
| **BUF634F in KC (TO-220) and KTT (TO-263) Packages** | | | | |
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2500 | V |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_S$ = (V+) – (V–) | Supply voltage | ±2.25 (4.5) | ±15 (30) | ±18 (36) | V |
| $T_A$ | Operating temperature | -40 | 25 | 85 | °C |

## 6.4 Thermal Information

| THERMAL METRIC(1) | | BUF634 | | | UNIT |
|---|---|---|---|---|---|
| | | D (SOIC) | KC (TO-220) | KTT (TO-263) | |
| | | 8 PINS | 5 PINS | 5 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 123 | 32.1 | 41.8 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 55 | 25.6 | 45 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 68 | 18.3 | 24.8 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 12 | 8.5 | 13.1 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 67 | 17.7 | 23.8 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | 0.7 | 2.4 | °C/W |

(1) For information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Electrical Characteristics: TO-220 and TO-263 Packages

at $T_A$ = +25°C[1], $V_S$ = ±15 V, specifications are for both low quiescent-current mode and wide-bandwidth mode (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| **INPUT** | | | | | | | | |
| | Offset voltage | | | | | ±30 | ±100 | mV |
| | Offset voltage vs temperature | | Specified temperature range | | | ±100 | | µV/°C |
| | Offset voltage vs power supply | | $V_S$ = ±2.25 V[2] to ±18 V | | | 0.1 | 1 | mV/V |
| | Input bias current | | $V_{IN}$ = 0 V | Low quiescent current mode | | ±0.5 | ±2 | µA |
| | | | | Wide bandwidth mode | | ±5 | ±20 | |
| | Input impedance | | $R_L$ = 100 Ω | Low quiescent current mode | | 80 \|\| 8 | | MΩ \|\| pF |
| | | | | Wide bandwidth mode | | 8 \|\| 8 | | |
| | Noise voltage | | f = 10 kHz | | | 4 | | nV/√Hz |
| **GAIN** | | | | | | | | |
| | Gain | | $R_L$ = 1 kΩ, $V_O$ = ±10 V | | 0.95 | 0.99 | | V/V |
| | | | $R_L$ = 100 Ω, $V_O$ = ±10 V | | 0.85 | 0.93 | | |
| | | | $R_L$ = 67 Ω, $V_O$ = ±10 V | | 0.8 | 0.9 | | |
| **OUTPUT** | | | | | | | | |
| | Current output, continuous | | | | | ±250 | | mA |
| | Voltage output | Positive | $I_O$ = 10 mA | | (V+) – 2.1 | (V+) – 1.7 | | V |
| | | Negative | $I_O$ = –10 mA | | (V–) + 2.1 | (V–) + 1.8 | | |
| | | Positive | $I_O$ = 100 mA | | (V+) – 3 | (V+) – 2.4 | | |
| | | Negative | $I_O$ = –100 mA | | (V–) + 4 | (V–) + 3.5 | | |
| | | Positive | $I_O$ = 150 mA | | (V+) – 4 | (V+) – 2.8 | | |
| | | Negative | $I_O$ = –150 mA | | (V–) + 5 | (V–) +4 | | |
| | Short-circuit current | | Low quiescent current mode | | | ±350 | ±550 | mA |
| | | | Wide bandwidth mode | | | ±400 | ±550 | |
| **DYNAMIC RESPONSE** | | | | | | | | |
| | Bandwidth, –3dB | | $R_L$ = 1 kΩ | Low quiescent current mode | | 30 | | MHz |
| | | | | Wide bandwidth mode | | 180 | | |
| | | | $R_L$ = 100 Ω | Low quiescent current mode | | 20 | | |
| | | | | Low quiescent current mode | | 160 | | |
| | Slew rate | | 20 Vp-p, $R_L$ = 100 Ω | | | 2000 | | V/µs |
| | Settling time | 0.1% | 20-V step, $R_L$ = 100 Ω | | | 200 | | ns |
| | | 1% | | | | 50 | | |
| | Differential gain | | 3.58 MHz, $V_O$ = 0.7 V, $R_L$ = 150 Ω | Low quiescent current mode | | 4% | | |
| | | | | Wide bandwidth mode | | 0.4% | | |
| | Differential phase | | 3.58 MHz, $V_O$ = 0.7 V, $R_L$ = 150 Ω | Low quiescent current mode | | 2.5 | | ° |
| | | | | Wide bandwidth mode | | 0.1 | | |

## 6.5 Electrical Characteristics: TO-220 and TO-263 Packages (continued)

at $T_A$ = +25°C[1], $V_S$ = ±15 V, specifications are for both low quiescent-current mode and wide-bandwidth mode (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | | |
| | Specified operating voltage | | | | ±15 | | V |
| | Operating voltage | | | ±2.25[2] | | ±18 | V |
| $I_Q$ | Quiescent current | $I_O$ = 0 mA | Low quiescent current mode | | ±1.5 | ±2 | mA |
| | | | Wide bandwidth mode | | ±15 | ±20 | |
| **TEMPERATURE** | | | | | | | |
| $T_J$ | Thermal shutdown temperature | | | | 175 | | °C |

(1) Tests are performed on high-speed automatic test equipment, at approximately 25°C junction temperature. The power dissipation of this product causes some parameters to shift when warmed up. See *Section 6.8* for overtemperature performance.
(2) Limited output swing available at low supply voltage. See output voltage specifications.

## 6.6 Electrical Characteristics: Wide-Bandwidth Mode for SOIC Package

at $T_A$ = 25°C, $V_S$ = ±15 V, BW pin connected to V–, and $R_L$ = 100 Ω connected to mid-supply (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **AC PERFORMANCE** | | | | | | |
| BW | Bandwidth, –3 dB | $R_L$ = 1 kΩ | | 210 | | MHz |
| | | $R_L$ = 100 Ω | | 200 | | |
| | Bandwidth for 0.1-dB flatness | $V_O$ = 10 $mV_{PP}$, $R_L$ = 100 Ω, $R_S$ = 50 Ω | | 50 | | MHz |
| SR | Slew rate | $V_O$ = 20-V step, $V_{IN}$-SR = 4000 V/µs | | 3750 | | V/µs |
| | Rise and fall time | $V_O$ = 200-mV step | | 1.3 | | ns |
| | Settling time to 0.1% | $V_O$ = 20-V step, $V_{IN}$-SR = 2500 V/µs | | 90 | | ns |
| | Settling time to 1% | $V_O$ = 20-V step, $V_{IN}$-SR = 2500 V/µs | | 20 | | ns |
| $e_n$ | Voltage noise | f = 1 kHz | | 3.4 | | nV/√Hz |
| $i_n$ | Current noise | f = 100 kHz | | 0.85 | | pA/√Hz |
| HD2 | 2nd-harmonic distortion | $V_O$ = 2 $V_{PP}$, f = 20 kHz | | –77 | | dBc |
| | | $V_O$ = 10 $V_{PP}$, f = 20 kHz | | –69 | | |
| HD3 | 3rd-harmonic distortion | $V_O$ = 2 $V_{PP}$, f = 20 kHz | | –77 | | dBc |
| | | $V_O$ = 10 $V_{PP}$, f = 20 kHz | | –56 | | |
| **DC PERFORMANCE** | | | | | | |
| $V_{OS}$ | Input offset voltage | $T_A$ = 25°C | | 36 | 65 | mV |
| | Input offset voltage drift(1) | $T_A$ = –40°C to 125°C | | 175 | | µV/°C |
| $I_B$ | Input bias current | $V_{IN}$ = 0 V | | 0.25 | 2 | µA |
| G | Gain | $V_O$ = ±10 V, $R_L$ = 1 kΩ | 0.95 | 0.99 | | V/V |
| | | $V_O$ = ±10 V, $R_L$ = 100 Ω | 0.93 | 0.95 | | |
| | | $V_O$ = ±10 V, $R_L$ = 67 Ω | 0.91 | 0.93 | | |
| **INPUT** | | | | | | |
| | Linear input voltage range | $R_L$ = 1 kΩ, $I_B$ < 10 µA | –13 | | 13 | V |
| $Z_{IN}$ | Input impedance | $R_L$ = 100 Ω | | 180 \|\| 5 | | MΩ \|\| pF |
| **OUTPUT** | | | | | | |
| | Output headroom to supplies | $I_O$ = ±10 mA | | 1.6 | 1.8 | V |
| | | $I_O$ = ±100 mA | | 2.0 | 2.2 | |
| | | $I_O$ = ±150 mA | | 2.2 | 2.5 | |
| $I_O$ | Current output, continuous | | | ±250 | | mA |
| $I_{SC}$ | Short-circuit current | | | ±375 | ±550 | mA |
| $Z_O$ | Output impedance | DC, $I_O$ = 10 mA | | 5 | | Ω |
| **POWER SUPPLY** | | | | | | |
| $V_S$ | Operating voltage range | | ±2.25 | | ±18 | V |
| $I_Q$ | Quiescent current | $I_O$ = 0 mA | | 8.5 | 12 | mA |
| PSRR | Power-supply rejection ratio | $V_S$ = ±2.25 V to ±18 V | 64 | 75 | | dB |
| **THERMAL SHUTDOWN** | | | | | | |
| | Thermal shutdown temperature | | | 180 | | °C |

(1) Based on electrical characterization over temperature of 35 devices.

## 6.7 Electrical Characteristics: Low-Quiescent-Current Mode for SOIC Package

at $T_A$ = 25°C, $V_S$ = ±15 V, BW pin left open, and $R_L$ = 100 Ω connected to mid-supply (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **AC PERFORMANCE** | | | | | | |
| BW | Bandwidth, –3 dB | $R_L$ = 1 kΩ | | 35 | | MHz |
| | | $R_L$ = 100 Ω | | 31 | | |
| | Bandwidth for 0.1-dB flatness | $V_O$ = 10 $mV_{PP}$, $R_L$ = 100 Ω, $R_S$ = 50 Ω | | 2.3 | | MHz |
| SR | Slew rate | $V_O$ = 20-V step, $V_{IN}$-SR = 4000 V/µs | | 3750 | | V/µs |
| | Rise and fall time | $V_O$ = 200-mV step | | 4 | | ns |
| | Settling time to 0.1% | $V_O$ = 20-V step, $V_{IN}$-SR = 2500 V/µs | | 400 | | ns |
| | Settling time to 1% | $V_O$ = 20-V step, $V_{IN}$-SR = 2500 V/µs | | 90 | | ns |
| $e_n$ | Voltage noise | f = 1 kHz | | 8.1 | | nV/√Hz |
| $i_n$ | Current noise | f = 10 kHz | | 0.3 | | pA/√Hz |
| HD2 | 2nd-harmonic distortion | $V_O$ = 2 $V_{PP}$, f = 20 kHz | | –54 | | dBc |
| | | $V_O$ = 10 $V_{PP}$, f = 20 kHz | | –65 | | |
| HD3 | 3rd-harmonic distortion | $V_O$ = 2 $V_{PP}$, f = 20 kHz | | –40 | | dBc |
| | | $V_O$ = 10 $V_{PP}$, f = 20 kHz | | –44 | | |
| **DC PERFORMANCE** | | | | | | |
| $V_{OS}$ | Input offset voltage | $T_A$ = 25°C | | 36 | 65 | mV |
| | Input offset voltage drift(1) | $T_A$ = –40°C to 125°C | | 175 | | µV/°C |
| $I_B$ | Input bias current | $V_{IN}$ = 0 V | | 0.03 | 0.25 | µA |
| G | Gain | $V_O$ = ±10 V, $R_L$ = 1 kΩ | 0.95 | 0.99 | | V/V |
| | | $V_O$ = ±10 V, $R_L$ = 100 Ω | 0.93 | 0.95 | | |
| | | $V_O$ = ±10 V, $R_L$ = 67 Ω | 0.91 | 0.93 | | |
| **INPUT** | | | | | | |
| | Linear input voltage range | $R_L$ = 1 kΩ, $I_B$ < 10 µA | –13 | | 13 | V |
| $Z_{IN}$ | Input impedance | $R_L$ = 100 Ω | | 1400 \|\| 5 | | MΩ \|\| pF |
| **OUTPUT** | | | | | | |
| | Output headroom to supplies | $I_O$ = ±10 mA | | 1.6 | 1.8 | V |
| | | $I_O$ = ±100 mA | | 2.0 | 2.2 | |
| | | $I_O$ = ±150 mA | | 2.2 | 2.5 | |
| $I_O$ | Current output, continuous | | | ±250 | | mA |
| $I_{SC}$ | Short-circuit current | | | ±350 | ±550 | mA |
| $Z_O$ | Output impedance | DC, $I_O$ = 10 mA | | 7 | | Ω |
| **POWER SUPPLY** | | | | | | |
| $V_S$ | Operating voltage range | | ±2.25 | | ±18 | V |
| $I_Q$ | Quiescent current | $I_O$ = 0 mA | | 1.5 | 2.3 | mA |
| PSRR | Power-supply rejection ratio | $V_S$ = ±2.25 V to ±18 V | 64 | 80 | | dB |
| **THERMAL SHUTDOWN** | | | | | | |
| | Thermal shutdown temperature | | | 180 | | °C |

(1) Based on electrical characterization over temperature of 35 devices.

## 6.8 Typical Characteristics: TO-220 and TO-263 Packages

at $T_A$ = 25°C, $V_S$ = ±15 V (unless otherwise noted)

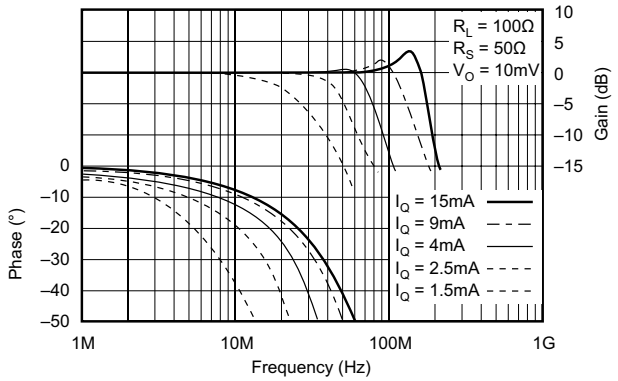



**Figure 6-1. Gain and Phase vs Frequency vs Quiescent Current**

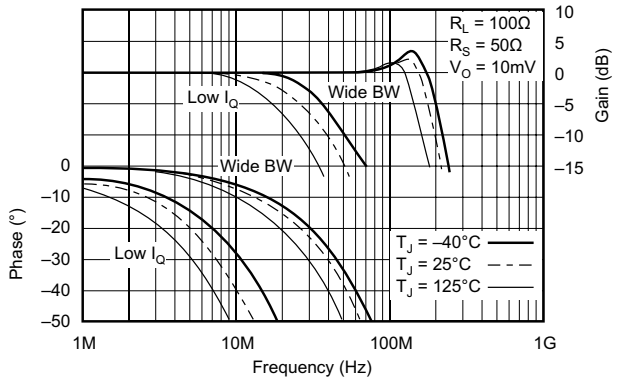



**Figure 6-2. Gain and Phase vs Frequency vs Temperature**

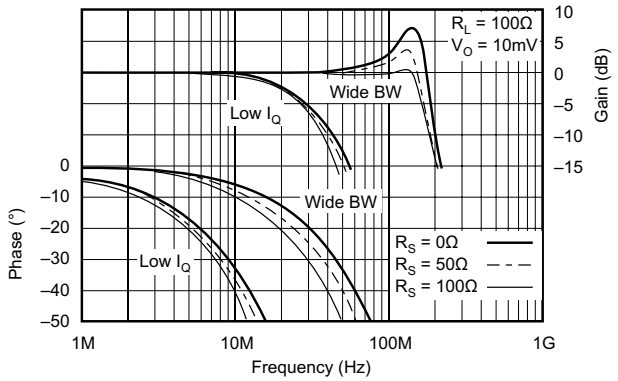



**Figure 6-3. Gain and Phase vs Frequency vs Source Resistance**

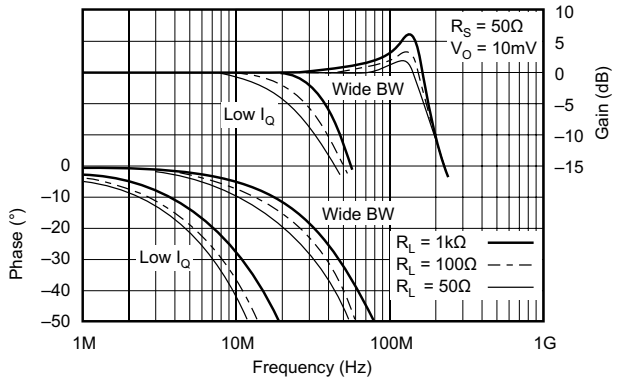



**Figure 6-4. Gain and Phase vs Frequency vs Load Resistance**

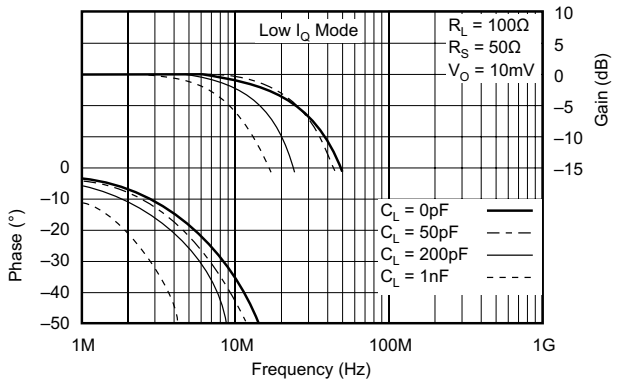



**Figure 6-5. Gain and Phase vs Frequency vs Load Capacitance**

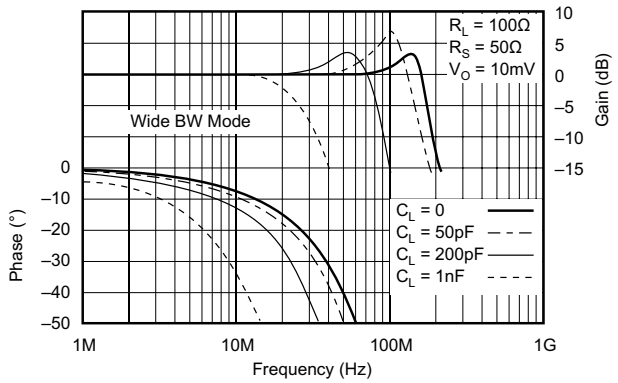



**Figure 6-6. Gain and Phase vs Frequency vs Load Capacitance**

## 6.8 Typical Characteristics: TO-220 and TO-263 Packages (continued)

at $T_A$ = 25°C, $V_S$ = ±15 V (unless otherwise noted)

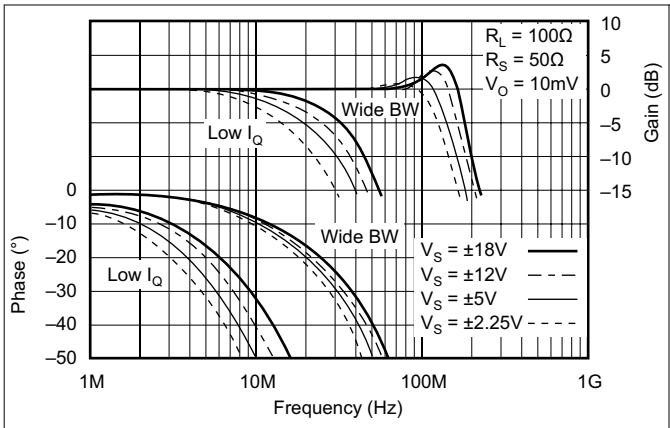



**Figure 6-7. Gain and Phase vs Frequency vs Power Supply Voltage**

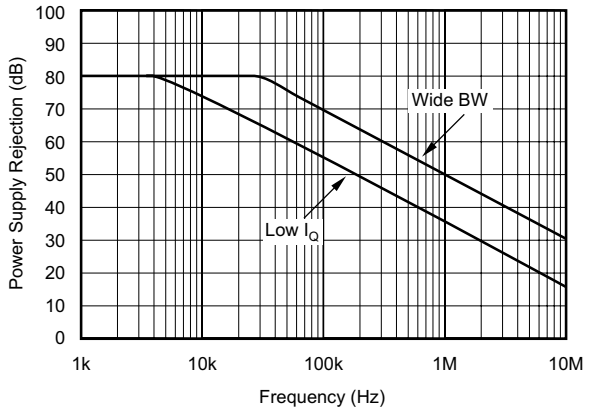



**Figure 6-8. Power Supply Rejection vs Frequency**

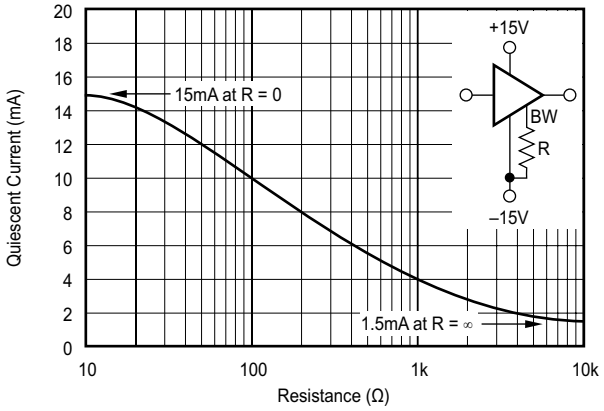



**Figure 6-9. Quiescent Current vs Bandwidth Control Resistance**

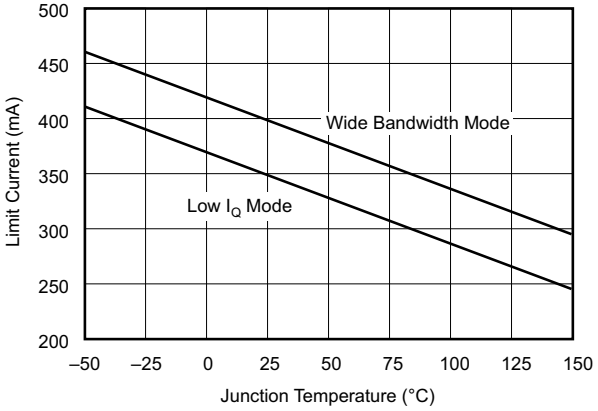



**Figure 6-10. Short-Circuit Current vs Temperature**

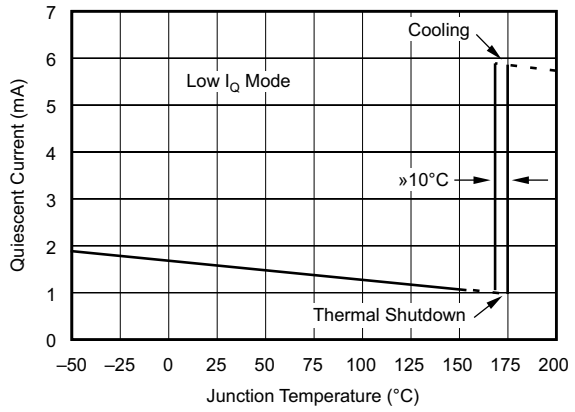



**Figure 6-11. Quiescent Current vs Temperature**

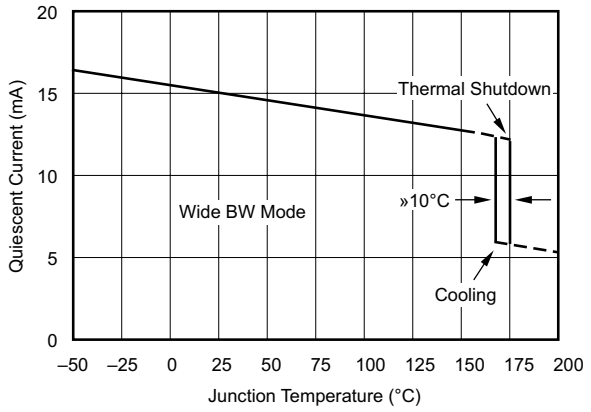



**Figure 6-12. Quiescent Current vs Temperature**

## 6.8 Typical Characteristics: TO-220 and TO-263 Packages (continued)

at $T_A$ = 25°C, $V_S$ = ±15 V (unless otherwise noted)

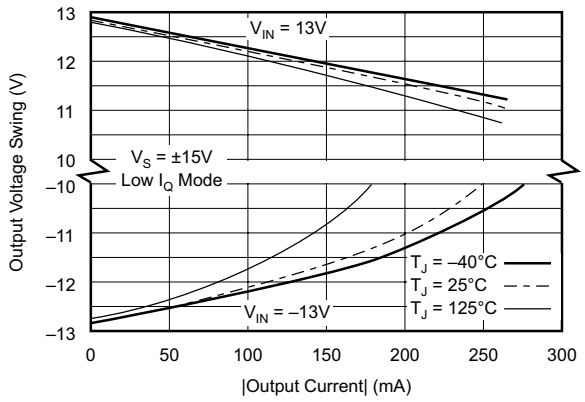



**Figure 6-13. Output Voltage Swing vs Output Current**

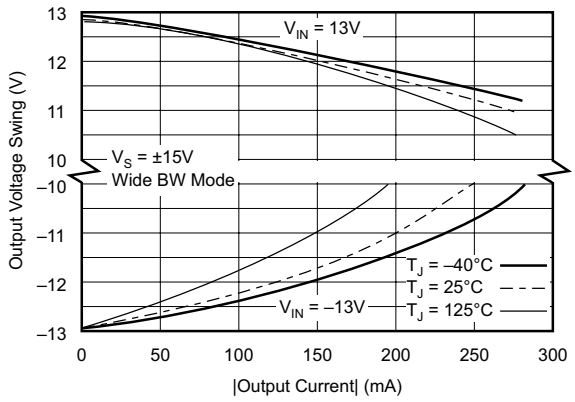



**Figure 6-14. Output Voltage Swing vs Output Current**

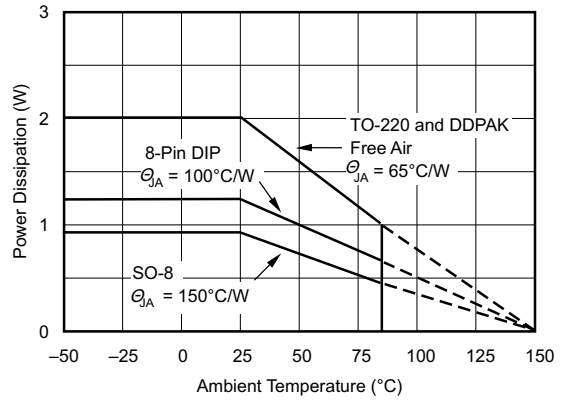



**Figure 6-15. Maximum Power Dissipation vs Temperature**

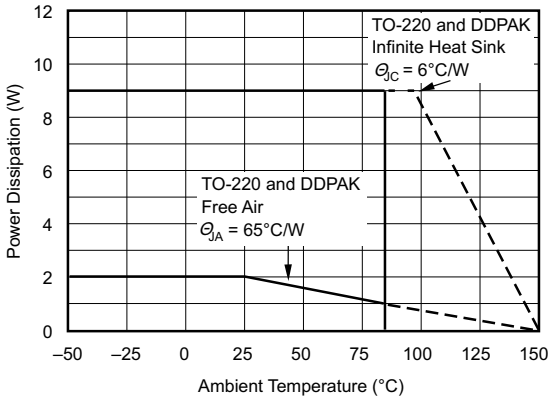
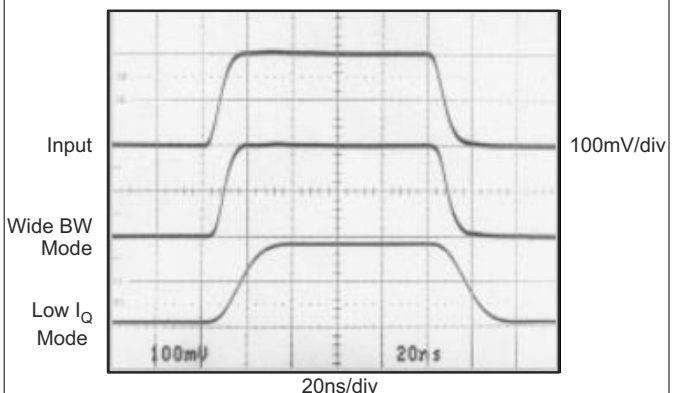
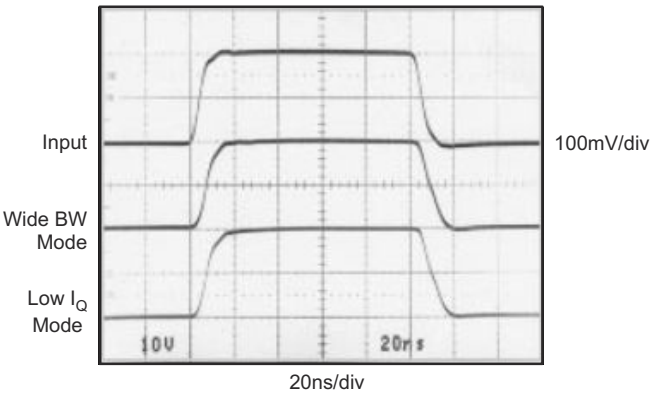



**Figure 6-16. Maximum Power Dissipation vs Temperature**




$R_S$ = 50 Ω, $R_L$ = 100 Ω

**Figure 6-17. Small-Signal Response**




$R_S$ = 50 Ω, $R_L$ = 100 Ω

**Figure 6-18. Large-Signal Response**

## 6.9 Typical Characteristics: SOIC Package

at $T_A$ = 25°C, $V_S$ = ±15 V, $R_S$ = 50 Ω, and $R_L$ = 100 Ω (unless otherwise noted).

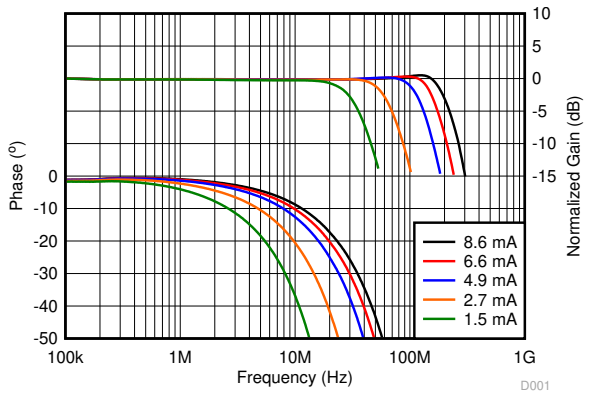
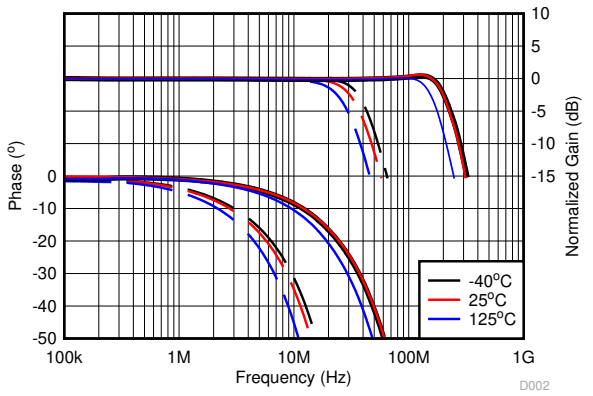
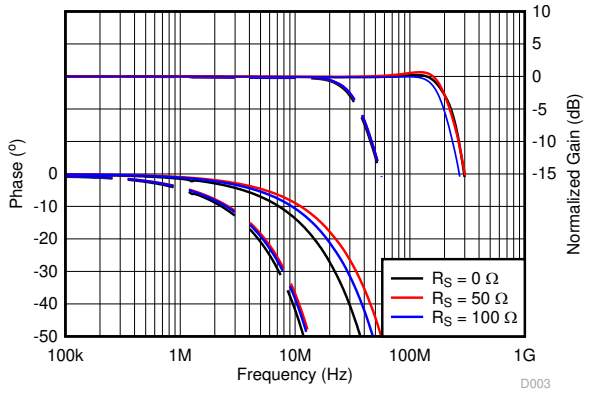



**Figure 6-19. Gain and Phase vs Frequency and Quiescent Current**



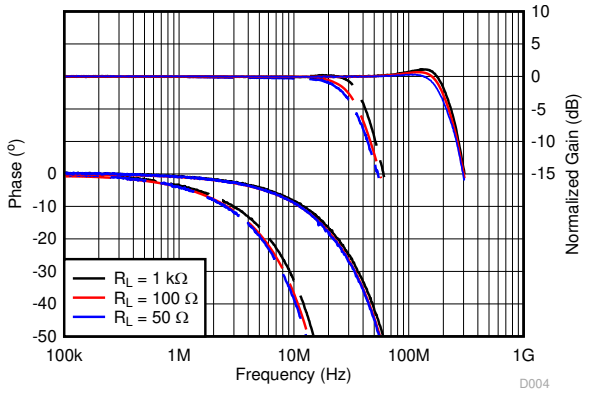

Solid lines indicate wide-BW mode, dashed lines indicate low-$I_Q$ mode

**Figure 6-20. Gain and Phase vs Frequency and Temperature**



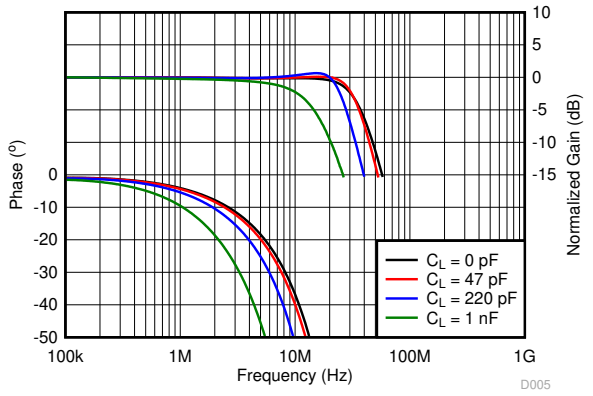

Solid lines indicate wide-BW mode, dashed lines indicate low-$I_Q$ mode

**Figure 6-21. Gain and Phase vs Frequency and Source Resistance**



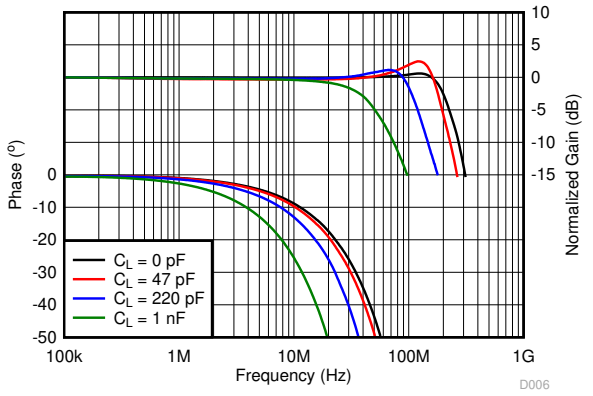

Solid lines indicate wide-BW mode, dashed lines indicate low-$I_Q$ mode

**Figure 6-22. Gain and Phase vs Frequency and Load Resistance**




Low-$I_Q$ mode

**Figure 6-23. Gain and Phase vs Frequency and Load Capacitance**

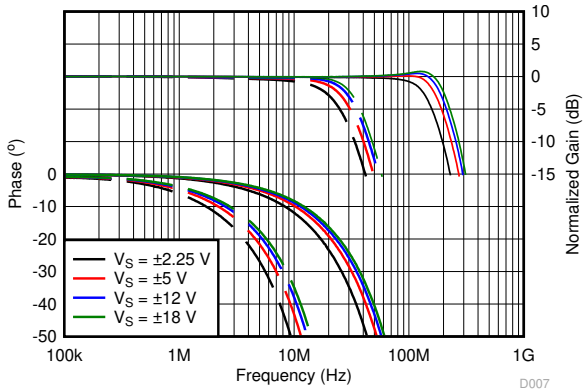



Wide-BW mode

**Figure 6-24. Gain and Phase vs Frequency and Load Capacitance**

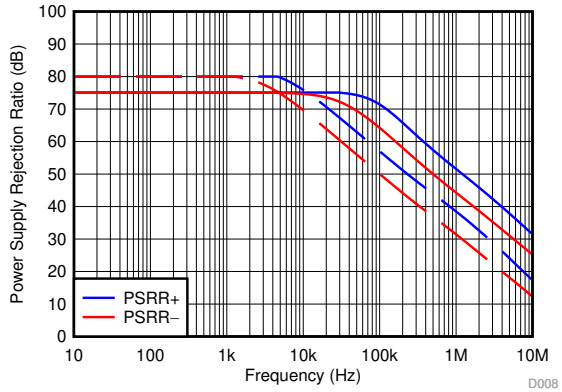
## 6.9 Typical Characteristics: SOIC Package (continued)

at $T_A$ = 25°C, $V_S$ = ±15 V, $R_S$ = 50 Ω, and $R_L$ = 100 Ω (unless otherwise noted).




Solid lines indicate wide-BW mode, dashed lines indicate low-$I_Q$ mode

**Figure 6-25. Gain and Phase vs Frequency and Power-Supply Voltage**




Solid lines indicate wide-BW mode, dashed lines indicate low-$I_Q$ mode

**Figure 6-26. PSRR vs Frequency**

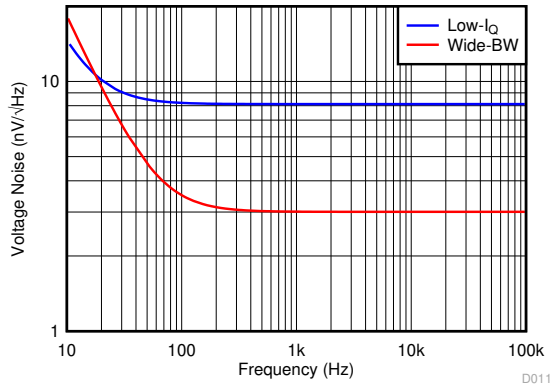



**Figure 6-27. Voltage Noise Density vs Frequency**

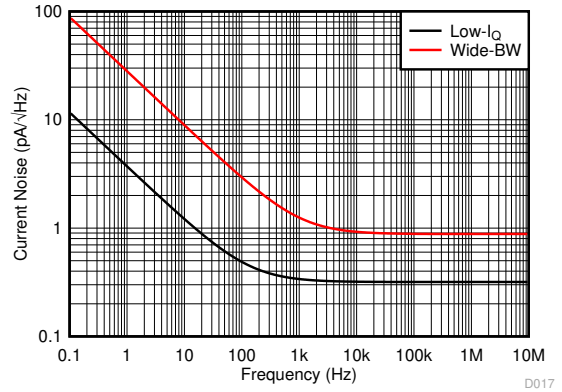
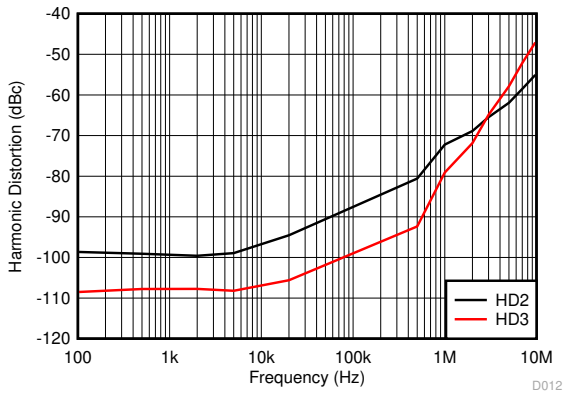
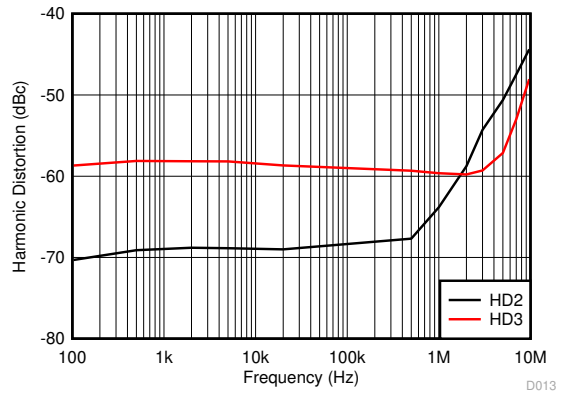



**Figure 6-28. Current Noise Density vs Frequency**




Wide-BW mode, $V_{IN}$ = 10 $V_{PP}$, $R_L$ = 1 kΩ

**Figure 6-29. Harmonic Distortion vs Frequency**

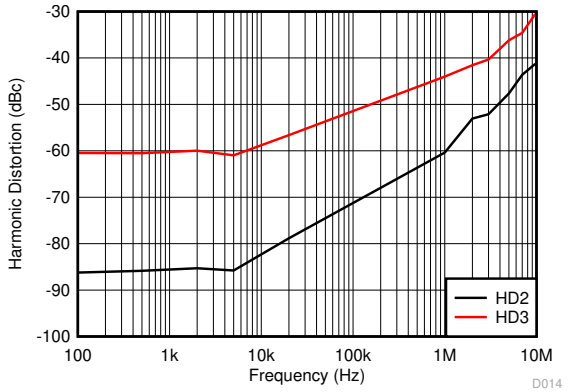



Wide-BW mode, $V_{IN}$ = 10 $V_{PP}$, $R_L$ = 100 Ω

**Figure 6-30. Harmonic Distortion vs Frequency**

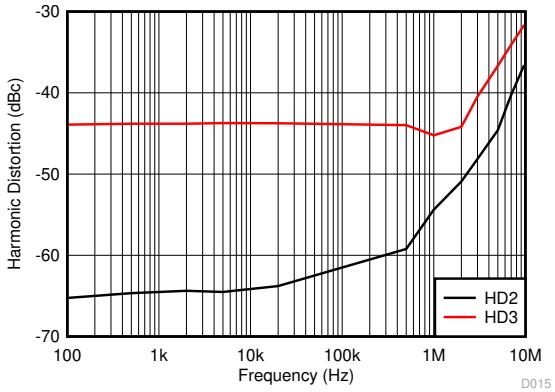
## 6.9 Typical Characteristics: SOIC Package (continued)

at $T_A$ = 25°C, $V_S$ = ±15 V, $R_S$ = 50 Ω, and $R_L$ = 100 Ω (unless otherwise noted).




Low-$I_Q$ mode, $V_{IN}$ = 10 $V_{PP}$, $R_L$ = 1 kΩ

**Figure 6-31. Harmonic Distortion vs Frequency**




Low-$I_Q$ mode, $V_{IN}$ = 10 $V_{PP}$, $R_L$ = 100 Ω

**Figure 6-32. Harmonic Distortion vs Frequency**

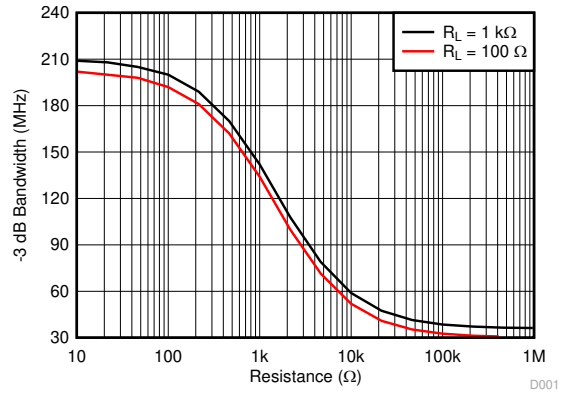



**Figure 6-33. Small-Signal Bandwidth vs Bandwidth Adjustment Resistance**

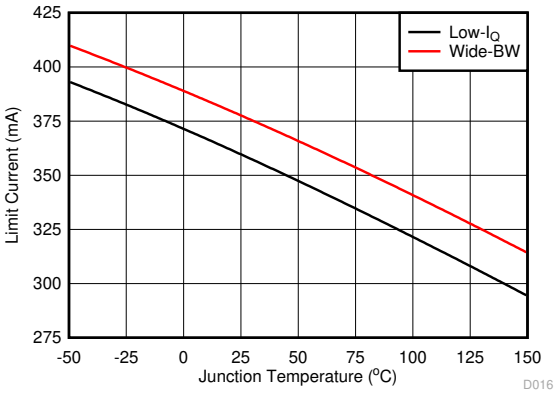
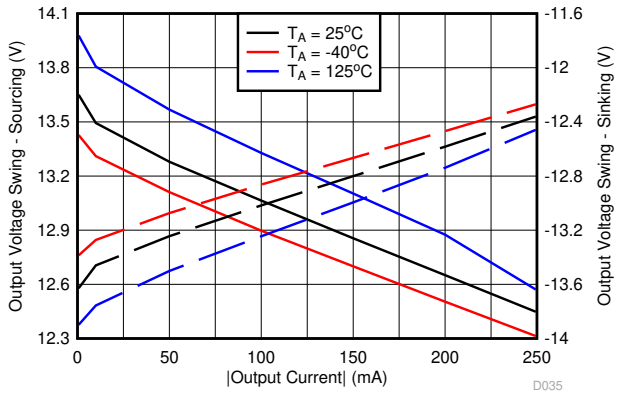
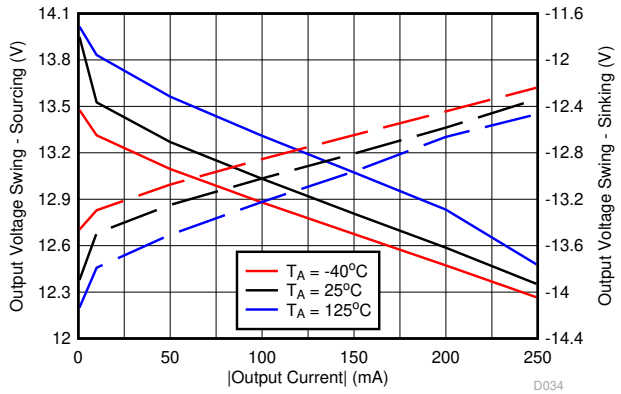



**Figure 6-34. Short-Circuit Current vs Temperature**




Wide-BW mode (solid lines indicate sourcing current, dashed lines indicate sinking current)

**Figure 6-35. Output Voltage Swing vs Output Current**




Low-$I_Q$ mode (solid lines indicate sourcing current, dashed lines indicate sinking current)

**Figure 6-36. Output Voltage Swing vs Output Current**

## 6.9 Typical Characteristics: SOIC Package (continued)

at $T_A$ = 25°C, $V_S$ = ±15 V, $R_S$ = 50 Ω, and $R_L$ = 100 Ω (unless otherwise noted).

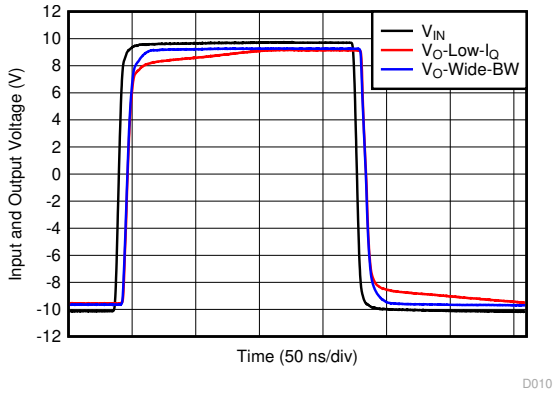



**Figure 6-37. Large-Signal Transient Response**

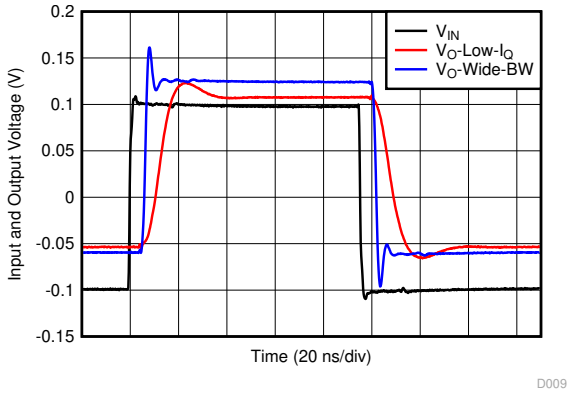
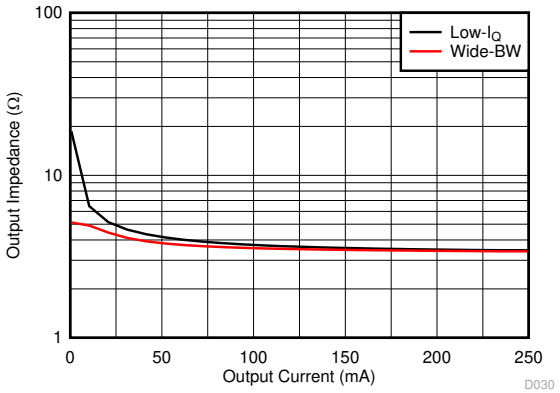
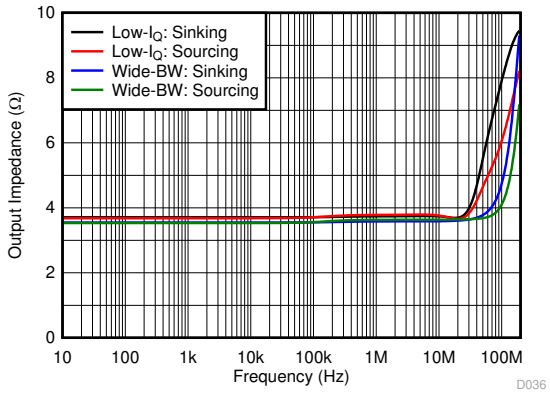



**Figure 6-38. Small-Signal Transient Response**




f = 100 kHz

**Figure 6-39. Output Impedance vs Output Current**




$I_O$ = 100 mA

**Figure 6-40. Output Impedance vs Frequency**

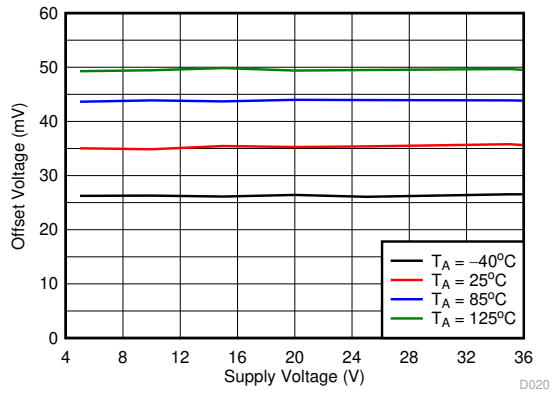
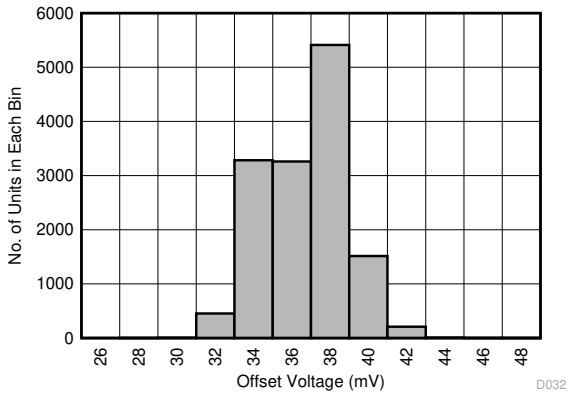



**Figure 6-41. Offset Voltage vs Supply Voltage**

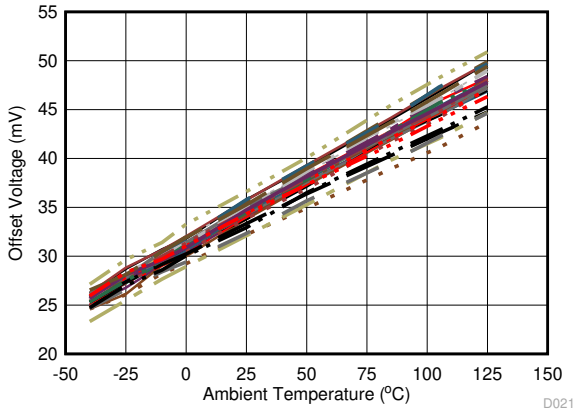



14000 devices, μ = 35.7 mV, σ = 2.15 mV

**Figure 6-42. Offset Voltage Distribution Histogram**

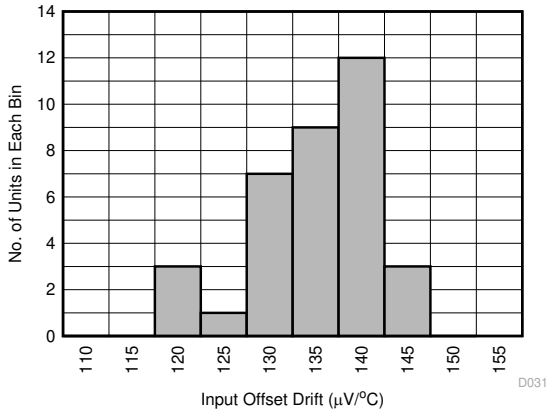
## 6.9 Typical Characteristics: SOIC Package (continued)

at $T_A$ = 25°C, $V_S$ = ±15 V, $R_S$ = 50 Ω, and $R_L$ = 100 Ω (unless otherwise noted).



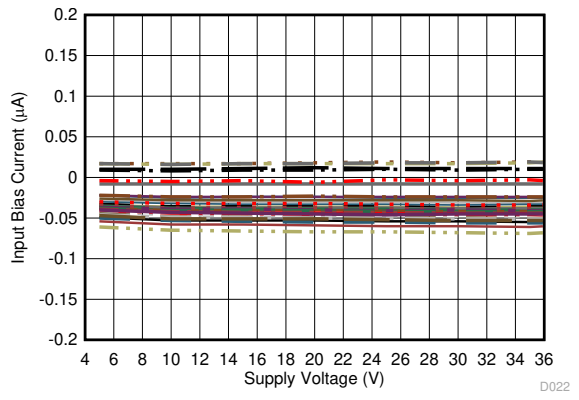

35 devices

**Figure 6-43. Offset Voltage vs Temperature**



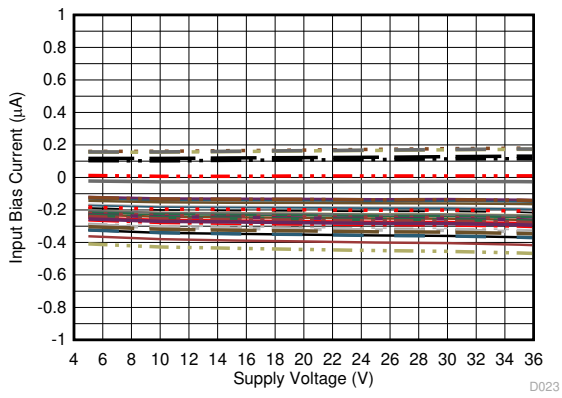

$T_A$ = –40°C to +125°C, 35 devices,
µ = 134 µV/°C, σ = 7.4 µV/°C

**Figure 6-44. Offset Voltage Drift Distribution Histogram**



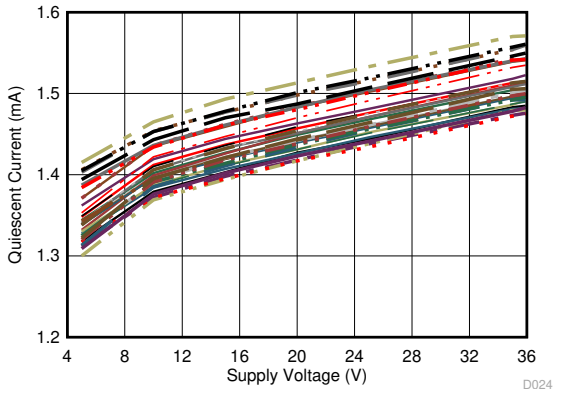

Low-$I_Q$ mode, 35 devices

**Figure 6-45. Input Bias Current vs Supply Voltage**



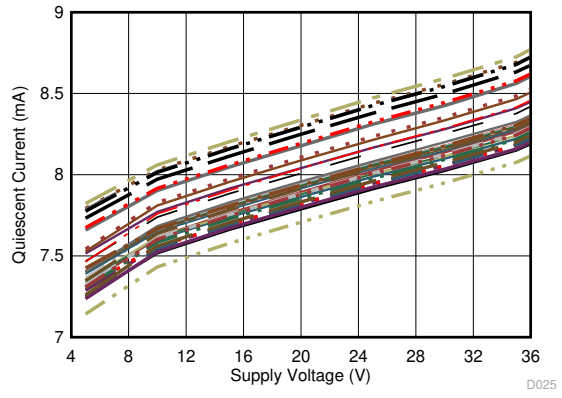

Wide-BW mode, 35 devices

**Figure 6-46. Input Bias Current vs Supply Voltage**




Low-$I_Q$ mode, 35 devices

**Figure 6-47. Quiescent Current vs Supply Voltage**

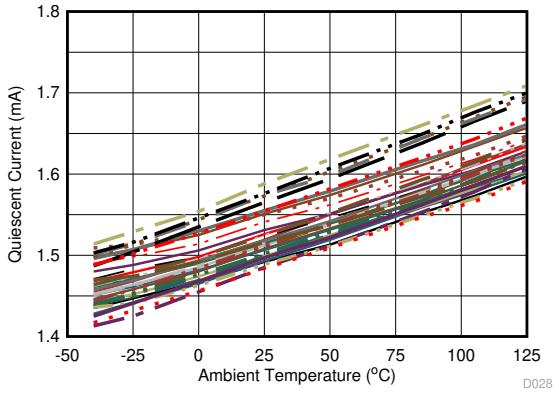



Wide-BW mode, 35 devices

**Figure 6-48. Quiescent Current vs Supply Voltage**

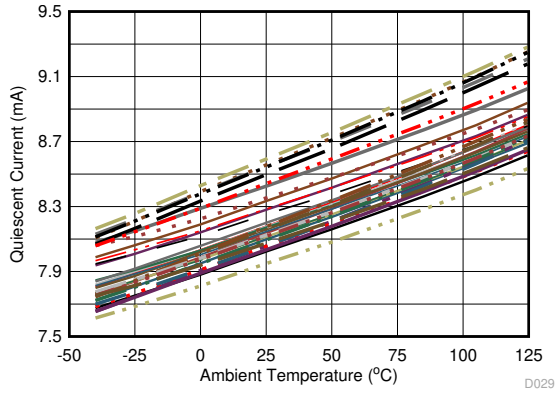
## 6.9 Typical Characteristics: SOIC Package (continued)

at $T_A$ = 25°C, $V_S$ = ±15 V, $R_S$ = 50 Ω, and $R_L$ = 100 Ω (unless otherwise noted).



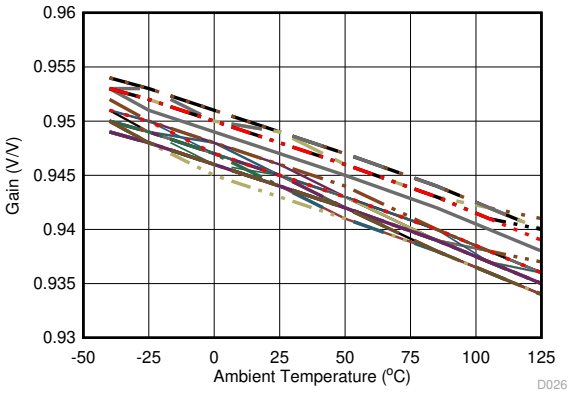

Low-$I_Q$ mode, 35 devices

**Figure 6-49. Quiescent Current vs Temperature**



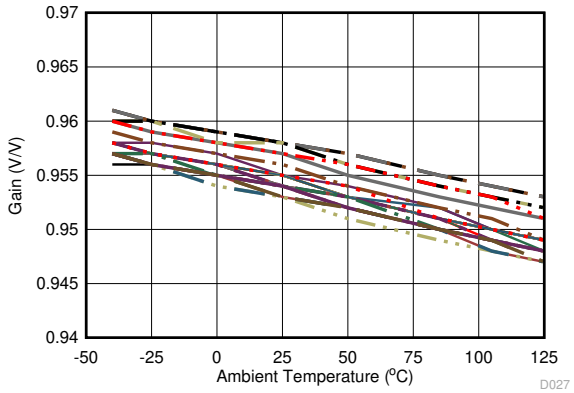

Wide-BW mode, 35 devices

**Figure 6-50. Quiescent Current vs Temperature**




Low-$I_Q$ mode, 35 devices

**Figure 6-51. Buffer Gain vs Temperature**




Wide-BW mode, 35 devices

**Figure 6-52. Buffer Gain vs Temperature**

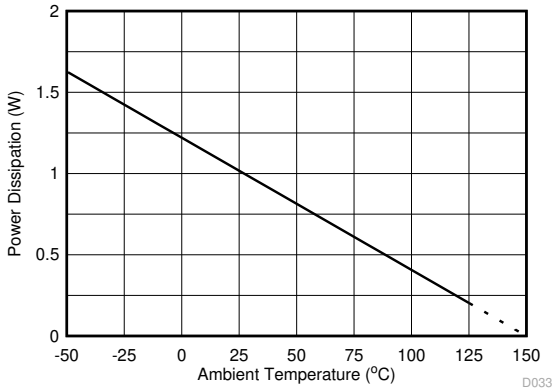



**Figure 6-53. Maximum Power Dissipation vs Temperature**

# 7 Detailed Description

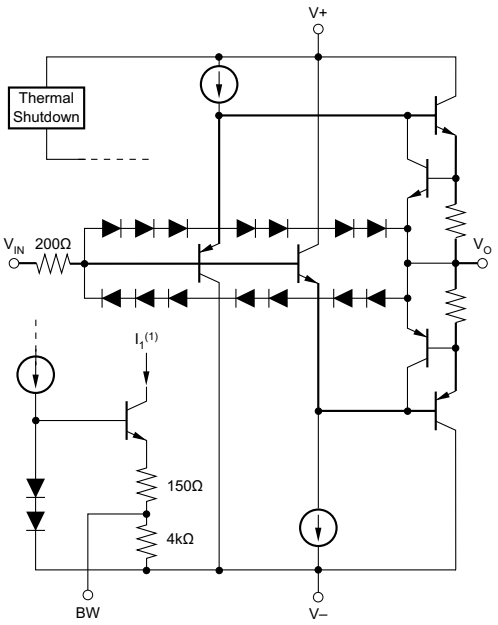
## 7.1 Overview

The BUF634 device is a high-speed, unity-gain open-loop buffer recommended for a wide range of applications. The BUF634 can be used inside the feedback loop of op amps to increase output current, eliminate thermal feedback, and improve capacitive load drive.

For low-power applications, the BUF634 operates on 1.5-mA quiescent current with 250-mA output, 2000-V/µs slew rate, and 30-MHz bandwidth. Bandwidth can be adjusted from 30 MHz to 180 MHz by connecting a resistor between V– and the BW pin; see Figure 6-9 and Figure 6-1. Output circuitry is fully protected by internal current limit and thermal shutdown, making this device rugged and easy to use.

For a simplified circuit diagram of the BUF634 showing the open-loop complementary follower design, see *Section 7.2*.

## 7.2 Functional Block Diagram




Signal path indicated in bold.
Note: (1) Stage currents are set by $I_1$.

**Figure 7-1. Internal Block Diagram: TO-220 and TO-263**

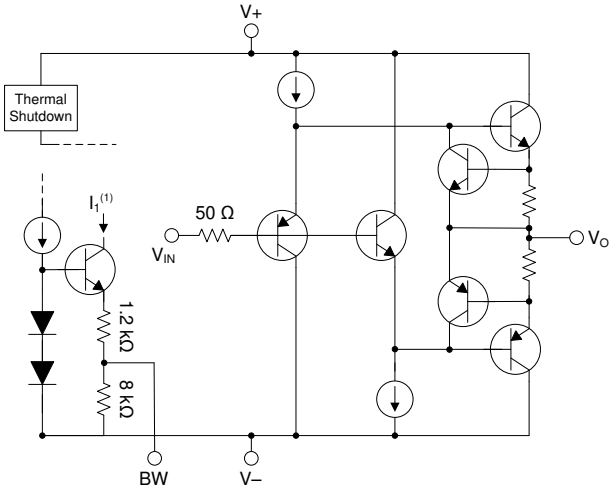



**Figure 7-2. Internal Block Diagram: SOIC**

## 7.3 Feature Description

### 7.3.1 Output Current

The BUF634 delivers up to ±250-mA continuous output current. Internal circuitry limits output current to approximately ±350 mA; see Figure 6-10. For many applications, however, the continuous output current is limited by thermal effects.

The output voltage swing capability varies with junction temperature and output current; see Figure 6-14. Although all four package types are tested for the same output performance using a high speed test, the higher junction temperatures with the DIP and SO-8 package types often provide less output voltage swing. Junction temperature is reduced in the TO-263 surface-mount power package because this package is soldered directly to the circuit board. The TO-220 package used with a good heat sink further reduces junction temperature, allowing maximum possible output swing.

## 7.4 Device Functional Modes

The BUF634 is operational when the power-supply voltage is greater than 4.5 V (±2.25 V). The maximum power supply voltage for the BUF634 is 36 V (±18 V). At low power supply conditions, such as ±2.25 V, the output swing can be limited. For additional information, see *Section 6.5*.

# 8 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 8.1 Application Information

Figure 8-1 shows the BUF634 device connected as an open-loop buffer. The source impedance and optional input resistor, $R_S$, influence frequency response: see *Section 6.8*. Bypass power supplies with capacitors connected close to the device pins. Capacitor values as low as 0.1 µF provide stable operation in most applications, but high output current and fast output slewing can demand large current transients from the power supplies. Solid tantalum 10-µF capacitors are recommended. High-frequency, open-loop applications can benefit from special bypassing and layout considerations. For more information, see *Section 8.1.1*.

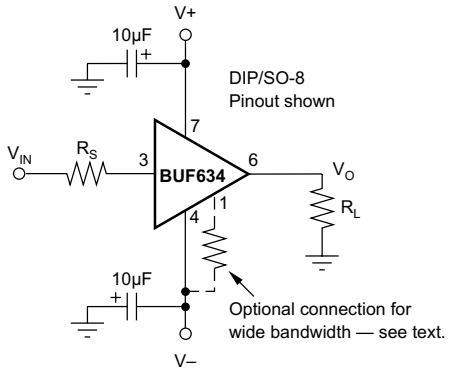



**Figure 8-1. Buffer Connections**

### 8.1.1 High Frequency Applications

The excellent bandwidth and fast slew rate of the BUF634 device are useful in a variety of high frequency open-loop applications. When operated open-loop, printed-circuit-board layout and bypassing technique can affect dynamic performance.

For best results, use a ground plane-type circuit board layout and bypass the power supplies with 0.1-µF ceramic chip capacitors at the device pins in parallel with solid tantalum 10-µF capacitors. Source resistance affects high-frequency peaking, step-response overshoot and ringing. Best response is usually achieved with a series input resistor of 25 Ω to 200 Ω, depending on the signal source. Response with some loads (especially capacitive) can be improved with a resistor of 10 Ω to 150 Ω in series with the output.

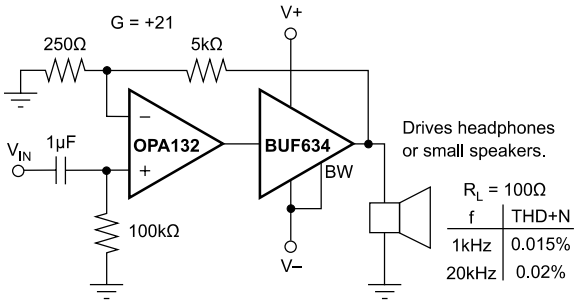



**Figure 8-2. High Performance Headphone Driver**

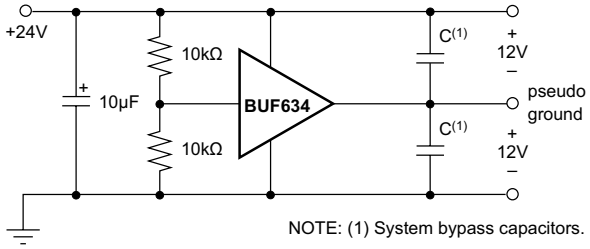



**Figure 8-3. Pseudo-Ground Driver**

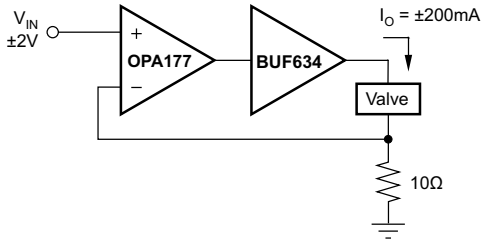



**Figure 8-4. Current-Output Valve Driver**

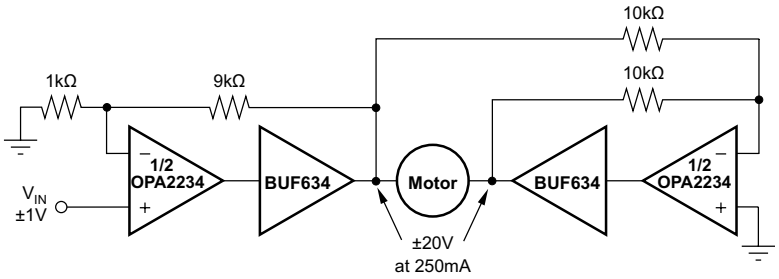
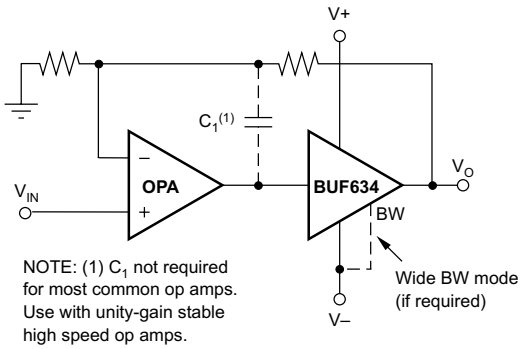



**Figure 8-5. Bridge-Connected Motor Driver**

## 8.2 Typical Application

### 8.2.1 Boosting Op Amp Output Current

The BUF634 device can be connected inside the feedback loop of most op amps to increase output current (see Figure 8-6). When connected inside the feedback loop, the offset voltage of the BUF634 device and other errors are corrected by the feedback of the op amp.




| OP AMP | RECOMMENDATIONS |
|---|---|
| OPA177, OPA1013<br>OPA111, OPA2111<br>OPA121, OPA234(1),<br>OPA130(1) | Use Low $I_Q$ mode. G = 1 stable. |
| OPA27, OPA2107<br>OPA602, OPA131(1) | Low $I_Q$ mode is stable. Increasing $C_L$ may cause excessive ringing or instability. Use Wide BW mode. |
| OPA627, OPA132(1) | Use Wide BW mode, $C_1$ = 200pF. G = 1 stable. |
| OPA637, OPA37 | Use Wide BW mode. These op amps are not G = 1 stable. Use in G > 4. |

NOTE: (1) Single, dual, and quad versions.

**Figure 8-6. Boosting Op Amp Output Current**

#### *8.2.1.1 Design Requirements*

- Boost the output current of an OPA627
- Operate from ±15V power supplies
- Operate from -40°C to +85°C
- Gain = 23.5 V/V
- Output current = ±250 mA
- Bandwidth greater than 100 kHz

#### *8.2.1.2 Detailed Design Procedure*

To make sure that the composite amplifier remains stable, the phase shift of the BUF634 must remain small throughout the loop gain of the circuit. For a G = +1 op-amp circuit, the BUF634 must contribute little additional phase shift (approximately 20° or less) at the unity-gain frequency of the op amp. Phase shift is affected by various operating conditions that can affect stability of the op amp; see *Section 6.8*.

Most general-purpose or precision op amps remain unity-gain stable with the BUF634 connected inside the feedback loop as shown. Large capacitive loads can require the BUF634 to be connected for wide bandwidth and stable operation. High-speed or fast-settling op amps generally require the wide bandwidth mode to remain stable and to maintain good dynamic performance. To check for stability with an op amp, look for oscillations or excessive ringing on signal pulses with the intended load, and worst-case conditions that affect phase response of the buffer. Connect the circuit as shown in Figure 8-6. Choose resistors to provide a voltage gain of 23.5 V/V. Select the feedback resistor to be 2.7 kΩ. Choose the input resistor to be 120 Ω.

#### 8.2.1.3 Application Curve

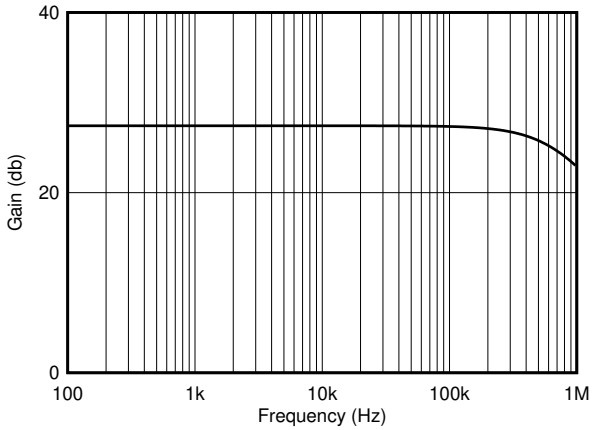



**Figure 8-7. Frequency Response of Composite Amplifier**

## 8.3 Power Supply Recommendations

The BUF634 is specified for operation from 4.5V to 36 V (±2.25 V to ±18 V). Many specifications apply from –40°C to +85°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in *Section 6.8*.

## 8.4 Layout

### 8.4.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information refer to *Circuit Board Layout Techniques*, SLOA089.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in Figure 8-9
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Clean the PCB following board assembly for best performance.
- Any precision integrated circuit can experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, bake the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

Power dissipated in the BUF634 causes the junction temperature to rise. A thermal protection circuit in the BUF634 disables the output when the junction temperature reaches approximately 175°C. When the thermal protection is activated, the output stage is disabled, allowing the device to cool. Quiescent current is approximately 6 mA during thermal shutdown. When the junction temperature cools to approximately 165°C, the output circuitry is again enabled. The die overheating can cause the protection circuit to cycle on and off with a

period ranging from a fraction of a second to several minutes or more, depending on package type, signal, load and thermal environment.

The thermal protection circuit is designed to prevent damage during abnormal conditions. Any tendency to activate the thermal protection circuit during normal operation is a sign of an inadequate heat sink or excessive power dissipation for the package type.

The TO-220 package provides the best thermal performance. When the TO-220 is used with a properly sized heat sink, output is not limited by thermal performance. The TO-263 also has excellent thermal characteristics; for good heat dissipation, solder the mounting tab to a circuit board copper area. Figure 8-8 shows typical thermal resistance from junction to ambient as a function of the copper area. The mounting tab of the TO-220 and TO-263 packages is electrically-connected to the V– power supply.

The DIP and SO-8 surface-mount packages are excellent for applications requiring high output current with low average power dissipation. To achieve the best possible thermal performance with the DIP or SO-8 packages, solder the device directly to a circuit board. Because much of the heat is dissipated by conduction through the package pins, sockets degrade thermal performance. Use wide circuit board traces on all the device pins, including pins that are not connected. With the DIP package, use traces on both sides of the printed circuit board if possible.

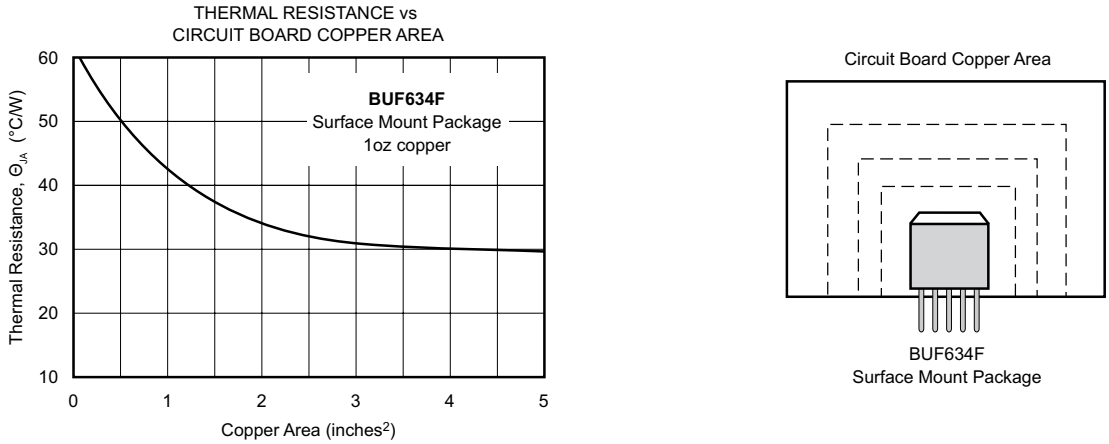



**Figure 8-8. Thermal Resistance vs Circuit Board Copper Area**

### *8.4.1.1 Power Dissipation*

Power dissipation depends on power supply voltage, signal, and load conditions. With dc signals, power dissipation is equal to the product of output current times the voltage across the conducting output transistor, $V_S$ – $V_O$. Power dissipation can be minimized by using the lowest possible power supply voltage necessary to provide the required output voltage swing.

For resistive loads, the maximum power dissipation occurs at a dc output voltage of one-half the power supply voltage. Dissipation with ac signals is lower. The *Power Amplifier Stress And Power Handling Limitations* application bulletin explains how to calculate or measure power dissipation with unusual signals and loads.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, limit the junction temperature to 150°C, maximum. To estimate the margin of safety in a complete design, increase the ambient temperature until the thermal protection is triggered. The thermal protection triggers more than 45°C greater than the maximum expected ambient condition of your application.

### 8.4.2 Layout Example

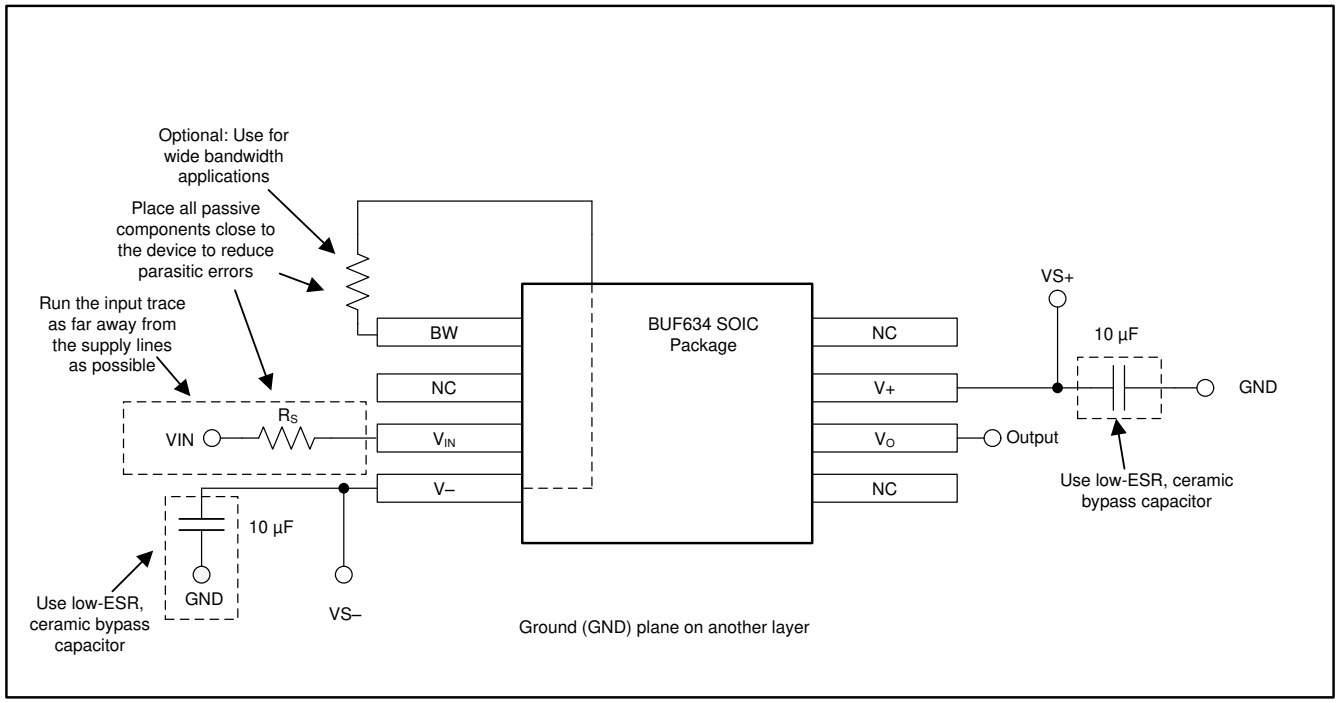



**Figure 8-9. BUF634 Layout Example**

# 9 Device and Documentation Support

## 9.1 Device Support

### 9.1.1 Development Support

#### *9.1.1.1 TINA-TI™ Simulation Software (Free Download)*

TINA-TI™ simulation software is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI simulation software is a free, fully-functional version of the TINA™ software, preloaded with a library of macromodels, in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Design tools and simulation web page, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

**Note**

These files require that either the TINA software or TINA-TI software be installed. Download the free TINA-TI simulation software from the TINA-TI™ software folder.

#### *9.1.1.2 TI Reference Designs*

TI reference designs are analog solutions created by TI's precision analog applications experts. TI reference designs offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits. TI reference designs are available online at https://www.ti.com/reference-designs.

## 9.2 Documentation Support

### 9.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Combining an Amplifier With the BUF634* application bulletin
- Texas Instruments, *Add Current Limit to the BUF634* application bulletin
- Texas Instruments, *Power Amplifier Stress and Power Handling Limitations* application bulletin
- Texas Instruments, *Shelf-Life Evaluation of Lead-Free Component Finishes* application report

## 9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

### 9.5 Trademarks

TINA-TI™ and TI E2E™ are trademarks of Texas Instruments.
TINA™ is a trademark of DesignSoft, Inc.
All trademarks are the property of their respective owners.

### 9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.7 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

## 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision B (March 2019) to Revision C (March 2024) | Page |
|---|---|
| • Deleted PDIP package from data sheet | 1 |
| • Deleted most instances of DDPAK name from data sheet and replaced with TO-263 | 1 |
| • Deleted paragraph comparing BUF634 with BUF634A | 1 |
| • Changed BUF634F to BUF634U for SOIC and PDIP packages in *ESD Ratings* | 4 |
| • Changed values for D (SOIC) package in *Thermal Information* table | 4 |
| • Added *Electrical Characteristics* table specifically for TO-220 and TO-263 packages | 5 |
| • Added *Typical Characteristics* section specifically for TO-220 and TO-263 packages | 9 |
| • Added new block diagram for SOIC packages | 18 |

| Changes from Revision A (November 2015) to Revision B (March 2019) | Page |
|---|---|
| • Added discussion of BUF634A upgrade device to *Features* and *Description* sections | 1 |
| • Changed amplifier to OPA2810 and deleted table from *Boost the Output Current of any Operational Amplifier* figure | 1 |
| • Added *Device Comparison Table* | 2 |

| Changes from Revision * (September 2000) to Revision A (April 2015) | Page |
|---|---|
| • Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. | 1 |

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| BUF634F/500 | Last Time Buy | Production | DDPAK/ TO-263 (KTT) \| 5 | 500 \| LARGE T&R | Yes | SN | Level-2-260C-1 YEAR | -40 to 125 | BUF634F |
| BUF634F/500.A | NRND | Production | DDPAK/ TO-263 (KTT) \| 5 | 500 \| LARGE T&R | Yes | SN | Level-2-260C-1 YEAR | -40 to 125 | BUF634F |
| BUF634F/500E3 | NRND | Production | DDPAK/ TO-263 (KTT) \| 5 | 500 \| LARGE T&R | Yes | SN | Level-2-260C-1 YEAR | -40 to 125 | BUF634F |
| BUF634FKTTT | Last Time Buy | Production | DDPAK/ TO-263 (KTT) \| 5 | 250 \| SMALL T&R | Yes | SN | Level-2-260C-1 YEAR | -40 to 125 | BUF634F |
| BUF634FKTTT.A | NRND | Production | DDPAK/ TO-263 (KTT) \| 5 | 250 \| SMALL T&R | Yes | SN | Level-2-260C-1 YEAR | -40 to 125 | BUF634F |
| BUF634FKTTTE3 | NRND | Production | DDPAK/ TO-263 (KTT) \| 5 | 250 \| SMALL T&R | Yes | SN | Level-2-260C-1 YEAR | -40 to 125 | BUF634F |
| BUF634T | Last Time Buy | Production | TO-220 (KC) \| 5 | 49 \| TUBE | Yes | SN | N/A for Pkg Type | -40 to 125 | BUF634T |
| BUF634T.A | NRND | Production | TO-220 (KC) \| 5 | 49 \| TUBE | Yes | SN | N/A for Pkg Type | -40 to 125 | BUF634T |
| BUF634TG3 | NRND | Production | TO-220 (KC) \| 5 | 49 \| TUBE | Yes | SN | N/A for Pkg Type | -40 to 125 | BUF634T |
| BUF634U | NRND | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | BUF 634U |
| BUF634U.B | NRND | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | BUF 634U |
| BUF634U/2K5 | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | BUF 634U |
| BUF634U/2K5.B | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | BUF 634U |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

**(4) Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

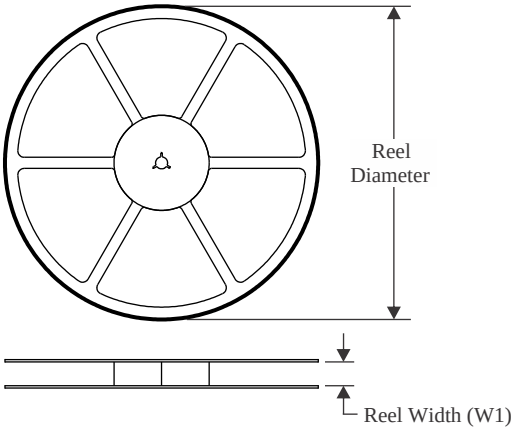
**(5) MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

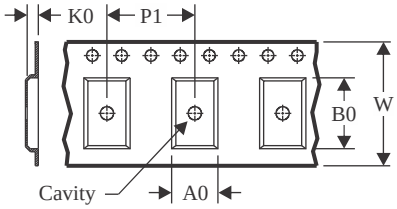
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

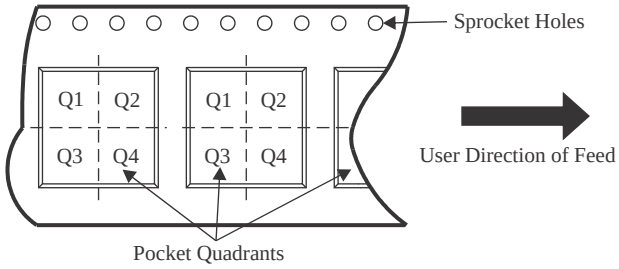



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

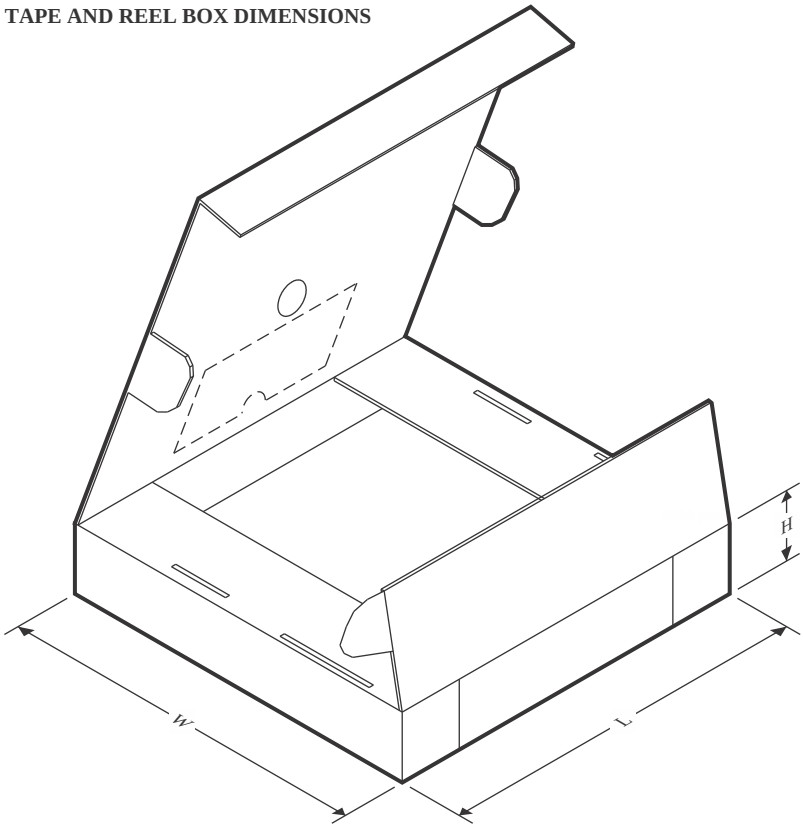
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| BUF634F/500 | DDPAK/ TO-263 | KTT | 5 | 500 | 330.0 | 24.4 | 10.9 | 16.1 | 4.9 | 16.0 | 24.0 | Q2 |
| BUF634FKTTT | DDPAK/ TO-263 | KTT | 5 | 250 | 330.0 | 24.4 | 10.9 | 16.1 | 4.9 | 16.0 | 24.0 | Q2 |
| BUF634U/2K5 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

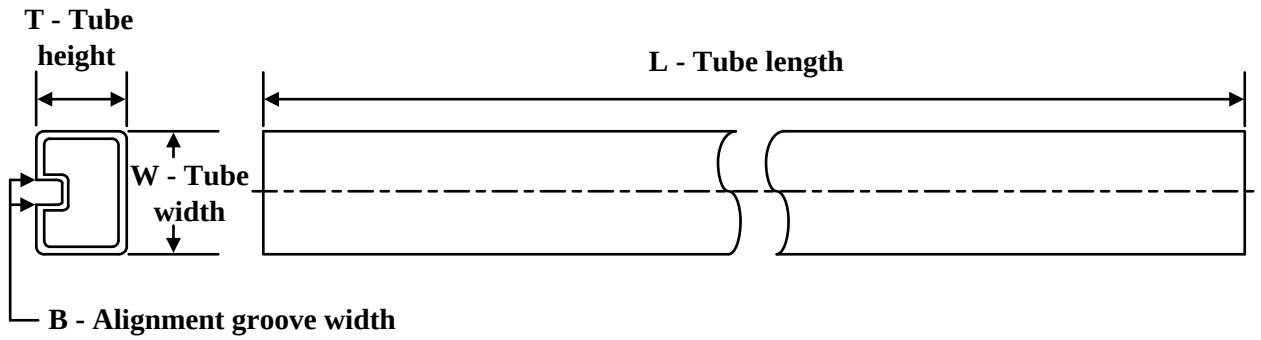
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

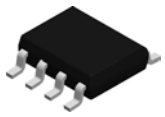
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| BUF634F/500 | DDPAK/TO-263 | KTT | 5 | 500 | 356.0 | 356.0 | 45.0 |
| BUF634FKTTT | DDPAK/TO-263 | KTT | 5 | 250 | 356.0 | 356.0 | 45.0 |
| BUF634U/2K5 | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |

## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| BUF634T | KC | TO-220 | 5 | 49 | 546 | 31 | 11930 | 3.17 |
| BUF634T.A | KC | TO-220 | 5 | 49 | 546 | 31 | 11930 | 3.17 |
| BUF634TG3 | KC | TO-220 | 5 | 49 | 546 | 31 | 11930 | 3.17 |
| BUF634U | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| BUF634U.B | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |

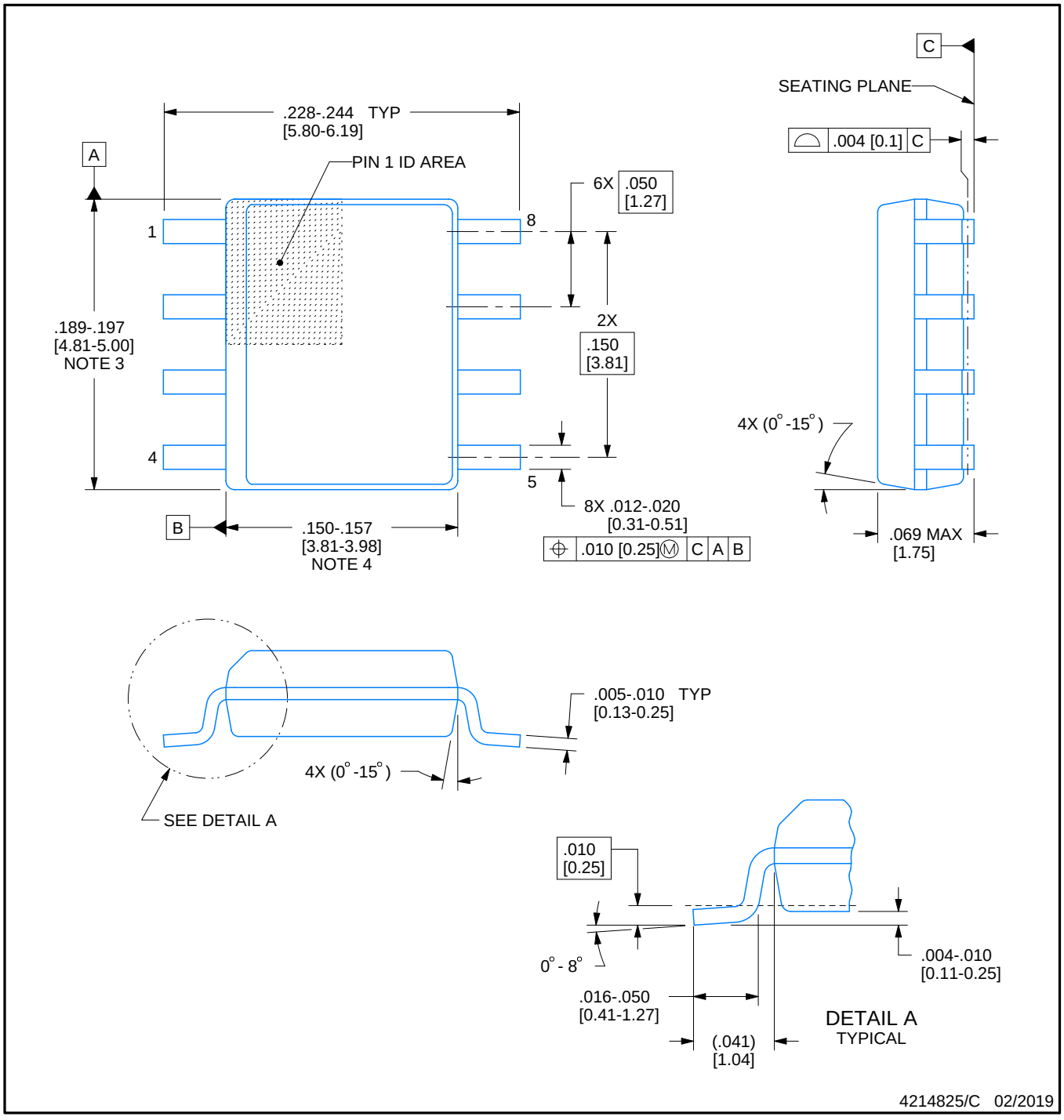


# PACKAGE OUTLINE

## D0008A

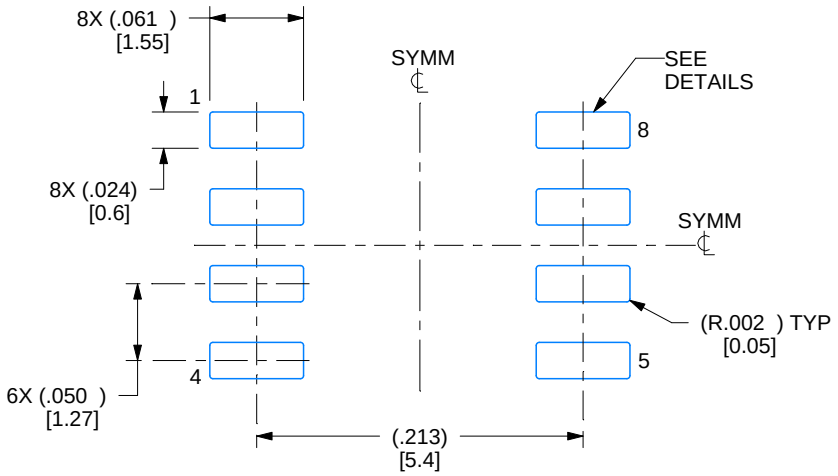
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

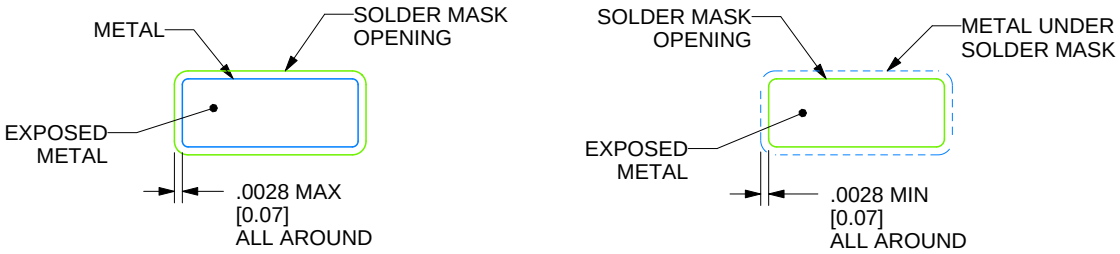



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

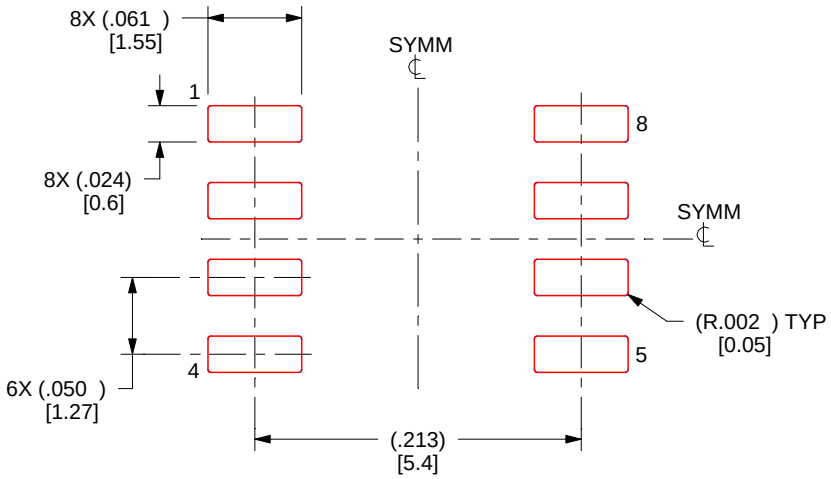
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0008A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

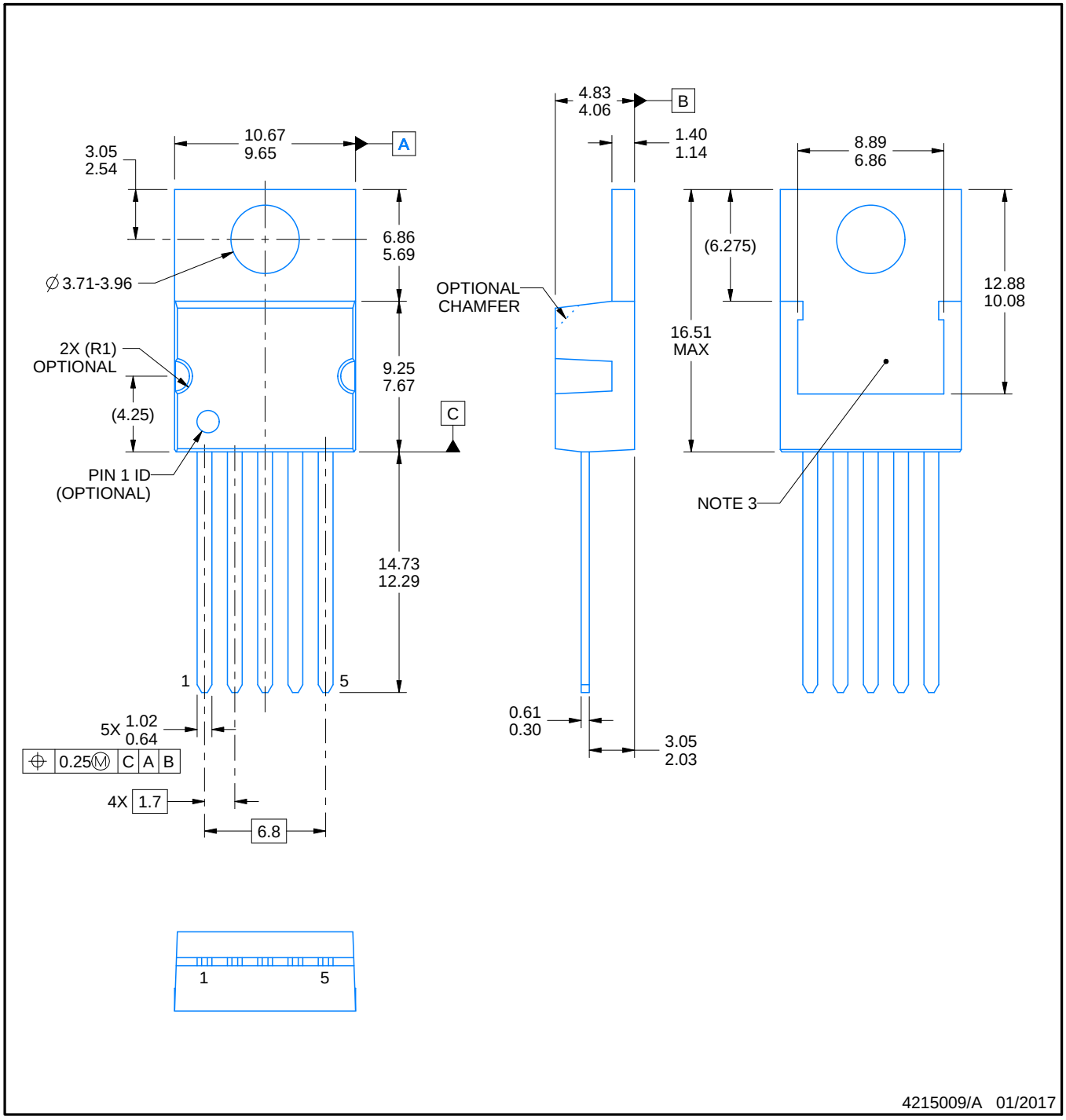
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# KC0005A

# PACKAGE OUTLINE

## TO-220 - 16.51 mm max height

TO-220




NOTES:

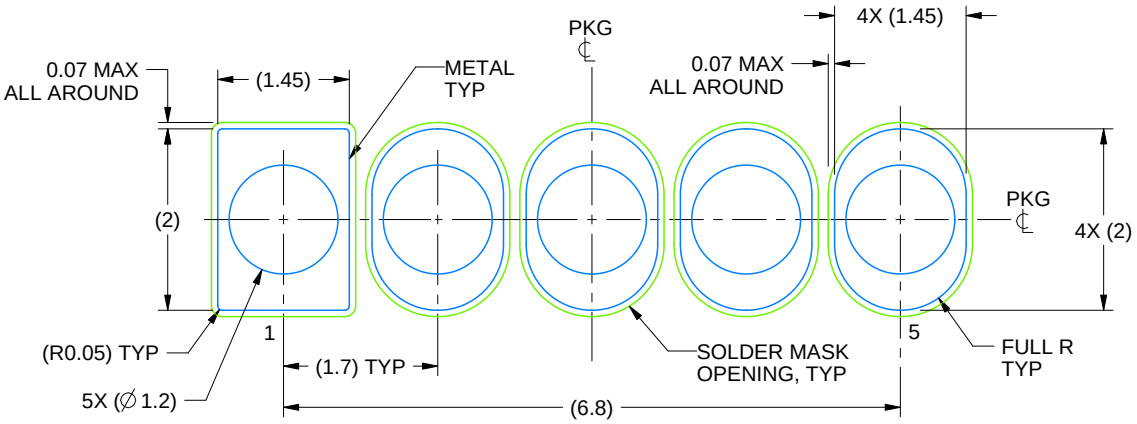
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Shape may vary per different assembly sites.

# EXAMPLE BOARD LAYOUT

## KC0005A

## TO-220 - 16.51 mm max height

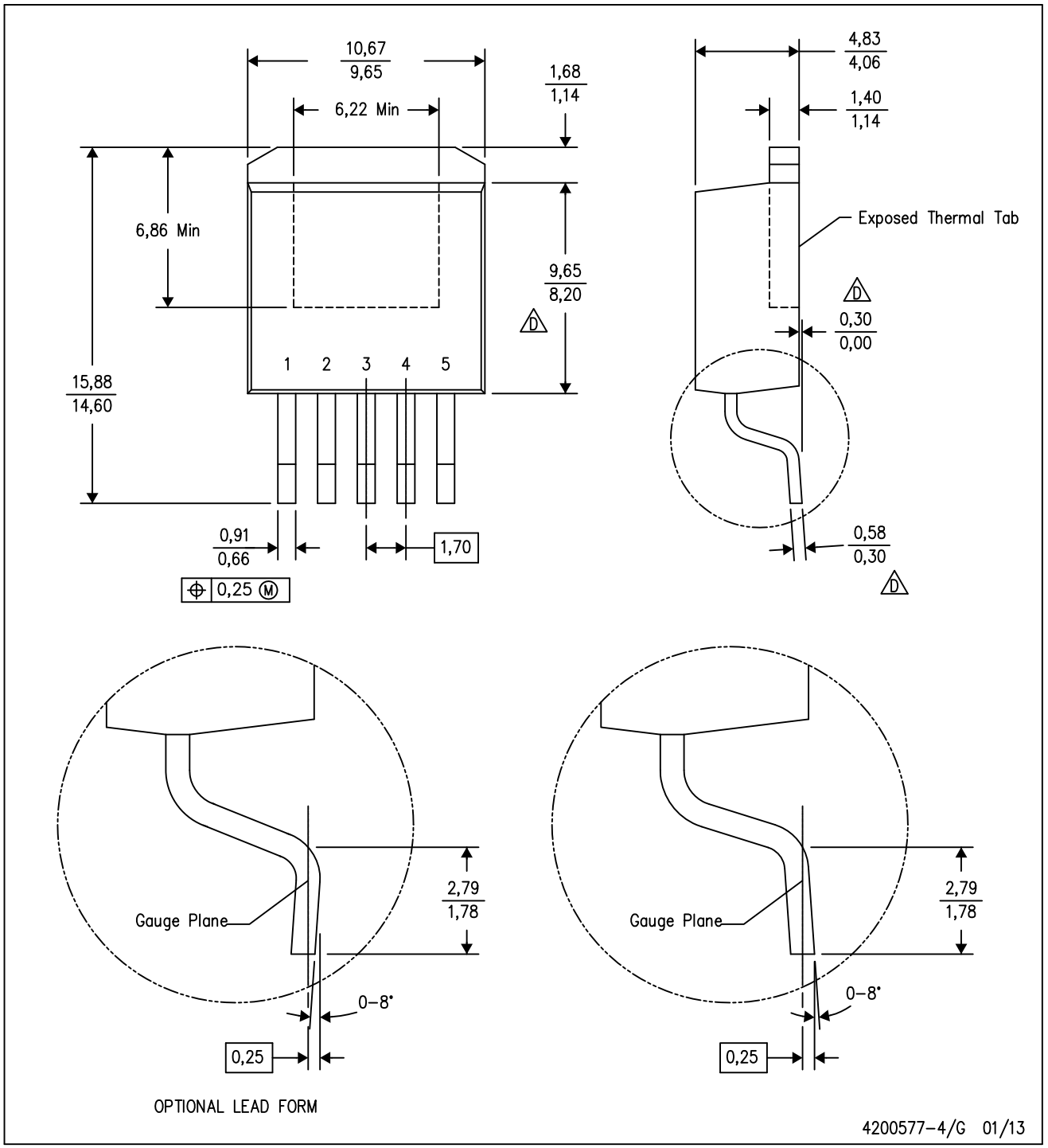
TO-220




LAND PATTERN
NON-SOLDER MASK DEFINED
SCALE:12X

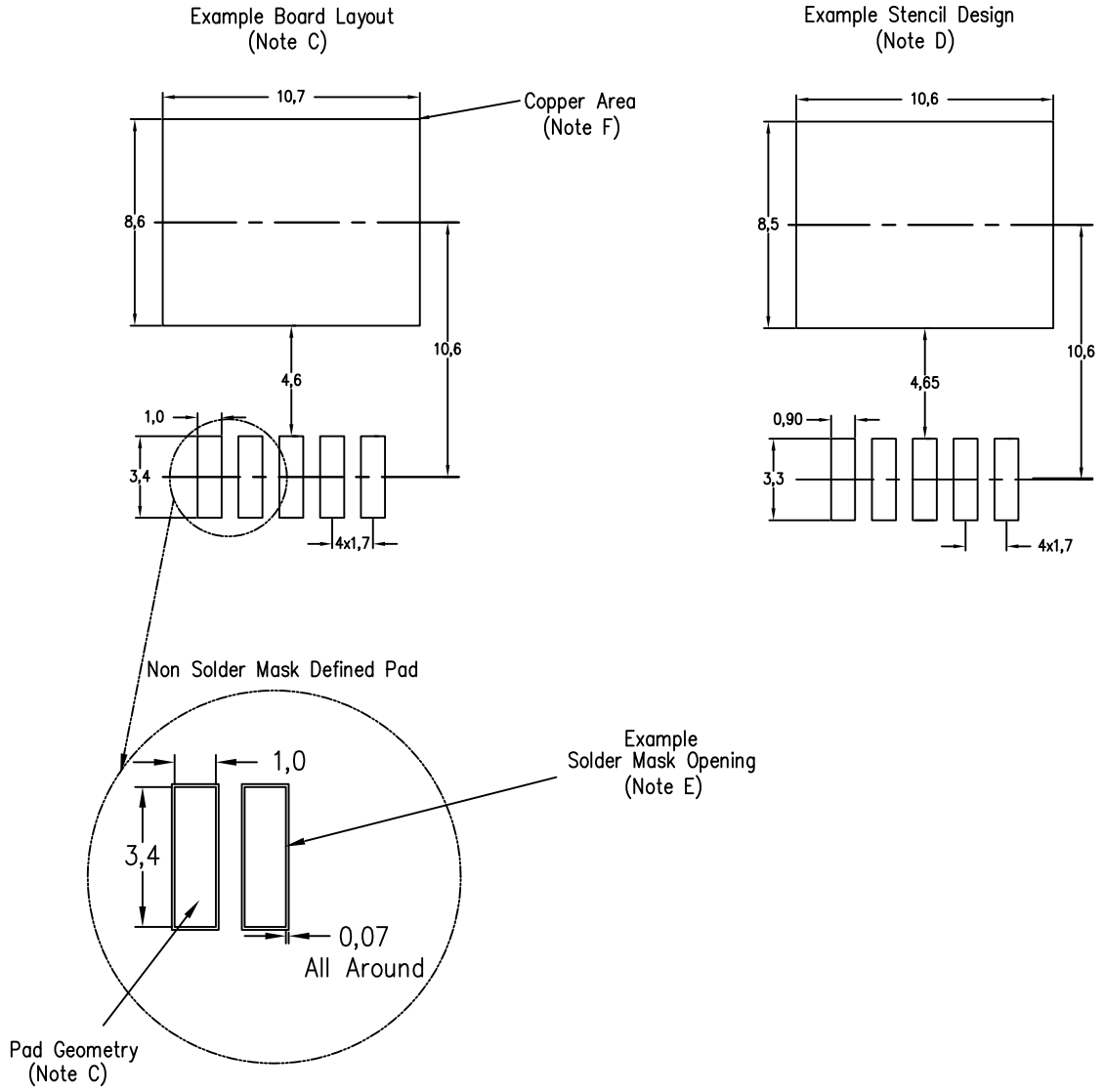
4215009/A 01/2017

KTT (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
D. Falls within JEDEC TO–263 variation BA, except minimum lead thickness, maximum seating height, and minimum body length.

KTT (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
F. This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.

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Last updated 10/2025