CC2755x10 SimpleLink Family of 2.4GHz High Performance Wireless MCUs

1 Features

Wireless MCU processing elements

- Arm® Cortex®-M33 processor (96MHz) with FPU (floating point unit), TrustZone®-M support, and CDE (custom datapath extension) for machine learning acceleration
- Algorithm Processing Unit (APU) (96MHz)
  - Mathematical accelerator for efficient vector and matrix operations
  - Bluetooth® Channel Sounding post-processing support for IFFT and advanced super-resolution algorithms such as MUltiple SIgnal Classification (MUSIC)

Wireless MCU memory

- Up to 1MB of in-system programmable flash
- Up to 162KB of SRAM
- 32KB of System ROM with secure boot root of trust (RoT) and a serial (SPI/UART) bootloader
- Serial wire debug (SWD)

MCU peripherals

- 23 GPIOs, digital peripherals can be routed to multiple GPIOs:
  - Two SWD IO pads, multiplexed with GPIOs
  - Two LFXT IO pads, multiplexed with GPIOs
  - 19 DIOs (analog or digital IOs)
- All GPIOs with wakeup and interrupt capabilities
- 3 × 16-bit and 1 × 32-bit general-purpose timers, quadrature decode mode support
- Real-time clock (RTC)
- Watchdog timer
- System timer for radio, RTOS, and application operations for Bluetooth® channel sounding postprocessing
- 12-bit ADC, up to 1.2MSPS, eight external inputs
- Temperature sensor and battery monitor
- 1× low-power comparator
- 2× UART with LIN capability
- 2× SPI
- 1× I^2C
- 1× I^2S

Security enablers

- Hardware Security Module (HSM) with proprietary controller and dedicated memories supporting accelerated cryptographic operations and secure key storage:
  - AES (up to 256 bits) crypto accelerator
  - ECC (up to 521 bits), RSA (up to 3072 bits) public key accelerator
  - SHA-2 (up to 512 bits) accelerator
  - True random number generator
  - HSM firmware update support
  - Differential power analysis (DPA) countermeasures for AES and ECC
- Separate AES 128-bit cryptographic accelerator (LAES) for latency-critical link-layer operations
- Secure boot and secure firmware updates
- Secure boot root of trust (RoT)
- Cortex®-M33 TrustZone-M, MPU, memory firewalls for software isolation
- Voltage glitch monitor (VGM)

Low-power consumption (VDDS at 3.3V)

- On-chip buck DC/DC converter
- RX current: 6.1mA
- TX current at 0dBm: 7.7mA
- TX current at +10dBm: 24.5mA (R variant)
- TX current at +20dBm: 143mA (P variant)
- Active mode MCU 96MHz (CoreMark®): 6.8mA
- Standby: 0.9µA (low power mode, RTC on, full SRAM retention)
- Shutdown: 160nA

Wireless protocol support

- Bluetooth® Core 6.0 Qualified
  - Support for Bluetooth® Channel Sounding (High Accuracy Distance Measurement)
- Matter
- Zigbee® 3.0 Certified
- Thread
- Proprietary systems
- Multi-protocol

High-performance radio

- 2.4GHz RF transceiver compatible with Bluetooth® Low Energy specification and IEEE 802.15.4 specification
- Output power up to +10dBm (R variant)
- Output power up to +20dBm (P variant)
- Integrated BALUN
- Integrated RF switch
- Receiver sensitivity:
  - Bluetooth® LE 125kbps: –103.5dBm
  - Bluetooth® LE 1Mbps: –97dBm
  - IEEE 802.15.4 (2.4GHz): –103dBm

Regulatory compliance

- Designed for systems targeting compliance with worldwide radio frequency regulations
  - EN 300 328 (Europe)
  - FCC CFR47 Part 15 (US)
  - ARIB STD-T66 (Japan)

Development tools and software

- LP-EM-CC2745R10-Q1 LaunchPad™ Development Kit
- SimpleLink™ Low Power F3 Software Development Kit (SDK)
  - Fully qualified Bluetooth® software protocol stack in the SDK
    - Up to 32 concurrent multirole connections
    - Bluetooth® Low Energy 6.0 Support
- Automotive SPICE (ASPICE) compliance for SDK components, including the Bluetooth® LE stack
- SysConfig system configuration tool
- SmartRF™ Studio for simple radio configuration

Operating ranges

- Junction temperature T_J: –40°C to 125°C
- Wide supply voltage range 1.71V to 3.8V

Package

- 6mm × 6mm QFN40 with wettable flanks
- 3.5mm × 3.4mm WCSP (Preview)

2 Applications

- Medical
  - Home healthcare – blood glucose monitors, blood pressure monitor, CPAP machine, electronic thermometer
  - Patient monitoring and diagnostics – medical sensor patches
  - Personal care and fitness – electric toothbrush, wearable fitness & activity monitor
- Building automation
  - Building security systems – motion detector, electronic smart lock, door and window sensor, garage door system, gateway
  - HVAC – thermostat, wireless environmental sensor
  - Fire safety system – smoke and heat detector
  - Video surveillance – IP network camera
- Lighting
  - LED luminaire
  - Lighting control – daylight sensor, lighting sensor, wireless control
- Factory automation and control
- Retail automation & payment – electronic point of sale
  - Electronic shelf label
- Grid infrastructure
  - Smart meters – water meter, gas meter, electricity meter, and heat cost allocators
  - Grid communications – wireless communications – Long-range sensor applications
  - Other alternative energy – energy harvesting
- Communication equipment
  - Wired networking
  - wireless LAN or Wi-Fi access points, edge router, Core Router, Small Business Switch
- Personal electronics
  - Connected peripherals – consumer wireless module, pointing devices, keyboards, and keypads
  - Gaming – electronic and robotic toys
  - Wearables (non-medical) – smart trackers, smart clothing

3 Description

The SimpleLink™ CC2755R and CC2755P family of devices are 2.4GHz wireless microcontrollers (MCUs), targeting Bluetooth® Low Energy (6.x and the upcoming versions), Zigbee (3.0 and the upcoming versions), Thread (1.3 and the upcoming versions), Matter (1.2 and the upcoming versions), and Proprietary 2.4GHz applications. These devices are optimized for low-power wireless communication with Over the Air Download (OAD) support in building automation (wireless sensors, lighting control, beacons), appliances, asset tracking, medical, and personal electronics (toys, HID, stylus pens) markets. Highlighted features of this device include:

- Support for features in Bluetooth® 6.0 and earlier versions:
  - LE Coded PHYs (Long Range), LE 2Mbit PHY (high speed), advertising extensions, multiple advertisement sets, CSA#2, as well as backward compatibility with earlier Bluetooth® Low Energy specifications
- Bluetooth® Channel Sounding technology support and an Algorithm Processing Unit (APU) to enable high accuracy, low cost, and a secure phase-based ranging mechanism for distance estimation

  - APU enables latency and power-efficient execution of distance-ranging signal processing algorithms, including FFT, super-resolution complex algorithms like MUltiple SIgnal Classification (MUSIC), and neural network algorithms.
- Arm®Custom Data Extension (CDE) instruction support for machine learning acceleration
- Fully qualified Bluetooth® software protocol stack included with the SimpleLink™ Low Power F3 Software Development Kit (SDK)
- Zigbee® protocol stack support in the SimpleLink™ Low Power F3 Software Development Kit (SDK)
- Thread protocol stack support in SIMPLELINK TI OPENTHREAD SDK
- Matter stack support in SIMPLELINK MATTER SDK
- Advanced security features for connected wireless MCUs:
  - An isolated HSM environment with a dedicated controller handling accelerated cryptographic and random number generation operations
  - Secure boot and firmware updates with the root of trust enabled by an immutable system ROM
  - Arm® Cortex M33 TrustZone-M based trusted execution environment support
  - Secure key storage support with HSM and TrustZone-M
  - Hardware fault sensors to mitigate low-cost, low-effort, non-invasive physical attack threats like voltage glitch injection
  - Dedicated AES-128 HW accelerator for handling timing-critical link-layer encryption/decryption operations
- Ultra-low standby current with full 162KB SRAM retention and RTC operation that enables significant battery life extension, especially for applications with longer sleep intervals
- Extended temperature support with the lowest standby current
- Integrated BALUN and integrated RF switch to support both transmit and receive operations on the same RF pin, even in the P version; thereby, enabling a reduced bill-of-material (BOM) board layout
- Excellent radio sensitivity and robustness (selectivity and blocking) performance for Bluetooth® Low Energy

The CC2755R and CC2755P devices are part of the SimpleLink™ MCU platform, which consists of Wi-Fi®, Bluetooth® Low Energy, Thread, Zigbee, Sub1GHz MCUs, and host MCUs that all share a common, easy-to-use development environment with a single core software development kit (SDK) and a rich toolset. A one-time integration of the SimpleLink™ platform enables you to add any combination of the portfolio's devices into your design, allowing 100 percent code reuse when your design requirements change. For more information, visit SimpleLink™ MCU platform.

Device Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
CC2755R105E0WRHAR	QFN40	6.0mm × 6.0mm
CC2755R105E0YCJR(3)	WCSP	3.5mm × 3.4mm
CC2755P105E0WRHAR	QFN40	6.0mm × 6.0mm

(1) For more information, see the *Mechanical, Packaging, and Orderable* addendum.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) PRODUCT PREVIEW only

4 Functional Block Diagram

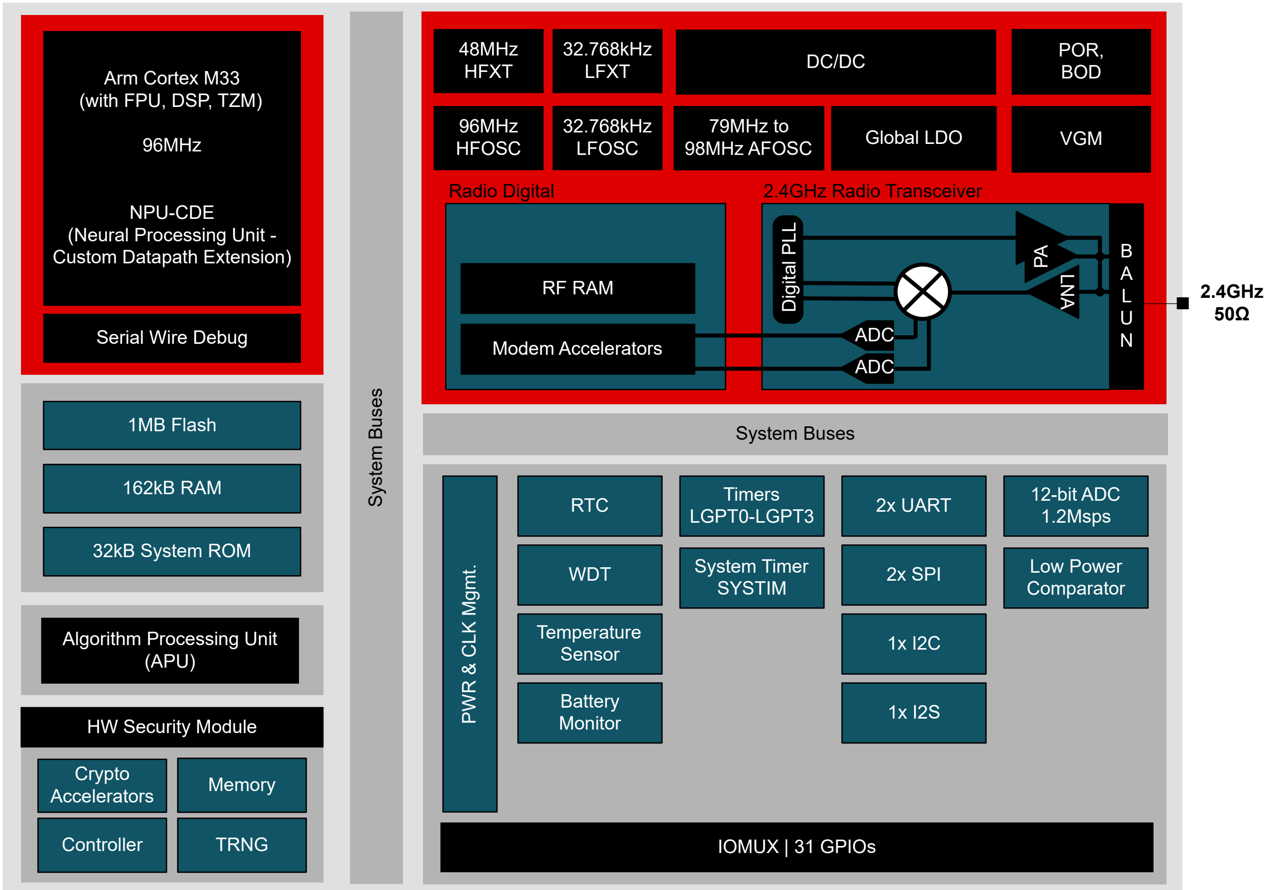

Figure 4-1. Functional Block Diagram

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5 Device Comparison

IP	CC2755P10	CC2755R10	CC2755R10 WCSP
CM33 (MCU)	✓	✓	✓
CDE (Custom Datapath Extension) (Machine Learning Acceleration)	✓	✓	✓
APU (Algorithm Processing Unit) (Bluetooth Channel Sounding Post-processing)	✓	✓	✓
HSM	✓	✓	✓
VGM	✓	✓	✓
2x UART, 2x SPI, 1x I2C, 1x I2S	✓	✓	✓
+10dBm PA	✓	✓	✓
+20dBm PA	✓		
ADC12	✓	✓	✓
Flash (KB)	1024(1)	1024(1)	1024(1)
SRAM (KB)	162	162	162
GPIO	23	23	31
QFN Package Size (mm×mm)	6 × 6	6 × 6	Not Available
WCSP Package Size (mm×mm)	Not Available	Not Available	3.5×3.4

(1) 96KB of the device flash memory is reserved for the HSM firmware.

6 Pin Configuration and Functions

6.1 Pin Diagrams

6.1.1 Pin Diagram—RHA package

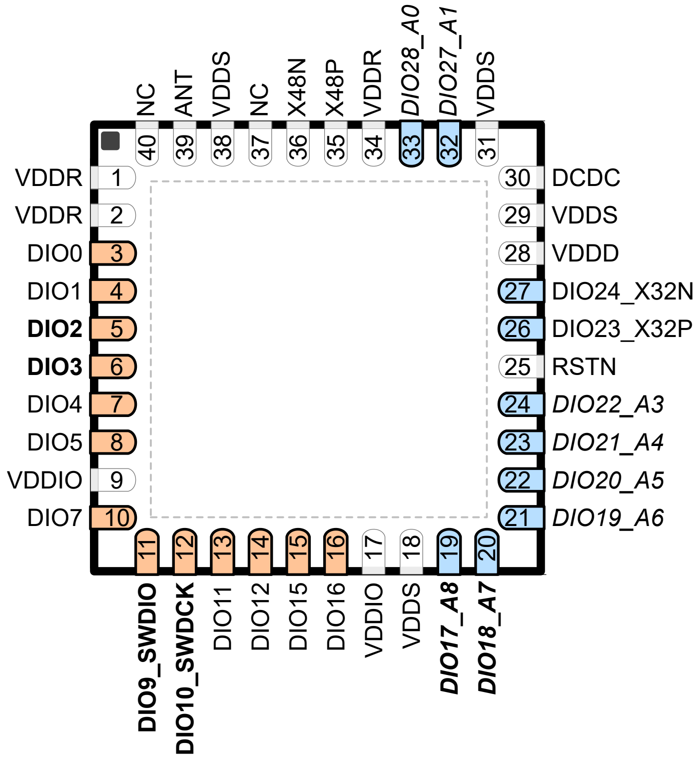

Figure 6-1. RHA (6mm × 6mm) Pinout, 0.5mm Pitch (Top View)

The following I/O pins marked in Figure 6-1 in **bold** have high-drive capabilities:

- Pin 5, DIO2
- Pin 6, DIO3
- Pin 11, DIO9_SWDIO
- Pin 12, DIO10_SWDCK
- Pin 19, DIO17_A8
- Pin 20, DIO18_A7

The following I/O pins marked in Figure 6-1 in *italics* have analog capabilities:

- Pin 19, DIO17_A8
- Pin 20, DIO18_A7
- Pin 21, DIO19_A6
- Pin 22, DIO20_A5
- Pin 23, DIO21_A4
- Pin 24, DIO22_A3
- Pin 32, DIO27_A1
- Pin 33, DIO28_A0

The following I/O pins marked in Figure 6-1 in *orange color* are supplied by VDDIO:

- Pin 3, DIO0
- Pin 4, DIO1
- Pin 5, DIO2
- Pin 6, DIO3
- Pin 7, DIO4
- Pin 8, DIO5
- Pin 10, DIO7
- Pin 11, DIO9_SWDIO
- Pin 12, DIO10_SWDCK
- Pin 13, DIO11
- Pin 14, DIO12
- Pin 15, DIO15
- Pin 16, DIO16

The following I/O pins marked in Figure 6-1 in *blue color* are supplied by VDDS:

- Pin 19, DIO17_A8
- Pin 20, DIO18_A7
- Pin 21, DIO19_A6
- Pin 22, DIO20_A5
- Pin 23, DIO21_A4
- Pin 24, DIO22_A3
- Pin 26, DIO23_X32P
- Pin 27, DIO24_X32N
- Pin 32, DIO27_A1
- Pin 33, DIO28_A0

6.1.2 Pin Diagram—YCJ package

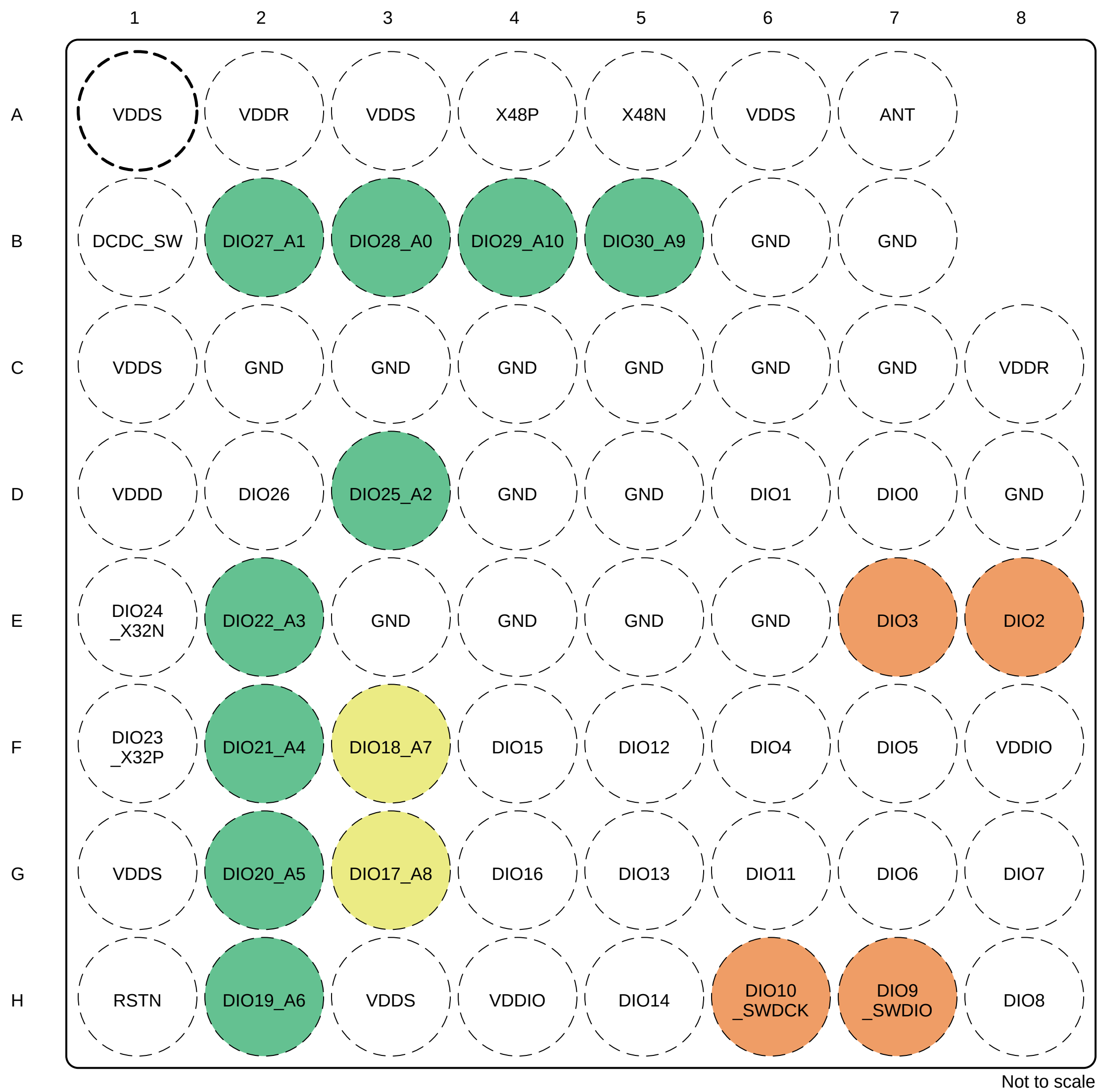

Figure 6-2. YCJ WCSP Pinout Preview (Top View)

Table 6-1. Legend

Legend
High Drive Capable
Analog Capable
Analog and High Drive Capable

The following I/O pins have high-drive capabilities:

- E8, DIO2
- E7, DIO3
- H7, DIO9_SWDIO
- H6, DIO10_SWDCK
- G3, DIO17_A8
- F3, DIO18_A7

The following I/O pins have analog capabilities:

- G3, DIO17_A8
- F3, DIO18_A7
- H2, DIO19_A6
- G2, DIO20_A5
- F2, DIO21_A4
- E2, DIO22_A3
- D3, DIO25_A2
- B2, DIO27_A1
- B3, DIO28_A0
- B4, DIO29_A10
- B5, DIO30_A9

Table 6-2. DIO Voltage Domains

VDDS	VDDIO
DIO17_A8	DIO0
DIO18_A7	DIO1
DIO19_A6	DIO2
DIO20_A5	DIO3
DIO21_A4	DIO4
DIO22_A3	DIO5
DIO23_X32P	DIO6
DIO24_X32N	DIO7
DIO25_A2	DIO8
DIO26	DIO9_SWDIO
DIO27_A1	DIO10_SWDCK
DIO28_A0	DIO11
DIO29_A10	DIO12
DIO30_A9	DIO13
	DIO14
	DIO15
	DIO16

6.2 Signal Descriptions

6.2.1 Signal Descriptions—RHA Package

Table 6-3. Signal Descriptions—RHA Package

PIN		I/O	TYPE	DESCRIPTION
NAME	NO.			
VDDR	1	—	Power	Internal supply, must be powered from the internal DC/DC converter or the GLDO(1) (2) (3)
VDDR	2	—	Power	Internal supply, must be powered from the internal DC/DC converter or the internal LDO(1) (2) (3)
DIO0	3	I/O	Digital	GPIO
DIO1	4	I/O	Digital	GPIO
DIO2	5	I/O	Digital	GPIO, high-drive capability
DIO3	6	I/O	Digital	GPIO, high-drive capability
DIO4	7	I/O	Digital	GPIO
DIO5	8	I/O	Digital	GPIO

Table 6-3. Signal Descriptions—RHA Package (continued)

PIN		I/O	TYPE	DESCRIPTION
NAME	NO.			
VDDIO	9	—	Power	1.71V to 3.8V split rail I/O supply(4)
DIO7	10	I/O	Digital	GPIO
DIO9_SWDIO	11	I/O	Digital	GPIO, SWD interface: mode select or SWDIO, high-drive capability
DIO10_SWDCK	12	I/O	Digital	GPIO, SWD interface: serial wire clock, high-drive capability
DIO11	13	I/O	Digital	GPIO
DIO12	14	I/O	Digital	GPIO
DIO15	15	I/O	Digital	GPIO
DIO16	16	I/O	Digital	GPIO
VDDIO	17	—	Power	1.71V to 3.8V split rail I/O supply(4)
VDDS	18	—	Power	1.71V to 3.8V supply(4)
DIO17_A8	19	I/O	Digital or Analog	GPIO, analog capability, high-drive capability
DIO18_A7	20	I/O	Digital or Analog	GPIO, analog capability, high-drive capability
DIO19_A6	21	I/O	Digital or Analog	GPIO, analog capability
DIO20_A5	22	I/O	Digital or Analog	GPIO, analog capability
DIO21_A4	23	I/O	Digital or Analog	GPIO, analog capability
DIO22_A3	24	I/O	Digital or Analog	GPIO, analog capability
RSTN	25	I	Digital	Reset, active low. No internal pullup resistor
DIO23_X32P	26	I/O	Digital or Analog	GPIO, 32kHz crystal oscillator pin 1, optional TCXO input
DIO24_X32N	27	I/O	Digital or Analog	GPIO, 32kHz crystal oscillator pin 2
VDDD	28	—	Power	Internal 1.32V regulated core-supply. Connect an external 1µF decoupling capacitor.(1)
VDDS	29	—	Power	1.71V to 3.8V supply (4)
DCDC	30	—	Power	Switching node of internal DC/DC converter(4)
VDDS	31	—	Power	1.71V to 3.8V supply. Connect an external 10µF decoupling capacitor.(4)
DIO27_A1	32	I/O	Digital or Analog	GPIO, analog capability
DIO28_A0	33	I/O	Digital or Analog	GPIO, analog capability
VDDR	34	—	Power	Internal supply, must be powered from the internal DC/DC converter or the internal LDO. Connect an external 10µF decoupling capacitor.(1) (2) (3)
X48P	35	—	Analog	48MHz crystal oscillator pin 1
X48N	36	—	Analog	48MHz crystal oscillator pin 2
NC	37	—	—	No Connect
VDDS	38	—	Power	1.71V to 3.8V supply(4)
ANT	39	—	RF	2.4GHz TX, RX
NC	40	—	—	No Connect(6)
EGP	—	—	GND	Ground – exposed ground pad(5)

(1) Do not supply external circuitry from this pin.
(2) VDDR pins 1, 2, and 34 must be tied together on the PCB.
(3) Output from internal DC/DC and LDO is trimmed to 1.5V.
(4) For more details, see the technical reference manual listed in Documentation Support.
(5) EGP is the only ground connection for the device. A good electrical connection to the device ground on the printed circuit board (PCB) is imperative for proper device operation.
(6) This pin is not connected to the die. In the LP-EM-CC2745R10-Q1 reference design, this pin is connected to ground to give better shielding on the antenna path.

6.2.2 Signal Descriptions—YCJ Package

Table 6-4. Signal Descriptions—YCJ Package Preview

PIN		I/O	TYPE	DESCRIPTION
NAME	NO.			
VDDR	C8	—	Power	Internal supply, must be powered from the internal DC/DC converter or the internal LDO(1) (2) (3)
VDDR	A2	—	Power	Internal supply, must be powered from the internal DC/DC converter or the internal LDO(1) (2) (3)
DIO0	D7	I/O	Digital	GPIO
DIO1	D6	I/O	Digital	GPIO
DIO2	E8	I/O	Digital	GPIO, high-drive capability
DIO3	E7	I/O	Digital	GPIO, high-drive capability
DIO4	F6	I/O	Digital	GPIO
DIO5	F7	I/O	Digital	GPIO
DIO6	G7	I/O	Digital	GPIO
VDDIO	F8	—	Power	1.71V to 3.63V split rail I/O supply
DIO7	G8	I/O	Digital	GPIO
DIO8	H8	I/O	Digital	GPIO
DIO9_SWDIO	H7	I/O	Digital	GPIO, SWD interface: mode select or SWDIO, high-drive capability
DIO10_SWDCK	H6	I/O	Digital	GPIO, SWD interface: clock, high-drive capability
DIO11	G6	I/O	Digital	GPIO, high-drive capability
DIO12	F5	I/O	Digital	GPIO, high-drive capability
DIO13	G5	I/O	Digital	GPIO
DIO14	H5	I/O	Digital	GPIO
DIO15	F4	I/O	Digital	GPIO
DIO16	G4	I/O	Digital	GPIO
VDDIO	H4	—	Power	1.71V to 3.63V split rail I/O supply
VDDS	H3	—	Power	1.71V to 3.63V supply
VDDS	G1	—	Power	1.71V to 3.63V supply
DIO17_A8	G3	I/O	Digital or Analog	GPIO, analog capability, high-drive capability
DIO18_A7	F3	I/O	Digital or Analog	GPIO, analog capability, high-drive capability
DIO19_A6	H2	I/O	Digital or Analog	GPIO, analog capability
DIO20_A5	G2	I/O	Digital or Analog	GPIO, analog capability
DIO21_A4	F2	I/O	Digital or Analog	GPIO, analog capability
DIO22_A3	E2	I/O	Digital or Analog	GPIO, analog capability
RSTN	H1	I	Digital	Reset, active low. No internal pullup resistor
DIO23_X32P	F1	I/O	Digital or Analog	GPIO, 32kHz crystal oscillator pin 1, Optional TCXO input
DIO24_X32N	E1	I/O	Digital or Analog	GPIO, 32kHz crystal oscillator pin 2
DIO25_A2	D3	I/O	Digital	GPIO
DIO26	D2	I/O	Digital	GPIO
DIO29_A10	B4	I/O	Digital	GPIO
DIO30_A9	B5	I/O	Digital	GPIO
VDDD	D1	—	Power	For decoupling of internal 1.28V regulated core-supply. Connect an external 1µF decoupling capacitor.(1)
VDDS	C1	—	Power	1.71V to 3.63V supply. Connect an external 10µF decoupling capacitor.
DCDC_SW	B1	—	Power	Switching node of internal DC/DC converter
VDDS	A1	—	Power	1.71V to 3.63V supply

Table 6-4. Signal Descriptions—YCJ Package Preview (continued)

PIN		I/O	TYPE	DESCRIPTION
NAME	NO.			
VDDS	A3	—	Power	1.71V to 3.63V supply
DIO27_A1	B2	I/O	Digital or Analog	GPIO, analog capability
DIO28_A0	B3	I/O	Digital or Analog	GPIO, analog capability
VDDR	A2	—	Power	Internal supply, must be powered from the internal DC/DC converter or the internal LDO. Connect an external 10µF decoupling capacitor.(1) (2) (3)
X48P	A4	—	Analog	48MHz crystal oscillator pin 1
X48N	A5	—	Analog	48MHz crystal oscillator pin 2
VDDS	A6	—	Power	1.71V to 3.63V supply
ANT	A7	I/O	RF	2.4GHz TX, RX
GND	E3	—	GND	Ground
GND	E4	—	GND	Ground
GND	E5	—	GND	Ground
GND	E6	—	GND	Ground
GND	D4	—	GND	Ground
GND	D5	—	GND	Ground
GND	D8	—	GND	Ground
GND	C2	—	GND	Ground
GND	C3	—	GND	Ground
GND	C4	—	GND	Ground
GND	C5	—	GND	Ground
GND	C6	—	GND	Ground
GND	C7	—	GND	Ground
GND	B6	—	GND	Ground
GND	B7	—	GND	Ground

(1) VDDR pins must be tied together on the PCB.
(2) Output from internal DC/DC and LDO is trimmed to 1.5V.
(3) For more details, see the technical reference manual listed in *Documentation Support*.

6.3 Connections for Unused Pins and Modules

6.3.1 Connections for Unused Pins and Modules—RHA Package

Table 6-5. Connections for Unused Pins—RHA Package

FUNCTION	SIGNAL NAME	PIN NUMBER	ACCEPTABLE PRACTICE(1)	PREFERRED PRACTICE(1)
GPIO (digital)	DIOn	3–8 10 13–16	NC, GND, or VDDS	NC
SWD	DIO9_SWDIO	11	NC, GND, or VDDS	NC(3)
	DIO10_SWDCK	12	NC, GND, or VDDS	NC(4)
GPIO (digital or analog)	DIOn_Am	19–24 32–33	NC, GND, or VDDS	NC
32.768kHz crystal	DIO23_X32P	26	NC or GND	NC
	DIO24_X32N	27		
DC/DC converter(2)	DCDC	30	NC	NC
	VDDS	18, 29, 31, 38	VDDS	VDDS

Table 6-5. Connections for Unused Pins—RHA Package (continued)

FUNCTION	SIGNAL NAME	PIN NUMBER	ACCEPTABLE PRACTICE(1)	PREFERRED PRACTICE(1)
Split Rail I/O supply	VDDIO	9, 17	VDDS	VDDS

(1) NC = No connect
(2) When the DC/DC converter is not used, the inductor between DCDC and VDDR can be removed. VDDR must still be connected, and the 10µF decoupling capacitor must be kept on the VDDR net.
(3) By default, an internal pullup is enabled on SWDIO.
(4) By default, an internal pulldown is enabled on SWDCK.

6.3.2 Connections for Unused Pins and Modules—YCJ Package

Table 6-6. Connections for Unused Pins—RKP Package

FUNCTION	SIGNAL NAME	PIN NUMBER	ACCEPTABLE PRACTICE(1)	PREFERRED PRACTICE(1)
GPIO (digital)	DIOn	D7, D6, E8, E7,F6,F7,G8,H7,H6, G6,F5,F4,G4,G7,H8, G5,H5,D2	NC, GND, or VDDS	NC
SWD	DIO9_SWDIO	H7	NC, GND, or VDDS	GND or VDDS
	DIO10_SWDCK	H6	NC, GND, or VDDS	GND or VDDS
GPIO (digital or analog)	DIOn_Am	G3,F3,H2,G2,F2,E2,B2,B3,D3,B4,B5	NC, GND, or VDDS	NC
32.768-kHz crystal	DIO23_X32P	F1	NC or GND	NC
	DIO24_X32N	E1		
DC/DC converter(2)	DCDC_SW	B1	NC	NC
	VDDS	H3,G1,C1,A1,A3,A6	VDDS	VDDS
Split Rail I/O supply	VDDIO	F8,H4	VDDS	VDDS

(1) NC = No connect
(2) When the DC/DC converter is not used, the inductor between DCDC and VDDR can be removed. VDDR must still be connected, and the 10µF DCDC capacitor must be kept on the VDDR net.

6.4 Peripheral Pin Mapping

6.4.1 RHA Peripheral Pin Mapping

Table 6-7. RHA (QFN40) Peripheral Pin Mapping

PIN NO. QFN40	PIN NAME	SIGNAL NAME	SIGNAL TYPE(1)	PIN MUX ENCODING	SIGNAL DIRECTION
1	VDDR	VDDR	—	N/A	N/A
2	VDDR	VDDR	—	N/A	N/A
3	DIO0	GPIO0	I/O	0	I/O
		T0C0		1	I/O
		T1F		2	O
		T3C0N		3	O
		LPCO		4	O
		T1C0		5	I/O
4	DIO1	GPIO1	I/O	0	I/O
		T1C0		2	I/O
		T2C0		3	I/O
		UART0TXD		4	O
		T1C1		5	I/O
		DTB15		7	O

Table 6-7. RHA (QFN40) Peripheral Pin Mapping (continued)

PIN NO. QFN40	PIN NAME	SIGNAL NAME	SIGNAL TYPE[(1)]	PIN MUX ENCODING	SIGNAL DIRECTION
5	DIO2	GPIO2	I/O	0	I/O
		T1C1		2	I/O
		T0PE		3	O
		UART0RXD		4	I
		T1C2		5	I/O
		DTB14		7	O
6	DIO3	GPIO3	I/O	0	I/O
		SPI0SCLK		1	I/O
		I2S0SCLK		2	I/O
		T2PE		3	O
		UART1TXD		4	O
		T2C0		5	I/O
		DTB13		7	O
7	DIO4	GPIO4	I/O	0	I/O
		SPI0PICO		1	I/O
		SPI0POCI		2	I/O
		T1C2		3	I/O
		UART1RXD		4	I
		T2C1		5	I/O
		DTB12		7	O
8	DIO5	GPIO5	I/O	0	I/O
		SPI0POCI		1	I/O
		SPI0PICO		2	I/O
		T2C1		3	I/O
		T3C1N		4	O
		T2C2		5	I/O
		DTB11		7	O
9	VDDIO	VDDIO	—	N/A	N/A
10	DIO7	GPIO7	I/O	0	I/O
		SPI0CSN		1	I/O
		T2C2		2	I/O
		I2S0WS		3	I/O
		T3C2N		4	O
		DTB10		7	O
11	DIO9_SWDIO	GPIO9	I/O	0	I/O
		T0C1		1	I/O
		T2C0N		2	O
		I2S0SD0		3	I/O
		T0PE		4	O
		I2C0SCL		5	I/O

Table 6-7. RHA (QFN40) Peripheral Pin Mapping (continued)

PIN NO. QFN40	PIN NAME	SIGNAL NAME	SIGNAL TYPE[(1)]	PIN MUX ENCODING	SIGNAL DIRECTION
12	DIO10_SWDCK	GPIO10	I/O	0	I/O
		T0C2		1	I/O
		T2C1N		2	O
		I2S0SD1		3	I/O
		T2PE		4	O
		I2C0SDA		5	I/O
13	DIO11	GPIO11	I/O	0	I/O
		SPI1POCI		1	I/O
		SPI1PICO		2	I/O
		SWO		3	O
		T3C0		4	I/O
		T1F		5	O
		DTB9		7	O
14	DIO12	GPIO12	I/O	0	I/O
		SPI1PICO		1	I/O
		SPI1POCI		2	I/O
		T2C2N		3	O
		T3C1		4	I/O
		T3C2		5	I/O
		DTB8		7	O
15	DIO15	GPIO15	I/O	0	I/O
		SPI1SCLK		1	I/O
		T3C2		2	I/O
		T1C0N		3	O
		LPCO		4	O
		T3C1		5	I/O
16	DIO16	GPIO16	I/O	0	I/O
		I2S0MCLK		1	O
		SPI1CSN		2	I/O
		EXTCI		3	I
		T1F		4	I
		T3C0		5	I/O
		DTB7		7	O
17	VDDIO	VDDIO	—	N/A	N/A
18	VDDS	VDDS	—	N/A	N/A
19	DIO17_A8	GPIO17	I/O	0	I/O
		I2S0SCLK		1	I/O
		UART0RTS		2	O
		T0C0		4	I/O
		LRFD0		5	O
		ADC8		6	I
		DTB6		7	O

Table 6-7. RHA (QFN40) Peripheral Pin Mapping (continued)

PIN NO. QFN40	PIN NAME	SIGNAL NAME	SIGNAL TYPE[(1)]	PIN MUX ENCODING	SIGNAL DIRECTION
20	DIO18_A7	GPIO18	I/O	0	I/O
		I2S0WS		1	I/O
		UART0CTS		2	I
		T0C1		4	I/O
		LRFD1		5	O
		ADC7		6	I
		DTB5		7	O
21	DIO19_A6	GPIO19	I/O	0	I/O
		SPI0CSN		1	I/O
		UART0TXD		2	O
		UART0RXD		3	I
		I2S0SD0		4	I/O
		LRFD2		5	O
		ADC6/LPC+		6	I
		DTB4		7	O
22	DIO20_A6	GPIO20	I/O	0	I/O
		SPI0SCLK		1	I/O
		UART0RXD		2	I
		UART0TXD		3	O
		I2S0SD1		4	I/O
		LRFD3		5	O
		ADC5/LPC+/LPC-		6	I
		DTB3		7	O
23	DIO21_A4	GPIO21	I/O	0	I/O
		SPI0PICO		1	I/O
		UART1TXD		2	O
		I2C0SCL		3	I/O
		T1C1N		4	O
		LRFD4		5	O
		ADC4/LPC+/LPC-		6	I
		DTB2		7	O
24	DIO22_A3	GPIO22	I/O	0	I/O
		SPI0POCI		1	I/O
		UART1RXD		2	I
		I2C0SDA		3	I/O
		T1C2N		4	O
		LRFD5		5	O
		ADC3		6	I
		DTB1		7	O
25	RTSN	RSTN	—	N/A	N/A

Table 6-7. RHA (QFN40) Peripheral Pin Mapping (continued)

PIN NO. QFN40	PIN NAME	SIGNAL NAME	SIGNAL TYPE[1]	PIN MUX ENCODING	SIGNAL DIRECTION
26	DIO23_X32P	GPIO23	I/O	0	I/O
		SPI1CSN		1	I/O
		UART1RTS		2	O
		LFCI		3	I
		T0C2		4	I/O
		T1C0		5	I/O
		LFXT_P		6	I
27	DIO24_X32N	GPIO24	I/O	0	I/O
		SPI1SCLK		1	I/O
		UART1CTS		2	I
		T0C0N		3	O
		LPCO		4	O
		T0C0		5	I/O
		LFXT_N		6	I
28	VDDD	VDDD	—	N/A	N/A
29	VDDS	VDDS	—	N/A	N/A
30	DCDC	DCDC	—	N/A	N/A
31	VDDS	VDDS	—	N/A	N/A
32	DIO27_A1	GPIO27	I/O	0	I/O
		SPI1PICO		1	I/O
		I2C0SCL		2	I/O
		CKMIN		3	I
		T0C1N		4	O
		LRFD6		5	O
		ADC1/AREF+		6	I
		DTB0		7	O
33	DIO28_A0	GPIO28	I/O	0	I/O
		SPI1POCI		1	I/O
		I2C0SDA		2	I/O
		T3C0N		3	O
		T0C2N		4	O
		LRFD7		5	O
		ADC0/AREF-		6	I
34	VDDR	VDDR	—	N/A	N/A
35	X48P	X48P	—	N/A	N/A
36	X48N	X48N	—	N/A	N/A
37	NC	NC	—	N/A	N/A
38	VDDS	VDDS	—	N/A	N/A
39	ANT	ANT	—	N/A	N/A
40	NC	NC	—	N/A	N/A
—	EGP	GND	—	N/A	N/A

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

6.4.2 YCJ Peripheral Pin Mapping

Table 6-8. YCJ (WCSP) Peripheral Pin Mapping Preview

PIN NO. WCSP	PIN NAME	SIGNAL NAME	SIGNAL TYPE[(1)]	PIN MUX ENCODING	SIGNAL DIRECTION
C8	VDDR	VDDR	—	N/A	N/A
D7	DIO0	GPIO0	I/O	0	I/O
		T0C0		1	I/O
		T1F		2	O
		T3C0N		3	O
		LPCO		4	O
		T1C0		5	I/O
D6	DIO1	GPIO1	I/O	0	I/O
		T1C0		2	I/O
		T2C0		3	I/O
		UART0TXD		4	O
		T1C1		5	I/O
		DTB15		7	O
E8	DIO2	GPIO2	I/O	0	I/O
		T1C1		2	I/O
		T0PE		3	O
		UART0RXD		4	I
		T1C2		5	I/O
		DTB14		7	O
E7	DIO3	GPIO3	I/O	0	I/O
		SPI0SCLK		1	I/O
		I2S0SCLK		2	I/O
		T2PE		3	O
		UART1TXD		4	O
		T2C0		5	I/O
		DTB13		7	O
F6	DIO4	GPIO4	I/O	0	I/O
		SPI0PICO		1	I/O
		SPI0POCI		2	I/O
		T1C2		3	I/O
		UART1RXD		4	I
		T2C1		5	I/O
		DTB12		7	O
F7	DIO5	GPIO5	I/O	0	I/O
		SPI0POCI		1	I/O
		SPI0PICO		2	I/O
		T2C1		3	I/O
		T3C1N		4	O
		T2C2		5	I/O
		DTB11		7	O

Table 6-8. YCJ (WCSP) Peripheral Pin Mapping Preview (continued)

PIN NO. WCSP	PIN NAME	SIGNAL NAME	SIGNAL TYPE[(1)]	PIN MUX ENCODING	SIGNAL DIRECTION
G7	DIO6	GPIO6	I/O	0	I/O
		I2S0MCLK		1	I/O
		T0C0N		2	I/O
		T1F		3	I
		LPC0		4	O
F8	VDDIO	VDDIO	—	N/A	N/A
G8	DIO7	GPIO7	I/O	0	I/O
		SPI0CSN		1	I/O
		T2C2		2	I/O
		I2S0WS		3	I/O
		T3C2N		4	O
		DTB10		7	O
H8	DIO8	GPIO8	I/O	0	I/O
		SPI1SCLK		1	I/O
		T3C2		2	I/O
		T1C0N		3	I
		LPC0		4	O
		T3C1		5	O
H7	DIO9_SWDIO	GPIO9	I/O	0	I/O
		T0C1		1	I/O
		T2C0N		2	O
		I2S0SD0		3	I/O
		T0PE		4	O
		I2C0SCL		5	I/O
H6	DIO10_SWDCK	GPIO10	I/O	0	I/O
		T0C2		1	I/O
		T2C1N		2	O
		I2S0SD1		3	I/O
		T2PE		4	O
		I2C0SDA		5	I/O
G6	DIO11	GPIO11	I/O	0	I/O
		SPI1POCI		1	I/O
		SPI1PICO		2	I/O
		SWO		3	O
		T3C0		4	I/O
		T1F		5	O
		DTB9		7	O
F5	DIO12	GPIO12	I/O	0	I/O
		SPI1PICO		1	I/O
		SPI1POCI		2	I/O
		T2C2N		3	O
		T3C1		4	I/O
		T3C2		5	I/O
		DTB8		7	O

Table 6-8. YCJ (WCSP) Peripheral Pin Mapping Preview (continued)

PIN NO. WCSP	PIN NAME	SIGNAL NAME	SIGNAL TYPE(1)	PIN MUX ENCODING	SIGNAL DIRECTION
G5	DIO13	GPIO13	I/O	0	I/O
		UART0TXD		2	I/O
		UART1TXD		3	I
		T0C1N		4	O
H5	DIO14	GPIO14	I/O	0	I/O
		UART0RXD		2	I/O
		UART1RXD		3	I
		T0C2N		4	O
F4	DIO15	GPIO15	I/O	0	I/O
		SPI1SCLK		1	I/O
		T3C2		2	I/O
		T1C0N		3	O
		LPCO		4	O
		T3C1		5	I/O
G4	DIO16	GPIO16	I/O	0	I/O
		I2S0MCLK		1	O
		SPI1CSN		2	I/O
		EXTCI		3	I
		T1F		4	I
		T3C0		5	I/O
		DTB7		7	O
H4	VDDIO	VDDIO	—	N/A	N/A
H3	VDDS	VDDS	—	N/A	N/A
G1	VDDS	VDDS	—	N/A	N/A
G3	DIO17_A8	GPIO17	I/O	0	I/O
		I2S0SCLK		1	I/O
		UART0RTS		2	O
		T0C0		4	I/O
		LRFD0		5	O
		ADC8		6	I
		DTB6		7	O
F3	DIO18_A7	GPIO18	I/O	0	I/O
		I2S0WS		1	I/O
		UART0CTS		2	I
		T0C1		4	I/O
		LRFD1		5	O
		ADC7		6	I
		DTB5		7	O

Table 6-8. YCJ (WCSP) Peripheral Pin Mapping Preview (continued)

PIN NO. WCSP	PIN NAME	SIGNAL NAME	SIGNAL TYPE[(1)]	PIN MUX ENCODING	SIGNAL DIRECTION
H2	DIO19_A6	GPIO19	I/O	0	I/O
		SPI0CSN		1	I/O
		UART0TXD		2	O
		UART0RXD		3	I
		I2S0SD0		4	I/O
		LRFD2		5	O
		ADC6/LPC+		6	I
		DTB4		7	O
G2	DIO20_A5	GPIO20	I/O	0	I/O
		SPI0SCLK		1	I/O
		UART0RXD		2	I
		UART0TXD		3	O
		I2S0SD1		4	I/O
		LRFD3		5	O
		ADC5/LPC+/LPC-		6	I
		DTB3		7	O
F2	DIO21_A4	GPIO21	I/O	0	I/O
		SPI0PICO		1	I/O
		UART1TXD		2	O
		I2C0SCL		3	I/O
		T1C1N		4	O
		LRFD4		5	O
		ADC4/LPC+/LPC-		6	I
		DTB2		7	O
E2	DIO22_A3	GPIO22	I/O	0	I/O
		SPI0POCI		1	I/O
		UART1RXD		2	I
		I2C0SDA		3	I/O
		T1C2N		4	O
		LRFD5		5	O
		ADC3		6	I
		DTB1		7	O
H1	RTSN	RSTN	—	N/A	N/A
F1	DIO23_X32P	GPIO23	I/O	0	I/O
		SPI1CSN		1	I/O
		UART1RTS		2	O
		LFCI		3	I
		T0C2		4	I/O
		T1C0		5	I/O
		LFXT_P		6	I

Table 6-8. YCJ (WCSP) Peripheral Pin Mapping Preview (continued)

PIN NO. WCSP	PIN NAME	SIGNAL NAME	SIGNAL TYPE(1)	PIN MUX ENCODING	SIGNAL DIRECTION
E1	DIO24_X32N	GPIO24	I/O	0	I/O
		SPI1SCLK		1	I/O
		UART1CTS		2	I
		T0C0N		3	O
		LPCO		4	O
		T0C0		5	I/O
		LFXT_N		6	I
D3	DIO25_A2	GPIO25	I/O	0	I/O
		SPI0CSN		1	I/O
		SPI1SCLK		2	I/O
		I2C0SCL		3	I
		I2S0SCLK		4	O
		T1C0N		5	O
		ADC2		6	I
D2	DIO26	GPIO26	I/O	0	I/O
		SPI0POCI		1	I/O
		SPI1PICO		2	I/O
		I2C0SDA		3	I
		I2S0WS		4	O
		T1C1N		5	O
D1	VDDD	VDDD	—	N/A	N/A
C1	VDDS	VDDS	—	N/A	N/A
B1	DCDC	DCDC	—	N/A	N/A
A1	VDDS	VDDS	—	N/A	N/A
A3	VDDS	VDDS	—	N/A	N/A
B2	DIO27_A1	GPIO27	I/O	0	I/O
		SPI1PICO		1	I/O
		I2C0SCL		2	I/O
		CKMIN		3	I
		T0C1N		4	O
		LRFD6		5	O
		ADC1/AREF+		6	I
		DTB0		7	O
B3	DIO28_A0	GPIO28	I/O	0	I/O
		SPI1POCI		1	I/O
		I2C0SDA		2	I/O
		T3C0N		3	O
		T0C2N		4	O
		LRFD7		5	O
		ADC0/AREF-		6	I

Table 6-8. YCJ (WCSP) Peripheral Pin Mapping Preview (continued)

PIN NO. WCSP	PIN NAME	SIGNAL NAME	SIGNAL TYPE(1)	PIN MUX ENCODING	SIGNAL DIRECTION
B4	DIO29_A10	GPIO29	I/O	0	I/O
		SPI0SCLK		1	I/O
		SPI1CSN		2	I/O
		I2C0SCL		3	I
		I2S0SD0		4	O
		T1C2N		5	O
		ADC10		6	I
B5	DIO30_A9	GPIO30	I/O	0	I/O
		SPI0PICO		1	I/O
		SPI1POCI		2	I/O
		I2C0SDA		3	I
		I2S0SD1		4	O
		ADC9		6	I
A2	VDDR	VDDR	—	N/A	N/A
A4	X48P	X48P	—	N/A	N/A
A5	X48N	X48N	—	N/A	N/A
A6	VDDS	VDDS	—	N/A	N/A
A7	ANT	ANT	—	N/A	N/A

6.5 Peripheral Signal Descriptions

6.5.1 RHA Peripheral Signal Descriptions

Table 6-9. RHA (QFN40) Peripheral Signal Descriptions

FUNCTION	SIGNAL NAME	PIN NO. QFN40	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
ADC	ADC0	33	I/O	I	ADC channel 0 input
	ADC1	32			ADC channel 1 input
	ADC3	24			ADC channel 3 input
	ADC4	23			ADC channel 4 input
	ADC5	22			ADC channel 5 input
	ADC6	21			ADC channel 6 input
	ADC7	20			ADC channel 7 input
	ADC8	19			ADC channel 8 input
ADC Reference	AREF+	32	I/O	I	ADC external voltage reference, positive terminal
	AREF-	33			ADC external voltage reference, negative terminal
Clock	X32P	26	I/O	I	32kHz crystal oscillator pin 1
	X32N	27	I/O	I	32kHz crystal oscillator pin 2
	X48P	35	—	I	48MHz crystal oscillator pin 1, Optional TCXO input
	X48N	36	—	I	48MHz crystal oscillator pin 2
	CKMIN	32	I/O	I	HFOSC tracking loop reference clock input
	LFCI	26	I/O	I	GPIO input for low frequency clock input (LFXT bypass clock from pin) or optional TCXO

Table 6-9. RHA (QFN40) Peripheral Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO. QFN40	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
Comparator	LPCO	3	I/O	O	Low power comparator output
		15			
		27			
	LPC+	21	I/O	I	Low power comparator positive input terminal
		22			
		23			
	LPC-	22			Lower power comparator negative input terminal
		23			
Digital Test Bus	DTB0	32	I/O	O	Digital test bus output 0
	DTB1	24			Digital test bus output 1
	DTB2	23			Digital test bus output 2
	DTB3	22			Digital test bus output 3
	DTB4	21			Digital test bus output 4
	DTB5	20			Digital test bus output 5
	DTB6	19			Digital test bus output 6
	DTB7	16			Digital test bus output 7
	DTB8	14			Digital test bus output 8
	DTB9	13			Digital test bus output 9
	DTB10	10			Digital test bus output 10
	DTB11	8			Digital test bus output 11
	DTB12	7			Digital test bus output 12
	DTB13	6			Digital test bus output 13
	DTB14	5			Digital test bus output 14
	DTB15	4			Digital test bus output 15

Table 6-9. RHA (QFN40) Peripheral Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO. QFN40	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
GPIO	GPIO0	3	I/O	I/O	General-purpose input or output
	GPIO1	4			
	GPIO2	5			
	GPIO3	6			
	GPIO4	7			
	GPIO5	8			
	GPIO7	10			
	GPIO9	11			
	GPIO10	12			
	GPIO11	13			
	GPIO12	14			
	GPIO15	15			
	GPIO16	16			
	GPIO17	19			
	GPIO18	20			
	GPIO19	21			
	GPIO20	22			
	GPIO21	23			
	GPIO22	24			
	GPIO23	26			
	GPIO24	27			
	GPIO27	32			
	GPIO28	33			
I^2C	I2C0SCL	11 23 32	I/O	I/O	I^2C clock
	I2C0SDA	12 24 33	I/O	I/O	I^2C data
I^2S	I2S0MCLK	16	I/O	O	I^2S main clock
	I2S0SCLK	6 19	I/O	I/O	I^2S serial clock
	I2S0WS	10 20	I/O	I/O	I^2S word select
	I2S0SD0	11 21	I/O	I/O	I^2S serial data 0
	I2S0SD1	12 22	I/O	I/O	I^2S serial data 1
	EXTCI	16	I/O	I	I^2S external clock

Table 6-9. RHA (QFN40) Peripheral Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO. QFN40	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
LRF Digital Output	LRFD0	19	I/O	O	LRF digital output 0
	LRFD1	20			LRF digital output 1
	LRFD2	21			LRF digital output 2
	LRFD3	22			LRF digital output 3
	LRFD4	23			LRF digital output 4
	LRFD5	24			LRF digital output 5
	LRFD6	32			LRF digital output 6
	LRFD7	33			LRF digital output 7
Power	VDDR	1 2 34	—	—	Internal supply
	VDDS	18 29 31 38	—	—	1.71V to 3.8V DIO supply
	VDDD	28	—	—	For decoupling of internal 1.32V regulated core-supply.
	VDDIO	9 17	—	—	1.71V to 3.8V split rail I/O supply
	DCDC	30	—	—	Switching node of internal DC/DC converter
Reset	RSTN	25	—	—	Global master device reset (active low)
RF	ANT	39	—	—	50-ohm RF port
SPI	SPI0SCLK	6 22	I/O	I/O	SPI0 clock
	SPI0POCI	7 8 24	I/O	I/O	SPI0 peripheral out controller in
	SPI0CSN	10 21	I/O	I/O	SPI0 chip-select
	SPI0PICO	7 8 23	I/O	I/O	SPI0 peripheral in controller out
	SPI1SCLK	15 27	I/O	I/O	SPI1 clock
	SPI1POCI	13 14 33	I/O	I/O	SPI1 peripheral out controller in
	SPI1CSN	16 26	I/O	I/O	SPI1 chip select
	SPI1PICO	13 14 32	I/O	I/O	SPI1 peripheral in controller out
SWD	SWDIO	11	I/O	I/O	Serial wire data input/output
	SWDCK	12	I/O	I	Serial wire clock input

Table 6-9. RHA (QFN40) Peripheral Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO. QFN40	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
Trace	SWO	13	I/O	O	Serial wire output
Timers - Capture/ Compare	T0C0	3	I/O	I/O	Capture input-0 / compare output-0 of Timer-0
		19			
		27			
	T0C1	11			Capture input-1 / compare output-1 of Timer-0
		20			
	T0C2	12			Capture input-2 / compare output-2 of Timer-0
		26			
	T1C0	3	I/O	I/O	Capture input-0 / compare output-0 of Timer-1
		4			
		26			
	T1C1	4			Capture input-1 / compare output-1 of Timer-1
		5			
	T1C2	5			Capture input-2 / compare output-2 of Timer-1
		7			
	T2C0	4	I/O	I/O	Capture input-0 / compare output-0 of Timer-2
		6			
	T2C1	7			Capture input-1 / compare output-1 of Timer-2
		8			
	T2C2	8			Capture input-2 / compare output-2 of Timer-2
		10			
	T3C0	13	I/O	I/O	Capture input-0 / compare output-0 of Timer-3
		16			
	T3C1	14			Capture input-1 / compare output-1 of Timer-3
		15			
	T3C2	14			Capture input-2 / compare output-2 of Timer-3
		15			
Timers - Complementary Capture/PWM	T0C0N	27	I/O	O	Complementary compare/PWM output-0 from Timer-0
	T0C1N	32			Complementary compare/PWM output-1 from Timer-0
	T0C2N	33			Complementary compare/PWM output-2 from Timer-0
	T1C0N	15	I/O	O	Complementary compare/PWM output-0 from Timer-1
	T1C1N	23			Complementary compare/PWM output-1 from Timer-1
	T1C2N	24			Complementary compare/PWM output-2 from Timer-1
	T2C0N	11	I/O	O	Complementary compare/PWM output-0 from Timer-2
	T2C1N	12			Complementary compare/PWM output-1 from Timer-2
	T2C2N	14			Complementary compare/PWM output-2 from Timer-2
	T3C0N	3	I/O	O	Complementary compare/PWM output-0 from Timer-3
		33			
	T3C1N	8			Complementary compare/PWM output-1 from Timer-3
	T3C2N	10			Complementary compare/PWM output-2 from Timer-3
Timers - Fault input	T1F	3	I/O	I	Fault input for Timer-1
		13			
		16			

Table 6-9. RHA (QFN40) Peripheral Signal Descriptions (continued)

<table>
<tr><th rowspan="2">FUNCTION</th><th rowspan="2">SIGNAL NAME</th><th>PIN NO.</th><th rowspan="2">PIN TYPE</th><th rowspan="2">SIGNAL DIRECTION</th><th rowspan="2">DESCRIPTION</th></tr>
<tr><th>QFN40</th></tr>
<tr><td rowspan="4">Timers - Prescaler Event</td><td rowspan="2">T0PE</td><td>5</td><td rowspan="2">I/O</td><td rowspan="2">O</td><td rowspan="2">Prescaler event output from Timer-0</td></tr>
<tr><td>11</td></tr>
<tr><td rowspan="2">T2PE</td><td>6</td><td rowspan="2">I/O</td><td rowspan="2">O</td><td rowspan="2">Prescaler event output from Timer-2</td></tr>
<tr><td>12</td></tr>
<tr><td rowspan="14">UART</td><td rowspan="3">UART0TXD</td><td>4</td><td rowspan="3">I/O</td><td rowspan="3">O</td><td rowspan="3">UART0 TX data</td></tr>
<tr><td>21</td></tr>
<tr><td>22</td></tr>
<tr><td rowspan="3">UART0RXD</td><td>5</td><td rowspan="3">I/O</td><td rowspan="3">I</td><td rowspan="3">UART0 RX data</td></tr>
<tr><td>21</td></tr>
<tr><td>22</td></tr>
<tr><td>UART0CTS</td><td>20</td><td>I/O</td><td>I</td><td>UART0 clear-to-send input (active low)</td></tr>
<tr><td>UART0RTS</td><td>19</td><td>I/O</td><td>O</td><td>UART0 request-to-send (active low)</td></tr>
<tr><td rowspan="2">UART1TXD</td><td>6</td><td rowspan="2">I/O</td><td rowspan="2">O</td><td rowspan="2">UART1 TX data</td></tr>
<tr><td>23</td></tr>
<tr><td rowspan="2">UART1RXD</td><td>7</td><td rowspan="2">I/O</td><td rowspan="2">I</td><td rowspan="2">UART1 RX data</td></tr>
<tr><td>24</td></tr>
<tr><td>UART1CTS</td><td>27</td><td>I/O</td><td>I</td><td>UART1 clear-to-send input (active low)</td></tr>
<tr><td>UART1RTS</td><td>26</td><td>I/O</td><td>O</td><td>UART1 request-to-send (active low)</td></tr>
</table>

6.5.2 YCJ Peripheral Signal Descriptions

Table 6-10. YCJ (WCSP) Peripheral Signal Descriptions Preview

<table>
<tr><th rowspan="2">FUNCTION</th><th rowspan="2">SIGNAL NAME</th><th>PIN NO.</th><th rowspan="2">PIN TYPE</th><th rowspan="2">SIGNAL DIRECTION</th><th rowspan="2">DESCRIPTION</th></tr>
<tr><th>WCSP</th></tr>
<tr><td rowspan="11">ADC</td><td>ADC0</td><td>B3</td><td rowspan="11">I/O</td><td rowspan="11">I</td><td>ADC channel 0 input</td></tr>
<tr><td>ADC1</td><td>B2</td><td>ADC channel 1 input</td></tr>
<tr><td>ADC2</td><td>D3</td><td>ADC channel 2 input</td></tr>
<tr><td>ADC3</td><td>E2</td><td>ADC channel 3 input</td></tr>
<tr><td>ADC4</td><td>F2</td><td>ADC channel 4 input</td></tr>
<tr><td>ADC5</td><td>G2</td><td>ADC channel 5 input</td></tr>
<tr><td>ADC6</td><td>H2</td><td>ADC channel 6 input</td></tr>
<tr><td>ADC7</td><td>F3</td><td>ADC channel 7 input</td></tr>
<tr><td>ADC8</td><td>G3</td><td>ADC channel 8 input</td></tr>
<tr><td>ADC9</td><td>B5</td><td>ADC channel 9 input</td></tr>
<tr><td>ADC10</td><td>B4</td><td>ADC channel 10 input</td></tr>
<tr><td rowspan="2">ADC Reference</td><td>AREF+</td><td>B2</td><td rowspan="2">I/O</td><td rowspan="2">I</td><td>ADC external voltage reference, positive terminal</td></tr>
<tr><td>AREF-</td><td>B3</td><td>ADC external voltage reference, negative terminal</td></tr>
<tr><td rowspan="6">Clock</td><td>X32P</td><td>F1</td><td>I/O</td><td>I</td><td>32kHz crystal oscillator pin 1</td></tr>
<tr><td>X32N</td><td>E1</td><td>I/O</td><td>I</td><td>32kHz crystal oscillator pin 2</td></tr>
<tr><td>X48P</td><td>A4</td><td>—</td><td>I</td><td>48MHz crystal oscillator pin 1, Optional TCXO input</td></tr>
<tr><td>X48N</td><td>A5</td><td>—</td><td>I</td><td>48MHz crystal oscillator pin 2</td></tr>
<tr><td>CKMIN</td><td>B2</td><td>I/O</td><td>I</td><td>HFOSC tracking loop reference clock input</td></tr>
<tr><td>LFCI</td><td>F1</td><td>I/O</td><td>I</td><td>GPIO input for low frequency clock input (LFXT bypass clock from pin) or optional TCXO</td></tr>
</table>

Table 6-10. YCJ (WCSP) Peripheral Signal Descriptions Preview (continued)

FUNCTION	SIGNAL NAME	PIN NO. WCSP	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
Comparator	LPCO	D7	I/O	O	Low power comparator output
		F4			
		E1			
		G7			
		H8			
	LPC+	H2	I/O	I	Low power comparator positive input terminal
		G2			
		F2			
	LPC-	G2			Lower power comparator negative input terminal
		F2			
Digital Test Bus	DTB0	B2	I/O	O	Digital test bus output 0
	DTB1	E2			Digital test bus output 1
	DTB2	F2			Digital test bus output 2
	DTB3	G2			Digital test bus output 3
	DTB4	H2			Digital test bus output 4
	DTB5	F3			Digital test bus output 5
	DTB6	G3			Digital test bus output 6
	DTB7	G4			Digital test bus output 7
	DTB8	F5			Digital test bus output 8
	DTB9	G6			Digital test bus output 9
	DTB10	G8			Digital test bus output 10
	DTB11	F7			Digital test bus output 11
	DTB12	F6			Digital test bus output 12
	DTB13	E7			Digital test bus output 13
	DTB14	E8			Digital test bus output 14
	DTB15	D6			Digital test bus output 15

Table 6-10. YCJ (WCSP) Peripheral Signal Descriptions Preview (continued)

FUNCTION	SIGNAL NAME	PIN NO. WCSP	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
GPIO	GPIO0	D7	I/O	I/O	General-purpose input or output
	GPIO1	D6			
	GPIO2	E8			
	GPIO3	E7			
	GPIO4	F6			
	GPIO5	F7			
	GPIO6	G7			
	GPIO7	G8			
	GPIO8	H8			
	GPIO9	H7			
	GPIO10	H6			
	GPIO11	G6			
	GPIO12	F5			
	GPIO13	G5			
	GPIO14	H5			
	GPIO15	F4			
	GPIO16	G4			
	GPIO17	G3			
	GPIO18	F3			
	GPIO19	H2			
	GPIO20	G2			
	GPIO21	F2			
	GPIO22	E2			
	GPIO23	F1			
	GPIO24	E1			
	GPIO25	D3			
	GPIO26	D2			
	GPIO27	B2			
	GPIO28	B3			
	GPIO29	B4			
	GPIO30	B5			
I^2C	I2C0SCL	H7	I/O	I/O	I^2C clock
		F2			
		B2			
		D3			
		B4			
	I2C0SDA	H6	I/O	I/O	I^2C data
		E2			
		B3			
		D2			
		B5			

Table 6-10. YCJ (WCSP) Peripheral Signal Descriptions Preview (continued)

FUNCTION	SIGNAL NAME	PIN NO. WCSP	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
I^2S	I2S0MCLK	G4	I/O	O	I^2S main clockl
		G7	I/O	O	
	I2S0SCLK	E7	I/O	I/O	I^2S serial clock
		G3			
		D3			
	I2S0WS	G8	I/O	I/O	I^2S word select
		F3			
		D2			
	I2S0SD0	H7	I/O	I/O	I^2S serial data 0
		H2			
		B4			
	I2S0SD1	H6	I/O	I/O	I^2S serial data 1
		G2			
		B5			
	EXTCI	G4	I/O	I	I^2S external clock
LRF Digital Output	LRFD0	G3	I/O	O	LRF digital output 0
	LRFD1	F3			LRF digital output 1
	LRFD2	H2			LRF digital output 2
	LRFD3	G2			LRF digital output 3
	LRFD4	F2			LRF digital output 4
	LRFD5	E2			LRF digital output 5
	LRFD6	B2			LRF digital output 6
	LRFD7	B3			LRF digital output 7
Power	VDDR	C8	—	—	Internal supply
		A2			
	VDDS	H3	—	—	1.71V to 3.8V DIO supply
		C1			
		G1			
		A1			
		A3			
		A6			
	VDDD	D1	—	—	For decoupling of internal 1.32V regulated core-supply.
	VDDIO	F8	—	—	1.71V to 3.8V split rail I/O supply
		H4			
	DCDC	B1	—	—	Switching node of internal DC/DC converter
Reset	RSTN	H1	—	—	Global device reset (active low)
RF	ANT	A7	—	—	50-ohm RF port

Table 6-10. YCJ (WCSP) Peripheral Signal Descriptions Preview (continued)

FUNCTION	SIGNAL NAME	PIN NO. WCSP	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
SPI	SPI0SCLK	E7	I/O	I/O	SPI0 clock
		G2			
		B4			
	SPI0POCI	F6	I/O	I/O	SPI0 peripheral out controller in
		F7			
		E2			
		D2			
	SPI0CSN	G8	I/O	I/O	SPI0 chip-select
		H2			
		D3			
	SPI0PICO	F6	I/O	I/O	SPI0 peripheral in controller out
		F7			
		F2			
		B5			
	SPI1SCLK	F4	I/O	I/O	SPI1 clock
		E1			
		H8			
		D3			
	SPI1POCI	G6	I/O	I/O	SPI1 peripheral out controller in
		F5			
		B3			
		B5			
	SPI1CSN	G4	I/O	I/O	SPI1 chip select
		F1			
		B4			
	SPI1PICO	G6	I/O	I/O	SPI1 peripheral in controller out
		F5			
		B2			
		D2			
SWD	SWDIO	H7	I/O	I/O	Serial wire data input/output
	SWDCK	H6	I/O	I	Serial wire clock input
Trace	SWO	G6	I/O	O	Serial wire output

Table 6-10. YCJ (WCSP) Peripheral Signal Descriptions Preview (continued)

FUNCTION	SIGNAL NAME	PIN NO. WCSP	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
Timers - Capture/ Compare	T0C0	D7	I/O	I/O	Capture input-0 / compare/PWM output-0 of Timer-0
		G3			
		E1			
	T0C1	H7			Capture input-1 / compare/PWM output-1 of Timer-0
		F3			
	T0C2	H6			Capture input-2 / compare/PWM output-2 of Timer-0
		F1			
	T1C0	D7	I/O	I/O	Capture input-0 / compare/PWM output-0 of Timer-1
		D6			
		F1			
	T1C1	D6			Capture input-1 / compare/PWM output-1 of Timer-1
		E8			
	T1C2	E8			Capture input-2 / compare/PWM output-2 of Timer-1
		F6			
	T2C0	D6	I/O	I/O	Capture input-0 / compare/PWM output-0 of Timer-2
		E7			
	T2C1	F6			Capture input-1 / compare/PWM output-1 of Timer-2
		F7			
	T2C2	F7			Capture input-2 / compare/PWM output-2 of Timer-2
		G8			
	T3C0	G6	I/O	I/O	Capture input-0 / compare/PWM output-0 of Timer-3
		G4			
	T3C1	F5			Capture input-1 / compare/PWM output-1 of Timer-3
		F4			
		H8			
	T3C2	F5			Capture input-2 / compare/PWM output-2 of Timer-3
		F4			
		H8			

Table 6-10. YCJ (WCSP) Peripheral Signal Descriptions Preview (continued)

FUNCTION	SIGNAL NAME	PIN NO. WCSP	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
Timers - Complementary Capture/PWM	T0C0N	E1	I/O	O	Complementary compare/PWM output-0 from Timer-0
		G7			
	T0C1N	B2			Complementary compare/PWM output-1 from Timer-0
		G5			
	T0C2N	B3			Complementary compare/PWM output-2 from Timer-0
		H5			
	T1C0N	F4	I/O	O	Complementary compare/PWM output-0 from Timer-1
		H8			
		D3			
	T1C1N	F2			Complementary compare/PWM output-1 from Timer-1
		D2			
	T1C2N	E2			Complementary compare/PWM output-2 from Timer-1
		B4			
	T2C0N	H7	I/O	O	Complementary compare/PWM output-0 from Timer-2
	T2C1N	H6			Complementary compare/PWM output-1 from Timer-2
	T2C2N	F5			Complementary compare/PWM output-2 from Timer-2
	T3C0N	D7	I/O	O	Complementary compare/PWM output-0 from Timer-3
		B3			
	T3C1N	F7			Complementary compare/PWM output-1 from Timer-3
	T3C2N	G8			Complementary compare/PWM output-2 from Timer-3
Timers - Fault input	T1F	D7	I/O	I	Fault input for Timer-1
		G6			
		G4			
		G7			
Timers - Prescaler Event	T0PE	E8	I/O	O	Prescaler event output from Timer-0
		H7			
	T2PE	E7	I/O	O	Prescaler event output from Timer-2
		H6			

Table 6-10. YCJ (WCSP) Peripheral Signal Descriptions Preview (continued)

FUNCTION	SIGNAL NAME	PIN NO. WCSP	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
UART	UART0TXD	D6	I/O	O	UART0 TX data
		H2			
		G2			
		G5			
	UART0RXD	E8	I/O	I	UART0 RX data
		H2			
		G2			
		H5			
	UART0CTS	F3	I/O	I	UART0 clear-to-send input (active low)
	UART0RTS	G3	I/O	O	UART0 request-to-send (active low)
	UART1TXD	E7	I/O	O	UART1 TX data
		F2			
		G5			
	UART1RXD	F6	I/O	I	UART1 RX data
		E2			
		H5			
	UART1CTS	E1	I/O	I	UART1 clear-to-send input (active low)
	UART1RTS	F1	I/O	O	UART1 request-to-send (active low)

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
VDDS	Supply voltage	–0.3	4.1	V
VDDIO	Split rail I/O supply voltage	–0.3	4.1	V
V_{in_dio}	Voltage on any digital pin(3) (4)	–0.3	VDDS + 0.3 or VDDIO + 0.3, max 4.1	V
V_{in_x48}	Voltage on crystal oscillator pins X48P and X48N	–0.3	1.24	V
V_{in_adc}	Voltage on ADC input	0	VDDS	V
V_{in_rf}	Input level, RF pins		10	dBm
I_{in_dio}	Input clamp current on any DIO pin		±2	mA
T_{stg}	Storage temperature	–55	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to ground, unless otherwise noted.
(3) Including analog capable DIOs
(4) For list of digital IO pins that are powered by VDDS or VDDIO, refer to the *Pin Configurations and Functions* section in the data sheet.

7.2 ESD and MSL Ratings

				VALUE	UNIT
QFN packages					
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins	±1000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	All pins	±250	V
WCSP packages					
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins	Update at RTM	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	All pins	Update at RTM	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Operating ambient temperature(1) (2)	–40	125	°C
Operating junction temperature(1) (2)	–40	125	°C
Operating supply voltage (VDDS)	1.71	3.8	V
Operating split rail IO supply voltage (VDDIO)	1.71	3.8	V
Rising supply voltage slew rate	0	100	mV/µs
Falling supply voltage slew rate(3)	0	1	mV/µs

(1) Operation at or near maximum operating temperature for extended durations will result in a reduction in lifetime.
(2) For thermal resistance characteristics refer to *Thermal Resistance Characteristics* table in this document.
(3) For small coin-cell batteries, with high worst-case end-of-life equivalent source resistance, a 10µF VDDS input capacitor must be used to enable compliance with this slew rate.

7.4 DC/DC

Measured on the LP-EM-CC2745R10-Q1 reference design with T_c = 25°C, V_{DDS} = 3.0V with DC/DC enabled (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDDS supply voltage for DCDC operation(1)		2.2	3.0	3.8	V
Inductor at VDDR pin	Typical value of the component on PCB (2)		6.8		µH
Load capacitor at VDDR pin	Typical value of the component on PCB (2)		10		µF

(1) When the supply voltage drops below the DCDC operation min voltage, the device smoothly transitions to use the on-chip GLDO regulator.
(2) The capacitor and inductor tolerances of up to ±50% across temperature and overall part tolerance are considered.

7.5 GLDO

Measured on the LP-EM-CC2745R10-Q1 reference design with T_c = 25°C, V_{DDS} = 3.0V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDDS supply voltage for GLDO operation		1.71	3.0	3.8	V
Load capacitor at VDDR pin	Typical value of the component on PCB (1)		10		µF

(1) Capacitor tolerance of up to ±50% across temperature and overall part tolerance is considered.

7.6 Power Supply and Modules

Over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDDS BOD (brown-out detector)					
Untrimmed brownout rising threshold	Before initial boot (1)		1.62		V
Trimmed brownout rising threshold (1)			1.68		V
Trimmed brownout falling threshold (1)			1.67		V
VDDS POR (power-on-reset)					
POR power-up level			1.5		V
POR power-down level			1.45		V

(1) The brown-out detector is trimmed at initial boot. The value is kept until device is reset by a POR reset or the RSTN pin.

7.7 Battery Monitor

Measured on the LP-EM-CC2745R10-Q1 reference design with T_c = 25°C, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			22		mV
Range		1.71		3.8	V
Accuracy	VDDS = 3.0V		30		mV

7.8 BATMON Temperature Sensor

Measured on the LP-EM-CC2745R10-Q1 reference design with V_{DDS} = 3.0V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution	T_c = 25°C		1.7		°C
Accuracy	–40°C to 0°C		±4.0		°C
Accuracy	0°C to 125°C		±2.5		°C

7.9 Power Consumption—Power Modes

Measured on the LP-EM-CC2745R10-Q1 reference design T_c = 25°C, V_{DDS} = 3.0V, DC/DC enabled (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Core Current Consumption with DCDC						
I_{core}	Active	MCU running CoreMark from Flash at 96MHz		7.2		mA
I_{core}	Active	MCU running CoreMark from Flash at 96MHz, VDDS = 3.3V		6.8		mA
I_{core}	Idle	Supply Systems and SRAM powered, flash disabled, DMA disabled		1.5		mA
I_{core}	Idle	Supply Systems and SRAM powered, flash disabled, DMA disabled, VDDS = 3.3V		1.45		mA
I_{core}	Idle	Supply Systems and SRAM powered, flash disabled, DMA enabled		1.7		mA
I_{core}	Idle	Supply Systems and SRAM powered, flash disabled, DMA enabled, VDDS = 3.3V		1.6		mA
I_{core}	Idle	Supply Systems and SRAM powered, flash enabled, DMA disabled		1.9		mA
I_{core}	Idle	Supply Systems and SRAM powered, flash enabled, DMA disabled, VDDS = 3.3V		1.8		mA
I_{core}	Idle	Supply Systems and SRAM powered, flash enabled, DMA enabled		2.2		mA
I_{core}	Idle	Supply Systems and SRAM powered, flash enabled, DMA enabled, VDDS = 3.3V		2.1		mA
I_{core}	Standby	RTC running, full SRAM retention LFOSC, DCDC recharge current setting (ipeak[(1)] = 0)		0.95		µA
I_{core}	Standby	RTC running, full SRAM retention LFOSC, DCDC recharge current setting (ipeak[(1)] = 0), VDDS = 3.3V		0.9		µA
I_{core}	Standby	RTC running, full SRAM retention LFXT DCDC recharge current setting (ipeak[(1)] = 0)		1.0		uA
I_{core}	Standby	RTC running, full SRAM retention LFXT DCDC recharge current setting (ipeak[(1)] = 0), VDDS = 3.3V		0.9		uA
Core Current consumption with GLDO						
I_{core}	Active	MCU running CoreMark from Flash at 96 MHz, DC/DC disabled		11.2		mA
I_{core}	Idle	Supply Systems and RAM powered, flash disabled, DMA disabled, DC/DC disabled		2.45		mA
I_{core}	Idle	Supply Systems and RAM powered, flash disabled, DMA enabled, DC/DC disabled		2.75		mA
I_{core}	Idle	Supply Systems and RAM powered, flash enabled, DMA disabled, DC/DC disabled		2.8		mA
I_{core}	Idle	Supply Systems and RAM powered, flash enabled, DMA enabled, DC/DC disabled		3.4		mA
I_{core}	Standby	RTC running, full SRAM retention, DC/DC disabled LFOSC, default GLDO recharge current setting		1.5		µA
I_{core}	Standby	RTC running, full SRAM retention, DC/DC disabled LFXT, default GLDO recharge current setting		1.6		uA
Reset, Shutdown Current Consumption						
I_{core}	Reset	Reset. RSTN pin asserted or VDDS below power-on-reset threshold		170		nA
I_{core}	Shutdown	Shutdown measured in steady state. No clocks running, no retention, IO wakeup enabled		160		nA
Peripheral Current Consumption						
I_{peri}	RF	Delta current with clock enabled, RF subsystem idle		80		µA
I_{peri}	Timers	Delta current with clock enabled, module is idle[(2)]		6.5		µA
I_{peri}	I^2C	Delta current with clock enabled, module is idle		11		µA
I_{peri}	SPI	Delta current with clock enabled, module is idle[(3)]		5		µA
I_{peri}	UART	Delta current with clock enabled, module is idle[(4)]		43		µA
I_{peri}	I^2S	Delta current with clock enabled, module is idle		190		µA
I_{peri}	CRYPTO (LAES)	Delta current with clock enabled, module is idle		10		µA
I_{peri}	APU	Delta current with clock enabled, module is idle		186		µA

(1) Ipeak refers to the programmable DCDC peak current setting used to vary the maximum DCDC load support.
(2) Only one LGPT timer instance enabled
(3) Only one SPI peripheral instance enabled
(4) Only one UART peripheral instance enabled

7.10 Power Consumption—Radio Modes (R variant)

Measured on the LP-EM-CC2745R10-Q1 reference design with T_c = 25°C, V_{DDS} = 3.0V with DC/DC enabled (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{RX}	Radio receive current	2440MHz, 1Mbps, system bus off (1)		6.7		mA
I_{RX}	Radio receive current	2440MHz, 1Mbps, V_{DDS} = 3.3V, system bus off (1)		6.1		mA
I_{RX}	Radio receive current	2440MHz, 1Mbps, DC/DC disabled, system bus off (1)		11.7		mA
I_{TX}	Radio transmit current	-8dBm output power setting 2440MHz, system bus off (1)		5.7		mA
I_{TX}	Radio transmit current	-8dBm output power setting 2440MHz, V_{DDS} = 3.3V, system bus off (1)		5.3		mA
I_{TX}	Radio transmit current	0dBm output power setting 2440MHz, system bus off (1)		8.4		mA
I_{TX}	Radio transmit current	0dBm output power setting 2440MHz, V_{DDS} = 3.3V, system bus off (1)		7.7		mA
I_{TX}	Radio transmit current	0dBm output power setting 2440MHz DC/DC disabled, system bus off (1)		14.7		mA
I_{TX}	Radio transmit current	+4dBm output power setting 2440MHz, system bus off (1)		10.6		mA
I_{TX}	Radio transmit current	+4dBm output power setting 2440MHz, V_{DDS} = 3.3V, system bus off (1)		9.7		mA
I_{TX}	Radio transmit current	+6dBm output power setting 2440MHz, system bus off (1)		19.4		mA
I_{TX}	Radio transmit current	+6dBm output power setting 2440MHz, V_{DDS} = 3.3V, system bus off (1)		17.7		mA
I_{TX}	Radio transmit current	+8dBm output power setting 2440MHz, system bus off (1)		22.3		mA
I_{TX}	Radio transmit current	+8dBm output power setting 2440MHz, V_{DDS} = 3.3V, system bus off (1)		20.3		mA
I_{TX}	Radio transmit current	+8dBm output power setting 2440MHz DC/DC disabled		38.6		mA
I_{TX}	Radio transmit current	+10dBm output power setting 2440MHz, system bus off (1)		27.1		mA
I_{TX}	Radio transmit current	+10dBm output power setting 2440MHz, V_{DDS} = 3.3V, system bus off (1)		24.5		mA
I_{TX}	Radio transmit current	+10dBm output power setting 2440MHz DC/DC disabled, system bus off (1)		46.5		mA

(1) System bus off refers to device idle mode, DMA disabled and flash disabled.

7.11 Power Consumption–Radio Modes (P variant)

Measured on the LP-EM-CC2755P10 (P variant) reference design with T_c = 25°C, V_{DDS} = 3.0V with DC/DC enabled (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{RX}	Radio receive current	2440MHz, 1Mbps, system bus off (1)		6.8		mA
I_{RX}	Radio receive current	2440MHz, 1Mbps, V_{DDS} = 3.3V, system bus off (1)		6.2		mA
I_{RX}	Radio receive current	2440MHz, 1Mbps, DC/DC disabled, system bus off (1)		11.7		mA
I_{TX}	Radio transmit current	-8dBm output power setting 2440MHz, system bus off (1)		6.2		mA
I_{TX}	Radio transmit current	-8dBm output power setting 2440MHz, V_{DDS} = 3.3V, system bus off (1)		5.8		mA
I_{TX}	Radio transmit current	0dBm output power setting 2440MHz, system bus off (1)		9.3		mA
I_{TX}	Radio transmit current	0dBm output power setting 2440MHz, V_{DDS} = 3.3V, system bus off (1)		8.6		mA
I_{TX}	Radio transmit current	0dBm output power setting 2440MHz DC/DC disabled, system bus off (1)		15.8		mA

Measured on the LP-EM-CC2755P10 (P variant) reference design with T_c = 25°C, V_{DDS} = 3.0V with DC/DC enabled (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{TX}	Radio transmit current	+4dBm output power setting 2440MHz, system bus off (1)		10.8		mA
I_{TX}	Radio transmit current	+4dBm output power setting 2440MHz, V_{DDS} = 3.3V, system bus off (1)		10.0		mA
I_{TX}	Radio transmit current	+6dBm output power setting 2440MHz, system bus off (1)		21.9		mA
I_{TX}	Radio transmit current	+6dBm output power setting 2440MHz, V_{DDS} = 3.3V, system bus off (1)		20.0		mA
I_{TX}	Radio transmit current	+8dBm output power setting 2440MHz, system bus off (1)		25.8		mA
I_{TX}	Radio transmit current	+8dBm output power setting 2440MHz, V_{DDS} = 3.3V, system bus off (1)		23.5		mA
I_{TX}	Radio transmit current	+8dBm output power setting 2440MHz DC/DC disabled		44.4		mA
I_{TX}	Radio transmit current	+10dBm output power setting 2440MHz, system bus off (1)		30.7		mA
I_{TX}	Radio transmit current	+10dBm output power setting 2440MHz, V_{DDS} = 3.3V, system bus off (1)		28.2		mA
I_{TX}	Radio transmit current	+10dBm output power setting 2440MHz DC/DC disabled, system bus off (1)		53		mA
I_{TX}	Radio transmit current	+12 dBm output power setting 2440 MHz, system bus off (1)		52		mA
I_{TX}	Radio transmit current	+12 dBm output power setting 2440 MHz, V_{DDS} = 3.3 V, system bus off (1)		52		mA
I_{TX}	Radio transmit current	+14 dBm output power setting 2440 MHz, system bus off (1)		62		mA
I_{TX}	Radio transmit current	+14 dBm output power setting 2440 MHz, V_{DDS} = 3.3 V, system bus off (1)		62		mA
I_{TX}	Radio transmit current	+16 dBm output power setting 2440 MHz, system bus off (1)		75		mA
I_{TX}	Radio transmit current	+16 dBm output power setting 2440 MHz, V_{DDS} = 3.3 V, system bus off (1)		75		mA
I_{TX}	Radio transmit current	+18 dBm output power setting 2440 MHz, system bus off (1)		99		mA
I_{TX}	Radio transmit current	+18 dBm output power setting 2440 MHz, V_{DDS} = 3.3 V, system bus off (1)		101		mA
I_{TX}	Radio transmit current	+20 dBm output power setting 2440 MHz, system bus off (1)		127		mA
I_{TX}	Radio transmit current	+20 dBm output power setting 2440 MHz, V_{DDS} = 3.3 V, system bus off (1)		132		mA
I_{TX}	Radio transmit current	+20 dBm output power setting 2440 MHz DC/DC disabled, system bus off (1)		136		mA
I_{TX}	Radio transmit current	+20 dBm output power setting 2440 MHz DC/DC disabled, V_{DDS} = 3.3 V, system bus off (1)		143		mA

(1) System bus off refers to device idle mode, DMA disabled and flash disabled.

7.12 Nonvolatile (Flash) Memory Characteristics

Over operating free-air temperature range and V_{DDS} = 3.0V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Flash sector size			2		KB

7.12 Nonvolatile (Flash) Memory Characteristics (continued)

Over operating free-air temperature range and V_{DDS} = 3.0V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supported flash erase cycles before failure, full bank(1) (2)		30			k Cycles
Supported flash erase cycles before failure, single sector(3)		60			k Cycles
Maximum number of write operations per row before sector erase(4)				83	Write Operations
Flash retention	105°C	11.4			Years
Flash retention	125°C	10			Years
Flash sector erase current (5)			5.8		mA
Flash sector erase time(6)	0 erase cycles		2.2		ms
Flash write current (5)	full sector at a time		6.6		mA
Flash write time(6)	full sector (2KB) at a time, 0 erase cycles		8		ms

(1) A full bank erase is counted as a single erase cycle on each sector.
(2) Aborting flash during erase or program modes is not a safe operation.
(3) Up to 16 customer-designated sectors can be individually erased an additional 30k times beyond the baseline bank limitation of 30k cycles.
(4) Each wordline is 2048 bits (or 256 bytes) wide. This limitation corresponds to sequential memory writes of 4 (3.1) bytes minimum per write over a whole wordline. If additional writes to the same wordline are required, a sector erase is required once the maximum number of write operations per row is reached.
(5) Current consumption when device is performing erase or write operations to a flash sector. DC/DC enabled (ipeak = 0). All peripherals are disabled.
(6) This number is dependent on flash aging and increases over time and erase cycles.

7.13 Thermal Resistance Characteristics

THERMAL METRIC	THERMAL METRIC	PACKAGE		UNIT(1)
		RKP (VQFN)	WCSP	
		40 PINS	62 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	26.4	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	14.7	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.1	TBD	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	TBD	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	8.1	TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.6	TBD	°C/W

(1) °C/W = degrees Celsius per watt

7.14 RF Frequency Bands

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	MIN	TYP	MAX	UNIT
Frequency bands	2360		2500	MHz

7.15 Bluetooth Low Energy—Receive (RX)

Measured on the LP-EM-CC2745R10-Q1 reference design with T_c = 25°C, V_{DDS} = 3.0V, f_{RF} = 2440MHz with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
125kbps (LE Coded)					
Receiver sensitivity	BER = 10^{-3}		–103.5		dBm
Receiver saturation	BER = 10^{-3}		10		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency		> (–250 / 250)(1)		kHz
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (37-byte packets)		> (–90 / 90)(1)		ppm
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (255-byte packets)		> (–90 / 90)(1)		ppm
Co-channel rejection(2)	Wanted signal at –79dBm, modulated interferer in channel, BER = 10^{-3}		–1.5		dB
Selectivity, ±1MHz(2)	Wanted signal at –79dBm, modulated interferer at ±1MHz, BER = 10^{-3}		8.5 / 4.5(3)		dB
Selectivity, ±2MHz(2)	Wanted signal at –79dBm, modulated interferer at ±2MHz, BER = 10^{-3}		42 / 31(3)		dB
Selectivity, ±3MHz(2)	Wanted signal at –79dBm, modulated interferer at ±3MHz, BER = 10^{-3}		42 / 40(3)		dB
Selectivity, ±4MHz(2)	Wanted signal at –79dBm, modulated interferer at ±4MHz, BER = 10^{-3}		44 / 42(3)		dB
Selectivity, ±6MHz(2)	Wanted signal at –79dBm, modulated interferer at ≥ ±6MHz, BER = 10^{-3}		49 / 43(3)		dB
Selectivity, ±7MHz	Wanted signal at –79dBm, modulated interferer at ≥ ±7MHz, BER = 10^{-3}		51 / 45(3)		dB
Selectivity, Image frequency(2)	Wanted signal at –79dBm, modulated interferer at image frequency, BER = 10^{-3}		31		dB
Selectivity, Image frequency ±1MHz(2)	Note that Image frequency + 1MHz is the co-channel – 1MHz. Wanted signal at –79dBm, modulated interferer at ±1MHz from image frequency, BER = 10^{-3}		4.5 / 40 (3)		dB
500kbps (LE Coded)					
Receiver sensitivity	BER = 10^{-3}		–99		dBm
Receiver saturation	BER = 10^{-3}		10		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency		> (–250 / 250)(1)		kHz
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (37-byte packets)		> (–90 / 90)(1)		ppm
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (255-byte packets)		> (–90 / 90)(1)		ppm
Co-channel rejection(2)	Wanted signal at –72dBm, modulated interferer in channel, BER = 10^{-3}		–3.5		dB
Selectivity, ±1MHz(2)	Wanted signal at –72dBm, modulated interferer at ±1MHz, BER = 10^{-3}		8 / 4.5(3)		dB
Selectivity, ±2MHz(2)	Wanted signal at –72dBm, modulated interferer at ±2MHz, BER = 10^{-3}		40 / 28(3)		dB
Selectivity, ±3MHz(2)	Wanted signal at –72dBm, modulated interferer at ±3MHz, BER = 10^{-3}		40 / 38(3)		dB
Selectivity, ±4MHz(2)	Wanted signal at –72dBm, modulated interferer at ±4MHz, BER = 10^{-3}		42 / 40(3)		dB
Selectivity, ±6MHz(2)	Wanted signal at –72dBm, modulated interferer at ≥ ±6MHz, BER = 10^{-3}		46 / 41(3)		dB
Selectivity, ±7MHz	Wanted signal at –72dBm, modulated interferer at ≥ ±7MHz, BER = 10^{-3}		48 / 42(3)		dB
Selectivity, Image frequency(2)	Wanted signal at –72dBm, modulated interferer at image frequency, BER = 10^{-3}		28		dB

7.15 Bluetooth Low Energy—Receive (RX) (continued)

Measured on the LP-EM-CC2745R10-Q1 reference design with T_c = 25°C, V_{DDS} = 3.0V, f_{RF} = 2440MHz with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Selectivity, Image frequency ±1MHz(2)	Note that Image frequency + 1MHz is the co-channel – 1MHz. Wanted signal at –72dBm, modulated interferer at ±1MHz from image frequency, BER = 10^{-3}		4.5 / 38(3)		dB
1Mbps (LE 1M)					
Receiver sensitivity	BER = 10^{-3}		–97		dBm
Receiver saturation	BER = 10^{-3}		10		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency		> (–250 / 250)(1)		kHz
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate,		> (–90 / 90)(1)		ppm
Co-channel rejection(2)	Wanted signal at –67dBm, modulated interferer in channel, BER = 10^{-3}		–5.5		dB
Selectivity, ±1MHz(2)	Wanted signal at –67dBm, modulated interferer at ±1MHz, BER = 10^{-3}		7.8 / 5.6(3)		dB
Selectivity, ±2MHz(2)	Wanted signal at –67dBm, modulated interferer at ±2MHz,BER = 10^{-3}		39 / 26(3)		dB
Selectivity, ±3MHz(2)	Wanted signal at –67dBm, modulated interferer at ±3MHz, BER = 10^{-3}		36 / 36(3)		dB
Selectivity, ±4MHz(2)	Wanted signal at –67dBm, modulated interferer at ±4MHz, BER = 10^{-3}		46 / 34(3)		dB
Selectivity, ±5MHz or more(2)	Wanted signal at –67dBm, modulated interferer at ≥ ±5MHz, BER = 10^{-3}		56		dB
Selectivity, image frequency(2)	Wanted signal at –67dBm, modulated interferer at image frequency, BER = 10^{-3}		26		dB
Selectivity, image frequency ±1MHz(2)	Note that Image frequency + 1MHz is the co-channel – 1MHz. Wanted signal at –67dBm, modulated interferer at ±1MHz from image frequency, BER = 10^{-3}		5.6 / 36(3)		dB
Out-of-band blocking(4)	30 MHz to 2000 MHz		–10		dBm
Out-of-band blocking	2003MHz to 2399MHz		–10		dBm
Out-of-band blocking	2484MHz to 2997MHz		–10		dBm
Out-of-band blocking	3000MHz to 12.75GHz (excluding VCO frequency)		–2		dBm
Intermodulation	Wanted signal at 2402MHz, –64dBm. Two interferers at 2405MHz and 2408MHz respectively, at the given power level		–38		dBm
Spurious emissions, 30MHz to 1000MHz(5)	Measurement in a 50Ω single-ended load.		< –59		dBm
Spurious emissions, 1GHz to 12.75GHz(5)	Measurement in a 50Ω single-ended load.		< –47		dBm
RSSI dynamic range(6)			67		dB
RSSI accuracy			±4		dB
RSSI resolution			1		dB
2Mbps (LE 2M)					
Receiver sensitivity	Measured at SMA connector, BER = 10^{-3}		–93		dBm
Receiver saturation	Measured at SMA connector, BER = 10^{-3}		10		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency		> (–250 / 250)(1)		kHz
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (255-byte packets)		> (–90 / 90)(1)		ppm
Co-channel rejection(2)	Wanted signal at –67dBm, modulated interferer in channel,BER = 10^{-3}		–7		dB
Selectivity, ±2MHz(2)	Wanted signal at –67dBm, modulated interferer at ±2MHz, Image frequency is at –2MHz, BER = 10^{-3}		9.5/ 6(3)		dB
Selectivity, ±4MHz(2)	Wanted signal at –67dBm, modulated interferer at ±4MHz, BER = 10^{-3}		37 / 29(3)		dB

7.15 Bluetooth Low Energy—Receive (RX) (continued)

Measured on the LP-EM-CC2745R10-Q1 reference design with T_c = 25°C, V_{DDS} = 3.0V, f_{RF} = 2440MHz with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Selectivity, ±6MHz(2)	Wanted signal at –67dBm, modulated interferer at ±6MHz, BER = 10^{-3}		40 / 36(3)		dB
Selectivity, image frequency(2)	Wanted signal at –67dBm, modulated interferer at image frequency, BER = 10^{-3}		6		dB
Selectivity, image frequency ±2MHz(2)	Note that Image frequency + 2MHz is the Co-channel. Wanted signal at –67dBm, modulated interferer at ±2MHz from image frequency, BER = 10^{-3}		–7 / 29(3)		dB
Out-of-band blocking(4)	30MHz to 2000MHz		–10		dBm
Out-of-band blocking	2003MHz to 2399MHz		–10		dBm
Out-of-band blocking	2484MHz to 2997MHz		–10		dBm
Out-of-band blocking	3000MHz to 12.75GHz (excluding VCO frequency)		–2		dBm
Intermodulation	Wanted signal at 2402MHz, –64dBm. Two interferers at 2408 and 2414MHz respectively, at the given power level		–38		dBm

(1) Actual performance exceeding Bluetooth specification listed here
(2) Numbers given as I/C dB
(3) X / Y, where X is +N MHz and Y is –N MHz
(4) Excluding one exception at F_{wanted} / 2, per Bluetooth Specification
(5) Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan)
(6) The device will saturate at –30dBm.

7.16 Bluetooth Low Energy—Transmit (TX)

Measured on the LP-EM-CC2745R10-Q1 (R variant) reference design with T_c = 25°C, V_{DDS} = 3.0V, f_{RF} = 2440MHz with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

VARIANT	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
General Parameters						
R variant	Max output power	Delivered to a single-ended 50Ω load through integrated balun		10		dBm
R variant	Output power programmable range	Delivered to a single-ended 50Ω load through integrated balun		30		dB
P variant	Max output power	Delivered to a single-ended 50Ω load through integrated balun		20		dBm
P variant	Output power programmable range	Delivered to a single-ended 50Ω load through integrated balun		40		dB

7.17 Bluetooth Channel Sounding

Measured on the LP-EM-CC2745R10-Q1 reference design with T_c = 25°C, V_{DDS} = 3.3V, f_{RF} = 2440MHz, Tx output power = +10dBm with DC/DC enabled (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
General Parameters						
	Supported PHY data rate		1		2	Mbps
T_IP1	Range of Interlude Time between Packets		40		145	µs
T_IP2	Range of Interlude Time between CS Tones		40		145	µs
T_FCS	Range of Time for Frequency Change Spacing		100		150	µs
T_PM	Range of Time for Phase Measurement		10		40	µs
T_SW	Range of Antenna switch time		0		10	µs
T_GD	Guard Time between modulated bits and CS Tones			10		µs
T_FM	Time for Frequency Measurement			80		µs

7.17 Bluetooth Channel Sounding (continued)

Measured on the LP-EM-CC2745R10-Q1 reference design with T_c = 25°C, V_{DDS} = 3.3V, f_{RF} = 2440MHz, Tx output power = +10dBm with DC/DC enabled (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
N_AP	Number of Antenna Paths		1		4	

7.18 Zigbee and Thread—IEEE 802.15.4-2006 2.4GHz (OQPSK DSSS1:8, 250kbps) - RX

Measured on the LP-EM-CC2745R10-Q1 reference design with T_c = 25°C, V_{DDS} = 3.0V, f_{RF}= 2440MHz with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
General Parameters					
Receiver sensitivity	PER = 1%		–103		dBm
Receiver saturation	PER = 1%		> 5		dBm
Adjacent channel rejection	Wanted signal at –82dBm, modulated interferer at ±5MHz, PER = 1%		40		dB
Alternate channel rejection	Wanted signal at –82dBm, modulated interferer at ±10MHz, PER = 1%		57		dB
Channel rejection, ±15MHz or more	Wanted signal at –82dBm, undesired signal is IEEE 802.15.4 modulated channel, stepped through all channels 2405 to 2480MHz, PER = 1%		63		dB
Blocking and desensitization, 5MHz from upper band edge	Wanted signal at –100dBm (3dB above the sensitivity level), CW jammer, PER = 1%		68		dB
Blocking and desensitization, 10MHz from upper band edge	Wanted signal at –100dBm (3dB above the sensitivity level), CW jammer, PER = 1%		69		dB
Blocking and desensitization, 20MHz from upper band edge	Wanted signal at –100dBm (3dB above the sensitivity level), CW jammer, PER = 1%		70		dB
Blocking and desensitization, 50MHz from upper band edge	Wanted signal at –100dBm (3dB above the sensitivity level), CW jammer, PER = 1%		71		dB
Blocking and desensitization, –5MHz from lower band edge	Wanted signal at –100dBm (3dB above the sensitivity level), CW jammer, PER = 1%		67		dB
Blocking and desensitization, –10MHz from lower band edge	Wanted signal at –100dBm (3dB above the sensitivity level), CW jammer, PER = 1%		68		dB
Blocking and desensitization, –20MHz from lower band edge	Wanted signal at –100dBm (3dB above the sensitivity level), CW jammer, PER = 1%		69		dB
Blocking and desensitization, –50MHz from lower band edge	Wanted signal at –100dBm (3dB above the sensitivity level), CW jammer, PER = 1%		70		dB
Spurious emissions, 1GHz to 12.75GHz	Measurement in a 50Ω single-ended load[(1)]		–53		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency		> (–100/100)		ppm
Symbol rate error tolerance	Difference between incoming symbol rate and the internally generated symbol rate		> (–100/100)		ppm
RSSI dynamic range			93		dB
RSSI accuracy			±4		dB

(1) Suitable for systems targeting compliance with EN 300 328, EN 300 440 class 2 (Europe), FCC CFR47, Part 15 (US) and ARIB STD-T-66 (Japan)

7.19 Zigbee and Thread—IEEE 802.15.4-2006 2.4GHz (OQPSK DSSS1:8, 250kbps) - TX

Measured on the LP-EM-CC2745R10-Q1 reference design with T_c = 25°C, V_{DDS} = 3.0V, f_{RF}= 2440MHz with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
General Parameters						
Max output power (R variant)	Delivered to a single-ended 50Ω load through integrated balun			10		dBm
Output power programmable range (R variant)	Delivered to a single-ended 50Ω load through integrated balun	Delivered to a single-ended 50Ω load through integrated balun		30		dB
PA step increment	Delivered to a single-ended 50Ω load through integrated balun	Differential mode, delivered to a single-ended 50Ω load through integrated balun		1		dB
IEEE 802.15.4-2006 2.4 GHz (OQPSK DSSS1:8, 250 kbps)						

7.19 Zigbee and Thread—IEEE 802.15.4-2006 2.4GHz (OQPSK DSSS1:8, 250kbps) - TX (continued)

Measured on the LP-EM-CC2745R10-Q1 reference design with T_c = 25°C, V_{DDS} = 3.0V, f_{RF}= 2440MHz with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Error vector magnitude, (R variant)	+10dBm setting	+10dBm setting		2%		

7.20 2.4GHz RX/TX CW

Measured on the LP-EM-CC2745R10-Q1 (R variant) reference design with T_c = 25°C, V_{DDS} = 3.0V, f_{RF} = 2440MHz with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

VARIANT	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Spurious emissions and harmonics							
R Variant,P Variant	Spurious emissions(1) (2) (3)	f < 1GHz, outside restricted bands	+10dBm setting		< –36		dBm
		f < 1GHz, restricted bands ETSI, MIIT			< –54		dBm
		f < 1GHz, restricted bands FCC			< –55		dBm
		f > 1GHz, including harmonics (ETSI)			< –30		dBm
		f > 1GHz (2300 - 2390 MHz, 2483.5 - 2500 MHz) (MIIT)			< –40		dBm
		f > 1GHz (2390 - 2400 MHz) (MIIT)			< –30		dBm
	Harmonics (1)	Second harmonic			< –42		dBm
		Third harmonic			< –42		dBm
P Variant	Spurious emissions(1) (2) (3) (4)	f < 1 GHz, outside restricted bands	+20 dBm setting		< –36		dBm
		f < 1GHz, restricted bands ETSI, MIIT			< –54		dBm
		f < 1 GHz, restricted bands FCC			< –55		dBm
		f > 1GHz, including harmonics (ETSI)			< –30		dBm
		f > 1GHz (2300 - 2390 MHz, 2483.5 - 2500 MHz) (MIIT)			< –40		dBm
		f > 1GHz (2390 - 2400 MHz) (MIIT)			< –30		dBm
	Harmonics(1)	Second harmonic			< –42		dBm
		Third harmonic			< –42		dBm

(1) Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), MIIT (China), and ARIB STD-T66 (Japan).
(2) To enable margins for passing FCC band edge requirements at 2483.5MHz, a lower than maximum output-power setting or less than 100% duty cycle may be used when operating at the upper 802.15.4 channel(s).
(3) To enable margin for passing MIIT band edge requirements at 2400 MHz and 2483.5 MHz, a lower than maximum output-power setting may be used when operating at the lower and upper BLE channels
(4) To enable margin for passing ETSI band edge requirements at 2400 MHz, a lower than maximum output-power setting may be used when operating at the lower BLE channel

7.21 Timing and Switching Characteristics

7.21.1 Reset Timing

PARAMETER	MIN	TYP	MAX	UNIT
RSTN low duration	1			µs

7.21.2 Wakeup Timing

Measured over operating free-air temperature with V_{DDS} = 3.0V (unless otherwise noted). The times listed here do not include any software overhead (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MCU, Reset/Shutdown to Active[(1)]		GLDO default charge current setting, VDDR capacitor fully charged[(2)]		350–450		µs
MCU, Standby to Active	MCU, Standby to Active[(3)](ready to execute code from flash), VGM disabled coming out of standby mode	DC/DC enabled, default recharge current configuration		43		µs
MCU, Standby to Active	MCU, Standby to Active[(3)] (ready to execute code from flash), VGM disabled coming out of standby mode	GLDO enabled, default recharge current configuration		43		µs
MCU, Standby to Active	MCU, Standby to Active (ready to execute code from flash), VGM enabled coming out of standby mode	DC/DC enabled, default recharge current configuration		80		µs
MCU, Standby to Active	MCU, Standby to Active (ready to execute code from flash), VGM enabled coming out of standby mode	GLDO enabled, default recharge current configuration		80		µs
MCU, Idle to Active		Flash enabled in idle mode		3		µs
		Flash disabled in idle mode		15		µs

(1) Wakeup time includes system ROM bootcode execution time (excluding any system ROM secure boot operations). The wakeup time is dependent on the remaining charge on VDDR capacitor when starting the device, and thus how long the device has been in Reset or Shutdown before starting up again.
(2) This is the best case Reset/Shutdown mode to Active mode time including system ROM bootcode operation (excluding any system ROM secure boot operations) for the specified GLDO charge current setting considering the VDDR capacitor is fully charged and is not discharged during the reset and shutdown events; that is, when the device is in reset / shutdown modes for only a very short period of time
(3) Dependent on VDDR capacitor voltage level

7.21.3 Clock Specifications

7.21.3.1 48MHz Crystal Oscillator (HFXT)

Measured on the LP-EM-CC2745R10-Q1 reference design with T_c = 25°C, V_{DDS} = 3.0V, unless otherwise noted.

	PARAMETER	MIN	TYP	MAX	UNIT
	Crystal frequency		48		MHz
ESR	Equivalent series resistance 6 pF < C_L ≤ 9 pF		20	60	Ω
	Equivalent series resistance 5 pF ≤ C_L ≤ 6 pF			80	Ω
C_L	Crystal load capacitance(1)	5	7(2)	9	pF
Start-up time(3)	Until clock is qualified.		130		µs

(1) Adjustable load capacitance is integrated into the device. External load capacitors are required for systems targeting compliance with certain regulations.
(2) On-chip default connected capacitance including reference design parasitic capacitance. Connected internal capacitance is changed through software in the Customer Configuration section (CCFG).
(3) Start-up time using the TI-provided power driver. Start-up time may increase if the driver is not used.

7.21.3.2 96MHz RC Oscillator (HFOSC)

Measured on the LP-EM-CC2745R10-Q1 reference design with T_c = 25°C, V_{DDS} = 3.0V, unless otherwise noted.

		MIN	TYP	MAX	UNIT
Center Frequency			96		MHz
Uncalibrated frequency accuracy	Frequency accuracy until HFXT tracking loop is enabled.		±3		%

7.21.3.3 80/90/98MHz RC Oscillator (AFOSC)

Measured on the LP-EM-CC2745R10-Q1 reference design with T_c = 25°C, V_{DDS} = 3.0V, unless otherwise noted.

	MIN	TYP	MAX	UNIT
Center Frequency		80 90.3168 98.304		MHz

7.21.3.4 32kHz Crystal Oscillator (LFXT)

Measured on the LP-EM-CC2745R10-Q1 reference design with T_c = 25°C, V_{DDS} = 3.0V, unless otherwise noted.

	MIN	TYP	MAX	UNIT
Crystal frequency		32.768		kHz
Supported crystal load capacitance	6		12	pF
ESR (Equivalent Series Resistance)		30	100	kΩ

7.21.3.5 32kHz RC Oscillator (LFOSC)

Measured on the LP-EM-CC2745R10-Q1 reference design with T_c = 25°C, V_{DDS} = 3.0V, unless otherwise noted.

		MIN	TYP	MAX	UNIT
Calibrated frequency			32.768(1)		kHz
Clock accuracy	Sleep clock accuracy when using LFOSC(2)		±500(3)		ppm

(1) When using LFOSC as a source for the low-frequency system clock (LFCLK), the accuracy of the LFCLK-derived Real Time Clock (RTC) can be improved by measuring LFOSC relative to HFXT and compensating for the RTC tick speed. This functionality is available through the TI-provided Power driver.
(2) Suitable for crystal-less operation of both Bluetooth LE peripheral and central roles with periodic RTC calibration using device HW and SW that is configured through the TI SysConfig tool. For further guidance, please reach out to Texas Instruments for support.
(3) The actual value is lower than ±500ppm prescribed by Bluetooth LE sleep clock accuracy specification.

7.22 Peripheral Characteristics

7.22.1 UART

7.22.1.1 UART Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT
UART rate			3	MBaud

7.22.2 SPI

7.22.2.1 SPI Characteristics

Using TI SPI driver, over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCLK} 1/tsclk	SPI clock frequency	Contoller and Peripheral Mode(1) 2.7V ≤ VDDS < 3.8V(2)			12	MHz
		Controller and Peripheral Mode(1) VDDS < 2.7V(2)			8	
DC_{SCLK}	SCLK Duty Cycle		45%	50%	55%	

(1) Assume interfacing with ideal SPI controller and SPI peripheral devices
(2) If VDDIO supply is used to power the specific pins whose DIOs are configured for SPI operation, then, the supply range applies to VDDIO in this case.

7.22.2.2 SPI Controller Mode

Using TI SPI driver, over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{SCLK\_H/L}$	SCLK high or gow time		$(t_{SPI}/2) - 1$	$t_{SPI} / 2$	$(t_{SPI}/2) + 1$	ns
$t_{CS.LEAD}$	CS lead-time, CS active to clock		1			SCLK
$t_{CS.LAG}$	CS lag time, last clock to CS inactive		1			SCLK
$t_{CS.ACC}$	CS access time, CS active to PICO data out				1	SCLK
$t_{CS.DIS}$	CS disable time, CS inactive to PICO high impedance				1	SCLK
$t_{HD.CI}$	POCI input data hold time		0			ns
$t_{VALID.CO}$	PICO output data valid time(1)	SCLK edge to PICO valid,C_L = 20pF			13	ns
$t_{HD.CO}$	PICO output data hold time(2)	C_L = 20pF	0			ns

(1) Specifies the time to drive the next valid data to the output after the output changing SCLK clock edge
(2) Specifies how long data on the output is valid after the output changing SCLK clock edge

7.22.2.3 SPI Timing Diagrams—Controller Mode

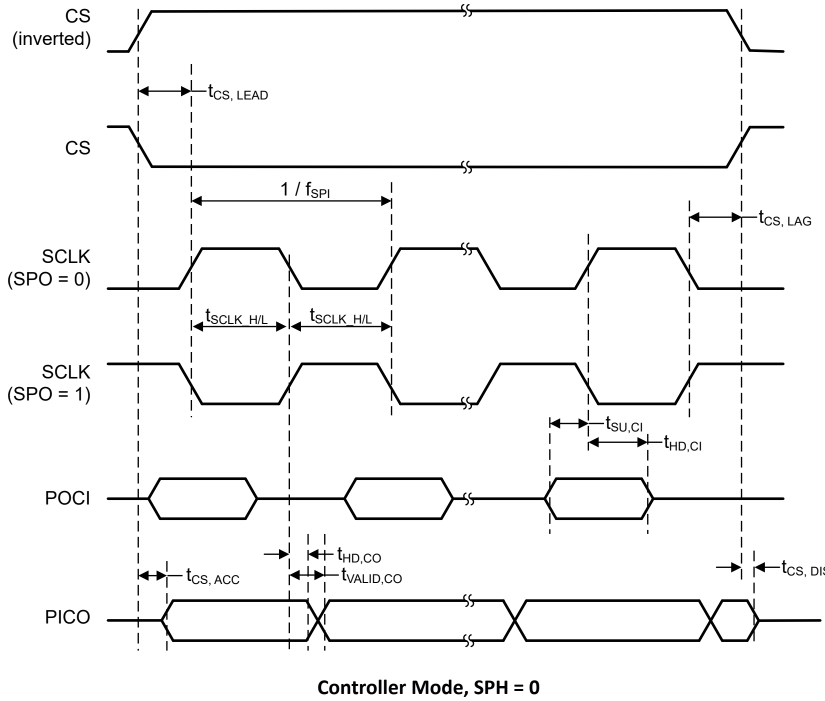

Figure 7-1. SPI Timing Diagram—Controller Mode, SPH = 0

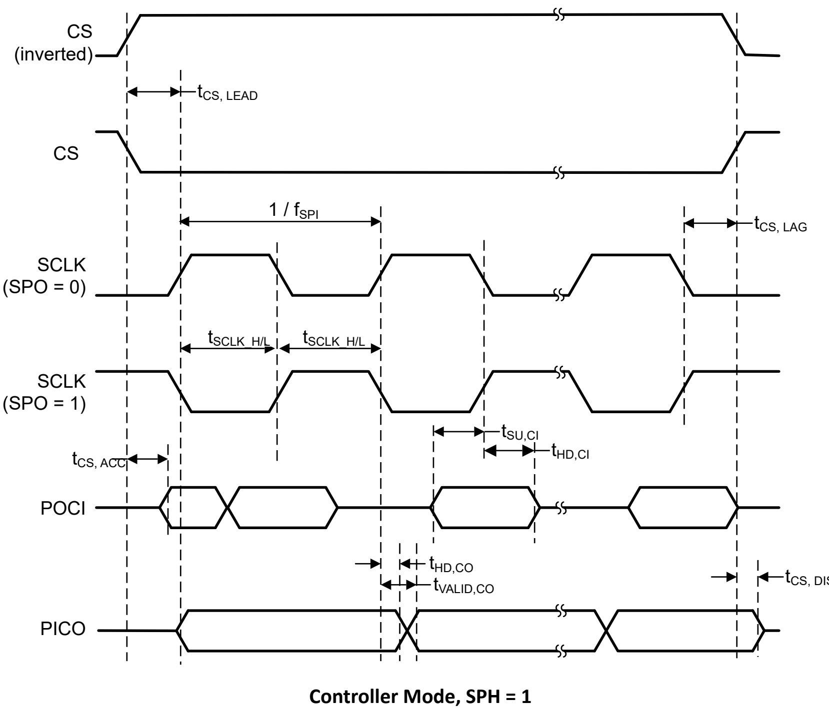

Figure 7-2. SPI Timing Diagram—Controller Mode, SPH = 1

7.22.2.4 SPI Peripheral Mode

Using TI SPI driver, over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{CS.LEAD}$	CS lead-time, CS active to clock		1			SCLK
$t_{CS.LAG}$	CS lag time, Last clock to CS inactive		1			SCLK
$t_{CS.ACC}$	CS access time, CS active to POCI data out	VDDS = 3.3V			35	ns
$t_{CS.ACC}$	CS access time, CS active to POCI data out	VDDS = 1.8V			50	ns
$t_{CS.DIS}$	CS disable time, CS inactive to POCI high inpedance	VDDS = 3.3V			35	ns
$t_{CS.DIS}$	CS disable time, CS inactive to POCI high inpedance	VDDS = 1.8V			50	ns
$t_{SU.PI}$	PICO input data setup time		13			ns
$t_{HD.PI}$	PICO input data hold time		0			ns
$t_{VALID.PO}$	POCI output data valid time(1)	SCLK edge to MISO valid,C_L = 20pF, 3.3V			35	ns
$t_{VALID.PO}$	POCI output data valid time(1)	SCLK edge to MISO valid,C_L = 20pF, 1.8V			50	ns
$t_{HD.PO}$	POCI output data hold time(2)	C_L = 20pF	0			ns

(1) Specifies the time to drive the next valid data to the output after the output changing SCLK clock edge
(2) Specifies how long data on the output is valid after the output changing SCLK clock edge

7.22.2.5 SPI Timing Diagrams—Peripheral Mode

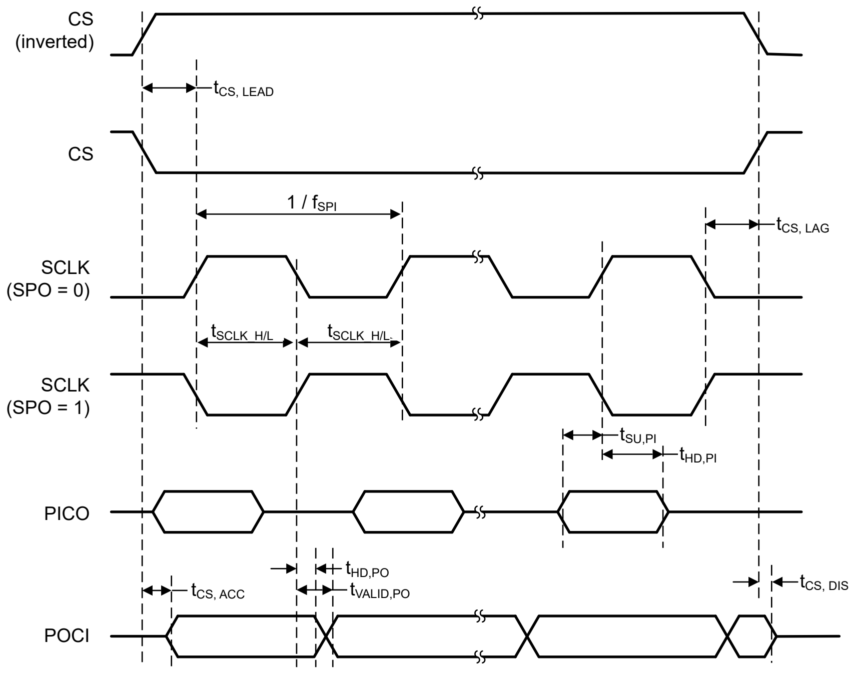

Figure 7-3. SPI Timing Diagram—Peripheral Mode, SPH = 0

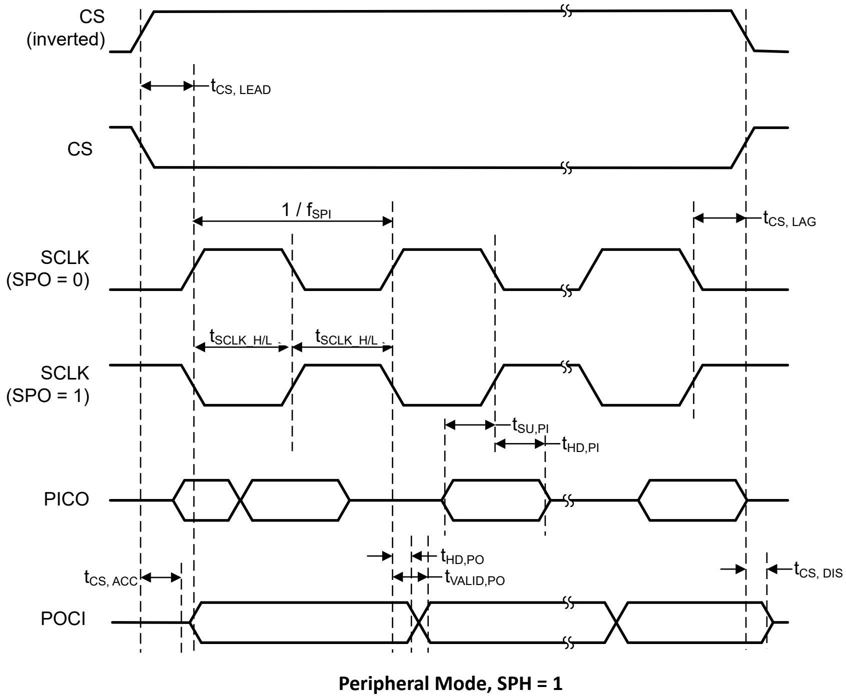

Figure 7-4. SPI Timing Diagram—Peripheral Mode, SPH = 1

7.22.3 I²C

7.22.3.1 I²C Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCL}	SCL clock frequency		0		400	kHz
$t_{HD,STA}$	Hold time (repeated) START	f_{SCL} = 100kHz	4.0			µs
$t_{HD,STA}$	Hold time (repeated) START	f_{SCL} > 100kHz	0.6			µs
$t_{SU,STA}$	Setup time for a repeated START	f_{SCL} = 100kHz	4.7			µs
$t_{SU,STA}$	Setup time for a repeated START	f_{SCL} > 100kHz	0.6			µs
$t_{HD,DAT}$	Data hold time		0			µs
$t_{SU,DAT}$	Data setup time	f_{SCL} = 100kHz	250			ns
$t_{SU,DAT}$	Data setup time	f_{SCL} > 100kHz	100			ns
$t_{SU,STO}$	Setup time for STOP	f_{SCL} = 100kHz	4.0			µs
$t_{SU,STO}$	Setup time for STOP	f_{SCL} > 100kHz	0.6			µs
t_{BUF}	Bus free time between STOP and START conditions	f_{SCL} = 100kHz	4.7			µs
t_{BUF}	Bus free time between STOP and START conditions	f_{SCL} > 100kHz	1.3			µs
t_{SP}	Pulse duration of spikes suppressed by input deglitch filter		50			ns

7.22.3.2 I²C Timing Diagram

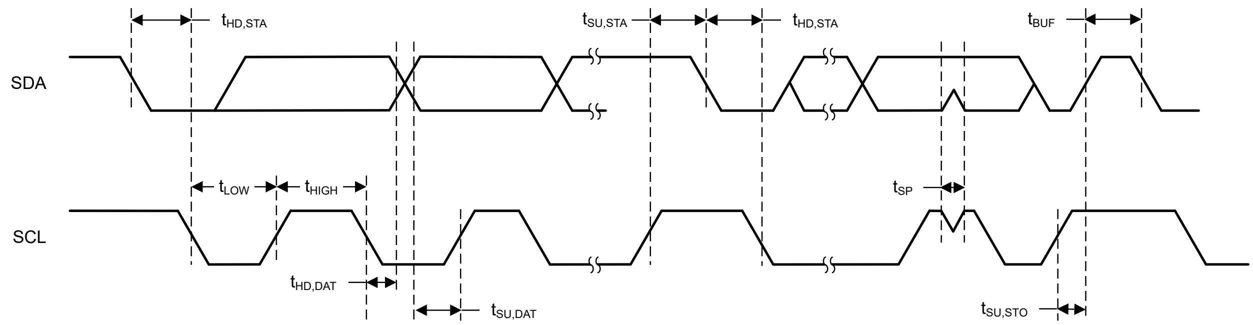

Figure 7-5. I²C Timing Diagram

7.22.4 I²S

7.22.4.1 I²S Controller Mode

Over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{EXTCI}	External clock input frequency				24	MHz
$EXTCI_{DC}$	External clock input duty cycle		40		60	%
f_{MCLK}	MCLK clock output frequency				24	MHz
$MCLK_{DC}$	MCLK clock duty cycle		46		52	%
f_{SCLK}	SCLK clock output frequency	VDDS = 1.71V			3.27	MHz
f_{SCLK}	SCLK clock output frequency	VDDS = 3.8V			6.145	MHz
$SCLK_{DC}$	SCLK clock duty cycle		46		54	%
$t_{WS,valid}$	WS data output valid time (Falling edge of SCLK to WS data valid)		42		49	ns
$t_{SDOUT,valid}$	SD data output valid time (Falling edge of SCLK to SD data valid)		37		62	ns
$t_{SDIN,setup}$	SD data input setup time (before rising edge of SCLK)		9			ns
$t_{SDIN,hold}$	SD data input hold time (after rising edge of SCLK)		5			ns

7.22.4.2 I²S Peripheral Mode

Over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK clock input frequency	VDDS = 1.71V			3.1	MHz
f_{SCLK}	SCLK clock input frequency	VDDS = 3.8V			6.145	MHz
$SCLK_{DC}$	SCLK clock duty cycle	VDDS = 1.71V	35		65	%
$SCLK_{DC}$	SCLK clock duty cycle	VDDS = 3.8V	40		60	%
$t_{SDOUT,valid}$	SD data output valid time (Falling edge of SCLK to SD data valid)		26		47	ns
$t_{WS,setup}$	WS data input setup time (before rising edge of SCLK)		15			ns
$t_{WS,hold}$	WS data input hold time (after rising edge of SCLK)		0			ns
$t_{SDIN,setup}$	SD data input setup time (before rising edge of SCLK)		9			ns

7.22.4.2 I2S Peripheral Mode (continued)

Over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{SDIN,hold}$	SD data input hold time (after rising edge of SCLK)		5			ns

7.22.5 GPIO

7.22.5.1 GPIO DC Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_A = 25°C, V_{DDS} = 1.8V					
GPIO pullup current	Input mode, pullup enabled, Vpad = 0V	39	66	109	µA
GPIO pulldown current	Input mode, pulldown enabled, Vpad = VDDS	10	21	40	µA
GPIO low-to-high input transition, with hysteresis	IH = 1, transition voltage for input read as 0 → 1	0.91	1.11	1.27	V
GPIO high-to-low input transition, with hysteresis	IH = 1, transition voltage for input read as 1 → 0	0.59	0.75	0.91	V
GPIO input hysteresis	IH = 1, difference between 0 → 1 and 1 → 0 points	0.26	0.35	0.44	V
T_A = 25°C, V_{DDS} = 3.0V					
GPIO VOH at 10mA load	high-drive GPIOs only, max drive setting (add MMR bits)	2.47			V
GPIO VOL at 10mA load	high-drive GPIOs only, max drive setting (add MMR bits)			0.25	V
GPIO VOH at 2mA load	standard drive GPIOs	2.52			V
GPIO VOL at 2mA load	standard drive GPIOs			0.20	V
T_A = 25°C, V_{DDS} = 3.8V					
GPIO pullup current	Input mode, pullup enabled, Vpad = 0V	170	262	393	µA
GPIO pulldown current	Input mode, pulldown enabled, Vpad = VDDS	60	110	172	µA
GPIO low-to-high input transition, with hysteresis	IH = 1, transition voltage for input read as 0 → 1	1.76	1.98	2.27	V
GPIO high-to-low input transition, with hysteresis	IH = 1, transition voltage for input read as 1 → 0	1.26	1.52	1.79	V
GPIO input hysteresis	IH = 1, difference between 0 → 1 and 1 → 0 points	0.40	0.47	0.54	V
T_A = 25°C					
VIH	Lowest GPIO input voltage reliably interpreted as a *High*	$0.8 \times V_{DDS}$			V
VIL	Highest GPIO input voltage reliably interpreted as a *Low*			$0.2 \times V_{DDS}$	V

7.22.6 ADC

7.22.6.1 Analog-to-Digital Converter (ADC) Characteristics

T_c = 25°C, V_{DDS} = 3.0V, unless otherwise noted.(1)
Performance numbers require use of offset and gain adjustments in software by TI-provided ADC drivers.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC Power Supply and Input Range Conditions						
$V_{(Ax)}$	Analog input voltage range	All ADC analog input pins Ax	0		VDDS	V
$I_{(ADC)}$ single-ended mode	Operating supply current into VDDS terminal	RES = 0x0 (12Bit mode), Fs = 1.2MSPS, Internal reference OFF (ADC.REFCFG_REFEN = 0), VeREF+ = VDDS		480		µA
		RES = 0x0 (12Bit mode), Fs = 266ksps, Internal reference ON (ADC.REFCFG_REFEN = 1), REFVSEL = 2.5V		365		µA
$C_{I\ GPIO}$	Input capacitance into a single terminal			5	7	pF
$R_{I\ GPIO}$	Input MUX ON-resistance			0.5	1	kΩ
ADC Switching Characteristics						

7.22.6.1 Analog-to-Digital Converter (ADC) Characteristics (continued)

T_c = 25°C, V_{DDS} = 3.0V, unless otherwise noted.(1)
Performance numbers require use of offset and gain adjustments in software by TI-provided ADC drivers.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
F_S ADCREF	ADC sampling frequency when using the internal ADC reference voltage	ADC.REFCFG_REFEN = 1, RES = 0x0 (12Bits), VDDS = 1.71V to VDDSmax			267(2)	ksps
F_S ADCREF	ADC sampling frequency when using the internal ADC reference voltage	ADC.REFCFG_REFEN = 1, RES = 0x1 (10Bits), VDDS = 1.71V to VDDSmax			308(2)	ksps
F_S ADCREF	ADC sampling frequency when using the internal ADC reference voltage	ADC.REFCFG_REFEN = 1, RES = 0x2 (8Bits), VDDS = 1.71V to VDDSmax			400(2)	ksps
F_S EXTREF	ADC sampling frequency when using the external ADC reference voltage	ADC.REFCFG_REFEN = 0, VeREF+ = VDDS, RES = 0x0 (12Bits), VDDS = 1.71V to VDDSmax			1.2(2)	Msps
F_S EXTREF	ADC sampling frequency when using the external ADC reference voltage	ADC.REFCFG_REFEN = 0, VeREF+ = VDDS, RES = 0x1 (10Bits), VDDS = 1.71V to VDDSmax			1.33(2)	Msps
F_S EXTREF	ADC sampling frequency when using the external ADC reference voltage	ADC.REFCFG_REFEN = 0, VeREF+ = VDDS, RES = 0x2 (8Bits), VDDS = 1.71V to VDDSmax			1.6(2)	Msps
$N_{CONVERT}$	Clock cycles for conversion	RES = 0x0 (12Bits)		14		cycles
$N_{CONVERT}$	Clock cycles for conversion	RES = 0x1 (10Bits)		12		cycles
$N_{CONVERT}$	Clock cycles for conversion	RES = 0x2 (8Bits)		9		cycles
t_{Sample}	Sampling time	RES = 0x0 (12-bit), R_S = 25Ω, C_{pext} = 10pF. ±0.5 LSB settling	166.6			ns
$t_{VSUPPLY/3(sample)}$	Sample time required when Vsupply/3 channel is selected		20			µs
ADC Linearity Parameters						
E_I	Integral linearity error (INL) for single-ended inputs	12-bit Mode, V_{R+} = VeREF+ = VDDS, VDDS = 1.71-->3.8		±2		LSB
E_D	Differential linearity error (DNL)	12-bit Mode, V_{R+} = VeREF+ = VDDS, VDDS = 1.71-->3.8		±1		LSB
E_O	Offset error	External reference, V_{R+} = VeREF+ = VDDS, VDDS = 1.71-->3.8	-3		3	mV
E_O	Offset error	Internal reference, V_{R+} = REFVSEL = 2.5V	-3		3	mV
E_G	Gain error	External Reference, V_{R+} = VeREF+ = VDDS , VDD = 1.71-->3.8		±2		LSB
E_G	Gain error	Internal reference, V_{R+} = REFVSEL = 2.5V		±40		LSB
ADC Dynamic Parameters						
ENOB	Effective number of bits	ADC.REFCFG_REFEN = 0, VeREF+ = VDDS = 3.3V, VeREF– = 0V, RES = 0x2 (8-bit)		8		bit
ENOB	Effective number of bits	ADC.REFCFG_REFEN = 0, VeREF+ = VDDS = 3.3V, VeREF– = 0V, RES = 0x1 (10-bit)		9.9		bit
ENOB	Effective number of bits	ADC.REFCFG_REFEN = 0, VeREF+ = VDDS = 3.3V, VeREF– = 0V, RES = 0x0 (12-bit)		11.2		bit
ENOB	Effective number of bits	ADC.REFCFG_REFEN = 1, REFVSEL = {2.5V, 1.4V}, RES = 0x2 (8-bit)		8		bit
ENOB	Effective number of bits	ADC.REFCFG_REFEN = 1, REFVSEL = {2.5V, 1.4V} , RES = 0x1 (10-bit)		9.6		bit
ENOB	Effective number of bits	ADC.REFCFG_REFEN = 1, REFVSEL = {2.5V, 1.4V}, RES = 0x0 (12-bit)		10.4		bit
ENOB	Effective number of bits	VDDS reference, RES = 0x0 (12-bit)		11.2		bit
SINAD	Signal-to-noise and distortion ratio	ADC.REFCFG_REFEN = 0, VeREF+ = VDDS = 3.3V, VeREF– = 0V, RES = 0x0 (12-bit)		69.18		dB
SINAD	Signal-to-noise and distortion ratio	ADC.REFCFG_REFEN = 1, REFVSEL = {2.5V, 1.4V}, RES = 0x0 (12-bit)		64.37		dB
SINAD	Signal-to-noise and distortion ratio	VDDS reference, RES = 0x0 (12-bit)		69.18		dB
ADC External Reference						
EXTREF	Positive external reference voltage input	ADC.REFCFG_REFEN=0, ADC reference sourced from external reference pin (VeREF+)	1.4		VDDS	V
EXTREF	Negative external reference voltage input	ADC.REFCFG_REFEN=0, ADC reference sourced from external reference pin (VeREF–)			0	V
ADC Supply Monitor						

7.22.6.1 Analog-to-Digital Converter (ADC) Characteristics (continued)

T_c = 25°C, V_{DDS} = 3.0V, unless otherwise noted.(1)
Performance numbers require use of offset and gain adjustments in software by TI-provided ADC drivers.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC Internal Input: V_{SUPPLY} / 3 Accuracy	V_{supply} voltage divider accuracy for supply monitoring	ADC input channel: Vsupply monitor	-1.5		1.5	%
ADC Internal Input: $I_{Vsupply / 3}$	V_{supply} voltage divider current consumption	ADC input channel Vsupply monitor. V_{supply}=VDDS=3.3V		10		µA
ADC Internal and VDDS Reference						
VDDSREF	Positive ADC reference voltage	ADC reference sourced from VDDS		VDDS		V
ADCREF	Internal ADC Reference Voltage	ADC.REFCFG_REFEN = 1, REFVSEL = 0, VDDS = 1.71V - VDDSmax		1.4		V
		ADCREF_EN = 1, REFVSEL = 1, VDDS = 2.7V - VDDSmax		2.5		V
I_{ADCREF}	Operating supply current into VDDA terminal with internal reference ON	ADC.REFCFG_REFEN = 1, VDDA = 1.7V to VDDAmax, REFVSEL = {0,1}		80		µA
t_{ON}	Internal ADC Reference Voltage power on-time	ADC.REFCFG_REFEN = 1		2		µs

(1) Using IEEE Std 1241-2010 for terminology and test methods
(2) Measured with 48MHz HFXT

7.22.7 Comparators

7.22.7.1 Low power comparator

T_c = 25°C, V_{DDS} = 3.0V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range		0		V_{DDS}	V
Clock frequency			32		KHz
Voltage divider accuracy	Input voltage range is between VDDS/4 and VDDS×3/4		97%		
Offset	Measured at V_{DDS} / 2 (Errors seen when using two external inputs)		±15		mV
Decision time	Step from –50mV to 50mV		1	3	Clock Cycle
Comparator enable time	COMP_LP disable → enable, VIN+, VIN– from pins, Overdrive ≥ 20mV		80		µs
Current consumption	Including using VDDS/2 as internal reference at VIN– comparator terminal		370		nA

7.22.8 Voltage Glitch Monitor

Over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VGM					
Current consumption from VDDS supply	VGM enabled		60		µA
Turn-on time	From VGM enabled to VGM ready		50		µs

7.23 Typical Characteristics

All measurements in this section are done with Tc = 25°C and VDDS = 3.0V, unless otherwise noted. See Recommended Operating Conditions for device limits. Values exceeding these limits are for reference only.

7.23.1 MCU Current

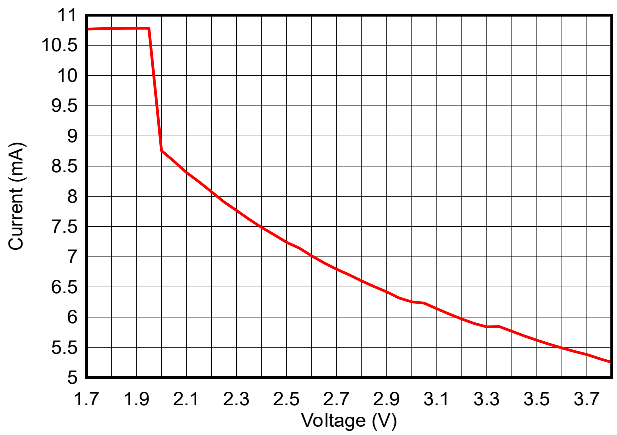

Figure 7-6. Active Mode (MCU) Current vs Supply Voltage (VDDS) (Running CoreMark)

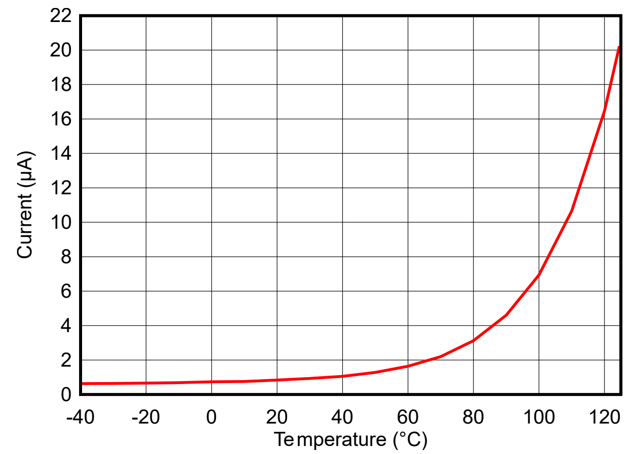

Figure 7-7. Standby Mode (MCU) Current vs Temperature (SRAM and partial register retention, RTC enabled), VDDS = 3.3V

7.23.2 RX Current

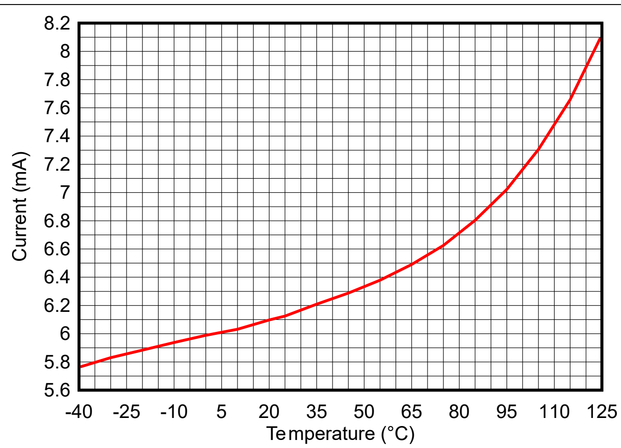

Figure 7-8. RX Current vs Temperature (BLE 1Mbps, 2.44GHz), VDDS = 3.3V

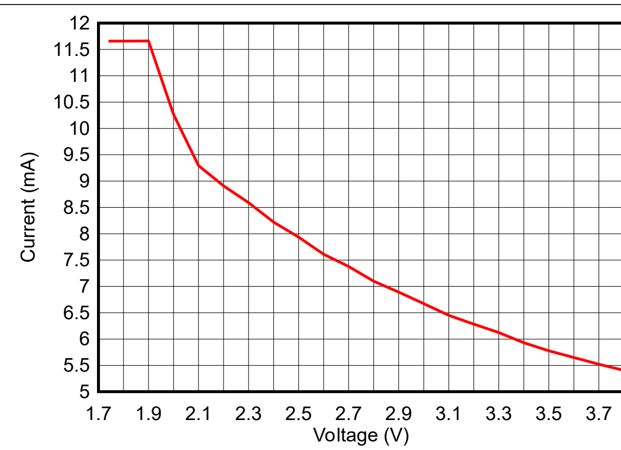

Figure 7-9. RX Current vs Supply Voltage (VDDS) (BLE 1Mbps, 2.44GHz)

7.23.3 TX Current

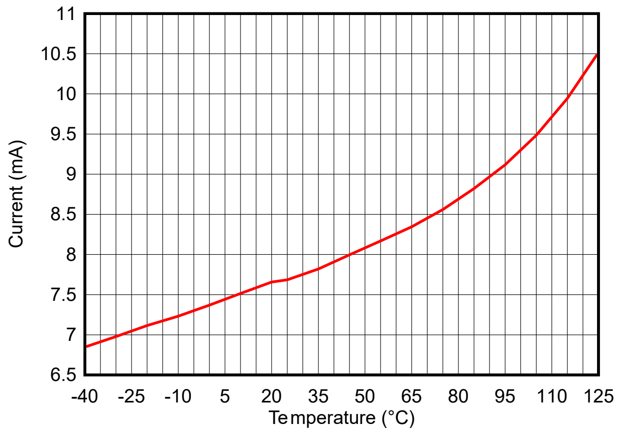

Figure 7-10. TX Current vs Temperature (BLE 1Mbps, 2.44GHz, 0dBm), VDDS = 3.3V

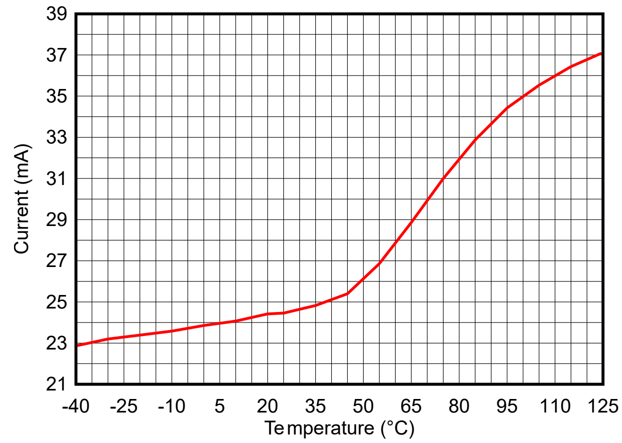

Figure 7-11. TX Current vs Temperature (BLE 1Mbps, 2.44GHz, +10dBm), VDDS = 3.3V

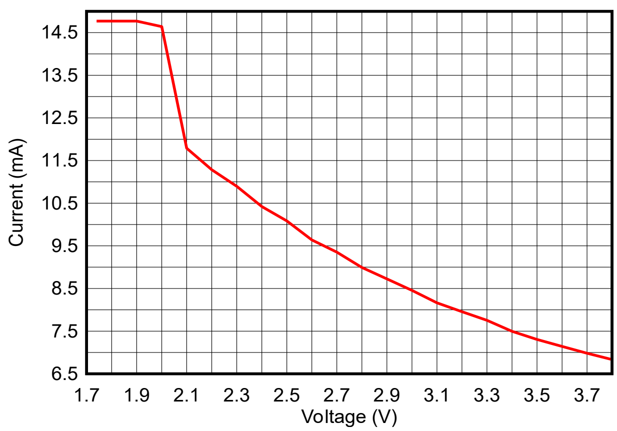

Figure 7-12. TX Current vs Supply Voltage (VDDS) (BLE 1Mbps, 2.44GHz, 0dBm)

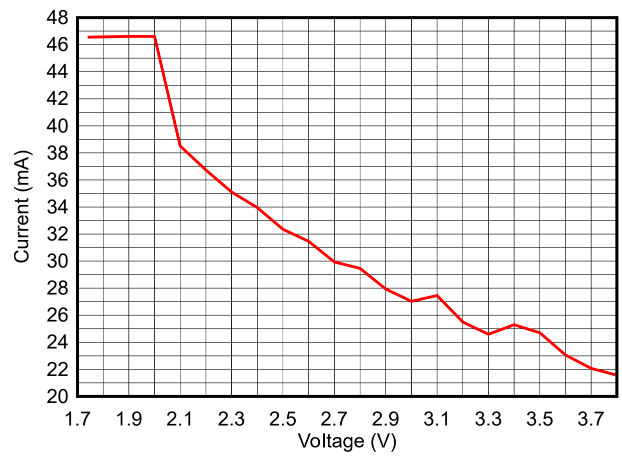

Figure 7-13. TX Current vs Supply Voltage (VDDS) (BLE 1Mbps, 2.44GHz, +10dBm)

Note

The DCDC load support increases with VDDS supply voltage up to a specific supply threshold. Beyond this threshold the load support typically drops before increasing again until the next threshold. For high TX output power settings, the load on VDDR can exceed the DCDC load support and the extra load is supplied by internal GLDO. This manifests as multiple slight peaks on the TX current curve as a function of increasing VDDS supply voltage.

Table 7-1 shows typical TX current and output power for different output power settings.

Table 7-1. Typical TX Current and Output Power (R variant)

2.4GHz, VDDS = 3.3V, DC/DC enabled, Temperature = 25°C (Measured on LP-EM-CC2745R10-Q1)			
txPowerTable Index	**TX Power Setting [dBm] (SmartRF Studio)**	**Typical Output Power [dBm]**	**Typical Current Consumption [mA]**
1	10	10	24.5
2	9	9	22.3
3	8	7.9	20.3
4	7.5	7.3	19.5
5	7	6.8	18.8
6	6.5	6.25	18
7	6	5.9	17.7
8	5.5	5.4	17.2
9	5	4.9	10.8
10	4.5	4.6	10
11	4	4.1	9.7
12	3.5	3.6	9.3
13	3	3.2	9.0
14	2.5	2.6	8.7
15	2	2.1	8.7
16	1.5	1.7	8.5
17	1	1.1	8.2
18	0.5	0.65	8.0
19	0	0.1	7.7
20	–4	–3.9	5.8
21	–8	–7.9	5.3
22	–12	–11.8	5.0
23	–16	–15.9	4.8
24	–20	–20	4.7

Table 7-2. Typical TX Current and Output Power (P variant)

2.4GHz, VDDS = 3.3V, DC/DC enabled, Temperature = 25°C (Measured on LP-EM-CC2755P10)			
txPowerTable Index	**TX Power Setting [dBm] (SmartRF Studio)**	**Typical Output Power [dBm]**	**Typical Current Consumption [mA]**
1	20	19.8	132
2	19	18.8	110
3	18	18.2	101
4	17	17.2	89
5	16	16	75
6	15	15.2	71
7	14	14.1	62
8	13	13	56
9	12	12.4	52
10	11	10.9	34
11	10	9.9	28.2
12	9	8.9	25.3
13	8	8	23.5
14	7	6.9	21.6
15	6	5.9	20
16	5	4.9	18.6
17	4	4.2	10
18	3	3.4	9.7
19	2	2.4	9.1
20	2	1.4	9.0
21	0	0.5	8.6
22	–4	-3.6	6.4
23	–8	-7.3	6.2
24	–12	-11.5	5.6
25	–16	-15.2	5.5
26	–20	-19.3	5.2

7.23.4 RX Performance

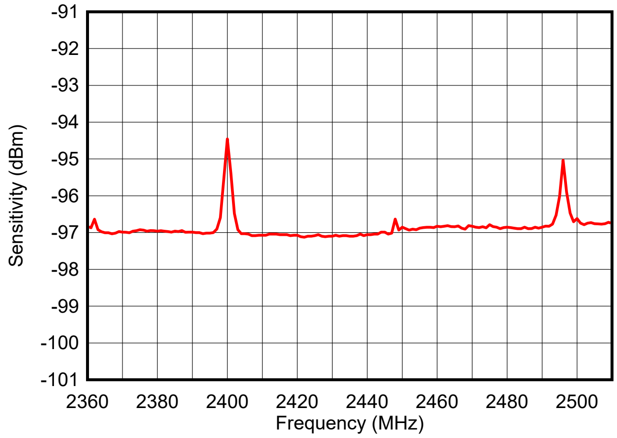

Figure 7-14. Sensitivity vs Frequency (BLE 1Mbps)

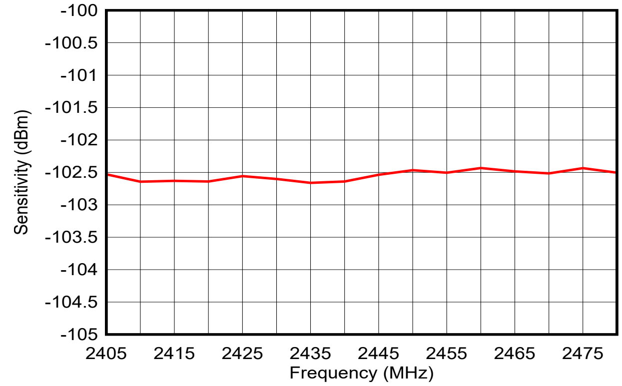

Figure 7-15. Sensitivity vs Frequency (IEEE 802.15.4 PHY)

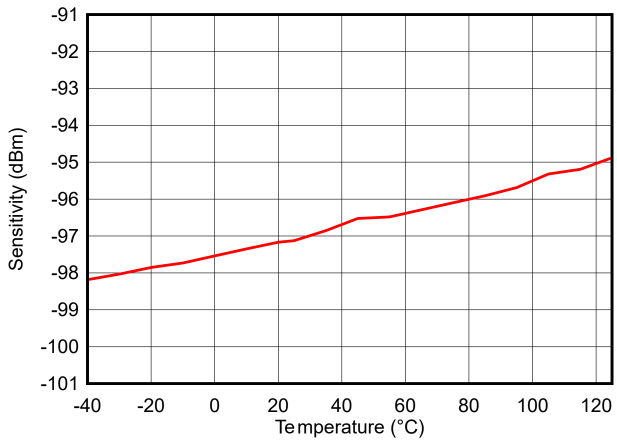

Figure 7-16. Sensitivity vs Temperature (BLE 1Mbps, 2.44GHz)

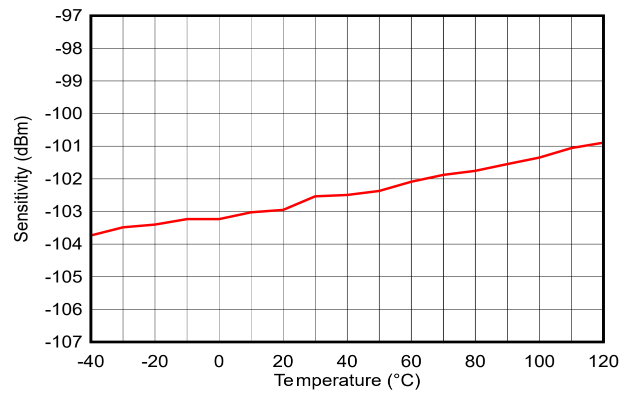

Figure 7-17. Sensitivity vs Temperature (IEEE 802.15.4 PHY)

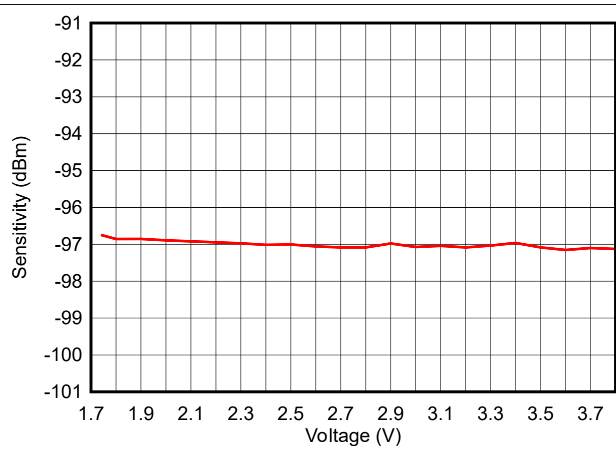

Figure 7-18. Sensitivity vs Supply Voltage (VDDS) (BLE 1Mbps, 2.44GHz)

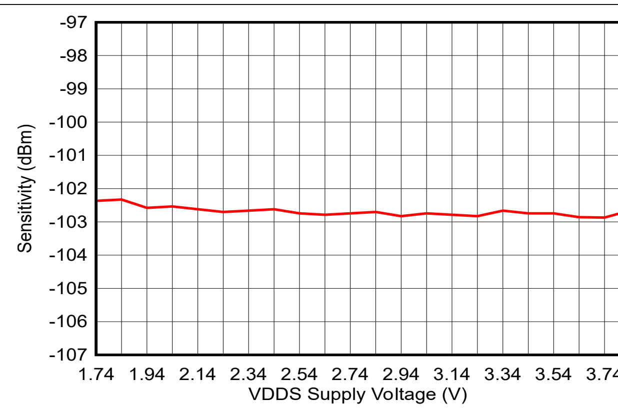

Figure 7-19. Sensitivity vs VDDS (IEEE 802.15.4 PHY)

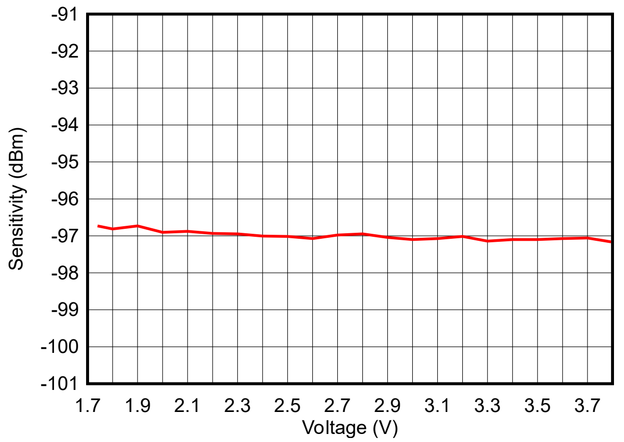

Figure 7-20. Sensitivity vs Supply Voltage (VDDS) (BLE 1Mbps, 2.44GHz, DC/DC Disabled)

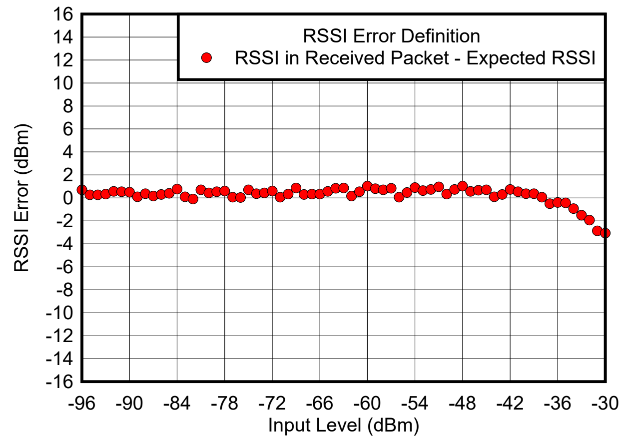

Figure 7-21. RSSI Error vs Input Level (dBm)

7.23.5 TX Performance

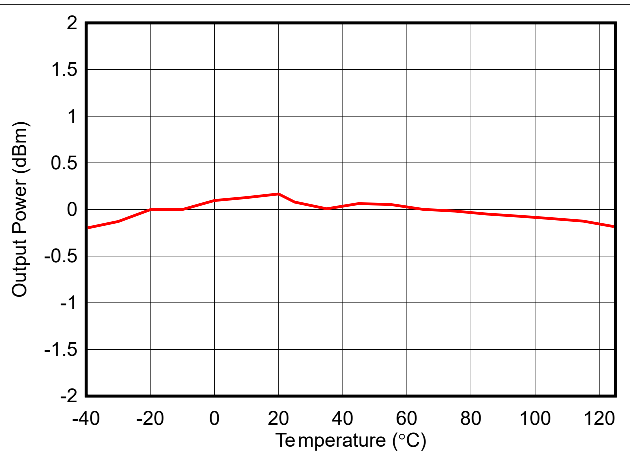

Figure 7-22. Output Power vs Temperature (BLE 1Mbps, 2.44GHz, 0dBm)

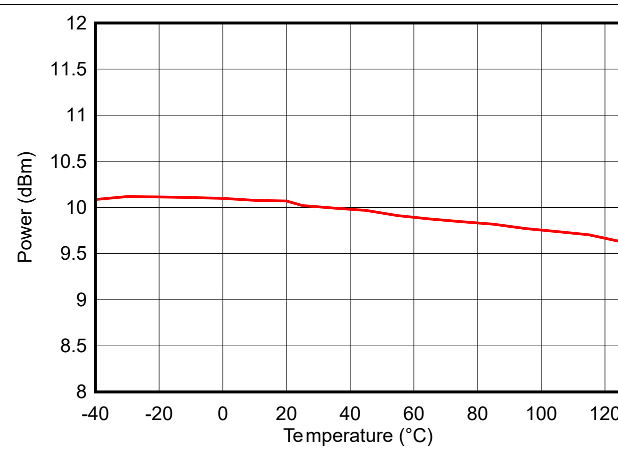

Figure 7-23. Output Power vs Temperature (BLE 1Mbps, 2.44GHz, +10dBm)

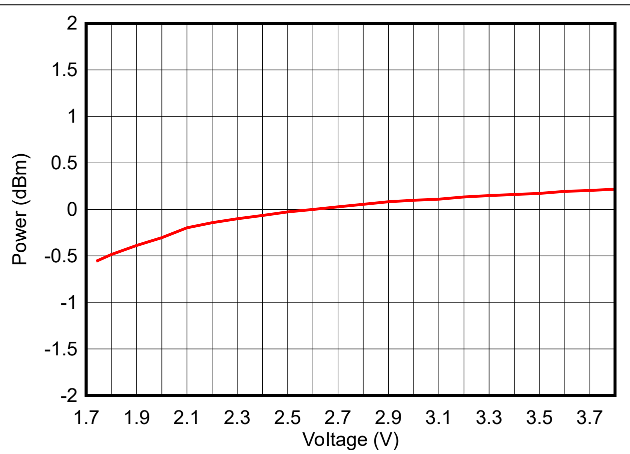

Figure 7-24. Output Power vs Supply Voltage (VDDS) (BLE 1Mbps, 2.44GHz, 0dBm)

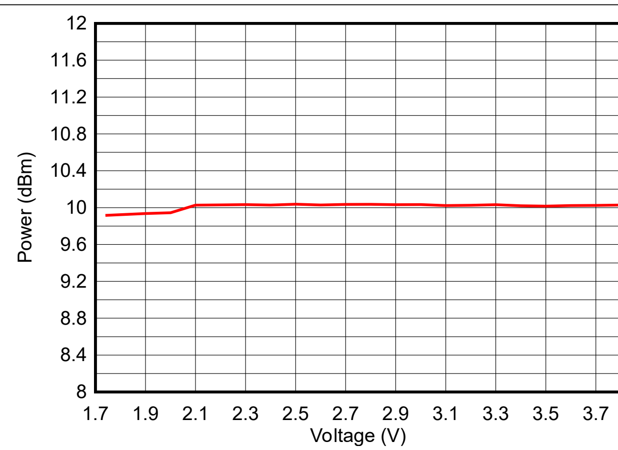

Figure 7-25. Ouput Power vs Supply Voltage (VDDS) (BLE 1Mbps, 2.44GHz, +10dBm)

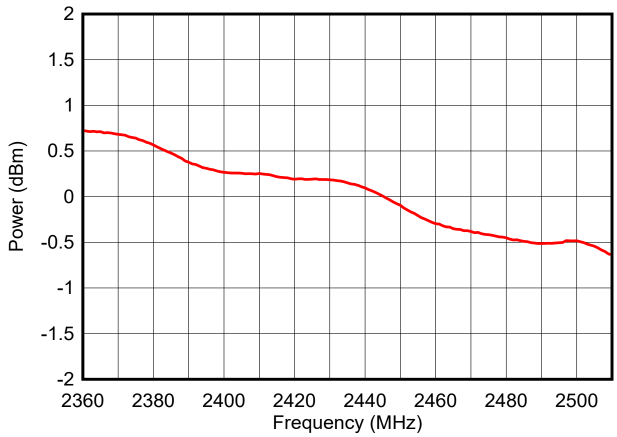

Figure 7-26. Output Power vs Frequency (BLE 1Mbps, 0dBm)

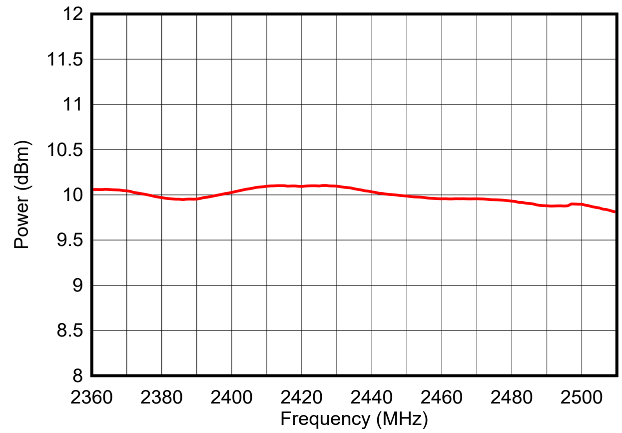

Figure 7-27. Output Power vs Frequency (BLE 1Mbps, +10dBm)

7.23.6 ADC Performance

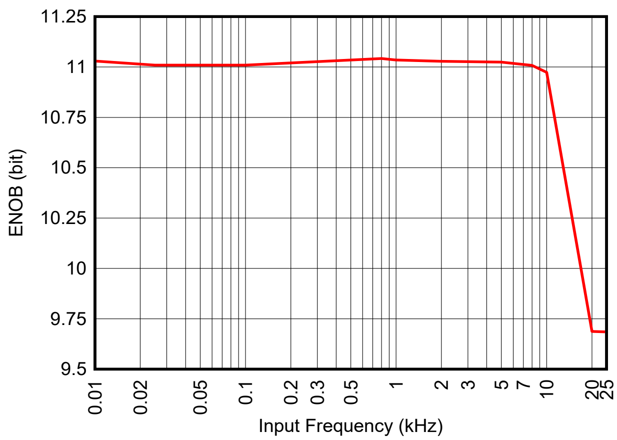

Figure 7-28. ENOB vs Input Frequency (Internal Reference)

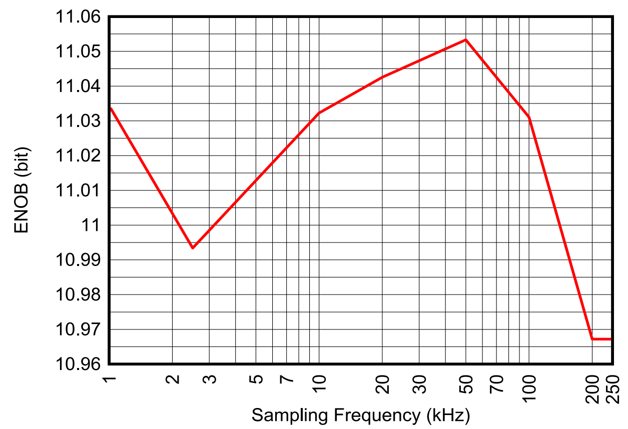

Figure 7-29. ENOB vs Sampling Frequency (V_{in}=3V Ramp Wave, Internal Reference, F_{in}=F_s/10)

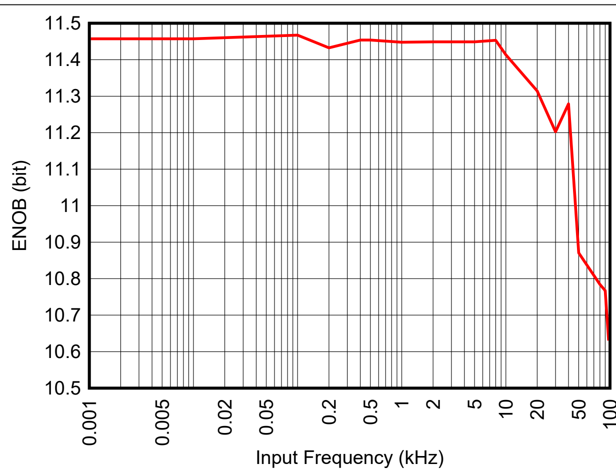

Figure 7-30. ENOB vs Input Freqency (External Reference = 3.0V)

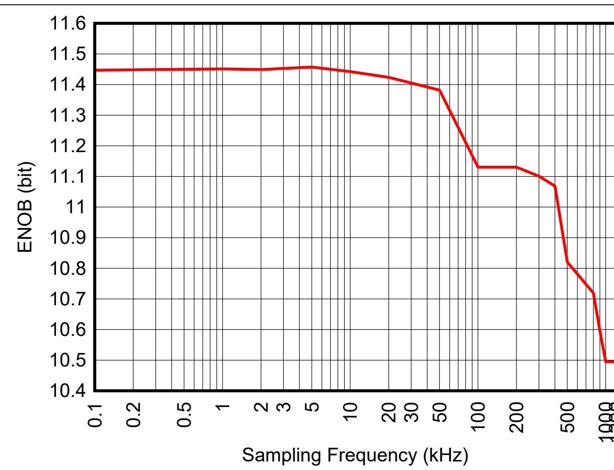

Figure 7-31. ENOB vs Sampling Frequency (V_{in}=3V Ramp Wave, Internal Reference, 200ksps)

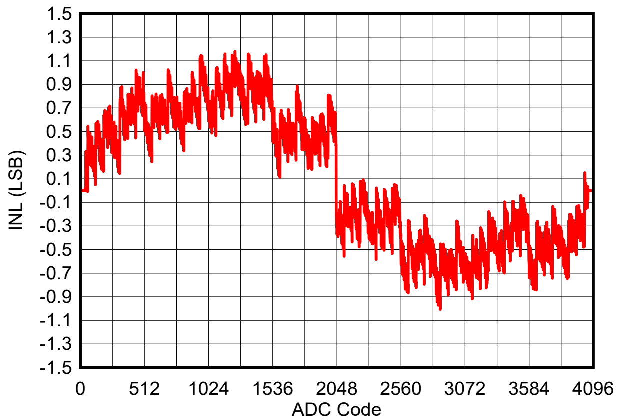

Figure 7-32. INL vs ADC Code (V_{in}=3V Ramp Wave, Internal Reference, 200ksps)

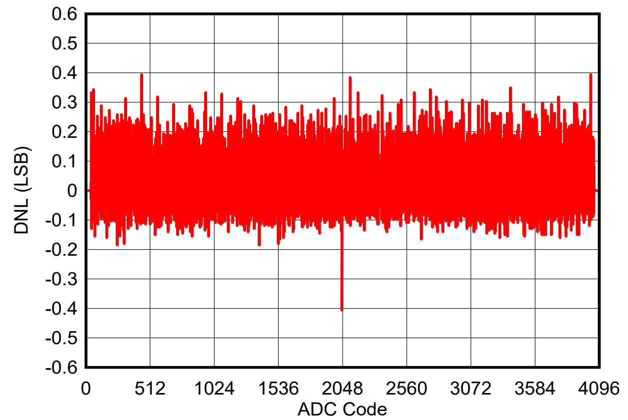

Figure 7-33. DNL vs ADC Code (V_{in}=3V Sine Wave, Internal Reference, 200ksps)

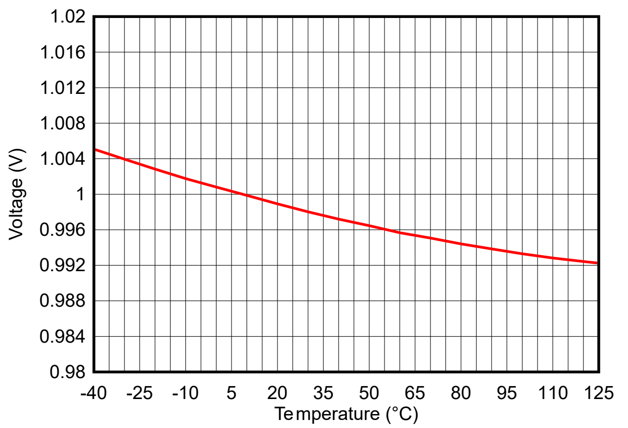

Figure 7-34. ADC Accuracy vs Temperature (V_{in}=1V, Internal Reference, 200ksps)

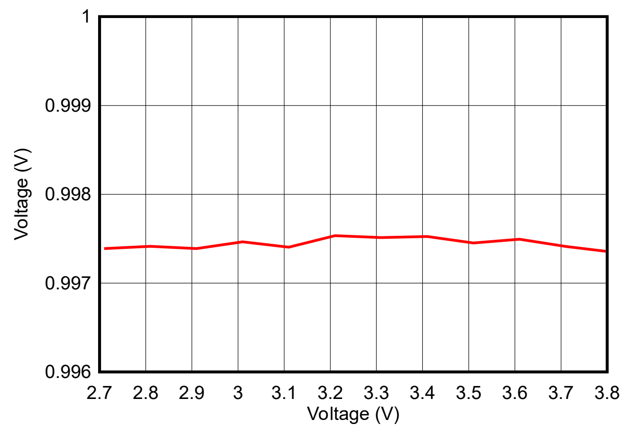

Figure 7-35. ADC Accuracy vs Supply Voltage (V_{in}=1V, Internal Reference, 200ksps)

8 Detailed Description

8.1 Overview

Section 4 shows the core modules of the CC2755 devices.

8.2 System CPU

The CC27xx SimpleLink™ Wireless MCU contains an Arm® Cortex®-M33 system CPU, which runs the application, the protocol stacks, and the radio. The Cortex-M33 processor achieves an optimal blend of real-time determinism, energy efficiency, software productivity, and system security. The 32-bit processor core is built with the mainline extension Armv8-M architecture designed for low-latency processing. The Cortex-M33 processor offers multiple benefits to developers, including:

- Real-time deterministic, high-performance interrupt handling with 32-bit performance
- Security foundation with the addition of TrustZone-M technology
- Low-power processing with ease of software development

The Cortex-M33 processor offers multiple benefits to developers, making it ideal for automotive, IoT, and embedded applications that require efficient security or digital signal control. Some of the features include:

- Armv8-M architecture with mainline extension
- Thumb/Thumb-2 subset instruction support
- 3-stage pipeline
- Software security:
  - TrustZone-M for Armv8-M, with Security Attribution Unit (SAU) of up to eight regions
  - Stack limit boundaries and checking
- DSP extension: including all the V8.1-M DSP/SIMD instructions
- Floating Point Unit (FPU): single precision floating point unit, IEEE 754 compliant
- Memory Protection Unit (MPU) with eight regions for the secure state (MPU_S) and eight regions for the non-secure state (MPU_NS)
- 24-bit SysTick timer for each security domain
- Integrated Nested Vectored Interrupt Controller (NVIC) supporting Non-Maskable Interrupt (NMI)
- Low-power sleep modes
  - Arm® SLEEP maps to the device's idle power mode
  - Arm® DEEPSLEEP maps to the device's standby power mode
- Serial Wire Debug ports with up to eight breakpoints and four watchpoints
- Data Watchpoint and Trace (DWT), and Instrumentation Trace Macrocell (ITM)
- 96MHz operation on CC27xx with 1.41DMIPS/MHz and 3.85 CoreMark®) / MHz (running CoreMark®) from flash) performance
- Arm® CDE (Custom Data Extension) instruction support for machine learning acceleration

Additionally, the CC27xx devices are compatible with all Arm® tools and software.

8.3 Radio (RF Core)

The low-power RF Core (LRF) implements a high-performance and highly flexible RF subsystem containing RF and baseband circuitry in addition to a software-defined digital radio (LRFD). LRFD provides a high-level, command-based API to the main CPU and handles all of the timing-critical and low-level details of many different radio PHYs. Several signals are also available to control external circuitry, such as RF switches or range extenders, autonomously.

The modem is highly configurable and has the flexibility to support future standards. It is not programmable by customers but is instead loaded with precompiled images provided in the radio driver in the SimpleLink™ Low Power F3 software development kit (SDK). This mechanism allows the radio platform to be updated for support of future versions of standards with over-the-air (OTA) updates while still using the same silicon. LRFD stores the code images in the RF SRAM and does not make use of any ROM memory; thus, image loading from flash only occurs once after boot, and no patching is required when exiting power modes.

8.3.1 Bluetooth® Low Energy

The RF Core offers full support for Bluetooth® Low Energy, including the high-speed 2Mbps physical layer and the 500kbps and 125kbps long-range PHYs (Coded PHY) through the TI-provided Bluetooth® stack or through a standardized host controller interface.

The RF Core and the TI-provided Bluetooth® stack support the Bluetooth® 6 Channel Sounding feature to enable a new high-accuracy and low-cost distance measurement method between two Bluetooth® LE devices.

8.3.2 802.15.4 (Thread, Zigbee, Matter)

Through a dedicated IEEE radio API, the RF Core supports the 2.4GHz IEEE 802.15.4-2011 physical layer (2 Mchips per second Offset-QPSK with DSSS 1:8), used in Thread and Zigbee protocols. TI also provides royalty-free protocol stacks for Thread and Zigbee, enabling a robust end-to-end solution.

8.4 Memory

The CC27xx devices support up to 1MB of nonvolatile (Flash) memory to provide storage for code and data. The flash memory is in-system programmable and erasable. Dual flash banks (up to 512kB each) are supported to enable reading/execution from one flash bank when erasing/writing to the other flash bank. Special flash memory sectors contain Customer Configuration (CCFG) and Security Configuration (SCFG) sections that are used by system ROM bootcode and TI-provided drivers to configure the device. The CCFG and SCFG configurations are generated using the device configuration Sysconfig tool.

Up to 162KB of ultra-low leakage system static RAM (SRAM) can be used for both storage of data and execution of code. Retention of SRAM contents in Standby power mode is enabled by default and included in Standby mode power consumption numbers. Parity checking for detecting bit errors in memory is an optional feature that is built-in to reduce chip-level soft errors and increase reliability. With the SRAM parity enabled, the SRAM size is limited to 144KB.

Upon regular device boot, the user application can use hardware mechanisms for SRAM clearing. To improve code execution speed and reduce power consumption when executing code from nonvolatile memory, a 4-way set-associative 8KB cache is enabled by default to cache and prefetch instructions read by the system CPU.

The system ROM includes device bootcode firmware that is the first piece of code that executes upon device power-up or reset. The system ROM handles the execution of device start-up routines, initial device trimming, and device security features, including secure boot operations and device lifecycle management. The system ROM also contains a serial (SPI and UART) bootloader that can be used for the initial programming of the device. The system ROM firmware includes open-source MCUBoot software that is licensed under APACHE-2.0. See the corresponding license terms and notice information in Software License and Notice section. Some system ROM firmware is licensed under the BSD-3-clause license.

8.5 Hardware Security Module (HSM)

The CC27xx devices have an integrated hardware security module (HSM) supporting an isolated environment for cryptographic, key management, secure counters, and random number generation operations. Selected algorithms are protected from differential power analysis (DPA) side channel attacks. Together with a large selection of open-source cryptography libraries provided with the Software Development Kit (SDK), the system enables secure and future-proof automotive and IoT applications to be easily built on the platform.

The following cryptographic functions using energy-efficient accelerators and RNG functions are accelerated by the HSM:

- Key Agreement Schemes
  - Elliptic Curve Diffie-Hellman with static or ephemeral keys (ECDH and ECDHE)
  - Diffie Hellman with static or ephemeral keys (DH and DHE)
- Signature Processing
  - Elliptic Curve Diffie-Hellman Digital Signature Algorithm (ECDSA)
  - Edwards-Curve Digital Signature Algorithm (EdDSA)
  - RSA PKCS #1 v1.5
  - RSA PSS
- Message Authentication Codes
  - AES CBC-MAC
  - AES CMAC
  - HMAC with SHA2-224, SHA2-256, SHA2-384, and SHA2-512
- Block Cipher Modes of Operation
  - AES CCM and AES CCM* (CCM-Star)
  - AES GCM
  - AES ECB
  - AES CBC
  - AES CTR
- Hash Algorithms
  - SHA2-224
  - SHA2-256
  - SHA2-384
  - SHA2-512
- Random Number Generation
  - TRNG (True Random Number Generator)
  - AES-CTR DRBG (Deterministic Random Bit Generator)

Cryptographic key sizes and types include:

- Advanced Encryption Standard (AES) key sizes of 128, 192, and 256 bits
- RSA key sizes up to 3072 bits (Sign and Verify supported), and up to 4096 bits (verify only)
- Diffie-Hellman key sizes of 2048 bits and 3072 bits
- Elliptic Curve Support
  - Short Weierstrass
    - NIST-P224 (secp224r1), NIST-P256 (secp256r1), NIST-P384 (secp384r1), NIST-P521 (secp521r1)
    - Brainpool-256R1, Brainpool-384R1, Brainpool-512R1
  - Montgomery
    - Curve25519
  - Twisted Edwards form
    - Ed25519

DPA countermeasures are implemented for:

- AES operations
- ECDSA operations

The HSM executes the HSM firmware from a secured flash region. 96KB of the device flash memory is reserved for the HSM firmware. The HSM firmware is verified by the HSM ROM during the HSM boot process. Secure firmware update of the HSM firmware image on-chip is handled by the system ROM bootcode and the HSM ROM.

The HSM also has a data RAM region that is not accessible to the rest of the system (system CPU, DMA, debug access, and so on). The data RAM region is retained in low-power modes, supporting quick power-up of the HSM and retention of key material. In addition to the storage of key material in data RAM, the HSM supports importing and exporting wrapped key material (NIST SP800-38F) with a key unique to the device, known as a HW Unique Key (HUK). This allows keys to be securely stored anywhere in the system's nonvolatile (Flash) memory.

The HSM is accessible to the application running on the system CPU in a controlled manner via the HSM mailbox interface. The HSM is a bus controller in the device and can access the system memory directly, enabling better efficiency for moving data during cryptographic operations.

The SimpleLink Low Power F3 software development kit (SDK) includes the encrypted and authenticated HSM firmware needed to be programmed on-chip for the HSM operation and drivers for all HSM functions.

8.6 Cryptography

The CC27xx devices also integrate LAES, an AES-128 cryptography hardware accelerator (outside the HSM), to support latency-critical link-layer encryption/decryption operations prescribed by the wireless protocols. It also has the benefit of being lower power and improves the availability and responsiveness of the system because the cryptography operations run in a background hardware thread. The AES hardware accelerator supports the following block cipher modes and message authentication codes:

- AES ECB encrypt-only
- AES CBC encrypt-only
- AES CTR encrypt/decrypt
- AES CBC-MAC
- AEC CCM (uses a combination of CTR + CBC-MAC hardware via software drivers)

Software implementation of AES GCM cipher mode using LAES for low-level cryptographic operations is supported. The AES hardware accelerator can be fed with plaintext/ciphertext from either the CPU or using DMA. Sustained throughput of one 16-byte ECB block per 23 cycles is possible, corresponding to > 30Mbps.

8.7 Timers

A large selection of timers is available as part of the CC27xx devices. These timers are:

Real-Time Clock (RTC)

The RTC is a 67-bit, 2-channel timer running on the LFCLK system clock. The RTC is active in STANDBY and ACTIVE power states. Upon asynchronous device resets (that is, reset pin, exit from shutdown, LF clock loss, and so on), the RTC is reset. However, upon internally generated synchronous device resets (for example, WDT, debug reset, system reset request, and so on), the RTC is not reset.

The RTC accumulates the time elapsed since its last reset on each LFCLK. It is also possible to update the RTC value as part of the RTC configuration to match a different time base. The RTC counter is incremented by LFCLK at a rate between 30kHz and 34kHz, depending on the LF clock source. LFINC indicates the period of LFCLK in µs with an additional granularity of 16 fractional bits and is used to increment time in the RTC. Hardware measurement circuitry can automatically measure the LFCLK period whenever HFXT is running and update LFINC.

The counter can be read from two 32-bit registers. RTC.TIME8U has a range of approximately 9.5 hours with an LSB representing 8 microseconds. RTC.TIME524M has a range of approximately 71.4 years with an LSB representing 524 milliseconds.

There is hardware synchronization between the system timer (SYSTIM) and the RTC so that the multichannel and higher resolution SYSTIM remain in synchronization with the RTC's time base.

The RTC has two channels: one compare channel and one capture channel, which is capable of waking the device out of the standby power state. The RTC compare channel is typically used only by system software and only during the standby power state.

System Timer (SYSTIM)

The SYSTIM is a 34-bit, 6-channel wrap-around timer with a per-channel selectable 32b time slice with either a 1µs resolution and 1h11m35s range or 250ns resolution and 17m54s range. One channel is reserved for system software, three channels are reserved for radio software, and two channels are freely available to user applications. All user-available channels support both capture and single-shot compare (posting an event) operations.

For software convenience, a hardware synchronization mechanism automatically ensures that the RTC and SYSTIM share a common time base. Another software convenience feature is that SYSTIM qualifies any submitted compare values so that the timer channel will immediately trigger if the submitted event is in the immediate past (4.294s with 1µs resolution and 1.049s with 250ns resolution).

General Purpose Timers (LGPT)

The CC27xx devices provide four LGPTs with 3 × 16-bit timers and 1 × 32-bit timers, all running on up to 48MHz. The LGPTs support a wide range of features such as:

- Three capture/compare channels
- One-shot or periodic counting
- Pulse width modulation (PWM)
- Time counting between edges and edge counting
- Input filter implemented on each of the channels for all timers
- IR generation feature using Timer-0 and Timer-1
- Dead band feature available on Timer-1

The timer capture/compare and PWM signals are connected to IOs through the IO controller module (IOC), and the internal timer event connections to CPU, DMA, and other peripherals are through the event fabric, which allows the timers to interact with signals such as GPIO inputs, other timers, DMA, and ADC. Two LGPTs support quadrature decoder mode to enable buffered decoding of quadrature-encoded sensor signals. The LGPTs are available in device Active and Idle power modes.

Table 8-1. Timer Comparison

CC27xx GP TIMER FEATURE	TIMER 0	TIMER 1	TIMER 2	TIMER 3
Counter Width	16-bit	16-bit	16-bit	32-bit
Quadrature Decoder	Yes	No	Yes	No
Park Mode on Fault	No	Yes	No	No
Programmable Deadband Insertion	No	Yes	No	No

Watchdog Timer

The watchdog timer is used to regain control if the system operates incorrectly due to software errors. Upon counter expiry, the watchdog timer resets the device when periodic monitoring of the system components and tasks fails to verify proper functionality. The watchdog timer runs on a 32kHz clock rate and operates in device active, idle, and standby modes, and cannot be stopped once enabled.

8.8 Algorithm Processing Unit (APU)

The APU is a generic mathematical acceleration module that operates with single-precision floating-point numbers (IEEE 754 format) and is optimized to work with complex numbers. The APU runs at 96MHz, operates autonomously from the main CPU in the system, and can be used to offload numerically intensive operations. This module handles efficient vector (and matrix) operations and sustains one complex Multiply-and-Add operation per clock cycle. These operations are extensively used in advanced post-processing algorithms needed for accurate phase-based distance estimation using the Bluetooth® LE Channel Sounding mechanism; thereby, optimizing the overall channel-sounding-based distance estimation latency and energy efficiency.

The APU has 8KB of local data memory (separate from the system RAM) where the application can read/write data. The APU incorporates a programmable core to handle advanced APIs developed for the APU hardware accelerator submodules. The SimpleLink™ Low Power F3 software development kit (SDK) includes the APU APIs that are executed by the APU programmable core within RAM-based local program memory (separate from the system RAM and VCE data RAM).

The user application handles chain-calling the different APU APIs and moving data in/out of the APU local data memory. The SimpleLink™ Low Power F3 software development kit (SDK) supports SW drivers and examples to enable APU operations.

8.9 Serial Peripherals and I/O

The CC27xx devices provide 2xUART, 2xSPI, 1xI2C, and 1xI2S serial peripherals.

The UART module implements universal asynchronous receiver and transmitter functions. They support flexible baud-rate generation up to a maximum of 3Mbps and IRDA SIR mode of operation.

The SPI module supports the SPI controller and peripherals up to 12MHz with configurable phase and polarity.

The I^2C module communicates with devices compatible with the I^2C standard. The I^2C interface can handle 100kHz and 400kHz operation and can serve as both controller and target.

The I^2S interface handles digital audio and can also interface with pulse-density modulation microphones (PDM).

The I/O controller (IOC) controls the digital I/O pins and contains multiplexer circuitry to allow a set of peripherals to be assigned to I/O pins in a fixed manner over DIOs. All digital I/Os are interrupt and wake-up capable, have a programmable pullup and pulldown function, and can generate an interrupt on a negative or positive edge (configurable). When configured as an output, pins can function as either push-pull, open-drain, or open-source.

Some GPIOs have high-drive capabilities, which are marked in bold in RHA (6mm × 6mm) Pinout, 0.5mm Pitch (Top View).

VDDIO split rail I/O supply enables using a different I/O supply rail compared to the main VDDS supply rail. This enables applications to interface with other system components at a different voltage level compared to the main VDDS power supply level. GPIOs supplied by VDDIO and VDDS supplies are listed in orange or blue, respectively, in RHA (6mm × 6mm) Pinout, 0.5mm Pitch (Top View). The voltage rails supplied on VDDS and VDDIO pins can ramp up and down in any order, independent of each other, and any combination of VDDS and VDDIO supplies being unpowered can be supported indefinitely. This simplifies the system-level power supply design, where it is not needed to control the availability or ramp-up/down sequence of these supplies at the VDDIO and VDDS pins.

For more information, see the *CC27xx SimpleLink™ Wireless MCU Technical Reference Manual*.

8.10 Battery and Temperature Monitor

A combined temperature and battery voltage monitor are available in the CC27xx devices. The battery and temperature monitor allow an application to continuously monitor on-chip temperature and supply voltage and respond to changes in environmental conditions as needed. The module contains window comparators to interrupt the system CPU when the temperature or supply voltage goes outside defined windows. These events can also be used to wake up the device from Standby mode through the Always-On (AON) event fabric.

8.11 Voltage Glitch Monitor (VGM)

The CC27xx devices support the VGM on-chip to mitigate security risks from low-cost and low-effort physical non-invasive fault attacks.

The VGM is enabled by default during device boot time operations. After the device boot operations, the VGM can be kept enabled or optionally disabled during device runtime operations based on application security needs.

8.12 µDMA

The device includes a direct memory access (µDMA) controller. The µDMA controller provides a way to offload data-transfer tasks from the system CPU, thus allowing for more efficient use of the processor and the available bus bandwidth. The µDMA controller can perform transfers between memory and memory or between memory and peripherals. The µDMA controller supports triggers from the various on-chip peripherals and can be programmed to automatically perform transfers between peripherals and memory when the peripheral is ready to transfer more data.

For applications using TrustZone-M, upon device bootup, the µDMA is configured as a secure peripheral by default and can be configured as a non-secure peripheral by the application. The µDMA channels cannot individually be configured as secure or non-secure peripherals, and so, the application is required to select at compile time if the SDK shall configure the µDMA controller as a secure or non-secure peripheral. The SimpleLink Low Power F3 SDK µDMA drivers support using the µDMA as a non-secure peripheral for application operations.

Some features of the µDMA controller include the following (this is not an exhaustive list):

- Channel operation of up to 12 channels, with 8 channels having a dedicated peripheral interface (multiplexed) and 4 channels having the ability to be triggered through configurable events. Transfer modes: memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral
- Data sizes of 8, 16, and 32 bits
- Ping-pong mode for continuous streaming of data

8.13 Debug

On-chip debugging is supported through the serial wire debug (SWD) interface, which is an Arm® bi-directional 2-wire protocol that communicates with the SWD controller and enables complete debug functionality. SWD is fully compatible with the Texas Instruments XDS family of debug probes. The Cortex M33 core supports advanced debugging features, including Data Watchpoint and Trace unit (DWT), which supports watchpoints and system profiling for the CM33 processor. The Cortex M33 core also supports Instrumentation Trace Macrocell (ITM), which supports print-style debugging to trace operating system (OS) and application events and provides diagnostic system information.

8.14 Power Management

To minimize power consumption, the CC27xx devices support multiple power modes and power management features (see Table 8-2).

Table 8-2. Power Modes

MODE	SOFTWARE CONFIGURABLE POWER MODES (1)				RESET PIN HELD
	ACTIVE	IDLE	STANDBY	SHUTDOWN	
CPU	Active	Off	Off	Off	Off
Flash	On	Available	Off	Off	Off
SRAM	On	On	Retention	Off	Off
Radio	Available	Available	Off	Off	Off
Supply System	On	On	Duty Cycled	Off	Off
CPU register retention	Full	Full	Full (2)	No	No
SRAM retention	Full	Full	Full	Off	Off
96 MHz high-speed clock (HFCLK)	HFOSC (3)	HFOSC (3)	Duty Cycled (4)	Off	Off
80/90/98 MHz Auxiliary Frequency Oscillator (AFOSC)	AFOSC	AFOSC	Off (5)	Off	Off
32 kHz low-speed clock (LFCLK)	LFXT or LFOSC	LFXT or LFOSC	LFXT or LFOSC	Off	Off
Peripherals	Available	Available	IOC, BATMON, RTC, LPCOMP	Off	Off
Wake-up on RTC	N/A	Available	Available	Off	Off
Wake-up on pin edge	N/A	Available	Available	Available	Off
Wake-up on reset pin	On	On	On	On	On
Brownout detector (BOD)	On	On	Duty Cycled	Off	Off
Power-on reset (POR)	On	On	On	On	On
Watchdog timer (WDT)	Available	Available	Available	Off	Off

(1) “Available” indicates that the specific IP or feature can be enabled by the user application in the corresponding device operating modes. “On” indicates that the specific IP or feature is turned on, irrespective of the user application configuration of the device in the corresponding device operating mode. “Off” indicates that the specific IP or feature is turned off and not available for the user application in the corresponding device operating mode.
(2) Software-based retention of CPU registers with context save and restore when entering and exiting standby power mode.
(3) In active and idle power modes, the HFOSC tracking loop is enabled by default, thereby enabling 48MHz HFXT as well.
(4) If LFOSC HW calibration is enabled in standby mode, then, HFOSC tracking loop requiring HFXT is dutycycled. If not, only HFOSC is duty-cycled during recharge cycles.
(5) AFOSC standby behavior is controlled by AFOSCCTL.AUTODIS. When set, AFOSC is disabled when entering standby. Enabling AFOSC again on standby exit must be done by software.

In the **Active** mode, both of MCU and AON power domains are powered. Clock gating is used to minimize power consumption. Clock gating to peripherals/subsystems is controlled manually by the CPU.

In **Idle** mode, the CPU is in sleep, but selected peripherals and subsystems (such as the radio) can be active. Infrastructure (Flash, ROM, SRAM, bus) clock gating is possible depending on the state of the DMA and debug subsystem.

In **Standby** mode, only the always-on (AON) domain is active. An external wake-up event, RTC event, or comparator event (LP-COMP) is required to bring the device back to active mode. Pin Reset will also drive the device from Standby to Active. MCU peripherals with retention do not need to be reconfigured when waking up again, and the CPU continues execution from where it went into standby mode. All GPIOs are latched in standby mode.

In **Shutdown** mode, the device is entirely turned off (including the AON domain), and the I/Os are latched with the value they had before entering shutdown mode. A change of state on any I/O pin defined as a wake from shutdown pin wakes up the device and functions as a reset trigger. The CPU can differentiate between a reset in this way and a reset-by-reset pin or power-on reset, or thermal shutdown reset, by reading the reset status register. The only states retained in this mode are the latched I/O state, the 3V register bank, and the flash memory contents.

Note

The power, RF, and clock management for the CC27xx devices require specific configuration and handling by software for optimized performance. This configuration and handling are implemented in the TI-provided drivers that are part of the SimpleLink Low Power F3 software development kit (SDK). Therefore, TI highly recommends using this software framework for all application development on the device. The complete SDK with FreeRTOS, device drivers, and examples are offered free of charge in source code.

8.15 Clock Systems

The CC27xx devices have the following internal system clocks.

- The 96MHz HFCLK is used as the main system (MCU and peripherals) clock. This is driven by the internal 96MHz RC Oscillator (HFOSC), which can track its accuracy against an external 48MHz crystal (HFXT). The HFOSC tracking loop is enabled by default by the system ROM bootcode. Radio and ADC operate with the external 48MHz crystal oscillator.
- The 32.768kHz LFCLK is used as the internal low-frequency system clock. It is used for the RTC, the watchdog timer (if enabled in standby power mode), and to synchronize the radio timer after exiting Standby power mode. LFCLK can be driven by the internal 30-34kHz RC Oscillator (LFOSC), a 32.768kHz watch-type crystal, or a clock input in LFXT bypass mode. When using a crystal or the internal RC oscillator, the device can output the 32kHz LFCLK signal to other devices, thereby reducing the overall system cost.
- The 80/90.3168/98.304 MHz AFOSC (Auxiliary Frequency Oscillator) is used as the high-frequency clock for generating needed frequencies to support audio I^2S operations. The AFOSC tracks the HFOSC, which in turn, tracks its accuracy against the external 48MHz crystal (HFXT). AFOSC can generate 80, 90.3168, and 98.304MHz clock frequencies with a 10ppb tracking accuracy from HFOSC.

8.16 Network Processor

Depending on the product configuration, the CC27xx device can function as a wireless network processor (WNP —a device running the wireless protocol stack with the application running on a separate host MCU), or as a system-on-chip (SoC—with the application and protocol stack running on the system CPU inside the device).

In the first case, the external host MCU communicates with the device using SPI or UART. In the second case, the application must be written according to the application framework supplied with the wireless protocol stack.

8.17 Integrated BALUN, High Power PA (Power Amplifier)

For applications that need an increased RF link budget, the CC27xx high-power PA device variants ("P" devices) can support RF transmit output power operation up to +20dBm EIRP (Effective Isotropic Radiated Power). To optimize the system BOM components for applications using the integrated high-power PA, the "P" devices support an integrated RF switch with a single RF pin capable of transmitting and receiving signals on the same pin.

The CC27xx "R" devices support the regular PA (CC27xxRx) with radio transmit output power up to +10dBm EIRP. Both the CC27xx "R" and the "P" variants support an integrated BALUN with a single-ended 50-ohm RF pin, thereby reducing the number of external components needed for the antenna interface.

9 Application, Implementation, and Layout

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Reference Designs

Follow these reference designs very closely when implementing designs using the device.

Special attention must be paid to RF component placement, decoupling capacitors, and DC/DC regulator components, as well as ground connections for all of these.

LP-EM-CC2745R10-Q1 Design Files
The CC2745R10-Q1 LaunchPad Design Files contain detailed schematics and layouts to build application-specific boards using the device.

Sub1GHz and 2.4GHz Antenna Kit for LaunchPad™ Development Kit and SensorTag
The antenna kit allows real-life testing to identify the optimal antenna for your application. The antenna kit includes 16 antennas for frequencies from 169MHz to 2.4GHz, including:

- PCB antennas
- Helical antennas
- Chip antennas
- Dual-band antennas for 868MHz and 915MHz combined with 2.4GHz

The antenna kit includes a JSC cable to connect to the Wireless MCU LaunchPad Development Kits and SensorTags.

9.2 Junction Temperature Calculation

This section shows the different techniques for calculating the junction temperature under various operating conditions. For more details, see *Semiconductor and IC Package Thermal Metrics*.

There are two recommended ways to derive the junction temperature from other measured temperatures:

1. From the package temperature:

$$T_J = \psi_{\mathrm{JT}} \times P + T_{\mathrm{case}} \tag{1}$$

2. From the board temperature:

$$T_J = \psi_{\mathrm{JB}} \times P + T_{\mathrm{board}} \tag{2}$$

P is the power dissipated from the device and can be calculated by multiplying the current consumption with the supply voltage. Thermal resistance coefficients are found in *Thermal Resistance Characteristics*.

Example:

In this example, we assume a simple use case where the radio is transmitting continuously at 0dBm output power. Let us assume we want to maintain a junction temperature of 105°C and the supply voltage is 3.3V. Using Equation 1, the temperature difference between the top of the case and junction temperature is calculated. To calculate P, look up the current consumption for TX 0dBm at 105°C from the plot Figure 7-10. At 105°C, the current consumption is approximately 9.5mA. This means that P is 9.5mA × 3.3V = 31.35mW.

The maximum case temperature is then calculated as:

$$T_{\mathrm{case}} < T_j - 0.2^{\circ C}/_{W} \times 31.35 \ \ mW = 104.99^{\circ}C \tag{3}$$

For various application use cases, current consumption for other modules may have to be added to calculate the appropriate power dissipation. For example, the MCU may be running simultaneously as the radio, peripheral modules may be enabled, and so on. Typically, the easiest way to find the peak current consumption, and thus the peak power dissipation in the device, is to measure as described in the *Measuring CC13xx and CC26xx Current Consumption* application report.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed as follows.

10.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to all part numbers and/or date-code. Each device has one of three prefixes/identifications: X, P, or null (no prefix) (for example, X is in preview; therefore, an X prefix/identification is assigned).

Device development evolutionary flow:

X Experimental device that is not necessarily representative of the final device's electrical specifications and may not use the production assembly flow.

P Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

null Production version of the silicon die that is fully qualified.

Production devices have been characterized fully, and the quality and reliability of the devices are demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate is still undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, *RHA*).

For orderable part numbers of devices in the RHA (6mm × 6mm) package type, see the *Package Option Addendum* of this document, the Device Information in Section 3, the TI website (www.ti.com), or contact your TI sales representative.

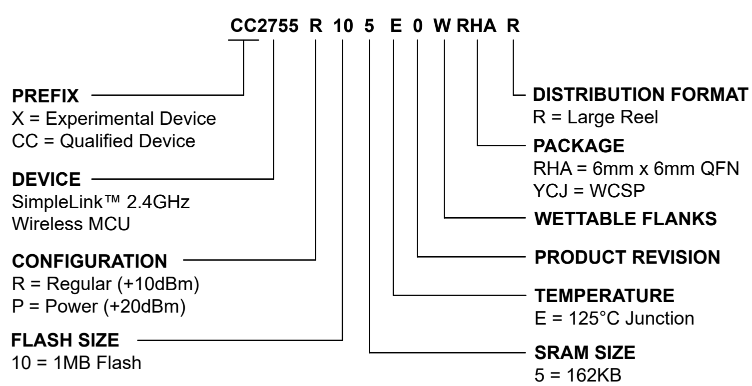

Figure 10-1. Device Nomenclature

10.2 Tools and Software

The CC2755x10 devices are supported by a variety of software and hardware development tools.

Software

SimpleLink™ low-power software development kit (SDK)

The SimpleLink low-power software development kit (SDK) provides a complete package for the development of wireless applications on the CC27xx family of devices. The SDK includes a comprehensive software package for the CC2755R and CC2755P devices, including the following protocol stacks:

- Bluetooth Low Energy 6.x
- Zigbee

- Thread
- Matter
- Proprietary Systems

The SimpleLink low-power SDK is part of TI's SimpleLink MCU platform, offering a single development environment that delivers flexible hardware, software, and tool options for customers developing wired and wireless applications. For more information about the SimpleLink MCU Platform, visit https://www.ti.com/simplelink.

Zephyr

Our Zephyr stack delivers a fully certified open-source and portable Bluetooth solution while maintaining low power, enabled by TI's Bluetooth LE Controller. Through a TI-managed downstream branch, we ensure faster delivery, bug fixes, and controlled updates for CC2340 and CC2755 devices. Customers benefit from portability across silicon vendors, extensive testing with Twister, Ztest frameworks and additional validation, plus a complete production-ready SDK and TI tool ecosystem.

Development Tools

Code Composer Studio™ Integrated Development Environment (IDE)

Code Composer Studio is an integrated development environment (IDE) that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio comprises a suite of tools used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface, taking you through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse® software framework with advanced embedded debug capabilities from TI, resulting in a compelling, feature-rich development environment for embedded developers.

CCS has support for all SimpleLink Wireless MCUs and includes support for EnergyTrace™ software (application energy usage profiling). A real-time object viewer plugin is available for Free-RTOS.

Code Composer Studio is provided free of charge when used in conjunction with the XDS debuggers included on a LaunchPad Development Kit.

IAR Embedded Workbench® for Arm®

IAR Embedded Workbench® is a set of development tools for building and debugging embedded system applications using assembler, C, and C++. It provides a completely integrated development environment that includes a project manager, editor, and build tools. IAR has support for all SimpleLink Wireless MCUs. It offers broad debugger support, including XDS110, IAR I-jet™, and Segger J-Link™. IAR is also supported out of the box on most software examples provided as part of the SimpleLink SDK.

A 30-day evaluation or a 32KB size-limited version is available through iar.com.

SmartRF™ Studio

SmartRF™ Studio is a Windows® application that can be used to evaluate and configure SimpleLink Wireless MCUs from Texas Instruments. The application will help designers of RF systems to easily evaluate the radio at an early stage in the design process. It is especially useful for generating configuration register values and for practical testing and debugging of the RF system. SmartRF Studio can be used either as a standalone application, through a command line interface to enable more automation, or together with applicable evaluation boards or debug probes for the RF device. Features of the SmartRF Studio include:

- Link tests send and receive packets between nodes
- Antenna and radiation tests set the radio in continuous wave TX and RX states
- Export radio configuration code for use with the TI SimpleLink SDK RF driver
- Custom GPIO configuration for signaling and control of external switches

CCS UniFlash	CCS UniFlash is a standalone tool used to program on-chip flash memory on TI MCUs. UniFlash has a GUI, command line, and scripting interface. CCS UniFlash is available free of charge.

10.2.1 SimpleLink™ Microcontroller Platform

The SimpleLink microcontroller platform sets a new standard for developers with the broadest portfolio of wired and wireless Arm® MCUs (System-on-Chip) in a single software development environment. Delivering flexible hardware, software, and tool options for your IoT applications. Invest once in the SimpleLink software development kit and use throughout your entire portfolio. Learn more about Simplelink.

10.2.2 Software License and Notice

The system ROM firmware includes open-source MCUBoot software licensed under APACHE-2.0. See the following links for more information:

- MCUBoot Apache 2.0 license terms
- MCUBoot notice information

10.3 Documentation Support

To receive notification of documentation updates on data sheets, errata, application notes, and similar, navigate to the device product folder on TI.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The current documentation that describes the MCU, related peripherals, and other technical collateral is listed as follows.

TI Resource Explorer

TI Resource Explorer	Software examples, libraries, executables, and documentation are available for your device and development board.

Errata

CC2755R/P Silicon Errata	The silicon errata describes the known exceptions to the functional specifications for each silicon revision of the device and describes how to recognize a device revision.

Application Reports

All application reports for the CC275xR10 devices are found in the device product folder.

Technical Reference Manual (TRM)

CC27xx SimpleLink™ Wireless MCU TRM	The TRM provides a detailed description of all modules and peripherals available in the device family.

10.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.5 Trademarks

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CoreMark® is a registered trademark of Embedded Microprocessor Benchmark Consortium Corporation.
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Eclipse® is a registered trademark of Eclipse Foundation.
IAR Embedded Workbench® is a registered trademark of IAR Systems AB.
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10.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from July 1, 2025 to November 30, 2025 (from Revision C (July 2025) to Revision D (December 2025)) **Page**

- Updated Bluetooth LE qualification status.......1
- Updated Zigbee certification status.......1
- Removed reference to BP-EM-CS.......1
- Updated part numbers in device information table.......2
- Added P device "Power Consumption - Radio Modes (P variant) table".......40
- Added P variant specifications in "Bluetooth Low Energy-Transmit (Tx)" table.......45
- Added China MIIT limits to "Spurious emissions and harmonics" table for both R and P variants.......48
- Added P variant specifications in "2.4GHz Rx/Tx CW" table.......48
- Added Zephyr to Software overview.......79

Changes from June 12, 2025 to July 11, 2025 (from Revision B (June 2025) to Revision C (July 2025)) **Page**

- Removed "Sensor Controller" Section.......68
- Updated radio description.......69
- Changed temperature calculation example.......78
- Updated development kit links.......79

Changes from May 30, 2025 to June 11, 2025 (from Revision A (May 2025) to Revision B (June 2025)) **Page**

- Updated YCJ package pin diagram.......9
- Updated signal descriptions table.......12
- Corrected table and added VDDIO information.......14
- Updated peripheral pin mapping table.......19

- Updated peripheral signal descriptions table.......... 29
- Updated development kit links.......... 79

Changes from October 1, 2024 to May 29, 2025 (from Revision * (October 2024) to Revision A (May 2025)) **Page**

- Updated security features list.......... 1
- Updated links.......... 2
- Updated block diagram.......... 4
- Updated the Device Comparison table.......... 6
- Added WCSP package.......... 7
- Add YCJ package pin diagram.......... 9
- Updated the description for pins 29 and 31.......... 10
- Added YCB peripheral signal descriptions.......... 29
- Added specifications.......... 37
- Updated nomenclature diagram.......... 79
- Added open source software license and notice.......... 81
- Updated documentation resources.......... 81
- Added YCJ package drawing.......... 84

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CC2755P105E0WRHAR	Active	Production	VQFN (RHA) | 40	4000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CC2755 P10
CC2755R105E0WRHAR	Active	Production	VQFN (RHA) | 40	4000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CC2755 R10
X2755R105E0WRHAR	Active	Preproduction	VQFN (RHA) | 40	4000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
X2755R105E0WRHAR.A	Active	Preproduction	VQFN (RHA) | 40	4000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
X2755R105E0WRHAR.B	Active	Preproduction	VQFN (RHA) | 40	4000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

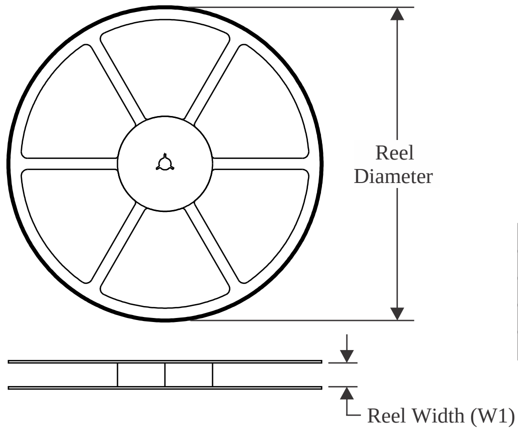
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

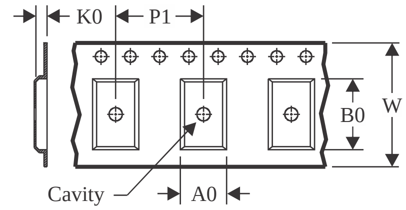
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

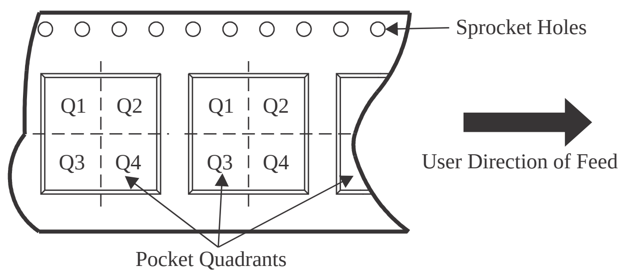


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

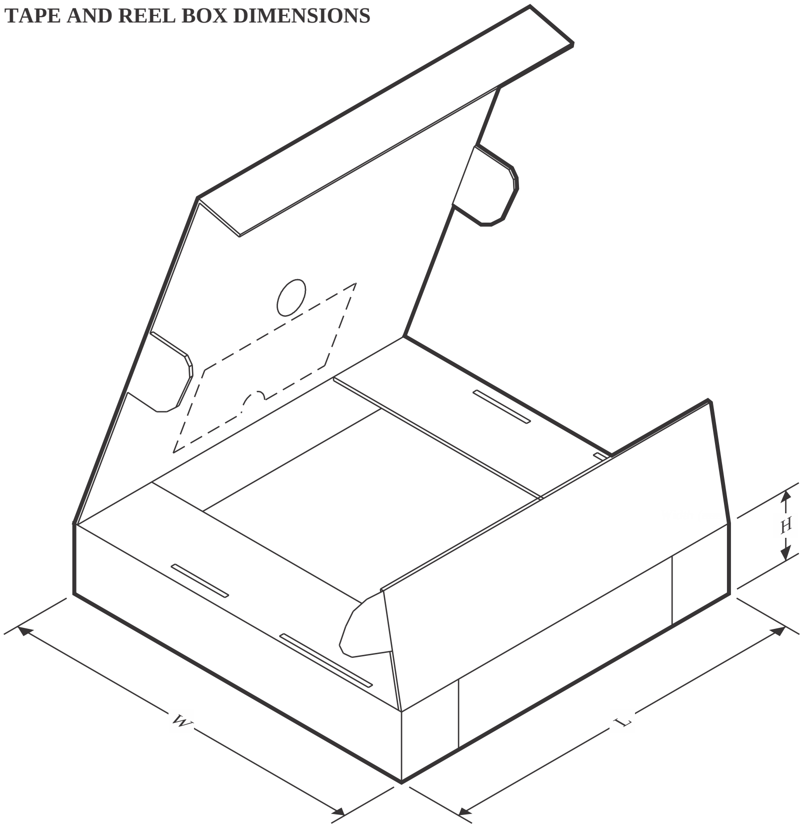
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CC2755P105E0WRHAR	VQFN	RHA	40	4000	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
CC2755R105E0WRHAR	VQFN	RHA	40	4000	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

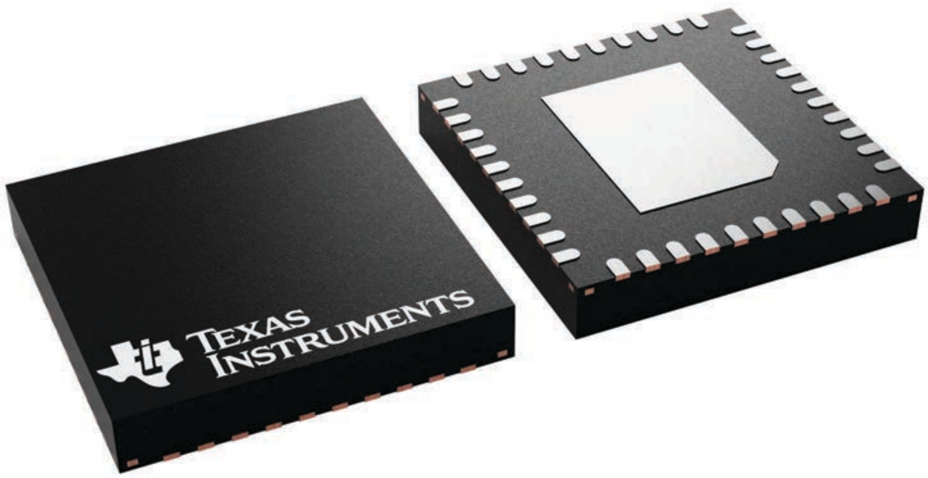
TAPE AND REEL BOX DIMENSIONS



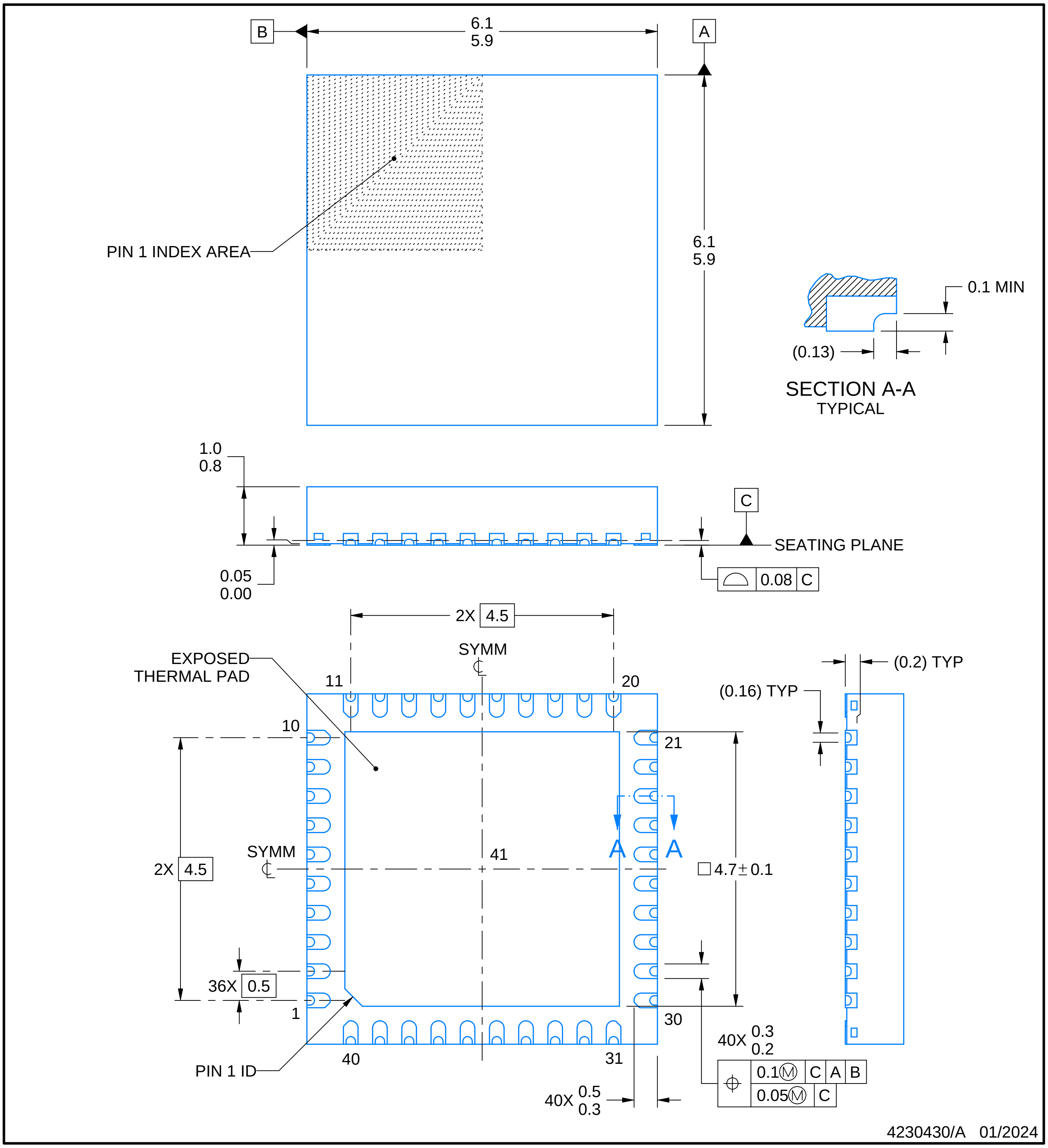
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CC2755P105E0WRHAR	VQFN	RHA	40	4000	367.0	367.0	35.0
CC2755R105E0WRHAR	VQFN	RHA	40	4000	367.0	367.0	35.0

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

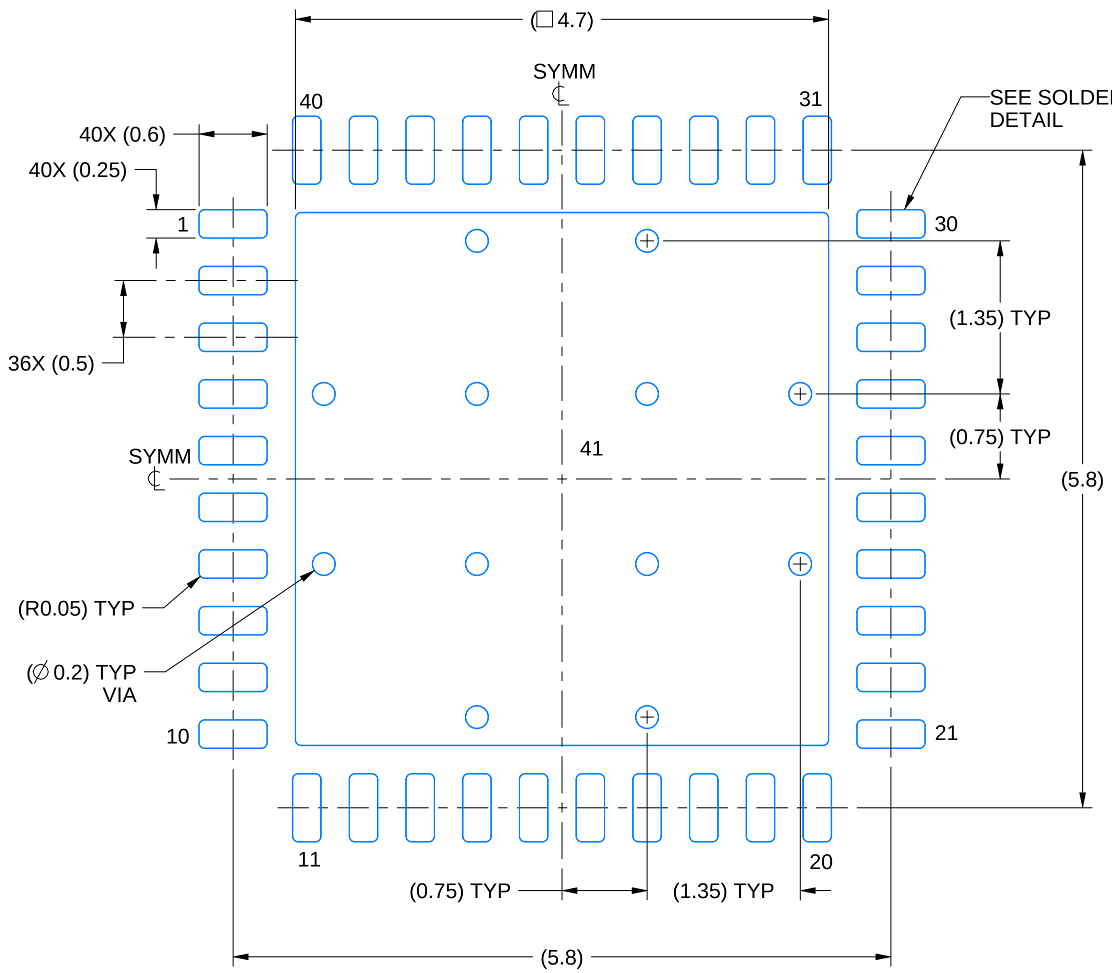


4225870/A

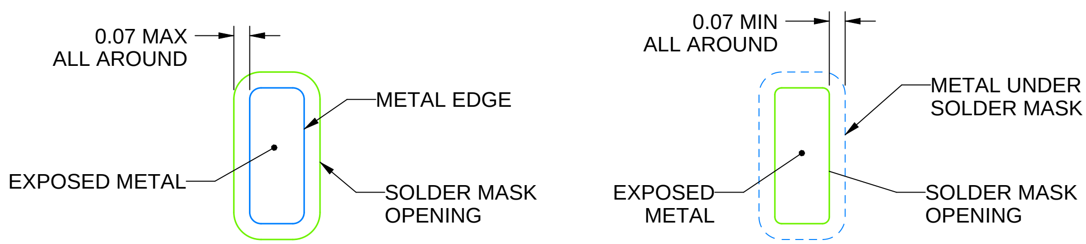


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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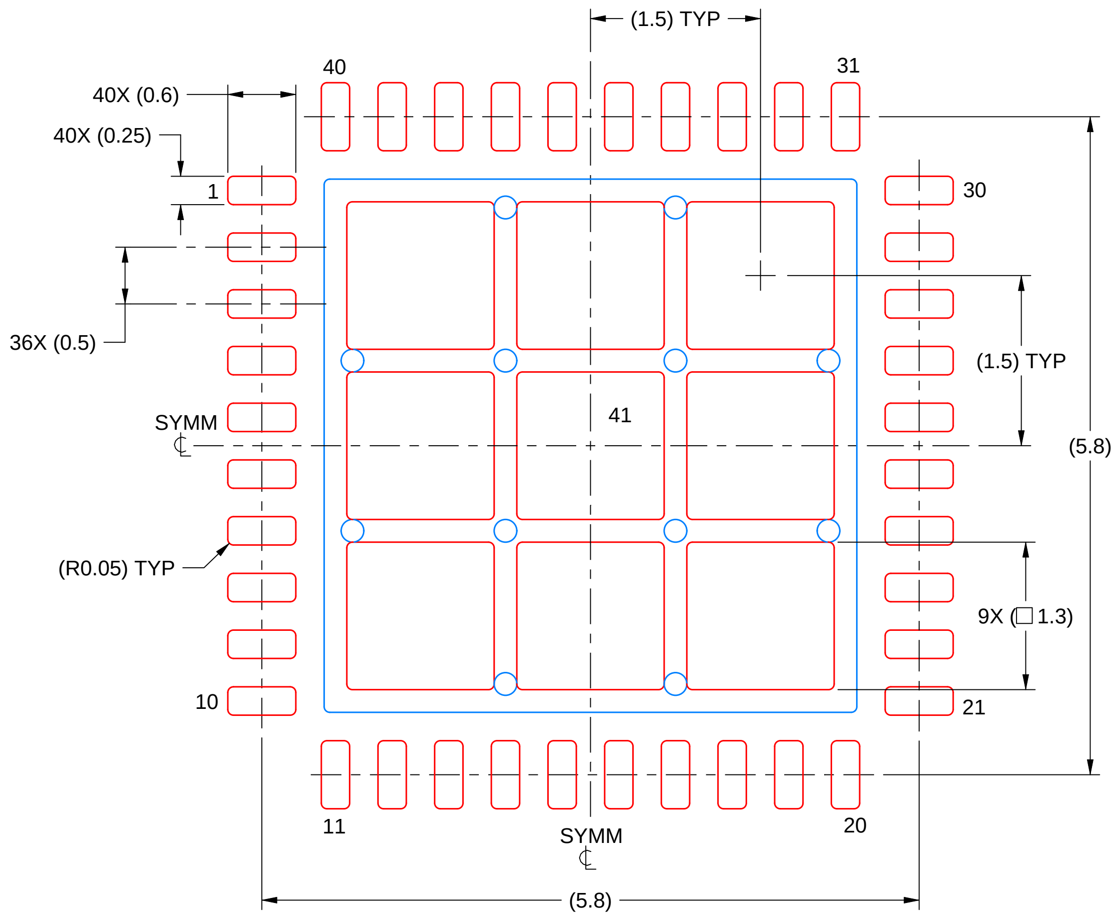
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 41
69% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.