CD326x Audio Interface Transmitter for Specially Enabled Headsets

1 Features

- Compatible with specially enabled audio interfaces (iPhone® and iPad®)
- Low quiescent current
  - Button mode (microphone not in use): 3µA
  - Tone mode (microphone in use): 110µA
- Miniature DSBGA (YZP) package
- ESD performance
  - Human body model: 2000V
  - Charged device model: 500V

2 Applications

- Wired headset signaling transmitter compatible with systems including a specially enabled audio interface
- See Chapter 54: *Headset Remote and Microphone Transmitter* in Accessory Design Guidelines for Apple Devices from the Apple Development Page

3 Description

The CD326x supports two operating modes; button mode and tone mode. Button mode offers no microphone support. Button mode passes the DC voltage from an external switch-resistor network (tied to the REM pin) to the MIC pin to measure the voltage externally. Tone mode offers microphone support and senses button presses based on an external switch-resistor network (tied to the REM pin). Tone mode generates corresponding ultrasonic signals that are superimposed (via a driver output on the TONE pin) on the system MICBIAS line. These signals control audio functions when connected to a specially enabled audio interface. The input DC bias level provided on the MIC pin controls button or tone mode selection. During tone mode, the CD326x also provides functionality to control or bias an external MEMS (micro-electrical-mechanical systems) technology microphone module.

Package Information

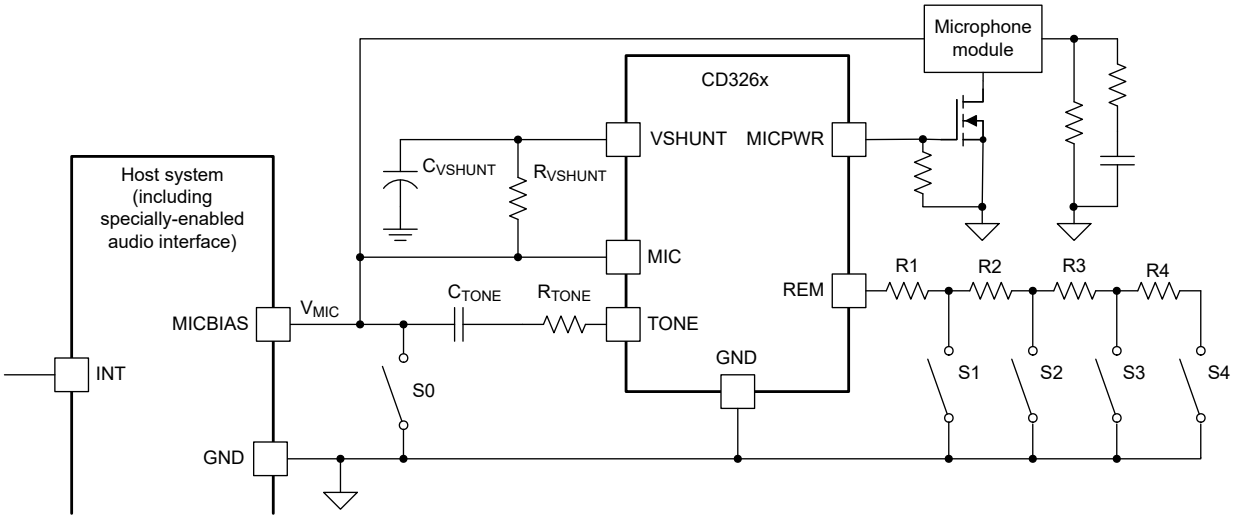
PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
CD3268	YZP (DSBGA, 6)	1.45mm × 0.95mm × 0.5mm
CD3269	YZP (DSBGA, 6)	1.45mm × 0.95mm × 0.5mm

(1) For all available packages, see the orderable addendum in Section 11

(2) The package size (length × width × height) is a nominal value and includes pins, where applicable

Device Information

PART NUMBER	TX ACK TONE FREQUENCY (kHz) (TYP)	EQUIVALENT BUTTON
CD3268	130	1
CD3269	165	2



Simplified Application

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4 Pin Configuration and Functions

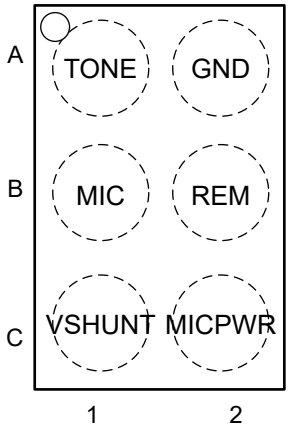


Figure 4-1. DSBGA Package, 6-Pin YZP (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
GND	A2	P	Ground
MIC	B1	I	Input DC bias; voltage determines the mode of operation.
MICPWR	C2	O	Microphone power; used as a control output to enable/disable an external microphone module.
REM	B2	I/O	Remote switch network
TONE	A1	O	Tone generator output
VSHUNT	C1	I	External microphone bias

(1) I = Input, O = Output, I/O = Input or Output, P = Power

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{SUPPLY}	Supply voltage, VSHUNT, MIC pins	-0.5	4.6	V
V_O	Output voltage, MICPWR, TONE pins	-0.5	4.6	V
I_{OK}	Output clamp current, MICPWR, TONE pins (V_O < 0)	-20		mA
V_I	Input voltage, REM pin	-0.5	4.6	V
I_{IK}	Input clamp current, REM pin (V_I < 0)	-20		mA
I_{SUPPLY} & I_{GND}	Continuous current through VSHUNT, MIC, or GND pins	-50	50	mA
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human Body Model	±2000	V
		Charged-Device Model	±500	

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{MICBIAS}$	Button Mode - Bias Voltage (MIC pin is connected to MICBIAS through a 1% 2.21kΩ resistor); MIC pin voltages in this range enable Button Mode	1.8		2.1	V
$V_{MICBIAS}$	Tone Mode - Bias Voltage (MIC pin is connected to MICBIAS through a 1% 2.21kΩ resistor); MIC pin voltages in this range enable Tone Mode	2.56		2.84	V
T_A	Ambient temperature	–40		85	°C

5.4 Thermal Information

THERMAL METRIC(1)		YZP (DSBGA)	UNIT
		6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance - YZP Package	123	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Biases, Currents, & Thresholds						
$I_{MICBIAS-B}$	Quiescent Current into MIC + VSHUNT	Button Mode, $V_{MICBIAS}$ = 2.1V, (Figure 6-2)		3	6	µA
I_{MIC-T}	Quiescent Current into MIC	Tone Mode, (Figure 6-3)		34	46	µA
$I_{VSHUNT-T}$	Quiescent Current into VSHUNT	Tone Mode(1), (Figure 6-3)		60	80	µA
I_{MIC-TA}	Active Current into MIC	Tone Mode, (Figure 6-4)		35	45	µA

5.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{VSHUNT-TA}$	Active Current into VSHUNT	Tone Mode(1), (Figure 6-4)		104	123	µA
V_{TR}	Tone Mode Threshold Voltage - Rising	MIC Rising (microphone enable), V_{MICPWR} = 1.0V, (Figure 6-6 and Figure 6-7)	2.20	2.35	2.5	V
V_{TF}	Tone Mode Threshold Voltage - Falling	MIC Falling (microphone enable), V_{MICPWR} = 0.4V, (Figure 6-6 and Figure 6-7)	0.55	0.8	1	V
V_{MICPWR}	MICPWR Output Voltage	I_{MICPWR} = 120µA to 150µA, (Figure 6-5)	1.51	1.56	1.61	V
R_{SO}	Shunt Regulator Output Impedance	Freq = 100Hz, (Figure 6-8)	5	18	25	Ω
		Freq = 20kHz, (Figure 6-8)	12	21	35	Ω
		Freq = 300kHz, (Figure 6-8)	300	458	650	Ω
		Freq = 1MHz, (Figure 6-8)	2600	2830	3300	Ω
R_{ONA}	Switch A, R_{DSON}	Tone Mode, I_{MICPWR} = 1mA, $V_{MICBIAS}$ = 2.56V, (Figure 6-9)		40	55	Ω
R_{ONB}	Switch B, R_{DSON}	Button Mode, I_{REM} = 1mA, V_{MIC} = 1.2V, (Figure 6-10)		22	30.5	Ω
Tone and Button Mode Parameters						
$e_{n-mic100}$	MIC Integrated Noise	100Hz to 20kHz, (Figure 6-1)		1.5	2	$µV_{RMS}$
$e_{n-mic1K}$	MIC Integrated Noise	1kHz to 20kHz, (Figure 6-1)		0.39	1	$µV_{RMS}$
f_{TONE1}	Button 1 Frequency - CD3268 ACK Tone	R_{REM} = 6.81kΩ, (Figure 6-13)	109	130	159	kHz
f_{TONE2}	Button 2 Frequency - CD3269 ACK Tone	R_{REM} = 9.42kΩ, (Figure 6-13)	138	165	200	kHz
f_{TONE3}	Button 3 Frequency	R_{REM} = 12.99kΩ, (Figure 6-13)	167	201	242	kHz
f_{TONE4}	Button 4 Frequency	R_{REM} = 19.8 kΩ, (Figure 6-13)	196	237	284	kHz
f_{CAL}	Calibration Frequency	(Figure 6-13)	225	271	325	kHz
f_{REL}	Button Release Frequency	(Figure 6-13)	81	97	117	kHz
BR_1	Button 1 Ratio	f_{TONE1} / f_{CAL}	0.470	0.488	0.500	
BR2	Button 2 Ratio	f_{TONE2} / f_{CAL}	0.600	0.609	0.630	
BR_3	Button 3 Ratio	f_{TONE3} / f_{CAL}	0.730	0.740	0.758	
BR_4	Button 4 Ratio	f_{TONE4} / f_{CAL}	0.860	0.876	0.890	
BR_{REL}	Button Release Ratio	f_{REL} / f_{CAL}	0.340	0.360	0.380	
R_{BT1}	Button 1 Boundary		6.61	6.81	7.01	kΩ
R_{BT2}	Button 2 Boundary		9.14	9.42	9.7	kΩ
R_{BT3}	Button 3 Boundary		12.60	12.99	13.38	kΩ
R_{BT4}	Button 4 Boundary		19.21	19.80	20.39	kΩ
V_{TA}	Tone Amplitude	R_{TONE} = 1MΩ, (Figure 6-11 and Figure 6-12)	350	550	720	mVp-p
		R_{TONE} = 100kΩ, (Figure 6-11 and Figure 6-12)	300	515	710	mVp-p
		R_{TONE} = 10kΩ, (Figure 6-11 and Figure 6-12)	200	390	620	mVp-p
		R_{TONE} = 1kΩ, (Figure 6-11 and Figure 6-12)	40	140	320	mVp-p

(1) This current is pulled through R_{VSHUNT} between MIC and VSHUNT and is the minimum current to keep VSHUNT regulated at 1.56V. Excess current through R_{VSHUNT} will be available to the load at MICPWR. Excess current not used by the load at MICPWR will be internally shunted to GND.

5.6 Timing Requirements

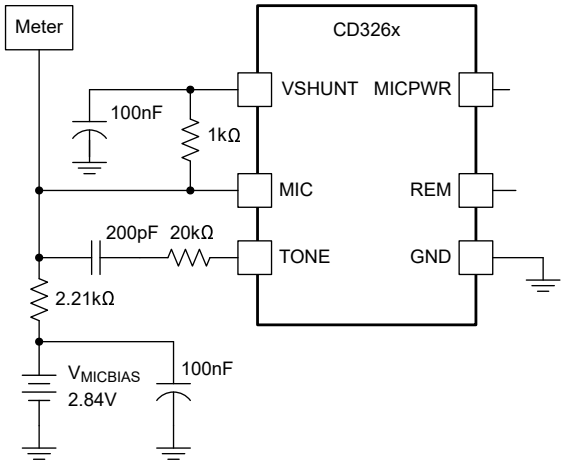
over operating free-air temperature range (unless otherwise noted)

PARAMETER	DEFINITION	MIN	TYP	MAX	UNIT
Tone, Button, and Switch Timing					
t_{CAL}	Calibration Tone Duration, (Figure 7-2)	0.8	0.9	0.98	ms
t_{ACK}	ACK Tone Duration, (Figure 7-2)	5.0	5.5	6.0	ms
t_{B}	Button Tone Duration	1.4	1.8	2.2	ms
t_{DB}	Button Debounce Time	8.4	9.1	10	ms
t_{M2T}	Tone Send Delay after Tone Mode Enable, (Figure 7-2)	4	6	8	ms
t_{ONA}	Switch A Enable Time, (Figure 7-2)	0.8	1.2	2	ms
t_{OFFB}	Switch B Disable Time, (Figure 7-2)	0.7	1	2	ms
t_{REG}	Shunt Regulator Enable Time: time from MIC = 2.3V to MICPWR = 1.56V, (Figure 7-2)	1	2.5	3.5	ms

6 Parameter Measurement Information

This section shows design schematics for select performance measurements.

6.1 e_{N-MIC} Microphone Integrated Noise Measurement



V_{MIC} must rise above 2.35V (typ) to enter tone mode before measurement.

Figure 6-1. Test Set-up for MIC Integrated Noise

6.2 Current Measurements

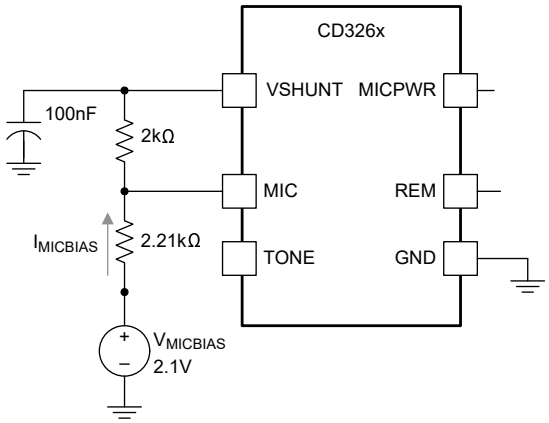
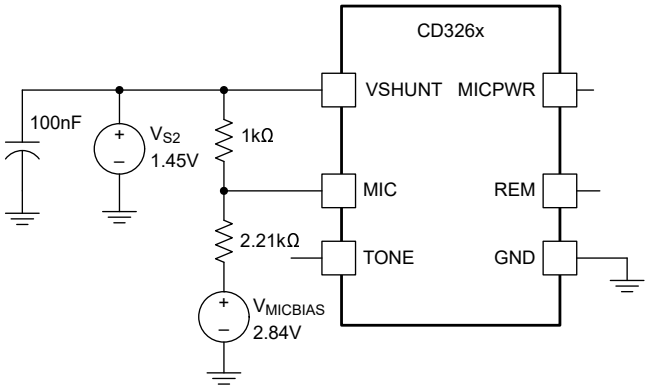


Figure 6-2. Test Set-up for Button Mode Current Measurement

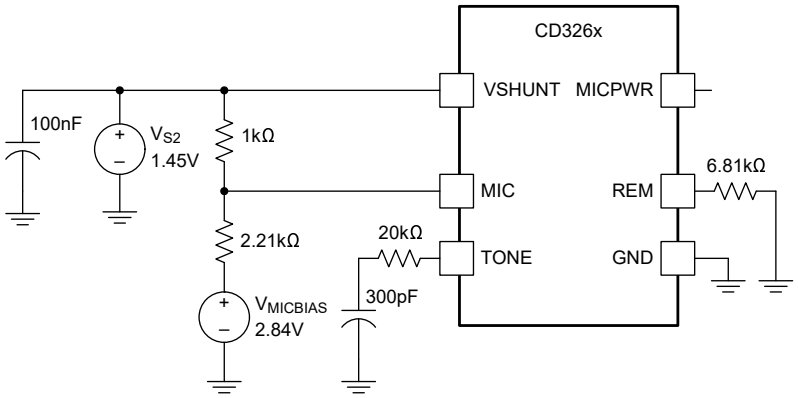


V_{MIC} must rise above 2.35V (typ) to enter tone mode before measurement is taken.

$$I_{MIC-T} = I_{MICBIAS} - \left(\frac{V_{MIC} - 1.45}{1.0k}\right)$$

$$I_{VSHUNT-T} = \left(\frac{V_{MIC} - 1.45}{1.0k}\right) - I_{VS2}$$

Figure 6-3. Tone Mode Quiescent Current Consumption Measurement



V_{MIC} must rise above 2.35V (typ) to enter tone mode before V_{S2} is applied.

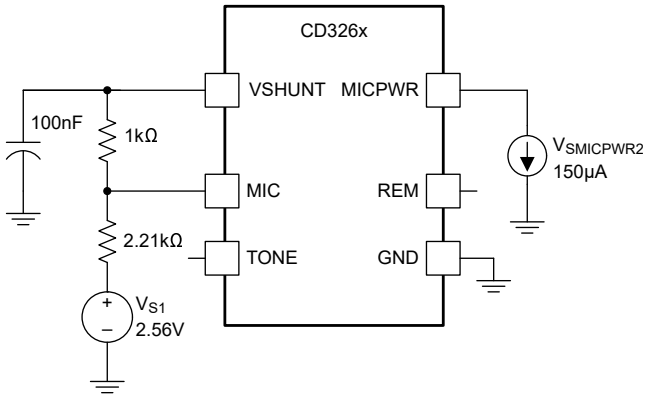
Current measurements are taken during calibration tone.

$$I_{MIC-T} = I_{MICBIAS} - \left(\frac{V_{MIC} - 1.45}{1.0k}\right)$$

$$I_{VSHUNT-T} = \left(\frac{V_{MIC} - 1.45}{1.0k}\right) - I_{VS2}$$

Figure 6-4. Tone Mode Active Current Consumption Measurement

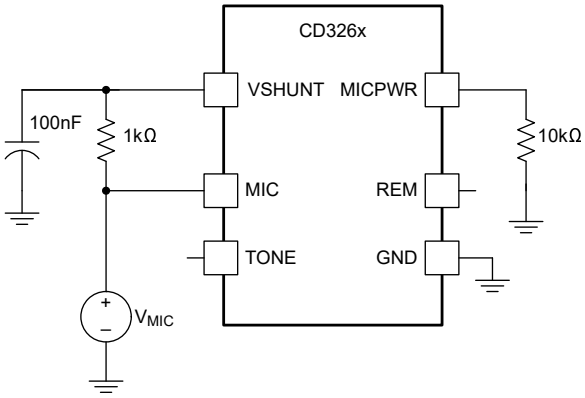
6.3 MICPWR Output Voltage Measurement



V_{MIC} must rise above 2.35V (typ) to enter tone mode before measurement is taken.

Figure 6-5. V_{MICPWR} Measurement

6.4 Tone Mode Threshold Measurements



V_{MIC} must rise above 2.35V (typ) to enter tone mode before measurement is taken.

Figure 6-6. V_{TR} and V_{TF} Measurement

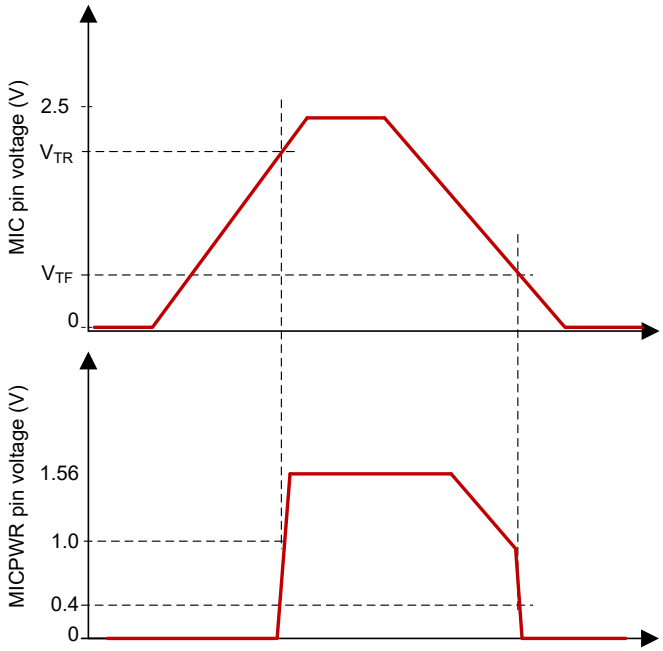
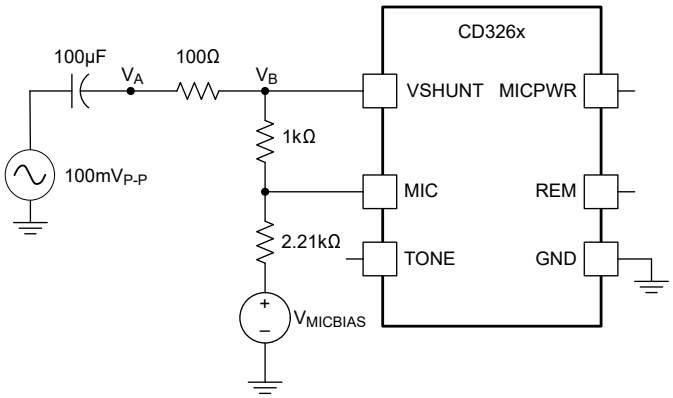


Figure 6-7. V_{TR} and V_{TF} Waveforms

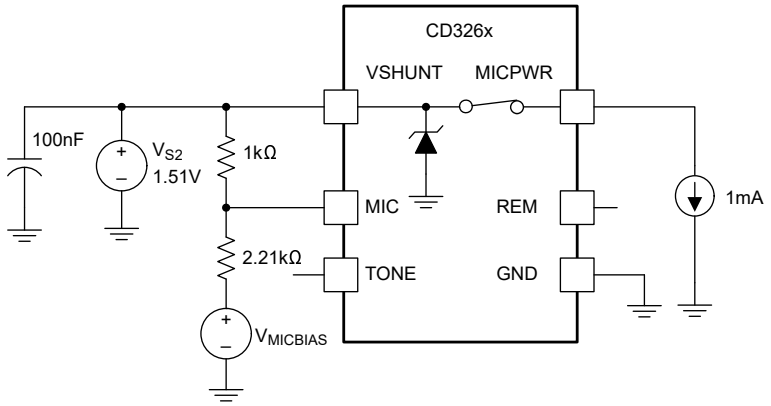
6.5 Impedance Measurements



V_{MIC} must rise above 2.35V (typ) to enter tone mode before measurement is taken.

$$R_{SO} = \frac{V_B}{(V_A - V_B)/100}$$

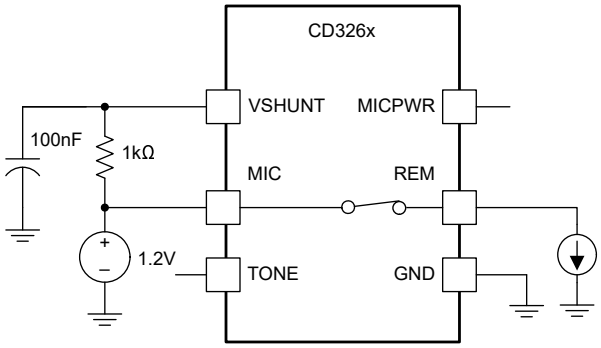
Figure 6-8. R_{SO} Shunt Regulator Impedance Measurement



V_{MIC} must rise above 2.35V (typ) to enter tone mode before measurement is taken.

$$R_{ONA} = \frac{1.51 - V_{MICPWR}}{1}$$

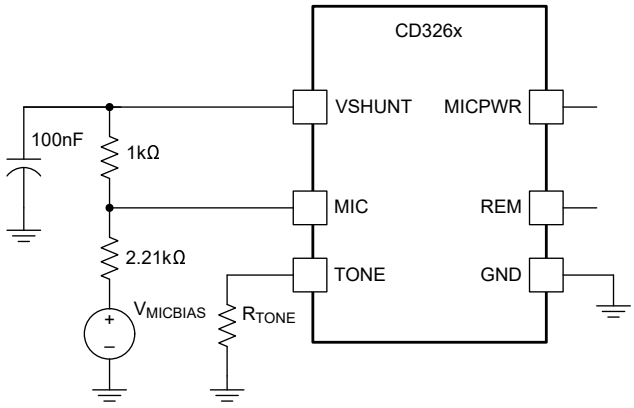
Figure 6-9. R_{ON} Switch A Measurement



$$R_{ONB} = \frac{1.2 - V_{REM}}{1}$$

Figure 6-10. R_{ON} Switch B Measurement

6.6 Tone Mode Output Measurements



V_{MIC} must rise above 2.35V (typ) to enter tone mode before measurement is taken.

Tone amplitude is measured during Cal Tone

Figure 6-11. V_{TA} Tone Amplitude Measurement

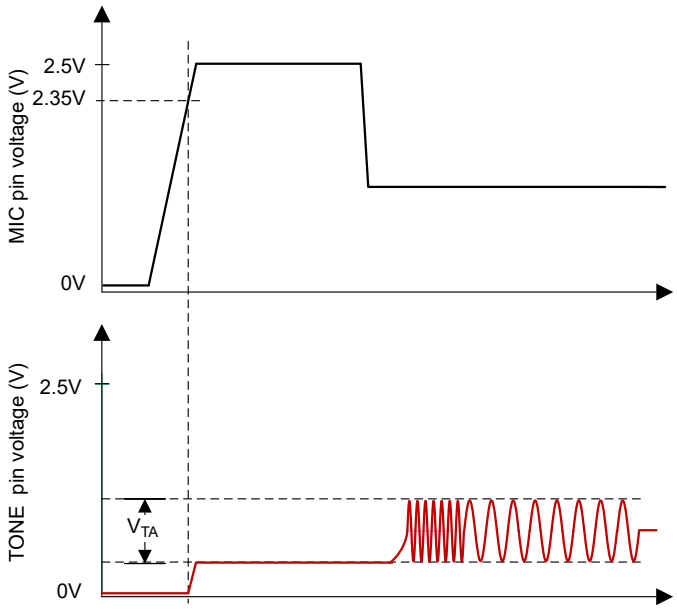
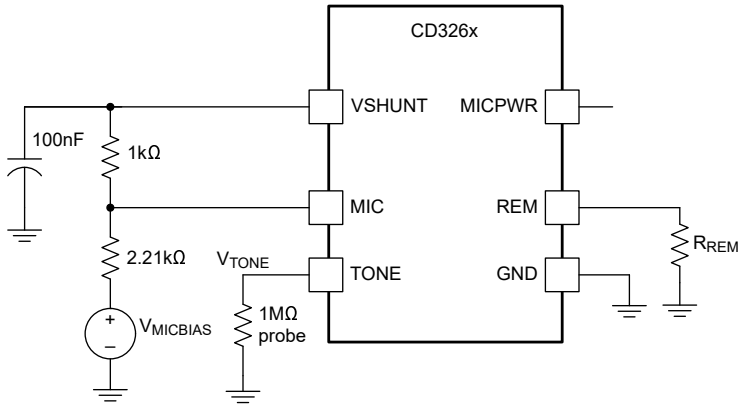


Figure 6-12. V_{TA} Waveforms



V_{MIC} must rise above 2.35V (typ) to enter tone mode before measurement is taken.

Figure 6-13. f_{TONE} Tone Frequency Measurement

7 Detailed Description

7.1 Overview

The CD326x communicates with a specially enabled audio interface to report detected remote button presses. Two basic modes are supported—button mode and tone mode—and the active mode is determined by the DC bias voltage level on the MIC pin (2.5V and 2.0V for tone mode and button mode respectively). The bias voltage is typically provided by a specially enabled audio interface.

During button mode operation, the CD326x operates as a pass-through element that connects the DC voltage on the REM pin to the MIC pin. The REM pin is connected to an external switch-resistor network where each switch represents a unique button. When a button is pressed, the DC level on the bias line is changed before being externally detected and measured by a specially enabled audio interface. Button mode does not support bias or control of an external microphone. In Figure 7-1, button mode is represented by switch A being open and switch B being closed.

During tone mode operation, the CD326x supports the use of an external MEMS microphone module. The module can be biased from the MICPWR pin or the MICPWR pin can be used to control an external circuit to enable or disable power to the microphone as shown in Figure 8-1. The REM pin is used to detect button presses from an external switch-resistor network, and the CD326x then generates a corresponding, ultrasonic signal on the TONE pin. The tones are unique to each button and are externally coupled to the system microphone bias line and MIC pin as seen in Figure 8-1. A specially enabled audio interface is able to determine the frequency of the tone, decode the tone into a specific button press, and control system operations accordingly. Most commonly, three button switches are used in the external switch-resistor network tied to the REM pin with the following functions: volume up, volume down, and center button. However, the CD326x supports up to four unique buttons, allowing for more customized functionality.

The CD326x also provides authentication, shunt regulation, and power-on-reset (POR) functionality. These are described in Section 7.3.

7.2 Functional Block Diagram

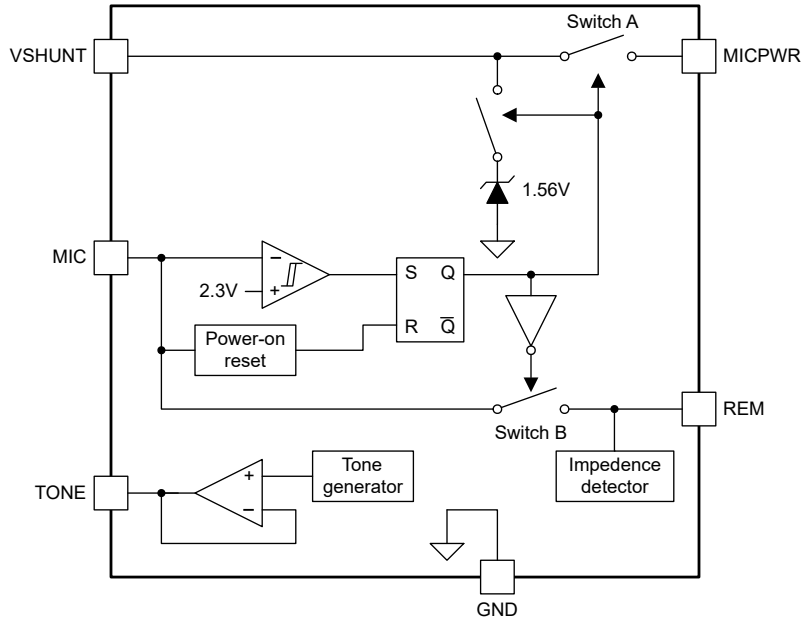


Figure 7-1. Functional Block Diagram

7.3 Feature Description

7.3.1 Tone Mode Start-up Timing

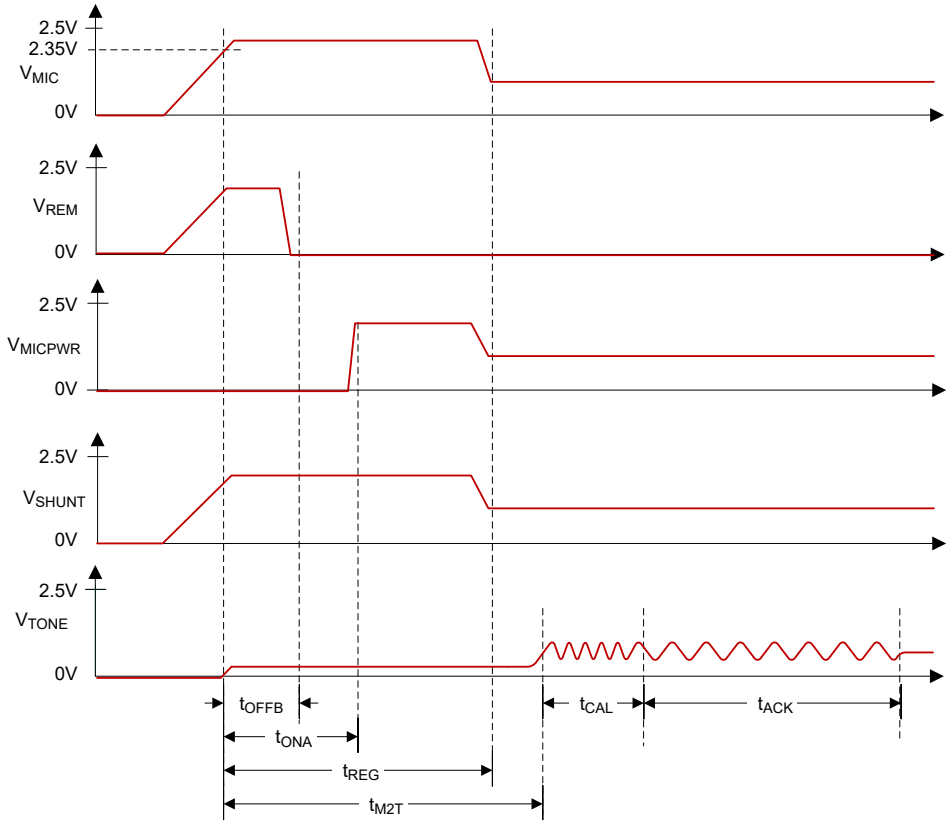


Figure 7-2. Tone Mode Start-up Timing

The tone mode start-up sequence is as follows:

1. After detecting V_{MIC} > 2.35V, the switch connecting the MIC and REM pins together (Switch B) is opened after time t_{OFFB}.
2. After a delay of t_{ONA} after V_{MIC} > 2.35V, the VSHUNT and MICPWR pins are shorted (with Switch A). The microphone is enabled by turning on the FET switch that is controlled by the MICPWR pin.
3. After a delay to allow the switches to settle, t_{M2T} after V_{MIC} > 2.35V, the CD326x sends a preset acknowledge (ACK) tone sequence.
4. The specially enabled audio interface detects the ACK sequence and authenticates the presence of the CD326x.

7.3.2 Authentication

To validate connectivity with a specially enabled audio interface, the CD326x provides an authentication sequence upon start-up. After enabling tone mode (applying V_{MIC} > 2.35V typical), the specially enabled audio interface waits to receive an acknowledgment from the CD326x. This acknowledgment is a tone sequence similar to a button press when operating as tone mode. When the CD326x recognizes tone mode upon power-up, the CD326x sends an acknowledgment (ACK) tone sequence to the specially enabled audio interface. The tone frequency is identical to the S1 button press tone for the CD3268 and to the S2 button press tone for the CD3269. However, the ACK tone sequence generates the second tone to be 3.7ms longer compared to the standard tone sequence for button presses.

The specially enabled audio interface reads the tone sequence as shown in Figure 7-6. The specially enabled audio interface takes three samples: the first to determine calibration frequency, the second to determine the

button/ACK frequency, and the third to differentiate between an authentication sequence and a button press. The third sample is taken 2.89ms after the second sample. If the specially enabled audio interface reads the ACK frequency during the third sample, the interface acknowledges a proper authentication sequence. If the tone frequency is not present during the third sample, the specially enabled audio interface recognizes the tone sequence as a button tone. When a button tone is recognized any time after the timeout period, the specially enabled audio interface records a button press event.

7.3.3 Shunt Regulator

An internal shunt regulator in the CD326x isolates the internal circuitry power supply from the MIC pin. The shunt regulator can provide power to an external microphone module through the MICPWR pin, or the MICPWR output can be used as an enable signal to control power to an external microphone module as shown in Figure 8-1. The CD326x regulates the MICPWR output to approximately 1.56V. The shunt regulator only regulates the VSHUNT and MICPWR pins during tone mode. During button mode operation, the CD326x powers down the regulator. An external resistance between the MIC and VSHUNT pins determines the current into the VSHUNT pin. The shunt regulator requires current of at least 93µA to maintain regulation of the VSHUNT pin. Any excess current becomes available to the load at MICPWR. Any further excess current is internally shunted to ground.

7.3.4 Power-on-reset

The CD326x has an internal power-on-reset (POR) circuit that holds all internal logic in a predetermined reset state until the supply voltage reaches a valid operating level and all internal nodes have stabilized. Figure 7-3 illustrates POR operation.

While the MIC pin is below V_{LVALID} (200mV typical), POR is in an indeterminate state. When the supply voltage on the MIC pin is greater than V_{LVALID}, the POR circuit asserts low until the supply rises to $V_{POR-RISE}$ (1.2V typical). When the supply reaches $V_{POR-RISE}$, the POR function enters a valid operating supply state, and the POR signal remains asserted low for a predetermined delay t_{DPOR} (1ms typical).

The POR function remains in the valid operating supply state until the supply voltage on the MIC pin falls below $V_{POR-FALL}$ (0.8V typical). Upon falling below this threshold, the POR circuit immediately asserts the POR signal and enters the original low-supply state until a valid operating supply voltage is supplied. When the POR circuit recognizes a low-supply voltage during t_{DPOR}, the circuit immediately resets the delay timer, maintains the asserted POR signal, and enters the low-supply state. After a valid operating supply voltage is reached again, the POR circuit repeats the operation.

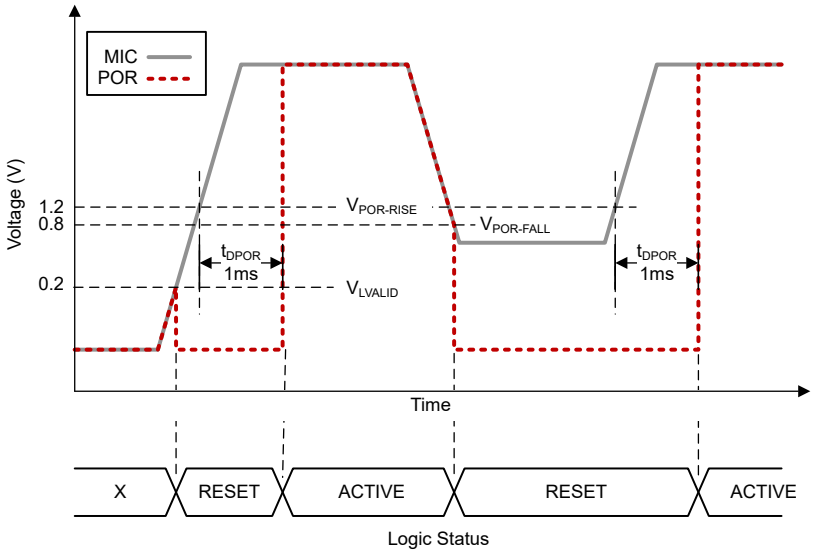


Figure 7-3. Power-on-reset (POR) Logic Signal

7.4 Device Functional Modes

7.4.1 Button Mode

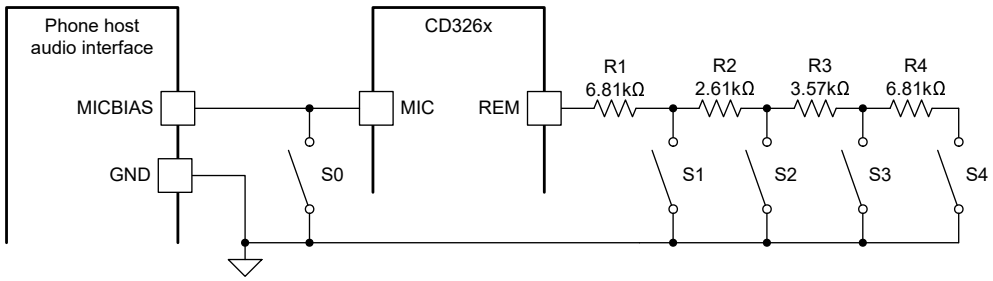
When the CD326x detects a MIC pin voltage below 2.35V (typ), the CD326x shorts the MIC and REM pins together and disables all other inputs and outputs. When a button press event occurs, the DC voltage on the microphone bias line changes according to the button being pressed. Table 7-1 shows the corresponding DC voltage for a given button press when using the resistor values in Figure 7-4. This DC level can then be detected by a specially enabled audio interface connected to the microphone bias line (MIC pin).

Switch S0 is a unique switch (typically controlled by a specially enabled audio interface) that shorts the MIC pin to ground. When Switch S0 shorts the MIC pin to ground, the specially enabled audio interface removes power from the CD326x. When power recovers, the CD326x enters button mode or tone mode depending on the voltage detected at the MIC pin.

Table 7-1. Typical Switch Voltage Values (Button mode)

Switch Closed	MIC Pin Voltage (V) (1)
S0	0
S1	1.510
S2	1.603
S3	1.690
S4	1.779

(1) $V_{MICBIAS}$ is the voltage on the MIC pin: 2.0V (typ)



≤1% tolerance resistors recommended

Figure 7-4. Recommended Button Mode Resistor Values

7.4.2 Tone Mode

When the CD326x detects a value higher than the rising tone mode threshold voltage (2.35V typical) on the MIC pin, the CD326x enters tone mode. When the device transitions to tone mode while supplying voltages below the tone mode threshold voltage, the overshoot voltage from the supply temporarily pushes the MIC pin voltage above the threshold. Decreasing the ramp of the supply or reducing the supply voltage are both options to reduce the inrush current leading to this functionality.

Figure 7-5 shows the start-up sequence for when the CD326x enters tone mode. Upon entering tone more, the device opens the switch that connects the MIC and REM pins (Switch B). After a predetermined delay, the device shorts the VSHUNT pin and the MICPWR pin (Switch A). This functionality aids in preventing unwanted noise from the internal circuitry being mixed onto the microphone bias line. Following another predetermined delay, the CD326x sends an acknowledge tone sequence as described in Section 7.3.2.

When a microphone is biased and in use, the switch-resistor network used for button mode causes large DC level shifts in the bias voltage. This level shift can result in unwanted, audible clicks, pops, or de-biasing of the microphone. To prevent these results, when the CD326x enters tone mode, the CD326x disconnects the switch-resistor network from the microphone bias line, provides power to an external microphone through a shunt regulator, and engages a tone generation circuit. The TONE pin AC couples the tones onto the microphone bias

line for a specially enabled audio interface to interpret. Using the output from the MICPWR pin, the external microphone can be biased directly or through an external circuit as shown in Figure 8-1.

During a typical application where I_{MICPWR} falls between 120µA and 150µA, the MICPWR pin provides a voltage from 1.51V to 1.61V (1.56V typical, see V_{MICPWR}). Leaving the MICPWR pin floating or drawing current outside of these limits results in voltage exceeding the MICPWR output voltage specifications. Additionally, increasing the voltage on the MIC pin above 2.5V drives the MICPWR output voltage above 1.61V.

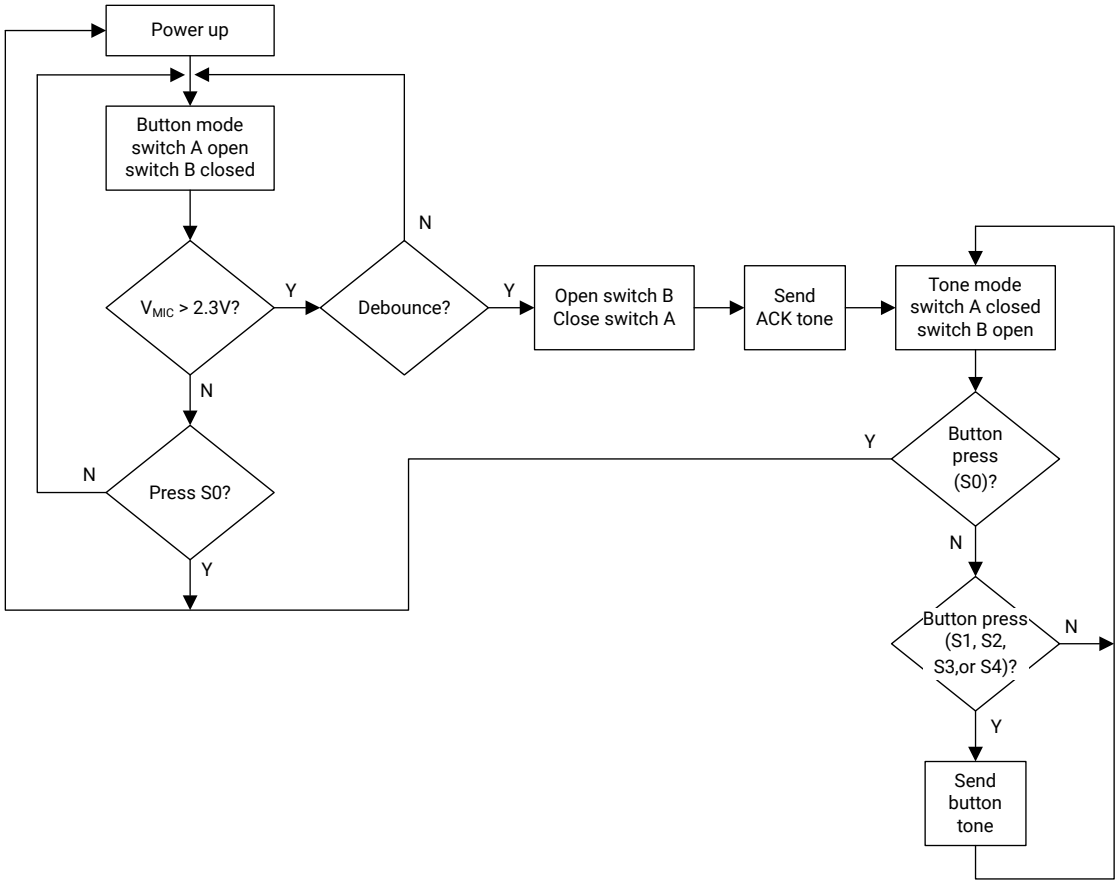


Figure 7-5. Tone Mode Power-up Sequence

For accuracy, the CD326x transmits two tones for each button press as shown in Figure 7-6. The first tone is enabled for a period of 0.9ms and is a calibration frequency. The second tone is enabled for a period of 1.8ms and is the unique frequency for the selected button. The specially enabled audio interface calculates the ratio of these two frequencies and translates the ratio into button press information. This functionality provides accurate results independent of clock frequency variation.

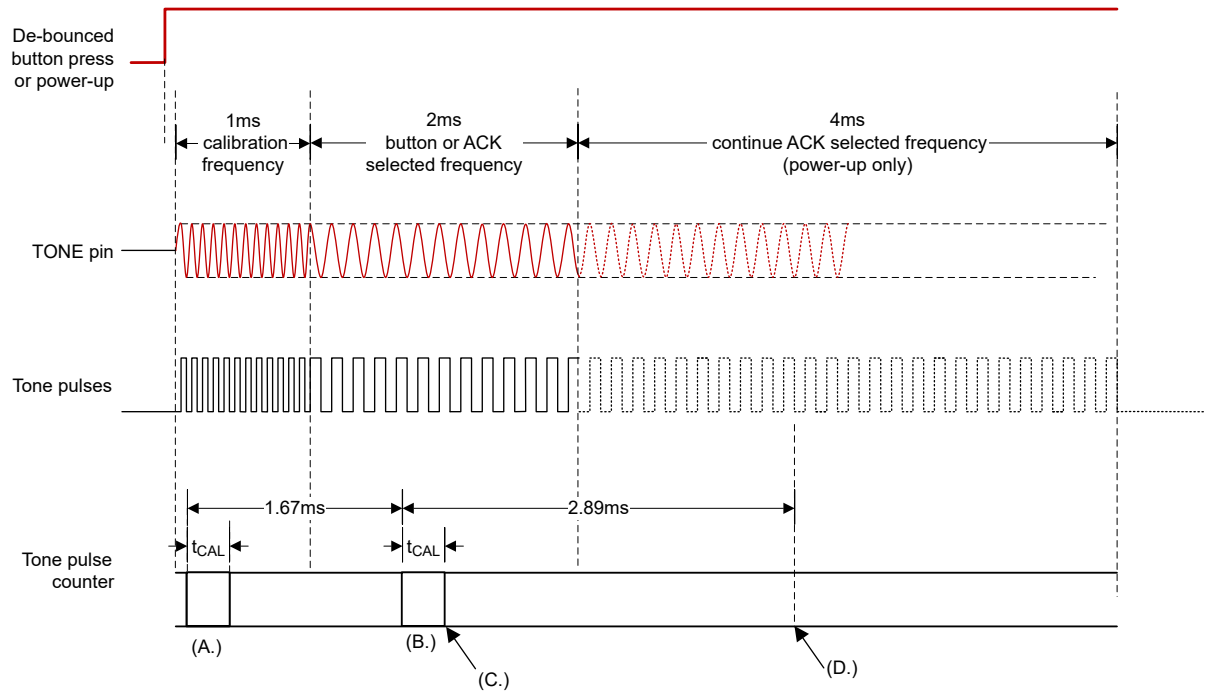


Figure 7-6. Tone Transmit and Decode Method

A. Count 63 tone pulses to set t_{CAL}.
B. Count *n* tone pulses over t_{CAL}.
C. Tone frequency decoded from *n* value.
D. Tone activity sampled. If active, ACK tone received. If not active, button tone received.

The CD326x remains in tone mode until the MIC pin voltage falls below 0.8V. When power recovers, the CD326x enters button mode or tone mode depending on the voltage detected at the MIC pin. See Section 7.3.4 for more details about this process.

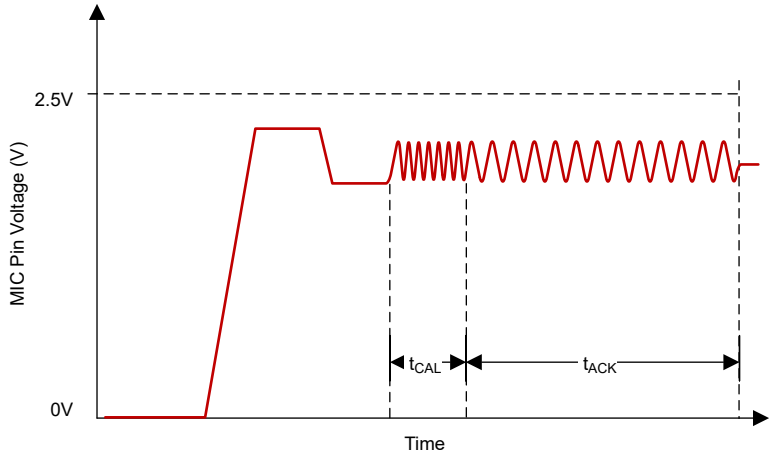


Figure 7-7. Tone Mode Acknowledge Timing

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The CD326x device is a highly efficient, small, and flexible wired headset signaling transmitter compatible with systems including a specially enabled audio interface. The design includes support for systems with and without a microphone while being compatible with up to four unique buttons.

8.2 Typical Application

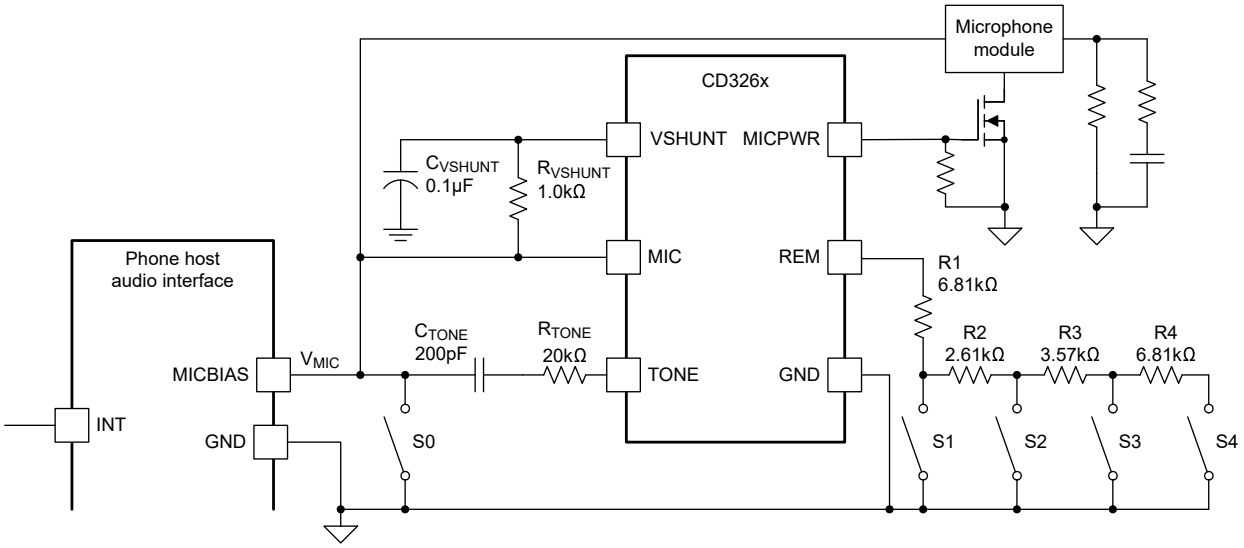


Figure 8-1. Typical Application

8.2.1 Design Requirements

Table 8-1. Typical Component Values

PARAMETER		VALUE	UNIT
C_{MIC}	MIC capacitor	10	µF
C_{VSHUNT}	VSHUNT capacitor	0.1	
C_{TONE}	TONE capacitor	200	pF
R_{MIC}	MIC resistor	1.0	kΩ
R_{VSHUNT}	VSHUNT resistor	1.0	
R_{TONE}	TONE resistor	20.0	
R1	S1 switch resistor	6.81	
R2	S2 switch resistor	2.61	
R3	S3 switch resistor	3.57	
R4	S4 switch resistor	6.81	

8.2.2 Application Curves

Figure 8-2 shows the tone generated from applying different resistance values on the REM pin. Applying and removing a resistance to the REM pin simulates a button press event which is detected by the CD326x. Recommended button resistor values can be found in Figure 7-4 and Section 5.5 (specifically button boundaries). Additionally, there are three sets of resistances between each band where either the generated tone is unstable, or where the device does not generate a tone (see Table 8-2).

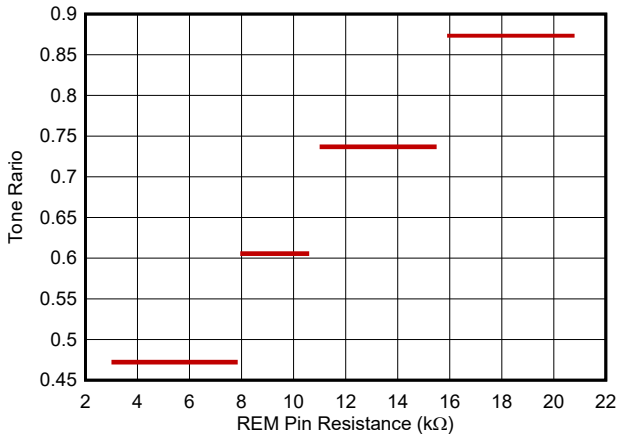


Figure 8-2. Generated Tone from REM Resistance Value

Table 8-2. Deadband Ranges

Button Transition		Deadband Range	
From	To	Low (kΩ)	High (kΩ)
Button 1	Button 2	7.85	7.95
Button 2	Button 3	10.60	11.00
Button 3	Button 4	15.50	15.90

For Figure 8-3 and Figure 8-4, active currents refer to the currents drawn by the VMIC and VSHUNT pins when a tone is being generated as part of tone mode operation.

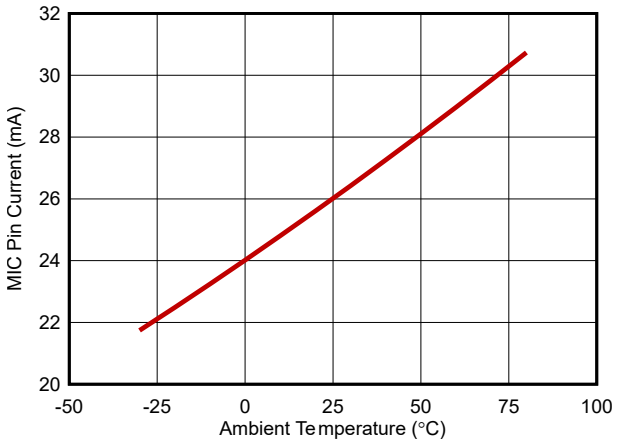


Figure 8-3. Active Current into MIC Pin vs Temperature

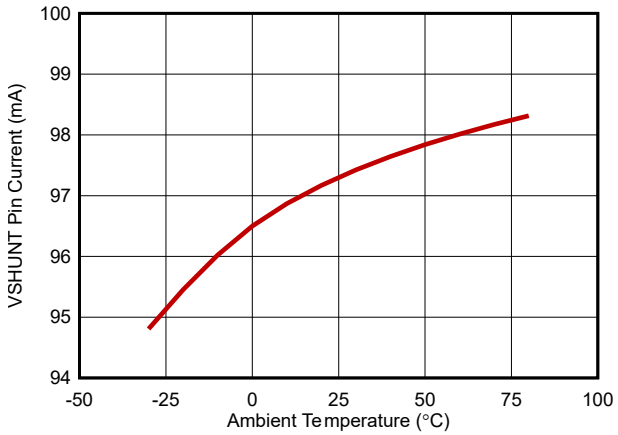


Figure 8-4. Active Current into VSHUNT Pin vs Temperature

8.3 Power Supply Recommendations

The power supply to the CD326x must have a current rating according to the supply voltage, output voltage, supply current, and output current of the CD326x.

8.4 Layout

8.4.1 Layout Guidelines

The system level performance metrics, including thermal performance, electromagnetic compliance (EMC), device reliability, and audio performance are all affected by the device and supporting component layout. The guidance provided in the applications section with regard to device and component selection can be followed by precise adherence to the layout guidance shown in the Section 8.4.2. This example represents an exemplary baseline balance of the engineering trade-offs involved with lying out the device. This design can be modified slightly as needed to meet the needs of a given application. In some applications, for instance, footprint size can be compromised to improve thermal performance through the use of additional contiguous copper neat the device. Conversely, EMI performance can be prioritized over thermal performance by routing on internal traces and incorporating a via picket-fence and additional filtering components. The recommended process is to start with the guidance shown in the Section 8.4.2 and work with TI field application engineers or through the E2E community to modify the layout based upon the application specific goals.

- See Figure 8-5 for the recommended layout of the CD326x, which is designed for common external GND connections. TI recommends placing all components as close as possible to the package pins. The recommended layout is implemented on the EVM and shown in the EVM user's guide.
- Provide low capacitive paths (with respect to all other nodes) for traces with high dv/dt. Therefore, the input and output capacitance must be placed as close as possible to the IC pins and parallel wiring over long distances as well as narrow traces must be avoided. Loops which conduct an alternating current must outline an area as small as possible, as this area is proportional to the energy radiated
- Use a ground plane with multiple vias for each terminal to create a low-impedance connection to GND for minimum ground noise.
- A single common GND plane is recommended to avoid a potential voltage difference between signals.
- When placing decoupling capacitors, especially for the VSHUNT pin, place the capacitors as close to the device as possible. Typically recommended capacitor is 0.1µF.

8.4.2 Layout Example

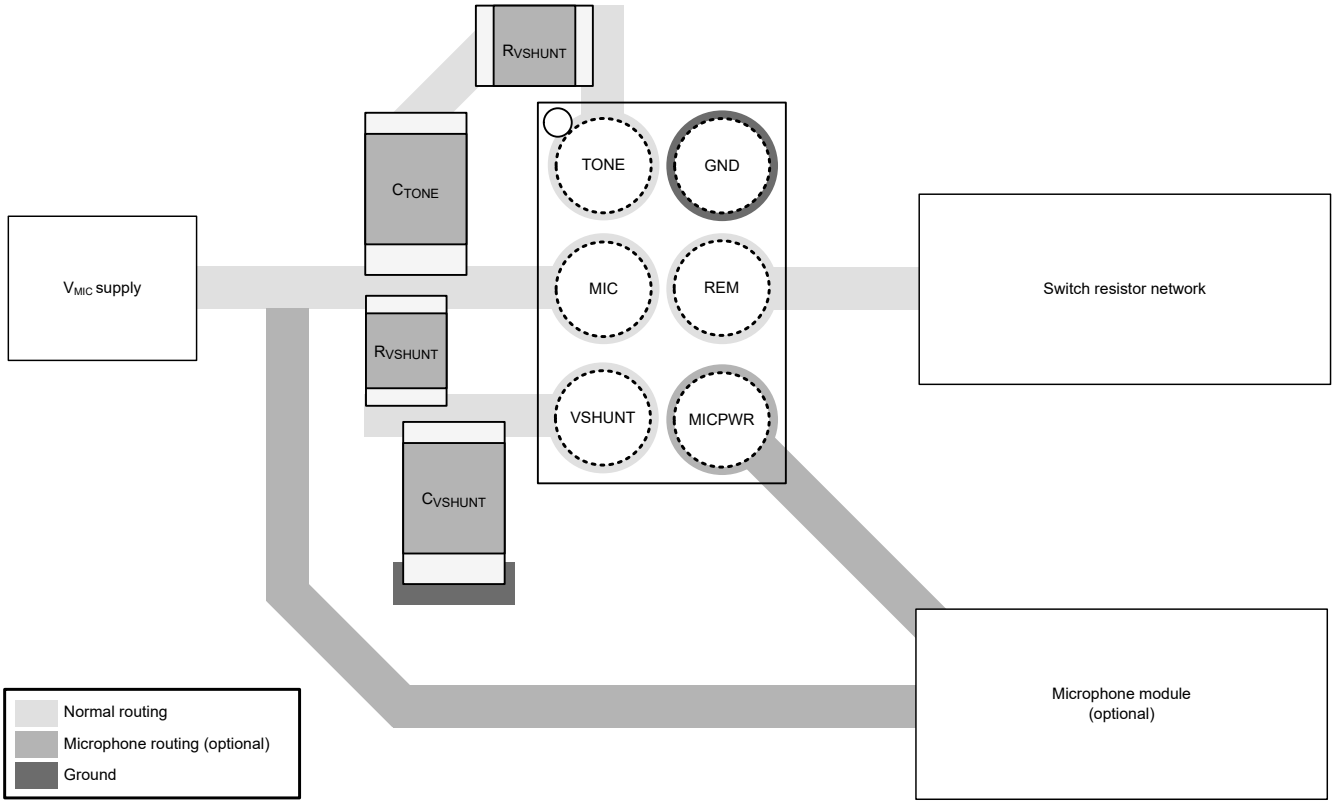


Figure 8-5. Layout Example

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Device Support

9.1.1 Third-Party Products Disclaimer

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9.1.2 Development Support

For development support on this product, see the following:

- Chapter 54: *Headset Remote and Microphone Transmitter* in Accessory Design Guidelines for Apple Devices from the Apple Development Page

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
May 2025	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

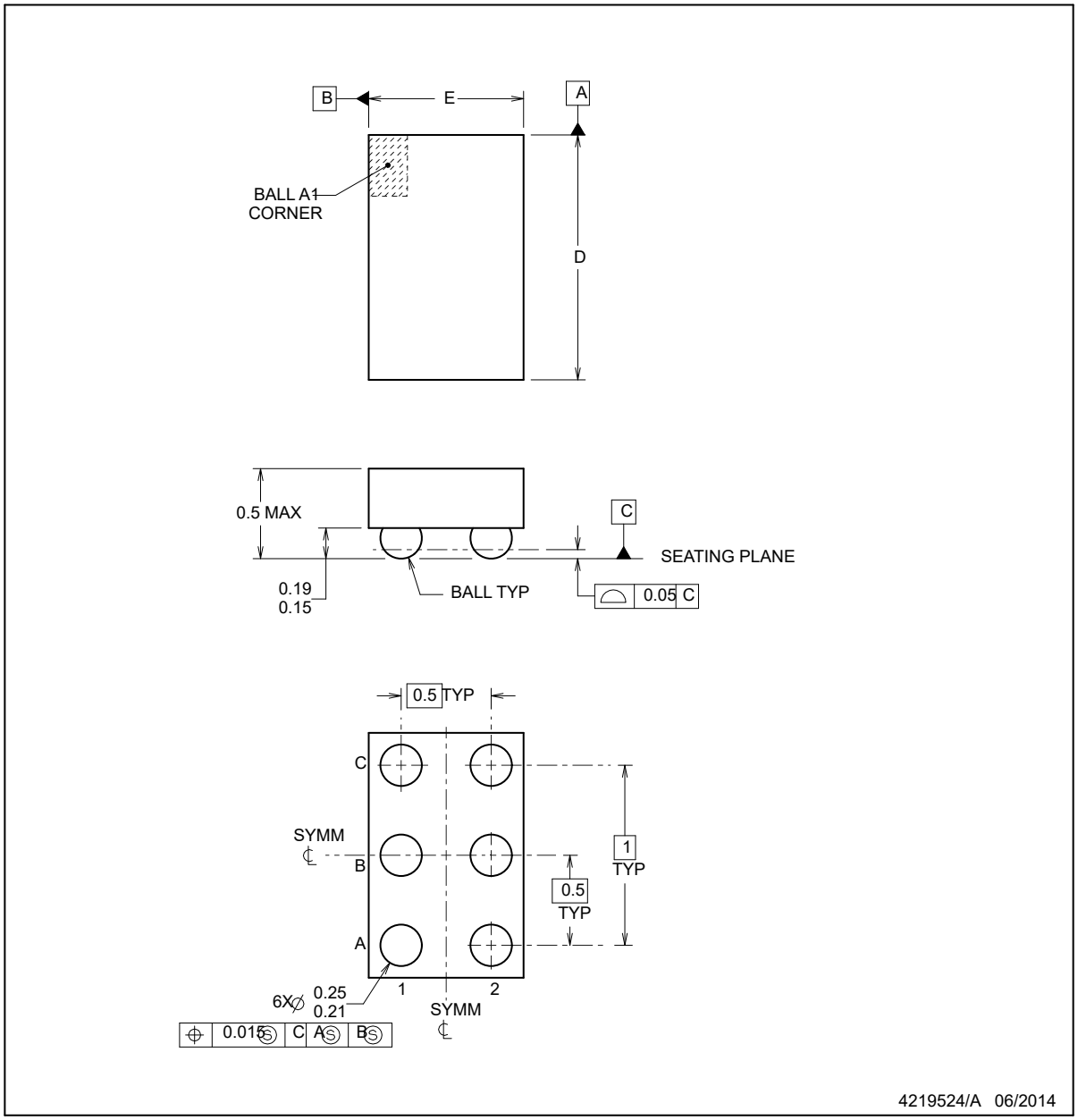
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

NanoFree Is a trademark of Texas Instruments.

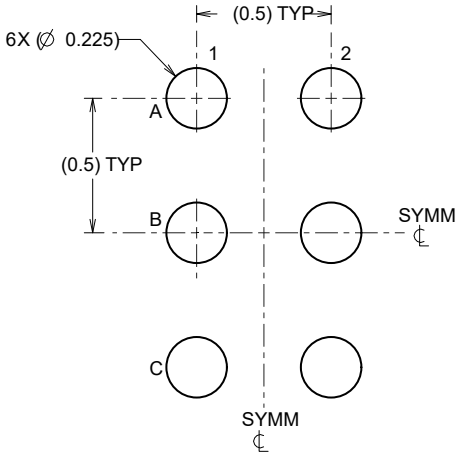
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree ™ package configuration.

EXAMPLE BOARD LAYOUT

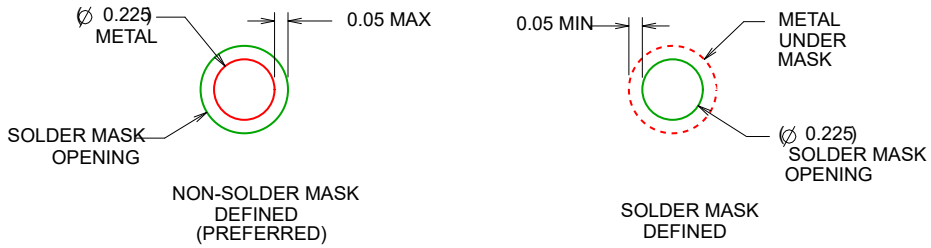
YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

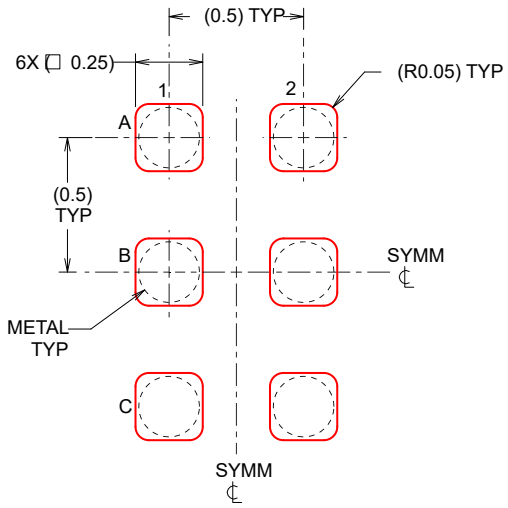
4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).

EXAMPLE STENCIL DESIGN

YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219524/A 06/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD3268A0YZPR	Active	Production	DSBGA (YZP) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(4H3, 4H5)
CD3269A0YZPR	Active	Production	DSBGA (YZP) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(4J3, 4J5)

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

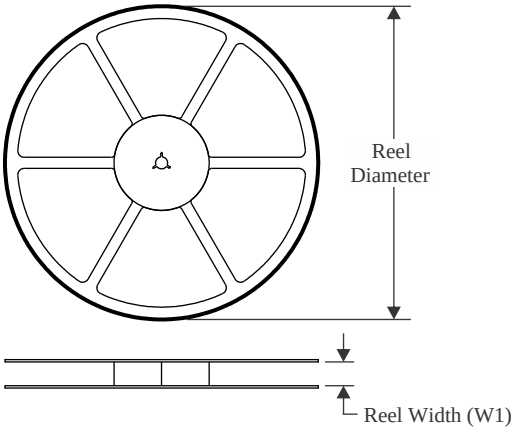
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

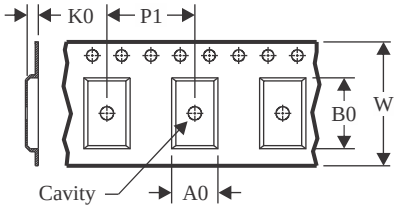
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

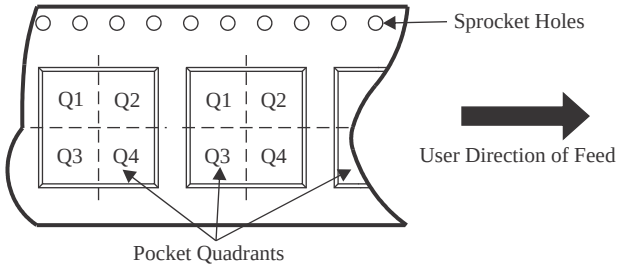


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

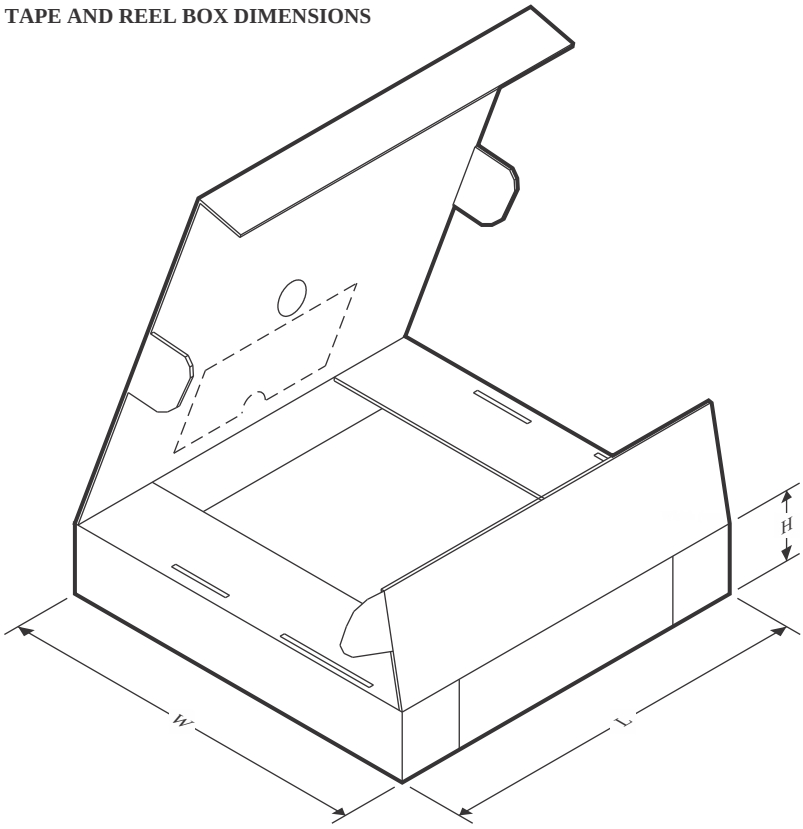
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD3268A0YZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1
CD3269A0YZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

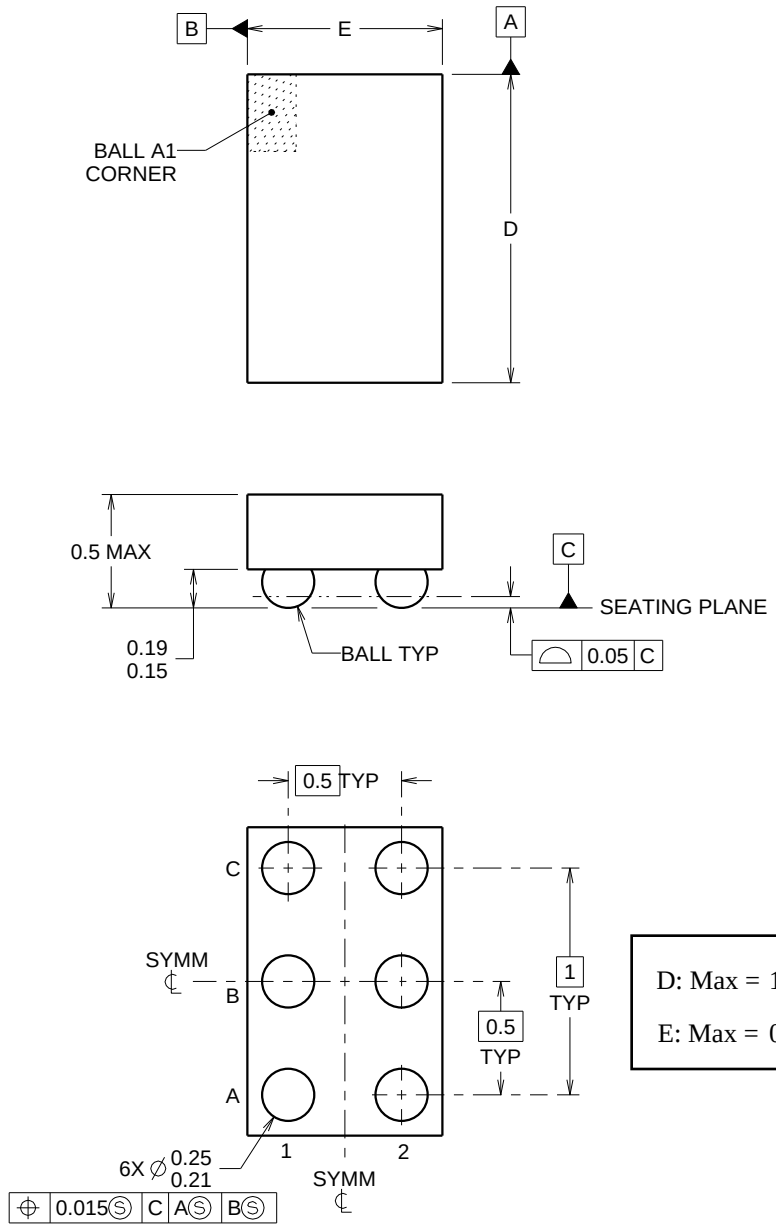
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD3268A0YZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0
CD3269A0YZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0

PACKAGE OUTLINE

YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 1.418 mm, Min =1.358 mm

E: Max = 0.918 mm, Min =0.858 mm

4219524/A 06/2014

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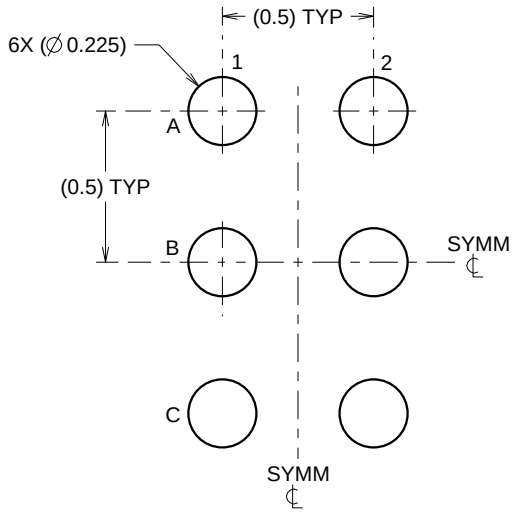
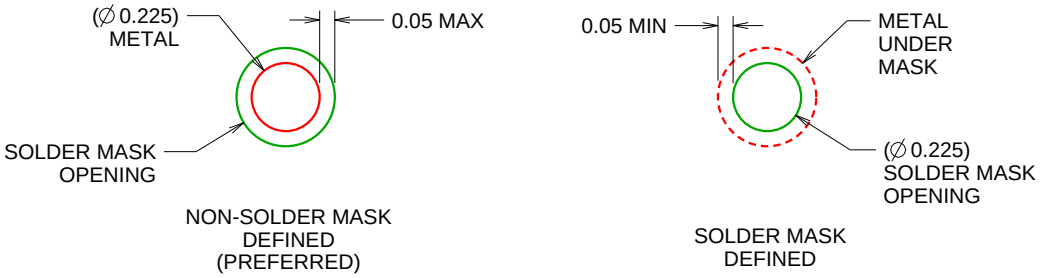
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.



LAND PATTERN EXAMPLE
SCALE:40X

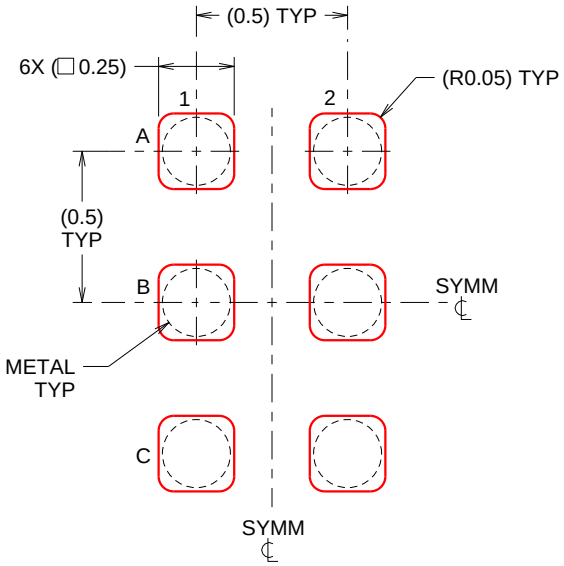


SOLDER MASK DETAILS
NOT TO SCALE

4219524/A 06/2014

NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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