

CD4031B Types

CMOS 64-Stage Static Shift Register

High-Voltage Types (20-Volt Rating)

■ CD4031B is a static shift register that contains 64 D-type, master-slave flip-flop stages and one stage which is a D-type master flip-flop only (referred to as a 1/2 stage).

The logic level present at the DATA input is transferred into the first stage and shifted one stage at each positive-going clock transition. Maximum clock frequencies up to 12 Megahertz (typical) can be obtained. Because fully static operation is allowed, information can be permanently stored with the clock line in either the low or high state. The CD4031B has a MODE CONTROL input that, when in the high state, allows operation in the recirculating mode. The MODE CONTROL input can also be used to select between two separate data sources. Register packages can be cascaded and the clock lines driven directly for high-speed operation. Alternatively, a delayed clock output (CL_D) is provided that enables cascading register packages while allowing reduced clock drive fan-out and transition-time requirements. A third cascading option makes use of the Q' output from the 1/2 stage, which is available on the next negative-going transition of the clock after the Q output occurs. This delayed output, like the delayed clock CL_D, is used with clocks having slow rise and fall times.

The CD4031B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (NSR suffix), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

Voltages referenced to V_{SS} Terminal) -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS -0.5V to V_{DD}+0.5V

DC INPUT CURRENT, ANY ONE INPUT ±10mA

POWER DISSIPATION PER PACKAGE (P_D):

For T_A = -55°C to +100°C 500mW

For T_A = +100°C to +125°C Derate Linearly at 12mW/°C to 200mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW

OPERATING-TEMPERATURE RANGE (T_A) -55°C to +125°C

STORAGE TEMPERATURE RANGE (T_{stg}) -65°C to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max +265°C

Features:

■ Fully static operation: DC to 12 MHz typ. @ V_{DD}-V_{SS} = 15 V

■ Standard TTL drive capability on Q output

■ Recirculation capability

■ Three cascading modes:

Direct clocking for high-speed operation

Delayed clocking for reduced clock drive requirements

Additional 1/2 stage for slow clocks

■ 100% tested for quiescent current at 20 V

■ Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C

■ Noise margin (over full package-temperature range)

1 V at V_{DD} = 5 V

2 V at V_{DD} = 10 V

2.5 V at V_{DD} = 15 V

■ 5-V, 10-V, and 15-V parametric ratings

■ Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

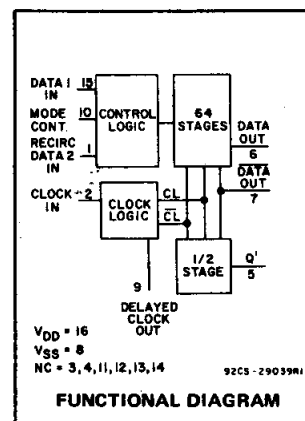
■ Serial shift registers

■ Time delay circuits

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T _A =Full Package-Temperature Range)	3	18	V



INPUT CONTROL CIRCUIT TRUTH TABLE

DATA	RECIRC.	MODE	BIT INTO STAGE 1
1	X	0	1
0	X	0	0
X	1	1	1
X	0	1	0

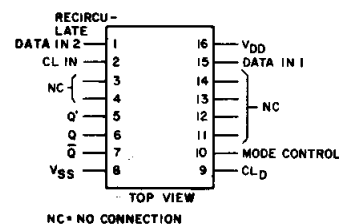
TYPICAL STAGE TRUTH TABLE

Data	CL	Data + 1
0		0
1		1
X		NC

TRUTH TABLE FOR OUTPUT FROM Q' (TERMINAL 5)

Data + 64	CL	Data + 64½
0		0
1		1
X		NC

1 = HIGH LEVEL 0 = LOW LEVEL
X = DON'T CARE NC = NO CHANGE



TERMINAL ASSIGNMENT

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STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS	
	V _O (V)	V _{IN} (V)	V _{DD} (V)	-55	-40	+85	+125	+25				
								Min.	Typ.	Max.		
Quiescent Device Current, I _{DD} Max.	—	0.5	5	5	5	150	150	—	0.04	5	μA	
	—	0.10	10	10	10	300	300	—	0.04	10		
	—	0.15	15	20	20	600	600	—	0.04	20		
	—	0.20	20	100	100	3000	3000	—	0.08	100		
Output Low (Sink) Current I _{OL} Min. Q	0.4	0.5	5	2.56	2.44	1.68	1.44	2.04	4	—	mA	
	0.5	0.10	10	6.4	6	4.4	3.6	5.2	10.4	—		
	1.5	0.15	15	16.8	16	11.2	9.6	13.6	27.2	—		
Q̄, Q', CL _D	0.4	0.5	5	0.64	0.61	0.42	0.36	0.51	1	—		
	0.5	0.10	10	1.6	1.5	1.1	0.9	1.3	2.6	—		
	1.5	0.15	15	4.2	4	2.8	2.4	3.4	6.8	—		
Output High (Source) Current, I _{OH} Min. Q, Q̄, Q', CL _D	4.6	0.5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	—	mA	
	2.5	0.5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—		
	9.5	0.10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—		
	13.5	0.15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	—		
Output Voltage: Low-Level, V _{OL} Max.	—	0.5	5	0.05			—			0	0.05	V
	—	0.10	10	0.05			—			0	0.05	
	—	0.15	15	0.05			—			0	0.05	
Output Voltage: High-Level, V _{OH} Min.	—	0.5	5	4.95			4.95			5	—	V
	—	0.10	10	9.95			9.95			10	—	
	—	0.15	15	14.95			14.95			15	—	
Input Low Voltage V _{IL} Max.	0.5, 4.5	—	5	1.5			—			—	1.5	V
	1.9	—	10	3			—			—	3	
	1.5, 13.5	—	15	4			—			—	4	
Input High Voltage, V _{IH} Min.	0.5, 4.5	—	5	3.5			3.5			—	—	V
	1.9	—	10	7			7			—	—	
	1.5, 13.5	—	15	11			11			—	—	
Input Current I _{IN} Max.		0.18	18	±0.1	±0.1	±1	±1	—	±10 ⁻⁵	±0.1	μA	

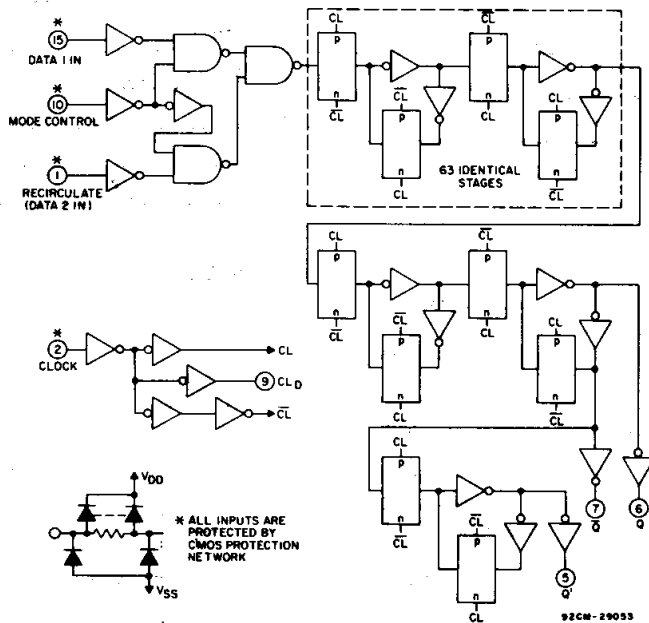


Fig. 1 — Logic diagram.

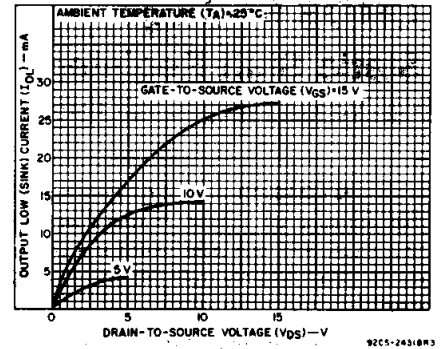


Fig. 2 — Typical output low (sink) current characteristics (I_{OL} sink current = 4X ordinate).

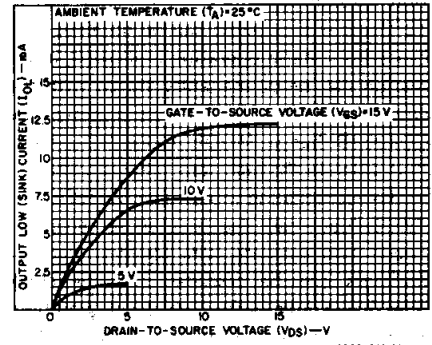


Fig. 3 — Minimum output low (sink) current characteristics (I_{OL} sink current = 4X ordinate).

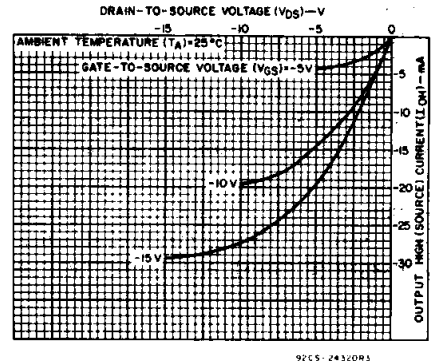


Fig. 4 — Typical output high (source) current characteristics.

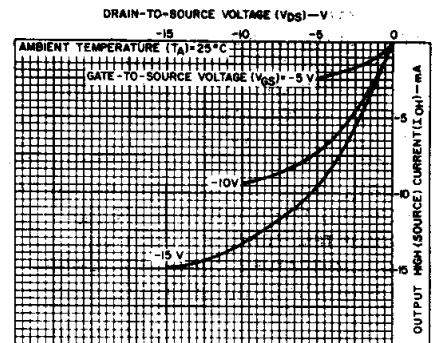


Fig. 5 — Minimum output high (source) current characteristics.

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DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$; Input $t_r, t_f = 20\text{ ns}$,
 $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
	$V_{DD}(\text{V})$	Min.	Typ.	Max.	
Propagation Delay Time: Clock to $\bar{Q}$, t_{PHL} , t_{PLH} ; Clock to Q, t_{PLH}	5	—	250	500	ns
	10	—	110	220	
	15	—	90	180	
Clock to Q' , t_{PHL} , t_{PLH} ; Clock to Q, t_{PHL}	5	—	190	380	ns
	10	—	80	160	
	15	—	65	130	
Clock to CL_D	5	—	100	200	ns
	10	—	50	100	
	15	—	40	80	
Transition Time, t_{THL} , t_{TLH} (Any Output, except Q, t_{THL})	5	—	100	200	ns
	10	—	50	100	
	15	—	40	80	
Q, t_{THL}	5	—	50	100	ns
	10	—	25	50	
	15	—	20	40	
Minimum Data Setup Time, t_S	5	—	30	60	ns
	10	—	15	30	
	15	—	10	20	
Minimum Data Hold Time, t_H	5	—	30	60	ns
	10	—	15	30	
	15	—	10	20	
Minimum Clock Pulse Width, t_W	5	—	120	240	ns
	10	—	50	100	
	15	—	40	80	
Maximum Clock Input Frequency, f_{CL}^{**}	5	2	4	—	MHz
	10	5	10	—	
	15	6	12	—	
Clock Input Rise or Fall Time, t_{rCL} , t_{fCL}^*	5	—	—	1000	μs
	10	—	—	1000	
	15	—	—	200	
Input Capacitance, C_{IN} (Any Input)	—	—	5	7.5	pF

*If more than one unit is cascaded in the parallel clocked application, t_{rCL} should be made less than or equal to the sum of the propagation delay at 50 pF and the transition time of the output driving stage.

**Maximum Clock Frequency for Cascaded Units;

a) Using Delayed Clock Feature in Recirculation Mode:

$$f_{\max} = \frac{1}{(n-1) CL_D \text{ prop. delay} + Q \text{ prop. delay} + \text{set-up time}} \quad \text{where } n = \text{number of packages}$$

b) Not Using Delayed Clock:

$$f_{\max} = \frac{1}{\text{propagation delay} + \text{set-up time}}$$

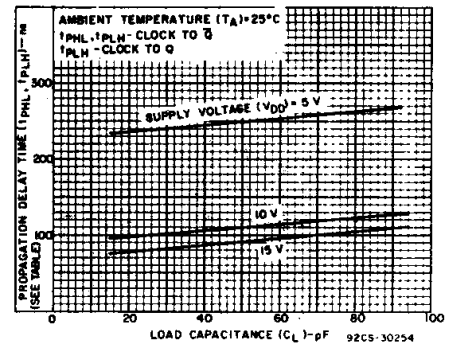


Fig. 6 — Typical propagation delay time as a function of load capacitance (see table).

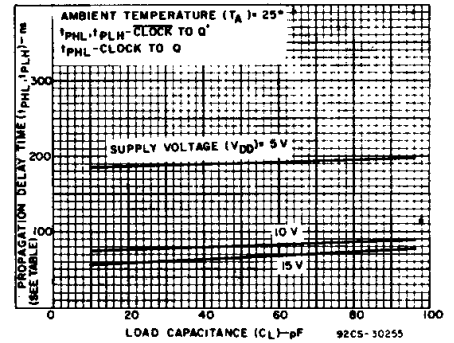


Fig. 7 — Typical propagation delay time as a function of load capacitance (see table).

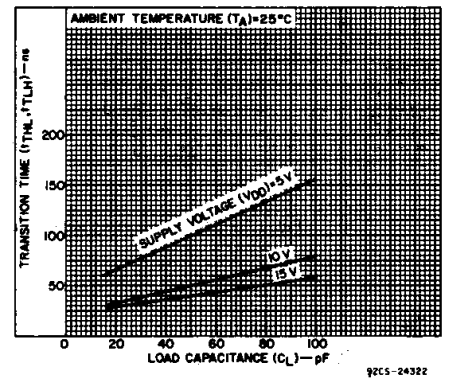


Fig. 8 — Typical transition time as a function of load capacitance (except Q, t_{THL}).

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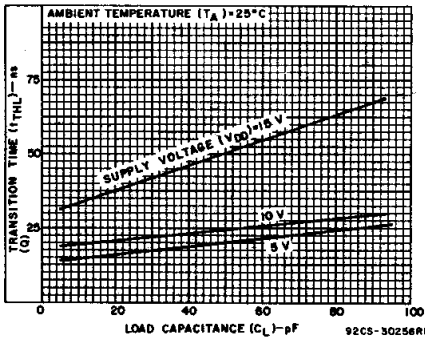


Fig. 9 - Typical transition time as a function of load capacitance (Q , t_{TL}).

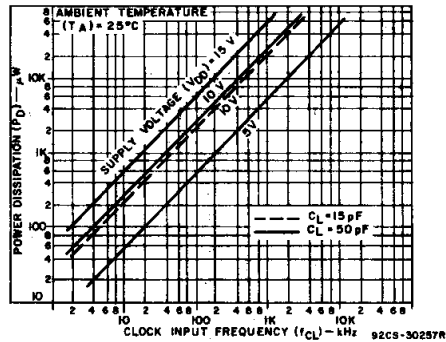


Fig. 10 - Typical dynamic power dissipation as a function of clock input frequency.

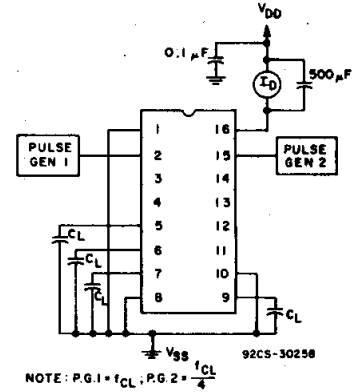


Fig. 11 - Dynamic power dissipation test circuit.

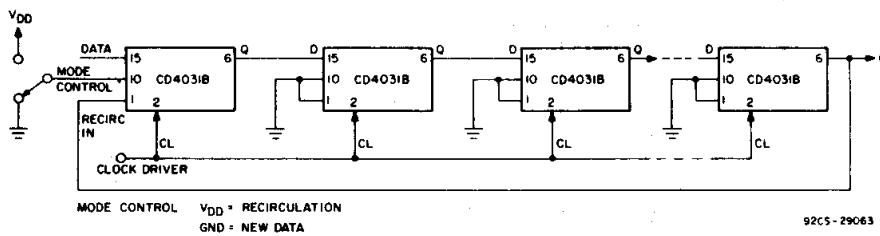


Fig. 12 - Cascading using direct clocking for high-speed operation (see clock rise and fall time requirement).

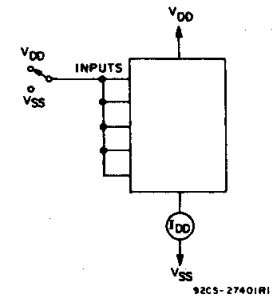


Fig. 13 - Quiescent-device-current test circuit.

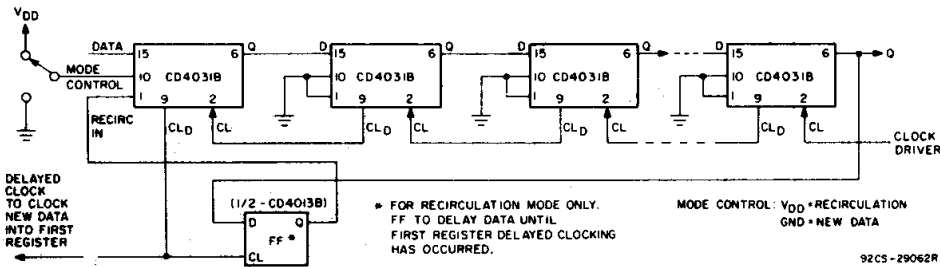


Fig. 14 - Cascading using delayed clocking for reduced clock drive requirements.

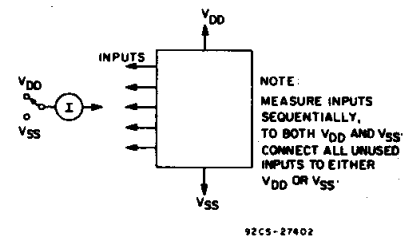


Fig. 15 - Input-leakage current.

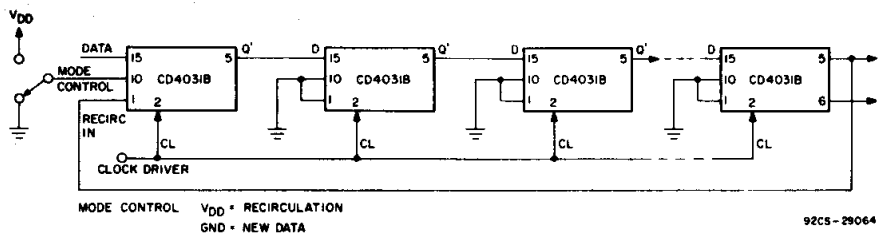


Fig. 16 - Cascading using half-clock-pulse delayed data output (Q') to permit use of slow rise and fall time clock inputs.

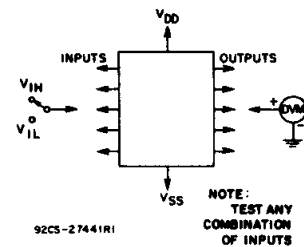
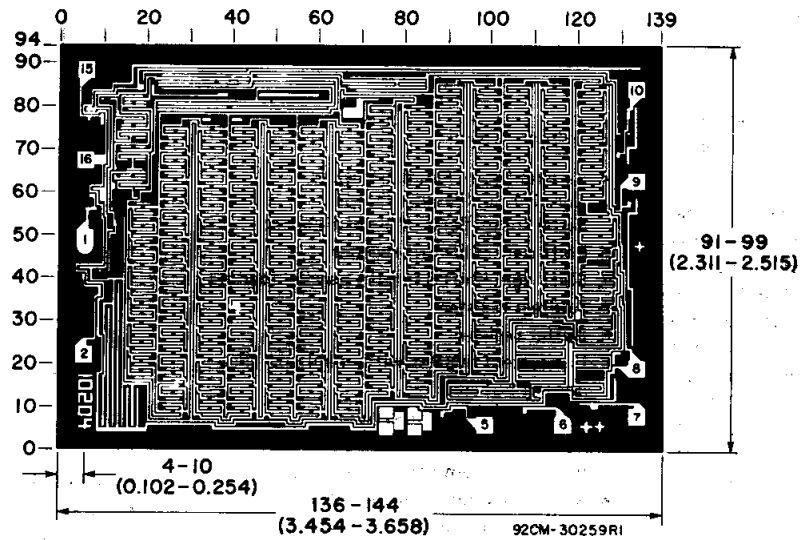


Fig. 17 - Input-voltage test circuit.

CD4031B Types



Chip dimensions and pad layout for CD4031B

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD4031BE	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4031BE
CD4031BE.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4031BE
CD4031BF3A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4031BF3A
CD4031BF3A.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4031BF3A
CD4031BPW	Obsolete	Production	TSSOP (PW) 16	-	-	Call TI	Call TI	-55 to 125	CM031B
CD4031BPWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM031B
CD4031BPWR.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM031B

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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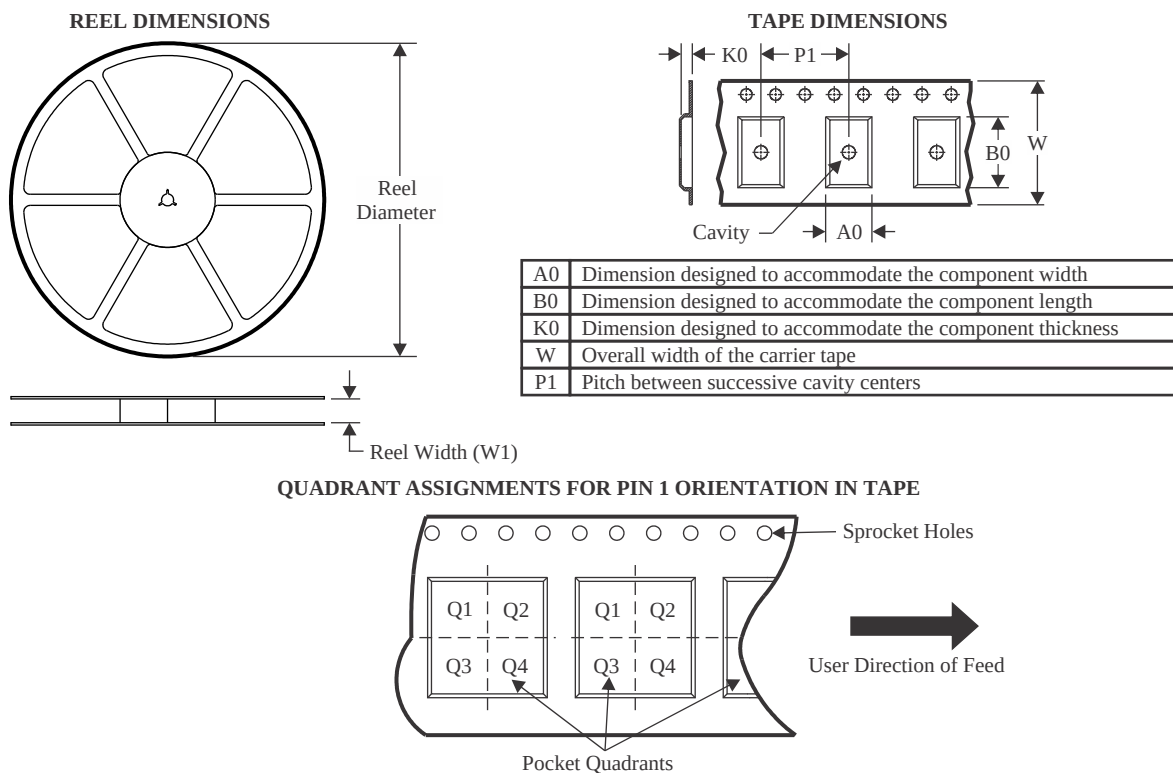
OTHER QUALIFIED VERSIONS OF CD4031B, CD4031B-MIL :

- Catalog : [CD4031B](#)
- Military : [CD4031B-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

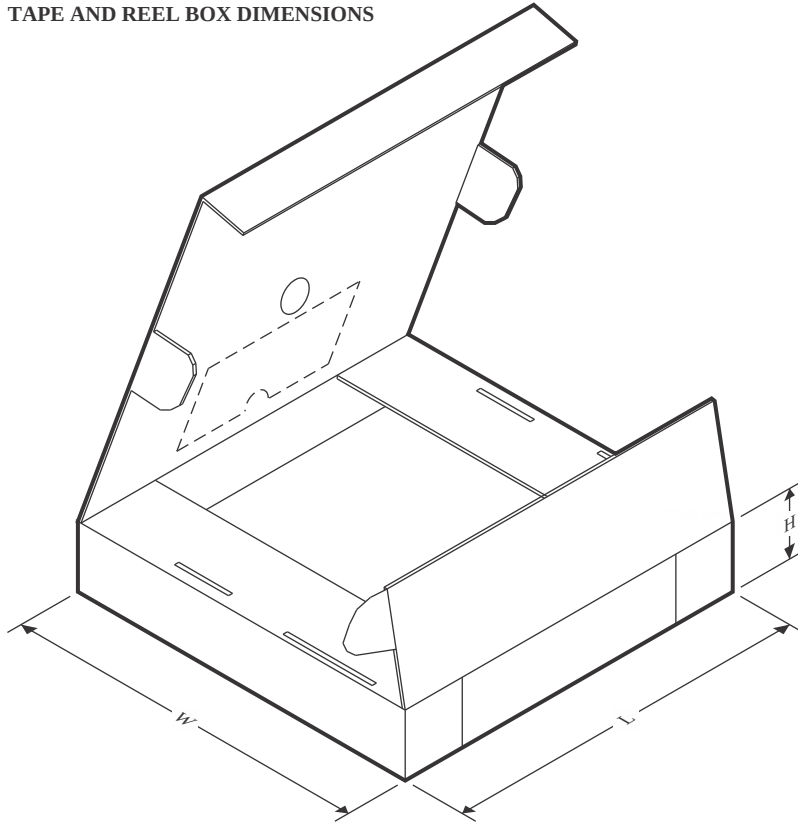
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4031BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



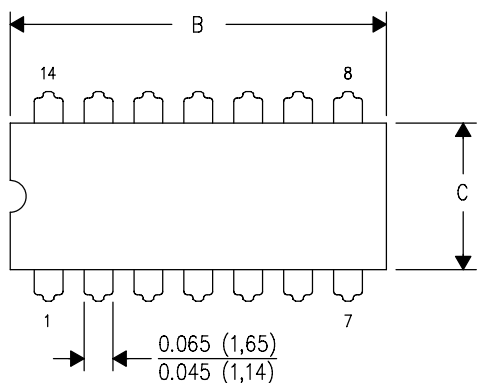
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4031BPWR	TSSOP	PW	16	2000	353.0	353.0	32.0

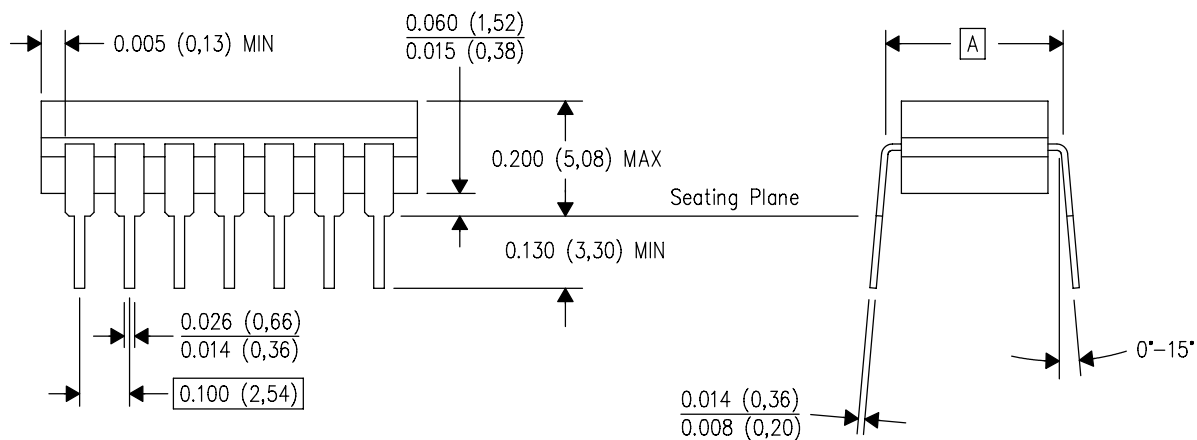
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE

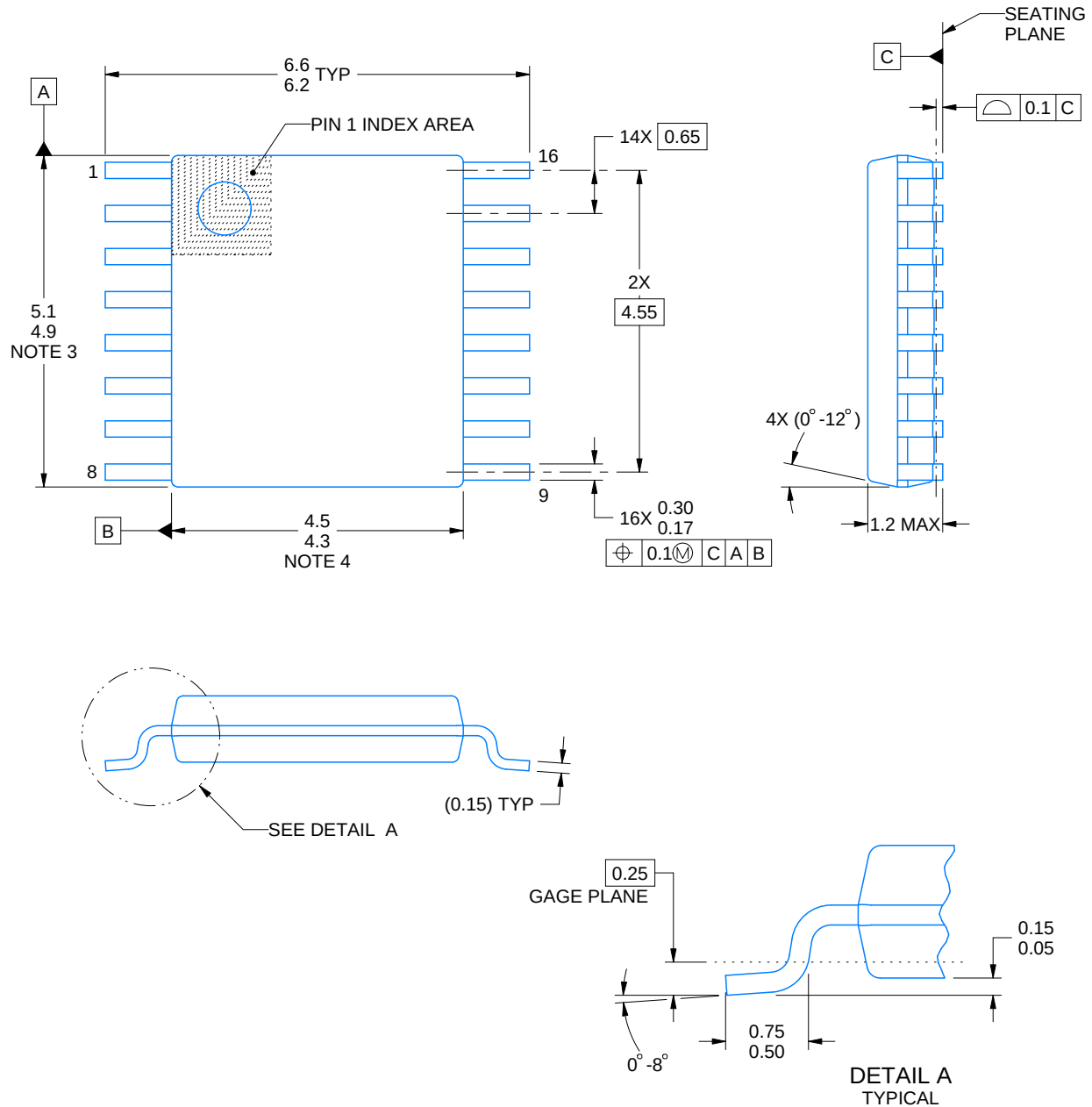
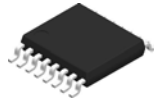


PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.



4220204/B 12/2023

NOTES:

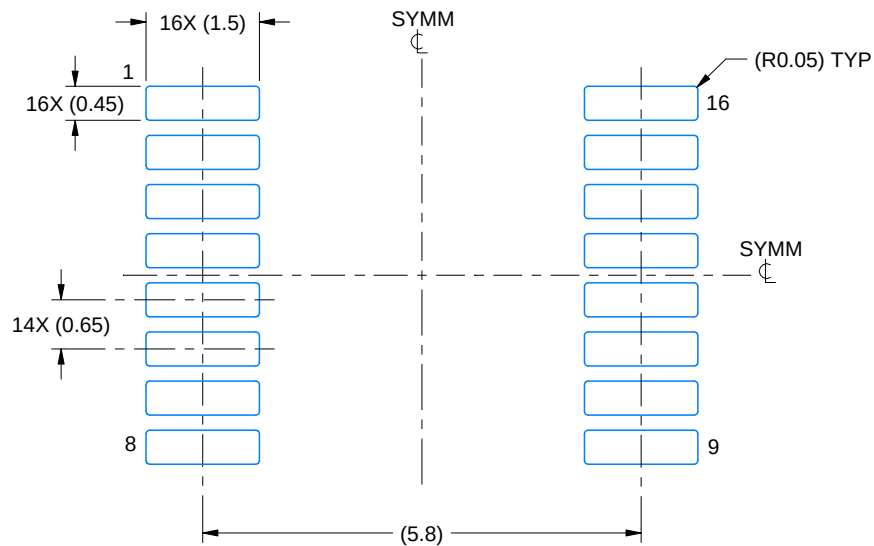
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

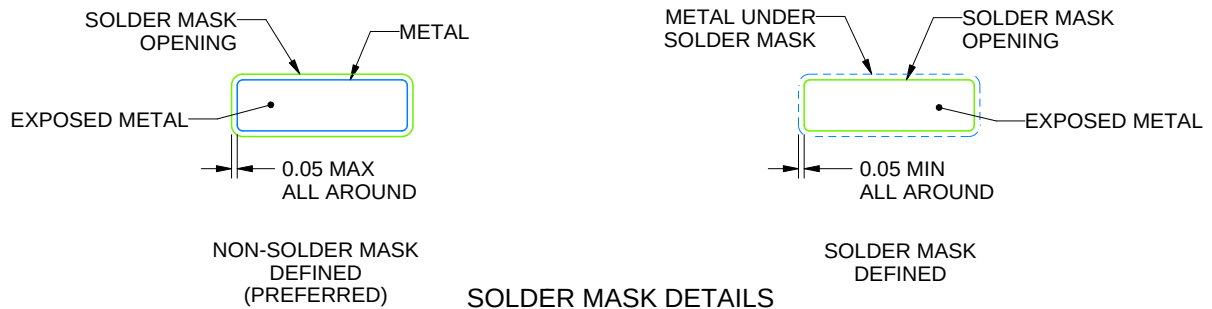
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

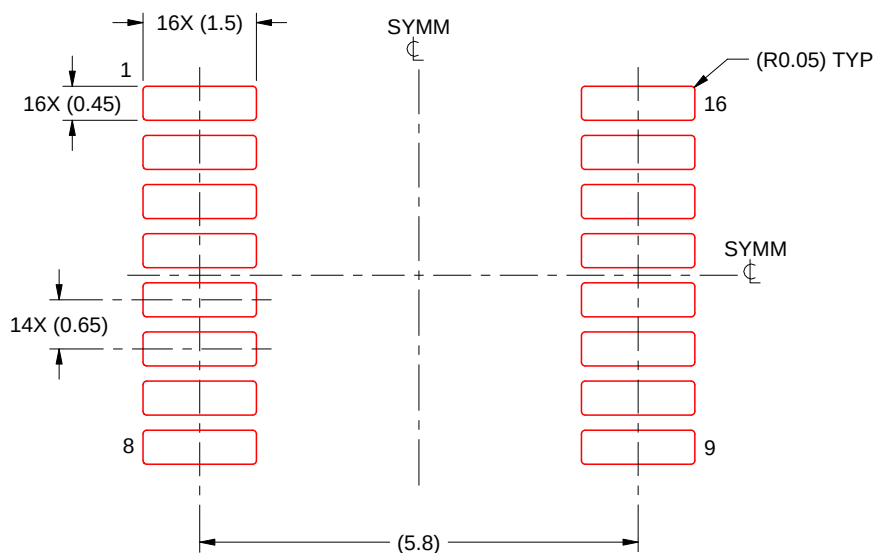
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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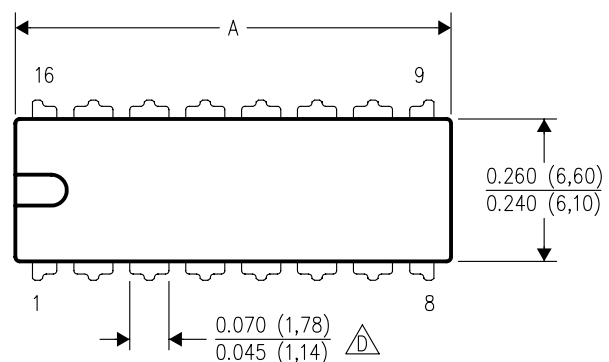
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

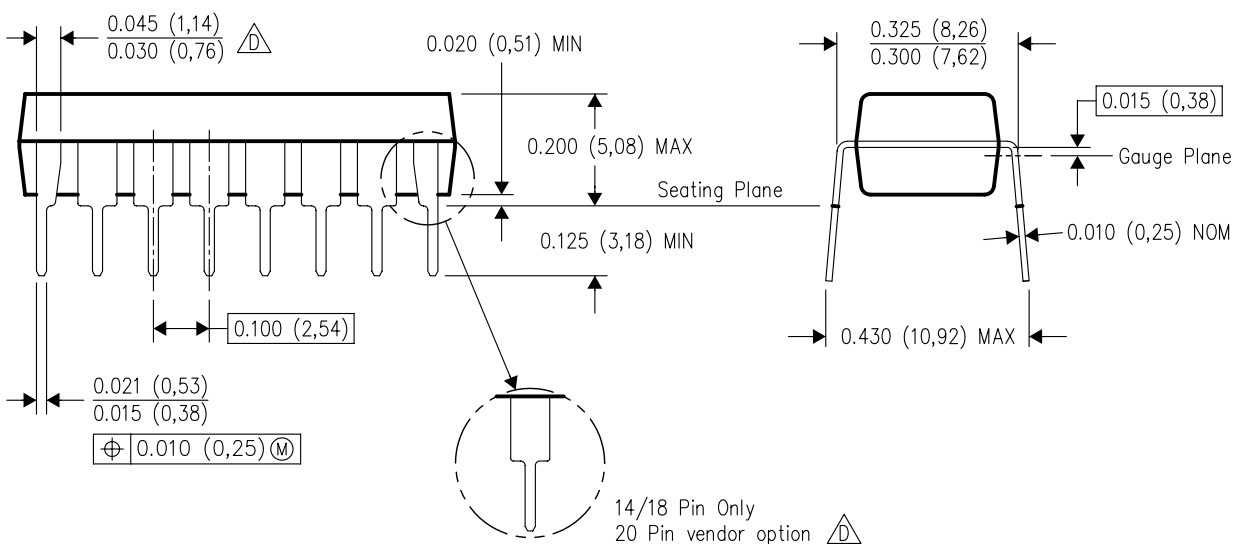
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



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- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 -  The 20 pin end lead shoulder width is a vendor option, either half or full width.

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