

CD4098B Types

CMOS Dual Monostable Multivibrator

High-Voltage Types (20-Volt Rating)

■ CD4098B dual monostable multivibrator provides stable retriggerable/resettable one-shot operation for any fixed-voltage timing application.

An external resistor (R_X) and an external capacitor (C_X) control the timing for the circuit. Adjustment of R_X and C_X provides a wide range of output pulse widths from the Q and $\bar{Q}$ terminals. The time delay from trigger input to output transition (trigger propagation delay) and the time delay from reset input to output transition (reset propagation delay) are independent of R_X and C_X .

Leading-edge-triggering (+TR) and trailing-edge-triggering (–TR) inputs are provided for triggering from either edge of an input pulse. An unused +TR input should be tied to V_{SS} . An unused –TR input should be tied to V_{DD} . A RESET (on low level) is provided for immediate termination of the output pulse or to prevent output pulses when power is turned on. An unused RESET input should be tied to V_{DD} . However, if an entire section of the CD4098B is not used, its RESET should be tied to V_{SS} . See Table I.

In normal operation the circuit triggers (extends the output pulse one period) on the application of each new trigger pulse. For operation in the non-retriggerable mode, $\bar{Q}$ is connected to –TR when leading-edge triggering (+TR) is used or Q is connected to +TR when trailing-edge triggering (–TR) is used.

The time period (T) for this multivibrator can be approximated by: $T_X = \frac{1}{2} R_X C_X$ for $C_X \geq 0.01 \mu F$. Time periods as a function of R_X for values of C_X and V_{DD} are given in Fig. 8. Values of T vary from unit to unit and as a function of voltage, temperature, and $R_X C_X$.

The minimum value of external resistance, R_X , is 5 k Ω . The maximum value of external capacitance, C_X , is 100 μF . Fig. 9 shows time periods as a function of C_X for values of R_X and V_{DD} .

The output pulse width has variations of $\pm 2.5\%$ typically, over the temperature range of $-55^\circ C$ to $125^\circ C$ for $C_X = 1000$ pF and $R_X = 100$ k Ω .

For power supply variations of $\pm 5\%$, the output pulse width has variations of $\pm 0.5\%$ typically, for $V_{DD} = 10$ V and 15 V and $\pm 1\%$ typically, for $V_{DD} = 5$ V at $C_X = 1000$ pF and $R_X = 5$ k Ω .

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, and MT suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

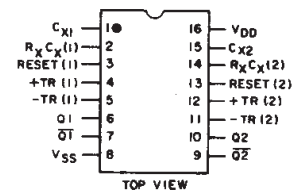
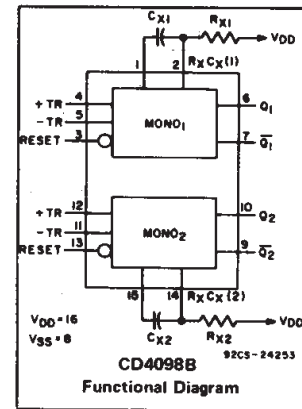
The CD4098B is similar to type MC14528.

Features:

- Retriggerable/resettable capability
- Trigger and reset propagation delays independent of R_X , C_X
- Triggering from leading or trailing edge
- Q and $\bar{Q}$ buffered outputs available
- Separate resets
- Wide range of output-pulse widths
- 100% tested for maximum quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and $25^\circ C$
- Noise margin (full package-temperature range):
 - 1 V at $V_{DD} = 5$ V
 - 2 V at $V_{DD} = 10$ V
 - 2.5 V at $V_{DD} = 15$ V
- 5-V, 10-V, and 15-V parametric ratings
- Standardized, symmetrical output characteristics
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices."

Applications:

- Pulse delay and timing
- Pulse shaping
- Astable multivibrator



TERMINALS 1, 8, 15 ARE
ELECTRICALLY CONNECTED
INTERNALLY

92CS-24648R1

TERMINAL ASSIGNMENT

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

Voltages referenced to V_{SS} Terminal)

–0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS

–0.5V to $V_{DD} + 0.5$ V

DC INPUT CURRENT, ANY ONE INPUT

± 10 mA

POWER DISSIPATION PER PACKAGE (P_D):

For $T_A = -55^\circ C$ to $+100^\circ C$

500 mW

For $T_A = +100^\circ C$ to $+125^\circ C$

Derate Linearly at 12 mW/ $^\circ C$ to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR $T_A =$ FULL PACKAGE-TEMPERATURE RANGE (All Package Types)

100 mW

OPERATING-TEMPERATURE RANGE (T_A)

$-55^\circ C$ to $+125^\circ C$

STORAGE TEMPERATURE RANGE (T_{stg})

$-65^\circ C$ to $+150^\circ C$

LEAD TEMPERATURE (DURING SOLDERING):

At distance $1/16 \pm 1/32$ inch (1.59 ± 0.79 mm) from case for 10 s max

$+265^\circ C$

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} V	LIMITS		UNITS
		MIN.	MAX.	
Supply-Voltage Range (For $T_A =$ Full Package-Temperature Range)	–	3	18	V
Trigger Pulse Width $t_W(TR)$	5 10 15	140 60 40	– – –	ns
Reset Pulse Width $t_W(R)$ (This is a function of C_X)	–	See Dynamic Char. Chart and Fig. 10		–
Trigger Rise or Fall Time $t_r(TR)$, $t_f(TR)$	5–15	–	100	μs

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TABLE I

CD4098B FUNCTIONAL TERMINAL CONNECTIONS

FUNCTION	V _{DD} TO TERM. NO.		V _{SS} TO TERM. NO.		INPUT PULSE TO TERM. NO.		OTHER CONNECTIONS	
	MONO ₁	MONO ₂	MONO ₁	MONO ₂	MONO ₁	MONO ₂	MONO ₁	MONO ₂
Leading-Edge Trigger/Retriggerable	3, 5	11, 13			4	12		
Leading-Edge Trigger/Non-retriggerable	3	13			4	12	5-7	11-9
Trailing-Edge Trigger/Retriggerable	3	13	4	12	5	11		
Trailing-Edge Trigger/Non-retriggerable	3	13			5	11	4-6	12-10
Unused Section	5	11	3, 4	12, 13				

NOTES:

1. A RETRIGGERABLE ONE-SHOT MULTIVIBRATOR HAS AN OUTPUT PULSE WIDTH WHICH IS EXTENDED ONE FULL TIME PERIOD (T_X) AFTER APPLICATION OF THE LAST TRIGGER PULSE.

The minimum time between retriggering edges (or trigger and retrigger edges) is 40 per cent of (T_X).

2. A NON-RETRIGGERABLE ONE-SHOT MULTIVIBRATOR HAS A TIME PERIOD T_X REFERENCED FROM THE APPLICATION OF THE FIRST TRIGGER PULSE.

INPUT PULSE TRAIN

RETRIGGERABLE MODE PULSE WIDTH (+TR MODE)

NON-RETRIGGERABLE MODE PULSE WIDTH (+TR MODE)

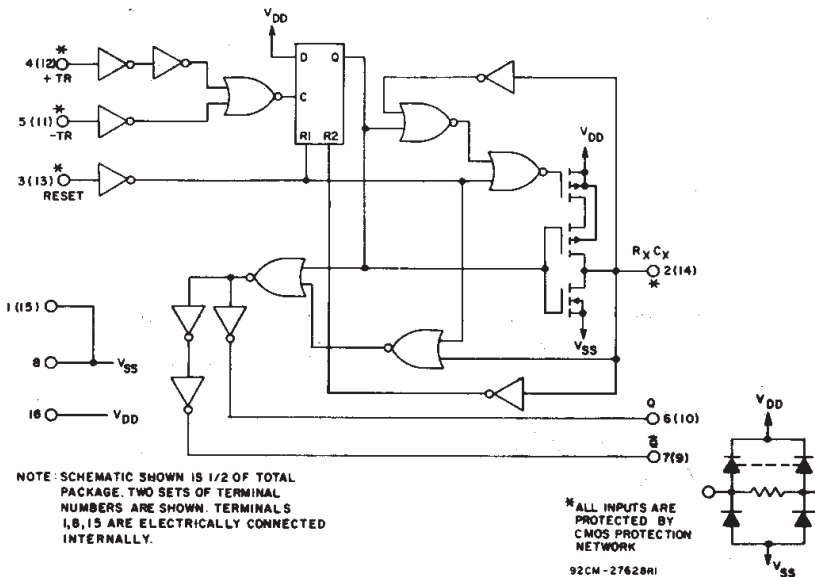


Fig. 4 — CD4098B logic diagram.

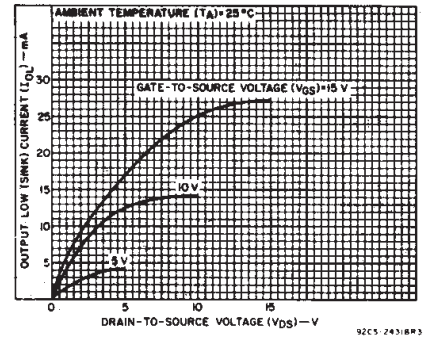


Fig. 1 — Typical output low (sink) current characteristics.

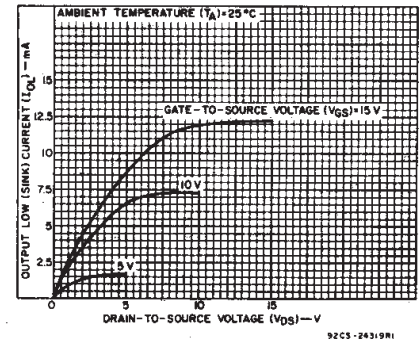


Fig. 2 — Minimum output low (sink) current characteristics.

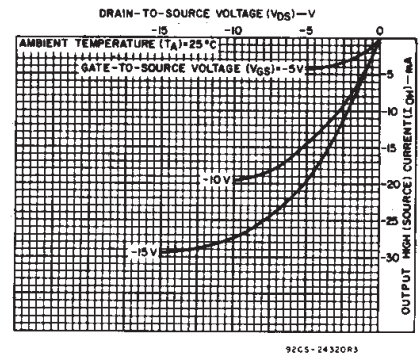


Fig. 3 — Typical output high (source) current characteristics.

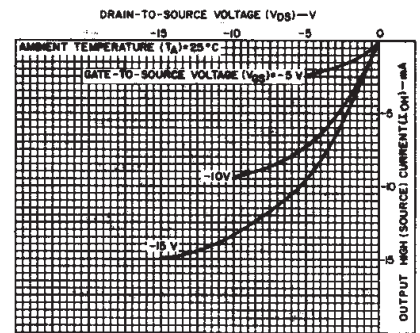


Fig. 5 — Minimum output high (source) current characteristics.

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COMMERCIAL CMOS
HIGH VOLTAGE ICs

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STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)	-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current I _{DD} Max.	—	0.5	5	1	1	30	30	—	0.02	1	μA
	—	0.10	10	2	2	60	60	—	0.02	2	
	—	0.15	15	4	4	120	120	—	0.02	4	
	—	0.20	20	20	20	600	600	—	0.04	20	
Output Low (Sink) Current, I _{OL} Min.	0.4	0.5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	0.5	0.10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0.15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current, I _{OH} Min.	4.6	0.5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	—	mA
	2.5	0.5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—	
	9.5	0.10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—	
	13.5	0.15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	—	
Output Voltage: Low-Level, V _{OL} Max.	—	0.5	5	0.05				—	0	0.05	V
	—	0.10	10	0.05				—	0	0.05	
	—	0.15	15	0.05				—	0	0.05	
Output Voltage: High-Level, V _{OH} Min.	—	0.5	5	4.95				4.95	5	—	V
	—	0.10	10	9.95				9.95	10	—	
	—	0.15	15	14.95				14.95	15	—	
Input Low Voltage, V _{IL} Max.	0.5,4.5	—	5	1.5				—	—	1.5	V
	1.9	—	10	3				—	—	3	
	1.5,13.5	—	15	4				—	—	4	
Input High Voltage, V _{IH} Min.	0.5,4.5	—	5	3.5				3.5	—	—	V
	1.9	—	10	7				7	—	—	
	1.5,13.5	—	15	11				11	—	—	
Input Current, I _{IN} Max.	—	0.18	18	±0.1	±0.1	±1	±1	—	±10 ⁻⁵	±0.1	μA

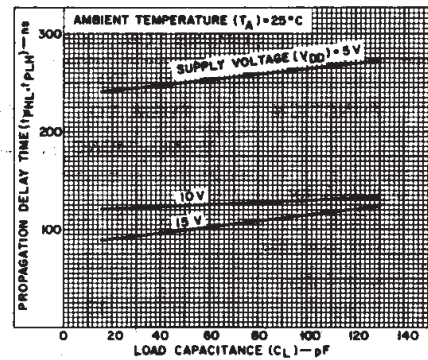


Fig. 6 – Typical propagation delay time vs. load capacitance, trigger into Q out. (All values of C_X and R_X .)

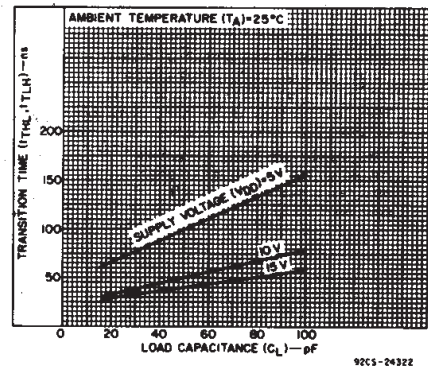


Fig. 7 – Transition time vs. load capacitance for $R_X = 5\text{ k}\Omega$ -10000 $\text{k}\Omega$ and $C_X = 15\text{ pF}$ -10000 pF .

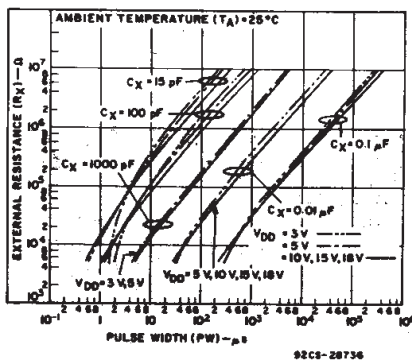


Fig. 8 – Typical external resistance vs. pulse width.

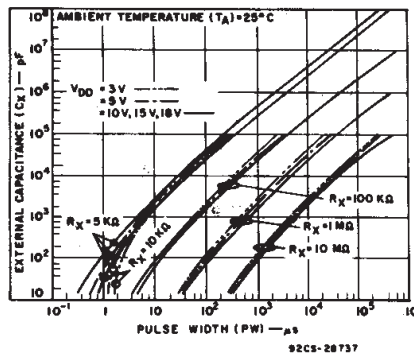


Fig. 9 – Typical external capacitance vs. pulse width.

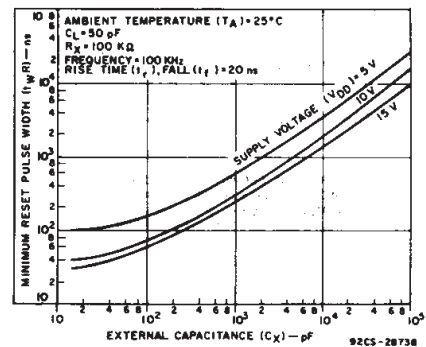


Fig. 10 – Typical minimum reset pulse width vs. external capacitance.

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DYNAMIC ELECTRICAL CHARACTERISTICS

At $T_A = 25^\circ\text{C}$; Input $t_r, t_f = 20\text{ ns}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$

CHARACTERISTIC	TEST CONDITIONS			LIMITS		UNITS
	R_X (k Ω)	C_X (pF)	V_{DD} (V)	Typ.	Max.	
Trigger Propagation Delay Time +TR, -TR to Q, $\bar{Q}$ t_{PHL} , t_{PLH}	5 to 10,000	≥ 15	5 10 15	250 125 100	500 250 200	ns
Minimum Trigger Pulse Width, t_{WH} , t_{WL}	5 to 10,000	≥ 15	5 10 15	70 30 20	140 60 40	ns
Transition Time, t_{TLH}	5 to 10,000	≥ 15	5 10 15	100 50 40	200 100 80	ns
t_{THL}	5 to 10,000	15 to 10,000	5 10 15	100 50 40	200 100 80	
	5 to 10,000	0.01 μF to 0.1 μF	5 10 15	150 75 65	300 150 130	
	5 to 10,000	0.1 μF to 1 μF	5 10 15	250 150 80	500 300 160	
Reset Propagation Delay Time, T_{PHL} , T_{PLH}	5 to 10,000	≥ 15	5 10 15	225 125 75	450 250 150	ns
Minimum Reset Pulse Width, t_{WR}	100	15	5 10 15	100 40 30	200 80 60	ns
			5 10 15	600 300 250	1200 600 500	
		0.1 μF	5 10 15	25 15 10	50 30 20	μs
			5 10 15	5 7.5 7.5	10 15 15	
Trigger Rise or Fall Time t_r (TR), t_f (TR)	—	—	5 to 15	—	100	μs
Pulse Width Match Between Circuits in Same Package	10	10,000	5 10 15	5 7.5 7.5	10 15 15	%
Input Capacitance, C_{IN}	Any Input			5	7.5	pF

TEST CIRCUITS

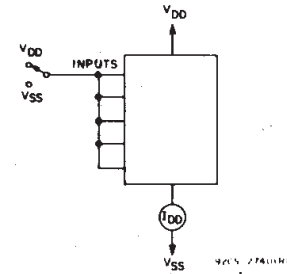


Fig. 12 - Quiescent-device-current test circuits.

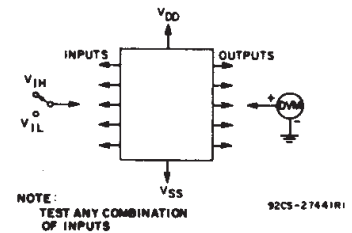


Fig. 13 - Input-voltage test circuit.

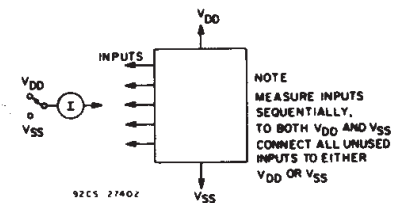


Fig. 14 - Input leakage current test circuit.

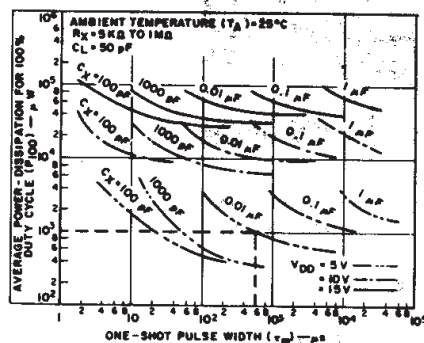
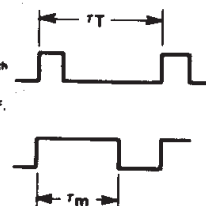


Fig. 11 - Average power dissipation vs. one-shot pulse width.

To calculate average power dissipation (P) for less than 100% duty cycle:
 P_{100} = average power for 100% duty cycle
 $P = \left(\frac{t_m}{T}\right) P_{100}$ where t_m = one-shot pulse width
 T = trigger pulse period
 e.g. For $t_m = 600\text{ }\mu\text{s}$, $T = 1000\text{ }\mu\text{s}$, $C_X = 0.01\text{ }\mu\text{F}$,
 $V_{DD} = 5\text{ V}$
 $P = \left(\frac{600}{1000}\right) 1000\text{ }\mu\text{W} = 600\text{ }\mu\text{W}$ (see dotted line on graph)



92CN-28739

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APPLICATIONS

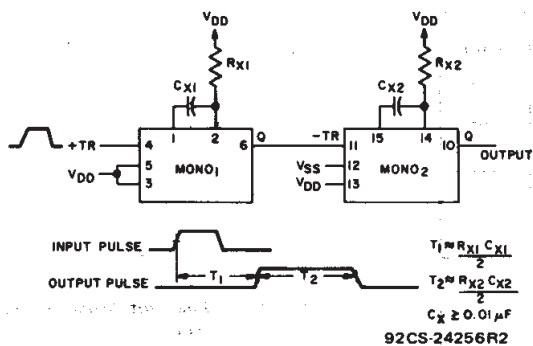


Fig. 15 – Pulse delay.

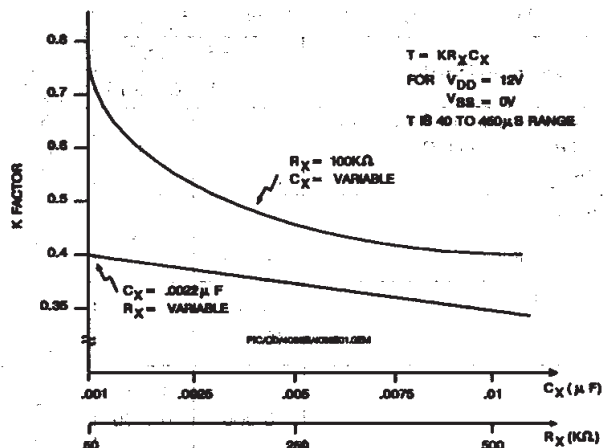


Fig. 17 – K-Factor for $V_{DD} = 12V$.

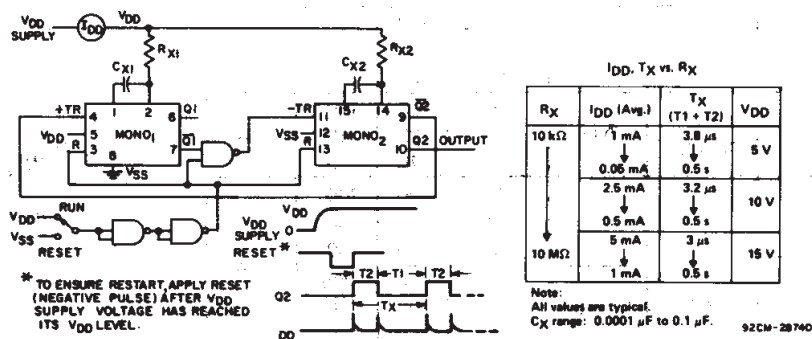
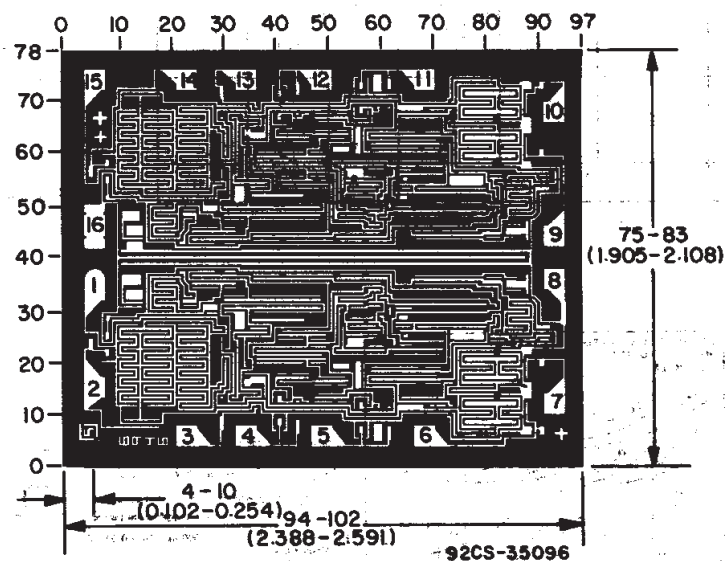


Fig. 16 – Astable multivibrator with restart after reset capability.



Dimensions and Pad Layout for CD4098BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD4098BE	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4098BE
CD4098BE.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4098BE
CD4098BEE4	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4098BE
CD4098BF	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4098BF
CD4098BF.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4098BF
CD4098BF3A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4098BF3A
CD4098BF3A.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4098BF3A
CD4098BM	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	CD4098BM
CD4098BM96	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4098BM
CD4098BM96.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4098BM
CD4098BM96G4	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4098BM
CD4098BMT	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	CD4098BM
CD4098BPW	Obsolete	Production	TSSOP (PW) 16	-	-	Call TI	Call TI	-55 to 125	CM098B
CD4098BPWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM098B
CD4098BPWR.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM098B
JM38510/17504BEA	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 17504BEA
JM38510/17504BEA.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 17504BEA
M38510/17504BEA	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 17504BEA

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF CD4098B, CD4098B-MIL :

- Catalog : [CD4098B](#)
- Military : [CD4098B-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4098BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4098BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4098BM96	SOIC	D	16	2500	353.0	353.0	32.0
CD4098BPWR	TSSOP	PW	16	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD4098BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4098BE.A	N	PDIP	16	25	506	13.97	11230	4.32
CD4098BEE4	N	PDIP	16	25	506	13.97	11230	4.32

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE

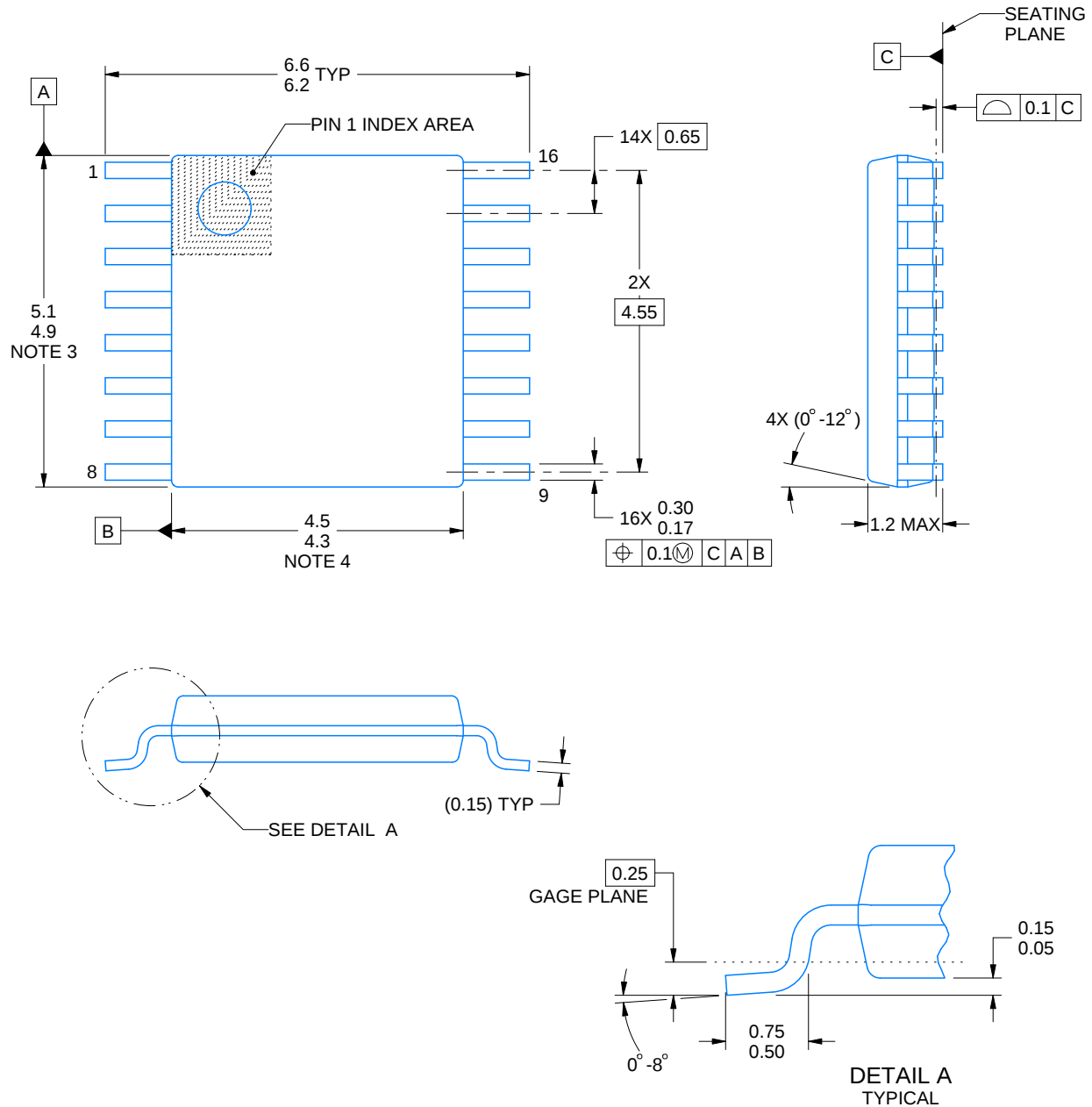
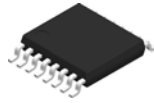


PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.



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NOTES:

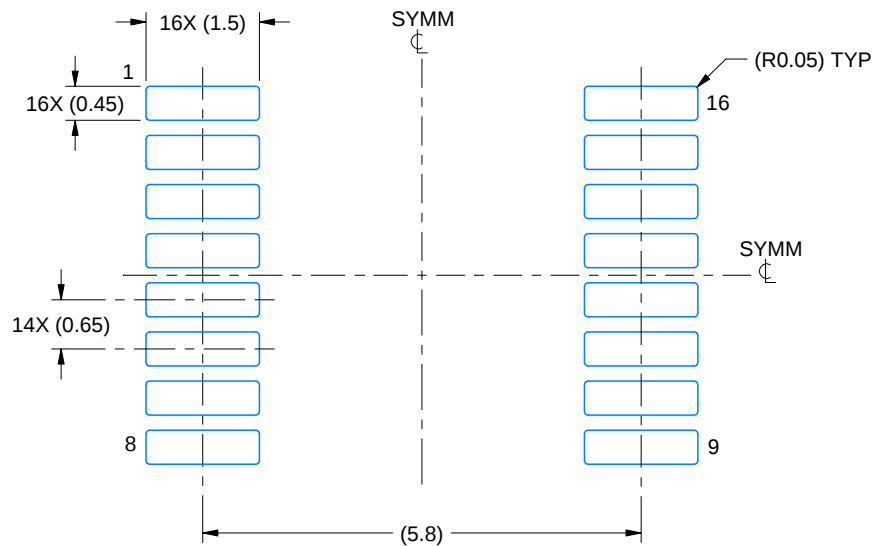
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

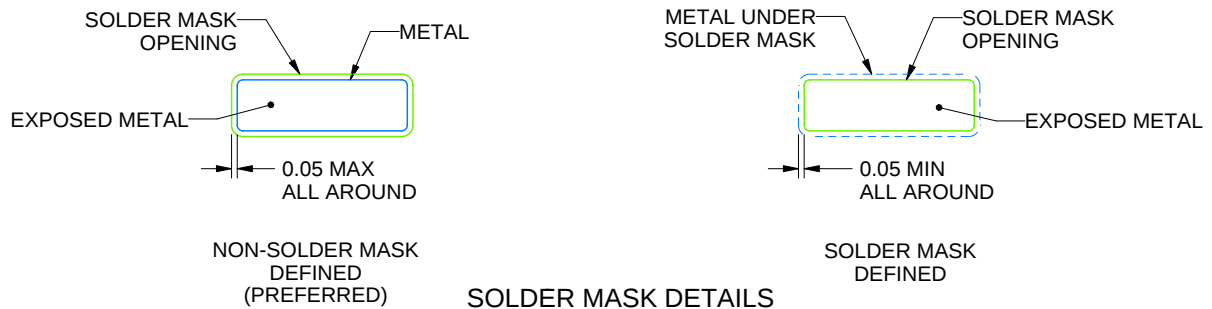
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

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